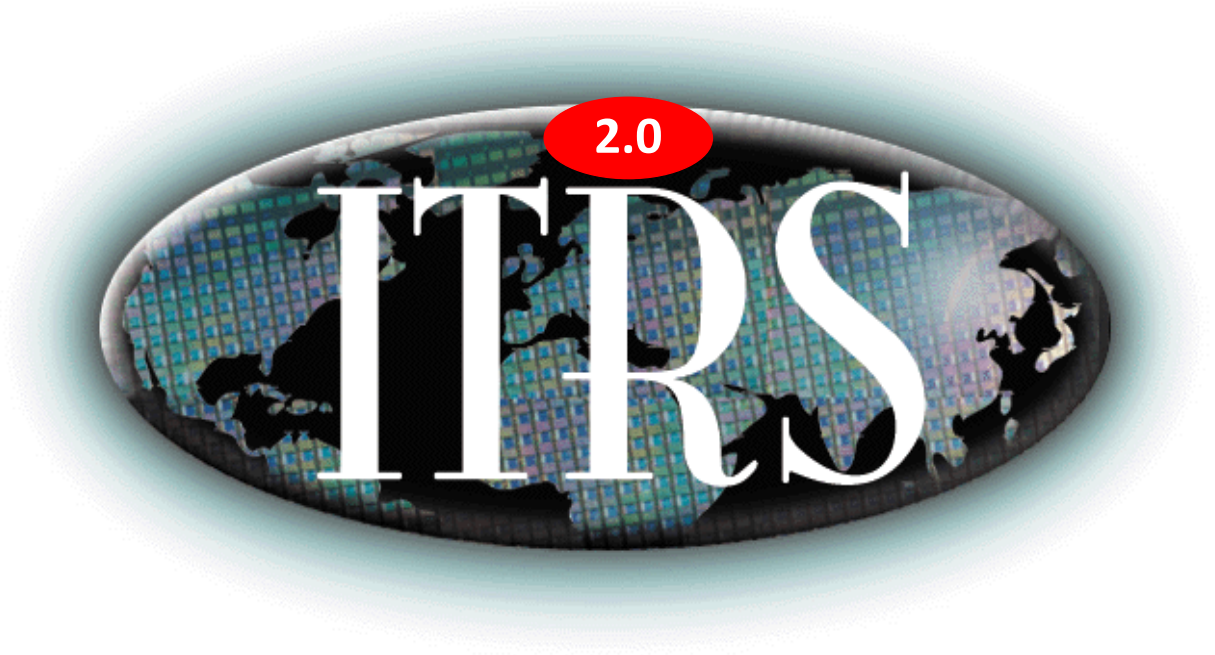

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2.0

2015 EDITION

LITHOGRAPHY

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Mission

The Lithography Technology Working Group's mission is to identify lithographic options that could enable future semiconductor nodes and better semiconductor products and to describe the driving forces for their implementation and the challenges to their implementation. We provide inputs to the More Moore team so that the More Moore roadmap incorporates lithographic capabilities and constraints.

Introduction

The overall 2015 roadmap shows a progression of new types of logic devices being introduced and many new types of memory devices as possible options in the future. This change in device structure drives what sort of patterning challenges will come in the future. In the past, flash memory and the fins in FinFET devices drove the industry to implement self-aligned quadruple patterning (SAQP). But in the future, planar flash memory will stop shrinking due to electrical reasons and fin structures will be replaced by gate all around structures and SAQP will continue to be usable to pattern these levels. Now it is the critical levels for DRAM and the metal levels for logic that will drive improved line and space patterning instead. And hole type patterns will continue to be a challenge. Tighter pitch metal levels drive tighter pitch vias, and new types of devices drive tighter pitch contacts. In addition, the projected introduction of vertical gate all around structures will drive patterning to produce even smaller hole type structures.

Lithographic patterning methods have critical dimension "cliffs" where a given patterning method can no longer be used to produce features with a half pitch below that value. For example, the theoretical limit for ArF immersion lithography is about 36nm half pitch, but if one actually imaged this pitch with ArF, the process window would be unacceptably low and it would be impossible to pattern any sort of two-dimensional feature, such as a line end or jog. So the practical limit of ArF immersion lithography for lines and spaces is about 40nm half pitch. The edge of a "cliff" is not one specific CD but is actually a small range of CDs, where the range depends on how much patterning process window is acceptable and how complex the desired pattern is. An example of this is seen in a published 22nm node logic chip design.[1] The smallest pitch metal layers in this design have a half pitch of 40nm, representing the line and space cliff for single exposure ArF immersion lithography; but the metal one level has a half pitch of 42nm, reflecting a more complicated design for this level to match the transistor structure just below it. Chip makers will tend to design layers on the larger side of cliffs where possible and to introduce layers at sizes below the current cliffs only when a new node is introduced and significant product improvement is gained. Printing smaller features than a cliff requires new tooling or a different process and almost always increases cost and/or process complexity.

Since patterning cliffs have importance in selecting patterning methods and designing chips, our possible options tables are structured around these cliffs. Roughly 40nm is the cliff for ArF immersion single exposure line and space patterning, so 20nm is the cliff for pattern doubling and 10nm is the cliff for pattern quadrupling using ArF immersion patterning. Since pattern doubling is in widespread manufacturing use and pattern quadrupling is already in use for layers

that can be quadrupled through self-aligned quadruple patterning (SAQP), this is our baseline process to compare possible new line and space patterning methods to.

Multiple patterning is also the baseline process for critical level hole type patterning. Hole type patterning is needed for contact, via and cut type levels. Double patterning of dense contact holes shrinks the pitch by approximately 30% and quadruple patterning shrinks the pitch by approximately 50%. This means that quadruple patterning of dense contact holes matches the shrink achieved with just double patterning of lines and spaces. So even though the designed pitches of the smallest hole type patterns in a chip design is larger than that of the smallest lines and spaces, already multiple patterning is in use for these levels, and the introduction of smaller pitch devices provides greater challenges for hole type patterns than for line and space type patterns. These types of patterns can be self-aligned, in the sense that the actual sides of a patterned contact hole are created by the features on either side of it rather than the dimension of the lithographically printed hole. In this case, the hole CD per se is not as critical as the edge placement error, or EPE, which is a combination of the effects of CD and overlay variations on the position of the outer edges of features.

Possible Options

Possible patterning options for different pitch ranges and their time frames for implementation are shown in figures 1 and 2, metal levels and for hole type patterns, respectively. The ranges in the left column reflect the litho "cliffs" described above. For Figure 1, the range down to 14nm half pitch is shown twice. The first instance shows that manufacturing processes for pitches in this range are already committed for 2017 using quadruple patterning (QP). The second instance relates to pitches in this range projected for production starting in 2019, where other patterning options are still possibilities.

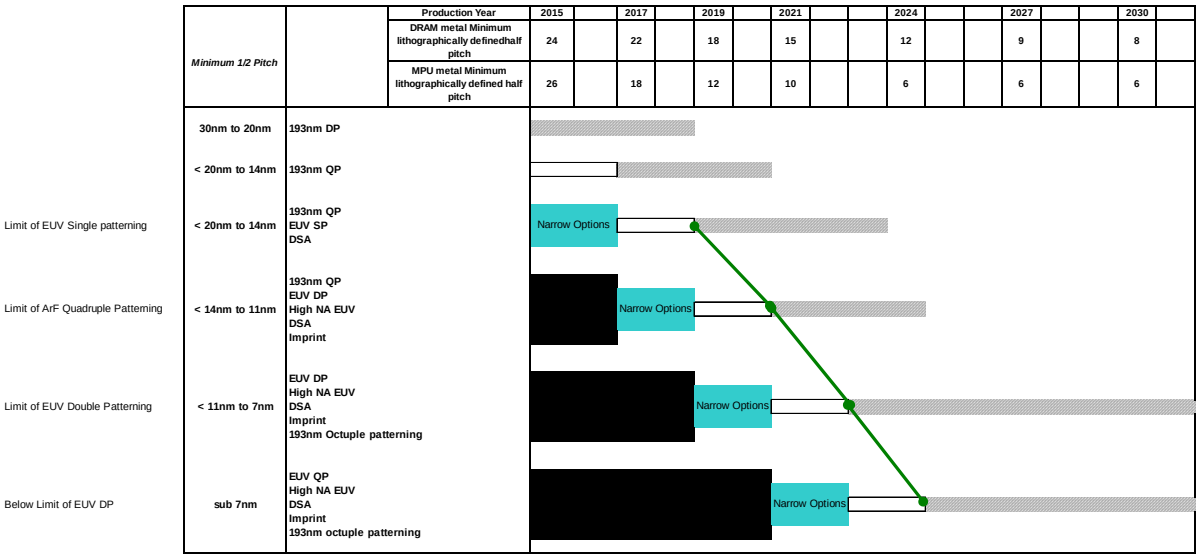

Figure 1: DRAM Critical and MPU Metal Level Potential Solutions

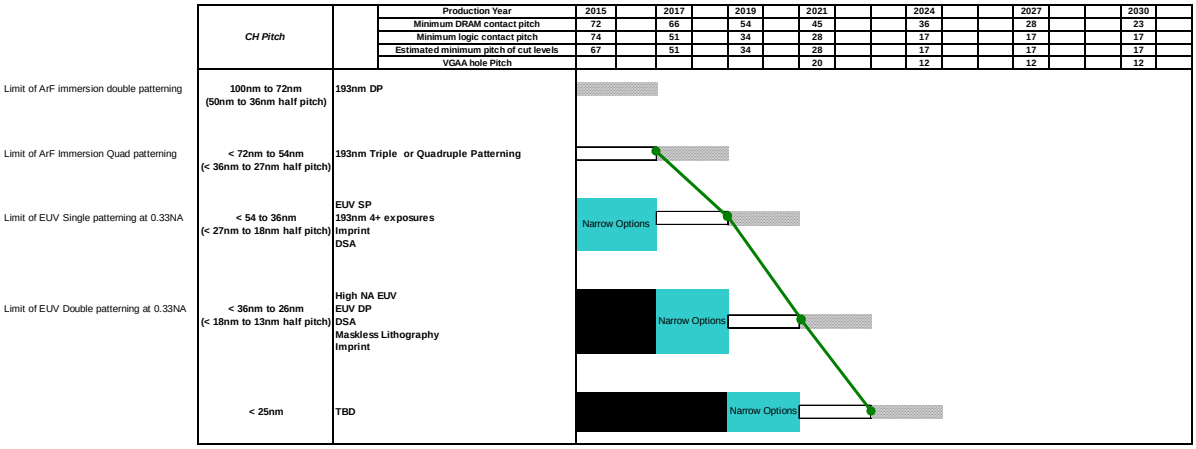

Figure 2: Hole Type Pattern Potential Solutions

For lines and spaces, quadruple patterning can be extended at least through 2018 and possible through 2022, depending on the complexity and tolerance control required of the projected 10nm half pitch metal levels projected for manufacturing in 2019 and 2021. The alternative technologies to multiple patterning shown in Figure 1 will have to show some substantial cost or design benefit over multiple pattering in order to be adopted before 2024.

For hole type patterns, quadruple patterning is also already in use. However, more than quadruple patterning is projected to be needed for early manufacturing production in 2019. The opportunity for implementing alternatives to multiple patterning is thus much sooner and more beneficial for the industry for hole type patterns than it is for line and space patterns.

Each possible alternative patterning option with current R&D for future devices is discussed in detail in the sections below

Multiple Patterning

Metal levels with a half pitch under 20nm using SAQP should start initial production lots some time in 2016 and will be accompanied by contact levels that require triple or quadruple patterning. Because quadruple patterning is already in use, our concern in this roadmap is whether multiple patterning will be extended beyond quadruple patterning, rather than can it work in manufacturing. Key challenges for extending multiple exposures lithography are cost, process complexity, and design issues, especially for random logic. The challenges relate more to managing the design and managing all the tolerance variations the many patterning steps entail, rather than in doing extra processing steps per se.

Specific challenges are somewhat dependent on the sort of multiple patterning being extended. One possible strategy for patterning metal levels is complementary lithography and SAQP, or complementary lithography and self-aligned octuple patterning. This strategy puts pressure on the patterning of cut levels that segment the lines into usable circuit elements. ArF lithography tools can be used for the cut levels, but many cut masks and printing steps are needed, leading to high cost and process complexity. The other strategy for patterning metal levels is to use a litho/etch, litho/etch type of multiple patterning processes. This enables more complicated designs, which are needed for some metal levels. In this case it is the additional lithography

steps for the lines themselves rather than the cuts that impose more cost and complexity to the process.

More than quadruple patterning will be needed in manufacturing for line and spaces patterns sometime between 2021 and 2024, depending on whether 10nm critical CDs can be quadruple patterned with adequate tolerance control or not. But more than quadruple patterning will be needed for hole type patterns as early at 2019. This suggests that hole type patterns are likely to be the first driver for the introduction of alternatives to multiple patterning.

Possible alternative technologies to multiple patterning with active development efforts underway are discussed individually below.

EUV Lithography

EUV is an exposure technique that uses light with a wavelength of 13.5nm and all reflective optics. The biggest issue with EUV has been source power. As of the 2013 ITRS roadmap, there was insufficient demonstrated source power to do much other than characterize the tools and some of the imaging. EUV exposure tools have made significant progress since that roadmap. Now customers are reported to have achieved throughputs of several hundred wafers a day over a period of several weeks. This wafer throughput is high enough to do chip process development work, but sufficient uptime is also needed. The current average availability of 55% to 60% reported by ASML, the tool manufacturer, is projected by them to improve to something over 70% in the beginning of 2016. Reaching this availability target and then improving throughput is the first key challenge for EUV. If the current power and availability roadmaps are met, production throughput capable tools are projected to be available in time for use in manufacturing the foundry "7nm" logic node production starting in 2018.

Other key challenges for EUV are defects and resist resolution, sensitivity and throughput. Defects relate both to mask defects and to particles generated during tool operation. EUV Pellicles are strongly desired to improve overall process defectivity. There is progress being reported on pellicles. Targeting hole type layers such as contacts and cut levels that have less bright area on the mask will make mask defects easier to manage. Per the possible options charts discussed above, this is the type of layer that requires patterning innovation the soonest; and thus is a likely first target for EUV use. Overall defectivity has to be demonstrated at close to manufacturing levels in 2016 for EUV to be committed for production in 2018.

EUV resist line edge roughness (LER), line width roughness (LWR) and contact hole critical dimension uniformity are also challenges. Reported resolution on a commercial scanner with commercial chemically amplified resist has reached 14nm half pitch with reasonable process windows, but the best reported results for LWR do not meet the numbers in the requirements table for litho, and the photo speed is worse than needed for scanners to reach their specified throughput.

Since lines and spaces produced with SADP and SAQP have very good roughness, EUV is unlikely to be used for levels that are suitable for these processes. Line and space patterns with a design that requires litho/etch-litho/etch type multiple patterning are more promising targets for EUV implementation. The most promising target for implementation is hole type levels that already requires multiple patterning using litho/etch type processes.

Progress has also been made on extendibility. ASML has stated that they will produce a 0.55NA EUV scanner that uses different magnification in the x and y directions and given an overall description of what such a tool would be like. We estimate the earliest they could have such a tool available would be 2020, suggesting it could be used in manufacturing in 2021. There has also been progress in novel metal based resists, which have the potential for imaging in thin films with adequate absorbance of EUV light.

Directed Self Assembly (DSA)

DSA is a chemical based process for creating patterns by using special polymers that separate into domains of different composition upon annealing. Lithographically printed guide features are used to direct the phase separation into producing useful patterns. Additional levels, such as "cut" levels are often used to trim the phase separated features after they form. DSA can be used for pitch multiplication, both of lines and spaces and of hole type patterns. DSA can also be used to "rectify" hole patterns. That is, larger holes can be made smaller and more uniform. Patterns with larger CDs require larger polymers and larger polymers are harder to anneal, so features that are relatively large are not suitable for DSA. Critical CDs for chips are just now reaching the range appropriate for DSA use. Guide structures appropriate for such CDs can be printed with ArF immersion scanners but could also be printed with other patterning methods.

DSA progress has clearly moved into a development phase at many Fabs. DSA materials are now available in gallon quantities from several vendors and there are enough publications to show that both memory and logic producers are working on DSA. The most likely first application of DSA is contact holes and/or cut levels, either for rectification or limited pitch multiplication. Limited pitch multiplication is using guide features to create pairs or other small numbers of contacts in close proximity to each other. For line/space pitch multiplication, DSA has to compete with SAQP and so far SAQP is reported to be superior in LER/LWR.[2] While the LER/LWR of DSA produced lines and spaces is not as good at that of SAQP, it is still considerably better that that of EUV. Contact hole CD uniformity is also considerably better than EUV. Assessments of these and other parameters are contained in an industry survey conducted by the ITRS and included in the tables accompanying this document.

The key challenges of DSA are pattern placement, defectivity and pattern inspection, and DSA compatible chip design and layout. Pattern placement is an issue for DSA features that are in between guide structures. Reported defectivity levels have improved in the past two year, but are not yet reported to be at manufacturing levels. Buried defects are a particular problem. With current DSA processes, it is desirable to do the defect inspection before etch. But there can be buried three dimensional defects in phase separation. These sorts of defects are a particular challenge to detect. Since DSA makes only very simple patterns so far, chip designs have to be remade to work with structures available by DSA and layout engines need to incorporate DSA related process windows in designing particular chips.

Nanoimprint

Nanoimprint is a technique in which three dimensional molds stamp a pattern into a liquid resist and the resist is cured into a solid pattern while still molded. Then the mold is peeled off and reused. Because it's a contact technique defectivity is a concern and because it has no

magnification factor (that is, the templates are 1X), making the templates is a challenge, especially at leading edge semiconductor dimensions. Flash memory, which is more defect tolerant than logic or DRAM, is the first target of nanoimprint. In 2015, new results were published indicating that throughput and overlay have improved significantly. Tools were announced that meet manufacturing throughput needs and are expected to be available for a possible first implementation in 2018. The overlay of these tools is coming close to the requirements for flash memory. Defectivity, template infrastructure and template inspection are still key challenges. These challenges depend significantly on the critical dimension of the pattern being printed. There is enough momentum in nanoimprint to make it possible to make a go/no-go decision for manufacturing sometime in 2016.

Maskless Lithography

Maskless lithography refers to the technique of direct writing circuit patterns in resist on a wafer using some sort of programmable writing tool. Maskless lithography tools currently under development use e beam lithography. Direct write is an intrinsically slow technique, and gets slower as scaled to smaller features. So current tool implementation under development uses tools that have multiple ebeams writing at once, either using multiple small ebeam columns or using one column and a specially designed chip that is a source of multiple ebeams, all of which go through the same column. The use of enough multiple beams at once is projected to give adequate throughput for chip writing. This technique is very appealing for low volume chip designs, where the costs of the masks can't be amortized over very many chips. These are typically logic chips. It is also potentially appealing for chip patterns that are very sparse in writing area, for example, hole type patterns such as contacts or cut levels, although the speed of writing such patterns will depend significantly on the tool architecture.

The principle of writing with multiple beams is well established and tool development for writing mask patterns with multiple beams is progressing well. But the mask tools still are expected to take many hours to write a mask. Writing wafers requires smaller features and faster throughput than the mask tools under development can come close to. Actually demonstrating a pilot type tool which integrates the writing of wafers with positional control of the images and some sort of throughput indicative of progress has not happened yet. So the key challenge for this technology is to actually build a working demo tool for writing whole wafers with chip like patterns and overlay control. Work is underway on this task, but the lack of recent published progress suggests that the earliest insertion point for such technology would be 2021 and the earliest insertion target would be the "5nm" logic node. Maskless lithography is shown in Figure 2 for this node because of the technique's potential for hole type patterns. The lack of relevant published performance targets for the tools under development makes it difficult to list maskless lithography as a possible option anywhere else in figures 1 or 2.

Summary

Table 1 shows a comparison of the key challenges of each of the possible patterning options discussed above, along with dates and product types for their earliest possible insertion.

Next Generation Technology	First Possible Use in Mfg.	Feature Type	Device Type	Key Challenges	Required Date for Decision making
Multiple Patterning Extension to >4X patterning	2020 to 2023	10nm or less hp metal for logic MPUs 10nm hp for LGAA structures	"5nm" node logic	-Extension to random logic -Printing and overlay of cut levels -Design to cost tradeoff	2018
EUV	2018	22 to 24nm hp CH/Cut Levels 18nm hp LS	"7nm" node logic 18nm DRAM	-Availability & Throughput -Mask Defects -Resist sensitivity and roughness -High NA field size	2016
NanoImprint	2017	14nm hp LS 20nm hp bit lines	2D Flash Memory 3D Flash Memory	-Defectivity -Overlay -Master Template writing and inspection <20nm -Template replication <20nm	2016
DSA (for pitch multiplication)	2018	Contact holes/cut levels	1x DRAM "7nm" node logic	-Pattern Placement -Defectivity and defect inspection -Design -3D Metrology	2016
Maskless Lithography (ML)	2021	Cut levels -- possibly 20nm on 40nm pitch (estimated)	"5nm" node logic (estimated)	-Concept demonstration -Functioning tool	2019

Table 1: Difficult Challenges

While the implementation dates for multiple patterning extension shown in the table above is later than the dates shown for new pattering technologies currently under development; that is because multiple patterning has already been demonstrated to support critical CDs needed earlier than 2021 to 2024. The alternative technologies can't just demonstrate patterning capability; they have to be better than multiple patterning for at least some levels to be selected for implementation. Each of the techniques contending with multiple patterning has its own strengths and weaknesses. They are shown in spider charts in Figure 3 below. Successful implementation of any of them requires improvement in some aspect of that technique. These strengths and weaknesses are relative to the current ITRS roadmap targets. These targets are harder than they were two years ago, so technologies can get worse compared to requirements despite making technological progress. Compared to 2013, EUV is closer to manufacturing readiness, but may have issues with resolution if there are further delays in implementation. Nanoimprint has improved its readiness significantly. DSA has improved its readiness slightly and maskless lithography has fallen farther behind requirements. We look forward to seeing progress in all these technologies during the next two years.

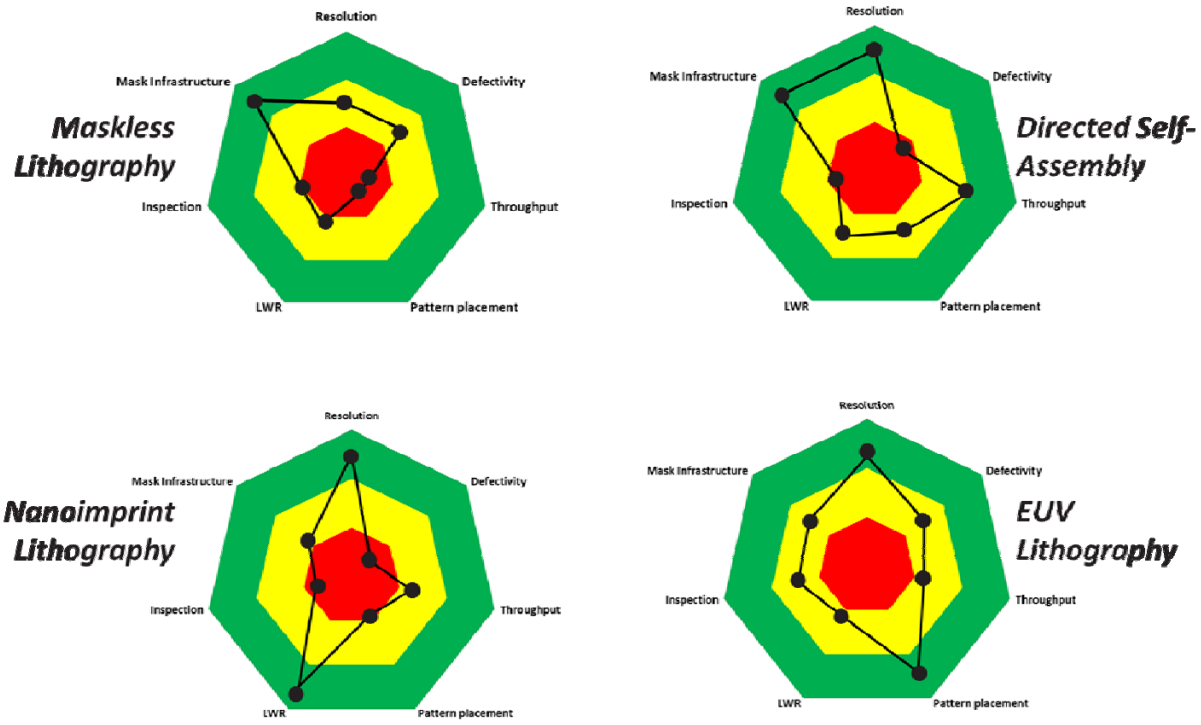

Figure 3: Radar charts comparing possible alternative to multiple patterning

Acknowledgements

This document and the associated set of Microsoft Excel tables was prepared by the ITRS Roadmap Lithography working group consisting of Tsukasa Azuma, Tatsuo Chijimatsu, Masayuki Endo, Ted Fedynyshyn, Heiko Feldmann, Emily Gallagher, Reiner Garreis, Cesar Garza, TS Gau, Frank Goodwin, Roel Gronheid, Naoya Hayashi, Franklin Kalk, Kunihiko Kasama, Insung Kim, Patrick Kearney, Sachiko Kobayashi, Toshio Konishi, Y.C. Ku, Keishiro Kurihara, David Kyser, Shy-Jay Lin, Dan Millward, Matt Malloy, Pawitter Mangat, Venkat Nagaswami, Hideo Nakashima, Patrick Naulleau, Mark Neisser, Yasushi Okubo, Katsumi Ohmori, Masahiko Okumura, Moshe Preil, Doug Resnick, Kazuhiro Takahashi, Hirofumi Takeda, Walt Trybula, Fumikatsu Uesawa, Mauro Vasconi, Geert Vandenberghe, Phil Ware, John Wiesner, Jim Wiley, Grant Willson, Obert Wood, Stefan Wurm, Tetsuo Yamaguchi, Jiro Yamamoto, John Zimmerman.

[1] C.-H. Jan et al., "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications", Electron Devices Meeting (IEDM), 2012 IEEE International

[2] D. Millward et al., "Graphoepitaxial and chemoepitaxial methods for creating line-space patterns at 33nm pitch: comparison to a HVM process", Proc. of SPIE Vol. 9423 (2015)