INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

ASSEMBLY AND PACKAGING

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ASSEMBLY AND PACKAGING

CHAPTER SCOPE

This chapter addresses the near-term Assembly and Packaging roadmap requirements and introduces many new requirements and potential solutions to meet market needs in the longer term. Assembly and Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input and voltage control. It also provides for thermal dissipation and the physical protection required for reliability.

Today Assembly and Packaging is a limiting factor in both cost and performance for electronic systems. This has resulted in acceleration of innovation. Design concepts, packaging architectures, materials, manufacturing processes and systems integration technologies are all changing rapidly. As traditional Moore's law scaling become more difficult, assembly and packaging innovation allowing scaling in the third dimension is taking up the slack.

This accelerated pace of innovation has resulted in development of several new technologies and expansion and acceleration of others introduced in prior years. Wireless and mixed signal devices, bio-chips, optoelectronics and MEMS have placed new requirements on packaging and assembly. The rapid adoption of these new elements in the expanding consumer electronics market has been a strong driver of innovations such as Systems in a Package (SIP), Wafer Level Packaging (WLP) and 3 Dimensional Packaging. New architectures include printable circuits, thinned wafers and both active and passive embedded devices are emerging as solutions to market requirements. The materials and equipment used in assembly and packaging are also changing rapidly to meet the requirements of these new architectures and the changing environmental regulatory requirements.

This Chapter is organized in five sections:

- Difficult Challenges
- Technology Requirements
- Infrastructure
- Potential Solutions
- Cross-Cut Issues

Wherever possible we have aligned the ITRS Assembly and Packaging chapter with other industry roadmap organizations including iNEMI, JISSO, and IPC.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test and reliability.

Many critical technology requirements are yet to be met and they are listed in Tables 93a and b below. Meeting these requirements will require significant investment in research and development. This investment is greater than current run rates and cannot be met through the current gross margin of the assembly and packaging suppliers. This gap in resources available and resources required may be the greatest of the Difficult Challenges.

Table 93a Assembly and Packaging Difficult Challenges—Near-term

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Impact of new materials	*BEOL materials including Cu/low κ* Direct wirebond and bump to Cu or improved barrier systems bondable pads Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system Improved fracture toughness of dielectric materials Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed Probing over copper/low κ Singulation technology for circuits incorporating ultra low κ dielectrics
Wafer Level Packaging	I/O pitch between 150 μm and 250 μm greater than 100 I/O Solder joint reliability Wafer thinning and handling technologies Compact ESD structures (this applies to other package types as well) TCE mismatch compensation for large die
Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Rapid turn around modeling and simulation Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) In package decoupling System level co-design EDA for "native" area array is required to meet the Roadmap projections Models for reliability prediction
Embedded Components	Low cost embedded passives: R, L, C Embedded active devices at both wafer and substrate level Wafer level embedded components
Thinned die packaging	Wafer/die handling for thin die Compatibility of different carrier materials (organics, silicon, ceramics, glass, laminate core) Reliability Testability Thin die for embedded active devices Electrical and optical interface integration
Close gap between chip and substrate – Improved Organic Substrates	Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Increased via density in substrate core Alternative plating finish to improve reliability Tg compatible with Pb free solder processing (including rework @260C)
High Current Density Packages	Electromigration Thermal/mechanical reliability modeling. Whisker growth Thermal dissipation
Flexible System Packaging	Conformal low cost organic substrates Small and thin die assembly Handling in low cost operation

Difficult Challenges ≥ 32 nm	*Summary of Issues*
3D Packaging	Thermal management Co-Design and simulation tools Wafer to wafer bonding Through wafer Via structure and via fill process Bumpless interconnect architecture
Fine Pitch Packages	Tighter tolerances for fine pitch BGA Minimizing kerf loss in singulation for small outline packages High temperature warpage for fine pitch BGA Reliability to meet drop test requirements for mobile electronics

Table 93b Assembly and Packaging Difficult Challenges—Long-term

Difficult Challenges <32 nm	*Summary of Issues*
Package Cost does not follow the Die Cost Reduction Curve	Margin in packaging is inadequate to support investment required to reduce cost Increased device complexity requires higher cost packaging solutions
Small Die with High Pad Count and/or High Power Density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: Improved current density capabilities Higher operating temperature
High Frequency Die	Substrate wiring density to support >20 lines/mm Lower loss dielectrics—skin effect above 10 GHz "Hot spot" thermal management
System-level Design Capabilityfor Integrated Chips, Passives, and Substrates	Partitioning of system designs and manufacturing across numerous companies will make optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Embedded passives may be integrated into the "bumps" as well as substrates.
Emerging Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	Organic device packaging requirements not yet define (will chips grow their own packages) Biological packaging will require new interface types

There are signs that the technical community is responding:

- University research in packaging is increasing around the world
- Chemical companies have increased their investment in the new materials required to meet the future needs across a broad front from low κ materials and high κ materials to new polymers for integrated passive components.
- Venture capital investment in packaging and interconnect technology is increasing after several years of absence
- Equipment companies are investing in new capability to meet the needs of emerging requirements for making and handling thinned wafers, thinned die and both wafer level and 3D packaging
- Government and Private research institutes are increasing their investment in this area:
  - Fraunhofer Institute, IMEC, LETI, IME and ITRI are prime examples
- Independent device manufacturers are investing in new packaging technology to meet the requirements of their products
- Consumer product companies are driving innovation in SiP and other new system integration architectures

Even with this increased investment the current level is inadequate to meet the Difficult Challenges within the Roadmap time frame. The acceleration of this investment and the efficient coordination of development among these groups will be necessary to achieve the scheduled Roadmap milestones for assembly and packaging. One of the major objectives of this chapter is to encourage and facilitate the coordination and focus of these efforts on the Difficult Challenges.

TECHNOLOGY REQUIREMENTS

Assembly and packaging technology requirements are being driven as much by the rapidly changing market requirements as by the advancing silicon technology generations. New package types are evolving in response to the demand for smaller, thinner and lighter electronic products for the rapidly expanding consumer market. Wafer Level Packaging (WLP) and System in Package (SiP) are two new packaging categories requiring implementation of new complex manufacturing technologies and significant infrastructure investments. Wafer Level Packaging, where the packaging functions are achieved through wafer level processing, holds the promise of lower cost and improved performance for single die packages. System in package, where system integration is achieved in die packaging, enables the smaller size, lower cost, higher performance and shorter time to market demanded for consumer electronics. These two package types represent paradigm shifts whose further advancements will in turn deliver technology to meet both the demands of future market applications and advancing semiconductor technology generations.

Optoelectronics, RF and Mixed Signal, MEMS devices and medical and biotechnology devices will require specialized packaging to serve new market applications. Their advancements will demand continued innovation in packaging technology.

Continuously decreasing cost per function remains key to growth of the electronics market. Packaging cost has not been scaling with IC manufacturing cost and even the limited cost-per-pin decreases have been flattening out. At the same time, new devices require increased package pin count. New technologies will be required to deliver increasing performance and higher pin count at lower cost. In addition, technical innovation is required to enable trade-offs among form, function, performance and time to market in today's consumer driven market. Wafer level packaging and System in package are two examples of the paradigm shifts that ultimately will achieve the low cost/high performance objectives of the industry.

New package reliability issues arise in the assembly and package of Cu low κ dielectric devices and other new materials and structures. With the introduction of these and other new package and device types there is much research needed in the reliability physics, related materials science and the physical environments where these products are being used. These technologies will be required if we are to meet the demand for increased reliability.

SINGLE CHIP PACKAGES

Moore's law scaling in IC manufacture has enabled rapid increase in performance and decrease in cost. This poses extreme challenges for assembly and packaging processes which do not have the same scaling advantages to reduce cost and improve performance. Incremental improvements in traditional assembly technologies will not be sufficient to meet market requirements. The technical requirements for single chip packages are summarized in Tables 94a and b.

Table 94a Single-chip Packages Technology Requirements—Near-term Years

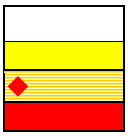
Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)									
Low-cost, hand held and memory	.27–.50	.26–.49	.25–.48	.24–.47	.23–.46	.22–.45	.21–.43	.20–.42	.20–.41
Cost-performance	.68–1.17	66–1.11	.64–1.05	.63–1.00	.62–.96	0.61–.94	.60–.92	0.58–.90	0.57–.89
High-performance	1.78	1.74	1.71	1.68	1.64	1.61	1.58	1.55	1.51
Harsh	0.29–2.61	0.26–2.34	0.25–2.11	0.23–2.00	0.22–1.90	0.22–1.54	.21-1.46	0.20–1.38	0.20–1.31
Chip Size (mm^2) [3] JISSO and ITRS not aligned									
Low-cost	100	100	100	100	100	100	100	100	100
Cost-performance	140	140	140	140	140	140	140	140	140
High-performance	600	630	662	695	729	766	804	750	750
Harsh	100	100	100	100	100	100	100	100	100
Maximum Power ($Watts/mm^2$) [4]									
Low-cost (Watts) [1]	2.80	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00
Cost-performance	0.65	0.70	0.74	0.79	0.83	0.85	0.85	0.89	0.98
High-performance	0.54	0.58	0.61	0.64	0.64	0.64	0.64	0.64	0.64
Harsh	0.16	0.18	0.18	0.20	0.20	0.22	0.22	0.24	0.25
Core Voltage (Volts)									
Low-cost	1	0.9	0.9	0.8	0.8	0.6	0.6	0.6	0.5
Hand-held	0.9	0.8	0.7	0.6	0.6	0.5	0.5	0.5	0.4
Cost-performance	1	0.9	0.9	0.8	0.8	0.6	0.6	0.6	0.6
High-performance	1	0.9	0.9	0.8	0.8	0.6	0.6	0.6	0.6
Harsh	1.2	1.2	1.2	1.2	1.2	1.2	1	1	0.9
Package Pincount Maximum [5][6] Not aligned with JISSO									
Low-cost	134–550	140–578	148–606	150–636	160–668	170–700	180–738	188–774	198–812
Cost-performance	550–900	550–990	600–1088	600–1198	660–1318	660–1450	720–1596	720–1754	800–1930
High performance	3000	3180	3371	3573	3787	4015	4256	4511	4736
Harsh	350	368	386	405	425	447	469	492	517
Minimum Overall Package Profile (mm)									
Low-cost	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
Cost-performance	0.80	0.80	0.80	0.65	0.65	0.65	0.65	0.50	0.50
High-performance	1.4	1.4	1.4	1.4	1.4	1.2	1.2	1	1
Harsh	0.80	0.80	0.80	0.80	0.80	0.80	0.80	0.70	0.70
Performance: Chip-to-Board for Peripheral Buses (MHz) [7]									
Logic/memory	100/400	100/533	100/667	100/800	100/800	125/800	125/800	125/1000	125/1000
Cost-performance (for multi-drop nets)	533	667	733	800	800	800	800	1000	1000
High-performance (for differential-pair point-to-point nets)	3125	3906	4883	6103	7629	9536	11920	14900	18625
Harsh	88	96	106	106	115	125	125	125	125
Maximum Junction Temperature									
Low-cost	125	125	125	125	125	125	125	125	125
Cost-performance	100	100	95	95	90	90	90	90	90
High-performance	100	100	95	95	90	90	90	90	90
Harsh	175	175	175	175	200	220	220	220	220
Operating Temperature Extreme: Ambient (°C)									
Low-cost (use case/purchase specification)	55/85	55/85	55/85	55/85	55/85	55/85	55/85	55/85	55/85
Cost-performance (MPU/Commercial)	45/70	45/70	45/70	45/70	45/70	45/70	45/70	45/70	45/70
High-performance	55	55	55	55	55	55	55	55	55
Harsh	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 200	-40 to 200	-40 to 200	-40 to 200

Table 94b Single-chip Packages Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)							
Low-cost, hand held and memory	.20–.39	.19–.38	.19–.37	.18–.36	.18–.35	.18–.34	.17–.34
Cost-performance	0.56–.87	0.55–.85	0.54–.83	0.53–.81	0.52–.80	0.51–.79	0.50–.79
High-performance	1.48	1.45	1.43	1.40	1.37	1.35	1.32
Harsh	.20–1.24	.19–1.17	.19–1.12	.18–1.06	0.18–1.00	.18–.94	.17–.89
Chip Size (mm^2) [3] JISSO and ITRS not aligned							
Low-cost	100	100	100	100	100	100	100
Cost-performance	140	140	140	140	140	140	140
High-performance	750	750	750	750	750	750	750
Harsh	100	100	100	100	100	100	100
Maximum Power ($Watts/mm^2$) [4]							
Low-cost (Watts) [1]	3.00	3.00	3.00	3.00	3.00	3.00	3.00
Cost-performance	0.98	0.98	1.08	1.08	1.08	1.12	1.12
High-performance	0.64	0.64	0.64	0.64	0.64	0.64	0.64
Harsh	0.25	0.27	0.28	0.28	0.29	0.29	0.3
Core Voltage (Volts)							
Low-cost	0.5	0.4	0.4	0.4	0.4	0.40	0.4
Hand-held	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Cost-performance	0.5	0.5	0.5	0.5	0.5	0.5	0.5
High-performance	0.6	0.5	0.5	0.5	0.5	0.5	0.5
Harsh	0.8	0.7	0.7	0.7	0.7	0.7	0.7
Package Pincount Maximum [5][6] Not aligned with JISSO							
Low-cost	208–850	218–896	230–940	240–988	250–1036	266–1088	278–1142
Cost-performance	800–2124	880–2336	880–2568	960–2824	960–3108	1050–3418	1050–3760
High performance	4973	5222	5483	5757	6045	6347	6665
Harsh	543	570	599	629	660	693	728
Minimum Overall Package Profile (mm)							
Low-cost	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Cost-performance	0.50	0.50	0.50	0.50	0.50	0.50	0.50
High-performance	1	1	1	1	1	1	1
Harsh	0.60	0.60	0.50	0.50	0.50	0.40	0.4
Performance: Chip-to-Board for Peripheral Buses (MHz) [7]							
Logic/memory	125/1000	125/1000	150/1200	150/1200	150/1200	150/1200	150/1200
Cost-performance (for multi-drop nets)	1000	1000	1200	1200	1200	1200	1200
High-performance (for differential-pair point-to-point nets)	23282	29102	36378	45472	56840	71051	88813
Harsh	125	150	150	150	150	150	150
Maximum Junction Temperature							
Low-cost	125	125	125	125	125	125	125
Cost-performance	90	90	90	90	90	90	90
High-performance	90	90	90	90	90	90	90
Harsh	220	220	220	220	220	220	220
Operating Temperature Extreme: Ambient (°C)							
Low-cost (use case/purchase specification)	55/85	55/85	55/85	55/85	55/85	55/85	55/85
Cost-performance (MPU/Commercial)	45/70	45/70	45/70	45/70	45/70	45/70	45/70
High-performance	55	55	55	55	55	55	55
Harsh	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200	-40 to 200

Notes for Table 94a and b:
Several entries are not aligned with JISSO
Chip size is below actual devices shipping today
Maximum chip power density will not occur in the largest die
Power density numbers are average per die. Within the die there may be hot spots with substantially higher local power density
Range in pin count for low cost and cost performance is due to different device types and package technologies employed
The chip size for cost performance is driven by microprocessors and high performance is driven by FPGA and ASIC devices

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Today wire bonding on 65 nm technology and 45 nm low κ devices is under development. In addition the impact of the mold compounds on silicon technologies using Cu/low κ material is not yet well understood. New approaches are required which are described in the materials section of this chapter.

The largest die today is 26 mm × 23 mm and current approaches cannot achieve this for 32 nm. The die size limit is the largest that can be manufactured with sustainable yields. This places practical limitations on die size that are less than maximum exposure equipment capability in most cases. Multi-die package technologies may be a more economical alternative to ever larger die with increasing numbers of transistors. The average die sizes, however, are likely to increase slowly as the process yields improve making larger devices economically advantageous. The likelihood of any drastic increase in die size in the near term is remote for reasons of economics due to yield considerations and time required to develop new technologies.

Packages to accommodate those larger die face challenges of increasing I/O and power requirements. The substrate dominates the cost of single chip packaging and the routing complexity of high I/O channel count with required power and ground support may further increase the cost. The substrate technology to accommodate finer lines and spaces, finer via pad geometries, finer via sizes and increasing layer counts will inevitably drive cost higher. Higher frequencies require improved signal integrity to minimize noise further increasing pressure on substrate wireability and therefore on cost.

HIGH PIN-COUNT PACKAGES

Since the introduction of the BGA in the early ‘90s, area array packages have enabled system designers to take advantage (cost effectively) of denser I/O interconnect schemes and package technology supporting thousands of I/O. The increase in I/O count continues with no end in sight.

There has been a dramatic increase in the need for high I/O count. Package pin count has grown even more rapidly as the higher frequency and higher power density demand more power and ground pins to meet signal integrity requirements. To meet the interconnect challenge, package substrate technology has introduced micro-via’s, blind and buried via’s, stacked via’s and tighter lines and spacing. Although substrate design rules have advanced to enable high density, several barriers had to be overcome. These include significant cost increases for design and test and a reduced supplier base.

Another issue with increasing I/O count packages is the routing complexity of the host PCB. As I/O speeds go deeper into the GHz spectrum, routing schemes for serial and parallel busses become very complex. This in itself has created, pro-longed design cycles with verification times increasing and system de-bug even more arduous. The introduction of SerDes technology is a step the industry is taking to reduce buss parallelism, thus reducing the number of interconnects between IC’s. Even single-ended parallel bussing to memory die is moving towards SerDes design with the introduction of Fully Buffered DIMM.

Design for signal integrity has lead to the requirement of improving the power sub-system in the package to the board. This has resulted in increasing the number of Vdd and Vss per signal I/O. Tightening I/O:Vdd:Vss ratios have resulted in increasing package pin counts and continue to increase with higher performance I/O technologies.

System-in-Package will become increasingly important to reduce the need for high density interconnects in the package substrate and PCB.

WAFER LEVEL PACKAGING

Wafer Level Packaging (WLP) is a technology in which all of the IC packaging is performed at the wafer level. A WLP technology requires all package interconnects to be continuously located within the chip outline (fan-in design) producing a true chip size package. From a systems perspective, the limitation on WLP is how many I/O can be placed under the chip and still have a board design that can be routed. Although the basic infrastructure has been available for several years the technology was not adopted since existing packaging solutions met market requirements.

WLP can provide a solution when requirements for continued decrease in size, increase in IC operating frequency and demand for cost reduction are not met by traditional packaging.. The advantages of WLP technologies include lower cost, improved performance, decreased power, shorter time to market and smaller size. WLP technologies are discussed in more detail in the potential solutions section.

SYSTEM IN A PACKAGE (MULTI-CHIP PACKAGES, 3D PACKAGING)

The reduction in size, weight, cost and power demanded by the consumer electronics market cannot be met without technical innovation. System in a package enables significant improvement in all these parameters.

Today the market is demanding shorter product life cycles while product complexity is increasing. System on a chip (SoC) solutions can address the size weight and power requirements but at the expense of increased cost per function and time to market as illustrated in Figure 90. The integration of highly complex systems must be carried out cost efficiently, with a high degree of miniaturization and flexibility. New integration techniques such as 3D integration packaging are become more important for SiP solutions. The SiP technology also allows incorporation of other circuit elements such as MEMS, optoelectronics and bio-electronics into the package reducing system cost and improving performance.

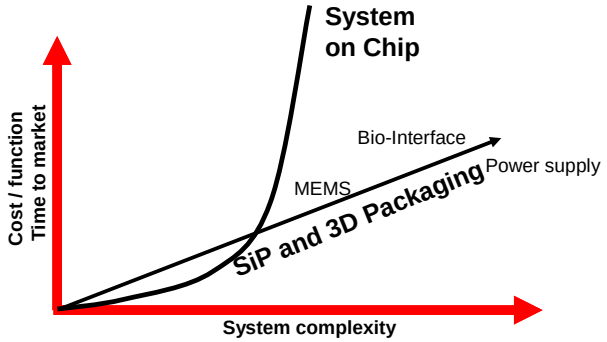


Figure 90 SoC and SiP Comparison for Cost per Function and Time to Market vs. Complexity

The key elements of SiP technology are:

- system partitioning/modularization
- chip-package co-design (on-chip, off-chip)
- integration of different functions in one package
- application of "add on" technologies to increase system functionality
- high dense component integration
- Known Good Die
- Test and reliability
- short time to market cycles
- low cost

FLEXIBLE SUBSTRATES AND INTERCONNECT

In many emerging applications electronic products must be flexible. An electronic product may be folded and twisted so it can fit into a very limited confined space or through its normal use such as for thin "smart cards". Flexibility is also important for some medical applications. For example, a hearing aid should be almost invisible and conform to the shape of each individual's ear. Telemedicine or patient monitoring applications can be enabled with transponders placed either

on or embedded in clothing. As cost continues to decrease, consumers will want electronic products integrated into their garments requiring compatibility with washing cycles in hot water with detergent, hot-air dryers and the heat and pressure of ironing.

ICs and passives devices may be surface-mounted on a flexible interconnecting substrate or integrated as thin film structures into flexible wiring layers. In some applications, these wiring layers must be stretchable. Die thinned to below 20 microns and embedded inside the wiring layers may use compliant bumping techniques for interconnect and thin molding for protection from the environment. Metal-coated polymer fibers may be deployed as conductive wires using a garment as the supporting substrate. A relatively large and flexible antenna could also be embroidered in a garment for patient monitoring or other RFID applications.

Flexibility of interconnect components such as microsprings and compliant bump structures will also be necessary to meet the requirements of future multi-chip packages. SiP with die and other components of varying thickness integrated into a dense package will require compliant structures to compensate for thickness variation and lack of coplanarity

OPTOELECTRONIC PACKAGING

For optoelectronic communication applications, a package is to provide the housing for components to implement the required functions and the interfacing ports to other functions in the overall system. The components are the light emitting device, the photo-detector, optical amplifier, the modulator, the driver IC, optical lenses, beam deflector … etc. The interfacing ports could be an optical window, an optical fiber, or an RF connector. For high data rate lasers, a thermoelectric cooler may also be needed in the housing.

In general, hermetic sealing is often necessary to protect the optical devices. TO header and butterfly packaging serve these needs. Alternative protection techniques for the less expensive, non-hermetically sealed organic packaging are required, especially for the extremely cost sensitive access network applications.

For high data rate communications using single mode fiber, the less than 0.5 μm tight alignment between single mode fiber and the optical device is an expensive requirement. For the cost sensitive access network applications, it is necessary to relax the alignment requirement, using the relative large diameter polymer optical fiber (POF) and automatic assembly to achieve 5 to 10 μm alignment accuracy. Note that adhesive is needed to assure the above alignment be maintained throughout the succeeding high temperature processes and product usage life. POF material improvement in attenuation reduction and data rate increase is required. Material development for poly-clad-silica (PCS) fiber must also be pursued.

For further cost reduction and performance improvement, vertical integration to include more functionality in a package is needed. For example, one may use wafer-level-packaging (WLP) process to integrate lenses or other micro-optical-electro-mechanical system (MOEMS) devices, and to provide environmental protection for a VCSEL wafer.

Some micro-optical components, e.g. polymer waveguides and beam reflectors, may be embedded in the SiP substrate. A BGA based SiP may house optical connectors, laser diodes, photodetectors, CMOS IC containing receivers/drivers and multiplexer/demultiplexer, plus RF connectors, and decoupling capacitors.

Digital Image sensors are being introduced in a wide range of consumer and industrial products including optical mouse, mobile phone, digital camera, PC, camcorder, scanners, security camera, etc. The high end applications are served by CCD image sensor devices, while the medium and low end applications are served by CMOS image sensor devices. Most image sensor dies are packaged in cavity packages with glass lids. For the high end applications, ceramic packages with hermetic sealing are preferred. For medium and low end packages plastic packages are preferred for lower cost. Optically clear molding compound or clear glob tops may be used for optical windows to save cost for the low end image sensors and communications components. Wafer level packaging approaches are becoming more prevalent due to its small form factor, low height, and low cost manufacturing potential. In this wafer level process the silicon wafer is sandwiched between two glass panels. The requirements are for combining image sensor device with other devices in the form of system in packages as subsystem module components.

RF PACKAGING

Many of the technology challenges for RF packaging arise from the fact that the IC packaging engineering practice, technology knowledge base, and manufacturing infrastructures have been based upon digital IC packaging developed in the last forty odd years. In RF packaging, the package is part of the RF circuit, and the packaging requirements for RF devices and for digital devices are not the same. The circuit performance is strongly influenced by the interaction of the

electromagnetic field with all the adjacent conductors and insulators. While they all require passive components, their characteristic parameters lie in different ranges. With the market demand for cell phones and other consumer oriented wireless portable products, the drive towards RF package integration with passive components, and for system in package with ASICs, memory devices and RF devices in the same package, further add to the breadth and complexity in RF packaging technology requirements.

RF technologies encompasses a broad range of market applications such as cellular phones, GPS, 3G cellular phones, WLAN, UWB, Direct Broadcast Satellite, mm Wave communications, vehicle anti-collision system, ranging from just below 1 GHz to approaching 100 GHz.

Plastic wirebond-leadframe molded packages are the low cost workhorse for low pin count devices in the industry. At the same time inductance characteristics associated with bonding wires and leaded packages, and effect of molding compound materials limit the RF performance. With the shorter interconnection paths in array packages with flip chip interconnect and WLP some of these problems can be reduced. It is important to provide RF package modeling tools and well as materials properties database for package design and device-package co-design for the broad spectrum of RF market applications. Corresponding improvements in materials properties—molding compounds, underfills, substrates—would be required.

Materials and process advancements such as in low temperature co-fired ceramic (LTCC), originally developed for military applications, have exhibited relatively low loss and shrinkage have a potential to further improve built embedded passive components. Progress in process science understanding, cost and manufacturability would be required for implementation in the higher frequency range market applications. To meet the low cost challenges, embedded inductance and capacitance components and networks in organic packaging for RF applications must be diligently pursued. One particularly challenging RF product family is RFID applications which require extremely low package cost, integration of antenna functions and the ability to protect the device in harsh environments.

SiP advancements provide great opportunities for placing RF and digital devices in a common package platform. The rich and diverse SIP technologies and manufacturing infrastructure—die and package stacking approaches such as PiP and POP as well as various embedded passive integration, will be applicable for RF applications. Particularly important will be the direction for reduction in size and weight of the SIP packages while increasing package complexity. It will be critical that RF physical design and modeling and simulations capabilities, and materials advances, mentioned previously for single chip package, be fully extended into the SIP arena where both RF and digital components share the common package platform. Tools to enable device package co-design in SIP packages will be very important.

In a SiP, RF ICs are modeled as multi-port S-parameter networks, which integrate well with the 2D and 3D frequency domain modeling for the SiP substrate having embedded passives. However, the digital ICs are represented as IBIS models, requiring time-domain signals in their inputs, and generating time-domain signals in their outputs. Time-consuming manual conversions between frequency- and time-domain signals by highly skilled designers are required. Automated modeling and physical design tools are needed to improve the SiP design turn-around time and overall cost.

MEMS

Micro-Electro-Mechanical Systems (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. While the electronics are fabricated using integrated circuit (IC) process sequences (e.g., CMOS, Bipolar, or BICMOS processes), the micromechanical components are fabricated using compatible “micromachining” processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices.

MEMS encompasses a wide variety of devices. MEMS may be classified into four categories based upon their generic functional applications: (1) RF MEMS, (2) Bio MEMS, (3) Inertial MEMS, and (4) Optical MEMS. For each category their functions and operational environments will dictate the packaging requirements. For example MEMS based accelerometers and gyroscopes are three dimensional structures with moving parts within the structure. The package must provide appropriate closed cavity space for the device functional operation. On the other hand packaging for some bio sensors must provide controlled open fluid access for specimen sampling with specifically defined surface absorption properties. Tabulated below are the functional and packaging requirements for these four MEMS categories.

MEMS Packaging → ↓	*RF MEMS*	*BioMEMS*	*Inertial MEMS*	*Optical MEMS*
Requirements	Electrical – low insertion loss – low back reflection – low contact resistance – frequency – signal isolation – package resonance – low parasitics Structural – low stress – small form factor Package – wafer level package – small form factor – hermeticity – low loss packaging material – light weight	Fluidic – low dead volume – sensitivity in detection – low back pressure – fluidic channel size – flow rate – heating/cooling rate Electrical – interface with electronic circuits Thermal – fast heating and cooling Optical – low optical loss Structural – low stress at fluidic joints Package – modular package – disposable	Structural – low stress – meet reliability requirements Thermal – temperature stabilization Electrical – sensitivity – switching time – frequency – Q factor Package – plastic package – wafer level package	Optical – low coupling loss – mirror rotation/angle Structural – low stress package – low shrinkage of UV epoxy – low warpage Thermal – thermal stabilization Electrical – switching speed and time Package – ceramic package – metal package
Difficult Challenges	Optimization of electrical and structural parameters Low cost materials to reduce insertion loss Form factor reduction Passive device integration	Co-design of fluidic, electrical thermal, optical and structural design Dead vacuum reduction Channel size reduction Zero back pressure Flow in nano channels Bubble elimination Bio compatibility of material	Structural design Reliability of package Vacuum/hermeticity Low cost Small form factor Integration into other systems	Optical, structural design to meet low coupling loss/reliability Low cost Integration into other systems
Potential Directions	RF system in package Bio-RF integration	3D microfluidic package Bio system in package Plastic based fluidic systems	MEMS system in package – mobile application – bio application – information technology	Wafer level package

MEDICAL AND BIO CHIP PACKAGING

Medical and biochip packaging require specialized properties and characteristics demanded by their application. Whether for implantable medical devices, point of care, or biomedical sensors, there are specific considerations for biocompatibililty, reliability, and manufacturing.

BIOCOMPATIBILITY

Biocompatibity requires no interaction of the materials with body tissues and fluids, no inflammatory reactions, no toxicity to bio-organisms and no outgassing or other decay products that may be harmful to bio-organisms. These materials must be chemically inert to various concentrations of bio-reagents including ethanol. Physical requirements posed by some applications include high flow rates and with significant back pressure.

BIO PACKAGING RELIABILITY

The medical devices industry has some distinct advantages over other industries from an environmental point of view. Once the device is implanted, it experiences a very stable temperature, i.e., a constant temperature of 37°C (98.6°F). Therefore, thermal excursion-induced package failure mechanisms and heat dissipation are not reliability concerns.

The medical devices industry, however, faces unique reliability requirements and qualifications. The major concerns of device manufacturers are patient safety and risk mitigation. For life-sustaining devices, the acceptable and actual component failure rate could be as low as 100 ppm, with the critical failure rate as low as a few ppm. The challenge is to

capture such low occurrence failures in reliability testing. As a result, the manufacturers often over-design with significant safety margins.

Electromagnetic interference is another major area for concerns. With the increasing power and presence of electromagnetic sources, such as power lines, theft-protection gates, cell phones, home electronic appliances, airport security, etc, the interference of the electromagnetic field with the medical devices and electronic packages must be mitigated by design and assessed by reliability testing.

Patients with the implanted devices will be exposed to demanding environments. Interference with medical equipment such as CT scanners and MRI scanners needs to be prevented by design. Pressure requirements are also imposed to ensure the devices and packages function during treatment in a barometric pressure chamber or while scuba diving.

Defibrillation devices could generate significant localized heating in the high voltage charging circuit when delivering therapy. The high voltage operation poses a considerable challenge on the package substrate and the printed circuit board (PCB). The temperature rise could result in dielectric breakdown in the PCB and or substrate, the failure of incorporated field effect transistors (FET), and the failure of capacitors.

INTEGRATED CIRCUIT

The Medical Industry has very different IC challenges from the general industry dominated by personal computers, commercial, automotive, etc. For Cardiac Devices, the IC is not speed driven, since the heart works in milliseconds not nanoseconds. In general the Cardiac IC's are a large part Analog or Mixed Signal, though the amount of Digital continues to increase proportionally. The "analog" heart is an integral part of the electrical system that the Cardiac Medical Device operates in.

The biggest challenge for implantable Device IC's is current drain. Ultra low transistor leakage is the key to extended battery life. Reducing the transistor leakage decreases the device replacement rate and extends the time between surgeries. Where the implantable Device Industry pushes the envelope is by pushing the IC Technologies to the very low end of the operating voltages and currents to extend battery life. Thus issues like Negative Bias Threshold Instability and Soft Errors are a major concern, which are increasing challenges in the Deep Submicron Technologies.

MANUFACTURING

The manufacturing of packages must be conducted in accordance with regulatory requirements for medical devices, imposing new requirements for control of the manufacturing environment, labeling of the packages, and documentation. Changes in material selection and manufacturing processes require approval by regulatory agencies such as the FDA in the United States. The low manufacturing volume and specific demands of medical electronics increase the difficulty of finding suppliers who will meet the requirements or invest R&D resources to do so.

COST

The continuous reduction in cost per function has been the key to growth of the electronics industry. This has been achieved historically through scaling of the wafer fabrication processes and improvements in design. The cost of assembly and packaging has not kept pace with the cost reduction in wafer fabrication and today packaging costs often exceed fabrication cost. The cost reduction challenge is made more difficult by several factors increasing cost of packaging. Lead free solder materials, low κ dielectrics and high κ dielectrics are more costly than the materials they replace. Higher processing temperatures and a wider range of environmental temperature associated with portable consumer electronics require new, more expensive, substrate and interconnect technology. The increasing power density and decreasing junction temperature require more efficient thermal management.

New technology is required to meet the demand for more cost effective packaging. Wafer level packaging and systems in a package are among the innovative approaches to reduce cost and achieve advantages of scaling similar to the front end processes.

RELIABILITY

Rapid innovation in packaging is evident from the introduction of new package formats including area array packages; leadless packages, direct chip attach, WLP, and SiP. In addition there are new packaging requirements emerging such as silicon technologies below 90 nm using Cu/low κ materials, interconnects to address the need for flexibility and

expanding heat and speed requirements, environmental constraints such as Pb-free and halogen-free requirements enforced by law and use of electronics in extreme environments. These changes and the introduction of the new materials and structures that they demand are posing new reliability challenges. This comes at a time when there must be a substantially higher reliability on a per transistor basis to meet market requirements. New applications require new tests such as drop tests important for mobile products. New technology will be required to meet the reliability goals including:

1. New reliability tests such as drop tests for mobile products
2. Correlation between field- and laboratory testing
3. Improved methods for failure detection and analysis e.g. X-ray, acoustic, nano-deformation and localized residual stress measurement
4. Materials and interface characterization
5. Simulation and modeling for life time prediction (multi-field coupling, structure-property correlation, ab-initio methods, modular and parametric approaches)

Some new package designs, materials and technologies will not be capable of the reliability required in all market applications. More in-depth knowledge of failure mechanisms coupled with knowledge of end product use conditions will be required to bring reliable new package technologies into the market-place.

Interfacial delamination will continue to be a critical reliability hazard that is worsened by the trends to larger chips, new materials and increased layer count. More layers require the understanding of more interfaces. Standard measurement methods and acceptance criteria for interfacial adhesion are lacking. Fundamental work is needed to establish adhesion strength and degradation rate versus environmental factors (temperature, relative humidity) as well as a function of interfacial physical (such as roughness, composition) and chemical (van de Waals, dipole, covalent) properties. The CTE mismatch between the chip and the substrate should be reduced to mitigate large chip packaging-related reliability issues without increasing TCE mismatch between package and PCB. Methods to predict reliability are required to these needs. With the promise of improved performance of nano materials, understanding of the physics of the thermal, electrical and mechanical interfaces will be essential for their implementation.

PACKAGE AND INTERCONNECT CHARACTERIZATION AND SIMULATION

Tools for rapid electrical and physical fault isolation in package and interconnect structures is critical. Faster techniques are needed to execute statistically significant studies of material bulk and interface properties. Developing extensions of current fault isolation and package analytical technologies (such as X-ray, acoustic, FIB or Moire) needs to be balanced with development of new technologies for small defect visualization (such as X-ray tomography). Organic chemical interface analysis techniques are growing in importance with the introduction of new organic materials. New characterization methods are required e.g. to investigate interface strength. Methods like TEM and the corresponding preparation methods, used for failure analysis in Si technology are needed for packaging. Analysis techniques for complex thermo-mechanical, thermo-chemo-mechanical, electro-chemical failure interactions need to be developed to identify and characterize failure mechanisms related to assembly and packaging.

SIMULATION

Many of the new materials and package configurations require extensive characterization. Use of simulation to help validate and understand reliability is required to assure that technologies are deployed with reasonable risk. Simulation methods to predict reliability are needed to speed development processes. This requires new modeling and optimization techniques for complex failure mechanisms involving electrical, thermal and mechanical interactions. Improved lifetime models are needed to enable reliability predictions on system level.

Simulation of use conditions is especially important for electronic products in new consumer use environments. Comprehensive knowledge of new materials properties and interfaces are essential for reliability predictions in various market and use environments.

RELIABILITY TESTING

Accelerated reliability tests and correlation to field data are essential for package characterization today. There is a need for new materials property measurement tools e.g. micro/nano bending test to identify elastic material properties. A data base of properties for packaging materials is needed.

New electrostatic discharge (ESD) test methods and equipment are required to accommodate increasing pin count and shrinking interconnect pitch. Improved handling solutions for bare chip and packaged devices will help ESD related reliability issues.

SOFT ERRORS

The reducing of feature size increases the influence of soft errors induced by cosmic radiation or other radiation sources, which can not be avoided by packaging. Thus, in addition to avoidance of soft errors caused by alpha emitting materials in packaging material, error correction needs to be implemented at both the circuit and system design level.

PACKAGING MATERIALS REQUIREMENTS

The Assembly and Packaging industry is in the midst of a sea change in materials. The bill of materials in packages only yesterday will not be the same tomorrow. And these changes are expected to accelerate in pace and scope in the coming years. Much of the near term new materials introduction is driven by environmental regulatory compliance requirements including Pb-Free and RoHS compliance (European Union Directive for Reduction of Hazardous Substances).

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly of next generation devices. With the mechanically weaker ultra low-κ dielectrics in the device, compatible underfill materials properties in the flip chip package will lessen the risk for interface stress damage to the dielectric layer. In the developments of potential solutions such as wafer level packaging and interconnect and system in package technologies will require materials and materials processing innovations beyond what is available today. The major materials challenges are summarized in Table 95.

NEW MATERIALS

Corresponding to the requirements coming from environmental issues such as Lead-free and Halogen-free, and the requirements on next generation devices utilizing Low-κ or Ultra Low-κ (ULK), the development of new infrastructure for package materials has been requested. For the above implementation, molding compound and package substrate, which are the principal materials to determine package reliability level, have to be modified considering the thermal-mechanical stress management to adapt for Lead-free, Halogen-free and Low-κ/ULK packaging. The essential technology on mold compound and package substrate for Lead-free would be that how they keep sufficient heat resistance during solder reflow from their material characteristic point of view. Key technologies are mentioned as follows.

Table 95 Materials Challenges

Materials Challenges	*Issues*
Wirebond	Materials that enable 20 micron pitch with minimal wire sweep Barrier metals for Cu wirebond pads to reduce intermetallics Cu wire for fine pitch wire bond
Underfills	Ability to support 100 micron pitch on large die Reduce stress on low-κ materials Compatibility with lead free reflow Compatibility with standoff of <40 microns
Materials Interfaces	Increased thermal conduction Improved adhesion
Materials Properties	Methodology and characterization database with in-situ materials properties for: – frequencies above 10 GHz, – very thin layers – thermal resistance measurement methodology
Molding Compound	Low modulus materials that reduce stress on low-κ wafer structures Molding compound for very fine pitch wiring Low cost compound compatible with flip-chip processing Improved thermal conductivity to meet increasing power density High temperature compatibility for harsh environments
Leadfree Solder Flip Chip Materials	Solder and UBM the supports high current density and minimizes electromigration
Embedded passives	Improved high frequency performance of dielectrics with κ above 1000 High reliability, better stability resistor materials Ferromagnetics for sensor and MEMS applications
LTCC	Low shrink dielectric Lower dielectric constant for high frequency application
Green materials	"Green" materials with the same or better process compatibility and cost as existing materials
WLP dielectrics	Dielectrics for WLP with curing temperature below 200°C

Continued evolution of wirebond interconnects as the industry work horse calls for new material sets (wire, capillary, molding compound, bond pad) to enable 25 and 20 µm pitches wirebond interconnect integrity. Due to rising reflow temperature for Lead-free package, heat resistance and package warpage have been major issues for molding compound materials. To improve heat resistivity, proper characteristics of water absorption and resin fracture toughness will be required.

The projected reduction of flip chip bump pitch to 100 µm and below will result in corresponding reduction in UBM via size, bump diameter and gap size. Innovation in solder and UBM materials set, and underfill materials will be required for high volume flip chip assembly structure meeting requirements in environmental excursions, current density, and thermo-mechanical stresses.

The packaging structure is a heterogeneous materials structure of metals, intermetallics, polymers and filled polymers, integrated with the different devices of diverse technologies. Introduction of new materials introduces new materials interfaces. Materials interface science and engineering addressing physical interface properties and thermal, mechanical and electrical properties of the die-package structure will be of prime importance.

New class of materials will be introduced into the packaging structure to enable new package features such as embedded and integrated passives, stacked and thinned dies, wafer level process and interconnect, flexible interconnect, MEMS, medical and bio chip applications.

Knowledge of packaging materials properties are critically needed for modeling and simulation of electrical, thermal, and reliability performance for package design release and new package development. Methods for accurate characterization of materials properties and materials interface properties for packaging materials in their use environment will be needed. Establishment of materials data base to make the materials information available to the community will be important for simulation in the drive for device-package co-design.

Understanding materials interfaces for metal/polymer, polymer/polymer and intermetallics for process development, reliability projection, thermal and electrical interface physics will be extremely important. Solder to UBM intermetallics evolvement under temperature environment exposures have shown to be a major factor for thermal cycle test and drop test reliability robustness. Quantitative understanding of physics of electromigration and thermal migration will bring good understanding to design and life forecast in flip chip solder bump interconnects. Interface metrology and materials data base will be important for new materials introduction.

EMBEDDED AND INTEGRATED PASSIVES

In order to meet ever-increasing performance improvement, product miniaturization, reliability, and cost reduction demands, the cost and performance of passive devices must be improved. Integrating and/or embedding passive components into the package or the die can provide the improved performance, smaller size and lower cost required for consumer products. The Potential Solutions section discusses this subject in more detail.

ASSEMBLY AND PACKAGING INFRASTRUCTURE CHALLENGES

There are many specific technical requirements for package design. They include the basic electrical and physical design required to produce the desired circuit performance and protect the circuit so that it performs reliably in the use environment for which it is designed. The overall requirements are described in this section. The details of structures, manufacturing tolerances and materials required to implement such structures are included in the Assembly and Packaging tables.

The advent of SiP technology brings systems integration issues to packaging and with it a need for new and better design tools supporting co-design of electrical, mechanical and thermal characteristics. Chip-Package-PCB (or even Chip-Package-PCB-System) co-design, taking into account package layout, routeablity, electrical performance and thermal management simultaneously is not yet adequately supported by computer aided design tools.

ELECTRICAL DESIGN REQUIREMENTS

Manufacturing tolerances have a major impact on the performance of electrical designs. The manufacturing tolerance roadmap, reflected by the tables, for via diameter, via alignment, metal thickness, line width and dielectric thickness must be aligned with the electrical requirements. The major issues defining design requirements are discussed below.

CROSS TALK

Circuit speed and density continue their improvements from one CMOS generation to the next. Faster circuits translate into shorter clock cycles and increased density gives rise to more closely spaced parallel threads. These device advancements demand increased package I/O at ever-increasing speed. These advanced circuits require packages that minimize device, package and system noise

A major noise source is crosstalk between parallel signal lines. Crosstalk noise is roughly proportional to the ratio of dielectric thickness to edge spacing between adjacent signal lines. For a given signal line width and spacing, a lower dielectric constant medium requires a thinner dielectric to obtain the same characteristic impedance, resulting in smaller crosstalk noise. Cross talk issues are also associated with fine pitch bonding wires and fine pitch vias.

Long signal paths and narrow traces cause signal attenuation and crosstalk noise resulting in poor signal to noise ratio. The conduction related losses can be minimized through wider signal traces and special low loss dielectrics at the cost of increased package size and increased materials cost.

Differential-pair signals require two I/O pads and two signal lines for each signal. It is important that the two interconnecting signal lines in a pair are equal in length and balanced with respect to the reference plane so that delta-I noise will have little impact. This approach improves cross talk noise at the expense of increasing the number and average length of signal lines.

There are several other factors which contribute to noise as the signal frequency increases. A small bend in the signal line, a small break in the reference plane, via interconnects between signal planes, and the return current induced on the reference planes may all contribute noise that has a significant impact on electrical performance. The design of package

substrates to minimize this noise will require 3D electromagnetic simulation and modeling tools for both time-domain and frequency-domain evaluations.

The magnitude of a digital signal is much larger than that of an analog signal. The crosstalk noise imposed on the analog signal lines by the large digital signals is the major noise source for mixed signal packages. The package substrate must be carefully designed to isolate digital transients when both types of circuits exist on the same package. The cellular phone handset often implemented as a system-in-package (SiP) is a prime example. The digital baseband, RF front-end, power amplifier (PA), antenna, impedance matching networks, filters and many other passive components are placed in close proximity. 3D electromagnetic modeling for the SiP substrate and embedded passive elements will be needed.

POWER DISTRIBUTION AND POWER SUBSYSTEM

Power integrity issues are becoming more critical in high-speed systems as frequency and system complexity increase and operating voltage decreases. A power delivery system includes power supply, PCB board, package and IC. Discrete decoupling capacitors are extensively used today to damp AC noise. The ESL (Equivalent Series Inductance) associated with discrete capacitors is the major factor limiting performance at high frequency. Embedded planar capacitors and on-die decoupling cells are used to reduce high-frequency noise due to high ESL in discrete capacitors. The power delivery system consists of die, package and board connected in series. Interactions between them may cause system resonance and design defects in any one may cause system failure. Die/Package/Board co-design methodology will be required for the complex systems of the future. Typically the power supply and bulk capacitors take care of the noise below 1 MHz, the PCB and local decoupling caps on the board take care of the noise from 1 MHz to 50 MHz and on-die decoupling is used for noise above 400 MHz. The cost of on-die decoupling will be an increasing problem. Due to resonance between package and die and package and PCB, it is difficult to control power distribution impedance over a wide frequency range. This results in a packaging related bottle-neck in high-speed power delivery system design and new technology is required.

THERMO-MECHANICAL CHALLENGES IN ELECTRONIC PACKAGING

MECHANICAL CHALLENGES

The constant drive for increased functionality and flexibility in the end product will be the key driver for the electronic industry in future. With shorter design turns and faster time to market, there is little room for error during the design, development, and validation phases. The continued geometric scaling of integrated circuits, and the introduction of low-κ dielectric film materials raised the reliability concern of mechanical stress damage in the device dielectric layers induced from the thermo-mechanical stresses in the combined package device structure. Legislative requirements for lead free and halogen free materials in electronic products introduced higher temperature stresses and new packaging materials and materials interfaces into the package. The packaging industry will be facing challenge of integration across multiple device technologies such as digital, RF and MEMS, Optoelectronics, displays and others on the same packaging platform. Expanding consumer markets introduced new paradigms in reliability requirements. To ensure reliability of the end products, it is imperative to have focused R&D efforts in mechanical and thermal modeling and simulation tools.

MECHANICAL MODELING AND SIMULATION AND VALIDATION

Electronic packages represent a classic case of convergence of multi-scale, multi materials and multi materials interface systems. Not only the length scale varies from nm to mm, but also material response varies from elastic to non-linear and time-temperature dependent characteristics. It is critically important to have practical and usable tools for predictive thermal mechanical and dynamic modeling of electronic packaging structures that would help the packaging engineers to predict the failure modes and to elucidate the failure mechanisms in the development stages. This would provide the capabilities for trade offs in design, materials and manufacturing processes, and ultimately in feature, performance and cost, and time to market. Such predictive modeling tool would need to be further integrated into device package co-design environments. Coupled analysis for thermal, electrical, hydrothermal, and mechanical characteristics would be desirable.

To complement mechanical analysis and modeling efforts, it is necessary to develop accurate materials properties data over a range of loading and environmental conditions. To augment this, characterization of interfacial properties such as polymer/metal and polymer/polymer interface fracture toughness and micromechanical properties are required. The key challenge in this area is also of length scales. Metrologies are needed that can handle thin films of sub-micron thickness to measure both bulk as well as interfacial response. Properties of materials such as the various intermetallics formed from solder UBM metals interaction which grow and evolve over time and temperature will be required. Physical failure

mechanisms such as electromigration, thermal migration in combination with mechanical stresses need to be understood and modeled for practical life assessment.

There is also a strong need to develop metrologies that can use efficiently to directly measure either stress or strain under both thermal and mechanical loading conditions in thin films (for example in layers within Silicon) in packaged form. For example interferometry based techniques with sub-micron resolution is required whereas the current state of art methods have spatial resolution of 1 to 2μm. Efforts are needed in extending some of the other known concept such as digital image correlations, micro-Raman spectroscopy, PZT sensors to sub-micron length scales.

THERMAL MODELING AND SIMULATION AND VALIDATION

Challenges in electronic package thermal management arises from the continued increase in power dissipation and power density of higher frequency devices while the keeping the system cost low. The rich menu of SIP packages where a number of dies (heat sources) are placed in thermally constrained environments, such as in embedded active devices, will pose challenges in thermal management in local hot spot as well as transient temperature spike. Long term materials degradation and thermal-electromigration will be thermally driven reliability concerns. In order to provide continued cost effective, high performance thermal solutions, infrastructure development in the following areas will be needed.

Computing complexity increases with the need for larger number of mesh elements driven by complicated stack-die and 3D packaging structures. This includes thermal-electrical coupled analysis due to increasing Joule heating within the package and at the interface between package and device as well as package and board. With nanoscale packaging materials under development the physics behind the thermal modeling tools needs to be extended and implemented.

As the thermal resistances are made smaller and smaller for high power devices, thermal metrology with better resolution and capabilities is required. For example there is strong need to establish industry wide transient thermal measurement technique standard. Efficient accurate thermal sensors to support accurate understanding of Joule heating temperature distribution in the package will be desirable.

EQUIPMENT REQUIREMENTS FOR EMERGING PACKAGE TYPES

Assembly and packaging innovations such as Wafer Level Package and System in Package have specialized equipment requirements. Current equipment used for wafer level packaging is often modified front end processing equipment. New equipment will be required for wafer level interconnects structures and specialized under bump metallurgy. Examples include: solder bumping, passivation, redistribution, through via interconnect, integrated passives, backside metallization, optical interconnect, dies to wafer and wafer to wafer bonding and post processing thinning. Improvement in throughput and operating cost (cost of ownership) are essential for meeting the cost reduction requirements of the Roadmap.

Wafer thinning equipment exists today but new equipment will be needed as wafer diameter increases and the die thickness continues to decrease. The principal issues will be stress relief and surface thickness variation including roughness. Wafers thinned to 10 μm or lees will require improved processes such as dry polishing, dry etching and other process combinations.

Another important equipment requirement will be for wafer or chip handling after thinning. Equipment for ultra thin wafer handling, singulation and ultra thin die handling (e.g. pick and place) will require new technology. In addition, a new generation of die and wafer carriers such as wafer tape and glass plates must be provided to enable safe handling after thinning.

Emerging System in Package products require assembly equipment with greater versatility and precision. Assembly of SIP with a variety of IC types, optical devices, MEMS devices and bio chips on the same substrate will require substantial extension of current assembly equipment capability.

POTENTIAL SOLUTIONS

WAFER LEVEL PACKAGING

Wafer Level CSP (WLCSP) is the first generation wafer level packaging (WLP) product introduced into the market place. WLCSPs today are typically of low I/O count and small die sizes. They are mainly being used in portable consumer markets where their small size, thickness, and weight are an advantage. The development of wafer level packaging (WLP)

is proceeding in several directions: a) from low I/O, small die applications to larger die and higher functionality applications, b) to extend to higher complexity applications such as 3D wafer integration and the development of passive components, and c) development of new applications such as memory packaging and MEMS packaging. WLP developments are motivated by the recognition that wafer level processing technology—parallel processing on all the dies on the wafer, is inherently more efficient than traditional package assembly.

The manufacturing process technology and high volume infrastructure enabling wide spread implementation of Wafer Level CSP in the market place have been based upon the adoption and implementation of established flip chip wafer bumping (under bump metallurgy, solder bumping, re-passivation, redistribution, wafer inspection, wafer probing) processes and equipment in the merchant market. The infrastructure in has been developed to serve the high volume needs of flip chip packaging in the high performance and cost performance markets.

The traditional drop ball WLCSP designs and processes are being further developed with stress compliant layers, underfill in board level assembly, and compliant bump structures to allow for larger die applications. Copper trace redistribution features have been introduced for higher power and lower signal loss applications.

The processes developed for copper redistribution are being introduced and extended to the fabrication of copper studs and passive components such as inductors, to be followed by capacitors and resistors. Eventually the combination of these components will lead to capabilities for the fabrication of filters. Integration of these components into WLP packages constitutes a first step towards 3D wafer integration.

Memory devices are being used in portable consumer products such as cell phones and PDAs in increasing quantities. WLP offers advantages in these applications, due to inherent lower cost, improved electrical performance and lower power requirements. Key enabling technologies to take full advantage of WLP for these applications will be the development of cost effective wafer level test and burn-in.

Wafer Level Packaging presents good potential for 3D wafer integration. This will require wafer level alignment, wafer to wafer alignment, and wafer thinning. 3D integration using Wafer Level processes will also require the development of WLP microvias. From a technical perspective, several methods already exist today to enable the manufacture of WLP microvias. The basic processes for the etching (DRIE), insulation, and metallization steps are relatively well known. The transition from laboratory demonstrations to high volume processes will require the development of an equipment infrastructure and the existence of viable cost competitiveness applications.

Optical packaging, or packaging for detectors, requires the use of materials other than silicon. For these applications, WLP technologies and processes will evolve to include materials such as glass, organic substances or flexible substrates. For some optics components, it is necessary to have manufacturing processes for windows with materials transparent to certain wavelengths. It will also be necessary to use flux-free fusible materials and processes to prevent the contamination of optical components.

Conventional packaging technologies for MEMS often require the use of processes, including high temperatures, that are incompatible with standard microelectronics techniques for WLP. New technologies, such as thin film packaging, which utilizes an in-situ lid formation process, currently being used for micro electromechanical systems such as accelerometers and BAW filters, could be extended to other types of MEMS devices. These technologies, as well as WLP reliability and testing methodologies will be required to enable the high volume manufacturing of WLP MEMS packaging.

The progress in the field of substrate thinning and thinned chip interconnection makes it possible to envision WLP with integrated passives for RFID and other flexible electronics applications for consumers.

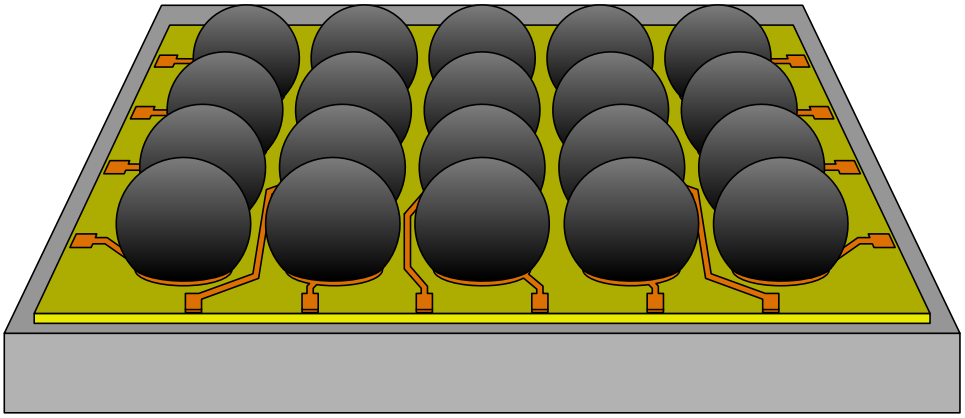


Figure 91 Example of a Wafer Level Package with Redistribution

CHIP TO NEXT LEVEL INTERCONNECT

The potential solutions for chip to next level interconnect are shown in Table 96. The values for wirebond pad pitches are shown single in line, and multiple tiered. The combinations of decreasing pitch size and multiple tier pad design provide for increasingly higher I/O requirements. The multiple tier wirebond pad design will require bonding over active circuit under pad, and bonding over low κ dielectric without damage to the circuit and dielectric materials.

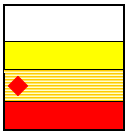
Table 96a Chip to Package Substrate—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Wire bond pitch—single in-line (micron)	**35**	**35**	**30**	**30**	**25**	**25**	**25**	**25**	**20**
2-row staggered pitch (micron)	**45**	**40**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Three tier pitch pitch (micron)	**45**	**40**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Wire bond—wedge pitch (micron)	**30**	**25**	**25**	**25**	**20**	**20**	**20**	**20**	**20**
Flying lead pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Flip chip area array pitch (micron)	**150**	**130**	**120**	**110**	**100**	**90**	**90**	**90**	**90**
Flip chip on tape or film pitch (micron)	**35**	**30**	**30**	**25**	**25**	**20**	**20**	**20**	**20**

Table 96b Chip to Package Substrate—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Wire bond pitch—single in-line (micron)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
2-row staggered pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Three tier pitch pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Wire bond—wedge pitch (micron)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Flying lead pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Flip chip area array pitch (micron)	**80**	**80**	**80**	**80**	**70**	**70**	**70**
Flip chip on tape or film pitch (micron)	**20**	**20**	**20**	**20**	**20**	**20**	**20**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 96a and b:
Validation for 100 µm pitch required
**This is for solder bump flip chip. For extremely high current applications, solder bump pad pitch may be larger to allow bigger via opening to UBM. Conductive adhesive flip chip is not addressed separately but may have smaller pitches for small die applications, provided high density substrate with competitive cost is available.*

The decreasing flip chip area array pitch provides a solution to the growing need for increasing chip signal I/O and increasing power density in cost performance and high performance applications in future technology generations. The short interconnect length in the flip chip structure has the advantages of low inductance and intra-chip electrical resistance. Native area array I/O design capabilities will be needed for improved electrical performance. This decreasing area array pitch will require advances in wafer bumping, wafer probing, underfill dispense, package substrates and test. While flip chip is expected to be the mainstay interconnect solution to serve the high performance and cost performance application segments applications, it also has advantages for the small form factor of handheld applications. When currents are low, conductive adhesives would be used.

These wirebond and flip chip chip-to-next level interconnect solution will enable a broadening single chip and multi-chip package menu. Automated design tools for optimizing trade-offs in chip-package design will be required where package solutions are the major competitive differentiators in the end electronic products.

PACKAGE TO BOARD INTERCONNECT

The organic ball grid array package (BGA) is expected to provide the industry with continued capability to deliver very high pin count components with many thousands of solder balls. In order to achieve the high pin count, the package size would grow larger and/or ball pitch would continue to shrink. The BGA pitch will however be relatively large compared to that achievable in the low cost or handheld segment where packages are small and high density boards are needed. The large pin count packages require the board routing density to be high. The slow improvement in board line width and spacing would provide some board routing density increase, but there is better opportunity for this density increase by reducing BGA pads on board and package. The smaller pads bring issues related to joint reliability and package ball co-planarity requirement. The joint reliability needs to be achieved through innovations in pad design, innovations in solder metallurgy and surface finishes, and in some cases use of board level under-fill. The co-planarity issue needs to be addressed through improvements in substrate material and design, better understanding of package behavior at high temperature, and working with process flow to do key co-planarity sensitive operations prior to solder ball attach. The Chip to Board pitch is shown in Table 97.

Table 97a Substrate to Board Pitch—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
BGA Solder Ball Pitch (mm) Conventional system Board									
Low-cost and hand-held	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
High-performance	**1**	**1**	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.5**
Harsh	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**
Small portable products using flex or other specialized subatrate									
Low-cost and hand-held	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**
CSP area array pitch (mm)	**0.3**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**
QFP lead pitch (mm)	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
SON land pitch (mm)	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**
QFN land pitch (mm)	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
P-BGA ball pitch (mm)	**1.0**	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**
T-BGA ball pitch (mm)	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**
FBGA ball pitch (mm)	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.15**
FLGA land pitch (mm)	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**

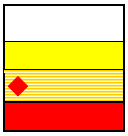
Note: T-BGA is tab interconnected BGA

Table 97b Substrate to Board Pitch—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
BGA Solder Ball Pitch (mm) Conventional system Board							
Low-cost and hand-held	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Small portable products using flex or other specialized substrates							
Low-cost and hand-held	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
CSP area array pitch (mm)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
QFP lead pitch (mm)	**0.3**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
SON land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
QFN land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
P-BGA ball pitch (mm)	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**
T-BGA ball pitch (mm)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
FBGA ball pitch (mm)	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**
FLGA land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**

Note: T-BGA is tab interconnected BGA

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



FINE PITCH BALL GRID ARRAY/CSP PACKAGES

FBGA is defined as the reduced-pitch version of BGA with the ball pitch of less than 1.0 mm. FBGA is specifically designed to realize higher-density packaging technologies for hand-held electronic devices. The technologies include substrate development for finer design rule, fine pitch bonding development, and package-structure designs to prevent warpage during reflow.

Shrinkage of the pitch to 0.4 mm required fine patterned substrate that enables routing from the die pads to package terminals. Also, surface mount process for 0.4 mm pitch FBGA should be tightly controlled. Japanese consumer market, however, saw several cell-phones equipped with 0.4 mm pitch FBGA processed by WLP technology in 2004. The ball pitch is expected to lower to 0.3 mm in 2006, 0.2 mm in 2008 and 0.15 mm in 2010 in a production phase. Shrinking ball pitch implies that the packages need underfill resin to assure solder joint reliability. Approaches to eliminate the use of underfill will be required.

Solder paste, which is applied during surface mount on a system board, is becoming thinner in response to the shrinkage of the terminal pitch. It requires tighter criteria of coplanarity both at room temperature and at high temperature during reflow. Especially, the lead-free package raised the peak temperature of the reflow condition, and makes high-temperature warpage more critical. WLP shows less warpage in a wide range of temperature. But increasing terminal count needs additional fringed area surrounding the die area to contain all balls underside of the package. The fringed area tends to warp during reflow as a result of the difference of the coefficients of thermal expansion of the die, mold compound and substrate. High-temperature warpage could be controlled by selecting the appropriate molding compound and substrate material to balance the CTE, designing balanced-package structure, and designing ball layout in the least sensitive manner for package warpage.

(The criteria for high-temperature warpage per terminal-pitch are currently under discussion in the standardization committee, and the roadmap table will be added in the next issue of ITRS.)

SOCKETED PARTS

A socket is used to provide a means of making separable electrical and mechanical connections for components such as high end microprocessors where this feature provides added value. The predominant socketable packages are pin grid array (PGA) and land grid arrays (LGA) packages. As the package pin count increases the pin pitch needs to reduce. For pin pitch below 1.27 mm, the pin diameter becomes too small making it susceptible to damage during substrate fabrication, package assembly, test and board assembly. And, as the number of pins on a package increases, probability of any of the pins being out of position also increases. So, for very high pin count packages, LGA technology is used along with appropriate socket contact. Although the LGA socket contacts at finer pitch are also susceptible to damage, the socket housing provides a good means of protecting these contacts. The scalability of LGA package land pitch is similar to that of the BGA. For socket pitch reduction, there are a variety of options available such as many unique variations in stamped metal spring contacts and wires embedded in elastomers. The LGA contact co-planarity needs to be small in order to minimize the contact deflection and load. The high layer count associated with high pin count packages as well as material and design optimizations can help achieve the co-planarity needed of such packages.

EMBEDDED AND INTEGRATED PASSIVES

An integrated passive component contains several R, L, and/or C elements on one substrate, replacing many discrete components. It may contain an array of similar elements, i.e. resistors or capacitors or inductor called passive arrays or an interconnected network of lumped or distributed R&C, or L&C, or R&L&C elements on one substrate called a passive network. Integrated passive refers to both. The price of an integrated passive component is likely to exceed that of all discrete components combined due to the relatively low market volume of a specific part. However, an integrated passive component reduces the component count and occupies a much smaller real estate on the motherboard or SiP substrate than that using the discrete components, contributing to the goal of product miniaturization. Integrated passives will be used only when required by size and performance considerations. Integrated passive may eliminate motherboard and SiP substrate vias and shorten interconnect length. This is an important consideration for performance improvement but it may be at the expense of longer time-to-market.

Passive components may be embedded in a package substrate, inside the IC die or on the wafer surface freeing the substrate surface for ICs and enabling product miniaturization. Embedded components must have stable values throughout the product life. The tolerance of the low cost embedded resistors and capacitors inside an IC is usually about 5%. Emerging requirements for some analog circuits are at 1%. Those implemented on the wafer surface have close

proximity to the active circuits minimizing parasitics and enabling active trimming. Design trade-offs must be made between the cost and performance depending upon system requirements.

Desired Figures of Merit	
Resistor Materials	*Capacitor Materials*
Range: 10Ω to 100KΩ	Dielectric Constant > 1000
TCR: 1000 ppm hot/cold	Thickness: ~10 Microns
CV: 5%	Breakdown Voltage > 100V
85RH/85C < 2% Drift	Ins. Resistance > $10^{11}\Omega$
Therm. Cycle < 2% Drift	Dissipation Factor: < 3%
Solder Dips < 2% Drift	Therm. Coeff. Cap: X7R Spec.

Embedded capacitors are critically important to high density, high performance systems. They can enable higher density, improved reliability by reducing solder joints, increased speed due to shorter signal paths and lower inductance. Embedded capacitors will be required for high density circuits operating at 2 GHz and above.

The processes used to pattern embedded resistors include photoprinting, screen printing and ink-jet printing. There are several limitations of these technologies today which limit the resistivity range and stability. In addition, adhesion promoters, reliable electrical contacts, compatibility with laser trimming and cost issues must be addressed to meet the requirements for performance, reliability and cost.

Materials and processes for fabricated passives must be compatible with the processing requirements for organic substrates. It may impact the process repeatability or the long time stability of these passives.

PACKAGE SUBSTRATES

Package substrates are both the most expensive component of most packages and the factor limiting package performance. The technology of package substrates will need to be expanded in several areas if the cost and performance projections of the Roadmap are to be met. The substrate properties required to meet market demand are shown in Tables 98 a through d.

Table 98a Package Substrate Physical Properties—Near-term Years

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Dielectric Constant (at 1 GHz)									
State of the Art	Rigid Structure	3.1	3.1	3	3	2.7	2.7	2.7	2.7	2.7
State of the Art	Buildup Structure	2.8	2.8	2.8	2.8	2.5	2.5	2.5	2.5	2.5
State of the Art	Tape Structure	2.5	2.5	2.2	2.2	2.2	2.2	2.2	2.2	2.2
State of the Art	Ceramics Structure/Low Dielectric Material	4	4	4	4	3	3	3	3	3
State of the Art	Ceramics Structure/High Dielectric Material	20	100	100	100	100	100	100	100	100
	Dielectric Loss (at 1 GHz)									
State of the Art	Rigid Structure	0.011	0.01	0.01	0.01	0.006	0.006	0.006	0.006	0.006
State of the Art	Buildup	0.003	0.002	0.002	0.002	0.002	0.002	0.002	0.002	0.002
State of the Art	Tape Structure	0.0005	0.0005	0.0002	0.0001	0.0001	0.0001	0.0001	0.0001	0.0001
State of the Art	Ceramics Structure	0.005	0.005	0.0005	0.005	0.005	0.005	0.005	0.005	0.005
	Water Absorption at 23°C/24hrs Dipped (Unit: %)									
State of the Art	Rigid Structure	0.05	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
State of the Art	Buildup with Reinforcement Material	0.05	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
State of the Art	Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
State of the Art	Tape Structure	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
	Young's Modulus (Unit: Gpa)									
State of the Art	Rigid Structure	45	45	45	45	45	45	45	45	45
State of the Art	Buildup with Reinforcement Material	30	30	35	35	35	35	35	35	35
State of the Art	Buildup without Reinforcement Material	6	6	6	6	6	6	6	6	6
State of the Art	Tape Structure	3	3	3	3	3	3	3	3	3
State of the Art	Ceramics Structure	100–300	50–400	50–400	50–400	50–400	50–400	50–400	50–400	50–400
	Peel Strength (Unit: kN/m)									
State of the Art	Rigid Structure	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6
State of the Art	Buildup Structure Buildup Layer	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6
State of the Art	Tape Structure	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

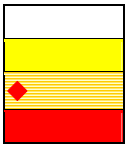


Table 98b Package Substrate Physical Properties—Long-term Years

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
	Dielectric Constant (at 1 GHz)							
State of the Art	Rigid Structure	**2.7**	**2.7**	**2.7**	**2.7**	**2.7**	**2.7**	**2.7**
	Buildup Structure	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**
	Tape Structure	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
	Ceramics Structure/Low Dielectric Material	**3**	**3**	**3**	**3**	**3**	**3**	**3**
	Ceramics Structure/High Dielectric Material	**100**	**100**	**100**	**100**	**100**	**100**	**100**
	Dielectric Loss (at 1 GHz)							
State of the Art	Rigid Structure	**0.006**	**0.006**	**0.006**	**0.006**	**0.006**	**0.006**	**0.006**
	Buildup	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**
	Tape Structure	**0.0001**	**0.0001**	**0.0001**	**0.0001**	**0.0001**	**0.0001**	**0.0001**
	Ceramics Structure	**0.005**	**0.005**	**0.005**	**0.005**	**0.005**	**0.005**	**0.005**
	Water Absorption at 23°C/24hrs Dipped (Unit: %)							
State of the Art	Rigid Structure	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**
	Buildup with Reinforcement Material	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**	**0.04**
	Buildup without Reinforcement Material	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
	Tape Structure	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
	Young's Modulus (Unit: Gpa)							
State of the Art	Rigid Structure	**45**	**45**	**45**	**45**	**45**	**45**	**45**
	Buildup with Reinforcement Material	**35**	**35**	**35**	**35**	**35**	**35**	**35**
	Buildup without Reinforcement Material	**6**	**6**	**6**	**6**	**6**	**6**	**6**
	Tape Structure	**3**	**3**	**3**	**3**	**3**	**3**	**3**
	Ceramics Structure	**50–400**	**50–400**	**50–400**	**50–400**	**50–400**	**50–400**	**50–400**
	Peel Strength (Unit: kN/m)							
State of the Art	Rigid Structure	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**
	Buildup Structure Buildup Layer	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**
	Tape Structure	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

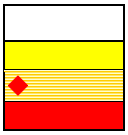


Table 98c Package Substrate Design Parameters—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Substrate cross-section core thickness (µm)									
Handhelds	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**30**	**25**
High density interconnect substrates	**100**	**60**	**50**	**40**	**40**	**35**	**35**	**30**	**30**
Build-up substrates	**400**	**200**	**200**	**150**	**130**	**100**	**90**	**80**	**80**
Coreless	**50**	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**30**
Blind via diameter (µm)									
Handhelds	**60**	**50**	**50**	**40**	**40**	**35**	**35**	**30**	**30**
High density interconnect substrates	**60**	**50**	**50**	**40**	**40**	**35**	**35**	**30**	**30**
Build-up substrates	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**25**	**25**
Coreless	**70**	**60**	**60**	**50**	**50**	**40**	**40**	**35**	**35**
Blind via stacks									
High density interconnect substrates	**2**	**2**	**3**	**3**	**3**	**3**	**4**	**4**	**4**
Build-up substrates	**4**	**5**	**5**	**6**	**6**	**6**	**6**	**6**	**6**
Coreless	**7**	**9**	**10**	**11**	**11**	**11**	**12**	**12**	**13**
PTH diameter (µm)									
	100	**80**	**75**	**70**	**60**	**50**	**50**	**45**	**45**
PTH land (µm)									
	230	**180**	**180**	**160**	**140**	**120**	**110**	**105**	**105**
Bump pitch (µm)									
High density interconnect substrates	**230**	**200**	**190**	**180**	**170**	**160**	**150**	**140**	**140**
Build-up substrates	**180**	**150**	**130**	**120**	**110**	**100**	**100**	**90**	**90**
Coreless	**180**	**150**	**130**	**120**	**110**	**100**	**100**	**90**	**90**
Lines/space width (µm)									
Rigid Structure	**45**	**40**	**35**	**30**	**30**	**25**	**25**	**22**	**22**
Build-up substrates (core layer)	**45**	**40**	**35**	**30**	**30**	**25**	**25**	**22**	**22**
Build-up substrate (build-up layer)	**18**	**15**	**15**	**10**	**10**	**10**	**9**	**8**	**8**
Coreless	**25**	**20**	**20**	**15**	**15**	**10**	**9**	**8**	**8**
Lines/space width tolerance (%)									
	10	**7**	**7**	**7**	**7**	**7**	**7**	**7**	**6**
Solder mask registration ± (µm)									
Handhelds	**25**	**25**	**20**	**15**	**15**	**15**	**12**	**12**	**11**
High density interconnect substrates	**40**	**25**	**20**	**15**	**15**	**15**	**12**	**12**	**11**
Build-up substrates	**40**	**25**	**25**	**20**	**20**	**15**	**12**	**12**	**11**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

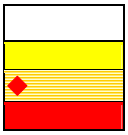
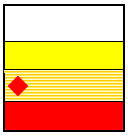


Table 98d Package Substrate Design Parameters—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Substrate cross-section core thickness (µm)							
Handhelds	**25**	**25**	**25**	**25**	**25**	**25**	**25**
High density interconnect substrates	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Build-up substrates	**70**	**70**	**70**	**70**	**70**	**70**	**70**
Coreless	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Blind via diameter (µm)							
Handhelds	**25**	**25**	**25**	**25**	**25**	**25**	**25**
High density interconnect substrates	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Build-up substrates	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Coreless	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Blind via stacks							
High density interconnect substrates	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Build-up substrates	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Coreless	**14**	**14**	**14**	**14**	**14**	**14**	**14**
PTH diameter (µm)							
	40	**40**	**40**	**40**	**40**	**40**	**40**
PTH land (µm)							
	100	**100**	**100**	**100**	**100**	**100**	**100**
Bump pitch (µm)							
High density interconnect substrates	**130**	**130**	**130**	**130**	**130**	**130**	**130**
Build-up substrates	**80**	**80**	**80**	**80**	**70**	**70**	**70**
Coreless	**80**	**80**	**80**	**80**	**70**	**70**	**70**
Lines/space width (µm)							
Rigid Structure	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Build-up substrates (core layer)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Build-up substrate (build-up layer)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Coreless	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Lines/space width tolerance (%)							
	5	**5**	**5**	**5**	**5**	**5**	**5**
Solder mask registration ± (µm)							
Handhelds	**10**	**10**	**10**	**10**	**10**	**10**	**10**
High density interconnect substrates	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Build-up substrates	**10**	**10**	**10**	**10**	**10**	**10**	**10**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Film type resins dominate as dielectrics for Build-Up substrates. Reinforcements of the film with fillers, mainly unwoven aramid, are slowly being introduced. The materials improvements are driven by the need to make finer circuits, lower thermal expansion, electrical characteristics improvements, etc. Core layer materials essentially follow the trend of rigid substrates with aramid as additional reinforcing material. LCP and other thermoplastic resins are beginning to emerge. High frequency applications drive the use of PTFE and cyanate materials. Coreless substrates are in development now and are expected to be available in volume production shortly.

Above trends in materials are progressing concurrently with the environmentally driven modifications to improve temperature robustness for lead-free assembly and to achieve halogen-free flame retardation.

High-speed transmission characteristics drive the demand for ever decreasing dielectric constant and low loss materials. Incremental materials improvements enable k~3.4. Materials are available with k down to 2.8 but they are highly priced. There are no clear, cost effective solutions available yet for k~2.5 and below.

For such low k, new reinforcement materials based not on E-glass in addition to low k resin systems need to be developed in the near future. Thermoplastic resins with high heat resistance based on olefine systems seem very feasible. Another approach is the development of porous systems.

Dielectric loss needs to be reduced by one order of magnitude in the future. PTFE and some cyanate resins achieve this. However cost effective solutions are not apparent yet.

The drive to halogen-free resin system is frequently met at the expense of dielectric properties. Therefore, a more dedicated effort to develop new, low-cost materials with low dielectric constant and low loss while being halogen-free is necessary.

As copper thickness shrinks in traces and PTHs, these features become susceptible to thermal expansion in the z-direction. Hence, CTE in z-direction must be reduced down to 20 ppm/degree for core materials and down to 10 ppm/degree for build-up dielectrics. The typical approach is to add filler to the resin system which frequently degrades other material properties or introduces process disadvantages.

Adhesion strength to copper traces is chiefly secured by a physical adhesion: rough, dendritic copper sticking into the resin. The typical roughness of Rz= 5 μm is approaching the base Cu thickness and thereby becomes a significant portion of the skin of conductor. Therefore, immediate action is required to develop chemical adhesion for smooth copper to dielectrics. Copper adhesion has to be sufficiently strong to survive processing until the traces and lands can be encapsulated with more dielectrics and/or solder mask.

BUILD-UP AND CORELESS SUBSTRATES

In the past, high performance flip chip packages were served by ceramic substrate technology which allowed near unlimited via configurations. Through vias enabled direct access of power from the board side to the corresponding chip pad while variable depth vias enabled maximum routing without unnecessarily blocking wiring channels.

The advent of organic substrates changed this design concept exclusively to through hole technology as these were based on printed wiring board technology. The invention of build-up technology introduced redistribution layers on top of cores. While the build-up layers employed fine line technology and blind vias, the cores essentially continued to use printed wiring board technology albeit with shrinking hole diameters.

The next step in the evolution of substrates was to develop high density cores where via diameters were shrunk to the same scale as the blind vias i.e. 50 μm. The initial applications were based on Teflon based dielectrics with metal alloy cores to manage package stresses. The full advantage of the dense core technology is realized when lines and spaces are reduced to 25 μm or less. Thin photo resists (<15 μm) and high adhesion, low profile copper foils are essential to achieve such resolution.

In parallel coreless substrate technologies are being developed. One of the more common approaches is to form vias in a sheet of dielectric material and to fill the vias with a metal paste to form the basic building block. A second building block is formed by laminating copper foil on both sides of the basic building block. Subsequent circuitization completes this building block. By laminating the appropriate selection of building blocks, a raw substrate is formed which only needs external finishing. Variations of this process are to form the building blocks on carrier sheets as single layers of circuitry which are the transferred by lamination to the composite stack. In either case, the dielectric materials have little or no

reinforcing material. Control of dimensional stability during processing will be essential. While different coreless technologies with proprietary designs and processes are emerging, significant market development is required to broaden the supply base, ensure stable quality and force cost reduction.

RIGID SUBSTRATE TECHNOLOGY

Rigid substrates may be divided by their application spaces: handheld and high performance.

Handhelds are driving ever thinner substrates. Total thickness has been reduced to 120 μm in high volume manufacturing and is continuing. The next stage will have to be film based materials like liquid crystalline polymers if I/O and fan out do not permit the conversion to WL packaging.

High performance packages with wire bond dice are beginning to utilize high density substrates with blind vias in laminate, essentially a build-up technology using prepreg instead of unreinforced resin. To achieve finer resolution, glass cloth with more uniform glass fiber density or glass mats will have to be developed while overall thickness of the resultant prepreg has to be reduced below 40 μm. Thereafter, film form resin systems with wire bonding resilience after lamination will have to be developed.

In general, the lack of the latter type of materials is impeding the improvement of resolution of lines and spaces.

SYSTEM IN PACKAGE (SIP) – SYSTEM LEVEL INTEGRATION

The concept of System-in-Package (SiP) has been around for many years driven by consumer electronics where increasing functionality, reducing cost and miniaturization are the main drivers. In many cases SiP offers greater flexibility, shorter time to market and less development cost than System on Chip (SoC).

The ITRS-TWG defines a SiP as follows:

"System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system."

SiP generally include both analog and digital circuitry as well as non-electronic devices. This definition includes a wide variety of solutions based on different substrates and interconnect technologies, use of integrated or discrete passives, and unlimited variations in size and performance. SiP can incorporate integrated passives, and devices of different technologies which makes them ideal for RF wireless systems (RF, baseband: + SRAM + flash memory).

A long term vision for SiP is the optimized heterogeneous integration of wireless, optical, fluidic and bio elements and interfaces with shielding and thermal management. New integration techniques allow integration of devices for sensing, signal and data processing, wireless and optical communication, power conversion and storage in a single package.

A strategy and technology to solve the known good die and known good package issues will be essential to the success 0f SiP.

TYPES/CATEGORIES OF SIP'S

There are several categories of SiP defined in Figure 92. SiP can be manufactured using ceramic, leadframe, organic laminate, silicon or even tape-based substrates. Passive components can be either embedded as part of the substrate construction or soldered or epoxy attached on the substrate surface. Stacked single packaged chips can also be considered as a SiP.

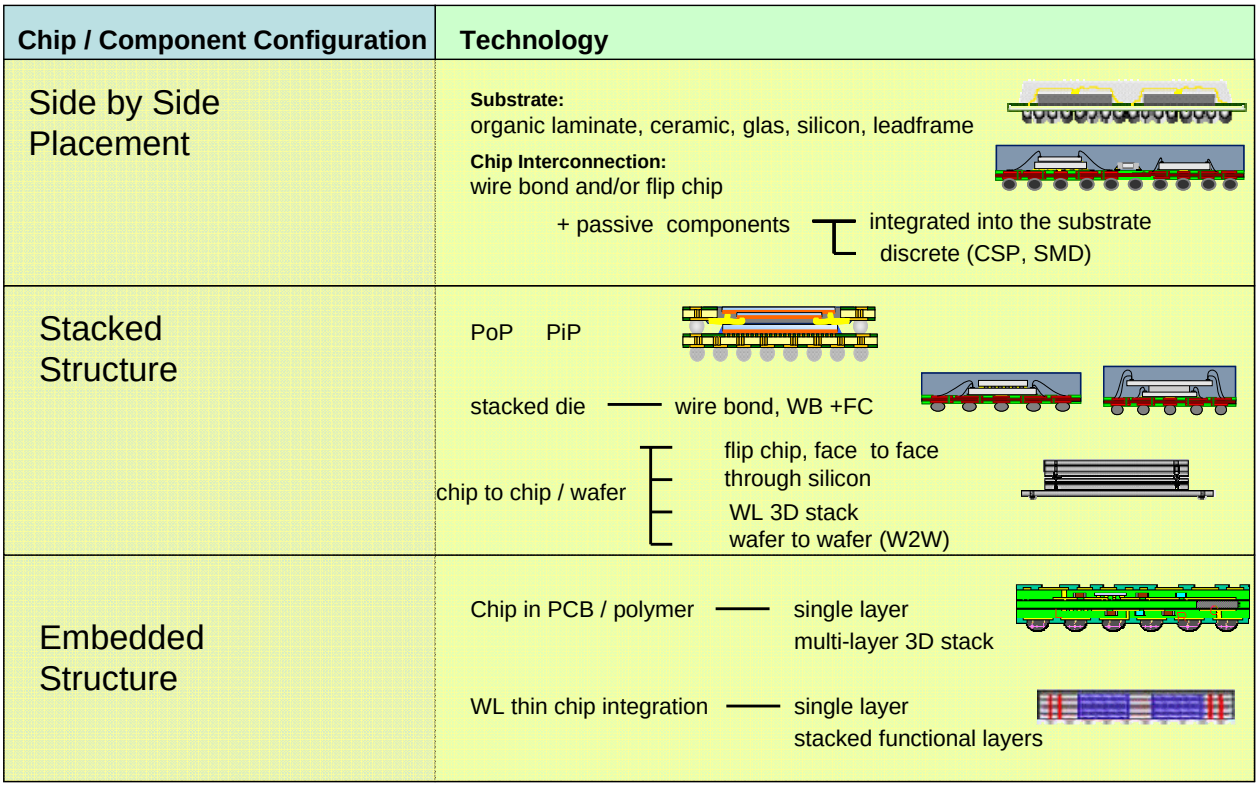


Figure 92 SiP Types and Categories

SIDE BY SIDE PLACEMENT (HORIZONTAL PACKAGES)

Side by side solutions have been used for many years. This SiP architecture offers higher integration density using a wide range of substrates (see Figure 92). Well established interconnection technologies such as wire bonding are typical. Advantages of side by side solutions are: improved heat dissipation, combining different interconnection technologies (wire bonding, flip chip, different types of semiconductor devices (e.g. Si, III/V) and integration of SMD components. Today "side by side solutions" are often combined with Stacked Structures in a single SiP.

STACKED STRUCTURES

Stacked structures increase density through use of the third dimension. This is implemented on different levels such as package stacking (PoP, PiP), die stacking, and chip to chip/wafer or wafer stacking. Advantages of stacked solutions are saving of board area and shorter interconnection between the devices.

PACKAGE-ON-PACKAGE (POP), PACKAGE-IN-PACKAGE (PIP)

This includes pre-packaged devices that are stacked on top of each other using leadframe, organic and flex-based substrates. The main advantage of this type of SiP´s is that it is possible to test each package before stacking and thus the "Known good die" problem is circumvented. Figure 93 represents some examples of different constructions.

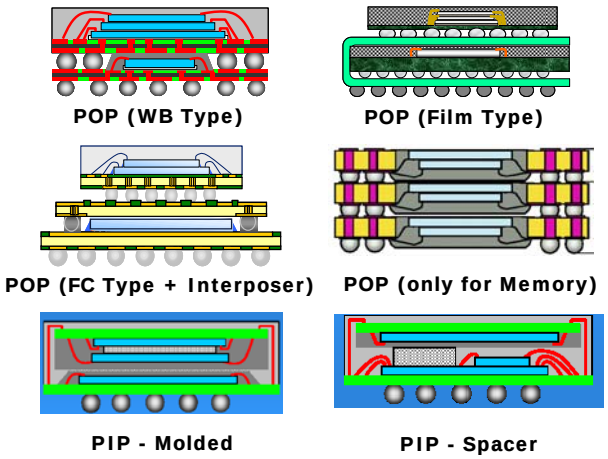


Figure 93 Technologies for Stacked Packages

STACKED DIE PACKAGES

Today Stacked Die Packages are common in mobile products. They take advantage of standard chip and wire bonding techniques and allow the use of existing infrastructure/equipment. Stacked Die Packages, for memory subsystems are in production in high volumes for *USB memory and CF, SD, XD memory*. One of the critical factors is reduction in overall package thickness. Current market requirements are for up to eight die assembled vertically in a single package with a mounted height of less than 1.2 mm. This requires thinner substrates, lower loop wire bonds, lower mold cap heights, and thinner die. As more die are used in each package, the thickness of each component becomes more critical.

The technologies used and development required to satisfy the requirement for thinned die are discussed in the wafer thinning section.

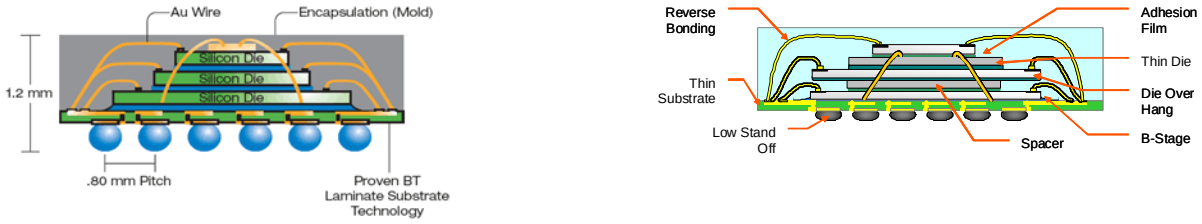


Figure 94 Examples of Stacked Die Packages

CHIP TO CHIP/WAFER STRUCTURE

Stacked Die Packages are not always appropriate for devices with high I/O densities, since the substrates cannot accommodate such high attachment pad and routing densities. As pin count per device is increased, the complexity of the interconnects is magnified and yields may suffer. At this time stacked die packages have limited ability to incorporate passive components. Flip chip technology, face to face and through silicon, e.g. inter-chip via—ICV, approaches offer the possibility of handling multiple devices with high I/O density.

The primary driver for 3D integration is size reduction i.e. minimum area/volume of an electronic system. Side by side solutions, stacked packages and stacked die solutions can result in relatively long interconnects. This is also the case for SoC solutions with very large chips. Long interconnects result in reduced speed and increased power consumption. 3D integration is one promising solution to solve this "interconnect bottleneck".

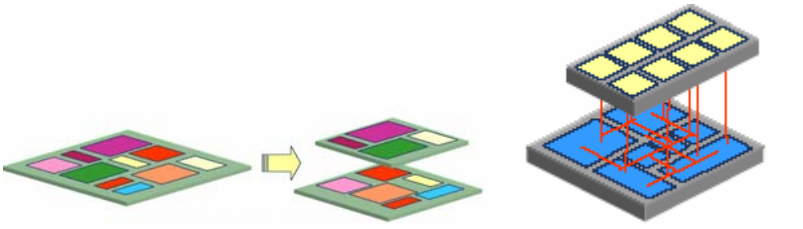


Figure 95 3D Integration Provides Space Saving and Short, Direct Interconnect Lines

Heterogeneous integration, providing "seamless" mixing of devices from different microelectronic technologies at the wafer level offers a mid-to long term challenge for 3D integration. If the functional "tiles" on the chip are stacked in the 3rd dimensions, the chip area is reduced, resulting in shorter interconnect lines.

EMBEDDED STRUCTURES

Embedding of electronic devices into or on the substrate is another example of 3D integration. In this case active and passive device are implemented into the system e.g. during the manufacturing process of the substrate itself (substrate level) or will be integrated as thinned devices during wafer level processing on a carrier (e.g. Si, glass, polymer). In addition to size reduction the integration of high Q passives leads to advantages in electrical behavior and reliability.

The driving forces for embedded active and passive elements are small size and low package weight. Lower wiring length allows for higher performance. There are the potentials for lower cost and improved reliability through reduced process steps and reduced solder joints. In addition to the very substantial challenges of physical design and manufacturing processes and reliability, the major challenges for embedded structure technology will be strategies and solutions for test, yield, and rework. Thin packages deliver small size, low weight, and increased performance at the same time.

TECHNOLOGIES FOR SIP

The realization of SiP requires integration of different components and functions, miniaturization, functionality, reliability, cost etc. A major challenge is the evolution towards heterogeneous integrating different components using different technologies and materials. The systems approach requires integrated co-design and manufacturing and has to merge interdisciplinary technological approaches and solutions. Table 99 gives an overview of present and future requirements, components and processes used for SiP.

Table 99 Package Level System Integration

				2005	2006	2008	2010	2012	2014
				High Performance/Low Cost, Handheld					
Passive devices	***Capacitor***	o for YES		o/o	o/o	o/o	o/o	o/o	o/o
	Resistor			o/-	o/o	o/o	o/o	o/o	o/o
	Inductor			-/o	o/o	o/o	o/o	o/o	o/o
Active devices	***Optical***	o for YES		o/o	o/o	o/o	o/o	o/o	o/o
	CCD/CMOS Sensor			-/o	-/o	-/o	-/o	-/o	-/o
	MEMS			-/-	-/-	-/o	-/o	-/o	-/o
Package Inner Structure	***IC to IC Connection***	o for Applicable	Wire	-/o	-/o	-/o	-/o	-/o	-/o
			Flip Chip	-/o	o/o	o/o	o/o	o/o	o/o
			Via Hole	-/-	-/o	-/o	-/o	-/o	-/o
	IC to Substrate Interconnection	o for Applicable	Wire	o/o	o/o	o/o	o/o	o/o	o/o
			Flip Chip	o/o	o/o	o/o	o/o	o/o	o/o
			Via Hole	-/-	-/o	-/o	-/o	-/o	-/o
Embedded Components	***IC***	o for Applicable	IC	o/o	-/-	/o	/o	o/o	o/o
	Passives		Capacitor	-/-	o/o	o/o	o/o	o/o	o/o
			Resistor	-/-	o/o	o/o	o/o	o/o	o/o
			Inductor	-/-	-/o	o/o	o/o	o/o	o/o
Substrate Material	***Organic***	o for Applicable	Rigid	o/o	o/o	o/o	o/o	o/o	o/o
			Flexible	-/o	-/o	-/o	-/o	-/o	-/o
	Inorganic		Ceramic	o/o	o/o	o/o	o/o	o/o	o/o
			Silicon	-/-	o/o	o/o	o/o	o/o	o/o

Today different technologies at wafer, substrate and board level are available to realize high miniaturized systems for different applications. Both conventional and new technologies are incorporated for SiP applications at both substrate and wafer level. Table 100 gives an overview of key processes at substrate- and wafer level for SiP.

Table 100 Processes used for SiP

Technologies and Processes for SiP	*Substrate Level*	*Wafer Level*
Pre-processing of wafers		
Thinning, dicing	ca.50 µm	< 20 µm
Wafer bumping	Low cost, pitch> 100 µm	Fine pitch and bumpless
Die attach		
Epoxy	■	
Tape	■	
Soldering		■
Polymer		■
Interconnects		
Wire bonding	Low loop bonding	/
Flip chip bump bonding	Mixed WB /FC	Size/pitch (>50 µm)
Face to face	/	Fine pitch (<10 µm) Thin interconnects
Bumpless/Seamless	Electroless	Thin film interconnects, fusion
Underfilling		
Via formation	Photo/drilling, laser	Through silicon etching, photo
Via metallization	Plating, electroless	Electroplating, CVD
Wiring	Substrate wiring (see chapter substrates)	Thin film redistribution
Encapsulation	Molding	Molding
		Wafer/wafer (glas) bonding

Legend: ■ most preferred used

Conventional interconnect technologies such as wire bonding, flip chip bonding, die attach etc. are used for SiP applications. The advantage is that existing equipment can be used and only minor process changes are required. One key challenge here is to find the right trade-offs of assembly and physical design rules for the application. For example in a stacked die solution trade-offs between thickness of the die, overhang dimensions, wire bond parameters etc. must be determined. Die attach technology is improving to meet the requirements of SiP. Tape die attach approaches, not available a few years ago, are now becoming available and are being further improved. Die attach materials and processes are being improved to allow further miniaturization, yield improvement and cost reduction.

Molding becomes challenging because of the move to Cu/low κ technologies and the requirement for thin packages. The mold process must be adjusted to allow lowest mold thickness over the top die (< 100 µm) in a stacked die solution.

WAFER LEVEL SiP AND 3 D INTEGRATION TECHNOLOGIES

In general the 3D integration is based on thinning, adjusted bonding and vertical (through silicon) metallization of completely processed device wafers by inter-chip vias. For wafer stacking approaches, the step raster on the device wafers must be identical. This is fulfilled for 3D integration of devices of the same kind (e.g. memories) but in the general case of different device types processing with identical step raster results in active silicon loss and an increase in fabrication cost.

Vertical system integration technologies with freely selectable inter-chip vias for 3D SiP enable high performance and extreme miniaturization. Manufacturing technologies that largely rely on wafer fabrication processes allows a comparatively favorable cost structure. On the other hand, wafer yield and chip area losses and final test will be major challenges for wafer stacking concepts. An example of processes for formation of 3D multiple device stacks is shown below. This approach (developed by Fraunhofer IZM) combines the interchip via process with the solid-liquid-inter-diffusion technique. Figure 96 shows the schematic cross section of this vertically integrated circuit stack process concept.

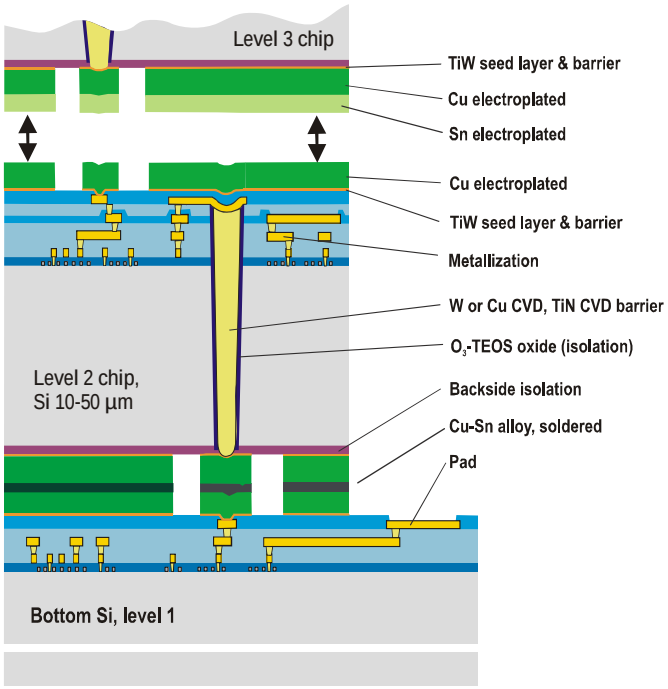


Figure 96 ICV-SLID Technology: Schematic for the Formation of Multiple Device Stacks

TECHNOLOGIES FOR EMBEDDED DEVICES

The need to save surface real-estate can be met by removing active and passive devices from the surface and embedding them into the substrate. By embedding simpler devices, the surface can be used for the high value devices such as microprocessors and custom ASICs. A number of approaches for embedding active and passive devices into/on the substrate have been under development for specific applications (aerospace, military). An example is the integration of power devices.

The main feature for device integration into a substrate is the embedding of thin chips into built-up layers of organic substrates and boards without sacrificing space on the substrate surface. Embedded active devices can be combined with integrated passive components. The processes, e.g. lamination, via formation, plating, and equipment from advanced substrate manufacturing may be used. The principle structure is shown in Figure 97.

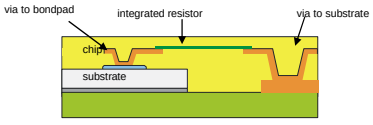


Figure 97 Principle of the Chip in Polymer (CiP-Fraunhofer) Structure with Embedded Active and Integrated Passive Devices

CHALLENGES FOR SIP

System-in-Package solutions have become commonplace in small form factor systems, such as mobile phones, PDAs, and other high-density portable electronics. The variety of solutions continues to expand from simple stacked packages to more complex solutions. Challenges with physical design, known good die, test strategy, wafer thinning, manufacturing processes and yield and substrate complexity will continue to drive new solutions particularly for 3D integration. Challenges in implementation of SIP include many of the issues associated with traditional large scale system packaging but in addition, a host of new issues must be addressed:

- Die, Package and System design integration tool including mixed digital and RF.

- Level of integration trade off of risk, cost and cycle time.
- Design tools which to accommodate new design challenges as SIP technology expands, such as for active and passive devices, package and substrates as well as for materials data base to reach optimal design for the system.
- MEMS, nanotechnology, and other new capabilities must be accommodated.
- Industry standard I/O specifications for "in package" interconnect between die with reduced drive, reduced swings, reduced ESD protection, etc to increase performance and reduce switching power dissipation (lower capacitance, etc.

THERMAL MANAGEMENT

TESTABILITY

Higher levels if integration in the package bring new challenges for test and reliability of the final assembly. A process to ensure that the die used are known good is essential. BIST or JTAG testing may not be sufficient to ensure functionality. A full functional test may then be required, as in the case of an MCM with logic and cache memory.

OPTICAL SIGNAL TRANSMISSION

The integration of optical transmission paths into a SIP will drive more test requirements into the assembly and packaging. The optical transmission performance is dependant on the physical aspects of the base material, the optical material (both the core and the cladding) and also the processing of the material during construction. Wall roughness will reduce the attenuation of the optical path and thus strict process parameters needs to be defined and followed.

TEST AND REWORK

Depending on technologies used partial repair may become difficult or impossible. Better redundancy/test and repair technologies are required for the final stack to achieve yield/cost targets.

RELIABILITY

There is a need to better understand and develop analysis capabilities for stress and thermal characteristics in stacked die packages. Very thin die and thin substrates and die of different processes including low κ dielectrics, flash, require reliability modeling so that problems can be anticipated during development rather than found when the product reaches life test or systems in the field. Understanding of acceleration factors will be important. Impact of various interconnects and interconnect stability after joining and definition of reliability requirements for new processes will also be needed.

SYSTEM IN PACKAGE OUTLOOK

In the medium to long term technologies can be expected that exploit unique nanometer scale phenomena integrated into microscale and macrosystems, providing integrated systems with unprecedented functionality and performance. To achieve this a number of issues must be addressed e.g. coupling molecular level structures and devices to larger scale platforms and devices, combining "top-down" and "bottom-up" assembly in order to create new classes of functional materials or to manufacture an integrated system, controlling the electrical interface between the different components and in mid- and long term scenario biological and non-biological components in one architecture, and coupling mechanical forces across nano, micro and macro scales, including the control of fluid-state transport or optical behavior. Fig xx presents a potential structure of a SIP.

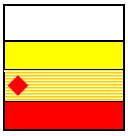
Table 101a System-in-a-Package Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Low cost/handheld	**600**	**600**	**700**	**800**	**800**	**800**	**800**	**800**	**800**
High performance	**1000**	**1200**	**1350**	**1500**	**1750**	**2000**	**2000**	**2000**	**2000**
Number of terminals—maximum RF	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**
Low cost/handheld (# die / stack)	**6**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
High performance (# die / stack)	**2**	**2**	**3**	**3**	**3**	**4**	**4**	**4**	**5**
Low cost/handheld (# die / SiP)	**6**	**8**	**8**	**8**	**9**	**11**	**12**	**13**	**14**
High performance (# die / SiP)	**4**	**5**	**6**	**6**	**6**	**7**	**7**	**7**	**8**
Minimum component size (microns)	**600x300**	**600x300**	**400x200**	**400x200**	**400x200**	**200x100**	**200x100**	**200x100**	**200x100**
Maximum reflow temperature (°C)	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**

Table 101b System-in-a-Package Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Low cost/handheld	**800**	**800**	**800**	**800**	**800**	**800**	**800**
High performance	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**
Number of terminals—maximum RF	**200**	**200**	**200**	**200**	**200**	**200**	**200**
Low cost/handheld (# die / stack)	**14**	**14**	**15**	**15**	**16**	**16**	**17**
High performance (# die / stack)	**5**	**5**	**6**	**6**	**6**	**7**	**7**
Low cost/handheld (# die / SiP)	**15**	**15**	**16**	**16**	**17**	**17**	**18**
High performance (# die / SiP)	**8**	**8**	**9**	**9**	**9**	**10**	**10**
Minimum component size (microns)	**200x100**	**200x100**	**200x100**	**200x100**	**200x100**	**200x100**	**200x100**
Maximum reflow temperature (°C)	**260**	**260**	**260**	**260**	**260**	**260**	**260**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



WAFER THINNING

Wafer thinning is part of back end processing. After the wafer thinning process, the wafers will continue in the manufacturing processes including wafer dicing, pick and place, and the different assembly and packaging processes such as wire bonding and molding. Thin wafer handling and thin die handling within the backend process flow would constitute an important part of the Wafer Thinning implementation in the back end for 200 mm and 300 mm wafers.

There are four basic wafer thinning processes: a) mechanical grinding, b) chemical mechanical polishing (CMP), c) wet etching and plasma, and d) dry chemical etching. A discussion of the specialized equipment required for this process can be found in the infrastructure section of this chapter.

A high volume wafer thinning manufacturing process may incorporate two or more of these methods for practical implementation. Typically a high volume grinding process would incorporate coarse grinding to remove the bulk of the wafer thickness and fine grinding to produce a smoother surface and to remove most of the mechanically damaged surface layer. To achieve better surface smoothness and thickness uniformity and to remove the remaining surface layers containing defects or microcracks, additional surface removing process steps would be employed. Today 50 µm wafer thickness for 200mm/300mm wafers are in volume production with total thickness variation (TTV) </= 2 µm.

Wafer thinning has been undertaken at the backend after the wafers are completely finished at the foundry. In the cases where additional backend processes are required, e.g. wafer bumping, wafer thinning is undertaken after bumping. Methodologies have been developed to protect the front side during the wafer thinning processing. The combination of larger wafer diameter (300 mm) and bumps at the wafer front surface makes it more difficult to reach lower thickness now available for non-bumped wafers. It is expected that with advances in wafer level packaging increasing function and complexity post foundry processing, the thinning techniques have to be considered part of the overall wafer level packaging process and equipment development advances.

A high volume thinned wafer production process must incorporate wafer thinning, thin wafer/die handling systems, such as a wafer tape carrier and/or glass carriers compatible with subsequent down stream back end processes and a singulation process. Single thinned die will be laminated and interconnected. (see 3D packaging section)

The table below represents the silicon thickness for traditional digital and mixed signal integrated circuits. There will be specialized applications associated with integrating silicon into flexible products such as RFID circuits incorporated into fabric or other thin film consumer products for which the wafers will be thinned to below 10 microns beginning in 2007.

Table 102a Thinned Silicon Wafer Thickness 200 mm/300 mm—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Min. thickness of thinned wafer (general product)	**75**	**70**	**65**	**60**	**55**	**50**	**45**	**40**	**40**
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)*	**50**	**25**	**20**	**20**	**15**	**15**	**10**	**10**	**10**

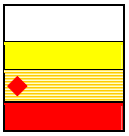
**Includes metallization and passivation*

Table 102b Thinned Silicon Wafer Thickness 200 mm/300 mm—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Min. thickness of thinned wafer (general product)	**40**	**40**	**40**	**40**	**40**	**40**	**40**
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)*	**10**	**8**	**8**	**8**	**8**	**8**	**8**

**Includes metallization and passivation*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



GLOSSARY OF TERMS

SYSTEM IN A PACKAGE (SIP)

System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system.

WAFER LEVEL PACKAGING (WLP)

Wafer level packaging (WLP) is a technology in which all the IC packaging and interconnection is performed on the wafer level prior to dicing. All elements of the package must be inside the boundary of the wafer. Chips mounted on a structured wafer (e.g. by face to face technologies) and packaged at wafer level before dicing are also considered as wafer level packages.

INTEGRATED PASSIVES

Integrated passives are arrays or networks of passive elements including resistors, capacitors and inductors integrated on a single substrate to form a single passive component.

EMBEDDED PASSIVES

Embedded passives are passive components that are incorporated into an IC, added on top of an IC through the addition of a layer, embedded in a build-up polymer interconnect layer or embedded in a package substrate.

3D PACKAGING

3D packageing refer to packaging technologies where a substantial fraction of the die to die interconnections are not planar to the package substrate.

QFP

A ceramic or plastic chip carrier with leads projecting down and away from all sides of a square package. Usually, the back side of the die is bonded to the leadframe substrate, and the electrical connections are made on the active top side of the die through wirebonding process and the whole package is encapsulated by a molding process.

QFN

A ceramic or plastic chip carrier with contact leads underneath the four sides of the package. Usually the backside of the die is bonded to the leadframe substrate, and the electrical connections are made to the top side through the wirebonding process.

P-BGA

A plastic package employing an array of solder balls for physical connection to the next level which is usually a printed circuit ball. Usually the back side of the die is bonded to a laminate substrate, and the electrical connections are made on the active top side of the die through wirebonding process, and the top side of the package is encapsulated by a molding process.

T-BGA

Tape BGA. Similar to P-BGA where the substrate are made of a circuitized metal on a polymer tape. The interconnection to the die made be made by thermocompression bonding in a single step.

FC-BGA

Flip Chip BGA. Similar to P-BGA where the die to substrate interconnection is made with the flip chip process, i.e. the die faces down with interconnection made through metal (solder) bumps on the die. Usually the space between the die and the substrate is filled with an underfill material.

FC-LGA

Flip Chip Land Grid Array. Similar to FC-BGA, without the solder balls on the array of contact lands on the substrate

CROSS-CUT ITWG ISSUES

DESIGN

6. Co-design of electrical/thermal and mechanical
7. Chip size roadmap
8. Thermal dissipation (per die/per package)
   a. Low power and high power density
   b. Hot spot issues
9. Native area array design
10. Co-design of MEMS and electrical, etc. functions

FACTORY INTEGRATION

DIE TRACEABILITY CROSSCUT WITH FACTORY INTEGRATION

When a customer returns a defective electronic product, it is extremely important to locate the defective component, identify the root-cause, and find a solution and implement it. The defect could be due to board assembly, packaging of active and/or passive components, or the IC. The IC manufacturer would like to identify the wafer where the defective IC comes from. The database will help find out the root-cause and facilitate the implementation of a solution.

Very often, a die could be one of several hundreds or even thousands in a 300 mm wafer. There is no room on the package surface to include information including die location on a specific wafer. Typically, the IC package carries only a "date code". This identifies a date on which many wafers have been processed and there is no information to indicate its location on a wafer.

The information gathered during wafer-level testing before dicing is extremely valuable to the IC users and manufacturers. The wafer ID, the locations of all failed ICs and their failure modes are available. Note that the amount of test data is about 2 GigaBytes for a 200 mm wafer, and 5 BG for a 300 mm wafer. A typical semiconductor factory processes 30,000 200 mm wafers, or 20,000 300 mm wafers each month. It would take 60 to 100 TeraBytes of storage space to store one month test data for a typical factory.

For the low-cost ICs, the test data is not kept at all to avoid the overhead cost associated with data storage. For the high value ICs, the test data is kept by the design houses, not at the semiconductor foundries. Note that it may be necessary to archive these data for years. For these high value ICs, it is possible to formulate a forward-looking strategy. The implementation of such a strategy involves extracting the signature of each high value wafer. The signature may include the following:

1. The location of fail chips. It is important to generate a wafer map for each failure type. The potential failure types are as follows:
   - Delay time beyond spec
   - Output voltage too high
   - Output voltage too low
   - Power supply voltage at 3 sigma below nominal
   - Power supply voltage at 3 sigma above nominal
   - Test temperature at 3 sigma below spec
   - Test temperature at 3 sigma above spec
   - Other information as appropriate
   - Additional information learned from experience
2. The locations and wafer maps of good chips, which pass within one sigma of test specs, which could be the delay time, the input or output voltage level,... etc.. In short, these are excellent chips in meeting specs.
3. The locations and wafer maps of good chips, which pass within plus or minus two sigma of test specs.

4. The locations and wafer maps of good chips, which pass within plus or minus three sigma of test specs.
5. Additional wafer-level signature information learned from experience.

As one accumulates knowledge on the above wafer-level signature, one may come to the conclusions that the complete test data (2 GB for each 200 mm wafer, or 5 GB for each 300 mm wafer) is not necessary. In other words, one would reduce the cost of test data storage.

In addition, the diagnosis of each field-return defective packaged-IC could be substantially shortened, since we would have immediately available prior knowledge as follows:

A. What kind of early failure could be expected from which wafer at which site?

B. What kinds of root-causes could be associated with these failures?

C. What kind of on-board or on-package test could be deployed for each potential root-cause?

D. Is a destructive analysis required for the root-cause diagnosis?

There are several questions to be answered during design of such a data system:

What could we learn should the returned defective packaged-IC defy our wafer-level signature information? Could the information be used to identify additional root-cause at wafer manufacturing, at IC packaging, or at board assembly? What are the possible additional wafer-level signature information should we gather?

INTERCONNECT

1. Low κ dielectric
2. 3D packaging
3. Thinned die
4. Top level metallurgy
5. Fine pitch chip to first level interconnect

RF/AMS WIRELESS

1. Cross talk
2. Pin count for each pin type
3. Low voltage operation
4. Specification for embedded passive component.

ENVIRONMENT, SAFETY AND HEALTH

1. Regulatory environment
2. New materials

MODELING AND SIMULATION

1. RF/mixed signal models for devices and packages
2. Integrated or coupled Thermal/mechanical/electrical package simulation
3. Design and Process tolerances taken into account in simulation tools
4. Modeling should include dynamic models (an example is shock associated with dropping a portable product)

METROLOGY

1. Materials properties needed
2. Impact of size on materials properties

TEST

1. SiP
2. High pin count packages
3. Wafer level packaging
4. Thermal management during test
5. Wafer level test
   a. Power and ground distribution during test
6. Burn-in