INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

EMERGING RESEARCH DEVICES

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SCOPE

The Semiconductor Industry is poised to sustain the extraordinary exponential growth of information technology for the next several years by continuing its unprecedented success in scaling CMOS beyond the 22 nm generation. Continued growth of information technology beyond ultimately scaled CMOS, in the nearer term, will require heterogeneous integration of new technologies with the CMOS platform, i.e., "enhanced CMOS." In the longer term the industry is facing an exciting but daunting challenge to invent one or more fundamentally new approaches to information and signal processing. This will likely require discovery and exploitation a new means of physically representing, processing, storing and transporting information via new materials, process, device, nano-architecture, and systems innovations.

A primary goal of this chapter is to stimulate invention and research leading to one or more new concepts to extend functional scaling of information processing substantially beyond "ultimately scaled" CMOS. This goal is accomplished by addressing the two technology-defining domains identified above—extending the CMOS platform via heterogeneous integration of new technologies and, later, via developing new technological and nano-architectural concepts. The intent is two-fold. First is to "cast a broad net" to gather in one place substantive, alternative concepts for memory, logic, and information processing nano-architectures that would, if successful, substantially extend the Roadmap beyond CMOS. As such, this discussion will provide a window into these candidate approaches. Second is to provide a balanced, critical assessment of these emerging new device technologies for information processing. In this regard, a brief new section is added to propose a set of fundamental principles that will likely govern successful extension of information processing technology substantially beyond that attainable with ultimately scaled CMOS. This broadened chapter, therefore, provides an industry perspective on emerging new device technologies and serves as a bridge between bulk CMOS and the realm of microelectronics beyond the end of CMOS scaling.

In previous editions, the scope of this chapter included new approaches to emerging research memory, logic, and nano-architecture to enable new information processing technologies. For the 2005 ITRS, the scope is expanded to include an important new section on Emerging Research Materials. This section introduces and describes those properties of essential new materials critically required to support realization of the emerging research memory and logic devices. Additionally, this new materials section includes synthesis techniques, metrology and characterization and the modeling and simulation infrastructure and tools needed to develop those required materials. Conventional materials and processes currently used in CMOS technology, which may be also be used to realize Emerging Research Devices, will be treated in the *Front End Processes (FEP) chapter*. Also, the sub-section on Non-classical CMOS, previously treated in the 2003 ERD chapter, has been transferred to the *Process Integration (PIDS)* and FEP chapters. With this expanded scope, the chapter now addresses all physical technologies contributing to new information technology paradigm, from materials and devices to device level nano-architectures.

The discussion is divided into the following four categories: 1) Materials, 2) Memory Devices, 3) Logic Devices, and 4) information processing Nano-architectures. The discussions provide some detail regarding their operation principles, advantages, challenges, maturity, and current and projected performance. Also included is a preliminary but interesting comparison of the performance projections and cost attributes for several speculative new approaches to information and signal processing. An interesting observation of this comparison is that the emerging devices, materials, technologies, and architectures, given their successful development, would extend applications of microelectronics to domains not accessible to CMOS, rather than competing directly with CMOS in the same domain.

Finally, inclusion of a concept in this chapter does not in any way constitute advocacy or endorsement of that concept.

DIFFICULT CHALLENGES

INTRODUCTION

The microelectronics industry is facing two classes of difficult challenges related to extending integrated circuit technology beyond the maturation of CMOS scaling. One set relates to extending CMOS beyond its generic density and functionality by integrating, for example, a new high speed, dense, and nonvolatile memory technology on the CMOS platform. Another class of challenges is to extend information processing substantially beyond that attainable by CMOS

using an innovative combination of, perhaps, new materials, devices and architectural means for representing, processing, transmitting, and storing information. These Difficult Challenges will be organized to separately discuss Device and Materials Difficult Challenges.

DEVICE TECHNOLOGIES

Difficult Challenges related to emerging research devices are further divided to those related to memory technologies and those related to logic devices. One such challenge is the need of a new memory technology that combines the best features of current volatile and non-volatile memories in a fabrication technology compatible with CMOS process flows. This would provide a memory device fabrication technology required for both stand-alone and embedded memory applications. The ability of an microprocesser unit (MPU) to execute programs is limited by interaction between the processor and the memory, and scaling does not automatically solve this problem. The current evolutionary solution is to increase MPU cache memory, thereby increasing the floor space that static RAM (SRAM) occupies on an MPU chip. This trend eventually leads to a decrease of the net information throughput. In addition, volatility of semiconductor memory requires external storage media with slow access (e.g., magnetic hard drives, optical CD, etc.). Therefore, development of *electrically accessible non-volatile* memory with *high speed* and *high density* would initiate a revolution in computer architecture. This development would provide a significant increase in information throughput even if traditional benefits of scaling were fully realized for nanoscale CMOS devices.

A longer-term challenge for information processing or logic devices is invention and reduction to practice of a new manufacturable information processing technology addressing "beyond CMOS" applications. Solutions to this challenge could open new opportunities for nanoelectronics beyond the end of CMOS scaling by extending current and enabling new information processing functionalities.

Table 52 Difficult Challenges—Emerging Research Device Technologies

Difficult Challenges ≥32 nm	*Summary of Issues*
Development and implementation into manufacturing of a non-volatile memory technology, scalable beyond 32 nm, combining the best performance features of both volatile and non-volatile memory technologies for both stand-alone and embedded applications.	Identification of the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, non-volatile RAM Development of a manufacturable, cost-effective fabrication technology integrable with the process flow for CMOS logic providing for seamless integration onto a CMOS platform
Difficult Challenges <32 nm	
Toward the maturation of CMOS scaling or beyond, discovery, reduction to practice, and implementation into manufacturing of novel, non-CMOS devices and architectures integrable (monolithically, mechanically, or functionally) with a CMOS platform technology. • 1D to extend charge based devices. • Articulate the fundamental physical principles needed to develop new device technologies. • Find a new information processing technology that addresses these fundamental principles (see the section entitled "Fundamental Guiding Principles"). • Make emerging logic and memory devices compatible. (A new logic technology may require a new compatible memory technology.) • Integrate the materials, device and architectural communities to interact and collaborate in discovering a new information processing technology.	No current approaches support the information processing technology required for "Beyond CMOS" satisfying the need for additional decades of functional scaling. Discovery and reduction to practice of new, low-cost methods of manufacturing novel information processing technologies. Any new technology for information processing must be compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A knowledge gap exists between materials behaviors and device functions. Current metrologies examine fixed material states, but do not probe the state change dynamics.

MATERIALS TECHNOLOGIES

The most difficult challenge for Emerging Research Materials is to deliver materials with controlled properties that will enable operation of emerging research devices in high density at the nanometer scale. To improve control of material properties for high-density devices, collaboration and coordination of synthesis with new and improved metrology and modeling must be undertaken. Improved metrology and modeling are needed to guide synthesis in developing material composition and nanostructure to produce materials with controlled, reproducible properties critical to device operation.

Each of the difficult challenges related to materials is crucial to progress in the technologies, and will require significant collaboration between synthesis, characterization, and modeling to enable extraction of critical properties for analysis of the potential performance in different device structures. Improving and optimizing materials requires understanding of the relationship between synthesis conditions, the resulting composition and structure, and how this affects the functional performance of the material. Thus, characterization must be done to establish the relationship between composition, structure, and functional properties and establishing models will help accelerate the optimization of the materials properties. As devices based on these materials are explored, models of the properties may enable evaluation of new device concepts with simulation. As devices are fabricated, different properties may need to be optimized to make them function, so models relating structure and composition to functional properties may accelerate material improvement. As results from controlled well-characterized experiments results are extracted, it would be valuable to establish a knowledge base to accelerate the development of devices, phenomenological models and *ab initio* models for nanometer-scale structured materials. In some cases, required metrology capabilities are research tools and have limited availability, so coupling of critical experiments with the required metrology tools may be challenging.

Table 53 Difficult Challenges—Emerging Research Materials Technologies

Difficult Challenges ≥32 nm	*Summary of Issues*
1D Charge State	Nanotube and nanowire properties, bandgap energy and carrier type, and mobility vary greatly at growth and are controlled by variations in composition, diameter and nanometer scale structure. Nanotubes and nanowires grow in random locations and orientations, which is incompatible with high density memory and logic applications.
Difficult Challenges <32 nm	*Summary of Issues*
Molecular State: Molecules with Controllable, Reproducible Switching Mechanisms	Molecular switching is often highly variable between device lots fabricated with the same chemicals and materials. Contact formation and bond structure may require atomic level control. While groups have been able to fabricate devices that exhibited charge storage, complex interactions have been observed with contact materials and redox reactions, but it is often difficult to determine whether switching and transport are through molecular transport or other mechanisms. No metrology tools are available to measure atomic structure details in carbon-based molecules embedded between two contact layers.
Spin State: Materials that Enable Spin Gain at Room Temperature and Dissipationless Transport	Ferromagnetic (FM) semiconductors only work at low temperatures < 200 K; need a room temperature FM semiconductor. New materials are needed that can enable spin amplification (gain).
Strongly Correlated Electron State	Materials with strongly correlated electron states have unique complex interactions between electric and magnetic properties, with complex ferromagnetic, anti-ferromagnetic phase transitions that may support spontaneous spin precipitation. The challenge is to determine whether these properties can be used to enable new devices at the nanometer scale.
Nanometer Scale Contact and Interface Formation	Materials and processes for establishing interfaces, such as contacts, passivation, etc., must produce interfaces that do not detrimentally affect the state variable or carrier of the state variable, and meet the functional requirements for the device, such as carrier transport. At the nanometer scale, interface materials must have good adhesion, which requires bonding, without detrimentally changing the properties of the device material.
Assembly of Nano-structured Materials	Nanostructure materials such as carbon nanotubes (CNTs) or molecules must be assembled in defined locations with controlled orientation and reproducible properties. (CNTs grow in random locations with random orientations.) Molecules only self-organize on a small number of material surfaces and require thiol functionalization for assembly on Au and defect formation is not understood.

NANO-INFORMATION PROCESSING TAXONOMY

Information processing to accomplish a specific system function, in general, requires several different interactive layers of technologies. A comprehensive list of these layers begins with the required application or system function, leading to system architecture, micro- or nanoarchitecture, circuits, devices, and last would-be materials. As shown in Figure 51 below, a different representation of this hierarchy begins with the lowest physical layer represented by a device and ends with the highest layer represented by a computational model. In this more schematic representation, focused on generic information processing, a fundamental unit of information (e.g., a bit) is represented by a computational state variable, e.g., the position of a bead in the ancient Abacus calculator or the charge or voltage state of a node capacitance in CMOS logic. A device provides the physical means of representing and manipulating a computational state variable among its two or more allowed states. The device is a physical structure resulting from the assemblage of a variety of materials

possessing certain desired properties obtained through exercising a set of fabrication processes. An important layer not shown in this hierarchy is the classes of materials and processes necessary to fabricate the required device structure. Architecture, or in this instance nanoarchitecture, is the physical means of organizing higher level functional primitives formed using devices to represent and enable execution of a computational model. A computational model is the means by which information is processed, e.g., logic, arithmetic, memory, cellular nonlinear network (CNN), or bio-inspired neuromorphic functions using digital, analog,or bio-inspired methods.

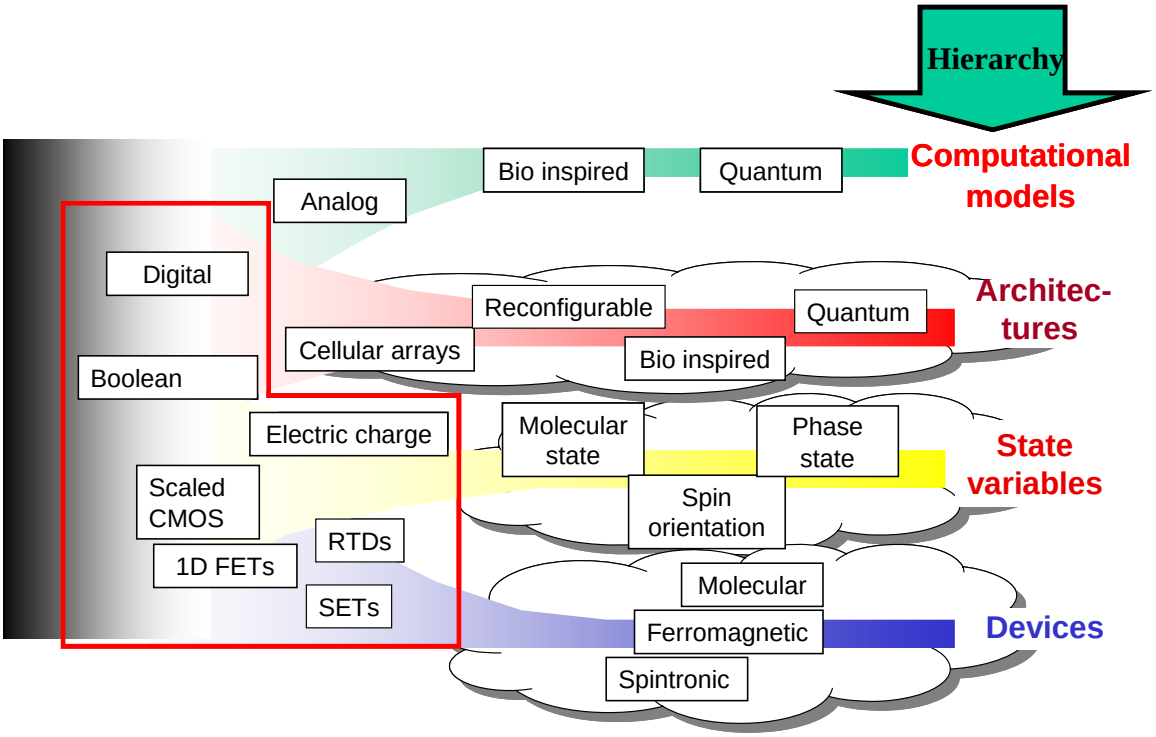

Figure 51 A Taxonomy for Nano Information Processing

The elements shown in the red box represent current CMOS and other technologies based on charge as the computational state variable used in Boolean architecture enabling a digital computational model. The entries to the right of the red box grouped in the four categories summarize possible approaches to new device structures enabling some of the indicated new state variables to achieve the new nano-architectures and computational model. A new information processing technology will likely require an innovative and interactive combination of new elements in each of these layers.

EMERGING RESEARCH DEVICES

MEMORY DEVICES

INTRODUCTION

The memory technologies tabulated in this section are a representative sample of published research efforts (circa 2003-2005) selected to describe some attractive alternative approaches. Historically, very few memory research options yield practical memory devices, and including a particular approach does not in any way constitute advocacy or endorsement. Conversely, not including a particular concept in this section does not in any way constitute rejection of that approach. This listing does point out that existing research efforts are exploring a variety of basic memory mechanisms. These mechanisms include charge isolated by surrounding dielectrics; remnant polarization on a ferroelectric gate dielectric, and resistance change caused by a variety of phenomena. Table 54 is an organization or taxonomy of the existing and emerging memory technologies into four categories. A strong theme is to merge each of these memory options onto a CMOS technology platform in a seamless manner. Fabrication is viewed as modification of or addition to a

CMOS platform technology. A goal is to present the end user with a device that in all ways behaves similar to the familiar silicon memory chip.

Because each of these new approaches attempts to mimic and improve on the capabilities of a present day memory technology, key performance parameters are provided in Table 55 for existing baseline and prototypical memory technologies. These parameters provide relevant benchmarks against which the current and projected performance of each new research memory technology may be compared.

The Emerging Research Memory technology entries in the current version of the Roadmap differ in several respects from the 2003 edition. These changes in technology entries dropped and added to this section are captured in the Transition Table for Emerging Research Memory Devices (Table 56). The changes are: 1) Drop Phase Change Memory; 2) Drop Floating Body DRAM; 3) Drop Single-electron Memory; 4) Add an entry for Ferroelectric FET Memory; and 5) Add an entry for Polymer Memory. The reasons and motivations for these changes are given in the Table 56.

This section is organized around a set of six technology entries shown in the column headers of Table 57. These entries were determined by a systematic survey of the literature to determine the areas of greatest worldwide research activity. Each technology entry listed has several sub-categories of devices that are grouped together to simplify the discussion. Key parameters associated with the technologies are listed in the table. For each parameter, three numbers for performance are given which indicate: 1) minimum performance, satisfactory for practical application, 2) theoretically predicted performance values based on calculations and early experimental demonstrations, 3) up-to-date experimental values of these performance parameters reported in the cited technical references.

The last row in Table 57 contains the number of papers on the particular device technology published in the last two years. It is meant to be a gauge of the amount of research activity currently taking place in the research community and it is a primary metric that determines which of the candidate devices are included in this table. The table has been extensively footnoted and details may be found in the indicated references. The text associated with the table gives a brief summary of the operating principles of each device and as well as significant issues that are not captured in the table.

MEMORY TAXONOMY

Table 54 provides a simple way to categorize memory technologies. In this scheme, equivalent functional elements that make up a cell are identified. For example, the familiar dynamic RAM (DRAM) cell that consists of an access transistor and a capacitor storage node is labeled as a 1 transistor-1 capacitor (1T1C) technology. Other technologies such as magnetic RAM (MRAM) where data is stored as the spin state in a magnetic material can be represented as a 1 transistor-1 resistor (1T1R) technology. Here the resistance "R" indicates that the cell readout is accomplished by sensing the current through the cell. The utility of this form of classification reflects the trend to simplify cells (i.e., reduce cell area) by reducing the number of equivalent elements to a minimum. Thus, early in the development of a given technology it is common to see multi-transistor multi-x (x equals capacitor or resistor) cells. As learning progresses, the structures are scaled down to a producible 1T1x form. The near ideal arrangement is to incorporate the data storage element directly into the transistor structure such that a 1T cell is achieved. In ultra-dense nanoelectronic memory arrays, instead of the transistor "T," a two terminal non-linear diode-like element may be used with a resistive memory element. Such structure is represented as 1 diode-1resistor (1D1R) technology.

An important property that differentiates emerging technologies is whether data can be retained when power is not present. Non-volatile memory offers essential use advantages, and the degree to which non-volatility exists is measured in terms of the length of time that data can be expected to be retained. Volatile memories also have a characteristic retention time that can vary from milliseconds to (for practical purposes) the length of time that power remains on.

Table 54 Memory Taxonomy

Cell Element	*Type*	*Non-volatility*	*Retention Time*
1T1R or 1D1R [A]	**MRAM**	**Non-volatile**	**> 10 years**
	Phase Change Memory	**Non-volatile**	**> 10 years**
	Polymer Memory	**Non-volatile**	**> 10 years**
	Molecular memory	**Non-Volatile**	**> years**
	Insulator Resistance Change Memory	**Non-Volatile**	**> years**
1T1C [A]	**DRAM**	**Volatile**	**~ seconds**
	FeRAM	**Non-volatile**	**> 10 years**
1T [A]	**FB DRAM**	**Volatile**	**< seconds**
	Flash Memory	**Non-volatile**	**> 10 years**
	SONOS	**Non-volatile**	**> 10 years**
	Nano Floating Gate Memory	**Non-volatile**	**> 10 years**
	Engineered Tunnel Barrier Memory	**Non-volatile**	**> 10 years**
	FeFET Memory	**Non-volatile**	**> years**
Multiple T [A]	**SRAM**	**Volatile**	**large**
	STTM [B]	**Volatile**	**small**

Notes for Table 54:
[A] 1T1R—1 transistor–1 resistor 1D1R—1 diode–1 resistor 1T1C—1 transistor–1 capacitor 1T—1 transistor
FB DRAM—floating body DRAM FeFET—ferroelectric FET Multiple T—multiple transistor SONOS—silicon/oxide/nitride/oxide/silicon
[B] STTM—scaleable 2-transistor memory—Yi, J. H., W. S. Kim, S. Song, Y. Khang, H.-J. Kim, J. H. Choi, H. H. Lim, N. I. Lee, K. Fujihara, H.-K. Kang, J. T. Moon, and M. Y. Lee. "Scalable Two-transistor Memory (STTM)," IEDM. (2001) 36.1.1–4.

Table 55 Current Baseline and Prototypical Memory Technologies

		Baseline Technologies					Prototypical Technologies			
		DRAM		SRAM [A]	Floating Gate [B]		SONOS	FeRAM	MRAM	PCM
		Stand-alone	Embed-ded		NOR	NAND				
Storage Mechanism		Charge on a capacitor		Interlocked state of logic gates	Charge on floating gate		Charge in gate insulator	Remanent polarization on a ferroelectric capacitor	Magnetization of ferroelectric contacts	Reversibly changing amorphous and crystalline phases
Cell Elements		1T1C		6T	1T		1T	1T1C	1T1R	1T1R
Feature size F, nm	**2005**	80	130	90	130	130	100	130	180	90
	2018	18	25	18	25	25	20	25	22	18
Cell Area	**2005**	$7.5F^2$	$12F^2$	$140\ F^2$	$10\ F^2$	$5\ F^2$	$7F^2$	$34F^2$	$25F^2$	$7.2F^2$
	2018	$5F^2$	$12F^2$	$140\ F^2$	$10\ F^2$	$5\ F^2$	$5.5F^2$	$16F^2$	$16F^2$	$4.7F^2$
Read Time	**2005**	<15 ns	1 ns	0.4 ns	14 ns	70 ns	14 ns	80 ns [D]	<25 ns [G]	60 ns [I]
	2018	<15 ns	<1 ns	70 ps	2.5 ns	12 ns	2.5 ns	<20 ns [E]	<0.5 ns	< 60 ns
W/E time	**2005**	<15 ns	1 ns	0.4 ns	1 µs/ 10 ms	1 ms/ 0.1 ms	20µs/20ms [J]	15 ns [F]	<25 ns [G]	50/120 ns [I]
	2018	<15 ns	0.2 ns	<0.1 ns	1 µs/ 10 ms	1 ms/ 0.1 ms	~10µs/10ms	1 ns	<0.5 ns [H]	Not known
Retention Time	**2005**	64 ms	64 ms	[C]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
	2018	64 ms	64 ms	[C]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
Write Cycles	**2005**	>3E16	>3E16	>3E16	>1E5	>1E5	1E7	1E13	>1E15	1E12
	2018	>3E16	>3E16	>3E16	>1E5	>1E5	1E9	>1E16	>1E15	1E15
Write operating voltage (V)	**2005**	2.5	2.5	1.2	12	15	5 - 6	0.9 – 3.3	1.8 [G]	3 [I]
	2018	1.5	1.5	0.7	12	15	4.0 – 4.5	0.7 – 1	<1.8	<3
Read operating voltage (V)	**2005**	2.5	2.5	1.2	2.5	2.5	2.5	0.9 – 3.3	1.8 [G]	3
	2018	1.5	1.5	0.8	1.2	1.2	2.5	0.7 – 1	<1.8	<3
Write energy (J/bit)	**2005**	1E-16	1E-16	7E-16	8E-15	8E-15	2E-15	2E-14	1E-10	1E-10
	2018	4E-17	4E-17	2E-17	3E-15	3E-15	3E-16	4E-15	2E-11	Not known
Comments								Destructive read-out	Spin-polarized Write has a potential to lower Write current density and energy [K]	

Notes for Table 55:
[A] High -performance embedded SRAM (see the Embedded Memory Requirements table in the System Drivers Chapter).
[B] Embedded applications (see the Embedded Memory Requirements table in the System Drivers Chapter).
[C] SRAM memory state is preserved so long as voltage is applied.
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[K] Jiang, Y., T. Nozaki, S. Abe, T. Ochiai, A. Hirohata, N. Tezuka, K. Inomata. "Substantial reduction of critical current for magnetization switching in an exchange-biased spin valve", Nature Materials. 3 (2004) 361-364.

Table 56 Transition Table for Emerging Memory Devices

	IN/OUT (Table 64)	*Reason for IN/OUT*	*Comment*
Ferroelectric FET Memory	**IN**	**Based on physics of operation, this memory has potential not realized in existing FeRAM**	**Some features of Nano-Ferroelectric memory: Nanoscale FE capacitor, non-destructive readout**
Polymer Memory	**IN**	**New materials structure, promising characteristics, several recent publications**	**PM is different from MIM memory: it consist of MIMIM structure**
Single-electron memory	**OUT**	**It does not fit any of the application categories**	**Small retention time, slow write, high soft error rate (SER)**
Floating body DRAM	**OUT**	**It became a mature prototypical technology**	**Not presented in PIDS chapter in 2005 ITRS**
PCM	**OUT**	**It became a mature prototypical technology**	**Presented in the 2005 *PIDS chapter***

Table 57 Emerging Research Memory Devices—Demonstrated and Projected Parameters

		Nano-floating Gate Memory [A]	Engineered Tunnel Barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	*Polymer* Memory	Molecular Memories
Storage Mechanism		Charge on floating gate	Charge on floating gate	Remanent polarization on a ferroelectric gate dielectric	Multiple mechanisms	Not known	Not known
Cell Elements		1T	1T	1T	1T1R or 1R	1T1R or 1R	1T1R or 1R
Device Types		1 Nanocrystal 2 Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-I-M 2 Solid Electrolyte 3 FE tunneling 4 FE Schottky diode 5 FE-I-FE	M-I-M (nc)-I-M	Bi-stable switch
Feature size F	Minimum required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	25 nm	10 nm [H]	22 nm [K]	5–10 nm [O]	5–10 nm	5–10 nm [AA]
	Demonstrated	90 nm [A]	180 nm [I]	~10 μm [L]	100 nm [P]	200 μm [W]	30 nm [AB]
Cell Area	Minimum required	$10F^2$	$10\ F^2$	$8F^2$	$10\ F^2$	$10\ F^2$	$10\ F^2$
	Best projected	$8–10F^2$	$8F^2$ [H]	$8F^2$	$8/5F^2$ [Q]	$8/5F^2$	$5F^2$
	Demonstrated	$16F^2$ [A]	Data not available	Data not available	Data not available	Data not available	Data not available
Read Time	Minimum required	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns
	Best projected	2.5 ns	2.5 ns	2.5 ns	<10 ns	<10 ns	<10 ns [AA]
	Demonstrated	20 ns [B]	20 ns [B]	20 ns [B]	2 ms [R]	~10 ns [X]	Data not available
W/E time	Minimum required	1 μs/10 ms	1 μs/10 ms	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	1 μs/10 ms	1 ns at 9V[H]	2.5 ns [B]	<20 ns [P]	Not known	<40 ns [AA]
	Demonstrated	W: 1–10 μs [C] E: 10–100 ms [D]	E: ~10 ms [I]	500 ns [L]	25 ns [P]	<10 ns [X]	~sec [AC]
Retention Time	Minimum required	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
	Best projected	>10 y	>10 y	>1y	>10 y	Not known	Not known
	Demonstrated	>200 hours [E]	>10 y [I]	30 days [M]	1 y [S]	6 month [Y]	2 months [AC]
Write Cycles	Minimum required	>1E5	>1E5	>1E5	>1E5	>1E5	>1E5
	Best projected	>1E5	>3E16	>3E16	>3E16	>3E16	>3E16
	Demonstrated	>1E4 [A]	5E4 [J]	1E12 [O]	1E5 [T]	>1E6 [X]	>2E3 [AD]
Write Operating Voltage (V)	Minimum required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	>3 V [F]	>3 V [F]	<0.9 V [K]	<0.5 V [U]	Not known	2 V [AE]
	Demonstrated	±6 [A]	6.5 [I]	±6 [O]	0.24 V [P]	~±2 [X]	~±1.5 V [AB]
Read Operating Voltage (V)	Min. required	2.5	2.5	2.5	2.5	2.5	2.5
	Best projected	0.7	0.7	0.7	<0.2 V [U]	0.7	0.3 [AA]
	Demonstrated	2.5 [B]	2.5 [B]	2.5 [B]	~0.2 V[P]	~1 [X]	0.5 [AB]
Write Energy (J/bit)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	5E-16 [G]	5E-16 [G]	2E-15 [N]	1E-15 [V]	Not known	2E-14 [AA]
	Demonstrated	2E-15 [G]	Data not available	Data not available	5E-14 [P]	1E-13 [Z]	Data not available
Comments		A natural evolution of the floating gate memory		Potential for non-destructive readout	Low read voltage presents a problem		
Research activity [AE]		123	12	74	39	25	68

[A] For consistency, all numbers representing the nanofloating gate memory refer to one source and one type of memory: Freescale nanocrystal memory, NOR architecture—Muralidhar, R., et al., "A 6V Embedded Silicon Nanocrystal Nonvolatile Memory for the 90 nm Technology Node,", IEDM Digest. (2003).

[B] Based on floating gate and SONOS data (see Table 55). The read voltage and read time of all 1T memory devices are expected to be similar .

[C] Hot electrom injection—Muralidhar, R., et al. "A 6V Embedded Silicon Nanocrystal Nonvolatile Memory for the 90 nm Technology Node," IEDM Digest. (2003).

[D] Fowler-Nordheim injection—Muralidhar, R., et al. "A 6V Embedded Silicon Nanocrystal Nonvolatile Memory for the 90 nm Technology Node," IEDM Digest. (2003).

[E] Experimentally, retention >200 h was observed. The number in the table is projected based on experimental data and first-principle modeling—Muralidhar, R., et al. "A 6V Embedded Silicon Nanocrystal Nonvolatile Memory for the 90 nm Technology Node," IEDM Digest. (2003).

[F] Based on minimum barrier height of 1.5 eV for non-volatile charge retention.

[G] Calculation is based on the max. program voltage and interconnect capacitance – see Note [6] to the Embedded Memory Requirements table in the System Drivers chapter).

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[N] Calculated based on the parameters of scaled FE capacitor projected in Ref. [K].

[O Estimation is based on conductive pad size (for max ON resistance of 10 kOhms) plus insulation distance from neighbouring cells.

[P] Kozicki, M. N., M. Mitkova, M. Park, M. Balakrishnan, and C. Gopalan. "Information storage using nanoscale electrodeposition of metal in solid electrolytes," Superlat. and Microstr. 34 (2003) 459–465.

[Q] $8F^2$ for 1T1R, $5F^2$ for 1R cells.

[R] Beck, A., J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer. "Reproducible Switching Effect in Thin Oxide Films for Memory Applications," Appl. Phys. Lett. 77 (2000) 139.

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[U] Electrochemical cell potentials control the write voltage. In appropriate combinations, 0.5 V will leave some safety margin. Read voltages will be significantly smaller.

[V] Estimated as $E \sim 0.5 * V^2 / R_{ON} * t_w$ for V=0.2 Volts, R_{ON}=2E5 Ohm , t_w=10 ns.

[W] Ouyang. J., C. W. Chu, C. R. Szmanda, L. P. Ma, and Y. Yang. "Programmable polymer thin film and non-volatile memory device", Nature Materials. 3.12 (2004) 918–922.

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[Z] Estimated based on experimental data reported in Ref. [AB]: $E \sim 0.5 * V^2 * I_{ON} * t_w$, for V_{ON}=2 Volts, I_{ON}=10μA , t_w=10 ns.

[AA] DeHon, A., S. C. Goldstein, P. J. Kuekes, P. Lincoln. "Nonphotolithographic nanoscale memory density prospects," IEEE Trans. Nanotechnology. 4.2 (2005) 215–228.

[AB] Wu, W., G-Y. Jung, D. L. Olynick, J. Straznicky, Z. Li, X. Li, D. A. A. Ohlberg, Y. Chen, S-Y. Wang, J. A. Liddle, W. M. Tong, and R. S. Williams. "One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography," Appl. Phys. A, 80 (2005) 1173–1178.

[AC] Chen Y., D. A. A. Ohlberg, X. M. Li, D. R. Stewart, R. S. Williams, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, D. L. Olynick, E. Anderson, "Nanoscale Molecular-switch Devices Fabricated by Imprint Lithography," Appl. Phys. Lett 82 (2003) 1610.

[AD] Wu, W., G-Y. Jung, D. L. Olynick, J. Straznicky, Z. Li, X. Li, D. A. A. Ohlberg, Y. Chen, S-Y. Wang, J. A. Liddle, W. M. Tong, and R. S. Williams. "One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography," Appl. Phys. A. 80 (2005) 1173–1178

[AE] The number of referred articles in technical journals that appeared in the Science Citation Index database for 7/1/2003–7/1/2005.

MEMORY DEVICES—DEFINITION AND DISCUSSION OF TABLE ENTRIES

Nanofloating gate memory (NFGM)—NFGM includes several possible evolutions of conventional floating gate and SONOS memories. There are two major approaches proposed to improve the performance of floating gate memory cells: 1) discrete-trap storage node with charge injection by hot carrier injection and Fowler-Nordheim (F-N) tunneling[1], 2) discrete-trap storage node with charge injection by direct tunneling.[2] Nanocrystal memory devices mitigate charge loss from storage layer to underlying oxide by storing charge in electrically isolated nanocrystals. For tunnel oxide thicknesses <35A, these devices may be programmed and erased by quantum mechanical direct tunneling. For larger tunnel oxide thicknesses required typically for non-volatile applications, charge may be injected using hot electron injection and erased by Fowler-Nordheim tunneling. While most studies have been performed with silicon nanocrystals, nanocrystals of other suitably chosen materials with appropriate conduction band offset to oxide can be chosen to optimize device performance.

In the NFGM with discrete-trap storage node, the floating gate consists of multiple nanocrystal dots or charge-trapping defects in insulator.[3] The multiple floating dots are separated and independent and electrons are injected to the dots via different paths. The retention time can be improved in the discrete-trap memory. Because the nano floating gate device mitigates charge loss to local tunnel oxide defects, it permits scaling of tunnel oxide from about 10 nm for floating gate technology to about 5 nm. This in turn scales the operating power supply voltages from about 9V to about 6V.[4]

It should be noted that NFGM is a natural evolution of the conventional floating gate memory and NFGM offers only marginal improvements in the operation parameters (see Tables 55 and 57). It may be impossible to match their speed and voltages to e.g., logic devices.

Engineered tunnel barrier memory includes graded (e.g., "crested") barrier floating gate memory[5, 6] and variable oxide thickness floating gate memory (VARIOT).[7] The graded barrier concept uses a stack of insulating materials to create a special shape of barrier enabling effective tunneling into and out of the storage node. The concept of a floating gate with graded tunnel barrier is very attractive, however the realization of layered dielectric tunnel barrier is very difficult. This requires new dielectric materials with graded bandgap and dielectric constant The concept of graded dielectric electronic materials is analogous to the graded III-V heterostructures. It is noteworthy that graded $Al_xGa_{1-x}As/GaAs$ structure was used to fabricate graded charge injection barrier,[8] the experimentally demonstrated predecessor of the graded injection barrier memory concept discussed above. The crested tunnel barrier stack structure $Si_3N_4/SiO_2/Si_3N_4$ was experimentally investigated and an improvement of its NVM characteristics was reported[9]. Also, there were recent studies of AlO_x and HfO_2[10, 11] layers as a possible candidate for the graded tunneling barrier.

In the VARIOT memory, a dual-layer dielectric stack with two different dielectric constants is used. This structure allows a high tunneling current at relatively low applied voltage while providing good data retention. Using an engineered tunneling barrier allows lowering the voltage necessary to program or erase the memory cell. Stacks consisting of SiO_2 and HfO_2 or Al_2O_3 have been experimentally studied, and they demonstrated lower voltage programming by tunneling and ten years of data retention.

Ferroelectric FET Memory—Conventional 1T1C ferroelectric RAM (FeRAM) require switchable polarization charges in the same order as charges stored on a DRAM cell capacitor. This leads to the necessity of 3D folded ferroelectric capacitor and limits the scalability to due the capacitor area requirements. In contrast, if the ferroelectric capacitors is integrated into the gate stack of a FET, the ferroelectric polarization directly affects charges in the channel and leads to a defined shift of the input characteristics of the FET. This 1T memory device is called ferroelectric FET (FeFET).[12] At the channel interface, a high quality insulator will still be required to guarantee a low interface state density. Hence, the device realistically shows a metal-ferroelectric-insulator-semiconductor (MFIS) gate stack. Sometimes, another metal layer is introduced between the ferroelectrics and the insulator (MFMIS). The FeFET device scales as a MOSFET. However, scaling is projected to end approximately with 22 nm, because the insulation layer becomes too thin and the properties of the ferroelectrics with respect to thickness dependence of the coercitive field will not allow further reduction.[13] In the last decade, many attempts have been made to fabricate FeFET-based non-volatile memories. The major challenge turned out to be the low retention time of the device, obviously caused by leakage charges which screen the ferroelectric polarization charges. Recently, significant improvements in the retention time have been reported.[14, 15] Other reliability issues such as fatigue and imprint are not yet thoroughly studied and understood.

Insulator Resistance Change Memory—A range of metal-insulator-metal (MIM) systems show electrical pulse induced resistance change effects. The mechanisms behind this effect can be grouped into the following categories:

1) Redox processes involving the electrode material or the insulator material, or both. The insulator needs to exhibit an ion conductivity. The material class is comprised of oxides, higher chalcogenides (including glasses), semiconductors, as well as organic compounds including polymers. One variant is based on the cation transport, the cathodic reduction, and the growth of metallic filaments. Primarily Ag- and Cu- based systems have been successfully realized in demonstrator cells.[16, 17] A filament thus formed connecting opposite electrodes leads to a low-resistance state, while oxidation dissolves the filament and restores the high-resistance state. Other variants originate from redox reactions that introduce an electronic conduction within the insulator material itself.[18, 19, 20] In most cases, a formation process is required before the bi-stable switching can be started. Often, the conduction is of filamentary nature. If this effect can be controlled, memories based on this bi-stable switching process can be scaled to very low feature sizes. The switching speed is limited by the ion transport. If the active distance that is relevant for the redox controlled bi-stable switching is small (in the < 10 nm regime) the switching time can be as low as a few nanoseconds. Precise predictions are not yet possible, because the details of the mechanism of the reported phenomena are still unknown.

2) Ferroelectric polarization effects. It is conceivable that the ferroelectric polarization modifies the tunneling properties of ultrathin films or modifies the Schottky-type space-charge layer in adjacent semiconducting layers.[21, 22] Several studies have been reported in the literature. The basic component of this memory is a MIM structure, using insulators, such as Cr-doped (Ba, Sr)TiO_3 or $SrZrO_3$,[23, 24, 25, 26] that show reproducible hysteresis in the leakage current. The write operation is performed by applying different voltages to the MIM structure, which results in reversible switching between a low-resistance and a high-resistance state. Multilevel switching can be achieved in this structure. Data is read by measuring resistance of the MIM structures at the voltages lower than the write voltages (typically the read voltage is less than 0.5 V.). The retention time of such MIM structure can be quite large—1-year retention was experimentally demonstrated. While stable and reproducible hysteresis was reported in MIM structures, a practical memory cell integrated with a sense transistor has not been demonstrated. At present, the ferroelectric origin of the observed switching phenomena was not definitely confirmed. In some cases, evidences for reversible formation/annihilation of conducting filaments were reported.[27]

Polymer Memory—The memory element is a thin-film, organic/metal/organic, triple-layer structure between two metal electrodes. One example of the organic material is 2-amino-4, 5-imidazoledicarbonitrile.[28, 29, 30, 31, 32] Polymer memory utilizes the effect of electrical bistability in such triple-layer: The structure can exhibit two states of different conductivities at the same applied voltage. The WRITE operation is performed by applying a voltage pulse to the structure, which results in reversible switching between a low-resistance and a high-resistance state. The ratio of the conductivities achieved between the two states was reported to be about 10^4. After transition occurs, the device remains in one of two states after turning off the power. The ERASE operation is performed by application of a reverse voltage pulse. A switching time of 10 ns was reported.

The major difference between the polymer memory and other electrically bistable resistive memory elements, such as insulator resistance change memory and molecular memory is the presence of the embedded metal layer within the organic films. Experimental results indicate that the embedded metal layer plays a critical role in bistable *I–V* characteristics of the polymer memory element.[28] Later, it was found that the embedded metal layer is electrically discontinuous, i.e., it consists of discrete metal nanoparticles. The operation mechanism of the polymer memory is still unclear. It does not appear to be associated with the formation of conducting filaments, as in the case of the Insulator resistance change memory and molecular memory. Other researchers[33] suggested that the mechanism of bistabilitry could be explained by the Simmons-Verderber theory,[34] according to which the changes in resistance are due to trapping the charge in the discrete metal nanocrystals. Recently, it was reported that a single-layer polymer M-I-M structure demonstrates similar behavior.[35]

Molecular Memory—Molecular memory is a broad term encompassing different proposals for using individual molecules as building blocks of memory cells in which one bit of information can be stored in the space of an atom or a molecule. One experimentally demonstrated approach is based on rapid reversible change of effective conductance of a molecule attached between two electrodes controlled by applied voltage.[36, 37, 38, 39] In this molecular memory data are stored by applying an external voltage that causes the transition of the molecule into one of two possible conduction states. Data is read by measuring resistance changes in the molecular cell. There are also concepts for combining molecular components with current memory technology, such as DRAM[40] and floating gate memory. The mechanism of conductivity switching in molecules is not completely understood. Some of the earlier reported experimental results on electron transport through molecules were found to be due to formation of metal filaments along the molecule attached between two metal electrodes.[41] The knowledge base of molecular electronics needs further work.

LOGIC DEVICES

INTRODUCTION

The dimensional scaling of CMOS device and process technology, as it is known today, will become much more difficult as the industry approaches 16 nm (6 nm physical channel length) around the year 2019 and will eventually approach an asymptotic end. Beyond this period of traditional CMOS scaling, it may be possible to continue functional scaling by integrating alternative electronic devices on to a silicon platform. These alternative electronic devices include, 1D structures (such as CNTs and compound semiconductor nanowires), RTDs, SETs, molecular and spin devices, all of which are discussed in this chapter. Most likely, these options will unfold their full potential only in combination with new and appropriate nanoarchitectures (see the *Architecture section* for a definition of nanoarchitecture).

However, these concepts still represent charge-based logic, and their scaling is fundamentally restricted by the thermodynamic limit concerning the minimum switching energy per binary operation. Beyond this limit, the grand challenge, then, is to invent and develop one or more new technologies based on something other than electronic charge that will extend the scaling of information processing technologies through multiple generations and several orders of magnitude in performance. These alternatives may include ferromagnetic logic and spin gain devices, as discussed here, and others yet to be determined. This is further discussed in the section below titled "*Emerging Technologies—A Critical Review," in the section "Technonologies beyond CMOS."*

Undoubtedly, there will be opportunities for innovation and invention to extend CMOS devices and the ultimate scaling of CMOS is the focus of intense research and development activities. These ultimate CMOS devices may be integrated with alternative electronic devices in novel and productive ways. However these advanced electronic technologies should be thought of as transitional technologies that will form a bridge to new, yet to be discovered, scalable approaches.

Such new technologies must meet certain operational requirements and possess certain compelling attributes to justify the very substantial investments that will be necessary to build a new infrastructure. First and foremost, any new information processing technology must provide the following:

1. Extend microelectronics orders of magnitude beyond the domain of CMOS and be capable of integration on or with a CMOS platform. This will require several of the following:
    - Functionally scaleable by several orders of magnitude beyond CMOS
    - High information/signal processing rate and throughput
    - Energy dissipation per functional operation substantially less than CMOS
    - Minimum scaleable cost per function
2. Room temperature operation.
3. Provide a means for an energy restorative functional process to sustain steady state operation (e.g., in traditional devices provide a gain mechanism.).

In the last section titled, "*Fundamental Guiding Principles*," a set of principles is proposed for consideration in exploring new "beyond CMOS" technologies for information processing.

The technology entries in the current version of the Roadmap differ in several respects from the 2003 edition. These changes are captured in the Transition Table for Emerging Logic devices (Table 58). The changes are: 1) Drop RSFQ from the section; 2) Add an entry for ferromagnetic logic; and 3) Drop E: QCA from this section. The reasons and motivations for these changes are given in the table.

This section is organized around a set of six technology entries shown in the column headers of Table 59. These entries were determined by a systematic survey of the literature to determine the areas of greatest worldwide research activity. Each of the technology entries listed has several sub-categories of devices that were grouped together to simplify the discussion. Key parameters associated with the technologies are listed in the table. For each parameter, two numbers are given which indicate currently measured experimental values and theoretically predicted values, respectively.

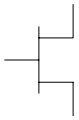
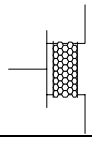
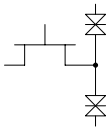
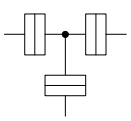
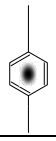
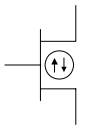
The last row in Table 59 contains the number of papers published in the last two years on the particular device technology. It is meant to be a gauge of the amount of research activity currently taking place in the research community and it is a primary metric that determines which of the candidate devices are included in this table. The table has been

extensively footnoted and details may be found in the indicated references. The text associated with the table gives a brief summary of the operating principles of each device and as well as significant issues that are not captured in the table.

Table 58 Transition Table for Emerging Logic Devices

	IN/OUT	*Reason for IN/OUT*	*Comment*
Ferromagnetic logic	**IN**	**Proposed ferromagnetic logic devices offer some new opportunities such as nonvolatility and re-configurability**	
RSFQ	**OUT**	**RSFQ is in production**	**Current assessment is that RSFQ will address several important specific applications that are beyond the scope of ITRS.**
E: QCA	**OUT**	**E:QCA does not fit any of the application categories**	**Slow operation, low temperatures are needed, M:QCA are addressed in *ferromagnetic logic*, molecular QCA are addressed in *molecular logic.***

Table 59 Emerging Research Logic Devices—Demonstrated Projected Parameters

Device								
		FET [B]	1D structures	Resonant Tunneling Devices	SET	Molecular	Ferromagnetic logic	Spin transistor
Types		Si CMOS	CNT FET NW FET NW hetero-structures Crossbar nanostructure	RTD-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin transistor
Supported Architectures		Conventional	Conventional and Cross-bar	Conventional and CNN	CNN	Cross-bar and QCA	CNN Reconfigure logic and QCA	Conventional
Cell Size (spatial pitch)	Projected	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [D]	3μm [H]	~700 nm [M]	~2μm [R]	250 nm [V, W]	100 μm [X]
Density (device/cm^2)	Projected	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	Projected	3E-18	3E-18	>3E-18	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	3E-7 [R]	6E-18 [W]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238 [C]	238 [C]	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	0.1	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	4.2 – 300 K	20 K [L]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	III-V Si-Ge	III-V Si	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research activity [A]			171	88	65	204	25	102

Notes for Table 58:

[A] The number of articles in technical journals that appeared in the Science Citation Index database for July 2003 – July 2005.

[B] For Si CMOS entry, parameters of high-performance MPU are used: "projected" (2020) and "demonstrated" (2005).

[C] Size and circuit speed scaling of these structures is the same as the scaling of MOSFETs.

[D] Appenzeller, J., Y.-M. Lin, J. Knoch, and P. Avouris. "Band-to-band tunneling in Carbon Nanotube Field-Effect Transistors," Phys. Rev. Lett. 93.19 (2003) 196805.

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[L] For SET logic circuits, device size/density, circuit speed, switching energy and operational temperature are interdependent. The values in the table were derived for a complex circuit operating at 1 GHz: Chen, R. H., A. N. Korotkov, and K. K. Likharev. "Single-electron transistor logic," Appl. Phys. Lett. 68.14 (1996) 1954.

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[N] In REF [M], the reported number of 2 THz for "intrinsic speed" of an experimental SET was derived from capacitance measurements, and not from experimental time-dependent characteristics.

[O] The value in the [ ] is the value that includes cooling energy. If an ideal Carnot refrigerator is used for cooling to the operation temperature T_c, the total switching energy $E_{sw} > E_c \cdot \frac{300}{T_c}$, where E_c is the net switching energy, when cooling energy is not taken into account.

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[R] Kuekes, P. J., D. R. Stewart, and R. S. Williams, "The crossbar latch: Logic value storage, restoration and inversion in crossbar circuits," Journal of Applied Physics. 93 (2005) 034301.

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LOGIC DEVICES—DEFINITION AND DISCUSSION OF TABLE ENTRIES

1D structures (Carbon Nanotubes and Nanowires)—The 2003 ITRS ERD chapter surveyed all the technology entries and found that 1D structures had greater potential impact on scaled nanoelectronics than any of the other entries even though the difficulties associated with their introduction into high volume manufacturing were still judged to be very great. Since then, the research activity in this area has matured to the point where one can identify the critical problems associated with 1D structures. The activities have centered around four main poles: 1) understand the basic physical mechanisms at work in quantum-confined transport including coherent transport; 2) synthesize nanotubes and nanowire materials with predictable and controllable characteristics; 3) address device fabrication issues like placement, contacting, doping, dielectric and gate material integration issues; and lastly, 4) characterize device issues such as transport efficiency, subthreshold slope, ambipolar conduction, RF response, I_{ON}/I_{OFF} ratios and others. An important issue related to application of 1D structures in MOSFETs is the need to place several such structures in parallel in a single device to obtain sufficient drain current needed to drive the capacitance of multiple load gates. This section seeks to briefly summarize the state of knowledge, provide pointers to the recent work in each of these four areas, and discuss remaining issues gating their application. The *Emerging Research Materials* section of this chapter provides additional discussion of the materials issues related to 1D structures.

Recent research into the physics of quantum-confined electron transport has focused on two areas. The first is to understand the effect of quantum confinement on electron mobility at realistic temperatures and bias conditions and the second is to evaluate the possibility of highly efficient coherent interference logic devices. The earlier expectation that mobility would increase because of a decreased density of states[42] has been supplemented with a more recent calculation that reaches the opposite conclusion.[43] A careful multiband calculation at room temperature with realistic material interfaces shows that mobility will decrease because of increased overlap of the electron and phonon wavefunctions. The definitive experiment has not yet been done. Coherent electron transport in 1D devices can, in principle, be operated in the terahertz (THz) range.[44] However such devices appear extremely impractical due to extreme lithographic precision, low operating temperatures, and the Fermionic nature of electrons that limits the total current in quantum confined structures.[45]

Significant progress has been made in the synthesis of nanotubes with controllable properties through the use of plasma enhanced chemical vapor deposition (PECVD). It is now possible to reliably produce nanotubes over 90% of which have semiconductor properties. While this is a long way from the purity requirements in manufacturing settings, it does represent significant progress. Again, this is discussed further in the Materials section of this chapter.

One of the fabrication challenges associated with CNT FETS is reliable positioning and growth of nanotubes at lithographically defined sites. Recently reported results have demonstrated catalyzed growth with a 2 nm placement accuracy.[46] The technique uses state-of-the-art E-beam lithography supplemented by an angled deposition technique of mono-disperse catalytic particles to achieve the high accuracy. Subsequent growth of CNTs at the particle sites achieves over 90% growth coverage. Another CNT-FET fabrication issue has been reliable *in situ* doping (especially P type doping). A novel scheme that combines chemical and electrostatic doping in a dual gate configuration allows operation as either a P-FET or N-FET under electrostatic control.[47] Progress in high-κ gate dielectrics and associated gate materials can be found in several references including the reference listed in the Endnotes section at the end of this chapter.[48] The quality of CNTs has improved to the point that the measured acoustic phonon mean free path is approximately 300 nm and the optical phonon mean free path is 15 nm.[49]

Direct measurement of the AC response of CNT FETS has been difficult using conventional techniques due to the small on-current in the range of 1 μA into a 50 Ω load. Recent results have demonstrated a broadband measurement technique that allows direct measurement up to 200 MHz.[50] Ambipolar conduction in Schottkey barrier CNT FETs is a significant impediment to general adoption because it limits I_{ON} to I_{OFF} ratios to unacceptably low values.

Resonant tunneling devices[51, 52]—Resonant tunneling devices for logic applications include resonant tunnel transistors (RTT) and hybrid devices incorporating resonant tunneling diodes and one or more FETs (RTD-FET). The RTDs are two terminal devices that intrinsically have a very high switching speed and exhibit a region of negative differential resistance in their I-V curves. These two characteristics make them potentially attractive as high speed switching devices. If two RTDs are connected in series, they have two stable operating points and can switch between the two stable points very quickly if a third terminal is added that can act as a gate. However, since the peak current through an RTD depends exponentially on the barrier thickness, it is inherently difficult to get reproducible device operation unless the gate also controls the peak current. Controlling the peak current is usually done by integrating a transistor with the series-

connected double RTDs on a common substrate.[53] This approach results in complex, epitaxially grown structures requiring very good control of film thicknesses.

Integration of a transistor with a pair of RTDs introduces delays to the inherently fast bistable switching times associated with capacitive charging and discharging of the transistor gate stack. The operational speed of the integrated device can be an order of magnitude slower than the intrinsic switching speeds of the RTDs themselves. Additional challenges include a limited I_{ON}/I_{OFF} ratio of 10 rather than the factor of 10^5 that CMOS digital circuit designers require and the inherent complexity of the integrated structure, which limits the dimensional scaling of the devices. The complexity of the hybrid devices makes them large with experimental spatial pitch values of order 3 μm being reported. Another issue is fabrication of silicon or silicon-germanium tunnel diodes with high peak-to-valley ratios.

Adding a control terminal to RTDs extends their usability to a variety of applications. This approach has been used to build resonant tunneling transistors.[54] RTTs have a negative transconductance that can be used in several logic circuits, e.g., in XOR gate with only one transistor.[55]

Traditionally, RTDs have been fabricated in III-V material systems that has limited their widespread applicability. Recently, several papers have described fabrication of group IV devices with Si compatible materials. These include a tri-state logic device fabricated in SiGe[56] and a Si-based field-induced band-to-band tunneling transistor.[57] Although these devices continue to have all the issues outlined above, fabrication in a Si compatible material structure substantially reduces the integration challenges.

Multi-valued logic circuits based on Si resonant tunneling MOS transistors (SRTMOS) were theoretically explored.[58] This theoretical analysis assumed that the SRTMOS has an ON current density of the order of 10^6 A/cm^2 and the I_{ON}/I_{OFF} ratio larger than 10^4. At this point, no experimental demonstration of resonant tunnel devices with both high current and high I_{ON}/I_{OFF} ratio is known.

A number of recent works explore the spin-polarized resonant tunneling, which could be useful for application in spintronic devices.[59, 60, 61] Another potential niche application for RTDs is in photodetectors for detection of single photons with low dark count rates and high efficiency.[62]

Overall, the resonant tunneling devices may be useful for certain niche applications requiring high speed and low dynamic range and low peak currents provided the manufacturing issues associated with uniformity of the tunneling barrier can be resolved. The principle focus of recent research activity involving RTDs has been in the area of integration on the silicon platform.

Single-electron transistors (SETs)—SETs[63] are three-terminal switching devices that can transfer electrons from source to drain one by one. Potentially, they can deliver high device density and power efficiency at good speed if the issues of noise immunity and low fanout can be solved.

The structure of SETs is almost the same as that of FETs. The important difference, however, is that in a SET the channel is separated from source and drain by tunneling junctions, and the role of channel is played by a quantum dot. Operational parameters of SETs depend on the size of the quantum dot. Single-electron devices operating at room temperature were experimentally demonstrated.[64, 65] However, operation of complex and fast SET logic circuits is generally limited to very low temperatures due to low noise immunity. Estimates[66] of the logic gate parameters, based on 2 nm SETs, are maximum operation temperature T~20 K, integration density n~10^{11} cm^{-2}, and speed of the order of 1 GHz.

There are two operational modes for implementing logic operations with single-electron devices. The first approach is to represent one bit by a single electron (bit state logic) and use a SET to transfer electrons one by one. In the second approach, each bit is represented by more than one electron that charges a capacitor, (voltage state logic) to a particular voltage. The voltage state logic approach is in general more robust but less power efficient.

SET logic circuits suffer from low noise immunity and limited fan-out relative to conventional MOSFET logic circuits. The low error immunity is due to the influence of stray charge but will be common to all nanoelectronic devices of similar scale. Similarly, the limited fan-out is a direct consequence of dealing with only a single electron.

Low error tolerance and low fan-out make it difficult for SETs to compete directly with CMOS devices used to implement Boolean logic operations. Therefore, it is important to develop applications and architectures that exploit the unique functionality of SET devices in an optimal way. Programmable SET logic and multi-value logic are examples of

possible functionality improvement by utilization of SETs. Utilization of the periodic nature of the SET I-V characteristic to implement "turnstile logic" is another example. Also, SET/FET hybrid circuits, where silicon-based single-electron logic elements are combined with MOSFETs show some promise.[67] Massive arrays of SETs may be used to implement associative recognitions tasks[68] connected with human cognition.

Molecular devices—The concept of molecular electronic devices is based on electronic properties of individual molecules tailored to perform logic operations and on the assembly of a large number of these functional building blocks into molecular circuits. Logic functions can be provided by electron transport and controlled switching behaviour of the molecules and may involve designated energy levels and charge states. Two-terminal devices such as resistive switches as well as three-terminal devices such as gated, transistor-like molecules are envisioned. The integration of these molecules into circuits requires the fabrication of contacts with atomic level precision and involves organic or inorganic interconnects on the nanometer scale.

The potential of this concept originates from a variety of aspects: 1) through chemical synthesis, the electronic properties of organic molecules may be tailored within a wide range; 2) the reproducibility between organic molecular units is perfect, in contrast to inorganic nanoclusters; 3) chemically induced self-organization processes may be exploited to assist the formation of near-perfect, highly regular molecular circuits; 4) very high device densities may be achieved. Since the size of complex molecules is in the order of approximately 1 nm, the limit will probably be determined by the size of the interconnect elements and the required spacing between the functional molecules in order to prevent undesired tunneling processes. Ultimate limits greater than 10^{12} cm^{-2} are certainly conceivable; 5) Due to the small number of electrons required for molecular switching processes, in combination with suitably low voltages, the switching energy may be significantly reduced compared to values for extended CMOS technology and may approach the thermodynamic limit, and 6) the speed of molecular devices is limited by elementary processes related to the transport and switching operation. Typically these processes will be a change of the molecular configuration, e.g., twisting vibrations or intramolecular charge transfer processes. The speed will very much depend on the specific nature of the process, but may reach into the > 1 THz regime. It should be noted that the speed of molecular circuits is expected to be much lower since it is limited by the transmission probability through the contacts and interconnects and by charging effects that correspond to the RC time delays of conventional circuits.

Many attempts have been made to build and characterize single molecular electronic devices, mainly since the mid-1990s. Molecular functions that have been reported include rectification,[69, 70, 71] controlled conduction through gating,[72, 73, 74] as well as switching.[75, 76] Typically, these results have been obtained in mechanical break junction experiments or by scanning probe techniques.

There have also been several reports about the integration of monomolecular films into crossing points of electrodes that showed resistive switching with high R_{OFF}/R_{ON} ratios[77] or negative differential resistance behaviour with high peak-to-valley ratios.[78] Detailed studies suggest, however, that many of these earlier reported experimental results on integrated films do not reflect the property of the organic molecules. Instead, the switching is probably caused by either redox processes involving the electrode material[79] or the formation and dissolution of metallic nanofilaments.[80] This is discussed further in the *Materials* section.

Experimental studies conducted to date have revealed the large number of challenges that have to be overcome before molecular electronics can be implemented. Major challenges include the realization of reproducible contacts to molecular building blocks that show sufficient electron transmission. Other challenges are the design of suitable interconnects and the interface to the outside world, the standard nano- and microelectronic pad sizes and signal levels. The stability of the molecular materials themselves through many cycles (~10^{10}) and through thermal processing cycles typical of CMOS processing also remains a very significant challenge. The design of molecular devices and circuits will be much more complex than today. This is because one has to take into account the fact that the electronic properties of the functional molecules, the contacts, and the interconnects are strongly coupled and cannot be treated separately as in conventional CMOS circuits.

Novel architectures are required to exploit the full potential of the concept of molecular electronics.[81, 82] These architectures need to incorporate memory and logic in very close proximity, in order to reduce the CV^2 switching losses. In addition, the novel architectures will have to be very defect-tolerant relative to today's CMOS circuits.

Beyond the paradigm of charge-based logic, organic molecules also might be employed to realize molecular magnets that might be used to control and manipulate the spin degree of freedom, independent of any charge transfer, within the concepts of spintronics.

Ferromagntic Logic Devices—Ferromagnetic logic devices are a class of alternative logic devices that use the local ferromagnetic orientation of a ferromagnetic material system such as Fe, Ni, or Co to store the computational state. All the devices in this class have the property of being non-volatile, radiation hard, and operating at room temperature that is derived from the properties of the ferromagnetic materials themselves. Examples of ferromagnetic logic devices are moving domain wall, (MDW)[83] and magnetic QCA (M:QCA).[84] The MDW device relies on the fact that the magnetic field present in segments of ferromagnetic strips points parallel to the strip because of the topological anisotropy of the wire. The strip will spontaneously segment itself into local nanodomains separated by domain walls. If the magnetic field vectors at a given domain wall meet head to head, the magnetic field is a local maxima, whereas if the field vectors meet tail to tail at a domain wall, the field is a local minima. The minima and maxima at the domain walls can be used to represent bits of information. Application of a magnetic field gradient along the direction of the strip will cause the domain wall to move in the direction of the gradient. Moving the domain wall through cusps patterned into the strip will cause the local nanodomains to spontaneously reverse their orientation relative to each other. Logic gates can be formed by applying a rotating magnetic field to a patterned structure that performs Boolean logic operations on the data encoded in the bit stream. Experimental demonstrations of MDW devices have so far employed a rotating bar magnetic to generate the rotating magnetic field. Because of that, the experimental frequencies have been limited to 27 Hz. The ultimate operational speed of the device is limited by the maximum domain wall velocity and speeds up to 1 GHz (limited by giant spin precession)[85] may be achievable.

Magnetic quantum cellular automata networks are very similar to the MDW devices in that information is stored in the magnetic orientation of an "output" ferromagnetic quantum dot. Information propagates through a patterned network of dots whose shape determines the logic function being performed. As in all QCA circuits, relaxation to the ground state is too slow for any type of practical device implementation. However, M:QCAs may be clocked by a globally applied magnetic field in a relatively straightforward way.

Spin logic devices—In 2005, the device concepts associated with this technology entry have evolved considerably relative to past editions. Previously the category "Spintronic Device" was mainly associated with the Datta-Das FET current modulator concept.[86, 87] This 2005 version of the roadmap will discuss other types of spin devices relying on different operational principles. They include a novel metal-oxide-semiconductor field-effect-transistor (referred to as a spin MOSFET). This device consists of a MOS gate structure and half-metallic-ferromagnet (HMF) contacts for the source and drain.[88] Other devices discussed include spin-torque transistor, magneto resistive element (MRE), hybride hall effect (HHE) devices, and spin gain transistor.

The spin MOSFET uses a highly spin polarized source in conjunction with spin dependent scattering in the drain as spin dependent effects that augment the usual gate-controlled electrostatic transport a heterojunction MOSFET. The resulting hybrid device combines the electrostatic and spin dependent control of the drain current to provide a device concept, which in theory meets several important criteria. They include 1) large magnetocurrent ratio for nonvolatile memory and logic functions, 2) high transconductance for high speed operation, 3) high amplification capability (voltage, current and/or power gains) to restore propagating signals between transistors, 4) small power-delay product and small off-current for low power dissipation, and 5) simple device structure for high degree of integration and high process yield. Spin MOSFET devices have been simulated to show the above criteria but no experimental demonstaration has been published. The principal experimental difficulties will likely center on the half metal source drain materials and problems with injection of spin-polarized electrons into the channel.

The "spin-torque transistor"[89] is based on the experimentally verified spin torque effect to modulate a source–drain current flow. This device concept has been reduced to practice and it is quite illustrative of the expanded device functionalities created by the fundamental interplay between electric charge and electronic spin. It also illustrates the role new materials can play in alternative logic technologies beyond CMOS.

The "spin-gain transistor"[90] is based on the experimentally observed and theoretically understood carrier mediated ferromagnetic phase transitions in dilute magnetic semiconductors.[91] In these experiments, relatively small changes in charge density in a quantum well structure are shown to induce spontaneous ferromagnetic ordering. This device[90] is similar to a magnetic bipolar transistor, where spin gain is achieved via creation of conditions for the ferromagnetic transition. This transition is caused by injecting enough carriers into the base region and then switching a small spin-polarized control current to break the isotropy and to induce spontaneous magnetization in the same direction as the control current. Spin gain in this case is defined to be the ratio of spin-polarized (for example, spin up) electrons in the collector current relative to the number of spin up electrons in the base. The spin gain transistor utilizes the number of electrons aligned along an arbitrary axis (i.e., spin-polarized electrons) to encode information in place of the absolute number of electrons typical of all conventional electronic devices. In such a system, the intrinsic property of some

material systems to undergo a spontaneous phase transformation can be exploited to achieve gain. In the "spin gain transistor" gain is achieved inducing a spontaneous phase transformation resulting from an increase in carrier density in the base of a bipolar type transistor. The strongly correlated electron material systems, discussed in the *Emerging Research Materials* section, support more complex magneto-electric phase relationships that potentially could be used as the basis for additional alternative logic devices. These expectations partially motivate the material studies taking place in this domain. This concept has not been experimentally demonstrated.

The magneto resistive element (MRE)[92] device utilizes four or more magneto resistive junctions each one of which is composed of a hard magnetic layer used for reference and a soft magnetic layer that can switch polarity dependent on the magnitude and direction of current in two input lines. If the magnetic layers are aligned, the resistance of the junction is low and if the magnetic layers are anti-parallel, the resistance will be high. For a two input logic gate, current in the two input lines is summed against the current in a third reference line to control the magnetic polarity in the soft magnetic layer. An output voltage is sensed across the pair of lines below the magneto resistive stack that is determined by the resistive states of the four magneto resistive stacks. Different logic functions are implemented simply by changeing the reference current in the reference line. The logic gates can be reconfigured from one Boolean function to another at the same speed as the logic operation itself.

Hybrid Hall effect [93] devices are somewhat simpler than MRE devices since only one ferromagnetic element per gate is needed. An HHE device consists of one or more input wires that pass over a region of ferromagnetic material. If the magnitude of the current along the input wire is sufficiently large, the magnetic field it generates will magnetize the ferromagnetic element in either the left or right direction, depending on the direction of current flow. Since ferromagnetic materials retain their magnetization state in the absence of an external magnetic field, the magnetization state of the ferromagnetic element can be used to store a binary value, interpreting one direction of magnetization as a logic 1 and the other as a logic 0. To observe the magnetization state of the ferromagnetic element, a bias current I is passed through the conductor at the base of the device in a direction perpendicular to the magnetic field. As specified by the Hall Effect,[94] the interaction of this current and the magnetic field generated by the ferromagnetic element produces a voltage perpendicular to the direction of the bias current. The magnitude of this voltage is determined by the Hall resistance of the device and the magnitude of the bias current, allowing trade-offs between the sensitivity required in the circuitry that reads the output voltage and the amount of bias current, and therefore bias power, required.

The prevalence and enormous economic impact of spin-based transport on magnetic storage media continues to drive the search for similar devices that can be applied to logic technology. A few concepts have emerged as indicated above but so far, no viable devices have been demonstrated, but the field of spin-transistors is the subject of a great deal of continuing research activity. However, while these proposed new structures are quite attractive concepts for the reasons cited above, they still rely on charge transport in one fashion or other and, therefore, are still quite limited in their potential to scale to device densities and speed beyond those attainable by ultimately-scaled CMOS.

EMERGING RESEARCH MATERIALS

INTRODUCTION

Many ERDs will require materials with dramatically improved or new properties, and the Emerging Research Materials Working Group has identified the critical materials properties required for fabrication and operation of these new devices and potential materials solutions. Fabrication of many of these new materials may require new chemicals, synthesis techniques, and metrology to characterize and improve their performance. Successful evaluation of the ERDs will require materials that have critical properties and interface materials properties that are optimized for device operation and this will require characterization and modeling to identify the materials properties that must be changed or improved. Synthesis of new chemicals for use in molecular devices will require increased understanding of the switching mechanisms, contact formation, and transport mechanisms. Similarly, fabrication of nano-structured materials, such as nanotubes or nanowires, for devices will require improved control and understanding of the impact of process on the structure, the resulting electronic properties and interface properties. Synthesis of materials for application in spin devices may require control of isotopic purity, impurity levels, spin relaxation and interface spin transmission and spin de-coherence mechanisms. If self-assembly mechanisms are to be useful to fabricate high density device materials, the synthesis mechanism must be capable of reproducibly constructing materials into desired patterns at a higher density than can be achieved with lithography. These challenges will require new metrology to characterize the resulting structure and critical materials and interface properties at the nanometer scale. In addition, modeling and simulation will be needed to analyze and identify chemical and structural changes to improve materials properties and the resulting device operation.

CRITICAL PROPERTIES

The viability of Emerging Research Devices is critically dependent on the ability of materials to support device operation. These device materials must also be integrable with CMOS, be stable, and reliable. Since devices are comprised of several materials and interfaces, this section will identify the critical requirements for the properties of the materials and interface properties.

The ERDs consist of a number of options for memory and logic devices based on conventional charge-based and alternative computational-state variables, which are identified below. The operating mechanisms required to change the state can be grouped into broad categories, also shown below. The material properties necessary to support computational state variables and switching mechanisms are identified in Table 60. Devices may require more than one of these mechanisms to operate effectively, and some materials may support more than one state variable and mechanism.

Table 60 Critical Emerging Research Materials' Properties

Computational State Variable	*Mechanisms To Change Computational State*	*Mechanism To Read Computational State*	*Critical Material Properties*	*Critical Interface Properties*
Charge State	▪ Charge transport via tunneling ▪ Ohmic conduction, diffusion ▪ Hot electron injection	▪ Voltage charge and discharge of a node	▪ Density of states as manifest in Eg, m_{eff}, and m (E,n,p,stress), and v(sat) [A] ▪ Dielectric constant (κ)	▪ Interface energy barrier height as manifest by electron affinity, fixed or trapped charge, stress, interface scattering, etc.
Spin State [Spin injection and transport in semiconductor]	▪ Voltage / electric field ▪ Magnetic field ▪ Spin injection from a ferromagnetic material ▪ Optical pumping (polarized photons)	▪ Output voltage ▪ Polarized optical emission ▪ Polarized optical transmission	▪ Spin orbit coupling (as manifest in spin lifetimes, and diffusion lengths) ▪ g-Factor [B] ▪ Ferromagnetic contact source: coercivity	▪ Interface band structure matching [energy and symmetry] (as manifest in spin injection efficiency) ▪ No band-bending
Spin State [Ferromagnetic Semiconductor]	▪ Temperature ▪ Modulation of hole concentration		▪ Spin exchange interaction and exchange splitting energy ▪ T Curie ▪ Moment per atom	▪ Interfacial spin orbit coupling as manifest in (interface magnetic anisotropy) ▪ Minimal band bending
Strongly Correlated Electron State	▪ Electric field ▪ coulomb moderated exchange interactions ▪ temperature ▪ magnetic field ▪ photon, phonon	▪ Magnetic Force microscopy (MFM) ▪ CMR [C] ▪ Polarized photon ▪ Electrical ▪ SEMPA [D] ▪ Neutron scattering	▪ T Curie, minimum "domain" size ▪ H&P coupling coefficient [E] ▪ E&M coupling coefficients [F] ▪ Compositional and oxygen control	▪ Surface and interface stability and stress ▪ Domain wall stability
Molecular Conformation State	▪ Chemical redox reactions ▪ Electromagnetic radiation ▪ Charge injection ▪ Electric fields ▪ Mechanical stimulus	▪ Charge transport	▪ Conformational conductance change ▪ Change in tunnel distance ▪ Delocalization-Localization of states	▪ Atomic energy levels in resonance with the molecular energy states (the contact atom must be considered as part of the molecule) ▪ Work function ▪ Contact material DOS [G]

Parameter Defining Notes for Table 60:

[A] Eg is the bandgap of the material, m_{eff} is the effective mass of the carriers in an electric field, the carrier transpoert mass, m, is a function of the electric field (E), the electron (n) and hole (p) concentrations and stress, and the carrier saturation velocity [v(sat)].

[B] The Lande' g-factor quantifies the efficiency of the spin anuglar momentum in producing a magnetic moment.

[C] CMR is Colossal Magnetoresistance, present when application of a sufficiently high magnetic field to the material results in a large change in electrical resistance of the material.

[D] SEMPA is scanning electron microscopy with polarization analysis of the secondary electrons.

[E] A magnetic field (H) induces a change of material polarization (P) and the coefficient indicates the magnitude of the polarization change with the magnetic field.

[F] An electric field (E) induces a change of material magnetization (M) and this coefficient indicates the magnitude of the magnetization change with the electric field.

[G] DOS is the density of electronic states for the contact material in this case.

1D CHARGE STATE MATERIALS

KEY CHALLENGE

The key challenges with 1D charge state materials are to: 1) grow nanotubes (NTs) and nanowires (NWs) with predefined electronic properties through control of diameter, structure, and composition, 2) position these structures in predefined locations and orientations, which may require sub-nanometer registration, and 3) form contacts and interfaces with desired electronic properties and adhesion.

GROWTH WITH CONTROLLED PROPERTIES AND LOCATION

INTRODUCTION

The most common growth technology of nano-structured materials uses different forms of chemical vapor deposition [CVD], but research is demonstrating that supercritical fluid transport also can be used to grow these structures. Critical research is needed to characterize the relationship between growth technique, temperature, conditions, catalyst composition and the resulting structure and electronic properties of the grown 1D nanostructures. Growth with controlled properties will require careful experimental characterization of electronic properties as a function of diameter, structure, including defects, and composition to develop models that can predict the electronic properties. Metrology to rapidly characterize the critical properties of large quantities is needed to enable synthesis optimization. *Ab-initio* models need optimized density function models to accurately predict density of states (DOS), bandgap energy (Eg), and conduction energy levels. These models will be used to evaluate sensitivity to defects, potential doping mechanisms and will enable device modelers to assess new device structures.

For 1D charge state materials to be useful as CMOS devices, it is critical that materials with well controlled properties be placed in high density at predefined locations with well-controlled orientations. There are two approaches to achieving these requirements: 1) place the catalyst in predefined locations and then apply an electric field to direct growth of ultra high purity materials in a specific orientation; and 2) grow the 1D materials, purify them, select materials with the right properties, and then use directed assembly to place them in positions that are pre-defined. Each of these approaches has significant challenges and will require coordinated efforts to enable them.

GROWTH WITH CONTROLLED PROPERTIES

Nanotube Growth and Property Control—For carbon nanotubes, the diameter and chirality are determined by the catalyst (Fe, Ni, Co mixtures) and CVD growth conditions and these determine the bandstructure which then determines the bandgap energy, effective mass and transport properties. Currently, carbon nanotubes grow with a range of diameters and chiralities with many of the tubes being metallic and the semiconducting tubes having a range of bandgap energies that is a function of chirality and which increases as the diameter decreases. Catalysts and processes must be developed to fabricate not only tubes with controlled chirality and diameter, but also with controlled doping for n, p, and intrinsic carrier concentration. Work to increase the concentration of semiconducting CNTs has demonstrated an increase from ~61% to ~90%[95] semiconducting by using a plasma CVD process at lower temperature, but this is far short of what would be required in the future. Thus, research is needed to understand the role of the catalyst, temperature, and chemistry in defining the diameter and chirality of the CNTs and then establish control of these properties. Metrology to characterize the bandgap distribution of nanotubes as grown and on wafers is urgently needed to enable these correlations. Development of catalysts and processes that can control the chirality and diameter will require understanding of the growth mechanisms and kinetics at the nanometer scale to be able to produce CNTs with controlled properties.

As grown semiconducting CNTs normally are p-type, and mechanisms are needed to controllably and selectively dope them both n- and p-type. Work has found that CNT carrier concentration can be modulated with exposure to NO_2 and NH_3,[96] but the change is not stable without the gas. Treatment of Schottky barrier CNT transistors with trifluoro-acetic acid (TFA) resulted in improved device operation[97] that was attributed to an effective change in the electrode work function by the polar molecules. These approaches may be more suitable for chemical sensor applications, but are not stable for embedded device applications. The ability to control hole concentration in CNTs by surface functionalization[98] has been demonstrated to be stable in air, but mechanisms will be needed to controllably dope the CNTs p- and n-type while embedded in a dielectric. Therefore, research is needed to explore different mechanisms to control carrier type through substitution in or after growth as well as charge transfer to or from interface layers.

Nanowire Growth and Property Control—Nanowires are also grown with a catalyst in a CVD process and the properties are controlled by the catalyst, gas chemistry, and crystal structure of the material. The catalysts have finite solubility in the common materials, Si, Ge, etc., at the growth temperatures, so could be integrated into the NW. As the nanowire grows, gas chemistry and temperature must be controlled to passivate the surface of the wire[99] and inhibit secondary

epitaxial growth on the sides of the tube. The preferred orientation of the NWs is to grow in the <111> direction, so this can be used to advantage,[100] however, since these wires are cylindrical, multiple surface orientations are present and this could make passivating surface states challenging as the diameter is reduced to small values. Critical issues will be the ability to grow NWs with controlled doping, and without the catalyst being integrated. Again, studies are needed to explore the growth process and the role of the catalyst in the formation of the crystal structure. There may also be a need to grow NWs with heterostructures such as Si-SiGe, etc., so the ability to grow low defect NWs with controlled interfaces will be important.

The carrier concentration can be achieved in the CVD process by using common dopants such as B, As, etc.; however, control of the dopant concentration and location in the NWs will be important. As the diameter of the NWs decreases, small amounts of dopant can result in high impurity concentrations and the resultant carrier concentration will be sensitive to small changes in the number of dopant atoms. Since heterostructures may be of interest, characterization of the stress dependence of electronic properties must be done for these as a function of structure and diameter.

NANOSTRUCTURE-DIRECTED GROWTH

Directed Growth in Predefined Locations—The challenges to this are to: 1) place the catalyst in predefined locations and have 100% of them produce NT/NW; 2) grow the NWs or NTs in a predefined orientation, and 3) grow 100% of the NT/NWs with the required control of electronic properties (bandgap energy, effective mass, etc.). Clearly, the patterning and reproducibility of the catalyst and growth process are critical and significant work must be undertaken to control these.

Nanotube Directed Growth—Growth of nanotubes in predefined locations in controlled orientations is extremely challenging, because they grow in random orientations depending on the catalyst orientation. Recently, electric fields have been used to direct carbon nanotubes in general directions,[101] but this is incapable of achieving nanometer registration. So, significant research is needed in directed growth of nanotubes.

Nanowire Directed Growth—Nanowires typically grow in preferred crystal orientations and this can be used to align with wafer crystal orientation.[102] However research is needed to improve location and orientation control to nanometer scale and make these reproducible.

NANOTUBE PURIFICATION AND DIRECTED ASSEMBLY

Since nanotubes are so difficult to grow in controlled orientations with controlled properties, an alternate approach is to separately purify nanotubes and use directed assembly to position them in predefined locations. The challenges to purification and assembly are to: 1) develop purification schemes that can differentiate between nanometer structures that are chemically the same, but structurally and electronically different; 2) achieve parts per trillion purity for specific properties; 3) cut them to predefined lengths, and 4) assemble them in predefined locations with 100% accuracy and sub nanometer registration. Several groups are exploring whether chemicals can differentiate between nanostructures with different electronic properties, but progress is slow and purity is in the tens of percent at this stage. Directed assembly in predefined locations would require the nanostructure to have a chemical function that would recognize the compliment at predefined locations on the substrate. Some have suggested DNA or chemicals with recognition abilities to make these alignments, while others have suggested electric fields or capillary forces to align the nanomaterials to pre-etched slots on the substrate. Other work demonstrates that nanowires grown on MBE templates can then be aligned and transferred to a new substrate.[103, 104] Each of these approaches has significant challenges that must be overcome. Significant research is needed to evaluate purification and directed assembly techniques.

1D CHARGE STATE MATERIAL INTERFACES

Formation of low resistance contacts to NWs and NTs is the biggest current challenge. Since the early days of semiconductor technology, the industry has produced low resistance contacts to metal by doping the semiconductor degenerately either n or p type followed by depositing a metal or forming a silicide. This eliminated potential barrier formation and also reduced the conductivity difference between materials. However, at the nanometer scale, the question is how to form low resistance contacts to these nanostructures when high-level doping of these materials is not possible, such as in CNTs. For CNTs, the lowest resistance contacts are formed with tantalum, but the contact resistance is higher than theoretical. For NWs, the question is whether low resistance contacts can be formed without having a degenerately doped region in the silicon, and if so, what level of doping is required. Significant research needs to be done to characterize the interactions occurring in contact formation and understand the impact on energy levels in the materials and any disruption of the device material. Research is also needed to explore new metals, alloys, and processes to form low resistance contacts. Since the amount of charge in the device will be low, high-κ gate dielectric and passivation

layers must have low interface states, charge trapping, and controlled fixed charge. For CNTs, the bonding of the dielectrics to the carbon may be challenging due to the low reactivity of CNTs. For NWs, multiple orientations will be exposed to the dielectrics and surface states may vary dramatically with orientation and this may become worse as the diameters are reduced.

CRITICAL METROLOGY FOR CARBON NANOTUBES

While improved control of sub-nanometer structure, composition, and properties is important, an equally important need is for metrology to rapidly measure the threshold voltage distribution of as grown carbon nanotubes (CNTs) in large batches. As researchers work to improve property control and yield of semiconductor tubes, they can only measure the properties of a small number of CNTs, so they are unable to determine whether process changes improve property distribution or control. While Raman spectroscopy can identify CNTs based on vibrational states, the spectra is sensitive to bundles, impurities, and chemical environment of the nanotubes. Rayleigh scattering is an emerging technology that can measure CNT electronic properties, but they must be positioned in a special fixture. The lack of a metrology capability to rapidly quantify CNT bandgap distribution will limit progress in improving growth processes and their control of properties.

MOLECULAR STATE MATERIALS

KEY CHALLENGE

The greatest challenge for molecular state electronics is to fabricate molecular film devices with reproducible switching and transport properties and validate that the transport is electronic switching of the molecule, rather than redox reactions with electrodes[105] or by formation and dissolution of nano-filaments[106] or other mechanisms.

INTRODUCTION

Molecular state devices exhibit a range of properties including non-linear IV characteristics and bi-stable states and many have been shown to be reproducible on a given device. Often, however, these characteristics vary greatly from sample to sample when fabricated under "identical" conditions. In a number of cases, transport through molecular wires has been verified to be through tunneling[107] and, in some cases, bi-stable states have been validated to be created by way of charge storage.[108] However, determination of the mechanism is often challenging and limited tools are available to determine the actual mechanism at the atomic level for an embedded film. Since most molecular devices are really an array of many of molecules in parallel, defects, collective molecular, or contact interactions could be occurring. Further complicating the situation is that switching actually may be redox reactions with electrodes or nanofiliament formation shunting the molecule(s). Resolving these issues will require a close collaboration between device, synthesis, characterization, and modeling to design experiments capable of separating the complex phenomenon that could be occurring. While these challenges are significant, progress is being made as device variability has been improving with experiments starting to separate many of these complex phenomenon, and even 1 kilobit functional circuits[109] have been constructed using these materials.

TRANSPORT AND IV NON-LINEARITY

As mentioned above, transport through some molecular wires was determined to be controlled by tunneling,[110] but other mechanisms may be involved in transport in other cases. For some devices, the IV characteristics have been shown to be reproducible for millions of cycles, but there can be large sample-to-sample variations in the voltage of onset of these non-linearities. More recent work is showing that the contact metal[111] and contact bonding hybridization[112] can have a significant impact on the operation of molecular devices. In devices, the lowest resistance path will dominate in the current voltage characteristics, so defects, regions of higher electric field, local contact interactions that change the electronic states of the molecule could be potential sources of these variations. Scanning tunnel microscopy (STM) has been used to characterize transport through individual molecules and identified rectification at Schottky barrier contacts and nonlinear IV transport for a molecule[113] with CH_2 tunnel barriers inserted. The ability to characterize the transport properties of individual molecules with STM or conductive atomic force microscopy (CAFM) may enable better understanding of the metal-molecule interface and the intrinsic transport properties of molecules versus collective effects in thin films. It is important to establish a methodology for first characterizing the current voltage characteristics to determine the transport mechanism and then a suite of diagnostics to determine the root cause of the variation in nonlinearity. If the transport is localized to a small area, characterization would need to focus on the variations in that region rather than the average over a larger area.

BI-STABLE STATES

Molecules that exhibit bi-stable states are of interest for potential application to memory or logic devices, but wide ranges of behavior are exhibited. In cases of nitro-amine based molecules,[114] the bi-stable states have been suggested to be based on charge storage on the nitro-amine with charge storage retention limited by hopping conduction leakage of the stored charge. In other cases storage has been for up to two months,[115] but the mechanism for storage has not been determined. As mentioned above, the electric fields can be very high at these small thicknesses, so interactions with the electrodes and environment could cause migration of metal to regions of high field on the molecule to form a metallic bridge at the tunnel. Again, a test suite needs to be developed to determine whether the mechanism is charge storage, redox, nanofilament formation, or other mechanisms. Furthermore, new metrology will need to be developed and applied to characterize the molecule in the bi-stable states to determine the origins of the bistability, decay mechanisms, and to determine whether they are controllable.

MOLECULAR STATE CONTACTS

Formation of contacts to molecules is critical to the operation of a device, because of the following: 1) the energy levels of the metal interact with the molecular energy levels and are critical in device operation, and 2) the top metal deposition with energetic atoms could cause disruption to the molecular film and bonding, or in some cases, metal redox reactions have occurred in some molecular device switching.[116] Recent work with molecular contacts has shown that the orientation of the contact atom to the molecule can change the operation of the molecular device,[117] so atomic level control of bonding and hybridization may be needed at this interface. For the bottom contact, most molecules are self-assembled on Au, and a thiol (sulfur) attaches the molecule to Au. This mechanism may modulate the operation of the molecule-metal interface. Recent work has demonstrated that molecules can be self-assembled onto silicon to eliminate the need for the thiol,[118, 119] and work is proceeding to identify new materials to contact the top of the molecules with less energetic processes. Since the molecular films are only ~2 nm thick, the electric fields are ~5 MV/cm with 1 volt applied, so the attractive force of the top and bottom contacts can apply large forces to the molecular film. This mechanism could initiate non-uniform breakdown processes when small defects are present on a surface or in the layer. As can be seen, contact formation is critical to operation of reliable molecular devices. Research is needed to develop metrology and methodologies that can separate molecular switching mechanisms from redox reactions and other phenomenon for embedded molecular films and enable development of reliable contact materials and processes for molecular devices.

METROLOGY

Since it is difficult to look through the top contact into the electronic structure, there needs to be significant interaction with metrology, molecular modeling, and synthesis to design experiments and test structures that can resolve these issues. New metrology capabilities such as inelastic electron tunneling spectroscopy[120] and backside FTIR[121] to study vibrational states, STM,[122, 123] conductive AFM, and Kelvin Probe AFM[124, 125] are beginning to enable understanding of the transport through individual molecules and interfaces. However new metrologies and additional research are needed to resolve these issues.

SPIN STATE MATERIALS

KEY CHALLENGES

The key challenges for materials for spin state devices are to identify: 1) ferromagnetic semiconductor materials with Curie temperatures above room temperature and are compatible with conventional semiconductors, and 2) materials that have properties capable of enabling spin gain in devices.

INTRODUCTION

Spin devices fall into two categories: 1) ferromagnetic semiconductor devices, and 2) semiconductor devices with spin polarized electrons injected from ferromagnetic junctions. The ferromagnetic semiconductor devices have made significant progress in improving performance, but are limited to operation below their Curie temperature which is < 200 K for most of these materials. Semiconductor devices with spin injection from ferromagnetic contacts are making rapid progress, but room temperature operation requires the use of ferromagnetic metals, such as Fe, Co, etc., which requires a tunnel barrier between the metal and semiconductor to overcome the conductivity mismatch. This challenging issue and technology could benefit from use of ferromagnetic semiconductors as the spin injector.

FERROMAGNETIC SEMICONDUCTOR DEVICES

MATERIAL PROPERTIES

Ferromagnetic semiconductor materials have an energy band structure that enables ferromagnetic ordering when the Fermi energy and thus carrier concentration is at the right level. Thus, application of an electric field or changing the carrier concentration will change the ferromagnetic ordered state of the material.

Most ferromagnetic semiconductor devices consist of a ferromagnetic layer integrated between semiconductor layers, so the compatibility of the materials at these hetero-interfaces is critical. A number of alloys including EuO, $CdCr_2Se_4$, GaMnAs, InMnAs, and GeMn are ferromagnetic with Curie temperatures less than 200 K and have been used to make ferromagnetic spin device structures. Other materials including transition metal compounds with ZnO, Si, and TiO_2 have reported ferromagnetic properties at higher temperatures, but carrier mediated ferromagnetic ordering has not been demonstrated to date. In many complex materials, magnetic probes can detect a ferromagnetic signal, but the presence of a segregated ferromagnetic phase is possible and must be eliminated.

TRANSPORT INTERFACES

Experimental results demonstrate that transport interfaces can have some level of stacking faults with minimal degradation of spin injection; however, rough interfaces with significant chemical intermixing can dramatically reduce spin injection. Thus, some lattice mismatch can be tolerated, but chemically unstable interfaces with significant intermixing are very detrimental. As new alloys are identified, it will be critical to evaluate their chemical compatibility with semiconductor materials to ensure they can form stable interfaces.

PASSIVATED INTERFACES

For passivated interfaces, these materials should not produce dramatic band bending in the semiconductor or ferromagnetic semiconductor. Such band bending will reduce the effectiveness of carrier modulated magnetism in the ferromagnetic semiconductor and spin orbit coupling could induce decoherence in the semiconductor materials. Furthermore, as dimensions approach the nanometer scale, these passivated interfaces could become more crucial in the functioning of these devices.

SPIN INJECTION MATERIALS

FERROMAGNETIC METAL SPIN INJECTORS

For spin injection from a ferromagnetic metal into a semiconductor, a tunnel barrier must exist between these materials to accommodate the large difference in conductivities,[126, 127] and both oxide[128] and Schottky barriers[129, 130] have been effectively demonstrated. For efficient injection of spin-polarized carriers into the semiconductor, the symmetry of the majority states of the metal at the Fermi energy must match that of the conduction band states of the semiconductor, while the minority band in the metal must have a different symmetry or couple only weakly to the semiconductor states. This requirement will limit the choice of ferromagnetic metals for a given semiconductor, but Fe has been effectively demonstrated for a number of II-VI and III-V semiconductors.

FERROMAGNETIC SEMICONDUCTOR SPIN INJECTORS

Interfaces for spin injection can tolerate stacking faults, but if significant roughening or interdiffusion of materials occurs, this can dramatically reduce the tunnel injection efficiency. The use of a ferromagnetic semiconductor would eliminate the need for the tunnel barrier and the interface would not need to be a perfect lattice match, but would need to have minimal intermixing and roughness. Ferromagnetic semiconductors, such as GaMnAs, InMnAs, and GeMn, could be valuable for injecting spin into semiconductor devices or for potential spin amplification; however, these materials are only ferromagnetic to < 200 K. This is a major limitation to use of these materials in devices, so higher T-Curie materials need to be found. Modeling has identified a number of candidate materials[131] and further work needs to be undertaken to investigate these and refine the model. A number of materials, including GaN and ZnO, have been reported to be ferromagnetic at room temperature with superconducting quantum interference devices (SQUIDs), but carrier mediated ferromagnetic exchange has not been experimentally verified in these materials. Research needs to be conducted to explore potential ferromagnetic semiconductor materials that are relatively close in lattice constant to Si or Ge. Furthermore, research is needed to understand the physical mechanisms that enable ferromagnetic behavior and determine whether new higher temperature materials could be developed. As devices and materials approach the nanometer scale, the structure and composition at the interfaces will become important and it will be necessary to understand this dependence.

PASSIVATED INTERFACES

For the semiconductor spin transport region of the device, band bending should be minimal to reduce spin orbital coupling that can produce decoherence, but little is known of interaction of the spin-polarized electrons with the interface in scattering. Thus, dielectrics should have little fixed charge and must not create interface states that could produce band bending. Recently, techniques have been demonstrated for studying scattering of non spin-polarized electrons at interfaces.[132] This experiment identified that spin up, down, and unpolarized electrons beams were scattered at different angles through spin-orbit coupling. Techniques similar to this may be useful in studying interfacial spin scattering in other material systems and studying spin orbit coupling parameters.

STRONGLY CORRELATED ELECTRON STATE MATERIALS

BACKGROUND

These materials are complex multi-metal oxides that include a transition metal with a unique crystal structure (Shubnikov Groups). In these materials, the transition metal is in an oxygen matrix and stress or phase transitions can cause ordered distortions of its bonding. These distortions cause splitting of energy levels and long range coordinated charge and spin ordering. In some of these materials, electric fields or magnetic fields can cause distortions that induce phase transitions that change the spin and/or charge ordering. This charge orbital and spin ordering can enable a variety of magneto-electric effects and phase transitions.

DEFINITIONS

- Ferroelectric material: Application of an electric field to the material induces a residual electric polarization.
- Ferromagnetic material: Application of an external magnetic field induces a ferromagnetic ordering that can produce a residual magnetization.
- Multiferroic (MF) material: Materials have multiple ferroic states (ferroelectric, ferromagnetic, ferrotoroidic, or ferroelastic) in the same phase. In the ERD, interest is for ferroelectric and ferromagnetic properties being coupled in the same phase. Application of a sufficient magnetic field can induce a change in electric polarization or application of sufficient electric field can induce a change in ferromagnetic state.
- Colossal magneto-resistance (CMR): Application of sufficient magnetic field to the material can dramatically change the electrical resistivity of the material.

KEY CHALLENGE

The key challenge is to determine whether the complex ferromagnetic and anti-ferromagnetic phase transitions and spin-charge-orbital ordering observed in neutron diffraction for these materials can demonstrate large room temperature multiferroic properties or stimulated spin alignment or spin waves at the nanometer scale and thus enable new spin device functionality.

MATERIAL PROPERTIES

A broad range of complex transition metal oxides exhibit strong electron correlation and this is manifest in high Tc superconductivity, ferroelectric properties, multiferroic behavior, colossal magneto resistance (CMR), and other effects. These effects are manifest when a Jahn-Teller distortion of the oxygen octahedral surrounding the transition metal removes degeneracy, splitting energy levels, and in some cases generating a half-filled metal state. The multiferroic properties of these materials may be of potential use for converting voltage to magnetism or magnetism to voltage in spin devices, but the coupling coefficients must be reasonably high above room temperature to be of value. Recent work on half-doped transition metal oxides ($RBaMn_2O_6$ where R=Sm, Eu, Gd, Tb, Dy, Ho, Y, and also Ba, Sr, and Ca could be interchanged) with strong correlation[133] highlights that these materials may be capable of switching and propagating spin waves.[134] These materials have complex antiferromagnetic/ferromagnetic phases that correspond to changes in the lattice at different temperatures. While high Curie temperatures have been reported for these strongly coordinated electron materials, the ferromagnetism becomes much weaker at room temperature.[135] The mechanism for this phenomena must be understood. Similarly, multiferroic materials are often electrically leaky at room temperature, so the multiferroic properties are usually verified at low temperatures.[136] The properties of these materials can be altered dramatically by modifying the lattice through variations in atomic radius of the metal atoms and the relative charge of the lattice. Changing the composition enables alterations of charge, crystal structure, orbital configuration, and spin states that provides opportunity to design materials with new properties. It is proposed that aligning the spins of a small number of atoms in the lattice may propagate and precipitate a broad spin alignment through the material,[137] because the material is in a "frustrated" or metastable state, where the spins are coordinated without spin alignment. Studies have demonstrated

large changes in ferromagnetic and anti-ferromagnetic ordering at critical phase transitions, which may support this model. It has been proposed that spin waves could propagate at very high speeds in the presence of pulsing electric fields or EM radiation and suggest that the orbital hybridization can be changed at frequencies approaching 100 THz.[138] While the orbital hybridization oscillation frequency may be high, the transport velocity would limit switching of larger areas and this is currently unknown. If spin were to propagate at the speed of sound in nanometer size areas, this would be relatively fast, but could not support longer distance spin transport. Thus, it is important to determine the mechanism and dispersion relationship for spin propagation in these materials.

Since these transition metal oxides, with strong electron correlation, have such a diversity of behavior, fabrication of novel device structures with these compounds may be possible. The major challenge is to determine whether these complex phenomenon and spin ordering effects can be translated into nanoscopic effects that can enable new device phenomenon. Nanometer scale structures in similar compounds exhibit multiferroic behavior,[139] and these small structures would have lower interfacial stress, because of the small areas involved. Thus, research is needed to determine whether the observed phase changes in spin alignment that occur and precipitate in these materials could be used in new spin-based device structures. It is important to experimentally determine whether introduction of spin alignment in a local region of these materials will propagate and amplify. It is also important to determine the energy of the switching, the potential spin propagation speed in these materials and effects of EM radiation, voltage pulses, etc., on their properties.

SYNTHESIS

The behavior of complex multi-metal oxides depends on their stochiometry and may also depend on oxygen vacancy concentration, thus controllable growth conditions will be critical for achieving reproducible material properties and performance. The ability to fabricate new structures with these materials allowing atomic level control of composition and oxygen using techniques such as MBE[140] may enable fabrication of new materials or superlattices[141] providing useful properties for novel device applications. Since many of the antiferromagnetic/ferromagnetic (AF/FM) properties are strongly dependent on lattice distortion, and stress could produce large nonuniformity of properties, management of stress at the nanometer scale will be critical[142] and especially challenging in thin films. Conversely, effective and controlled management of stress, for example via growth of superlattice structures, could possibly offer another degree of freedom to control and engineer the multiferroic properties of these materials.

INTERFACE MATERIALS

While many of the properties of materials that will interface to these AF/FM materials are unknown, the contact materials must not detrimentally interact with the AF/FM material. The operation, fatigue, and imprint of ferroelectric materials have been degraded with metal contacts, so other conductive oxide layers have been used.[143] Furthermore, the stress in these materials is crucial to operation, so interface materials should not create or modulate stress. The compatibility of these materials with semiconductor materials will be critical if they are to be integrated with spin or semiconductor devices. Due to the low crystal symmetry of these materials, thin films of these form twins on semiconductors such as Ge, Si or GaAs, which will be challenging. On the other hand, growth of nanostructured materials[144] or atomic layer epitaxial growth on off axis substrates[145] may reduce the twinning. Much research is needed to study the interactions of these materials in growth with semiconductors and metals, and to understand and eliminate the degradation mechanisms that have been observed to date.

CHARACTERIZATION AND MODELING

While the interface and growth issues are challenging, the most important question is whether the unique properties of complex multi-metal oxides can be accessed to function as nanoscale device elements. This will require development of new test structures to determine the coupling coefficients of multiferroic materials, determine whether the metastable spin state can produce stimulated reversible spin transitions or spin wave propagation with spin injection at the nanometer scale. Before significant resources are applied to resolving synthesis, interface, and integration issues, evidence needs to be presented that the complex AF/FM phase transitions that have been characterized with neutron scattering, X-ray, and optical spectroscopy can produce spin and magnetic transitions that could operate in nanometer scale materials and devices.

For device applications, the most important verification is the ability to change and measure states with an externally applied stimulus, such as an electric field or a magnetic field; however, most of the properties of these materials are difficult to measure. Recently, a material was found to be multiferroic with a Curie temperature of 370 K; however, it was not possible to electrically measure the MF operation above 130 K[146] because the film became electrically leaky.

Similarly, tunneling magneto resistance has rapidly declined by 200 K even though the strongly coordinated materials had a Curie temperature of over 340 K.[147] This leaky behavior is being attributed to interface issues, which must be understood and overcome if these materials are to be useful.

The modeling of the complex phase transitions of these materials needs to explain how their properties will be manifest in macroscopic or nanoscopic phenomenon. Modeling at the atomic and lattice level needs to explain how orbital phenomenon and localized effects will extend to longer range magnetism and spin propagation. Models of the electrical leakage and magnetic loss mechanisms are needed to understand whether these are fundamental to the materials or related to defects and interface issues. This will require significant work between the experimental and modeling communities.

MATERIAL SYNTHESIS

INTRODUCTION

Materials synthesis focuses on the fabrication of new materials or molecules through unit processes and will include potential interactions with earlier fabricated materials, but does not consider the fabrication of integrated devices. This section will include the synthesis of new macromolecules, self-assembled thin uniform and template films, nano-structured materials, and interface materials. Many of these emerging capabilities are very speculative, but should be explored to determine whether they could add significant value in the fabrication of emerging research devices. As these are being evaluated, the fundamental limitations of these capabilities should be examined to determine whether they have a viable intersection with the ITRS.

MOLECULAR SYNTHESIS (MOLECULES AND MACROMOLECULES)

Molecular synthesis describes the fabrication of molecules and macromolecules for application to molecular devices (already discussed in the Molecular State section), thin films, directed, and self-assembly agents. Improved understanding of the relationship between molecular structure and electronic properties may enable design and application of new molecules with unique properties as new elements of emerging research devices. Furthermore, needs for sub-nanometer directed and self-assembly may require molecules designed to recognize other molecules or structures as registration features. Thus, research is needed to understand the relationship between molecular structure and potential assembly mechanisms and their limitations in directed assembly.

THIN FILM SYNTHESIS

Thin film synthesis focuses on the new requirements for fabrication of emerging research devices with unit processes that are covered in the *FEP chapter* of the ITRS. Synthesis of emerging research materials may need new chemical precursors and deposition techniques with atomic level control, but it is too early to speculate on this.

SELF AND DIRECTED ASSEMBLY

The most critical need for directed or self assembly is for fabrication of nanostructured materials with sub-nanometer placement and orientation accuracy, and that are aligned to lithographically defined features. This capability could enable fabrication of materials and devices with sub lithographic features, which would be registered to lithographically defined (top down) features, enabling connection to CMOS devices and interconnects.

A central feature of self-assembling materials is that the individual material components are coded (via their shape, size, charge, etc.) to guide construction of the nanostructure. Many research examples of self-assembling material systems involve formation of only simple patterns (such as porous alumina or block copolymer structures) and often have local order, but lack long-range order. Furthermore, because many of these processes are thermodynamically driven, their defect levels are higher than those achieved using lithographic processes. Critical research is needed to establish the fundamental size, alignment, and orientation limitations of different self-assembly techniques.

To determine whether self-assembly growth conditions are compatible with CMOS processing and can interface with top down CMOS fabrication, directed self-assembly techniques involving strain or surface tension should be evaluated to determine whether they can align bottom-up nanostructures to top-down defined features. Exploratory research should also be done to determine the potential ability of directed assembly with electromagnetic fields, fluid flow, optical fields, bio and DNA methods to align nanostructures and self-assembled materials in a high-density form with lithographically defined features.

CONTACT MATERIAL ISSUES

Each emerging research material has significant electrical contact challenges and will require substantial research to understand the material interactions and mechanisms. This will require development of new interface materials, understanding of the interface formation processes, and mechanisms that could degrade material properties. Thus, new metrology, test structures, and techniques will need to be developed to characterize the structure, composition, and their impact on the resulting material properties.

CHARACTERIZATION

INTRODUCTION

The development of materials for emerging research logic and memory devices requires nanoscale metrologies to enable identification and optimization of critical physical and electrical properties of these emerging materials and to support extraction of parameters for modeling and simulation of materials synthesis and material properties. Since these emerging research materials are in the research stage and would be used in nanometer scale devices, the metrology needs are primarily fundamental and detailed characterization, not process metrology. The extreme sensitivity of the electronic properties of these nanodevices to small perturbations in structural, chemical, and local electrical properties requires extremely sensitive analytical measurements. Furthermore, the addition of materials not typical to the semiconductor industry (e.g., organic molecules) presents new characterization challenges. Several characterization needs that span the variety of materials are identified and briefly reviewed here. The *Metrology* chapter of the ITRS will focus on possible solutions to meet these needs.

3-DIMENSIONAL, ANGSTROM RESOLUTION, ATOMIC SENSITIVITY (STRUCTURE AND COMPOSITION)

Many of the emerging devices and associated materials do not possess simple planar geometries. Furthermore, properties are typically sensitive to nanoscale structure and minute compositional changes of materials. For example, one of the issues with bottom-up grown nanowires is that small amounts of metal catalyst used to grow the nanowires can migrate into the nanowire and affect the electrical properties. Also, small amounts of hydrogen bonded to carbon nanotubes or to other organic molecules in molecular electronics can strongly impact electrical transport properties. Therefore, physical characterization techniques are required that characterize structure and composition in 3-dimensions, with angstrom resolution and with atomic sensitivity. Most analytical laboratories are extremely comfortable characterizing compositions approaching 10^{10} atoms at spatial resolutions of 100 nm. There is significant capability and ongoing research in characterizing composition approaching 10^{3} atoms at spatial resolutions of several nanometers. New characterization technology and understanding is needed for characterizing compositions approaching single atoms with spatial resolution approaching Angstroms. Currently, the most widely used approaches for 3D characterization involve 2D projection or surface morphologic imaging with limited chemical mapping. Current metrology for characterizing nanostructures includes the transmission electron microscope (TEM), aberration corrected TEM, electron energy loss spectroscopy (EELS), atomic force microscope (AFM), and scanning tunneling microscope (STM). Emerging work in modeling the interaction of electron beams with nanostructured materials is helping interpret complex TEM pictures on nanostructured materials and these techniques may have value with other probe technologies.

Another significant issue is that in many emerging devices, the active component of the device is buried within other materials. For example, in molecular electronics, self-assembled monolayers (SAMs) are typically buried between two electrodes. Interfaces to all ERMs are very important to the operation of the devices, so understanding the resulting structure and composition is critical. At the nanometer scale, materials embedded between interfaces can be changed by the formation process or change during operation. It is not possible to measure these changes because most optical or electron probes lose spatial and compositional sensitivity as they travel through materials.

PROFILING OF LOCAL PROPERTIES

Spectroscopy techniques, such as optical absorption, Raman, ESR, NMR, and photoemission can provide information on chemical bonding and electronic properties, and band structure of large samples, and so measure collective properties. However, these spectroscopic techniques cannot measure these properties for individual nanometer sized materials as they interface with other materials. Most emerging research devices will be fabricated at the nanometer scale and local electronic and physical properties strongly impact the final device properties. For example, the potential drop as a function of position across a molecule or nanowire has a strong influence on its current-voltage characteristics. scanning tunneling microscopy provides near Angstrom resolution but effectively measures the local electron density and requires conductive substrates. Conductive atomic force microscopy can provide resistance but is limited to roughly 10 nm resolution in the lateral direction. Scanning Kelvin probe microscopy (SKPM) can profile local potentials but is also

limited to approximately 10 nm lateral resolution. Measurement of local quantities such as electronic densities of state, spin populations, and barrier heights as well as transport and dynamic properties such as electrical conductivity or transition times will be needed to determine whether materials have necessary performance for device applications. To characterize other material properties at the nanometer scale, AFM-like tools need to couple with other stimuli, such as magnetic fields, electric fields, etc., to create new probes such as nano-photoconductivity, and nano-internal photoemission.

METROLOGY FOR CHARACTERIZATION OF BAND STRUCTURE AND STATE PROPERTIES OF NANOSCALE MATERIALS

For emerging research materials, one of the most critical challenges is characterization of the response of these material components to the stimulus that will change the state as a function of the material, chemical, and structural variability. For example, fundamental understanding and characterization of transport through molecules has been limited by the lack of reproducible experiments and the inability to determine the source of the structural or electronic differences between these experiments. To achieve reproducible electrical measurements of emerging technologies requires a variety of robust test structures with associated measurement and analysis methodologies.

Different test structures are required to probe a variety of state properties including conductance, capacitance, spin, and high-frequency response. A fundamental challenge is to design and fabricate test structures that enable extraction of useful information from measurements. The nanoscale property measurement is dependent on the test structure and interfaces. For example, recent work has suggested that many of the reported transport measurements of molecules and semiconductor nanowires are limited by the contact rather than the intrinsic properties of the molecule or nanowire. Test structures, and associated measurement and analysis protocols must be designed so that they enable extraction of fundamental parameters that can be compared to theory and physical characterization. Correlation of these property measurements with physical parameters will enable the improvement of emerging research materials and devices with predictability of performance including variations at the nanoscale.

MODELING AND SIMULATION

Modeling and simulation are critical in both providing fundamental understanding of the physical mechanisms and processes for both charge-based and non-charge-based technologies and in interpreting metrology for nanotechnology nodes. As the size of materials for devices continues to decrease, the impact of interfaces on the measured material properties will make separation of "bulk" and interface properties much more difficult. As new material properties are characterized, models will need to be developed to guide synthesis thus enabling exploration of new structures and more complex interactions between materials. Establishment of an experimental database with results from well-characterized structures could accelerate the development of more accurate reduced and *ab initio* models. To get more quantitative material property mapping at the nanometer-scale requires development of models of probe interaction with nanostructured materials. Improved structure and property mapping for more accurate TEM, AFM, Conductance AFM, Kelvin Probe AFM, Magnetic Force Microscopy (MFM) and other new techniques could improve development of nanometer scale material models.

The material models for the more revolutionary computational state variable based devices, such as spin, molecular charge transport, and Orbitronic are very immature and will need significant correlation between measurement and phenomenological models to be useful. However, the relatively smaller number of atoms (for example, order of 10,000 for 10 nm devices) involved may open the door for use of *ab-initio* simulations of new materials and their interfaces.

At present empirical methods can simulate up to 1,000,000 atoms and density functional theory (DFT) and quantum Monte Carlo methods can simulate up to 1000 atoms. Current applications include: equilibrium energies, density of states, reaction rates, effects of defects, and transport within nanostructures and through interfaces. Despite recent advances, theory has many limitations that gate applicability to systems of practical interest for quantitative correlations. Among the most urgent shortcomings of existing theory are the description of excited states (bandgap energies), and realistic time scales to simulate fully dynamical systems to self-consistently bridge multiple time scales. Researchers also lack a consistent theoretical description to quantitatively describe the interfaces between the soft and hard/soft condensed matter systems. Such interfaces are characterized by a wide range of interactions from a very weak hydrogen bonding to strong covalent and ionic bonding (this covers several orders of magnitude in energy).

For 1D materials, research is needed to model the growth of NT and NW structures and the role of catalyst, temperature and CVD gas chemistry as was discussed in the *1D Charge State Challenge* section.

For correlated electron systems, models need to be developed that can explain the interactions between spin, charge, and lattice changes for potential use in spin wave propagation. This would need to quantify the energy associated with spin switching and transport and identify speed limitations.

In the early stages of a technology, modeling and simulation are often not sufficiently accurate to provide precise quantitative answers, but often can provide general qualitative assessment of property changes due to modifications in the structure, composition, or defects. Thus, modeling and simulation are expected to play a critical role with metrology in characterizing properties of emerging research materials.

EMERGING RESEARCH ARCHITECTURES

INTRODUCTION

This section on emerging research architectures is included because device choices in the future will be determined by the following hierarchy: applications →computer architecture → micro and nanoarchitecture → circuits → devices → materials. It is important to distinguish between the two ways in which the term "architecture" can be used. The term "computer architecture" includes all the systems elements, including software, needed to meet the needs of a given information processing application. "Micro- and nanoarchitecture" refers to the implementation details of how the various computing functions can be organized for high information throughput and minimum expense and energy cost. Currently, most all of the relevant publications in this area are concerned with what are best described as nanoarchitectures. These are assemblies of nanodevices, with device numbers at present typically in the range 10 to 10,000, although these numbers may be expected to increase. The assemblies are designed to implement basic functions such as logic, arithmetic, memory, image recognition, database searching, etc. It is generally assumed that these assemblies could subsequently be grouped into much larger assemblages. Table 61 summarizes these architectural approaches.

The characteristics of nanoscale devices and fabrication methods that must be considered in developing appropriate circuits and computing architectures include regularity of layout, manufacturing defects, unreliable device performance, device transfer functions, interconnect limitations, and thermal power generation. Regular layouts are favored because they are likely to be compatible with self-assembly methods that may have to be used at dimensions below those for which the standard "top-down" lithographic-defined subtractive processing techniques are used. The device performance is a consequence of both the physical principles and the inherent variability associated with the nanoscale, where it is estimated that significant quantities of devices, perhaps up to many percent, will suffer from manufacturing defects. In addition, in-service defects and transient errors will have to be overcome. Device transfer functions include the need for gain, input-output isolation, etc.,[148] so that workable circuits can be developed. Interconnect limitations come from the following two origins: 1) the geometrical challenge of accessing extremely small devices with connections that will transfer information at the needed speed and bandwidth, and 2) the transformation of interconnect dimensions from the nanoscale to the physical world of realizable system connections. Heat dissipation comes from the device switching energy and also the energy needed to drive signals through circuits. The limitations of nanoscale devices impose restrictions on organizations that are available for future architectures. Local computing tiles composed of simple device structures have been proposed that are interconnected with nearest neighbors through crossbar interconnect arrangements that bound the devices. Other organizations are inspired by biological systems, which have much larger circuit fan-out than used in today's technology.

For all nanoscale organizations, the management of defective and error-prone devices will be a critical element of any future architecture, since the defect rates are expected to be much higher than current practice. One characteristic feature of publications on nanoarchitecture is the emphasis on defect tolerance and to a lesser extent tolerance to transient faults. The goal of fault and defect-tolerant implementations is to enable reliable circuits and computing using unreliable devices. Defects can occur as permanent defects from hardware manufacturing, as defects that occur in-service, and as semi-permanent errors such as random charge hopping that affects single-electron transistors. In addition, transient errors (e.g., single event upsets (SEU)) may result from radioactive decay products or cosmic rays, or from noise, crosstalk, and power-supply or temperature fluctuations. Defective devices may be functional but still not meet the tolerance and reliability requirements for effective large-scale circuit operation. These effects are expected to be particularly acute for nano- and molecular scale devices and will require significant resources to control. Several techniques exist for overcoming the effects of inoperative devices. All of these techniques use the concept of redundancy in resources or in time. Reconfigurable computing (RCF, see below) is the archetypal technique for coping with manufacturing defects. Transient errors and in-service defects require different strategies. The most representative techniques are as follows: *R*-fold modular redundancy (RMR),[149] NAND multiplexing (NAND-M),[150] and error-correction coding for memory.[151]

In this context, redundancy usually means static redundancy—redundant rows and columns, for example. Dynamic redundancy is used to catch and correct problems "on the fly" and is a more expensive use of resources. It is not yet clear just how much dynamic redundancy will be needed at the nano and molecular levels until more nanodevice/nanocircuit data become available and improved computing models are developed.

ARCHITECTURES—DEFINITION AND DISCUSSION OF TABLE ENTRIES

FINE-GRAINED PARALLEL IMPLEMENTATIONS IN NANOSCALE CELLULAR ARRAYS

INTRODUCTION

For nanoscale devices, the integration level will probably be terascale (10^{12} devices/cm^2). For such large numbers of devices, many new information processing and computing capabilities are possible in principle that would not be considered at the gigascale level of integration. For many reasons, these devices will probably need to be interconnected mostly locally and patterned in grids or arrays of cells. There are three main classes of fine-grain structure. One class consists of completely regular, grid-like arrays, completely filled with very simple elements that typically interact only with their four nearest neighbors. This class includes some types of quantum cellular automata (QCA), with simple quasi-binary elements, and the much larger group of cellular neural (or nonlinear) networks (CNN), whose elements are typically much more powerful processors, whether digital, analog, or a combination of the two. The second class consists of QCA elements that are arranged in groups in a complicated and typically sparse layout, controlled by overlying/underlying electric or magnetic fields. The third type of nanoarchitecture is the programmable gate logic array (PGLA) structure, in which small blocks of crossbar or grid-connected elements are arranged, that are subsequently programmed to implement various logic functions, then connected as required using additional programmable crossbars. Given its importance and pervasiveness, the PGLA structure is discussed below in a separate section entitled *Reconfigurable Computers*.

QUANTUM CELLULAR AUTOMATA

The QCA paradigm is one in which an array of cells, each interacting with its neighbors, is employed in a locally interconnected manner. Such cells are typically envisioned to be electrostatically coupled quantum dots,[152, 153, 154, 155] magnetic field coupled nanomagnets,[156, 157] or various molecular structures.[158] Some electronic and magnetic QCA circuits have been fabricated, but there are questions, as yet unresolved, about the utility of QCA architectures. One problem is that although it is sometimes claimed that these systems are potentially very low power, in practice a complex system of control clocking fields would have to be generated, involving additional wiring and operational heat dissipation. A second problem is that fully-filled arrays of QCA elements are only capable of implementing a very limited set of algorithms, while the theoretically more useful class of sparsely-filled QCA structures will require additional patterning processes to form the spatially non-uniform set of QCA elements. A third problem is that electronic QCA would ideally operate in an adiabatic quantum evolution but are likely to be coupled quasi-isothermally to their environment. It has been shown for magnetic QCA running at 300 K, that this isothermal evolution results in a drastic performance slowdown (from a theoretical ~1 GHz to ~100 kHz); similar processes are likely to affect electronic QCA systems.

CELLULAR NONLINEAR NETWORKS

A CNN is an array of mainly identical dynamical systems called cells that satisfy two properties as follows: 1) most interactions are local, within a distance of one cell dimension, and 2) the computational state variables can be continuous valued signals (not necessarily digital). A template specifies the interaction between each cell and all its neighbor cells in terms of their input, state, and output variables. The interaction between the variables of one cell may be either a linear or nonlinear function of the variables associated with its neighbor cells. A cloning function determines how the template varies spatially across the grid and determines the dynamical response of the array to boundary values and initial conditions. Since the range of interaction and the connection complexity of each cell are independent of the number of cells, the architecture is potentially scalable, although providing defect tolerance requires extra component redundancy. Programming the array consists of specifying the dynamics of a single cell, the connection template, and the cloning function of the templates. This approach is simpler than traditional VLSI design methodology since the functional components are simple and reusable.

CNNs can be used to implement Boolean logic and functions such as majority gates, MUX gates, and switches. CNNs can simulate many mathematical problems such as diffusion and convection and nervous system functions. The CNN organization also lends itself to implementing defect management techniques as discussed below. Devices that might be used include quantum dot QCAs, SETs,[159] and RTDs. Tunneling phase logic has been combined with CNN to enable

neural-like spike switching waveforms and low power dissipation,[160] although more recent work suggests that tunneling phase logic may have significant constraints on the minimum allowable power.[161]

One caution concerning CNNs is that despite the potential applications discussed above, the only published applications to date have been for analog image processing. However, algorithms for pattern recognition and analysis can be implemented very efficiently in CNNs, and an enormous body of relevant literature exists for mesh-connected, purely digital, processor arrays, which are the antecedents of CNNs.

RECONFIGURABLE COMPUTERS

Far and away the most frequently researched class of nanoarchitecture is the reconfigurable (RCF) architecture, typically based on the use of programmable gate logic arrays, and inspired by the CMOS-based massively parallel Teramac of 1995-1998.[162] The use of PGLAs, or variations on the same theme, is an important characteristic of most current nanoarchitecture designs. These designs typically use crossbar structures, not only for routing signals between PGLA blocks, but also inside the blocks themselves, because the use of simple, regular, crossbar structures is believed to offer the best chance for eventually fabricating nanocomputers with more than 10^{10} devices on a chip. Table 62, which is organized on a chronological basis, summarizes the characteristics of some recent nanoarchitecture concepts and implementations, many of which use crossbar and PGLA-like structures that could be used in a reconfigurable computer system.

BIOLOGICALLY INSPIRED ARCHITECTURE IMPLEMENTATIONS

Biologically inspired computing implies emulation of human and biological reasoning functions. Such architectures possess basic information processing capabilities that are organized and reorganized in goal-directed systems. The living cell is the biological example of a goal-directed organism and has the features of flexibility, adaptability, robustness, autonomy, and interactivity. The programming model does not involve millions of lines of code but rather modules of encoded instructions that are activated or deactivated by regulatory modules to act in concert with an overall goal-directed system. Algorithms inspired by computational neurobiology have been the first approach to computing systems that exhibit such behavior, implemented either as unique processors or on general-purpose architectures. However, there is an enormous gap in understanding of how biological pathways or circuits function, so there is much learning needed before this knowledge can be captured in useable computing systems.

At the nanoscale, devices are more stochastic in operation and quantum effects become the rule rather than the exception. It is unlikely that existing computational models will be an optimal mapping to these new devices and technologies, and this is the motivation for biologically inspired algorithms. Although biological neural circuits use loosely coupled, relatively slow, globally asynchronous, distributed computing with unreliable (and occasionally failing) components, mimicking their behavior in non-CMOS hardware, in particular copying their enormous fan-in/fan-out, is still in its infancy. Furthermore, even simple biological systems perform highly sophisticated pattern recognition and control. Biological systems are self-organizing, tolerant of manufacturing defects, and they adapt, rather than being programmed, to their environments. The problems they solve involve the interaction of an organism/system with the real world.[163]

In comparison with digital computers, the basic components of biological systems—neurons, synapses, axons, and dendrites—are very slow, with time frames in the milliseconds range. Somewhat surprisingly, although the human brain only consumes 10–30 W while carrying out functions that are extremely difficult or as yet impossible to emulate with conventional computers, individual synapses are relatively inefficient, consuming approximately 10^{-15} J of energy per bit of information that they generate.[164]

The interconnect capabilities of biological architectures are the key to their massive parallelism. The connectivity of neurons in humans provides the best-known example of this. One cubic millimeter of cortex contains about 10^5 neurons and 10^9 synapses (10^4 synapses/neuron) and the human cortex has about 10^{10} neurons and 10^{14} synapses. Thus the fan-out per neuron ranges from 1,000 to 10,000 in humans.[165] This amounts to about 1–10 synapses/μm^3. Many neurons are not connected to nearest neighbors but rather to different cell classes required to execute the goal-directed function. This enormous interconnectivity requires a different approach to managing information and algorithmic complexity than is implemented in current computing systems. In addition, the large fan-out will require either large-gain devices or circuit approaches based on additional signal processing mechanisms, and new three-dimensional connection structures will have to be devised.

The feasibility of using nanoscale electronic devices and interconnects to implement such massively parallel, adaptive, self-organizing computational models is starting to become an active research area. In general, such architectures should

be of interest for complex digital and intelligent signal processing applications such as advanced human computer interfaces. These interfaces will include elements such as computer recognition of speech, textual, and image content as well as problems such as computer vision and robotic control. These classes of problems require computers to find complex structures and relationships in massive quantities of low-precision, ambiguous, and noisy data.

Implementations of biologically inspired systems can be either entirely analog or digital, or a hybrid of the two.[166] Each has its advantages and disadvantages. Analog has more density than digital, and many of the algorithmic operations, such as leaky integration, that often appear in this class of algorithms, can be implemented very efficiently in analog, but digital representation of computations allows more flexibility and allows multiplexing of expensive computer hardware by a number of network nodes. This is particularly attractive when the network is sparsely activated. On the other hand, analog is much harder to design and debug due to the lack of mature design tools. Also analog quantities are much more difficult to store reliably and bit precision may not be acceptable with small numbers of electrons and low values of voltage and current. Digital implementations use many more transistors and power per operation and must eventually interface with analog signals in the real world.

The communications functions, even in analog systems, are best performed digitally. Most neurons communicate via inter-spike-intervals using the time between pulses to represent a signal versus current or voltage. This type of signaling is noise tolerant and may scale to single electron systems. However single-electron systems do not have the gain required to drive large fan-out circuits typical of biological implementations. Relatively little work has been performed on nanoscale devices and circuits that would provide such functions.[167]

COHERENT QUANTUM COMPUTING

Coherent quantum devices rely on the phase information of quantum wavefunctions to store and manipulate information. The phase information of any quantum state is called a "qubit." The core idea of quantum information processing or quantum computing is that each individual component of an infinite superposition of wavefunctions is manipulated in parallel, thereby achieving massive speed-up relative to conventional computers. The challenge is to manipulate wavefunctions so that they can perform a useful function and then find a way to read out the result of the calculation. A further challenge is that only a small number of algorithms have been found, for which quantum computing offers performance benefits over conventional computers. A comprehensive description of the current state of development of quantum computing in all its aspects, including architecture, is given in the Quantum Information Science and Technology Roadmap,[168] to which the reader is referred.

TRENDS

As can be seen from Table 62, the main trend is the development of nanoarchitectures that are based on crossbar, or crossbar-like, architectures that can be programmed to implement PGLA-like logic or memory functions. The table, which includes only a sample of reported developments, is in chronological order, and illustrates the rapid increase in sophistication and complexity of the circuit analyses over the last two or three years. At present most of these structures have only been analysed theoretically, but it is expected that more nanoarchitectures will be implemented when experimental devices start to be fabricated in larger numbers. Most of these nanoarchitectures have interfaces between high-density nanodevices and lower-density CMOS I/O or control devices. Perhaps the most promising feature of recent publications is the indication that high manufacturing defect rates can probably be managed, with relatively modest device, space, and power overheads. It has frequently been argued that parallelism will provide enormous benefits, by overcoming possible speed limitations of relatively slow nanodevices. This is probably true for a significant number of applications (e.g., image processing, database searching), but some applications (for example, data compression on serial data streams) may benefit only marginally from parallelism; further research is needed in this area.

Physical, technological, and practical constraints on devices and systems have indirect implications for architectures (in particular, the amount of effective parallelism) that might be used in the future. These constraints include principles and processes such as the Heisenberg uncertainty principle, thermally-induced current or voltage fluctuations, shot noise, or user-comfort constraints such as a maximum heat dissipation of ~100-200 W for a desktop PC.[169, 170, 171, 172] There are proposals to decrease power consumption and heat dissipation based on charge recovery[173] and reversible[174] or adiabatic[175] computing. Concerns about the feasibility of reversible and adiabatic schemes can be found in the literature.[176, 177, 178] In summary, the ultimate limits of practical nanodevice performance, and their implications for new architectures, have not yet been fully assessed.

Table 61 Emerging Research Architecture Implementations

Architecture Implementations	*Quantum Cellular Automata*	*Cellular Nonlinear Networks*	*Reconfigurable Implementations*	*Biologically Inspired Implementations*
Application Domain	Complex signal processing	Fast image processing Associative memory Complex signal processing	Reliable computing with unreliable devices Historical example: Teramac FPGA implementation	Goal-driven computing using simple and recursive algorithms High computational efficiency for certain applications
Device And Interconnect Implementations	Arrays of nanodots or molecular assemblies	Resonant tunneling devices, SETs	Molecular switches Crossed arrays of 1D structures Switchable interconnects	Molecular organic and bio-molecular devices and interconnects
Information Throughput	Fan-out =1 throughput constrained by adiabatic clocking requirements	Fan-out close to unity	Fan-out variable but performance degraded slightly by need for defect management schemes	Massive parallelism Requires some long-range data transfer Fan-out very high in brains ($\sim 10^4$)
Power	Power comparable to scaled CMOS (~0.2 MIPS/mW) Data streaming applics will need ~100 MOPS/mW	Power comparable to scaled CMOS (~0.2 MIPS/mW) Data streaming applics will need ~100 MOPS/mW	Only preliminary estimates, but these are encouraging	High parallelism allows lower operational speeds Power consumption of human brain 10–30 W at millisecond rates
Interconnects	No local interconnects, but many control lines are needed	Local interconnects with neuron-like waveforms	Interconnects by crossed arrays	Interconnects distributed over a range of distances
Error Tolerance	Sensitive to background charge Low temperature operation	Not determined	Multiple modular redundancy and multiplexing for transient errors	Highly dynamical neural-like systems Implement adaptive self-organization, fault tolerance
Defect Tolerance	Not demonstrated	Not determined	Reconfiguration (RCF)	Inherently insensitive to defects through adaptive algorithms
Manufacturability	Precise dimensional control needed	Tight tolerances on tunnel rates of all junctions to minimize jitter	Self assembly possible	Not demonstrated
Comments	Only limited programming models	Locally active and locally connected Cell and array design immature (no fan-out)	Supports memory-based computing Applications in dependable systems	Backed by extensive neural network research Algorithmic implementations need more research
Maturity	Demonstration	Demonstration	Demonstration	Concept
Test	Not demonstrated	Demonstrated only for image processing	Self-test or requires extensive pre-computing test	Test functions are included in the adaptive algorithms used
Research papers (2003-2005)	QCA – 89 (QCA and nano – 39)	CNN – 215 (CNN and nano – 11)	Reconfigurable – 3228 (Reconfigurable and nano – 53)	Bio-inspired or neuromorphic – 158 (Bio-inspired or neuromorphic and nano – 20)

Table 62 Circuit and/or Architecture Implementations—Theory and Experiment

Structure type	*Device type*	*Theory /Experiment*	*Size*	*Defect Tolerant*	*Comments*	*References*
Crossbar non-volatile memory	Crossed CNTs, using van der Waals forces to latch	Experiment and theory	Single experimental devices	NA	Only one refereed publication	Rueckes[179]
Logic gates	Crossed CNTs	Experiment	4 devices	NA	Early nanowire logic demonstration	Bachtgold[180]
Logic gates	Crossed Si nanowires	Experiment	3 devices	NA	Early nanowire logic demonstration	Huang[181]
Crossbar hybrid molecular-CMOS blocks	Resistors + RTDs	Theory	~100 K devices	Assumed reconfiguration	"NanoFabric," "NanoBlock"	Goldstein[182]
Crossbar memory	Rotaxane molecules	Experiment	8×8 bit	~10%	Bistable tunnel junctions	Luo[183], Chen[184]
Logic blocks with CMOS I/O	Randomly overlapped molecular NDR resistors	Theory + Experiment (single devices)	Single devices (experiment); 1-bit adder, NAND gate (theory)	> 50 % for successful NAND gate operation	"Nanocell"	Tour[185]
Crossbar address decoder	Crossed Si nanowire FET	Experiment	4×4 wire	NA	~250 nm wire spacing	Zhong[186]
Crossbar nanowire arrays	NA	Experiment	~10×10 wires at 20 nm pitch	NA	Wires down to 16 nm pitch	Melosh[187]
Neuromorphic crossbar structures	SET latches	Theory	3744 neurons modeled	~40%	Overlapping nano and micro crossbars: "CrossNet"	Turel[188]
Crossbar /PGLA	n-type, p-type molecular FET	Theory	4-bit micro-processor	~10%	Estimated area ~1% of current PGLAs.	Snider[189]
Error-correcting logic blocks	Not specified	Theory	ALU; pipeline control stage	~3%	"NanoBox"	KleinOs[190]
Flexible architecture for digital, analog, mixed-signal	Not specified	Theory	12 devices	~4%	Would need 3D structures	Beiu[191]
PGLA-like logic arrays	e.g., cross bars with molecular devices	Theory	e.g., 4×4 bit multiplier	20% dead devices	"NanoPLA"	Naeimi[192]
Nanowire FET arrays	Metal to Si nanowire	Experiment	~3000 transistors	~80% yield	Uses Langmuir-Blodgett to align nanowires	Jin[193]
Crossbar memory arrays	e.g., NW FETs	Theory	~Gbit memory	~5% junction defect rate	Estimated 0.6 W per Tbit/s read rate	DeHon[194]
Crossbar latch	Metal-molecule-metal junction	Experiment	Single device	NA	Logic storage, restoration /inversion	Kueckes[195]
Hybrid molecular- CMOS digital crossbar logic	SET latch	Theory	64-bit full adder modeled	~20%	Developed from NetCell	Strukov[196]
SET logic circuits	SET	Experiment	4 dual-gated SETs	NA	AND, NAND gates operate at 1.9 K	Nakajima[197]
Crossbar circuits	Resistor or diode molecules etc.	Theory	4-bit microproc.	~3%	Uses non-exhaustive coding	Snider[198]

Refer to the Endnotes section for references.

EMERGING TECHNOLOGIES—A FUNCTIONAL COMPARISON

INTRODUCTION

The technological challenges for the information processing industry in the post CMOS-scaling era are quite difficult because it is not clear what needs to be done. This section relates some of the new information processing technologies to each other and to scaled CMOS using four application-driven parameters to gain an overall perspective on the issues and opportunities.

There is a growing consensus that from about 2020 forward, information-processing technology will consist of a heterogeneous set of novel and widely disparate device technologies integrated on a silicon platform consisting of very fast, very small, and very low-cost CMOS devices. These novel devices will span a very broad range of materials, operational principles, functionalities, logic systems, data representations, and architectures. In general, their characteristics will be complementary to scaled CMOS, perhaps extending CMOS to new applications. However, none of the new technologies currently being explored is thought to have a real possibility of replacing silicon CMOS.

FUNCTIONAL PARAMETERIZATION AND COMPARISON

Figure 52 shows a parameterization of a selected set of emerging technologies and CMOS in terms of speed, size, cost, and switching energy.[1] Two of the technologies are introduced in the *Logic* and *Architecture* sections (molecular and quantum) and three others (plastic, optical, and NEMS) are briefly introduced in this section. (Biologically Inspired computing is also described in the Architecture section, and, like CMOS, is plotted for the purpose of reference comparison; RSFQ has been dropped from the Logic section.) The first three parameters in this figure are used to define a 3D space and the fourth parameter, switching energy, is displayed as color code shown in the legend. All the scales are logarithmic and cover many orders of magnitude as shown in the graph. Each of the technologies displaces a certain volume in this parameter space and is color-coded in a solid color representing the energy required for a single gate operation. Each of the volumes is also projected onto the bounding 2D planes so that quantitative values can be determined. The projections of the volume corresponding to a given technology are shown as rectangles filled with the same color as the corresponding volume.

In the absence of firm measured data, a number of assumptions were made to estimate the parameters for the emerging technologies. The parameters used for each technology are listed in Table 63. If an emerging technology is in the conceptual stage with no measured data, the parametric assumptions are based on the underlying physical principles. If some measured data exists, the assumptions involve an estimate on how far the technology can be scaled. In this case, the scaling arguments are based on physical principles.

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[1] *Mr. David Jaeger of North Carolina State University is gratefully acknowledged for providing technical support in the preparation of Figure 52.*

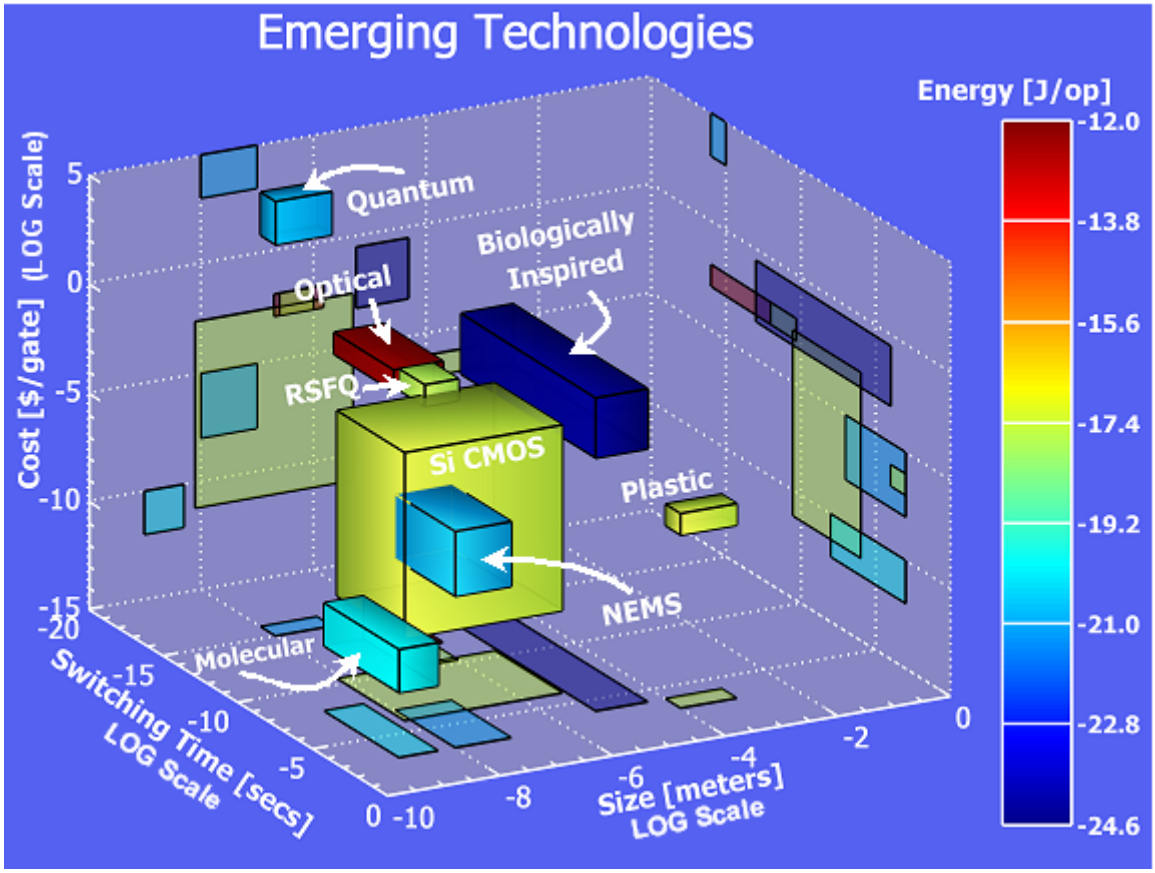

Figure 52 Parameterization of Emerging Technologies and CMOS— Speed, Size, Cost, and Switching Energy

Several of the technologies listed are strongly tied to a single application area or niche where the technology is particularly effective. For example, quantum computing can be used to find prime factors very efficiently by means of Shor's algorithm but is much less efficient used for other applications. In this case, an "effective" time per operation is defined as the time required by a classical device in a classical architecture using a classical algorithm to do the calculation. Therefore the "effective" operation time of an N-qubit quantum computer factoring a large number is very much faster than the operation time of an N-gate classical computer because of the inherent parallelism associated with quantum computing. Similar arguments can be made for biologically inspired and optical computing.

This figure conveys meaningful information about the relative positions of the emerging technologies in this application space. It shows that few of the new technologies are directly competitive with scaled CMOS and most are highly complementary. It also shows very clearly the benefit to be derived from heterogeneous integration of the emerging technologies with silicon to expand its overall application space. Figure 52 and Table 63 represent initial estimates for the comparison of these very disparate technologies. In addition to this comparison, the further intent of this figure and table is to stimulate substantive discussion of the basis and means for making this comparison.

Table 63 Estimated Parameters for Emerging Research Devices and Technologies in the year 2016

Technology	T_{min} sec	T_{max} sec	CD_{min} m	CD_{max} m	Energy J/op	Cost min $/gate	Cost max $/gate
Si CMOS	3E-11[2]	1E-6	8E-9	5E-6	4E-18	1E-11	3E-3
RSFQ	1E-12	5E-11	3E-7	1E-6	2E-18	1E-3	1E-2
Molecular	1E-8	1E-3	1E-9	5E-9	1E-20	1E-12	1E-10
Plastic	1E-4	1E-3	1E-4	1E-3	4E-18	1E-7	1E-6
Optical (digital, all optical)	1E-16	1E-12	2E-7	2E-6	1E-12	1E-3	1E-2
NEMS (conservative)	1E-7	1E-3	1E-8	1E-7	1E-21	1E-8[3]	1E-5
Biologically Inspired	1E-13	1E-4	6E-6	5E-5	unknown	5E-4	3E-1
Quantum	1E-16	1E-15	1E-8	1E-7	1E-21	1E3	1E5

In this table T stands for system cycle time (switching time), CD stands for critical dimension (e.g., physical gate length), Energy is the intrinsic operational energy of one device, and Cost is defined as $ per gate.

DEFINITION AND DISCUSSION OF TABLE ENTRIES

Plastic Transistors—Plastic transistors are defined to be thin film transistor (TFT) devices fabricated on plastic substrates. The active layer of the TFT can be amorphous or poly-Si as well as organic semiconductors. Often, the TFTs are combined with organic light emitting diodes (OLEDs) to form intelligent, flexible display devices than can be bent, folded, worn, or conformally mapped on to arbitrarily shaped surfaces. All-plastic chips based entirely on organic materials have already been demonstrated whose mechanical flexibility offers totally new perspectives to, for example, the rapidly growing market of identification and product tagging as well as for pixel drivers for flexible displays.[199] Typical devices have a supply voltage of 10 V and critical dimensions of 100 μm with reasonable electron mobilities and I-V characteristics. Pentacene-based plastic transistors with I_{on}/I_{off} current ratio $>10^5$ at operating voltage ranges as low as 5 Volts have been reported.[200] Analog and digital circuits using organic (pentacene) transistors on polyester substrates have been fabricated and characterized. The highest operation frequency reported to date for organic circuits on plastic substrates is 1.7 kHz.[201] Plastic transistors have the potential to provide very low-cost, rugged large area electronics that have many potential applications.[202, 203] A process technology consisting just of printing operations on paper-based substrates would have an intrinsic cost structure similar to color inkjet printing today. It could support disposable devices such as periodicals and dynamic bar codes.

Optical[204]—Optical computing is based on using light transmission and interaction with solids for information processing. The potential advantages of digital optical computers relate to the following properties of light as a carrier of information:

- Optical beams do not interact with each other
- Optical information processing functions can be performed in parallel (e.g., performing a Fourier transform)
- Ultimate high speed of signal propagation (speed of light)

It should be noted that what is called the all-optical computer still contains electronic components, such as lasers and nonlinear elements in which a material's optical properties are affected by charge carriers or atoms interacting with light. Some disadvantages of digital optical computing include the following:

- The relatively large size of components (e.g., optical switch) arising from diffraction limitation
- Potential of high-speed computation can be realized only at the expense of dissipated power. For example, in an optically controlled phase change material (switch or memory), faster rearrangement of atoms in a cell requires a larger supply of energy. In a practical device "computing at the speed of light" is unlikely since it would require a huge operational energy.

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[2] *T_{min} for silicon CMOS is based on the local clock rate for the 22 nm node (physical gate length < 9 nm), and not upon CV/I intrinsic switching time.*

[3] *Estimated on the principle of reasonable cost and assumed two-dimensional architecture of NEMS computer.*

Near-term opportunities in optoelectronics are in integration of photonic components with sub-100 nm CMOS. Another opportunity arises from using optically controlled phase-change materials, such as phase change memory (PCM). Another direction is perfection of existing analog optical computers, which perform Fourier processing much faster than electronics. Analog optical computers are fast and operate with continuous data, while their accuracy is not comparable to that of digital computers.

Nano-electro-mechanical systems (NEMS)—In the concept of the nanomechanical computer, mechanical digital signals are represented by displacements of solid rods, and the speed of signal propagation is limited to the speed of the sound (for example, 1.7×10^4 m/s in diamond). Optimistic estimates predict NEMS logic gates that switch in 0.1 ns and dissipate less than 10^{-21} J and computers that perform 10^{16} instructions per Watt (compared to 5×10^{12} instruction per Watt in human brain operation). This estimated switching energy is below the thermodynamic limit of $kT\ln2$ for irreversible computation. It is believed[205] that this low dissipation is possible because NEMS computation is logically reversible. More conservative estimates of characteristics of the NEMS computers can be made based on recent demonstration of a VLSI-NEMS chip for parallel data storage.[206] Reported storage densities are 500 Gbit/in^2. The highest data rates achieved so far are 6 Mbit/sec. A summary of the conservative estimates of parameters of the NEMS computers is given in Table 63.

Rapid Single Flux Quantum (RSFQ)[207]—RSFQ logic is a dynamic logic based upon a superconducting quantum effect, in which the storage and transmission of flux quanta (Fluxon) defines the device operation. The basic RSFQ structure is a superconducting ring that contains one Josephson Junction (JJ) plus an external resistive shunt. The storage element is the superconducting inductive ring and the switching element is the Josephson Junction. RSFQ dynamic logic uses the presence or absence of the flux quanta in the closed superconducting inductive loop to represent a bit as a "1" or "0," respectively. With RSFQ, circuit speeds above 100 GHz, perhaps up to 800 GHz, are possible, which is their principal advantage. However, their ultimate scaling density appears to be limited due to factors that also limit their binary information throughput to be much less than that for scaled silicon. There also appears to be no viable way to avoid cryogenic operation, which imposes a substantial cost burden. Commercial application to niche applications where speed is the dominant requirement is likely to continue but wide-scale application is unlikely.

Biologically Inspired—(see the *Architecture* section for further discussion) The human brain is defined to be the archetypal *biologically inspired* or *neuromorphic* information processing device and is included here to provide a basis of comparison with silicon-based information processing systems. The scale length of individual neurons is estimated from the volume of the brain and the estimated number of neurons. It is possible to derive an "effective operation time" of biologically inspired computing as explained in the overview of this section. In that case, the reference operation is vision processing where there is a great deal of information relating to technological systems. The effective times defined in this way are very much faster that the synaptic speed and reflects that the interconnect density of the human brain is very much greater than any silicon-based system. The speed quoted in Table 56 for T_{min} is based on the estimated information-processing rate of 1×10^{13} bits per second[208] related to vision processing. Similarly, the speed quoted in Table 63 for T_{max} is the experimentally observed time scale for opening and closing of synapses. Each neuron will connect to between 100 and 10,000 synapses, one of the primary ways in which the architecture of the human brain differs from silicon-based systems.

The fundamental parameters of the human brain[209] are estimated to be:

- Number of neurons—2E10
- A single neuron can make 100 to 10,000 synaptic connections
- Mass—1.3 kg[210]
- Volume—1600 cm^3
- Power consumption—15–30 Watts
- Information stored—1E12 (short term) bits
- Information process speed—1E13 bits/second

The set of secondary parameters shown in Table 63 is based on the fundamental parameters above.

EMERGING TECHNOLOGIES—A CRITICAL REVIEW

INTRODUCTION

While the role of nanoscale devices in meeting future computing and communications applications is not clear at this point, undoubtedly there will be many needs that could benefit from the terascale level of integration that such devices

offer. As discussed in the previous section, these devices will encompass a broad range of fabrication methodologies and functional modalities. They may extend scaled CMOS to new applications in a highly complementary fashion. Conversely, there are significant limitations that arise with nanoscale devices that will impact their usefulness. In particular, as mentioned above, their near-term applications will require nanoscale devices to be functionally and technologically compatible with silicon CMOS. In the longer term, charge-based nanoscale devices may be supplemented with one or more new information processing technologies using a quite new logic "computational state variable" or means of representing a unit of information (a bit). The purpose of this section, therefore, is to introduce a set of technology evaluation criteria (see notes for Tables 64 and 65) and, based on these criteria, to offer a critical assessment of those technology entries for memory and logic being considered for post CMOS-scaling information processing. Additionally, charge-based approaches will be discussed in this section separately from those approaches proposing use of a new means for data representation or "computational state variable." This separate discussion addresses an important question related to new charge-based information processing approaches concerning the fundamental limits of an elemental switch (size, energy, speed, etc.).

TECHNOLOGIES BEYOND CMOS

OVERALL TECHNOLOGY REQUIREMENTS

Scalability—First and foremost the major incentive for developing and investing in a new information processing technology is to discover and exploit a new domain for scaling information processing functional density and throughput per Joule substantially beyond that attainable by CMOS. Silicon-based CMOS and related technology has provided several decades of scaling of MOSFET densities. The goal of a new information processing technology is to replicate this success by providing additional decades of functional and information throughput rate scaling using a new technology.

Gain (Logic Devices)—The gain of nanodevices is an important limitation for current combinatorial logic where gate fan-outs require significant drive current and low voltages make gates more noise sensitive. New logic and low-fan-out memory circuit approaches will be needed to use most of these devices for computing applications. Signal regeneration for large circuits may need to be accomplished by integration with CMOS. In the near-term integratability of nanodevices to CMOS silicon is a key requirement due to both the need for signal restoration for many logic implementations and also the established technology and market base. This integration will be necessary at all levels from design tools and circuits to process technology.

OFF/ON Ratio (Memory Devices)—The OFF/ON ratio of a memory device is the ratio of the access resistance of a memory storage element in the OFF state to its access resistance in the ON state. For non-volatile memories, the OFF/ON ratio represents the ratio between leakage current of an unselected memory cell to the read current of a selected cell. This definition will apply to new memory technologies so long as they have a selection device. In cross-point memories, a very large OFF/ON ratio is required to minimize power dissipation and maintain adequate read signal margin.

Power Limitations—Clock speed versus density trade-offs for electron transport devices will dictate that for future technology generations, clock speed will need to be decreased for very high densities or conversely, density will need to be decreased for very high clock speeds. Nanoscale electron transport devices mostly fit into the former category and will best suit implementations that rely on the efficient use of parallel processing more than on fast switching.

Device Transfer Function—Nanoscale devices may perform circuit functions directly due to their nonlinear outputs and therefore save both real estate and power. In addition, nanodevices that implement both logic and storage in the same device would revolutionize circuit and nanoarchitecture implementations.

Error Rate—The error rate of all nanoscale devices and circuits is a major concern. These errors arise from the highly precise dimensional control needed to fabricate the devices and also from interference from the local environment, such as spurious background charges in SETs. Large-scale error detection and correction schemes will need to be a central theme of any architecture and implementations that use nanoscale devices.

Operation Temperature—Nanodevices must be able to operate at or close to room temperature for most practical applications.

CMOS Technological and Architectural Compatibility—The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principle economic benefit of such an approach is it allows the industry to fully apply previous technology investments to future products. An alternative

technology as a goal should utilize the tremendous investment in infrastructure to the highest degree possible. The need for CMOS architectural compatibility is motivated by the same set of concerns that motivate the CMOS technological compatibility, namely the ability to utilize the existing CMOS infrastructure. The architectural compatibly is defined in terms of the logic system and data representation used by the alternative technology. CMOS utilizes Boolean logic and a binary data representation and ideally, the alternative technology would need to do so as well.

CHARGE-BASED NANOSCALE DEVICES

An important issue regarding charge-based nanoelectronic switch elements is related to the fundamental limits to the scaling of these new devices, and how they compare with CMOS technology at its projected end of scaling. The 2005 ITRS projects the scaling of CMOS slightly beyond the 16 nm node. This node represents a physical gate length for a MPU/ASIC device of 6 nm with an average power dissipation of approximately 100 W/cm^2. A recent analysis[211] concludes that the fundamental limit of scaling a charge-based switch is only a factor of 5× smaller than the physical gate length of a CMOS MOSFET in 2020. Furthermore the density of these switches is limited by maximum allowable power dissipation of approximately 100 W/cm^2, not by their size. The conclusion of this work is that MOSFET technology scaled to its practical limit in terms of size and power density will closely reach the theoretical limits of scaling for charge-based devices. Consequently, application of *emerging charge-based* logic technologies, such as 1D structures (nanowires and nanotubes) and molecular structures may be best suited for use as a replacement of the silicon channel in an otherwise silicon-based MOSFET technology infrastructure. In other words, use of 1D or molecular structures for *charge-based switches* to develop a completely new information processing technology, including binary switches, memory elements, interconnects (local and global) may not be justified to obtain a relatively modest maximum of 5× scaling in size or speed. This conclusion is particularly true since the device density is limited by power dissipation and not by the size of the binary switch. The corollary of this observation is that the search for alternative logic devices should embrace the concept of using state variables other than electric charge.

ALTERNATE COMPUTATIONAL-STATE-VARIABLE NANOSCALE DEVICES

In this context, the term "computational state variable" refers to the notion of the finite state machine introduced by Turing in 1930s. The idea is that there are numerous ways to manipulate and store computational information or logic state. The earliest example of a finite state storage device was the abacus, which represents numerical data by the position of beads on a string. In this example, the computational state variable is simply a physical position, and the operator accomplishes readout by looking at the abacus. The operator's fingers physically move the beads to perform the data manipulations. Early core memories used the orientation of magnetic dipoles to store state. Similarly, paper tapes and punch cards used the presence or absence of holes to store the state of the computational variable.

POTENTIAL PERFORMANCE ASSESSMENT FOR MEMORY AND LOGIC DEVICES

The purpose of this section is to assess the potential performance associated with each new memory and logic nanoscale device technology discussed for post-CMOS scaling applications in this chapter. This assessment of potential performance can help inform industrial evaluation of each nanoscale device technology and the industry's investment decisions among the many competing approaches. The Relevance Criteria and Technology Performance Evaluation are given and defined below.

RELEVANCE CRITERIA

Post CMOS-scaling nanoscale devices span multiple applications, computational state variables, and technologies and are extremely diverse in nature. A set of nanoelectronics relevance conditions has been defined to parameterize the extent to which a given technology is applicable to information processing applications, particularly those in the near term.

Each post CMOS-scaling nanoscale memory and logic technology is evaluated against each Relevance Criteria according to a single factor. This factor relates to the *projected potential performance* of each nanoscale device technology, assuming its successful development to maturity, for each Relevance Criterion, *compared to that for silicon CMOS at 22 nm for logic or, for memory, the comparable existing memory technology*. Performance potential is assigned a value from 1–3, with "3" substantially exceeding CMOS at 22 nm, and "1" substantially inferior to CMOS or, again, a comparable existing memory technology (see below). The Relevance Criteria are defined in the notes of Tables 64 and 65. This evaluation is determined by a poll of members of the ERD working group composed of individuals of a variety of technical backgrounds and expertise.

Logic—Individual Performance Potential for Logic Related to each Technology Evaluation Criterion

3	Substantially exceeds CMOS * *or* is compatible with CMOS architecture ** *or* is monolithically integrable with CMOS wafer technology ****or* is compatible with CMOS operating temperature **(**i.e., **Substantially Better than Silicon Logic**)
2	Comparable to CMOS * *or* can be integrated with CMOS architecture with some difficulty ** *or* is functionally integrable (easily) with CMOS wafer technology ****or* requires a modest cooling technology, T ≥ 77K (i.e., **Comparable to Silicon Logic**)
1	Substantially (2×) inferior to CMOS * *or* can not be integrated with CMOS architecture ** *or* is not integrable with CMOS wafer technology ****or* requires very aggressive cooling technology, T < 77K (i.e., **Substantially Worse that Silicon Logic**)

Memory—Individual Performance Potential for Memory Related to each Technology Evaluation Criterion

3	Substantially exceeds the appropriate Baseline Memory Technology * *or* is compatible with CMOS wafer technology ** *or* is monolithically integrable with CMOS wafer technology ****or* is compatible with CMOS operating temperature **(**i.e., **Substantially Better than Silicon Baseline Memory Technology**)
2	Comparable to the appropriate Baseline Memory Technology * *or* can be integrated with CMOS architecture with some difficulty ** *or* is functionally integrable (easily) with CMOS wafer technology ****or* requires a modest cooling technology, T ≥ 77K (i.e., **Comparable to Silicon Baseline Memory Technology**)
1	Substantially (2×) inferior to the appropriate Baseline Memory Technology * *or* can not be integrated with CMOS architecture ** *or* is not integrable with CMOS wafer technology ****or* requires very aggressive cooling technology, T < 77K (i.e., **Substantially Worse than Silicon Baseline Memory Technology**)

Overall Performance Assessment (OPA) = Performance Potential Summed over the eight Evaluation Criteria for each Technology Entry)
Maximum Overall Performance Assessment (OPA) = 24
Minimum Overall Performance Assessment (OPA) = 8

Overall Performance Assessment for Technology Entries

Potential for the Technology Entry is projected to be significantly better than silicon CMOS or baseline memory (compared using the Technology Evaluation Criteria) (OPA >20)	***Potential***
Potential for the Technology Entry is projected to be slightly better than silicon CMOS or baseline memory (compared using the Technology Evaluation Criteria) (OPA = >18 – 20)	***Potential***
Potential for the Technology Entry is projected to be slightly less than silicon CMOS or baseline memory (compared using the Technology Evaluation Criteria) (OPA = >16 – 18)	***Potential***
Potential for the Technology Entry is projected to be significantly less than silicon CMOS or baseline memory (compared using the Technology Evaluation Criteria) (OPA ≤ 16)	***Potential***

TECHNOLOGY PERFORMANCE ASSESSMENT

Tables 64 and 65 summarize the results of the critical review assessment of emerging research memory and logic technologies. This technology evaluation is illustrated in further detail for each Memory Technology in Figures 53a through 53f and for each Logic Technology in Figures 54a through 54f. Several new technology candidates for memory applications are identified as quite promising. These include nanofloating gate memory, engineered tunnel barrier memory, ferroelectric FET memory, and insulator resistance change memory. Conversely, no candidate technology or logic applications, other than 1D charge state, are currently identified to be very promising. Therefore, research is needed to identify promising new logic devices.

Table 64 Performance Evaluation for Emerging Research Memory Device Technologies (Potential)

Memory Device Technologies (Potential)	Scalability [A]	Performance [B]	Energy Efficiency [C]	OFF/ON "1"/"0" Ratio [D1]	Operational Reliability [E]	Operate Temp [F] ***	CMOS Technological Compatibility [G]**	CMOS Architectural Compatibility [H]*
Nano Floating Gate Memory	2.5	2.5	2.5	2.5	2.2	2.7	2.7	3.0
Engineered Tunnel Barrier Memory	2.2	2.3	2.3	2.3	2.4	2.8	2.8	3.0
Ferroelectric FET Memory	1.9	2.3	2.5	2.2	2.0	3.0	2.6	3.0
Insulator Resistance Change Memory	2.5	2.5	2.0	2.2	1.9	2.8	2.6	2.8
Polymer Memory	2.1	1.5	2.3	2.2	1.6	2.9	2.3	2.5
Molecular Memory	2.3	1.5	2.4	1.6	1.4	2.6	1.9	2.3

Table 65 Performance Evaluation for Emerging Research Logic Device Technologies (Potential)

Logic Device Technologies (Potential)	Scalability [A]	Performance [B]	Energy Efficiency [C]	Gain [D2]	Operational Reliability [E]	Room Temp Operation [F] ***	CMOS Technological Compatibility [G]**	CMOS Architectural Compatibility [H]*
1D Structures (CNTs & NWs)	2.4	2.5	2.3	2.3	2.1	2.8	2.3	2.8
Resonant Tunneling Devices	1.5	2.2	2.1	1.7	1.7	2.5	2.0	2.0
SETs	1.9	1.5	2.6	1.4	1.2	1.9	2.1	2.1
Molecular Devices	1.6	1.8	2.2	1.5	1.6	2.3	1.7	1.8
Ferromagnetic Devices	1.4	1.3	1.9	1.5	2.0	2.5	1.7	1.7
Spin Transistor	2.2	1.3	2.4	1.2	1.2	2.4	1.5	1.7

Relevance Criteria Notes for Tables 64 and 65:
[A] Scalability—In order to derive the economic benefit of incrementalism, any alternative technology should be scalable through multiple generations. It will be desirable to make incremental modifications to the alternative technology and achieve integer multiples of performance. In other words, it should be possible to articulate a Moore's law for the proposed technology
[B] Performance—Future performance metrics will be very similar to current performance metrics. They are cost, size, speed and energy dissipation.
[C] Energy efficiency—Energy efficiency appears likely to be the limiting factor of any post CMOS device using electric charge or electric current as a state variable. It also appears likely that it will be dominant criterion in determining the ultimate applicability of alternate state variable devices.
[D1] OFF/ON or "1"/"0" ratio (Memory)—The OFF/ON ratio of a memory device is the ratio of the access resistance of a memory storage element in the OFF state to its access resistance in the ON state. For non-volatile memories, the OFF/ON ratio represents the ratio between leakage current of an unselected memory cell to the read current of a selected cell. This definition will apply to new memory technologies so long as they have a selection device. In cross-point memories, a very large OFF/ON ratio is required to minimize power dissipation and maintain adequate read signal margin.
[D2] Gain (Logic)—The gain of nanodevices is an important limitation for current combinatorial logic where gate fan-outs require significant drive current and low voltages make gates more noise sensitive. New logic and low-fan-out memory circuit approaches will be needed to use most of these devices for computing applications. Signal regeneration for large circuits may need to be accomplished by integration with CMOS. In the near-term integratability of nanodevices to CMOS silicon is a key requirement due to both the need for signal restoration for many logic implementations and also the established technology and market base. This integration will be necessary at all levels from design tools and circuits to process technology.
[E] Operational reliability—Operational reliability is the ability of the memory and logic devices to reliably operate within their operational error tolerance given in their performance specifications.
[F] Room temperature operation—Room temperature operation is desirable because advanced cooling systems can add substantially to the cost.
[G] CMOS technological compatibility—The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principle economic benefit of such an approach is it allows the industry to fully apply previous technology investments to future products. Any alternative technology will need to utilize the tremendous investment in infrastructure to the highest degree possible.
[H] CMOS architectural compatibility—This criterion is motivated by the same set of concerns that motivate the CMOS technological compatibility, namely the ability to utilize the existing CMOS infrastructure that currently exists. The architectural compatibly is defined in terms of the logic system and data representation used by the alternative technology. CMOS utilizes Boolean logic and a binary data representation and ideally, the alternative technology would need to do so as well.

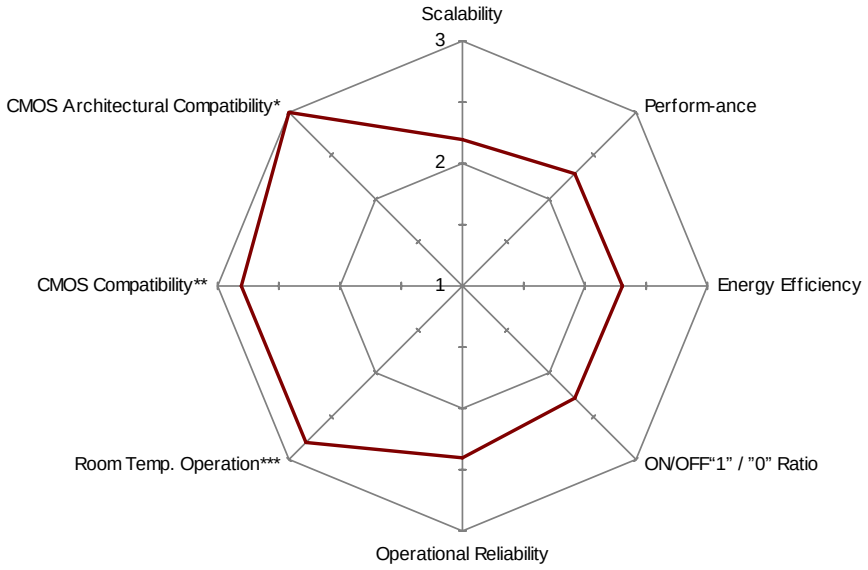

Figure 53a Technology Performance Evaluation for Nano Floating Gate Memory

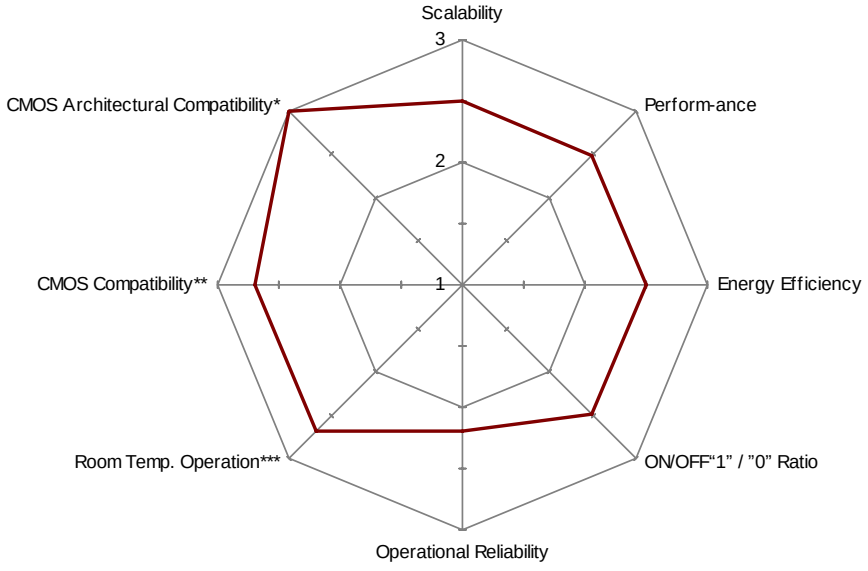

Figure 53b Technology Performance Evaluation for Engineered Tunnel Barrier Memory

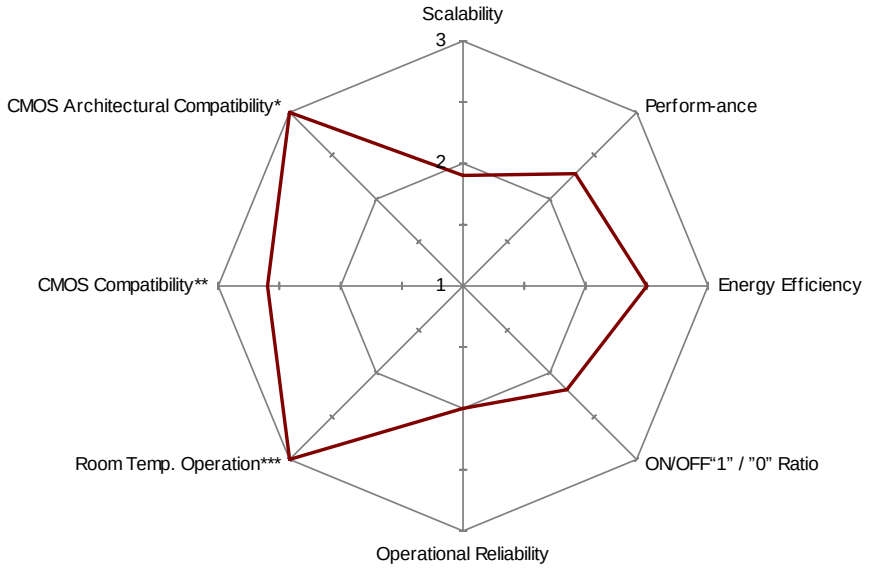

Figure 53c Technology Performance Evaluation for Ferroelectric FET Memory

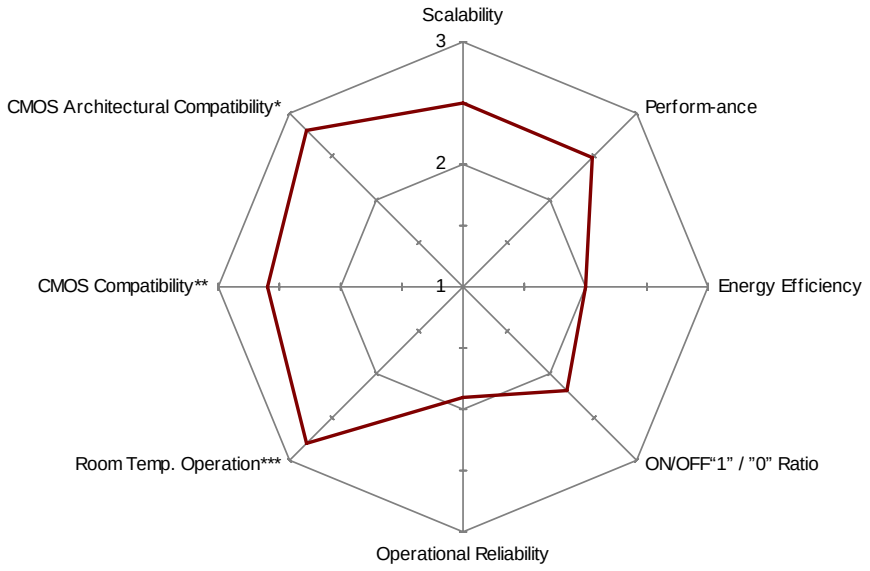

Figure 53d Technology Performance Evaluation for Insulator Resistance Change Memory

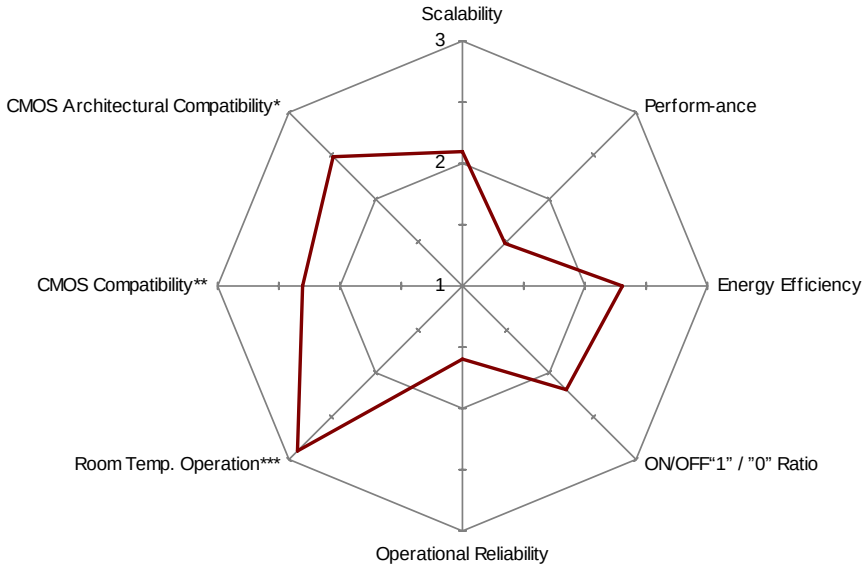

Figure 53e Technology Performance Evaluation for Polymer Memory

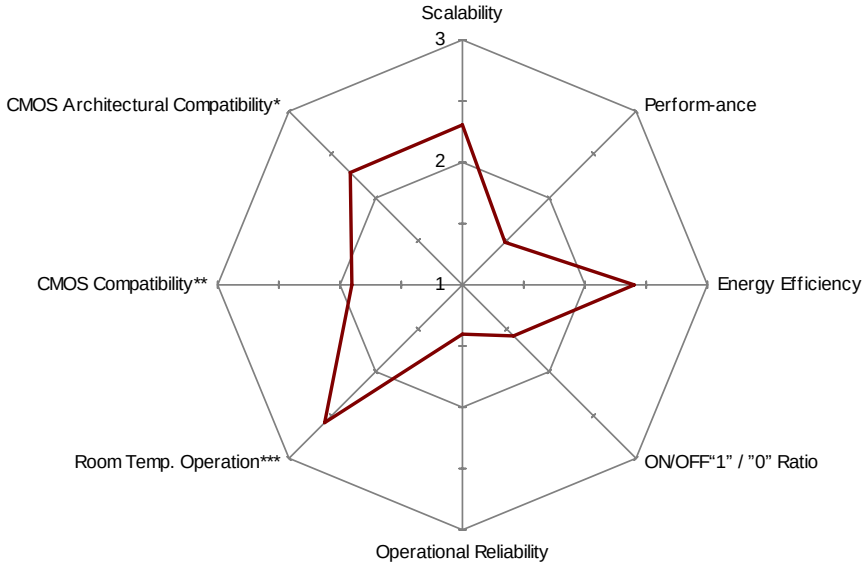

Figure 53f Technology Performance Evaluation for Molecular Memory

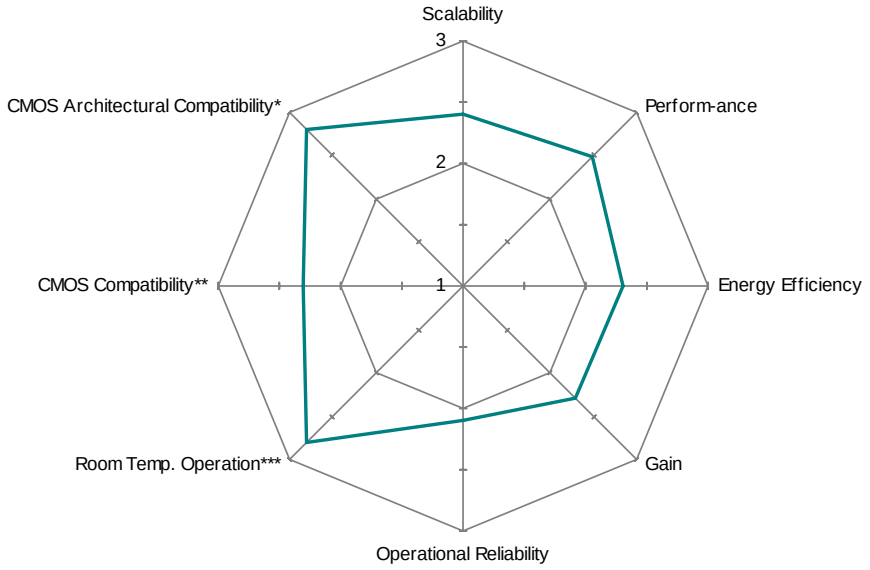

Figure 54a Technology Performance Evaluation for 1D Logic Structures (CNTs and NWs)

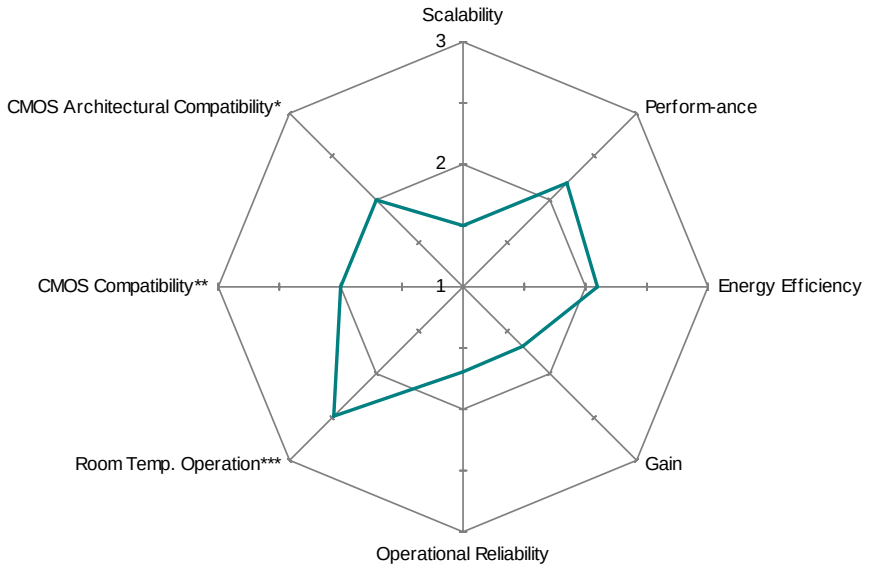

Figure 54b Technology Performance Evaluation for Resonant Tunneling Logic Devices

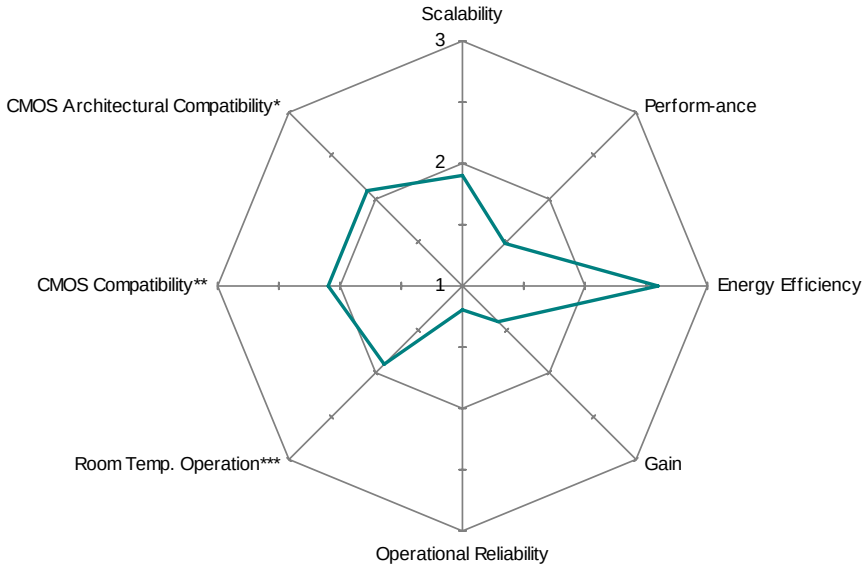

Figure 54c Technology Performance Evaluation for Single-Electron Logic Transistors

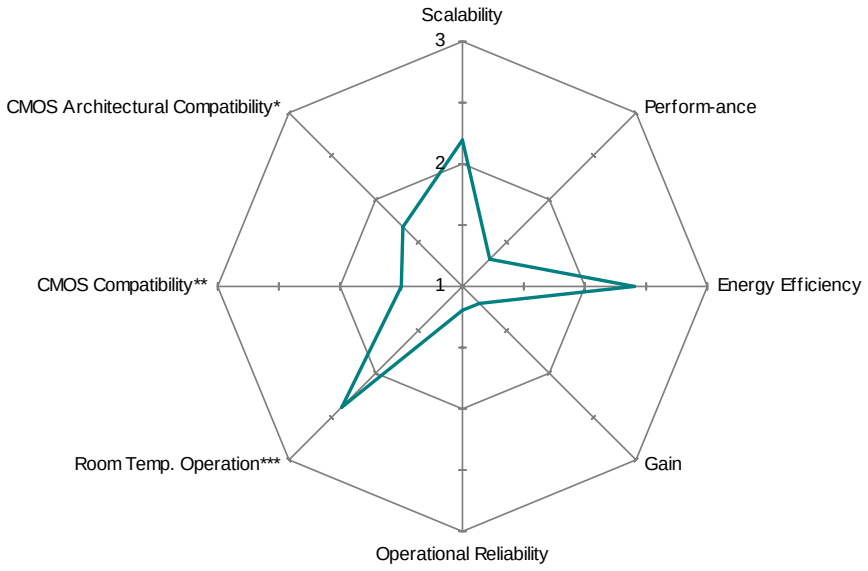

Figure 54d Technology Performance Evaluation for Molecular Logic Devices

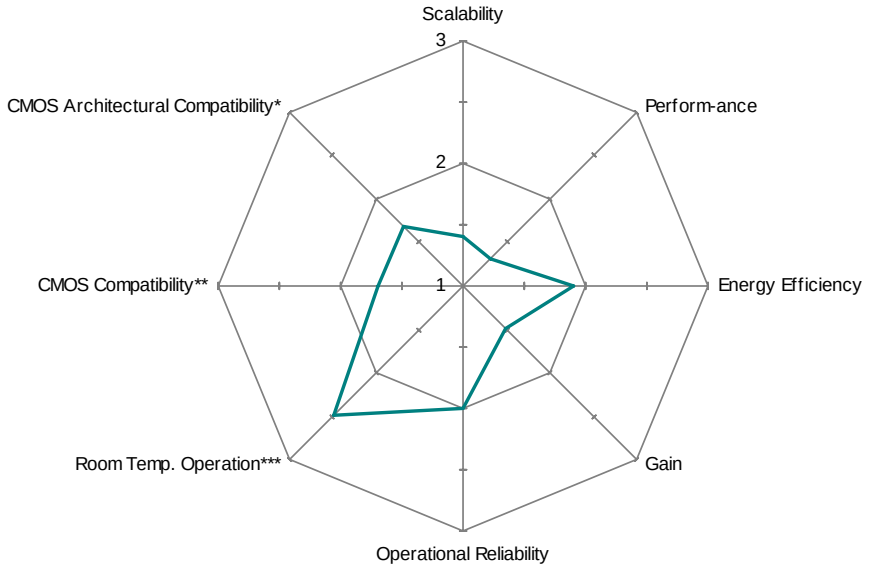

Figure 54e Technology Performance Evaluation for Ferromagnetic Logic Devices

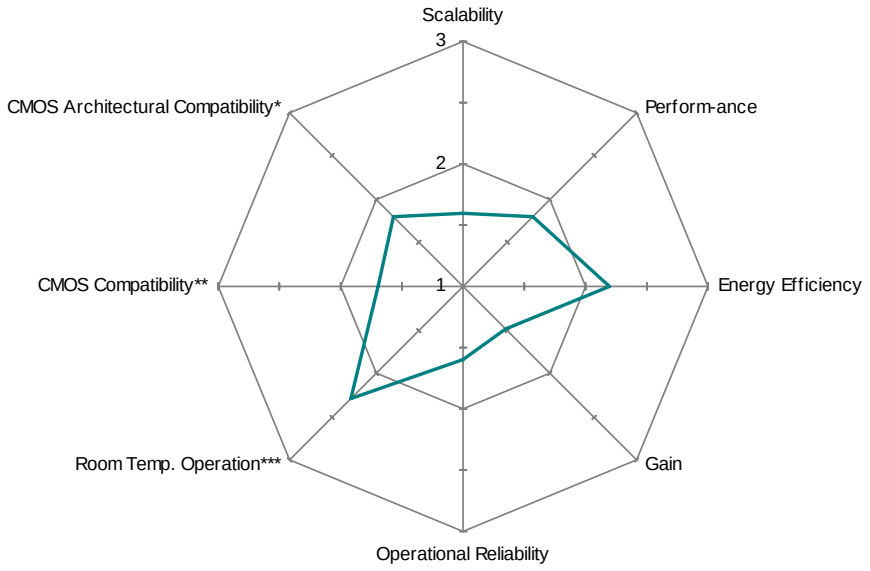

Figure 54f Technology Performance Evaluation for Spin Logic Devices

FUNDAMENTAL GUIDING PRINCIPLES—"BEYOND CMOS" INFORMATION PROCESSING

INTRODUCTION

In considering the many disparate new approaches proposed to provide order of magnitude scaling of information processing beyond that attainable with ultimately scaled CMOS, the Emerging Research Devices Working Group proposes the following comprehensive set of guiding principles. We believe these "Guiding Principles" are necessary for a new "Beyond CMOS" information processing technology to dramatically enhance scaling of functional density and performance while simultaneously reducing the energy dissipated per functional operation. Further this new technology would be realized using a highly manufacturable fabrication process.

The purpose in proposing these "Principles" is to stimulate a vigorous discussion of those factors that will necessarily govern emergence of a new paradigm for "Beyond CMOS" information processing.

GUIDING PRINCIPLES

COMPUTATIONAL STATE VARIABLE(S) OTHER THAN SOLELY ELECTRON CHARGE

These include spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration and other quantum states. The estimated performance of alternative state variable devices to ultimately scaled CMOS should be made as early in the program as possible to enable down-selection and identify key trade-offs.

NON-THERMAL EQUILIBRIUM SYSTEMS

These are non-thermal equilibrium systems that serve to reduce the perturbations of stored information energy in the system caused by thermal interactions with the environment. This function can be accomplished by systems that perform all computational processing functions in a time short compared to the system's energy relaxation time. Thermal fluctuations will require energy barriers of order 10 kT to prevent random fluctuations of computational state in any bistable-switching device where k_b is Boltzmann's constant and T is the effective temperature. One path to low energy, room temperature switching is to find systems that can operate out of thermal equilibrium with the phonon bath so the effective temperature T for the system is less than the general environment. Nuclear spin is a naturally occurring example of such a system.

NOVEL ENERGY TRANSFER INTERACTIONS

These interactions could provide the interconnect function between communicating information processing elements. Energy transfer mechanisms for device interconnection perhaps would be based on short range interactions, including quantum exchange and double exchange interactions, electron hopping, Forster coupling (dipole–dipole coupling), tunneling and coherent phonons.

NANOSCALE THERMAL MANAGEMENT

This might be accomplished by manipulating lattice phonons for constructive energy transport and heat removal. These would include phonon stop band structures for local energy redistribution and structures for non-isotropic heat transport

SUB-LITHOGRAPHIC MANUFACTURING PROCESS

One example of this principle is directed self-assembly of complex structures composed of nanoscale building blocks This requirement is essential to fabricate blocks including quantum dots, semiconductor nanocrystals, metallic nanocrystals, and resonant cavities (metacrystals) in a bulk material capable of supporting the quantum interactions described above (e.g., complex metal oxides). These self-assembly approaches should address non-regular, hierarchically organized structures, be tied to specific device ideas, and be consistent with high volume manufacturing processes.

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