INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

METROLOGY

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METROLOGY

Metrology is defined as the science of measurement. For the purposes of the ITRS, we define it as the measurements made to research, develop, and manufacture integrated circuits, including measurements made on materials used for integrated circuits and their packaging. Metrology was the first semiconductor technology area to routinely work in the area of nanoelectronics. A variation in features size one tenth of the nominal dimension often results in significant changes in device properties. With this in mind, one can see that thin film and interfacial layer thickness as well as line width variations control has already moved to near atomic sized requirements. As the industry moves further into the world of nanoelectronics, metrology, including materials characterization, will take on greater challenges and become even more critical. *One gap is the ability to measure properties of materials such as thickness on the sidewalls of densely patterned features such as gates, FINS, and trenches*. The fundamental challenge for materials characterization is imaging and measurement of materials properties at sub-atomic dimensions. The fact that some materials properties are not localized to atomic dimensions is noteworthy. The fundamental challenge for factory metrology will be the measurement and control of atomic dimensions while maintaining profitable high volume manufacturing.

Metrology continues to enable research, development, and manufacture of integrated circuits. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability. In some instances, existing methods can be extended for several technology generations. In other cases, necessary measurements may be done with inadequate equipment. The uncertain nature of device design adds to the challenge. Long-term research into nano-devices may provide both new measurement methods and potential test vehicles for metrology. *In situ* methods continue to move into manufacturing. All metrology is connected to factory-wide automation that include database and intelligent information from data capability. Off-line materials characterization is also evolving toward compatibility with factory-wide automation. Advanced microscopy and other probing techniques are quickly becoming commercially available even as the fundamental understanding of their use and interpretation remains a part of basic research. Successful implementation of new materials characterization methods relies on development of rapid sample preparation for materials characterization. Although thorough materials characterization is a critical part of materials and process development, predicting the necessary metrology for manufacturing remains an elusive goal. Issues resolved by process improvements leave open the question of what to measure during device manufacturing to ensure reliability.

Control of a number of transistor properties such as enhanced mobility through either substrates with stressed surface layers or process induced stressed channels remain difficult challenges. Measurement of stress in strained silicon surface layers is possible. Direct measurement of stress in a nano-sized, buried area such as the stressed channel is not presently possible. Often, one must measure a film or structure property at the surface and use modeling to determine the resultant property of a buried layer. The expected trend is the combined use of modeling with measurement of features at the wafer surface.

The Metrology roadmap has repeated the call for a proactive research, development, and supplier base for many years. The relationship between metrology and process technology development needs fundamental restructuring. In the past the challenge has been to develop metrology ahead of target process technology. Today we face major uncertainty from unresolved choices of fundamentally new materials and radically different device designs. *Understanding the interaction between metrology data and information and optimum feed back, feed forward, and real-time process control are key to restructuring the relationship between metrology and process technology.* A new section has been added to the Metrology Roadmap that covers metrology needs for emerging technology paradigms such as spintronics and molecular electronics.

Research and development of new as well as evolutionary metrology technology must keep pace with the three-year schedule for introduction of new technology generations. The roadmap for feature size reduction drives the timeline for metrology solutions for new materials, process, and structures. New substrate materials such as silicon on insulator and strained silicon channels add to the complexity of measurements. Metrology development must be done in the context of these issues. Metrology enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The increasing diversity of chip types will spread already limited metrology resources over a wider range of challenges. The metrology community including suppliers, chip manufacturers, consortia, and research institutions must provide cooperative research, development, and prototyping in order to meet the ITRS timeline. *The forefront developments in measurement technology must be commercialized in a timely manner.* The feature sizes and materials a decade away in the 2003 Roadmap already greatly challenge the measurements used in process and materials development.

2 Metrology

The near-term challenges for metrology revolve around the need for controlling scaling as well as new materials, processes, and structures used for nanoelectronic transistors and interconnect. The lack of certainty in the 32 nm technology generation has a significant impact on metrology development. FINFETs and other new structures require measurement of films on sidewalls and other highly challenging configurations. The large number of candidate materials being considered for each generation require characterization in evaluation and control in development and process. Moreover, it is entirely possible that different materials will be used by different manufacturers at a given technology generation, potentially requiring different metrologies. In the near term, advances in electrical and physical metrology for high- and low-κ dielectric films must continue. The requirement for technology for measurement of devices on ultra-thin and possibly strained silicon on insulator comes from the best available information that is discussed in the *Front End Processes* Roadmap. The increasing emphasis on active area measurements instead of test structures in scribe (kerf) lines places new demands on metrology. Long-term needs at the sub-22 nm technology generation are difficult to address due to the lack of clarity of device design and interconnect technology. The selection of a replacement for copper interconnect remains a research challenge. Although materials characterization and some existing inline metrology apply to new device and interconnect structures, development of manufacturing capable metrology requires a more certain knowledge of materials, devices, and interconnect structures.

All areas of measurement technology (especially those covered in the *Yield Enhancement chapter*) are being combined with computer integrated manufacturing (CIM) and data management systems for information-based process control. Although integrated metrology still needs a universal definition, it has become the term associated with the slow migration from offline to inline and *in situ* measurements. The proper combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

Metrology tool development requires access to new materials and structures if it is to be successful. It requires the availability of state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of production. This requires a greater attention to expanding close ties between metrology development and process development. When the metrology is well matched to the process tools and processes, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

SCOPE

The metrology topics covered in the 2005 *Metrology* roadmap are microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; *in situ* sensors and cluster stations for process control; reference materials; correlation of physical and electrical measurements; and packaging. These topics are reported in the following sections in this chapter: Microscopy; Lithography Metrology; Front End Processes Metrology; Measurements for Processes Facing Statistical Limits and Physical Structures Reaching Atomic Dimensions; Interconnect Metrology; Materials and Contamination Characterization; Integrated Metrology; Reference Measurement Systems, Reference Materials; and Characterization and Metrology for Emerging Devices.

International cooperation in the development of new metrology technology and standards will be required. Both metrology and process research and development organizations must work together with the industry including both the supplier and IC manufacturer. Earlier cooperation between IC manufacturers and metrology suppliers will provide technology roadmaps that maximize the effectiveness of measurement equipment. Metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. Despite the existence of standardized definitions and procedures for metrics, individualized implementation of metrics such as measurement precision to tolerance (P/T) ratio is typical.[1] The P/T ratio for evaluation of automated measurement capability for use in statistical process control relates the measurement variation (precision) of the metrology cluster to the product specification limits. Determination of measurement tool variations is sometimes carried out using reference materials that are not representative of the product or process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. It is also possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a need for metrics that accurately describe the resolution capability of metrology tools for use in statistical process control. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio. However, because the type of resolution depends on the process (such as thickness and width require spatial resolution

[1] *For example, refer to SEMI E89-0999 "Guide For Measurement System Capability Analysis."*

while levels of metallics on the surface require resolution of atomic percent differences), topic-specific metrics may be required. A new need is for a standardized approach to determination of precision when the metrology tool provides discrete instead of continuous data. This situation occurs, for example, when significant differences are smaller than the instrument resolution.

The principles of integrated metrology can be applied to stand-alone and sensor-based metrology itself. Factors that impact tool calibration and measurement precision such as small changes in ambient temperature and humidity could be monitored and used to improve metrology tool performance and thus improve statistical process control.

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for metrology should decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS-based metrology and nano-technology are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 32 nm technology generation. Metrology needs after 2013 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 116 presents the ten major challenges for metrology.

Table 116 Metrology Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low-κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new low-κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. Metal gate work function characteization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 32 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

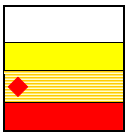
Table 117a Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*	
Microscopy										
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	0.29	0.25	0.22	0.2	0.18	0.16	0.14	0.13	0.12	*MPU Gate*
Microscopy capable of measurement of patterned wafers having maximum aspect ratio/diameter (nm) (DRAM contacts) [A]	15	16	16	17	17	>20	>20	>20	>20	*D1/2*
	95	85	76	67	60	50	40	35	30	
Materials and Contamination Characterization										
Real particle detection limit (nm) [B]	32	28	25	22	20	18	16	14	13	*MPU*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	27	23	22	19	17	15	13	12	11	*D1/2*
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	*MPU Gate*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	*MPU Gate*

Table 117b Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	
Microscopy								
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	0.1	0.09	0.08	0.07	0.06	0.06	0.05	*MPU Gate*
Microscopy capable of measurement of patterned wafers having maximum aspect ratio/diameter (nm) (DRAM contacts) [A]	>20	>20	>20	>20	>20	>20	>20	*D1/2*
	28	25	23	20	18	16	14	
Materials and Contamination Characterization								
Real particle detection limit (nm) [B]	11	10	9	8	7	6	6	*MPU*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	9	8	7	6	6	5	5	*D1/2*
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	*MPU Gate*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	*MPU Gate*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 117a and b:
[A] Metal and via aspect ratios are additive for dual-Damascene process flow.
[B] This value depends on surface microroughness and layer composition.
[C] The requirements for metal contamination have been changed based on less stringent requirements found in Front End Processes chapter Surface Preparation Technology Requirements table, Note F.

MEASUREMENTS FOR PROCESSES FACING STATISTICAL LIMITS AND PHYSICAL STRUCTURES REACHING ATOMIC DIMENSIONS

As the dimensions of integrated circuit devices continue to shrink, the finite dimensions of the atoms within the structures are leading to statistical variations in critical dimensions and thus device properties. Furthermore, , the physical properties are deviating from bulk properties because of quantum mechanical and mean free path effects. For instance, the lattice spacing of silicon atoms in a 32 nm gate represents about 1% of the gate length. The effects of statistical variations may be even more pronounced in gate dielectric structures composed of multi-layers of different components, each only several atoms thick. The engineering of such structures must take these statistical variations of dopant atoms and intrinsic defects and the quantum mechanical effects of confined structures into account to obtain sufficiently uniform device and circuit performance for large-scale integration. The issue of line width roughness and its effect on electrical CD is compounded with doapnt atom statistical variation (*See the linked discussion by D. Herr*).

Advances in interconnect technology are using conductor materials such as copper that must be excluded from the semiconductor and the low-κ interconnect structures. Process and process modeling advances are required to deposit barrier layers only several atoms thick that are pin hole free. Metrology must be developed to ensure the integrity of these barrier layers.

Several issues challenge measurement of transistor structures. Metrology of gate dielectric structures requires a standardized model of the quantum mechanical effects at the silicon–dielectric interface and gate electrode–dielectric interface. Stochastic modeling strategies are required to supplement deterministic modeling techniques. Mechanical stress is now used to improve transport properties of transistors; metrology and modeling need to be developed to optimize and control these effects. Statistical variations in real materials and structures are independent of measurement uncertainties, and add quadratically to the total uncertainty of the values of measured quantities. In addition, they must be taken into account in circuit and process design in ways that are not yet envisioned. It appears that the measurement of a number of parameters specified for future device generations elsewhere in this document cannot be met for fundamental reasons having little to do with metrology *per se*.

MICROSCOPY

Microscopy is used in most of the core technology processes where two-dimensional distributions,that is digital images of the shape and appearance of integrated circuit (IC) features, reveal important information. Usually, imaging is the first, but many times the only step in the "being able to see it, measure it, and control it" chain. Microscopes typically employ light, electron beam, or scanned probe methods. Beyond imaging, online microscopy applications include critical dimension (CD) and overlay measurements along with detection, review, and automatic classification of defects and particles. Because of the high value and quantity of wafers, the need for rapid, non-destructive, inline imaging and measurement is growing. Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies. Microscopy techniques and measurements based on them must serve the technologists better giving fast, detailed, adequate information on the processes in ways that help to establish process control in a more automated manner. *Refer to the supplemental file for more details on Microscopy.*

Electron Microscopy—There are many different microscopy methods that use electron beams as sources of illumination. These include scanning electron microscopy, transmission electron microscopy, scanning transmission electron microscopy, electron holography, and low-energy electron microscopy. Scanning electron microscopy and electron holography are discussed below, and transmission electron microscopy, scanning transmission electron microscopy, and low-energy electron microscopy are discussed in the section on Materials and Contamination Characterization.

Scanning Electron Microscopy (SEM)—continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation. New inline SEM technology, such as the use of ultra-low-energy electron beams (< 250 eV) and high energy SEM may be required for overcoming image degradation due to charging, contamination, and radiation damage of the sample surface, while maintaining adequate resolution. Improving the resolution of the SEM by the reduction of spherical aberration leads to an unacceptably small depth of field and SEM imaging with several focus steps and/or use of

algorithms that take the beam shape into account might be needed (*for more detail refer to linked paper on DOF*). Aberration correction lens technology has migrated from transmission electron microscopy to SEM providing a significant increase in capability. Other non-traditional SEM imaging techniques such as the implementation of nano-tips, and electron holography need to be developed, if they can prove to be production-worthy methodologies. A new alternative path could be high-pressure or environmental microscopy, which opens the possibility for higher accelerating voltage high-resolution imaging and metrology. Binary and phase-shifting chromium-on-quartz optical photomasks have been successfully investigated with this mode of high-resolution scanning electron microscopy. It has been found that the gaseous sample environment minimizes sample charging and contamination. This methodology also holds good potentials for the inspection, imaging and metrology of wafers.

To be able to make statistically sound SEM measurements it is essential to collect the right kind and amount of information. The collection of more then needed information leads to loss of throughput, not enough, or wrong type to loss of control. It is important to develop metrology methods that reveal and express the needed information with the indication of the validity of the measurements. Data analysis methods that adhere to the physics of the measurement and do use all information collected were demonstrated to be better than arbitrary methods. Measured and modeled image and fast and accurate comparative techniques are likely to gain importance in SEM dimensional metrology.

A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and the deposition of charge in gate structures, may set fundamental limits to the utility of all microscopies relying on charged particle beams.

Determination of the real 3D shape for sub-90 nm contacts/vias, transistor gates, interconnect lines, or damascene trenches will require continuing advances in existing microscopy and sample preparation methods. Cross-sectioning by FIB and lift-out for imaging in a TEM or a STEM has been successfully demonstrated.

He ion Microscopy—has been proposed as a means of overcoming the issues associated with the spread in effect probe size associated with the interaction of finely focused electron beams and the sample. Potential applications of this technology include CD, defect review, and nanotechnology.

Scanning probe microscopy (SPM)—may be used to calibrate CD-SEM measurements. Stylus microscopes offer 3D measurements that are insensitive to the material scanned. Flexing of the stylus degrades measurements, when the probe is too slender. The stylus shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High stiffness probe materials, such as short carbon nano-tubes, may alleviate this problem.

Far-field optical microscopy—is limited by the wavelength of light. Deep ultra-violet sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of defects is needed. Optical microscopes will continue to have application in the inspection of large features, such as solder bump arrays for multi-chip modules.

For *defect detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes. High-speed scanning has been demonstrated with arrayed SPMs, (that might be faster than SEMs) but issues associated with stylus lifetime, uniformity, characterization, and wear need to be addressed. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput and operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs.

LITHOGRAPHY METROLOGY

Lithography metrology continues to be challenged by rapid advancement of patterning technology. New materials in all process areas add to the challenges faced by Lithography Metrology. A proper control of the variation in transistor gate length starts with mask metrology. Although the overall features on a mask are four times larger than as printed, phase shift and optical proximity correction features are roughly half the size of the printed structures. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology have to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimensionand overlay are also becoming more challenging. CD control for transistor gate length continues to be a critical part of manufacturing ICs with increasing clock speeds. The metrology needs for process control and dispositioning of product continue to drive improvements in precision, relative

accuracy and matching. Acceleration of research and development activities for CD and overlay are essential if we are to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability.

On-product monitors of effective dose and focus extend utility of conventional microscopy-based CD metrology systems in process control applications. The same system can output CD and overlay measurements, as well as lithography process monitors. Process control capability and efficiency of such metrology are improving. The infrastructure to support such new applications is generally available. Monitors of effective dose and focus for lithography process control have also been developed for conventional optical metrology systems, such as used in overlay metrology. Similar capabilities, in addition to CD, sidewall, and height metrology, are now emerging in scatterometry. In all cases, rather than measure CD for the purpose of process control, with every feature's CD being a complex function of both dose and focus, these systems output measurements of process parameters themselves, with metrology errors as low as 1% (3 σ) for dose and ~10 nm (3 σ) for focus. Today's process monitor performance levels boast P/T = 0.1 for lithography process window with 15% for dose and 200 nm for focus, enabling further reduction of K1 in high volume manufacturing and extending the utility of optical microlithography. While the demands on metrology systems' stability and matching are likely to increase[1], work in this area has already initiated the development of tighter control and matching, being a pre-requisite of accurate CD metrology[2], not just of process control applications and dedicated process monitors.

Capable and efficient direct process monitor-based lithography process control has the potential to overcome technology limitations of conventional CD metrology. The on-going change of lithography process control methodology can be accelerated by industry collaboration to define the expectations in direct process control, with tests of performance and standards for both new metrology applications and applications environment. This change will, likely, result in the lithography metrology where capable and efficient means of process control are supplemented by, and are differentiated from, superior critical dimension metrology proper. However, to meet measurement requirements for next generation technology especially in the areas of CD metrology for calibration and verification of compliance for advanced mask designs (for example, 1-D and 2-D/3-D CD metrology through pitch and layouts, in presence of OPC and RET, various printing conditions), new levels of absolute accuracy are required.

There is no single metrology method or technique that can deliver all needed information. Therefore, in order to be able to meaningfully compare and match the results of various dimensional metrology tools and methods parameters beyond repeatability and precision need to be addressed. Each measurement application requires consideration of the need for relative accuracy (senstivity to CD variation and insensitivity to secondary characteristic variation), absolute accuracy (traceability to absolute length scale), LER and sampling, and the destructive nature of the measurement.

It would be ideal to have all metrology tools properly characterized for measurement uncertainty including a breakout of the leading contributors to this uncertainty. It is recommended to use internationally accepted methods to state measurement uncertainty. This knowledge would help to make the most of all metrology tools, and it would prevent situations in which the measured results do not provide the required information. Finally, once the largest contributors to measurement errors are known, a faster development of better instruments could take place. It is now recommended to state the measurement uncertainty of various dimensional metrology tools according to internationally accepted methods and to identify (quantify) the leading contributors.

Although a number of potential solutions for CD measurement exist, there is no unique technique that matches every measurement requirement. Often, special test structures are measured during manufacturing. When this is the case, active device dimensions are not measured. CD-SEM continues to be used for wafer and mask measurement of lines and via/contact. A considerable effort has been aimed at overcoming electron beam damage to photoresist used by 193 nm exposures and that will continue when alternative lithography techniques, like immersion and EUVL, are introduced. Stack materials, surface condition, line shape, and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements. Developments in electron beam source technology that improve resolution and precision are being tested. CD-SEM is facing an issue with poor depth of field unless a new approach to SEM-based CD measurement is found. High-voltage CD-SEM and low loss detectors have been proposed as means of extending CD-SEM.[3]

Scatterometry has moved into manufacturing, and does provide line shape metrology. Scatterometry refers to both single wavelength—multi angle optical scattering and to multi-wavelength—single angle methods. Recent advances have resulted in the ability to determine CD and line shape without the aid of a library of simulated results. Scatterometry has already been shown to provide a tighter distribution of key transistor electrical properties when used in an advanced

process control mode. The next step is the development of scatterometry for contact and via structures. Scatterometry models assume uniform optical property of line and background materials. Surface anomalies and non-uniform dopant distribution may affect scatterometry results. Therefore, scatterometry models need calibration and periodic verification. Litho and etch microloading effects may noticeably affect line CD. Since scatterometry makes measurements on special test structures, other CD metrology techniques (such as SEM or AFM) need to be employed to establish correlation between CD of the scatterometry structure and CDs of the circuit. Scatterometry needs to be capable of measuring smaller test structures while improving measurement precision.

The use of "feed forward" control concepts must be extended to lithography metrology taking data at least from resist and mask measurements and controlling subsequent processing, such as etch, to improve product performance. "Feed back" controlling strategy is required as well to set properly process parameter setup from a huge amount of previously collected data. The use of overlay measurement equipment for CD control has also been reported. This method is based on the fact that the change in line width also affects the length of the photoresist lines that can then be measured using the optical microscope of the overlay system. A special test structure with arrays of line and arrays of spaces is required.

CD-AFM measurements are an excellent means of verifying line shape and calibrating CD measurements. New probe tip technology and 3-D tiltable cantilever is required if CD-AFM is to be applied to dense line measurement below 90 nm. Focus–Exposure correlation studies (especially for contact/via) can be done using all of the above methods as well as by the dual-beam FIB (SEM plus focused ion beam) where there is an immediate correlation with line shape. Electron holography has been proposed as a long term CD measurement technology.

Line edge roughness (LER) is an important part of lithography process control. Line width roughness (LWR) is an important part of etch process control. The Lithography Roadmap provides metrics for both LER and LWR. In 2001, LWR requirements were listed as LER. LWR was included in the 2001 ITRS because it was correlated to an increase in transistor leakage current but not to changes in drive current.[4] It is important to note that the precision requirement for LER are several years ahead of those required for CD as indicated below. Although CD-SEM and lithography process simulation systems have software that determines LER, there is no standard method of determining line edge roughness. Thus standardized assessment of the status of LEW and LWR versus roadmap requirements is not possible.

LER/LWR is evaluated by two methods: spectral analysis and measurement of LER/LWR amplitude / degree (generally, 3 σ of residuals from average position or average CD). Fourier spectrum of LER/LWR is becoming popular in R&D; however, 3 σ is still the most useful index for practical in-line metrology. In evaluating LER/LWR, length of the inspected edge, L, and sampling interval of edge-detection, Δy, are the most important measurement parameters because 3 σ strongly depends upon these values. These two parameters have been discussed intensively. They should be chosen with considering the purpose of measurement. When evaluating in-gate roughness, L should be equal to the gate width of transistor. There are several backgrounds to take into consideration for deciding Δy in this case. Depth of the junction, which is regarded as one of the most important parameter for LER/LWR definition, could be the minimum spatial period to be measured. When evaluating LER/LWR over the all spatial-frequency region, L should be 2 μm or more because long-period LER components have the most significant amplitudes. In this case, it has been reported that 10 nm of Δy is sufficiently small from the viewpoint of LER/LWR measurement precision, because higher frequency components, which cannot be detected with this interval, are small enough compared with the total LER/LWR observed in a 2-μm-long line such that they maybe considered insignificant. This is explained by the universal characteristics of LER/LWR spectrum; power spectral density decays as $1/f^m$ (f; frequency, m=2.0 to 2.3 for a random-walk edge).[5, 6] It has also been confirmed that measurement error is 5 % or less in measuring 2-μm-long LWR when setting Δy to 10 nm.[5] On the other hand, 4 nm for Δy until the 32 nm node and 2 nm for the 22 nm node and beyond has also been proposed; this sampling scheme detects the shortest period of gate LWR transferred by the ion implantation, with the benefit of this definition being valid for years to come, and which improves measurement precision. The choice between these different values for Δy is still being discussed.

The recommended LER/LWR metric is thus defined as the 3σ of residuals measured along 2-μm-long line for the present; however, transistor performance could be more sensitive against in-gate roughness in the future. In that case, a new index for in-gate roughness (such as high-frequency LWR) should be additionally defined. To evaluate LWR-caused gate-CD variation separately, low-frequency LWR index should also be defined.

Another important factor in measurement of LWR/LER on imaging tools is edge detection noise. This noise has the effect of adding a positive bias to any roughness measurement. This is shown by the equation $LWR_{meas}^2 = LWR_{actual}^2 + \sigma_\varepsilon^2$ where LWR_{meas} is the measured value, LWR_{actual} is the actual roughness of the target, and σ_ε is the noise term, defined

as the reproducibility of locating an edge along one single sampling point. The size of σ_ε has been measured to be on the order of 2.5 nm, which means that at future technology nodes this measurement artifact could mask the actual roughness to be measured. A methodology has been demonstrated to remove this noise term, leading to an unbiased estimation of the roughness. Use of this is deemed very important to ensuring accuracy of roughness measurement in the future, and should be a key ingredient in allowing for intercomparison of data across the litho-metrology community.[77]

Considering the afore-mentioned points, the LER/LWR definition and detailed measurement conditions should continue to be discussed, and the LER/LWR table values periodically reviewed. It should also be noted that there are many other kinds of LER/LWR to possibly be considered, such as gate-LWR in the high-, low-, and full spatial-frequency regions, LER/LWR in features of other process modules such as interconnect, etc. (even roughness in the contact hole or via edge could be a potential issue). To begin discussion on the definitions of these roughnesses, we must first collect experimental data for the relationship between the device performance and roughness. Second, it is important to re-consider whether or not the definition of the LER/LWR should be revised in accordance with the shrinking half pitch. Third, the required precision and accuracy in the LER/LWR measurement should be quantitatively based on the LER/LWR dependence of device performance. In this case, it is necessary to consider the factors which degrade measurement accuracy such as LER/LWR bias. [7]

Critical dimension measurement capability does not meet precision requirements that comprehend measurement variation from individual tool reproducibility, tool-to-tool matching and sample-to-sample measurement bias variation. Precision is defined by SEMI as a multiple of reproducibility. As indicated in the introduction, reproducibility includes repeatability, variation from reloading the wafer, and long-term drift. In practice, reproducibility is determined by repeated measurements on the same sample and target over an extended period of time. Although the precision requirements for CD measurement in the ITRS have always included the effects of line shape and materials variation, repeated measurements on the same sample would never detect measurement uncertainty related to sample-to-sample bias variation. Therefore, with the current methodology the uncertainty of measurement associated with variation of line shape, material, layout, or any other parameter will not be included in the precision. Typically, reference materials for CD process control are specially selected optimum or "golden" wafers from each process level. Thus, industry practice is to determine measurement precision as a reproducibility of the measurement for each process level. The measurement bias is not detected. This approach misses measurement bias variation component of measurement uncertainty. In light of this, a new metric, total measurement uncertainty (TMU), has been proposed. The components of total uncertainty need to be properly assessed for every metrology tool. This would allow meaningful comparisons and improved tool matching. Total measurement variation defines a new precision-like variable P(TMU). P(TMU) would be determined using a technology representative set of samples that accounts for variations in measurement bias associated with each process level. One way to reduce TMU is to correct CD measurement bias at each process level.

Calibration of inline CD metrology equipment requires careful implementation of the calibration measurement equipment. For example, laboratory based, cross-sectional SEM or CD-AFM must have precision that matches or exceeds inline CD and have to be frequently calibrated. Reference materials used during manufacturing must be representative to the actual process level and structure. Due to the importance of maintaining control of transistor gate length as well as other structures, different metrology systems may be selected for transistor gate control. Reports of this approach already exist.

CD measurement has been extended to line shape control. Tilt beam CD-SEM, comparison of line scan intensity variation versus line scans from a golden wafer, scatterometry, CD-AFM, and the dual beam FIB (electron and ion beam systems) have all been applied to line shape measurement. Sidewall angle has been proposed as the key process variable. Already, photoresist lines have shapes that are not well described by a single planar description of the sidewall. Line edge and line width roughness along a line, vertical line edge roughness, and rounded top shapes are important considerations in process control. As mentioned above, precision values change with each process level. This adds to the difficulty in determination of etch bias (the difference in CD before and after etch). Electrical CD measurements provide a monitoring of gate and interconnect line width, but only after the point where reworking the wafers is no longer possible and does not allow a real-time correction of process parameter. Electric CD measurements are limited in their applicability to conducting samples.

Mask metrology is moving beyond the present optical technology. Binary and phase-shifting chromium on quartz optical photomasks have been successfully investigated with high-pressure/environmental scanning electron microscopy. The successful application of this methodology to semiconductor photomask metrology is new because of the recent availability of a high-pressure SEM instrumentation equipped with high-resolution, high-signal, field emission technology in conjunction with large chamber and sample transfer capabilities. The high-pressure SEM methodology employs a

gaseous environment to help to compensate for the charge build-up that occurs under irradiation with the electron beam. Although potentially very desirable for the charge neutralization, this methodology has not been seriously employed in photomask or wafer metrology until now. This is a new application of this technology to this area, and it shows great promise in the inspection, imaging, and metrology of photomasks in a charge-free operational mode. This methodology also holds the potential of similar implications for wafer metrology. For accurate metrology, high-pressure SEM methodology also affords a path that minimizes, if not eliminates, the need for charge modeling.

Lithography metrology consists not only of overlay and CD metrology (essentially microscopy to measure width, depth, and shape of printed features after completion of the lithography step), but also includes the process control and characterization of materials needed for lithography process, especially photoresists, phase shifters, and antireflective coatings (ARCs). As these lithography materials become more complex, the materials characterization associated with them also increases in difficulty. Additionally, most non-lithography materials used in the wafer fabrication process (gate oxides, metals, low-κ dielectrics, SOI substrates, etc) enter the lithography process indirectly, since their optical properties affect the reflection of light at a given wavelength. Even a small variation in process conditions for a layer not normally considered critical to the lithography process (such as the thickness of the buried oxide in SOI wafers) can change the dimensions or shapes of the printed feature, if this process change affected the optical response of the layer.

As a minimum, the complex refractive index (refractive index n and extinction coefficient κ) of all layers needs to be known at the lithography wavelength. Literature data for such properties are usually not available or obsolete and not reliable (derived from obsolete reflectance measurements on materials of unknown quality followed by Kramers-Kronig transform). In ideal cases, n and κ can be measured inline using spectroscopic ellipsometry at the exposure wavelength. Especially below 193 nm, such measurements are very difficult and usually performed outside of the fab by engineering personnel. EUV optical properties can only be determined using specialized light sources (such as a synchrotron). Therefore, materials composition is often used as a figure of merit, when direct measurement of the optical properties is not practical. But even two materials with the same composition can have different optical properties (take amorphous and crystalline Si as an example).

Additional complications in the determination of the optical properties of a material arise from surface roughness, interfacial layers, birefringence, or optical anisotropy (often seen in photoresists or other organic layers responding to stress), or depth-dependent composition. For some materials for a wafer fab, it is impossible to determine the optical properties of such material, since the inverse problem of fitting the optical constants from the ellipsometric angles is underdetermined. Therefore, physical materials characterization must accompany the determination of optical properties, since physical characteristics, materials properties, and optical constants are all inter-related.

Overlay measurements are challenged by phase shift masks (PSM) and optical proximity correction (OPC) masks, and the use of different exposure tools and/or techniques for different process layers will compound the difficulty. Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with scanning probe microscopy (SPM). The need for new target structures has been suggested as a means of overcoming the issues associated with phase shift mask and optical proximity mask alignment errors not detectable with traditional targets. Overlay for on-chip interconnect will continue to be challenging. The use of chemical mechanical polishing for planarization degrades target structures. Thus as requirements for tighter overlay control are introduced, the line edge of overlay targets in interconnect are roughened. The low-κ materials used as insulators will continue to make overlay more difficult especially as porous low κ move into manufacturing.

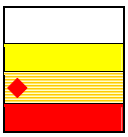
The dramatic tightening of the overlay budget up to 20% [or 25%] of the device half-pitch, required for advanced applications in DRAM and NVM, calls for a faster introduction of alternative measuring solutions, like high-voltage SEM and scatterometry techniques, which are still far from being mature enough today, and may require breakthroughs also in metrology integration.

The Lithography Metrology Requirements Tables are divided into wafer and mask requirements Tables 118a and b, and 118 a, b, c, and d, respectively. The mask metrology requirements are further divided into the needs for each type of exposure technology: optical, EUV, and electron projection.

Table 118a Lithography Wafer Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
Flash ½ Pitch (nm) (Un-contacted Poly)	*76*	*64*	*57*	*51*	*45*	*40*	*36*	*32*	*28*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Printed gate CD control (nm) Uniformity (variance) is 12% of CD Allowed lithography variance = 3/4 total variance of physical gate length *	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.4
Wafer dense line CD control (nm) * Uniformity is 13.5% of CD Allowed lithography variance = 3/4 total variance	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
Wafer minimum contact hole (nm, post etch) from lithography tables	85	72	64	57	51	45	40	36	32
Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	10.4	8.8	7.8	7.0	6.2	5.5	4.9	4.4	3.9
Line width roughness (nm, 3 σ) < 8% of CD ***	2.6	2.2	2	1.8	1.6	1.4	1.3	1.1	1
Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.67	0.58	0.52	0.46	0.42	0.37	0.33	0.29	0.27
Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	1.77	1.49	1.33	1.18	1.05	0.94	0.84	0.74	0.66
Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)****	2.08	1.76	1.57	1.40	1.25	1.10	0.98	0.88	0.78
Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.52	0.44	0.40	0.36	0.32	0.28	.25	0.22	0.20
Maximum CD measurement bias (%)	10	10	10	10	10	10	10	10	10
Aspect Ratio Capability for Trench Structure CD Metrology	15:1	15:1	15:1	15:1	15:1	15:1	15:1	15:1	20:1
Wafer overlay control (nm)	15	13	11	10	9	8	7.1	6.4	5.7
Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	1.51	1.27	1.13	1.01	0.90	0.80	0.71	0.64	0.57

** All precision values are 3 Sigma in nm and include metrology tool-to-tool matching. Requirement is for precision value at top, middle, and bottom CD.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology generation dimension. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.
***** Bottom CD for contacts presently requires measurement by FIB.*



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 118b Lithography Wafer Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash ½ Pitch (nm) (Un-contacted Poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Printed gate CD control (nm) Uniformity (variance) is 12% of CD Allowed lithography variance = 3/4 total variance of physical gate length *	1.1	1.0	0.9	0.8	0.7	0.6	0.6
Wafer dense line CD control (nm) * Uniformity is 13.5% of CD Allowed lithography variance = 3/4 total variance	3.0	2.6	2.3	2.1	1.9	1.7	1.5
Wafer minimum contact hole (nm, post etch) from lithography tables	28	25	23	20	18	16	14
Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	3.4	3.1	2.8	2.4	2.2	2.0	1.7
Line width roughness (nm, 3 σ) <8% of CD ***	.9	0.8	0.7	.6	0.6	.5	.5
Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.23	0.21	0.19	0.17	0.15	0.12	0.12
Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	0.59	0.53	0.47	0.42	0.37	0.33	0.30
Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)****	0.69	0.61	0.56	0.49	0.44	0.39	0.34
Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	.18	0.16	0.14	.13	0.12	.1	.1
Maximum CD measurement bias (%)	10	10	10	10	10	10	10
Aspect Ratio Capability for Trench Structure CD Metrology	20:1	20:1	20:1	20:1	20:1	20:1	20:1
Wafer overlay control (nm)	5.1	4.5	4.0	3.6	3.2	2.8	2.5
Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	0.51	0.45	0.40	0.36	0.32	0.28	0.25

** All precision values are 3 Sigma in nm and include metrology tool-to-tool matching. Requirement is for precision value at top, middle, and bottom CD.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology generation dimension. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.
***** Bottom CD for contacts presently requires measurement by FIB.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

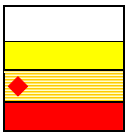


Table 119a Lithography Metrology (Mask) Technology Requirements: Optical—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU gate in resist (nm)	*54*	*48*	*42*	*38*	*34*	*30*	*27*	*24*	*21*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Flash ½ Pitch (nm) (Un-contacted Poly)	76	64	57	51	45	40	36	32	28
DRAM/Flash CD control (3sigma) (nm)	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	3.8	3.4	3.0	2.6	2.4	2.2	1.9	1.7	1.6
Wafer overlay control (nm)	15	13	11	10	9	8	7	6	6
DRAM Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Wafer contact CD control (nm)* Uniformity is 13.5% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	10.0	8.4	7.5	6.6	5.9	5.3	4.7	4.2	3.7
Mask nominal image size (nm) [B]	214	191	170	151	135	120	107	95	85
Mask minimum primary feature size [D]	150	133	119	106	94	84	75	67	59
Optical Section									
Minimum OPC size (opaque at 4×, nm) [D]	90	80	70	64	56				
Image placement (nm, multi-point) [F]	9	8	7	6.1	5.4	4.8	4.3	3.8	3.4
CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Mask error factor (MEF) from lithography tables isolated lines, binary	1.4	1.4	1.6	1.8	2	2.2	2.2	2.2	2.2
MEEF dense lines, binary or attenuated phase shift mask [G]	2	2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
MEF contacts [G]	3	3	3.5	4	4	4	4	4	4
CD Uniformity (3 Sigma at 4×, nm) Refer to Lithography Chapter Table for Optical Mask Requirements									
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	3.8	3.3	2.6	2.0	1.7	1.4	1.2	1.1	1.0
Mask CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	7.1	6.0	4.8	4.3	3.8	3.4	3.0	2.7	2.4
Mask contact CD control (nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	4.7	4.0	3.0	2.4	2.1	1.9	1.7	1.5	1.3
Mask image placement metrology (precision, P/T=0.1)	0.9	0.8	0.7	0.6	0.5	0.5	0.4	0.4	0.3
Mask CD precision (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] (P/T=0.2 for isolated lines, binary**)	0.8	0.7	0.5	0.4	0.3	0.3	0.2	0.2	0.2
Mask CD precision (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	1.4	1.2	0.96	0.86	0.77	0.68	0.61	0.54	0.48
Mask contact CD precision(nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	0.9	0.8	0.6	0.5	0.4	0.4	0.3	0.3	0.3
Specific Requirements									
Alternated PSM phase mean deviation	2	1	1	1	1	1	1	1	1
Phase metrology precision, P/T=0.2	0.4	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3	3	3	3	3	3	3
Phase uniformity metrology precision, P/T=0.2	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6

Table 119b Lithography Metrology (Mask) Technology Requirements: Optical—Long-term Years

Optical Masks not part of potential solutions beyond 22 nm, grey-colored cells indicate the transition

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Flash ½ Pitch (nm) (Un-contacted Poly)	**25**	**23**	**20**	**18**	**16**	**14**	**13**
DRAM/Flash CD control (3sigma) (nm)	**3.0**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**	**1.5**
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**1.3**	**1.2**	**1.1**	**1.0**	**0.8**	**0.7**	**0.7**
Wafer overlay control (nm)	**5**	**5**	**4**	**4**	**3**	**3**	**3**
DRAM Contact after etch (nm)	**28**	**25**	**23**	**20**	**18**	**16**	**14**
Wafer contact CD control (nm)* Uniformity is 13.5% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	**3.3**	**3.0**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**
Mask nominal image size (nm) [B]	**76**	**67**	**60**	**54**	**48**	**42**	**38**
Mask minimum primary feature size [D]	**53**	**47**	**42**	**37**	**33**	**30**	**26**
Optical Section							
Minimum OPC size (opaque at 4×, nm) [D]							
Image placement (nm, multi-point) [F]	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**	**1.7**	**1.5**
CD uniformity allocation to mask (assumption)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Mask error factor (MEF) from lithography tables isolated lines, binary	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
MEEF dense lines, binary or attenuated phase shift mask [G]	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
MEF contacts [G]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
CD Uniformity (3 Sigma at 4×, nm) Refer to Lithography Chapter Table for Optical Mask Requirements							
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**0.8**	**0.8**	**0.7**	**0.6**	**0.5**	**0.5**	**0.5**

Table 119b Lithography Metrology (Mask) Technology Requirements: Optical—Long-term Years (continued)

Optical Masks not part of potential solutions beyond 22 nm, grey-colored cells indicate the transition

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
Mask CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	2.1	1.9	1.7	1.5	1.4	1.2	1.1
Mask contact CD control (nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	1.2	1.1	0.9	0.8	0.7	0.7	0.6
Mask image placement metrology (precision, P/T=0.1)							
Mask CD precision (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] (P/T=0.2 for isolated lines, binary**)	0.2	0.2	0.1	0.1	0.1	0.1	0.1
Mask CD precision (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	0.43	0.38	0.34	0.30	0.27	0.24	0.21
Mask contact CD precision(nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	0.2	0.2	0.2	0.2	0.1	0.1	0.1
Specific Requirements							
Alternated PSM phase mean deviation							
Phase metrology precision, P/T=0.2							
Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3				
Phase uniformity metrology precision, P/T=0.2	0.6	0.6	0.6				

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

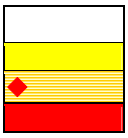


Table 119c Lithography Metrology (Mask) Technology Requirements: EUV—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Flash ½ Pitch (nm) (Un-contacted Poly)				51	45	40	36	32	28
Image placement error (nm, multipoint)				6.1	5.4	4.8	4.3	3.8	3.4
CD Uniformity (3 sigma at 4×, nm)									
Isolated lines (MPU gates) Uniformity is 10% of CD Mask error factor varies with year				3.4	3.0	2.7	2.4	2.1	1.9
Dense lines (DRAM half-pitch) Uniformity is 15% of CD Mask error factor varies with year				8.2	7.3	6.5	5.8	5.2	4.6
DRAM contact after Etch				57	51	45	40	36	32
Contact/Vias Uniformity is 10% of CD mask error factor varies with year				7.6	6.8	4.8	4.3	3.8	3.4
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**				0.68	0.61	0.54	0.48	0.43	0.38
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**				1.6	1.5	1.3	1.2	1.0	0.92
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**				1.5	1.4	1.0	0.86	0.76	0.68
Specific Requirements									
Mean peak reflectivity				65%	66%	66%	66%	67%	67%
Peak reflectivity uniformity (3 sigma %)				0.69%	0.58%	0.47%	0.42%	0.37%	0.33%
Absorber sidewall angle tolerance (degrees)				1	1	0.75	0.69	0.62	0.5
Absorber LER (3 sigma, nm)				3.2	2.8	2.5	2.2	2.0	1.8
Mask substrate flatness (peak-to-valley, nm)				75	60	50	41	36	32
Metrology mean peak reflectivity precision (P/T=0.2, %)				1.30%	1.30%	1.30%	1.30%	1.30%	1.30%
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)				0.14%	0.12%	0.09%	0.08%	0.07%	0.07%
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)				0.20	0.20	0.15	0.14	0.12	0.10
Absorber LER metrology precision (3 sigma, P/T=0.2)				0.64	0.57	0.50	0.45	0.40	0.36
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)				15	12	10	8.2	7.3	6.5

Before 22 nm; grey-colored cells indicate the transition to EUV technology.

**All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
***Measurement tool performance needs to be independent of target shape, material, and density.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

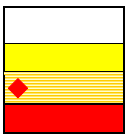


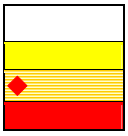
Table 119d Lithography Metrology (Mask) Technology Requirements: EUV—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Flash ½ Pitch (nm) (Un-contacted Poly)	25	23	20	18	16	14	13
Image placement error (nm, multipoint)	3	2.7	2.4	2.1	1.9	1.7	1.5
CD Uniformity (3 sigma at 4×, nm)							
Isolated lines (MPU gates) Uniformity is 10% of CD Mask error factor varies with year	1.7	1.5	1.3	1.2	1.1	1.0	0.9
Dense lines (DRAM half-pitch) Uniformity is 15% of CD Mask error factor varies with year	4.1	3.7	3.3	2.9	2.6	2.3	2.1
DRAM contact after Etch	28	25	23	20	18	16	14
Contact/Vias Uniformity is 10% of CD mask error factor varies with year	3.0	2.7	1.8	1.6	1.4	1.3	1.1
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**	0.34	0.30	0.27	0.24	0.21	0.19	0.17
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**	0.82	0.73	0.65	0.58	0.52	0.46	0.41
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**	0.61	0.54	0.36	0.32	0.29	0.26	0.23
Specific Requirements							
Mean peak reflectivity	67%	67%	67%	67%	67%	67%	67%
Peak reflectivity uniformity (3 sigma %)	0.29%	0.26%	0.23%	0.21%	0.19%	0.17%	0.15%
Absorber sidewall angle tolerance (degrees)	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Absorber LER (3 sigma, nm)	1.6	1.4	1.3	1.1	1.0	0.9	0.8
Mask substrate flatness (peak-to-valley, nm)	29	26	23	20	18	16	14
Metrology mean peak reflectivity precision (P/T=0.2, %)	1.30%	1.30%	1.30%	1.30%	1.30%	1.30%	1.30%
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)	0.06%	0.05%	0.05%	0.04%	0.04%	0.03%	0.03%
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)	0.10	0.10	0.10	0.10	0.10	0.10	0.10
Absorber LER metrology precision (3 sigma, P/T=0.2)	0.32	0.28	0.25	0.22	0.20	0.18	0.16
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)	5.8	5.1	4.6	4.1	3.6	3.2	2.9

Grey cells indicate transition years of technologies.

**All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
***Measurement tool performance needs to be independent of target shape, material, and density.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 119 a and b:
[A] The designation for CD measurement for isolated lines in the near term is a result of roadmap process range and the need for tool matching in the precision requirement makes this requirement very difficult to achieve. A work-around for isolated line CD measurement is to use a single tool and avoid tool matching. Long term, CD measurement for 25 nm linewidths requires a technology breakthrough because extension of known methods may not be possible.
[B] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio that equals 4×.
[C] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.
[D] Mask OPC Feature size—Minimum width of the smallest non-printing features on the mask.
[E] The CD process range for isolated gate lithography is 4/5 of the total CD process range of 1/10 the CD at 3σ.
The CD process range is 4/5 of the 15% of CD for dense lines and 2/3 the 15% for contact/via. Process ranges are variances. It is important to note that the mask part of the lithography process range is allowed 40% of the total lithography process range. The mask error factor (MEF) reduces the CD process range, and its effect is calculated by dividing the process range by the MEF.
[F] The mask error factor for isolated lines on a binary mask changes from 1.4 to 1.6 at 65 nm.
[G] The mask error factor for alternating phase shift masks is 1.
[H] The mask error factor for dense lines is 2 from the 100nm to 70 nm . It is 2.5 at 65 nm, and is 3 for 57 and 50 nm.
[I] The mask error factor for contact and via lines is 3 from the 100nm to 70 nm. It is 3.5 at 65 nm, and is 4 for 57 and 50 nm.

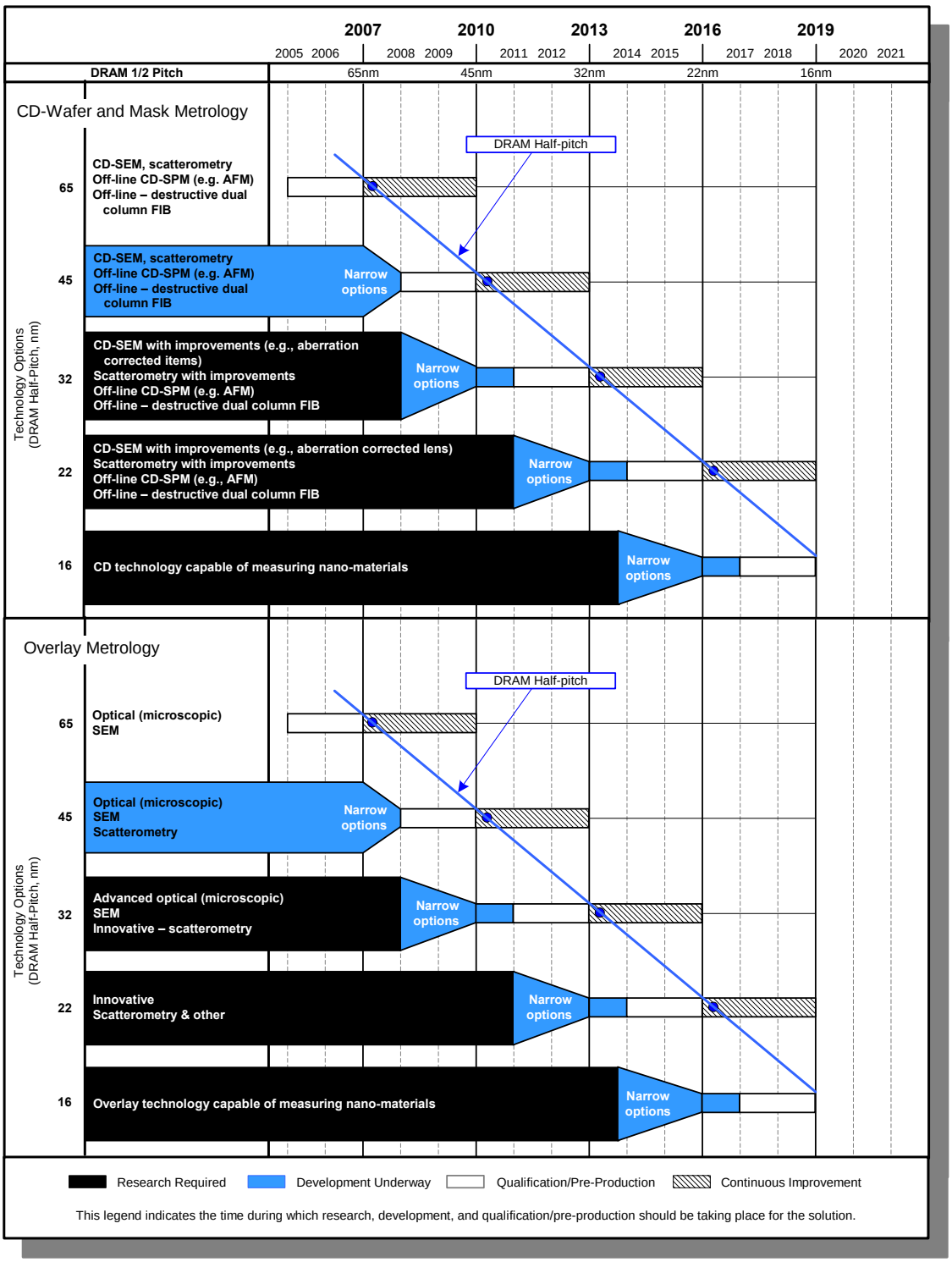


Figure 106 Lithography Metrology Potential Solutions

FRONT END PROCESSES METROLOGY

The device community has shown that CMOS-like transistors, which are referred to as non-classical CMOS, are likely to be the switching devices that will be manufactured over the next fifteen years. The choice of process and design drive the final selection of metrology. It is likely that a variety of different designs will be used, and that Front End Processes and

transistor design will become more of a competitive advantage for IC manufacturers. Many experts believe that FINFETs and CMOS on ultra-thin SOI are the most like candidate technologies. Metal gate electrode and "wrap around" gates with high-κ dielectric stacks. The many ways that process technology has been used to provide stress induced channel mobility is but one example of how diverse processes have become. Metrology development is hard pressed to meet the challenges posed by the accelerated introduction of new technology generations. This requires accelerated advancements of metrology for transistor development and fabrication. In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front-end plasma etch technologies are covered. Process integration issues such as the need to control leakage current and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Metrology requirements for Front End Processes are shown in Table 120, and the Potential Solutions are shown in Figure 107.

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
*Metrology for metal gate thickness and composition**									
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**	**0.5x10^{10}**
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**	**0.5x10^{9}**
High-performance EOT (Extended planar bulk)	**1.2**	**1.1**	**1.1**	**0.9**	**0.75**	**0.65**	**0.5**	**0.5**	
High-performance EOT (FDSOI)				**0.9**	**0.8**	**0.7**	**0.6**	**0.5**	**0.5**
High-performance EOT (DG)							**0.8**	**0.7**	**0.6**
Low power EOT (bulk)	**1.4**	**1.3**	**1.2**	**1.1**	**1**	**0.9**	**0.9**	**0.9**	
Low power EOT (DG)							**0.9**	**0.9**	**0.8**
Low power EOT (FD)							**0.9**	**0.9**	**0.8**
± 3σ dielectric process range (EOT) (nm)	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**
EOT measurement precision 3σ (nm) [B]	**0.0048**	**0.0044**	**0.0044**	**0.0036**	**0.003**	**0.0026**	**0.002**	**0.002**	**0.002**
DRAM stacked capacitor structure including electrodes	**Cylinder /Pedestal MIM**	**Cylinder /Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM/ others**	**Pedestal MIM**	**Pedestal MIM/ others**	**Pedestal MIM/ others**
DRAM stacked capacitor electrodes (near term)	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**
DRAM stacked capacitor dielectric material	**ALO/TAO /others**	**ALO/TAO /others**	**ALO/TAO/ others**	**ALO/TAO/ others**	**ALO/TAO/ others**	**ALO/TAO/ others**	**new material**	**new material**	**new material**
DRAM stacked capacitor dielectric constant	**40**	**50**	**50**	**50**	**50**	**50**	**50**	**60**	**60**
EOT (nm) for stacked capacitor	**1.8**	**1.4**	**0.8**	**0.8**	**0.8**	**0.7**	**0.7**	**0.6**	**0.5**
DRAM stacked capacitor dielectric physical thickness (nm)	**18**	**17.5**	**10**	**10**	**10**	**8.75**	**8.75**	**9**	**7.5**
± 3 σ process range	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**
DRAM capacitor dielectric physical thickness measurement precision (nm 3s) [C]	**0.0072**	**0.0056**	**0.0032**	**0.0032**	**0.0032**	**0.0028**	**0.0028**	**0.0024**	**0.002**
Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	**1.5–2.5 E18**	**2.0–4.0 E18**	**2.5–5.0 E18**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**
Dopant atom	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008	**17.6**	**15.4**	**13.8**	**8.8**	**8**	**7.2**	**12.8**	**11.2**	**10.4**
Extension lateral abruptness (nm/decade) [M]	**3.5**	**3.1**	**2.8**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	**3.5**	**3.1**	**2.8**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
At-line dopant concentration precision (across concentration range) [D]	**4%**	**4%**	**4%**	**4%**	**4%**	**2%**	**2%**	**2%**	**2%**
Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]		**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	
Metal gate work function for FDSOI MPU/ASIC | fm – Ei| (eV)| NMOS/PMOS [***]				**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**
Metal gate work function for multi-gate MPU/ASIC [***]							**midgap**	**midgap**	**midgap**
Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]		**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Metal gate workfunction for FDSOI LOP [***]							**midgap**	**midgap**	**midgap**
Metal gate work function for multi-gate LOP [***]							**midgap**	**midgap**	**midgap**
Metal gate work function for bulk LSTP |Ec,v – fm| (eV) [***]				**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Metal gate work function for FDSOI and multi-gate LSTP | fm - Ei| (eV)| NMOS/PMOS [***]									
*Metrology for metal gate thickness and composition**									
Starting silicon layer thickness (SOI) (fully depleted) (tolerance ± 5%, 3s) (nm) [M]	**20–36**	**19–34**	**18–33**	**17–31**	**16–30**	**15–19**	**15–18**	**14–17**	**14–17**
SOI Si thickness precision (3s in nm)	**0.1**	**0.095**	**0.09**	**0.085**	**0.08**	**0.075**	**0.075**	**0.07**	**0.07**

Grey cells indicate transition years of technologies.

** Cell colors indicate this is an overarching metrology for metal gate thickness and composition that are critical challenges during the long-term years.*

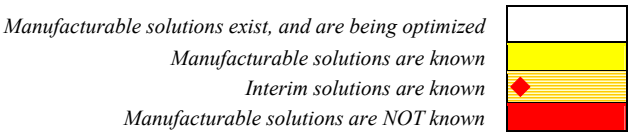


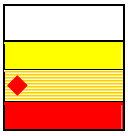
Table 120b Front End Processes Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
*Metrology for metal gate thickness and composition**							
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**$0.5x10^{10}$**	**$0.5x10^{10}$**	**$0.5x10^{10}$**	**$0.5x10^{10}$**	**$0.5x10^{10}$**	**$0.5x10^{10}$**	**$0.5x10^{10}$**
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**$0.5x10^{9}$**	**$0.5x10^{9}$**	**$0.5x10^{9}$**	**$0.5x10^{9}$**	**$0.5x10^{9}$**	**$0.5x10^{9}$**	**$0.5x10^{9}$**
High-pPerformance EOT (Extended planar bulk)							
High-performance EOT (FDSOI)	**0.5**	**0.5**					
High-performance EOT (DG)	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Low power EOT (bulk)							
Low power EOT (DG)	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**	**0.7**
Low power EOT (FD)	**0.8**	**0.8**	**0.7**	**0.8**			
± 3σ dielectric process range (EOT) (nm)	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**
EOT measurement precision 3σ (nm) [B]	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**	**0.002**
DRAM stacked capacitor structure including electrodes	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**	**Pedestal MIM**
DRAM stacked capacitor electrodes (near term)							
DRAM stacked capacitor dielectric material	**new material**	**new material**					
DRAM stacked capacitor dielectric constant	**70**	**80**	**80**	**90**	**100**		
EOT (nm) for stacked capacitor	**0.5**	**0.4**	**0.4**	**0.3**	**0.25**		
DRAM stacked capacitor dielectric physical thickness (nm)	**8.75**	**8**	**8**	**6.75**	**6.25**	**0**	**0**
± 3 σ process range	**± 4%**	**± 4%**	**± 4%**	**± 4%**	**± 4%**		
DRAM capacitor dielectric physical thickness measurement precision (nm 3s) [C]	**0.002**	**0.0016**	**0.0016**	**0.0012**	**0.001**	**0**	**0**
Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	**NA**	**NA**	**NA**	**NA**	**NA**		
Dopant atom	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**		
Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008	**8.8**	**8**	**7.2**	**6.4**	**5.6**		
Extension lateral abruptness (nm/decade) [M]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**		
Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**		

Table 120b Front End Processes Metrology Technology Requirements—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
At-line dopant concentration precision (across concentration range) [D]	2%	2%	2%	2%	2%		
Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]							
Metal gate work function for FDSOI MPU/ASIC | fm – Ei| (eV)| NMOS/PMOS [***]	± 0.1	± 0.1					
Metal gate work function for multi-gate MPU/ASIC [***]	midgap	midgap	midgap	midgap	midgap	midgap	midgap
Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]							
Metal gate work function for FDSOI LOP [***]	midgap	midgap	midgap	midgap	midgap	midgap	midgap
Metal gate work function for multi-gate LOP [***]	midgap	midgap	midgap	midgap	midgap	midgap	midgap
Metal gate work function for bulk LSTP |Ec,v - fm| (eV) [***]							
Metal gate work function for FDSOI and multi-gate LSTP | fm - Ei| (eV)| NMOS/PMOS [***]	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
Starting silicon layer thickness (SOI) (fully depleted) (tolerance ± 5%, 3s) (nm) [M]	13–16	13–15	13–15	12–14	12–14		
SOI Si thickness precision (3s in nm)	0.065	0.065	0.065	0.06	0.06	0.1	0.1

Grey cells indicate transition years of technologies.
** Cell colors indicate this is an overarching metrology for metal gate thickness and composition that are critical challenges during the long-term years.*



Notes for Table 120a and b:
[A] The use of SOI wafers requires metrology development.
[B] Precision calculated from P/T=0.1=6× precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as Ta_2O_5 will be used at and after the 70 nm logic half pitch and possibly at 100 nm. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\varepsilon_{high-\kappa}/\varepsilon_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick Ta_2O_5 (κ= ~25) layer has a 1 nm equivalent oxide (κ =3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.
[C] In the case of MIS structure, physical thickness, $t_{(diel)}$, is calculated using the equation of $t_{(diel)}=(t_{eq.ox}\text{-}1\ nm)_{diel}\ \varepsilon_{high-\kappa}/3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, t_{diel} is calculated using the equation of $t_{diel}= t_{eq.ox}\ \varepsilon_{high-\kappa}/3.9$. Here teq.ox is equivalent oxide thickness, and t_{diel} is dielectric constant of the dielectric material.
[D] High- precision measurements with low systematic error are required.

The impact of shrinking dimension on FEP metrology is already the point where research devices and materials exhibit materials properties associated with nano-science. For example, the optical properties of ultra-thin SOI below 5 nm as associated with quantum confinement. Furthermore, the properties of nanowire like shapes such as a FIN in a FINFET are quantum confined in two dimensions. The dielectric function of crystalline materials is characterized by the critical points associated with direct or indirect transitions between the valence and conduction bands. The energy of these critical points is shifted by quantum confinement or strain.

Starting materials—Many of the metrology challenges related to starting materials involve the emerging class of layered materials such as SOI, strained silicon, and combinations of these technologies. The trend toward thinner layers, along with multiple layer interfaces pose a challenge to most material metrology techniques.

Areas of concern include the following:

- Bulk Ni and Cu measurement on p+, SOI, SSi,and SSOI wafers
- Measurement of 10^{9}–10^{10} cm^{-3} Fe (and other bulk metals) in the top Si of thin SOI wafers
- Measurement variability of nitrogen concentrations < 1×10^{14} cm^{-3} in nitrogen-doped epi and annealed wafers
- Thickness and uniformity of very thin SOI layers (<20 nm)
- Defectivity of thin layers (e.g., threading dislocations, "HF defects")
- Particle detection (<100 nm) on layered surfaces

Metrology requirements for nanotopography (nanometer-scale surface height variation over a 2–20 mm length scale) are still emerging. Small particle detection (< 50 nm) continues to be of concern for the future. Note that the silicon starting materials particle requirements below 90 nm size will not use sub-90 nm metrology but will model the sub-90 nm particle requirement based upon 90 nm particle detection. More information can be found in the Starting Materials section of the *Front End Processes chapter*.

Silicon-On-Insulator (SOI) is entering the mainstream of IC device applications, and this is expected to grow further along the Roadmap. An expectation has been that the materials specifications for polished silicon substrates would be transferred to SOI specifications. However, the underlying insulator structure in SOI negatively affects many of the metrology capabilities used for polished silicon substrates. Thus, there is an inability to measure and control SOI material properties at the level desired. This leads to a major challenge for SOI metrology, one that the metrology community must address soon. For more details on these metrology challenges see the FEP chapter on Starting Materials.

The use of strained silicon without SOI has emerged as potential solution for channel mobility enhancement at an early date than foreseen in the 2001 roadmap. Metrology issues for strained silicon are discussed in the Materials Characterization Section of the Metrology chapter.

Surface preparation—In situ sensors for particles, chemical composition, and possibly for trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Yield Enhancement chapter*. Particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter. The role of impurities in high-κ gate dielectrics, and therefore their measurement requirements, is a future research topic.

Thermal/thin films—Both new materials and new transistor design will continue to challenge metrology over the next fifteen years. The transition from silicon oxynitride to alternate materials with higher dielectric constants remains a key metrology challenge. Development of metrology for high-κ materials needs to continue and metrology for the interface layer remains a difficult challenge. The FEP roadmap shows the first use of high κ in both low-power and high-performance devices in 2005. Potential solutions that enable interfacial control include inline optical metrology that extends either into the infra-red and/orthe ultra-violet wavelength range. FINFET and wrap around gates mean that the gate dielectric is on a sidewall. Continued development and standardization of electrical testing at high frequencies and new methods for dielectric reliability testing are required. Higher κ electrical testing by traditional capacitor and transistor structures, Hg-probe type capacitor testing, and non-contact, corona discharge methods are all under development. There is considerable evidence that the dielectric properties of transistor and capacitor dielectric films after deposition are different from those subsequent to thermal processing, and this complicates comparison of electrical and physical methods. Correlation must improve. Application of materials characterization methods such as scanning transmission electron microscopy and X-ray reflectivity to higher κ materials as well as methods for controlling Ge in SiGe channels are discussed in the Materials and Contamination Characterization section of this Metrology chapter.

Metrology must be further developed for controlling gate electrode processes. Examples of new gate electrode processes and thickness include multiple thickness for poly silicon gate. The control of the thickness, composition, and work function of metal gate electrodes is a new metrology need.

Carrier mobility enhancement through process induce stress continues to be a critical component of transistor technology. Typically, NMOS transistors are given tensile stress through the process conditions and thickness of the silicon nitride cap layer. PMOS transistors are given compressive stress through a variety of means. The replacement of the silicon in

the source and drain with SiGe or the use of tightly controlled design of the shallow trench isolation process are two examples. The distance between the PMOS gate and the STI provides an indication of the stress. Direct measurement of the stress in the nano-sized area of the transistor continues to be difficult to impossible. Through modeling, measurable quantities such as the thickness of the silicon nitride cap layer can be related to NMOS channel mobility. As new processes are introduced, the challenge renews itself. Further complicating the challenge is the timing of the potential transition to stressed silicon substrates and the introduction of FINFETS or wrap around gates.

FERAM—Although the thickness of the dielectric films are 100 to 200 nm, optical models for inline film thickness measurement of the metal oxides must be developed when a new materials set is used. The main metrology need is for fatigue testing of the capacitor structures at 10^{16} read write cycles and above.

Doping technology—Improved inline process measurements to control active dopant implants is required beyond 90 nm. Presently, 4-point probe measurement is used for high dose implant and thermally modulated optical reflectance is used for low-dose implant process control. Both methods require improvement, and a new technique that provides direct *in situ* measurement of dose, dopant profile, and dose uniformity would allow real-time control. New methods for control of B, P, and As implants are also needed, and several inline systems based on x-ray/electron interactions optimized for B, P, and As dose measurement have recently been introduced. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of new, non-destructive measurement methods such as carrier illumination (an optical technology) are under evaluation. Two- and preferably three-dimensional profiling of active dopant concentrations is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology.

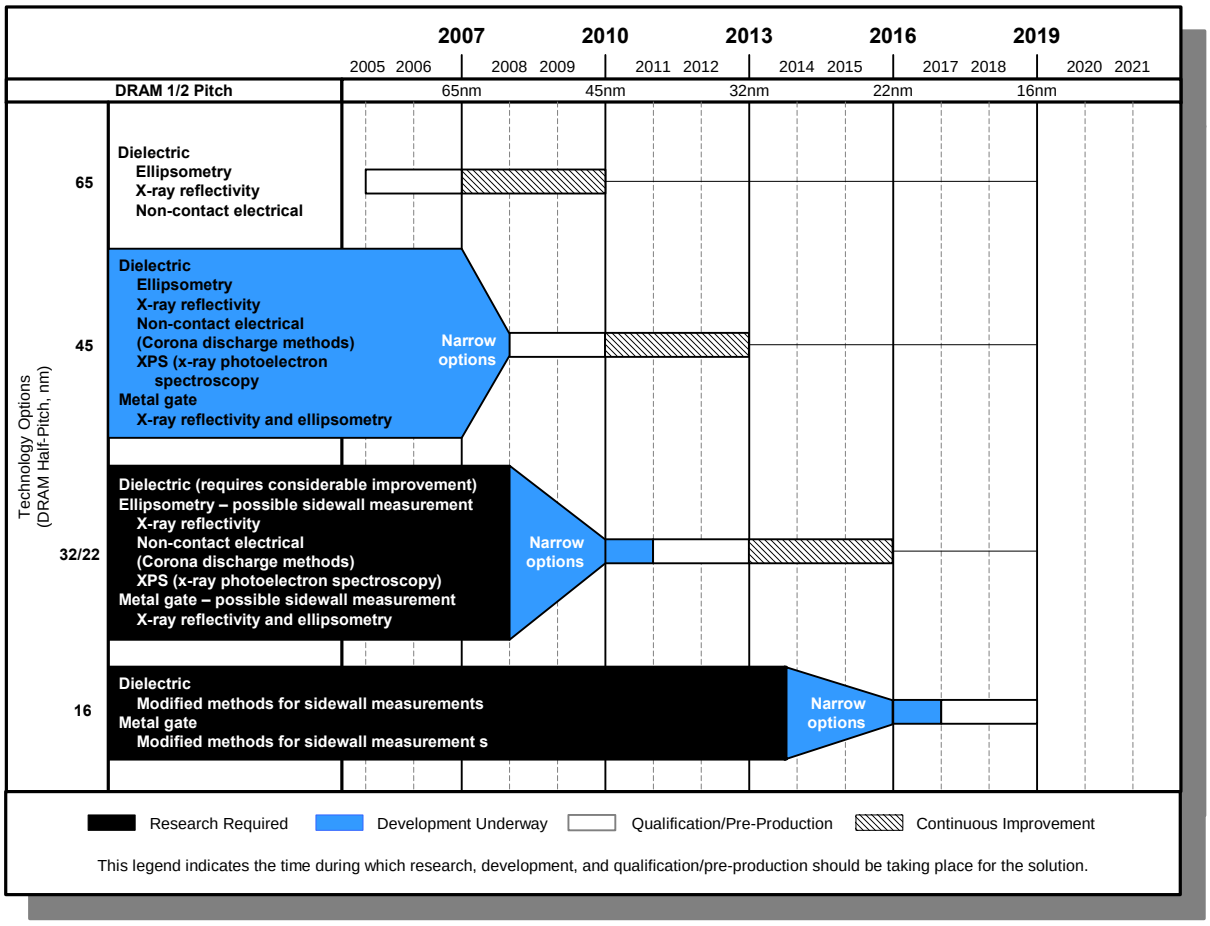


Figure 107 FEP Metrology Potential Solutions

INTERCONNECT METROLOGY

Interconnects, including all of the IC structures necessary to connect from silicon to the boards and boxes of the outside world, have become a potential performance roadblock for the continuation of the semiconductor industry on the Moore's Law curve. This roadblock has components in both technology and cost. It has technology components spanning the necessary transition from aluminum/SiO_2 to Cu/low κ, as well as in transitions to more radical approaches to interconnects beyond the metal/dielectric system. It has cost components in the anticipated high cost of fabrication of alternatives to the incumbent metal dielectric interconnect system for global interconnects using current technology. Among the potential roadblocks and cost issues inherent in the switch from aluminum/SiO_2 to Cu-low κ are the significant challenges for new metrology for process development, manufacturing validation, and process control. For example, in Cu-low κ it is desired to produce minimal thickness barriers between Cu and dielectrics. This has resulted in a need for metrology for detailed characterization of extremely thin layers and "zero thickness" interfaces without the undesirable effects occurring during destructive sample preparation. *One of the most challenging issues facing interconnect metrology is the lack of measurement capability for sidewalls of trenches and vias.* The anticipation of moves to radical interconnect options, such as optical interconnects, has led to new metrology issues such as the need to profile optical properties of very narrow waveguides, and to be able to identify extremely small optical defects in such waveguide materials. Some of the needed metrology problems have been solved with creative applications and advances of existing techniques, and some new techniques have been developed. However, some problems have been identified as particularly difficult, and possibly not having solutions within the confines of currently envisioned metrology techniques.

Interconnect needs for metrology, as noted above, include continuing evolutionary advances in existing metrology techniques, as well as the increasing need for novel metrology approaches for more radical interconnect structures. The following sections will first describe some of the needs and status of existing metrology techniques for current Interconnects, and will then address some of the needed advances for future directions in interconnect.

CU-LOW κ METALLIZATION ISSUES AND METROLOGY NEEDS

CU METALLIZATION ISSUES

The industry now has experience in development and manufacturing of both single- and dual-damascene Cu-low κ interconnects. This experience provides important guidance on what process parameters to control as well as an indication of which measurements are mainly used in research and development, as well as during volume manufacturing. This experience has also identified new needs for metrology, some of which has been provided and some of which remains to be achieved. The processing of Cu interconnects is significantly different than the processing was for aluminum interconnects. The most significant difference is in the use of electrodeposition for depositing the copper, as opposed to the low pressure, reactive deposition methods used for aluminum. This change in deposition method has resulted in many new needs for process metrology. Among the most important of these is the need for precise control of electrochemical deposition baths, and identification of very low-level impurities that may cause resistivity increases in electrochemically deposited copper. We now know that the reliability of copper metal interconnects is degraded by the effects of electro and stress migration, and that the primary degradation modes are associated with surface diffusion of Cu along the interfaces between the Cu and dielectrics and barriers. Voids in metal lines and vias that occur during processing have also been identified as significant yield loss initiators. Voiding problems can show up after deposition/CMP/anneal, or from agglomeration of micro-voids due to electro or stress migration. Another significant problem relating to voids is a need to be able to identify relatively small, isolated voids in large fields of patterned Cu conductors. These isolated voids often do not show up as yield loss, but can be an incipient cause of later reliability failures. These voids may be on the surface of the conductors, but are often buried within the conductor pattern or in vias. Additional issues with Cu metallization arise from the use of thin barriers to isolate the Cu from underlying dielectrics. These thin barriers raise significant needs for measurement capabilities of ultra thin layers, interface properties, and defects and materials structure on sidewalls in very narrow channels.

The problems noted above have all been found to be important for Cu metallization at 90 nm and above. As the industry moves below 90 nm, it is expected that these issues will still be present, but that additional issues will arise. While we do not know all of the new issues that will arise, several problems associated with our inability to extrapolate current techniques to the very small geometries, or increasing importance of currently acceptable limitations of metrology for future technology technology generations, are already clear. Among these future needs for Cu metallization metrology is the increasing importance of metrology for ultra thin layers—especially barriers on sidewalls. This need requires not only the ability to establish physical properties and structure of these layers with thicknesses <2 nm, but also to identify and characterize defects in the films. An additional problem area that is currently not extensively studied, but that is expected to become increasingly important at smaller conductor geometries is the interface between the Cu and the barrier or

dielectric that it interfaces. As the Cu conductors become smaller, it is expected that interface scattering will cause significant increases in resistivity of very narrow lines.

CU METALLIZATION METROLOGY

Copper electroplating systems need quantitative determination of the additives, byproducts and inorganic contents in the bath to maintain the desired properties in the electroplated copper film. Process monitoring requires *in situ* measurements of additives, byproducts and inorganic content that result from bath aging. A mass spectrometry based method of real-time sampling of bath contents provides a new potential solution. Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid Chromatography can be used to quantitative measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for the monitoring of inorganics.

There is some concern about the application of statistical process control to very thin barrier layers. Interconnect technical requirements indicate that barrier layers for future technology will be <5 nm thick. The 2001 ITRS specified a process window of 20% total thickness variation. The measurement precision (6σ) for a 6 nm film must be $\leq$0.12 nm, which is beyond current capabilities. It may be possible to use existing metrology capability to determine the presence or absence of these very thin films without using traditional SPC. Presently, a number of measurement methods are capable of measuring a barrier layer under seed copper when the films are horizontal. These methods include acoustic methods, X-ray reflectivity, and X-ray fluorescence. Some of these methods can be used on patterned wafers. At-line determination of the crystallographic texture (grain orientation) has been demonstrated using grazing X-ray diffraction. Detection of voids in copper lines is most useful after CMP and anneal processes. A metric for copper void content has been proposed in the Interconnect Roadmap and in line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Many of the methods are based on detection of changes in the total volume of the copper lines. The typical across-chip variation in the thickness of copper lines will mask the amount of voiding that these methods can observe. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, spatially resolved (for product wafers) multi-layer thickness measurements.

Inline measurement of crystallographic phase and crystallographic texture (grain orientation) of copper/barrier films is now possible using X-ray diffraction based methods. This technology is under evaluation for process monitoring, and the connection to electrical properties and process yield is being investigated.

Post CMP processes for interconnect structures require measurement of dishing and erosion in the copper lines. Current optical and acoustic techniques have been explored, but need to address the statistical sampling requirements for the accurate detection of dishing and erosion on a manufacturing environment.

Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.

Advances in measurement technology have enabled *in situ* control of Chemical Mechanical Polishing (CMP) and determination of the thickness of buried barrier films on horizontal surfaces. The pose size distribution of porous low κ can be measured using small angle X-ray scattering or ellipsometric porisimetry. Although voids can be detected in fields of copper lines, most methods determine a change in the volume of copper lines. Thus, process induced changes such as those that occur across the wafer from CMP can mask the presence of voids. Metrology for inline control of bath chemistry is being implemented.

Some measurements remain elusive. For example, measurement of barrier and seed copper film thickness on sidewalls is not yet possible. Recently crystallographic texture measurements on sidewalls have been reported. Adhesion strength measurements are still done using destructive methods. End point detection for etch must be developed for new etch stop materials for porous low κ. Detection of killer pores and voids is not yet possible.

The accelerated reduction in feature size makes development of metrology for high aspect ratio features a greater challenge for on-chip interconnect development and manufacture. Critical dimension measurements are also a key enabler for development of interconnect processes. CD metrology must be extended to very high aspect ratio structures made from porous dielectric materials and requires 3D information for trench and via/contact sidewalls. These measurements will be further complicated by the underlying multi film complexity.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline measurements for interconnect structures are made on simplified structures or monitor wafers and are often destructive. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide

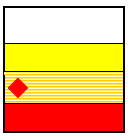
physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Metrology requirements for Interconnect are shown in Table 121 and the potential solutions are shown in Figure 108 below. The new measurement requirements for void detection in copper lines and killer pores in low κ appears to be difficult or impossible to meet. The need is to have a rapid, inline observation of very small number of voids/larger pores. The main challenge is the requirement that the information be a statistically significant determination at the percentage specified in Table 121.

Table 121a Interconnect Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	500	500	500	500	500	500	500	500	500
Measurement of deposited barrier layer at thickness (nm)	7.3	6	5.2	4.3	3.7	3.3	2.9	2.6	2.4
Process range (± 3σ)	10%	10%	10%	10%	10%	10%	10%	10%	10%
Precision σs (nm) for P/T=0.1 [B]	0.073	0.06	0.052	0.043	0.037	0.033	0.029	0.026	0.024
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	24	21	19	17	15	14	13	13	10
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1% or more of total metal level conductor volume of copper lines and vias.	8	7	6.5	5.7	5	4.5	4	3.5	3.2
Detection of killer pore in ILD at (nm) size	8	7	6.5	5.7	5	4.5	4	3.5	3.2
Measure interlevel metal insulator bulk/effective dielectric constant (κ) and anisotropy on patterned structures [C]	≤ 2.7 3.1–3.4	≤ 2.7 3.1–3.4	≤ 2.4 2.7–3.0	≤ 2.4 2.7–3.0	≤ 2.2 2.5–2.8	≤ 2.2 2.5–2.8	≤ 2.2 2.5–2.8	≤ 2.0 2.3–2.6	≤ 2.0 2.3–2.6

Table 121b Interconnect Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	500	500	500	500	500	500	500
Measurement of deposited barrier layer at thickness (nm)	2.1	1.9	1.7	1.5	1.3	1.2	1.1
Process range (± 3σ)	10%	10%	10%	10%	10%	10%	10%
Precision σs (nm) for P/T=0.1 [B]	0.021	0.019	0.017	0.015	0.013	0.012	0.011
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	10	9	8	7	7	6	6
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1% or more of total metal level conductor volume of copper lines and vias.	2.8	2.5	2.2	2	1.8	1.6	1.4
Detection of killer pore in ILD at (nm) size	2.8	2.5	2.2	2	1.8	1.6	1.4
Measure interlevel metal insulator bulk/effective dielectric constant (κ) and anisotropy on patterned structures [C]	≤ 2.0 2.3–2.6	≤ 1.8 2.1–2.4	≤ 1.8 2.1–2.4	≤ 1.8 2.1–2.4	≤ 1.6 1.9–2.2	≤ 1.6 1.9–2.2	≤ 1.6 1.9–2.2



LOW κ DIELECTRICS ISSUES AND METROLOGY NEEDS

LOW κ DIELECTRIC ISSUES

The move from SiO_2 to other dielectrics to provide lower dielectric constants in interconnect structures is proving as much, if not more, of a challenge to the semiconductor industry than the move from Al metallization to Cu. A significant part of the difficulties has come from the fact that low κ materials available thus far have significantly different physical and mechanical properties than the prior SiO_2. Among the primary differences are significantly different mechanical properties, and the presence of pores in the material. The lower mechanical strength has resulted in a new set of issues stemming from problems resulting from materials and processes used in back end manufacturing showing up as problems at assembly and packaging. A significant part of the problem is that there is no convenient and competent metrology tools and methodology to qualify materials at the back end process stage for assembly and packaging viability. A second major issue has been identified with characterization of porous materials. At the present time there are no metrology techniques and methodologies to identify anomalously large or significantly connected pores (so called "killer pores") in otherwise smaller pored materials. There are also no available metrology techniques to characterize the materials on the sidewalls of low κ patterns for physical properties, chemical structure, and electrical performance. This capability needs to be able to identify and quantify very thin layers on these sidewalls related to physical layers and damage due to processes such as pore sealing and plasma etch. These features need to be quantifiable both on continuous sidewall surfaces and into pores on porous materials. The two issues noted above, along with the standard measurements associated with dielectrics, need to be addressed for not only today's dielectrics, but also for those that will be used in the few nanometer generations of the not too distant future.

LOW-κ METROLOGY

Inline metrology for non-porous low-κ processes is accomplished using measurements of film thickness and post CMP flatness. *In situ* sensors are widely used to control CMP. Metrology continues to be a critical part of research and development of porous low-κ materials. The need for transition of some of the measurements used during process development into volume manufacturing is a topic of debate. Examples include pore size distribution measurement. Pore size distribution has been characterized off-line by small angle neutron scattering, positron annihilation, a combination of gas absorption and ellipsometry (ellipsometric poresimetry), and small angle X-ray scattering (SAXS). SAXS and ellipsometric poresimetry can be used next to (at-line) a manufacturing line. The need for moving these methods into the fab is under evaluation. Detection of large, "killer, pores in patterned low κhas been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap.

High-frequency measurement of low-κ materials and test structures has been developed up to 40 GHz. This needs to be extended to ~100 GHz because 20 GHz clocks have rising and falling edges much above 40 GHz. As a result of extensive evaluation, the interconnect community no longer considers this measurement a critical need in the near term. Low-κ materials seem to have constant dielectric functions over the frequency range of interest (from 1 GHz to 10 GHz).

Thinning of porous low κ during chemical mechanical polishing technology must be controlled, and available flatness metrology further developed to for patterned porous low-κ wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations have developed (continue to develop) flatness tests that provide the information required for statistical process control that is useful for lithographic processing.

Interconnect specific CD measurement procedures must be further developed for control of etch processes. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capabilities of current inline CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels. Furthermore, scatterometry must be extended to contact and via structures. Electrical test structures continue to be an important means of evaluating the R-C properties of patterned low-κ films.

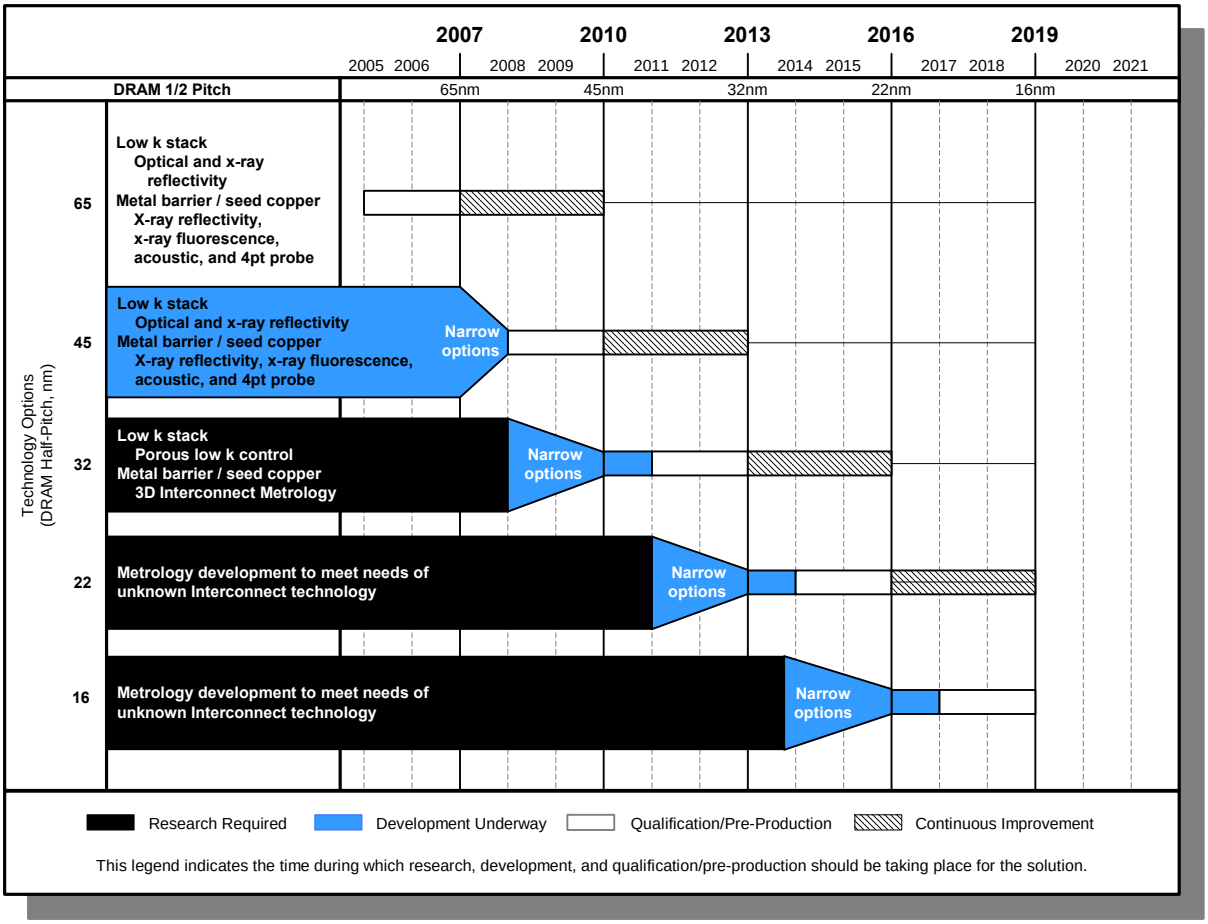


Figure 108 Interconnect Metrology Potential Solutions

MATERIALS AND CONTAMINATION CHARACTERIZATION

The rapid introduction of new materials, reduced feature size, new device structures, and low-temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility.

The declining thickness of films currently used, moving into the sub-nanometer range, creates additional difficulties to the current available optical and opto-accoustic technologies. Shorter wavelengths of light even into the X-ray range are currently investigated to overcome the challenge of inline film thickness and composition detection.

Often, offline methods provide information that inline methods cannot. For example, transmission electron microscopy (TEM) and scanning TEM (STEM), especially those capable of annular dark field (ADF) imaging, provide the highest resolution spatial or cross-sectional characterization of ultra thin films and interfacial layers. TEM/STEM methods require sample preparation methods that may relax some of the strain present in the sample before preparation. ADF-STEM systems equipped with X-ray detection and electron energy loss instrumentation have provided new information about interface chemical bonding. High-performance secondary ion mass spectrometry (SIMS), and its variant time-of-flight (TOF) SIMS, provide contamination analysis of surfaces and thin film stacks. Grazing incidence X-ray reflectivity (XRR) provides measurement of thin film thickness and density, while grazing incidence X-ray diffraction provides information about the crystalline texture of thin films. The importance of using diffuse scattering in addition to specular scattering during XRR seems to be critical to building interfacial models from XRR that can be compared to interfacial models from other methods such as TEM/STEM, SIMS, and ion backscattering. Field emission Auger electron spectroscopy (FE-AES) provides composition analysis of particulate contamination down to less than 20 nm in size. Offline characterization of

physical properties such as void content and size in porous low-κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials. Many of these tools are now available for full wafers up to 300 mm in diameter.

Continued development of TEM and STEM imaging capability is required. Several technologies are being applied to materials and process development for critical areas such as high and lowκ. Interfacial imaging has been greatly improved by the ADF detector for STEM imaging. Electron energy loss spectroscopy (EELS) can be done in an area with a diameter of approximately 0.2 nm. With this greatly improved spatial resolution, electron energy loss (ELS) characterization can be used to characterize interfacial regions such as that between high κ and silicon substrate. STEM with ADF imaging and EELS are becoming more routine in manufacturing support labs. Advances in image reconstruction software have also improved image resolution and thus interfacial imaging. Several improvements in TEM/STEM technology are now commercially available including lens aberration correction and monochromators for the electron beam. Recent breakthroughs in aberration corrected scanning TEM look very promising and reveal details such as single misplaced atoms in a junction.

Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating peaks that overlap and cannot be resolved with current generation lithium-drifted-silicon EDS detectors. Such new X-ray detectors will allow resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. Beta site systems are now being tested. These detectors can also be implemented in micro XRF systems, using either an electron beam or a micro focus X-ray beam as excitation source. Both are currently in beta phase. XPS (X-ray photon electron spectroscopy) is also currently being developed as a means to determine thickness and composition of thin (up to 50 nm) films.

A new approach to contamination control is being developed for inline measurement. Real-time sampling of wet chemical baths has been added to a mass spectrometry based detection system for measurement of trace contamination in the bath solutions.

While these and other offline characterization tools provide critical information for implementing the Roadmap, there are still many challenges. Characterization of the high-κ gate stacks to be used will be very difficult due to the length-scale for which electrical properties are determined. For example layer-to-layer chemical intermixing is easily confused with physical interface roughness, and characterization is difficult in these situations due to matrix-induced effects and overlapping signals. In addition, as the device features continue to shrink and new non-planar MOS devices are developed, the applicability of characterizing planar structures as representative of the device feature becomes more questionable. Furthermore, ongoing scaling makes the analysis of contamination in high aspect ratio structures even more difficult.

The introduction of new materials will raise new challenges in contamination analysis, such as happened with copper metallization where the very real possibility of cross contamination has led to the need to measure bulk copper contamination down to the order of 10^{10} atoms/cm^3 and surface copper contamination even in the edge exclusion and bevel regions, all because of the high diffusivity properties of this deleterious metal. Device shrinks are also tending to lower the thermal budgets allowed for processing so that the behavior of metal contamination and how to reduce its negative effects are changing the characterization needs. For example, low-temperature processing is changing which surface contamination elements, and at what levels, need to be controlled and therefore measured. A key example is the role of surface calcium on very thin gate oxide integrity, and the difficult challenge of measuring this surface element at the 10^8 atoms/cm^3 level. Traditional methods such as vapor phase decomposition ICPMS can have day-to-day limitations at this level. In addition, low-temperature processing is changing how metal contamination gettering is achieved, challenging the way to characterize material properties to ensure proper gettering.

The unexpected acceleration of the use of strained silicon without SOI has resulted in new metrology and characterization requirements earlier than predicted in the 2003 Roadmap; these are currently under evaluation and development. Gate oxide metrology becomes even more complex if strained Si channel structures are used as the starting material instead of bulk Si or SOI wafers. Strained Si is either grown on thick relaxed SiGe buffer layers on bulk Si or on compliant substrates consisting of thin SiGe layers on SOI. In both cases, the metrology of the starting material is crucial with a large number of parameters to be controlled: 1) thickness and Ge profile of the SiGe buffer, 2) thickness of the strained Si channel, 3) roughness of the Si/SiGe interface and the Si surface, 4) magnitude and local variation of stress in the Si channel, 5) threading dislocation density in the Si channel (high sensitivity of the measurement is needed, since the desirable dislocation density is very low (at $<10^3$-10^4cm^{-2})), 6) density of other defects, such as twins, dislocation pile-

ups, or misfit dislocations, particularly at the SiGe/Si channel interface, 7) distribution of dopants in channel and buffer (particularly after thermal annealing.

Transmission electron microscopy is readily available to determine thicknesses and interface/surface roughness of strained silicon on a microscopic scale. Both threading and misfit dislocations can be seen in TEM images, but TEM sensitivity to dislocations is poor because of the limited field of view. Atomic force microscopy determines the surface roughness of the Si channel. Etch pit density (EPD) measurements determine the density of threading dislocations near the surface. Clear prescriptions for EPD are needed to select the etch depth. The meaning of lines and points in the EPD optical images need to be explained. Computer-controlled data analysis of EPD images is desirable, but not feasible at the moment. X-ray topography is another technique offering promise for defect detection. The Ge and dopant profiles can easily be measured with SIMS. A high sputtering rate is needed for thick SiGe buffers, while high depth resolution (possibly with a low-energy floating ion gun) enables the analysis of the thin Si channel and of the channel/buffer interface. Optical carrier excitation using a red photodiode directed at the sputtering crater avoids SIMS charging artifacts. This is particularly important for strained Si over SOI and for undoped layers.

Unique properties associated with strained silicon are being addressed with a variety of metrology methods. Stress of the Si channel is the crucial parameter that determines the lattice strain affecting the electronic band structure to provide mobility enhancement of electrons or holes. Raman spectroscopy can measure the stress, while TEM and XRD measure strain. Measuring stress is possible using Raman spectrometry since the energy of the Si-Si vibration in the Si channel depends on stress. However, the phonon deformation potential (describing the variation of the Si-Si phonon energy with stress) is not firmly established for thin Si channels. Such Raman measurements need to be performed using a UV laser to avoid penetration of the laser into the Si substrate. At 325 nm wavelength, the entire Raman signal stems from the thin Si channel, simplifying data analysis. For longer wavelengths, the Si-Si vibration in the SiGe buffer appears complicates the signal. The energy of the Si-Si vibration in SiGe depends on alloy composition and stress, which provides additional information. Raman mapping yields the stress distribution across the wafer with a maximum resolution of about 0.5 μm, thus allowing prediction of transistor-to-transistor variations in mobility enhancement. It would be desirable to improve this resolution, possibly using solid or liquid immersion techniques. Micro- XRD is also applied to measure the stress in small structures, but currently the analysis spot is in the 5–10 micron range, making device analyzis not yet feasible. This limitation is a serious challenge for Micro XRD.

Analysis of ellipsometry data for strained Si channels is complicated, since the dielectric function of Si depends on the stress. This relationship (described by the piezo-optical or elasto-optical tensors) is qualitatively understood, but sufficiently accurate quantitative data for fitting ellipsometry data of strained Si channels is lacking to extract the Si channel thickness. When only considering the UV portion of the ellipsometry spectra, there is some hope in the capability to determine the gate oxide thickness, at least for sufficiently smooth surfaces. For rougher surfaces, there is an additional source of error, since surface roughness enters the ellipsometry analysis in a similar fashion as the native or gate oxide. For accurate gate oxide metrology, the Si surface roughness should be an order of magnitude less than the gate oxide thickness. This is satisfied for bulk Si starting materials, but may cause concerns for measurements on strained Si channels. Confinement effects in the thin Si channel are not yet an issue in the visible and UV portions of the ellipsometry spectra. In principle, ellipsometry should not only be able to determine the Si channel thickness, but also the Ge content of the SiGe buffer underneath. In practice, however, the Ge content determined from ellipsometry data is much too low, possibly due to ignoring the strain effects on the Si dielectric function. (On pseudomorphic Si/SiGe heterostructures, ellipsometry is much more successful.)

X-ray reflectivity is an attractive alternative to spectroscopic ellipsometry to determine strained Si channel thickness since the refractive index for X-rays is very close to 1 and does not depend on the stress. Indeed, for Si channel thicknesses of the order of 10–20 nm, a clear series of interference fringes (sometimes accompanied by an additional large-angle peak of unknown origin) is obtained. However, determining the Si channel thickness using commercial software fitting packages does not always yield the correct value (in comparison to TEM). Possibly, this is related to surface roughness that is more difficult to handle for X-ray reflectivity experiments than for spectroscopic ellipsometry because of the smaller wavelength. Experimental concerns about X-ray instrument reliability and alignment are similar to that described for measurements on high-κ gate dielectrics. High-resolution triple-axis X-ray diffraction has been used successfully (using lab and synchrotron X-ray sources) to determine the vertical Si lattice constant in the channel, another measure for the stress in the structures.

A number of microscopy methods are in the research and development phase. These include the point projection microscope (electron holography) and low-energy electron microscopy. Low-energy electron microscopy has been used to study surface science for several years. The application of this method to materials characterization and possibly to

inline metrology needs to be studied. A discussion of these methods is provided in the Microscopy Section of the Metrology Roadmap.

One of the five long-term difficult challenges for metrology is structural and elemental analysis at device dimensions. Fulfilling this need will require developing materials characterization methods that provide atomic maps. Local Electrode Atom Probe (LEAP) and similar methods hold promise of providing atom-by-atom maps for conductive samples. LEAP technology needs further development of the method and its application as it currently has difficulties in measuring non-conductive and complex structures with both conducting and non-conducting features. One challenge will be obtaining near 100% detection of each element during data acquisition. Electron tomography is a growing region of interest and is being pursued by both tilt-series and focal series methods in both STEM and TEM. Aberration corrected TEM is currently shows promise in this area as smaller and more intense probes and higher beam may allow increased resolution and signal to noise required for tomorgraphic analysis.

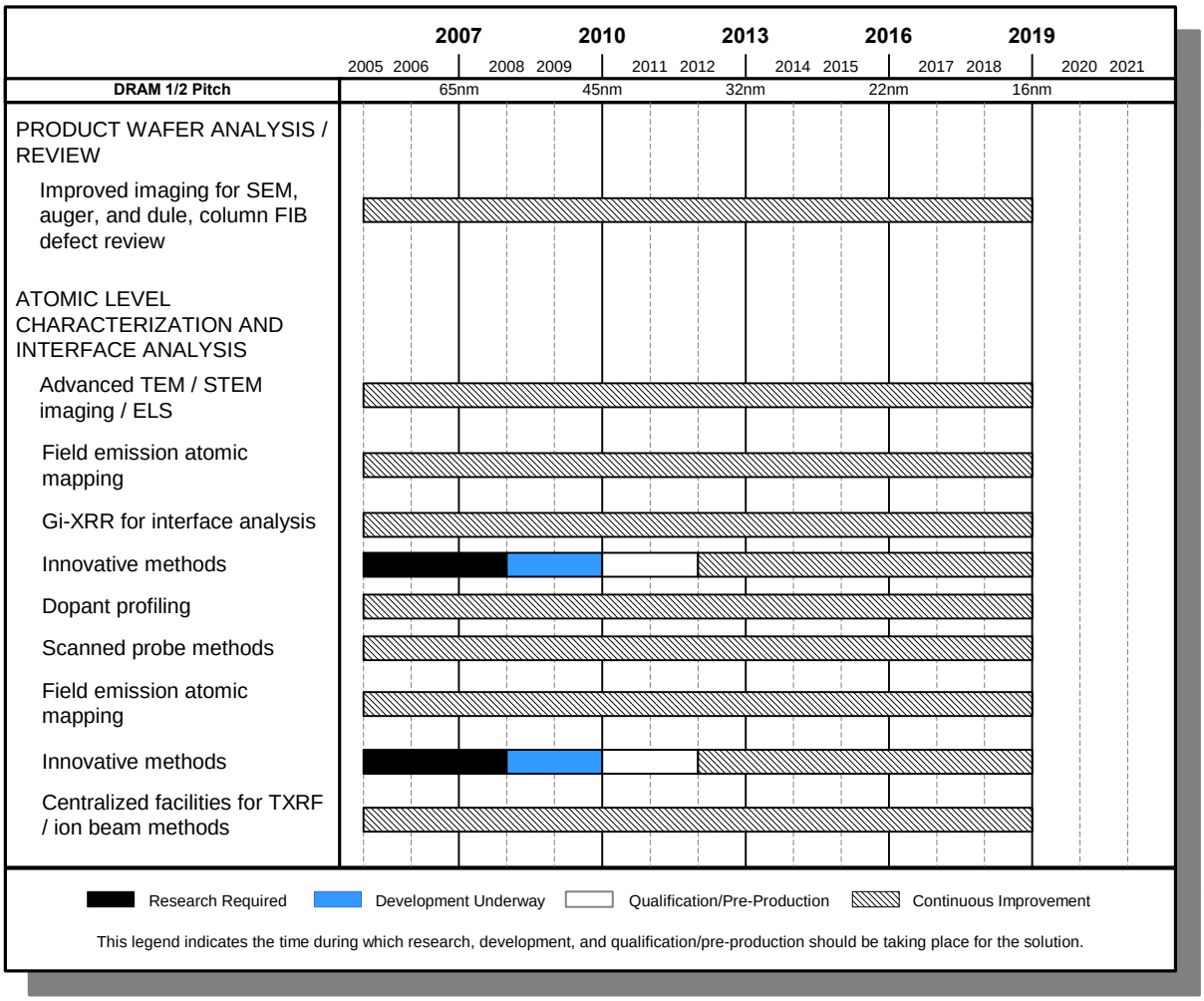


Figure 109 Materials and Contamination Potential Solutions

REFERENCE MEASUREMENT SYSTEM

A Reference Measurement System (RMS) is an instrument, or a set of several instruments, that complement each other in their ability to excel in various aspects of dimensional metrology. An RMS is well characterized using the best the science and technology of dimensional metrology can offer: applied physics, sound statistics, and proper handling of all measurement error contributions. Because an RMS has been well characterized, it is more accurate, perhaps by an order of magnitude, and more precise than any instrument in a production fab.[8] An RMS must be sufficiently stable that other

measurement systems can be related to it. An RMS can be used to track measurement discrepancies among the metrology instruments of a fab, and to control the performance and matching of production metrology instruments over time.

Due to the performance and reliability expected from this instrument, the RMS requires a significantly higher degree of care, scrutiny, and testing than other fab instruments. Through its measurements this "golden" instrument can help production and reduce costs. However, this is an instrument that, by the nature of the semiconductor process, must reside within the clean environment of the fab so that wafers measured within this instrument can be allowed back into the process stream. Wafers from any other fab can come for measurements and be returned to serve as in-house references across the company or companies.

REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties typically used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar instruments at different locations (internally or externally), or between the model and experiment. Reference materials are also extremely useful in testing and benchmarking instrumentation.

Reference materials can be obtained from a variety of sources and come in a variety of forms and grades. Depending on the source, they may be called Certified Reference Materials (CRM), Consensus Reference Materials, NIST Traceable Reference Materials (NTRM®) or Standard Reference Materials (SRM®).[2] The US National Institute of Standards and Testing (NIST) is one of the internationally accepted national authorities of measurement science in the semiconductor industry. NIST has also recognized the difficulty of keeping pace with the IC industry through the traditional method of need identification, instrumentation and technique development, and the development of SRMs. Several approaches allow the industry to supplement NIST's ability to supply reference materials. Commercial suppliers can submit potential calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark for the series of artifacts checked by NIST.[3]

Another approach is the development of consensus reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM International. The National Metrology Institutions (NMI) in different countries develop and maintain standards that might be suitable and should be consulted. There is an effort among many of the leading NMIs, including NIST, to coordinate cross comparisons of their measurements and standards to arrive at a mutual recognition sometime in the near future to avoid duplication of efforts.[4]

There are several technical requirements related to reference materials and certification, as follows:

- Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be much smaller than the desired calibration uncertainty.
- Reference materials may be difficult to manufacture with the desired attributes; frequently it is necessary to use specialized manufacturing techniques in short runs to obtain the samples to be measured and certified.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.
- The final measurement uncertainty in an industry measurement employing a reference material is a combination of uncertainty in the certified value of the reference material and additional uncertainties associated with comparing the reference material to the unknown. For this reason, the uncertainty in the reference material must be smaller than the desired uncertainty of the final measurement. An industry rule of thumb is that uncertainties in the certified value of the reference material be less than ¼ of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy (including both bias and variability) better than ¼ of the required final accuracy of the measurement for which it will be used.

[2] *NTRM® and SRM® acronyms are registered trademarks of NIST.*
[3] *Use of the NTRM mark on a subsequent series of artifacts, even of the same type, requires additional verification testing by NIST.*
[4] *Refer to The International Bureau of Weights and Measures's website http://www.bipm.org/en/convention/mra/*

- Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.
- It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process equipment development. Each type of reference material has its own set of difficult challenges, involving different combinations of the challenges described above.

INTEGRATED METROLOGY AND ADVANCED PROCESS CONTROL

Metrology plays a key role enabling productivity gains made through advanced process control (APC). The trend toward integrated metrology—from offline to inline to *in situ* techniques—enables a richer, more powerful spectrum of process control strategies. At this point, advances in APC have been driven primarily by successes in run-to-run (R2R) control and in fault detection and classification (FDC). The advances in integrated metrology and APC have been substantial though in some ways serendipitous. It is clear that: 1) APC has demonstrated major value to the industry, and has been adopted by most manufacturers; 2) APC capabilities and associated sensors and metrology to support APC are available today for key process areas such as CMP and lithography, but 3) a truly comprehensive APC manufacturing strategy is not yet reality, nor is a portfolio of sensors and metrology tools to support complete factory-wide deployment, particularly given the profound changes in materials, processes, and device structures expected for future technology generations. The benefits already realized from APC are driving the development of new sensor technologies and associated control software, which will allow factory-wide comprehensive solutions to be realized in the near future.

APC comprises two different thrusts as follows:

1) *Course correction* is aimed at adjustment of process parameters in order to compensate for systematic drift in equipment, incoming product variation, and process behavior. Here, R2R control has been the dominant driver, in which inline metrology is employed for feedback or feed-forward control, either on a wafer-to-wafer or batch-to-batch basis to maintain product quality in the presence of process variations, and also to reduce non-product wafers. Real-time control, based on *in situ* and real-time sensors for during-process course correction, generally requires further development of more process-specific sensors with sufficient metrological precision.

2) *Fault management* is directed at rapid identification and response to equipment problems. The primary driver has been fault detection and classification (FDC), in which *in situ* and real-time sensors are used to identify common equipment faults, suggest or initiate repair actions, and reduce product scrap. Additional benefit is envisioned as sensor and metrology data are combined with informatics approaches to enable more sophisticated classification of more subtle fault sources, along with fault prognosis and maintenance rescheduling consistent with overall tool and factory efficiency improvement. Building on the increasing confidence that R2R and FDC successes have provided, the challenges for these two APC components are to add real-time control to R2R control for course correction, and to expand FDC to broader fault management.

Inline metrology tools now underpin broad implementations of R2R control, involving both feedback and multi-step feed-forward univariate or multivariate control capabilities. While *in situ* real-time sensors in principle can drive run-to-run control, they have been primarily exploited for real-time fault detection, with a limited number of examples in real-time course correction (e.g., interferometric etch end-point control). The economic value of both run-to-run course correction and real-time fault detection have led to advances in equipment engineering capabilities (EEC),that is, broad integration of APC hardware, models and algorithms with factory-level information distribution, scheduling, and operations. Despite these advances, availability of comprehensive APC systems requires further R&D in sensors, control strategies, new applications, and improved user interfaces to these APC systems to reduce the barriers to understanding and acceptance of APC.

Since R2R is primarily based on inline metrology, it delivers value primarily by compensating for longer-term process and equipment drifts, using feedback information to adjust process settings for the next wafer, and/or compensating for incoming product variability (wafer-to-wafer, lot-to-lot, etc.) by using feed-forward information to adjust the subsequent process(es) experienced by the same wafer. FDC delivers value by determining the health of the tool or process through evaluation of *in situ* information (process, equipment, and wafer). This evaluation may occur in real-time, i.e., during processing, or as summary activity after processing has been completed. In the latter case, inline wafer metrology represents a driver for FDC as well as R2R control. The increased availability and standardization of R2R control and FDC and their associated interfaces will also lead to control strategies and solutions that incorporate both capabilities in a complementary fashion. R2R control and FDC will be integrated as follows: 1) at the data storage level, thereby supporting data sharing and data mining between application types; 2) at the user interface level, thereby reducing the APC learning curve and allowing APC to be represented as a single entity in the factory; 3), at the logic interaction level,

whereby control rules will allow FDC results to impact R2R control operation and vice-versa to support complementary utilization of these capabilities, and 4) eventually, at the algorithm level, where FDC and R2R models and modeling approaches would be integrated. Items 1) through 3) above will be critical to the realization of comprehensive factory-wide manufacturing strategies. The technology to support all of these items is incomplete. Other factors that will lead to factory-wide strategies include hierarchical control solutions, cascaded control between processes, and coordination of control with yield management applications. Another key APC enabler is the development of standards that define the interaction of the APC applications with each other and with outside agents, and ensure access to wafer, process and equipment data as necessary to support these applications.

APC will benefit from the move to integrated metrology. Though a significant number of benefits from R2R control can be achieved with offline metrology. For example, with lithography overlay and CD control, integrated metrology will provide benefit by the following: 1) shortening the control loop time, thereby improving control accuracy; 2) eliminating the human and associated wafer transport factors associated with non-integrated metrology; 3) allowing the metrology to be better tuned and optimized to the process; and 4) automating the matching process through recipe download to the tool and metrology. All of these factors lead to improved throughput and yield. Today integrated metrology is prevalent only in CMP (film thickness), but it is beginning to appear in etch (film thickness and CD) and lithography (CD) process types. Overlay metrology for lithography must evolve from offline (stand-alone) to inline for improved throughput and enabling of 100% sampling with minimal throughput penalty. Inline metrology, as a replacement for offline metrology, will improve throughput, reduce cycle time, allow for increased sampling (number of wafers as well as points per wafer), and reduce control feed forward and feedback lag times.

Difficult challenges must be overcome before integrated metrology is accepted on a large scale. These challenges are in the areas of: 1) performance and cost for integrated metrology, which should be comparable to those for stand-alone metrology; 2) impact on tool throughput (which should approach zero); 3), integration; 4) data management; 5) setup (including calibration and training) and configuration time; 6) difficulty and cost of maintenance and its impact on tool up-time, and 7) the understanding that the level of accuracy of integrated metrology is a function of the integration and control environment (unlike stand-alone metrology), and accuracy equivalence with stand-alone metrology may not be required to deliver significant benefit.

To the extent that real-time, *in situ* sensors can be made sufficiently quantitative and precise, they will add the capability for real-time course correction that compensates for short-term, random process variability. In turn, this will enable a true real-time APC, in which *in situ* sensors with real-time response drive both course correction and fault detection. The availability of real-time course correction will stimulate a new APC hierarchy, in which real-time course correction and fault detection operate at the tool (unit process) level much as regulatory control of equipment has long been practiced. Real-time course correction will tighten unit process variability as seen by inline metrology, but benefit from run-to-run control will remain. This scenario suggests that a new control hierarchy should be developed which optimizes algorithms and responsibilities within the overall APC strategy, and which delivers metrology information upward in the hierarchy (e.g., *in situ* sensor data may enhance run-to-run control).

In situ sensor technology remains far from complete. A reasonable group of sensors based on optical, chemical, and electrical signals from processes are available, but their development and demonstration as sufficiently quantitative metrology techniques for course correction has been limited. Note that the course correction demands substantially higher quantitative accuracy at this point than does fault management. *In situ* sensors that measure across-wafer uniformity and vertical profile are particularly needed, and if possible these should be accompanied by equipment designs that enable real-time control actions that directly compensate for nonuniformities.

While *in situ*, real-time sensors are broadly deployed for detection and response to key equipment failure modes, *in situ* sensor and inline metrology have yet to be broadly coordinated and integrated to enable causal identification of more subtle failure modes and optimized maintenance/repair scheduling (such as fault classification and prognosis). This is an important challenge given the economic consequences of downtime for preventive or emergency equipment maintenance.

In situ sensors face additional challenges in the wealth of complex materials, processes, and device structures anticipated for future technology generations. Measuring the composition, thickness, and uniformity of ultrathin gate dielectrics or metallic barrier layers presents a significant challenge, even with the adoption of atomic layer deposition (ALD). ALD chemistries, as well as materials, are complex, and their advantages must be compromised with the demands of manufacturing throughput. Nanoporous low-κ materials, and particularly their interfaces with barrier layers, present an equal challenge for *in situ* sensors. *In situ* chemical identification is increasingly critical where surface chemistry plays a key role in product quality (for example, in high-κ gate dielectrics, electroplating additives, CMP, and low-κ dielectrics).

A key factor that will dictate not only the capability, but also acceptance, of all forms of APC and integrated metrology is *data quality*. Poor data quality can cause an APC system to reduce process performance rather than improve it. A prerequisite to APC deployment is thus acceptable levels of data quality provided by the tool, metrology, and sensors. Data quality issues include availability, timeliness (of data capture and delivery), accuracy, resolution, freshness, and contextual richness (including time stamping). APC systems will benefit from the quantification of data quality by identifying minimum data quality required for effective APC deployment. Thus the roadmap must establish minimum data quality requirements for each application and technology generation to support effective APC. A link is provided to show *key sensor technology requirements*.

METROLOGY FOR EMERGING RESEARCH MATERIALS AND DEVICES

This section covers the materials and device characterization and inline measurement needs for emerging materials and devices. (Refer to the Emerging Research Devices chapter)

3D ATOMIC IMAGING AND SPECTROSCOPY

Aberration Corrected TEM and STEM w/ELS

Aberration corrected lens technology has revolutionized transmission and scanning transmission electron microscopy. Commercially available TEM and STEM systems have demonstrated sub 0.1 nm resolution and electron energy loss spectra have located atoms in an atomic column. STEM systems are approaching 3D atomic resolution through the confocal nature of the images. This technology has already been applied to nanotechnology. Aberration-corrected high resolution TEM images of nanowires have resolved the atoms in gold nanodot catalysts and the epitaxial relationship between the nanodot and the silicon nanowires. Some of the achievements of aberration corrected electron microscopy of nanotechnology include:

- Observation of Hf atoms in the interface between high-κ gate dielectrics and the silicon substrate
- ELS spectra of a single Sr atom in an atomic column of $CaTiO_3$
- Imaging both K and I atoms of a KI crystal inside a carbon nanotube
- Observation of the movement of atoms in nanodots
- Observation of the relationship between the gold atoms in the nanodot gold catalyst and a silicon nanowire.

Achieving the full potential of aberration correction and its associated advances such as energy filters for the electron source and higher energy resolution/electron energy loss *requires advances in image and spectral modeling*. Multi-slice simulations are already being modified for nanowire and other applications. These first simulations indicate that the observation of twinning defects in nanowires requires use of multiple angles of observation. The impact of nano-dimensions on electron diffraction patterns is also interesting.

Microscopy of carbon containing samples needs to move beyond just carbon nanotubes. Despite all the above-mentioned advances, microscopy of soft matter remains exceedingly difficult. As the current density increases, bonds are more readily broken in molecular samples. Higher energy resolution for ELS is critical to understanding molecular samples.

Local Electrode Atom Probe

LEAP is an advanced version of field ionization. An electrode is placed in close proximity to a small cone-shaped sample. The electric field between the sample and the local electrode ionizes atoms from the sample that are collected on a two-dimensional, position sensitive detector. The original atomic position is determined from geometric considerations and the atomic mass from time of flight. Because the electrode is closer to the sample a smaller voltage can be used to produce the same filed strength as in field ionization. This allows the field to be pulsed at a considerably higher rate, and counting as many a million atoms is now possible. The local electrode is the key break through that allows for the higher counting rates. It is important to note the need for conducting samples. LEAP brings us closer to the dream of atomic mapping in three dimensions. Because detection efficiency is approximately 60%, atomic maps are not yet capable of achieving this dream.

OTHER MICROSCOPY NEEDS

Assumption—there is a need for characterizing the structure and local properties of current CMOS devices as they scale down in size, as well as for anticipating the metrology requirements of post CMOS device technologies.

Probes of Local Properties with High Spatial Resolution: Opportunities

Scanning Probe Microscopy (SPM) is a platform upon which a variety of local structure/property tools have been developed with spatial resolution spanning 50-0.1 nm Scanning Capacitance Microscopy, Spreading Resistance Microscopy and Conductive Tip Atomic Force Microscopy have been optimized for dopant concentration profile measurement with spatial resolution dependent on dopant concentration. Recent developments in SPM involving frequency dependent signals on the sample and tip, and simultaneous perturbation with more than one frequency and/or probe expand the range and resolution of measurements.

Local Measurements Related to Charge and Transport—In situ measurement during device operation or implementation of frequency dependent measurements is enabled with multiple contacts to the sample. A family of frequency dependent measurements, Scanning Impedance Microscopy, Nano Impedance Spectroscopy, span 8 orders of magnitude in frequency to quantify interface and defect properties, including charge trapping. Individual defects in molecular nanowires can be detected with these tools, as well as contact potential at local scales.

Scanning Surface Potential Microscopy (also called Kelvin Force Microscopy), related to work function, can easily map materials variations at 10s nm scale and can be exploited to characterize FET and interconnect structures. At higher energy resolution surface potential variations that occur on high k dielectric films before metal deposition can be characterized providing insight on interface properties after metallization. There is recent evidence that the spatial resolution of this technique can be extended to atomic scales.

Recent observations with SPM and quantum dots demonstrated that single electron detection is possible. While single electron detection is necessarily a low temperature, it implies the potential for increased energy resolution for localized measurements.

Local Measurements Related to Spin—A scanning probe related tool, Magnetic Resonance Force Microscopy, has recently demonstrated that single spins can be detected with magnetic probes. Further development will determine limitations on spatial resolution and the potential to study spin polarization and characterize spin based devices.

At lower sensitivity Magnetic Force Microscopy can be used to map current flow through devices. To be generally useful the limits of field detection and development of magnetic tips is required.

Complex Properties—Future generations devices involving a wider materials set, perhaps including organic and biomolecular constituents require additional property measurements. Utilizing high frequencies in various detection configurations yields local dielectric constant, electrostriction, piezo electric coefficient, switching dynamics, etc. These measurements are critical in the development of capacitor based memory and for hybrid device structures, as well as dielectric characterization.

Multiple Modulation and Combined Probes—The combination of multiple measurements is sometimes necessary to isolate properties and is sometimes useful to maximize information. For example electrostatic interactions that occur during magnetic force measurements and can be incapacitating. By measuring surface potential at high frequency, nulling it, and measuring magnetic forces at low frequency, the interactions are separated and quantified. This approach can be applied to produce generalized metrology tools.

Probes of Local Properties with High Spatial Resolution: Challenges

The challenges to implementing these tools on increasingly miniaturized devices and complex materials sets in an industrial environment are similar.

General Accessibility—The time from development in the lab to commercialization results in a large gap between capability and accessibility. This is particularly critical now that device research is encompassing new materials for high k dielectrics, exploring information storage options and looking toward post CMOS technologies. For some companies the design time line is on the order of 6 years. Other mechanisms of accessibility are necessary meet roadmap requirements.

Increased resolution—In all cases a trend toward higher spatial resolution is desirable. For some SPM tools fundamental principles will limit ultimate resolution. Other tools are so new, that limits have not been examined. Recent results in SSPM and work function spectroscopy suggest that atomic scale resolution is possible for some of the complex property probes. If so, new physics will emerge and theory will be required to interpret the output.

There is a potential to increase the energy resolution of most of the measurements, as demonstrated by inelastic tunneling and single electron detection. The maximum energy resolution will be achieved at low temperature, which is a trade off with convenience.

Tip Technology—Commercial vendors have developed a large toolbox of specialized SPM cantilevers and tips. Reproducibility is often an issue; in some cases yields of good tips are on the order of 30%. More important is the gap between commercially available cantilevers/tips and those required for tool development. This becomes more difficult as the tips envisioned for tool development involve embedded circuitry and complex tip geometries.

Calibration Standards—The lack of calibration standards for nm sized physical structures is a significant problem. At high spatial resolution under specialized circumstances, atomic structure can be used. Carbon nanotubes have been suggested as a general alternative and demonstrated for electrostatic property calibration as well. Standard calibration processes should be developed.

OPTICAL PROPERTIES OF NANOMATERIALS

The optical properties of crystalline materials, especially semiconductors, are modified by quantum confinement and surface states. The fundamental expression of the optical response of a material is its dielectric function. The imaginary part of the dielectric function is directly related to the absorption of light. In direct or indirect band gap materials, the optical response is characterized by critical points where electrons are excited from the top of a valence band to the conduction band. The discussion of Jellison about critical points in bulk silicon is useful in describing the impact of nano-dimensions.[9] In bulk crystalline silicon, the amount of light absorption at a particular wavelength is a result of the band structure. The probability of absorption is a function of the symmetry of the wavefunctions of the states in the valence band and the conduction band, and on the joint density of states. As noted by Jellison, high probabilities of absorption exist where there are large regions in **k**-space (k space is momentum space and is and the wavevector k is defined along specific directions in a crystal) where the energy separation E is nearly constant.[11] The critical points in the dielectric function are defined as these (constant energy separation) regions of **k**-space that result in large joint density of states and are referred to as critical points in the Brillouin zone. Features in the visible and near ultraviolet optical spectra of materials are often a result of critical points in the Brillouin zone. In silicon, the E_o' critical point; is the smallest energy for a direct transition with an energy of ~3.4 eV. This is called the direct band gap. Other critical points in silicon include the feature seen in the optical spectrum at ~4.25 eV (~292nm) called the E_2 critical point.

The symmetry of a bulk sample results in both the band structure and the joint density of states. Quantum confinement in one, two, or three dimensions changes the energy of the critical points and the joint density of states. Thus, the shape of imaginary part of the dielectric function of nano-sized materials is altered by the change in the joint density of states and the appearance of new critical points due to the confinement. One interesting example is the emergence of strong anisotropy in silicon nanaowires less than 2.2 nm in diameter and the appearance of new low energy absorption peaks for light polarizations along the wire axis.[10]

ELECTRICAL CHARACTERIZATION FOR EMERGING MATERIALS AND DEVICES

Many emerging nanoelectronic devices exhibit non-conventional behavior such as negative differential resistance [11] and hysteretic switching.[12, 13] New electrical measurement methodologies and analyses will be required to characterize the behavior of these new emerging materials and devices. Certain traditional parameters, such as mobility, are much more challenging to extract at the nanoscale.[14] It is important to determine what parameters are determining final device performance for a given emerging device technology. In addition, the behavior of some categories of emerging devices are based upon completely different mechanisms than those in traditional CMOS. For example certain devices have intrinsically quantum mechanical behavior, while others do not utilize charge transport to change the computational state, but rely upon other mechanisms such as magnetic flux changes. Salient device parameters and their extraction methods will need to be defined for such new devices that switch by different physical principals than standard MOSFET structures. Methodologies will need to be established for characterizing the stability and reliability of new device structures and circuit architectures.

In addition to advances in electrical test methodologies, viable test structures are critically needed to reliably and repeatably interface nm-sized elements (such as individual molecules and nm-sized semiconductor quantum dots) with larger electrodes and leads that can be electrically contacted by probes or wire bonds. Methods to contact sub-lithographic components of emerging nanoelectronic devices are perhaps the greatest challenge for the electrical characterization of emerging materials and devices. Furthermore, parametric test structures need to be developed that interrogate the interface

between metal interconnect and the active region of nano-scale devices, especially those fabricated with organic materials. Parameters such as work function, barrier height, and transport process need to be investigated and defined for metal interconnect systems for devices fabricated with unconventional materials.

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