INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

SCOPE

Radio frequency and analog/mixed-signal (RF and AMS) technologies now represent essential and critical technologies for the success of many semiconductor products. Such technologies serve the rapidly growing wireless communications market. They depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe and others of which are not compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table.

Recognizing wireless applications, which are enabled by RF and AMS technologies, as a new system driver for the ITRS, the International Roadmap Committee (IRC) requested in 2003 that III-V compound semiconductor devices be included in the roadmap. This IRC request also included addressing semiconductor market requirements that are likely to be met by products from CMOS compatible processing and those that are likely to be met by products from processing that is not compatible with CMOS processing.

The purposes of this 2005 ITRS RF and AMS Chapter are as follows:

1. Present the challenges that RF and AMS technologies have in meeting the demands of wireless applications for cellular phones, wireless local area networks, wireless personal area networks (PAN), phased array RF systems, and other emerging wireless communication, radar, and imaging applications operating between 0.8 GHz and 100 GHz.
2. Address the intersection of Si complementary oxide semiconductor (CMOS), bipolar CMOS (BiCMOS), and SiGe heterojunction bipolar transistors (HBTs) with III-V compound semiconductor devices.

The 2003 RF and AMS roadmap had four sections on AMS, RF Transceivers, and Power Amplifiers (PAs) for 0.8 GHz to 10 GHz applications and Millimeter-Wave (mm-Wave) for 10 GHz to 100 GHz applications. This 2005 RF and AMS Chapter has been restructured to provide more consistent requirements of the basic technology elements (CMOS, bipolar devices, and passives) used in wireless communication front-end circuits and to maintain the original 2003 applications driven roadmap. This 2005 RF and AMS Chapter has five main sections. The four sections on RF and AMS CMOS, RF and AMS Bipolar Devices, Passives for RF and Analog, and Power Amplifiers cover the 0.8 GHz to 10 GHz applications and one section on mm-Wave covers the 10 GHz to 100 GHz applications. These frequencies refer to the nominal carrier frequencies for communications and are not necessarily the clock or operating frequencies of the individual devices and circuits. Even though the mm-wave spectrum is considered to start at 30 GHz, this section has been extended down to 10 GHz because the challenges, technical requirements, and technologies for the 10 GHz to 30 GHz spectrum are similar to those for the 30 GHz to 100 GHz spectrum.

In addition to the five sections mentioned above, this chapter will also discuss the increasing significance of signal isolation. As wireless communications systems migrate to support more multi-mode, multi-in/multi-out radio functions, maintaining signal isolation among radio functions and digital baseband functions becomes a very demanding and critical challenge. However, unlike for the other technologies in this chapter, there are at present no clear definitions and figures of merit for signal isolation performance. Consequently, there are no technology requirement tables for signal isolation. This 2005 Chapter will attempt to highlight the importance and the need for more attention to the challenges of signal isolation.

Today, group IV semiconductors (Si and SiGe) dominate below 10 GHz and III-V compound semiconductors dominate above 10 GHz. The range in frequencies where competition amongst elemental and compound semiconductors changes with time and is expected to move to higher frequencies. Nevertheless, while SiGe has shown capability in mm-wave range, it is unlikely to replace III-Vs in applications where either high power gain or ultra low noise is required.

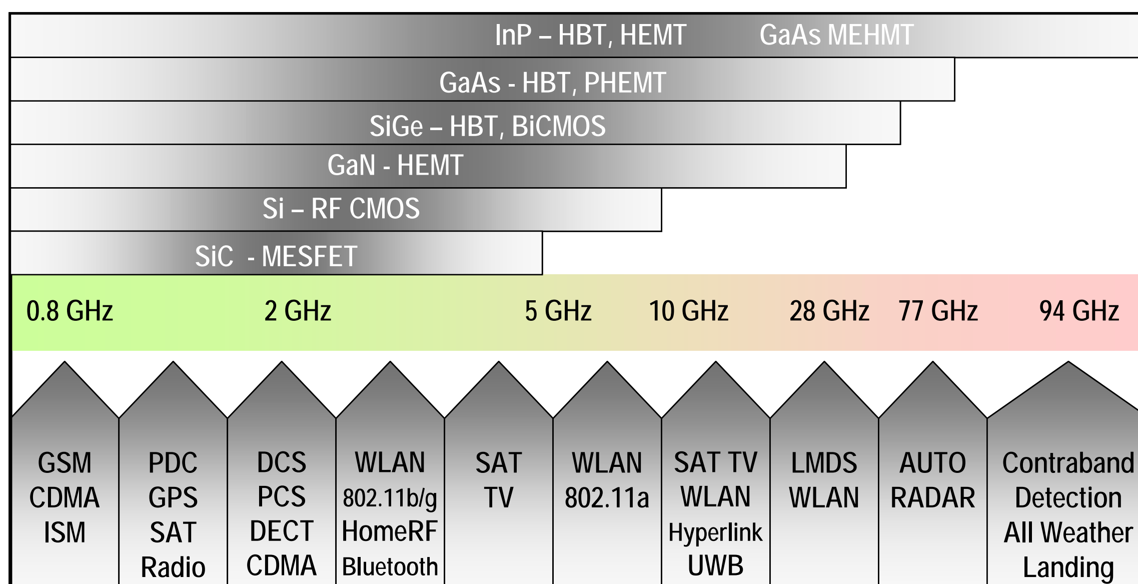

Figure 44 Application Spectrum[1]

Figure 44 schematically presents the scope of this chapter in terms of the interplay among commercial wireless communication applications, available spectrum, and the kinds of elemental and compound semiconductors likely to be used. The consumer portions of wireless communications markets are very sensitive to cost. As a result, developing RF and AMS technology roadmaps on such applications is not straightforward. Cost is one of the key factors determining the choice of technologies among the kinds of RF semiconductor and device technologies shown in the top part of Figure 44. These boundaries are not as well defined as Figure 44 may suggest, but are broad, diffuse, and change with time. The boundary between the group IV semiconductors Si and SiGe and the III-V semiconductor GaAs has been moving to higher frequencies with time and for other applications the boundary between GaAs and InP is tending to shift to lower frequencies. And eventually, metamorphic high electron mobility transistors (MHEMTs) may displace both GaAs pseudomorphic high electron mobility transistors (PHEMTs) and InP high electron mobility transistors (HEMTs) for certain applications. As an example, SiGe HBT technology is already today very promising for 77 GHz automotive radar applications. The wide bandgap semiconductors such as SiC and GaN will be used for infrastructure such as base stations at frequencies typically above about 2 GHz. Increased interests for the 94 GHz band arises from its applications for all weather landing and other security needs. III-V compound semiconductors have additional metrics than those usually associated with CMOS processes. These other metrics include carrier frequency for wireless applications and the printed gate length.

In future years, it is expected that the frequency axis in Figure 44 will lose its significance in defining the boundaries among technologies for some of the applications listed therein. This expectation occurs because most of the technologies in Figure 44 can provide very high operating frequencies. The future boundaries will be dominated more by such parameters as noise figure, output power, power added efficiency, and linearity. Performance tends to increase in the following order: Si CMOS, SiGe, GaAs, and InP. Two or more technologies may coexist with one another for certain applications such as cellular transceivers, modules for terminal PAs, and mm-wave receivers. Today, BiCMOS in cellular transceivers has the biggest share in terms of volume compared to CMOS. But, the opposite may occur in the future as evident by the expanding wireless local area network (WLAN) connectivity market that is dominated by CMOS transceivers. Today, both GaAs HBT and discrete laterally diffused metal oxide semiconductor (LDMOS) devices in modules for terminal power amplifiers have big market shares compared to GaAs PHEMTs and GaAs metal semiconductor field effect transistors (MESFETs) but these may be displaced by SiC and GaN as these technologies mature. In the future, silicon-based technologies having higher integration capabilities will gain importance as systems require higher degrees of functionality. Today we see GaAs PHEMTs and InP HEMTs in mm-wave receivers. In the future, we may see competition from SiGe HBTs, GaAs MHEMTs, and GaN HEMTs.

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[1] *Adapted from Figure 1 in Microwave Journal of the paper by D. Barlas, et. al., page 22, June 1999 and printed with permission from the Editor, Microwave Journal.*

The drivers for wireless communications systems are cost, frequency bands, power consumption, functionality, size of mobile units, very high volumes of product, and standards and protocols. Also, RF technologies often require additional headroom with respect to performance because several conflicting or competing requirements have to be met simultaneously. These include power added efficiency (PAE), high output power, low current, and low voltage. Increased RF performance for silicon is usually achieved by geometrical scaling. Increased RF performance for III-V compound semiconductors is achieved by optimizing carrier transport properties through materials and bandgap engineering. During the last two decades, technologies based on III-V compounds have established new business opportunities for wireless communications systems. When high volumes of product are expected, silicon and more recently silicon-germanium replace the III-Vs in those markets for which these group IVs can deliver appropriate performance at low cost.

In addition to the foregoing technical drivers, other wireless communication industries' drivers exist for RF and AMS technologies. They include the following: 1) regulations from various governments that determine the frequency availability and 2) standards and protocols that determine transmit power, frequency channels and their bandwidths and that also impact overall system performance. Situations may occur where national or regional standards and protocols influence international technical competition. While beyond the scope of this section, they are mentioned to provide another perspective on the broader context in which to view RF and AMS technologies. Such drivers often affect advances in RF and AMS technologies much more than they affect advances in many of the other technologies described in this 2005 ITRS.

The wireless communication circuits considered as application drivers for this roadmap may be classified into AMS circuits (including analog-to digital and digital-to analog converters), RF transceiver circuits (including low noise amplifiers (LNAs), frequency synthesizers, voltage controlled oscillators, driver amplifiers and filters) and PAs.

ISOLATION

The scope of this section covers signal isolation on chip and in package. Signal isolation is a particular issue for scaled technologies and increased complexity in integration level for wireless ICs. The difficulty and cost of isolation for integrating analog and high-performance digital functions on a chip are expected to increase with scaling. Further, integrating various high-performance, high-precision, and power-efficient analog functions on the same chip or in the same package presents challenges for current and future wireless communication systems. Signal isolation may become the most difficult obstacle preventing full system-on-chip (SOC) implementation because of the exceedingly high RF voltage created by the power amplifier and the power management circuits and the numerous frequencies generated internally by the intermediate frequency (IF) blocks. Even for system-in-package (SIP) implementation, signal isolation must be carefully managed to prevent performance degradation as the wireless communication schemes become more complicated. At the moment, it is difficult to agree on appropriate metrics for assessing the progress of signal isolation in the context of this RF and AMS roadmap. Thus, this chapter does not contain tables on technology requirements and potential solutions for signal isolation. Perhaps, such tables will appear in the 2007 ITRS

RF AND AMS CMOS (0.8 GHZ–10 GHZ)

The scope of this section includes RF and analog characteristics of CMOS devices in the Low Standby Power (LSTP) Roadmap and higher voltage devices that are required for precision analog applications or for driving RF signals off-chip. The LSTP Roadmap was selected as the basis for this section of the RF and AMS Roadmap because portable applications require low standby power and higher bias voltages than conventional CMOS. The devices in this roadmap are identical to those in the LSTP roadmap, but they are placed into production one year later. These devices are in circuits for transceivers, frequency synthesizers, and LNAs. Although analog speed is mainly driven by RF, there are certain analog-specific needs for analog precision MOS. This section also includes discussions on analog precision MOS device scaling, but with relatively high voltages to achieve high signal-to-noise ratios and low signal distortion.

RF AND AMS BIPOLAR DEVICES (0.8 GHZ–10 GHZ)

The scope of this section includes bipolar devices in wireless applications at moderate frequencies (< 10 GHz) and moderate power levels (< 0.5 W). This includes bipolar devices in the LNAs, transceivers, drivers and some integrated low power amplifier applications, but does not include devices used exclusively for mm-wave applications that are covered in the mm-Wave Section or used exclusively for high-power applications that are covered in the Power Amplifier section.

Key driving forces included in the current bipolar roadmap include speed, power consumption, noise, and breakdown voltage. Other important considerations not addressed in the current roadmap include cost and linearity as these are more

complex functions of not only the device technology but also the architecture and other system level trade-offs that go beyond the scope of this section.

PASSIVES FOR RF AND ANALOG (0.8 GHZ–10 GHZ)

The scope of this section includes passive components used in RF and AMS circuits for wireless communications: 1) capacitors, 2) resistors, 3) inductors, 4) varactors, and 5) passives for power amplifiers. Unlike digital CMOS circuits, the performance of many RF and AMS circuits are mainly determined by the performance of passive elements. Voltage and temperature coefficients are key parameters for capacitors and resistors. Also, capacitors and resistors are used in AMS circuits such as analog-to-digital and digital-to-analog converters that have clock frequencies below 0.8 GHz.

POWER AMPLIFIERS (0.8 GHZ–10 GHZ)

The scope of this section includes: III-V HBTs, III-V PHEMTs, Si metal oxide semiconductor field effect transistors (MOSFETs) and SiGe HBTs for terminal PAs. High voltage devices in base station power amplifiers, such as Si laterally diffused MOS (LDMOS), GaAs FET, SiC FET and GaN FET, are also described in this Section. The key driving forces are integration of components and cost.

Wireless communications require both portable and fixed transmitters and receivers to form a connected network. The public is most familiar with portable devices that take the form of cellular telephones and wireless PDAs, but these portable devices have to interface with the wire-line telephone network. It is the cellular base station that provides this connection. The base station transmitter provides the outgoing data link to the cellular telephone. Relatively high RF power (600 W) is required to achieve the desired cellular phone coverage. A single base station may contain ten's of these 600 W transmitters to handle all of the cellular phone traffic at a particular base station site. The heart of these transmitters is the RF semiconductor power device that must provide the final amplification to the data signal in order to achieve the desired output power. Typically, several semiconductor devices are connected in parallel to achieve these high powers. Silicon LDMOS transistors are now the technology of choice for cellular systems at 900 MHz and at 1900 MHz because of their technological maturity and low cost. Gallium arsenide RF power transistors are also used at these frequencies and will be used more as wireless infrastructure frequencies move up to the 3500 MHz range. Gallium arsenide devices are more expensive, but offer higher efficiency and higher power density than silicon LDMOS. The higher power density is important because it reduces the complexity of the RF matching networks required to efficiently connect the power transistor to the other parts of the transmitter circuitry. A less complex matching network has lower loss. Gallium nitride is another technology coming over the technological horizon and offers even bigger improvements over gallium arsenide. Gallium nitride has power densities four times larger than silicon LDMOS or gallium arsenide. This tremendous increase in power density is the result of GaN’s higher breakdown voltage and the higher current density.

MILLIMETER WAVE (10 GHZ–100 GHZ)

The scope of this section includes both low noise and power transistors that are based on several competing technologies: GaAs MESFET, GaAs PHEMT, InP HEMT, GaAs MHEMT, GaN HEMT, InP HBT and SiGe HBT. Today, compound semiconductors dominate the 10–100 GHz range. The device types most commonly used for analog mm-wave applications are HEMT, PHEMT, and MHEMT while the device types most commonly used for mixed-signal and high-speed applications are predominately MESFET and HBT. Except for MESFETs and SiGe HBTs, all device types employ epitaxial layer stacks that are composed of ternary or quaternary compounds derived from column III and V of the periodic chart. There is great diversity in the nature and performance of these devices because device properties are critically dependent on the selection of materials, thickness, and doping in the stack, which are proprietary to the manufacturer. Trade-offs among power, efficiency, breakdown, noise figure (NF), linearity, and other performance parameters abound. One consequence of these trade-offs is that the “lithography roadmap” is not the primary driver for mm-wave performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit, such as maximum transit frequency (F_t) and maximum frequency of oscillation (F_{max}). Performance trends are driven primarily by a combination of desirable trade-offs and “bandgap engineering” of the epitaxial layer stack in concert with shrinking lithography. Thus, the focus for the mm-wave tables in this Section is on the major performance metrics for near-term emerging markets—noise figure, power, efficiency, breakdown, and, to a lesser extent, lithography dimensions. Because III-V technologies are rapidly changing, the long-term projections for tables on III-Vs in the 2005 ITRS are not included. Compound semiconductors do not enjoy the long-term heritage of silicon-based devices, nor do they follow Moore’s Law. Amongst the four sections, this section has the greatest diversity in combinations of materials, device types, applications, and performance.

As mentioned earlier, the spectrum between 10 and 40 GHz will see increasing competition from silicon-based technologies such as RF CMOS and SiGe. MESFETs may still be used in legacy applications through the current decade but it is unlikely that any new designs will be produced in MESFET technology. GaN technology is rapidly advancing. As its materials technology matures and reliability is proven, GaN technology will find applications in the lower end of the spectrum for power amplifiers and high dynamic range LNAs.

DIFFICULT CHALLENGES

ISOLATION

Signal isolation, especially between the digital and analog regions of the chip, is a particular challenge for scaled technologies and for increased integration complexity. Noise coupling may occur through the power supply, ground, and shared substrate. The difficulty of integrating analog and high-performance digital functions on a chip increases with scaling in both device geometry and supply voltage. Signal isolation is critical for success in co-integrating high performance analog circuits and highly complex digital signal processing (DSP) functions on the same die or substrate. Such co-integration is required in many modern communication systems to reduce size, power, and cost.

The signal isolation specifications necessary for the system integration of cellular chipsets represent a very significant challenge to both technologists and EDA tool providers. The on-chip signal isolation is influenced by power planning, substrate choice, and package parasitics and involves many areas in technology, circuit design, packaging and assembling, and system integration. Signal isolation may become the most difficult obstacle preventing full SOC implementation due to the exceedingly high RF voltage created by the PA and the power management circuits and due to the numerous frequencies generated internally by the intermediate frequency blocks. The challenge of signal isolation is made even greater because a consensus does not exist on which parameters are the most appropriate ones to measure and because measuring and characterizing isolation and computer simulations for predicting isolation parameters are not mature enough to support efficiently the deployment of signal isolation technology.

Electronic design and automation (EDA) software tools are not equipped today to handle the integration of the four distinct wireless system building blocks—1) analog and mixed-signal (including certain digital functions), 2) transceiver, 3) power amplifier, and 4) power management. EDA tools are beyond the scope of this chapter. They are discussed in the *Design Chapter*. EDA tools for 1) integrating digital and RF design techniques, 2) easier interfacing and importing into the layout environment, and 3) integrating thermal analysis and modeling tools are especially critical because of greater performance requirements placed on PAs as integration densities increase and more demands to reduce the time-to-market for new products. In addition, the need for fast and accurate 3D electromagnetic and RF simulation is growing due to the increased use of multi-layer module boards for SIP solutions and the increased interest in mm-wave applications like automotive radar.

RF AND AMS CMOS

The steady improvement in the digital performance of the basic devices in the LSTP Roadmap derived from scaling will also result in continuous improvement in RF and analog performance. However, the requirement of low standby power for digital circuits limits the rate of reduction in gate oxide thickness relative to gate length and, for conventional device structures, drives ever increasing doping concentration in the device channel. These trends degrade voltage gain and increase the threshold mismatch between adjacent devices. The introduction of new materials such as high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes makes predicting trends uncertain for threshold and current mismatch and for 1/f noise. In addition, integration of passive elements such as varactors and resistors will require new techniques. Eventually, fundamental changes in device structures such as the introduction of dual-gate, fully-depleted silicon-on-insulator (SOI) will be required to sustain continued performance and density improvement. The fully-depleted SOI structure prohibits a contact to the device body. Thus, the electrical characteristics of these devices are fundamentally different than that of conventional CMOS. These differences include benefits for circuit designers as well as obstacles to be overcome. Potential benefits include higher voltage-gain and lower coupling between the drain and body. Furthermore, SOI device behavior degrades at high bias due to accumulation of channel charge due to avalanche current. Thus, the fabrication of conventional precision analog and RF driver devices and resistors and varactors may require separate process steps with the attendant increase in die cost. Finally, the steady reduction in analog supply voltage poses a significant circuit design challenge.

RF AND AMS BIPOLAR DEVICES

Near-term challenges for BiCMOS technology include reducing the cost of BiCMOS technology while improving power and the increased difficulty with integrating bipolar devices in aggressively scaled CMOS due to conflicting thermal budget requirements. The major long-term challenge for BiCMOS technology includes enabling the scaling of bipolar power supply to reduce power consumption versus CMOS technology.

PASSIVES

Passive components include resistors, capacitors, inductors, varactors, transformers, and transmission lines. They are frequently used for impedance matching, resonance circuits, filters, and bias circuits in radio frequency integrated circuits (RFICs), such as LNAs, voltage controlled oscillators (VCOs), mixers, and PAs. Even in some RF circuits, the performance of RF CMOS transistors is usually good enough for most of the applications below 10 GHz. Therefore, the RF performance of passive devices always plays a key role in determining the overall characteristics of the entire circuit. For instance, integrating VCOs into RF transceivers with standard CMOS technologies is usually the most challenging, because there are many critical parameters that must be considered. Examples of such critical parameters are large frequency tuning range, low power consumption, and low phase noise. All these parameters are primarily determined by the passives in the inductor-capacitor-tank (LC-tank) circuits of VCOs (see also the AMS Section in the *System Drivers Chapter*).

Integrating passives into RF chips is progressing in this era of SOC in order to realize low-cost RF CMOS technology, especially for some consumer electronics. When incorporating passives into a standard CMOS process, there are some additional photolithography and processing steps. Moreover, new materials may be required. Therefore, there are always tradeoffs between processing cost and device performance. Nevertheless, this is quite a complex and application-dependent topic, because capacitors and inductors usually occupy much more Si area than active devices. Consequently, another optimization scheme should be implementing extra process steps or adding process complexity to increase the unit capacitance for smaller die size. Long-term challenges for passive elements will include the need to integrate new materials in a cost-effective manner to realize high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap.

POWER AMPLIFIERS

In 2005, the bulk of the consumer market for power amplifier technologies continues to be RFICs and modules for cellular subscriber handsets. Handset sales are expected to easily exceed 700 million units per year in 2005. WLAN and Bluetooth SOC applications have quickly become another significant driver of integrated PA modules, with volumes expected to exceed tens of millions of units in 2005. These applications, which typically have very strict performance specifications, are extremely sensitive to price/performance trade-offs. This trade-off continuously drives the industry towards highly integrated low-cost system solutions. In the cellular subscriber area, market for PAs is increasingly migrating away from packaged single die with RFICs to multi-band multi-mode integrated modules that deliver a complete amplifier solution and contain several different components. This preferred strategy requires a much-reduced RF component count at the handset assembly level. This preference is in line with the increase in outsourcing by the handset manufacturers to third party assembly houses. These RF modules typically integrate all or most of the matching and bypassing networks, and may also provide power detection, power management, filtering and RF switches for both transmit/receive and band selection. The RF performance of cellular power amplifiers is a very strong function of the handset battery voltage. For 2005, we continue to see the proliferation of 3V-based systems in disagreement with published expectations from 2003 and 2004 ITRS PA tables. The 2005 tables were revised accordingly.

Increased activity in the integration into the module of all other radio functions, such as transceivers, frequency synthesis, and filters and digital sections is a logical extension of the integrated PA module. This highly integrated solution would provide a true single radio module solution in a small footprint that has a digital interface to the handset's DSP and central processing unit (CPU) and that handles essentially all post-baseband RF functions for a given application. There is little doubt that such SIP single radios will eventually become commonplace in the industry. The challenges for the semiconductor technology community will likely be how to meet the cost and performance targets, with as much integration as possible available in the semiconductor technologies.

The major challenges for base station PAs revolve around several fundamental issues that are common to all high frequency, high power transistors. The first of these issues is the ability to match the input and especially the output impedance of the very large transistors to the other parts of transmitter amplification chain. Poor matching results in reduced efficiency in the amplification lineup and in the transmitter lineup not achieving the desired output power or

linearity. The higher power density of gallium nitride devices would help substantially because a physically smaller device is easier to match to the other parts of the transmitter system. Another major challenge for base station power amplifiers is heat dissipation. The DC to RF efficiency is at best about 50%, which means that half of the DC power is converted to heat. This heat raises the temperature of the device that negatively impacts performance and device reliability. Base station devices are designed to achieve a MTTF (Mean Time To Failure) of 100 years. This means that half of the devices will fail the pre-established degradation criteria in 100 years. This may seem like a stringent requirement, but based on reliability statistical analysis this translates to a 10% failure in 20 years. Base stations, in general, are designed to be functional for 20 years. Gallium nitride devices also provide advantages in the area of thermal management. First, gallium nitride is a wide bandgap material, which means its RF performance degrades more slowly than Si or GaAs devices at elevated temperatures. Because of its refractory characteristics GaN should also have longer MTTFs than either Si LDMOS or GaAs. Because of its refractory characteristics GaN should also have longer MTTFs than either Si LDMOS or GaAs. Because of the immaturity of the technology longer MTTFs have not been demonstrated, but hold significant promise. One final advantage of GaN is that the GaN epitaxial devices layers can be grown on a SiC substrate. The higher thermal conductivity of SiC has contributed to the higher power density demonstrated by GaN devices when SiC is used at the substrate.

MILLIMETER WAVE

Compound semiconductor technologies have a number of similarities with silicon technologies and yet in many ways are distinctly different. While III-Vs have benefited from the advances in manufacturing equipment and chemistries, the development of these tools and chemicals is focused on the silicon industry and is not necessarily optimum for compound semiconductor processing. For example, the mass density of GaAs is about 2× that of Si, and because GaAs is more fragile, wafers are generally processed at 0.025-inch thickness (about 50% thicker than Si wafers) and result in a significant weight factor for automated wafer handling equipment and spinners. Additionally, the need to thin wafers to 0.002-inch thickness for thermal dissipation makes wafer breakage a yield issue that must be addressed.

Six-inch diameter semi-insulating GaAs wafers are routinely available and are becoming the *de facto* standard, although some foundries are still at four-inch. The move to six-inch and eight-inch substrates will be driven not only by economies of scale and chip cost but also by equipment availability. GaAs tends to be two generations behind Si in wafer size, with InP a further generation behind. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from the advances in processing equipment. This continued pace in substrate size is particularly true for SiC, which still suffers from a significantly high defect density. Today there is no production source of semi-insulating GaN substrates. Most GaN device epitaxy is done on SiC substrates. Significant technology breakthroughs will be required before GaN becomes commercially viable. Unresolved issues remain regarding SiC versus GaN substrates for GaN HEMTS. Advances in high resistivity Si substrates must also be addressed as SiGe HBT and RF CMOS push toward the mm-wave spectrum.

Device challenges, some of which are unique to III-Vs include the following: 1) the requirement for substrate vias for low inductance grounds in microstrip mm-wave circuits; 2) techniques for heat removal including wafer thinning and for low parasitic air-bridge interconnects; 3) high breakdown voltages for power devices; and 4) non-native oxide passivation. While these issues have been mostly solved for GaAs, they need to be applied successfully to the emerging III-V technologies of InP, SiC, and GaN. One of the critical challenges for high power III-V devices is thermal dissipation. This challenge is especially true for high-power density devices such as GaN.

TECHNOLOGY REQUIREMENTS

CHANGES IN THE TECHNOLOGY REQUIREMENTS TABLES FOR 2005

Each of the five sections contains Technology Requirements Tables. The major changes made in the Tables given here since the 2004 Updates for these Tables.

RF AND AMS CMOS (0.8 GHz – 10 GHz)

1. Derived from 2004 AMS and RF Transceiver Technology Requirement Tables.
2. Merged high-speed analog CMOS and RF CMOS.
3. Merged precision analog CMOS and driver CMOS.
4. The trends of higher integration and performance levels for logic with mixed-signal circuitry have continued with the following results:

a. Steadily increasing digital processing capabilities enabling more signal treatments to be done in the digital domain.
b. Increased F_t and F_{max} along with reduced RF noise.
c. Use of a second or a third input/output (I/O)-transistor gate oxide to 1) optimize performance at higher voltages, 2) support interfaces to the outside world, and 3) maintain the high signal-to-noise requirements for mixed-signal applications.
d. Introduction of multiple threshold voltages enables optimization of digital power-delay and offers design options for mixed-signal and RF applications.
e. Reduced power levels for digital, RF, and analog functions.

RF AND AMS BIPOLAR DEVICES (0.8 GHz – 10 GHz)

1. Derived from 2004 AMS and RF Transceiver Technology Requirement Tables.
2. Separated Bipolar Technology Requirement Table into the 3 sub-areas:
   a. High Speed – highest speed bipolar devices.
   b. RF – most typical bipolar devices used for wireless.
   c. High Voltage – bipolar devices from part of the former 2004 Update Power Amplifier Table.
3. Included silicon (SiGe) bipolar devices, but not III-V HBTs. The III-V HBTs are in the Power Amplifier and mm-Wave Tables.
4. Other major changes from 2004 Technology Requirements Tables:
   a. Added rows for all device types to give F_t, F_{max}, and breakdown voltage between the collector and emitter with base open (BV_{ceo}).
   b. Removed power supply requirement because they are more meaningful for CMOS.
   c. Added current density at peak F_t for high-speed devices.
5. There is some overlap with other tables in the areas of:
   a. High-Speed Bipolar in the mm-Wave Table.
   b. High-Voltage Bipolar in the PA Table.

PASSIVES FOR RF AND AMS (0.8 GHz – 10 GHz)

1. Derived from 2004 AMS, RF Transceiver, and PA Technology Requirement Tables.
2. Separated into the 3 sub-areas:
   a. Analog – for low frequency analog/mixed signals applications.
   b. RF – for RF applications.
   c. PA – for power amplifier applications.
3. Divided analog section into MOS capacitor and resistor (thin-film, back-end-of-line (BEOL) resistor and p+ polysilicon resistor).
4. Divided RF section into metal-insulator-metal (MIM) capacitor, inductor, and MOS varactor.
5. Divided PA section into PAs, III-Vs, Passives, and PA Silicon/SeGe Passives.
6. PA passives requirements remain largely unchanged.

POWER AMPLIFIERS (0.8 GHz – 10 GHz)

1. Removed passives from the 2005 PA Table and incorporated them into the Passives Table.
2. PA table remains essentially unchanged. PA device evolution is slow due to nearly fixed battery voltages and ruggedness requirements.
3. SiGe multi-band cellular PAs are being sampled but they are not yet present in any significant volumes. CMOS PA's are being discussed and sampled, but demonstrations of viable and rugged PAs are still not published.
4. Highly integrated modules with multi-layer laminates and low temperature co-fired ceramics (LTCC) are dramatically reducing the total RF front end area.

5. The PA Potential Solutions Table shows silicon integration enablers for PA integration into system chip with a focus on SOI and high resistance substrates and above-IC RF micro-electro-mechanical systems (MEMS) technology.
6. For Base station PAs:
   a. Device cost, as measured by dollars per RF Watt, is projected to steadily decrease from about $0.70/W today to less than $0.50/W by 2008.
   b. Applications are moving from 2 GHz and below to higher frequencies, such as WiMAX at 3.5 GHz and from saturated power amplifiers to more linear power amplifiers for CDMA and WCDMA.
   c. The trend for all semiconductor device technologies is to move to higher voltage that will increase power density and reduce device size for the same output power.
   d. As frequencies increase, LDMOS will experience challenges from GaAs FET and SiC MESFET. SiC technology will be supplanted by GaN technology.

MILLIMETER WAVE (10 GHz – 100 GHz)

1. Projections are taken out only to near term [~2011, as in previous years because:
   a. Compound semiconductors do not have the decades of history from which to extrapolate as does silicon.
   b. The compound semiconductor industry is smaller and less mature and makes fewer and smaller investments than the silicon semiconductor industry does.
2. Gate dimensions are not shrinking as fast as predicted in the 2003–2004 roadmaps:
   a. The 70 nm gate will not be in production until the 2007 time frame.
   b. The advances in performance are tied more to material and device technologies. For example, MHEMTs have higher performance than PHEMTs have at the same lithographic dimensions.
3. Some technologies will tend to obsolescence during this decade.
   a. No new designs are expected for low noise GaAs MESFETs beyond 2006. Foundries are likely to produce for legacy products and for end-of-life markets only. The same trends also apply to low voltage power MESFETs.
   b. PHEMTs and InP HEMTs may lose ground to MHEMTs late in the decade.
4. GaN is advancing much faster than predicted in 2003 and 2004. Some parameters that were colored “red” for 2007 in the 2004 Update Table have already been demonstrated; but materials quality and device reliability are still issues for volume production.

RF AND AMS CMOS

The trends of the CMOS roadmap to support higher integration and performance levels for logic with mixed-signal circuitry have continued. Its continued focus on 1/f noise, passive component density, and device matching is imperative to satisfy the increasing demands on power and area efficiency. Emerging issues from this increased integration level are analog device modeling and protection against electrostatic discharge.

Performance and cost considerations will continue to drive modularity of process features in order to adapt the technology to specific SOC architectures. However, the more stringent mixed-signal transistor requirements may force the addition of process complexity to achieve integration goals. CMOS technology is gaining importance in the field of mixed-signal at the cost of bipolar and Si or SiGe-based BiCMOS processes. Technology requirements today are driven by the need for lower power consumption, lower noise, and lower cost in RF transceivers. In the near future, technology requirements will also be driven by the need to enable reconfiguring the RF transceiver in a software-defined radio and to enable higher level synthesis in RF transceivers (refer to the *Systems Drivers Chapter)*. Additional technology requirements are to increase signal isolation for multi-mode and multi-band capabilities

Table 46a RF and Analog Mixed-Signal CMOS Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Performance RF/Analog [1]									
Supply voltage (V) [2]	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**
T_{ox} (nm) [2]	**2.2**	**2.1**	**2.0**	**1.9**	**1.6**	**1.5**	**1.4**	**1.4**	**1.3**
Gate Length (nm) [2]	**75**	**65**	**53**	**45**	**37**	**32**	**28**	**25**	**22**
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	**47**	**40**	**32**	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**190**	**180**	**160**	**140**	**100**	**90**	**80**	**80**	**70**
σ V_{th} matching (mV·µm) [5]	**6**	**6**	**6**	**6**	**5**	**5**	**5**	**5**	**5**
I_{ds} (µA/µm) [6]	**19**	**15**	**13**	**11**	**9**	**8**	**7**	**6**	**6**
Peak F_t (GHz) [7]	**120**	**140**	**170**	**200**	**240**	**280**	**320**	**360**	**400**
Peak F_{max} (GHz) [8]	**200**	**220**	**270**	**310**	**370**	**420**	**480**	**530**	**590**
NF_{min} (dB) [9]	**0.33**	**0.3**	**0.25**	**0.22**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Precision Analog/RF Driver [1]									
Supply voltage (V)	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**1.8**	**1.8**	**1.8**	**1.8**
T_{ox} (nm) [10]	**5**	**5**	**5**	**5**	**5**	**3**	**3**	**3**	**3**
Gate Length (nm) [10]	**250**	**250**	**250**	**250**	**250**	**180**	**180**	**180**	**180**
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$ [11]	**220**	**220**	**220**	**220**	**220**	**160**	**160**	**160**	**160**
1/f Noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**500**	**500**	**500**	**500**	**500**	**180**	**180**	**180**	**180**
σ V_{th} matching (mV·µm) [5]	**9**	**9**	**9**	**9**	**9**	**6**	**6**	**6**	**6**
Peak F_t (GHz) [7]	**40**	**40**	**40**	**40**	**40**	**50**	**50**	**50**	**50**
Peak F_{max} (GHz) [8]	**70**	**70**	**70**	**70**	**70**	**90**	**90**	**90**	**90**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

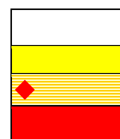
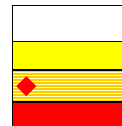


Table 46b RF and Analog Mixed-Signal CMOS Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Performance RF/Analog [1]							
Supply voltage (V) [2]	**1**	**1**	**1**	**1**	**1**	**1**	**1**
T_{ox} (nm) [2]	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**	**0.9**
Gate Length (nm) [2]	**20**	**18**	**16**	**14**	**13**	**12**	**11**
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	**30**	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**60**	**50**	**50**	**50**	**40**	**40**	**30**
σ V_{th} matching (mV·µm) [5]	**5**	**5**	**4**	**4**	**4**	**4**	**3**
I_{ds} (µA/µm) [6]	**5**	**4**	**4**	**3**	**3**	**3**	**2**
Peak F_t (GHz) [7]	**440**	**490**	**550**	**630**	**670**	**730**	**790**
Peak F_{max} (GHz) [8]	**650**	**710**	**790**	**890**	**950**	**1020**	**1110**
NF_{min} (dB) [9]	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Precision Analog/RF Driver [1]							
Supply voltage (V)	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.5**	**1.5**
T_{ox} (nm) [10]	**3**	**3**	**3**	**3**	**3**	**2.6**	**2.6**
Gate Length (nm) [10]	**180**	**180**	**180**	**180**	**180**	**130**	**130**
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$ [11]	**160**	**160**	**160**	**160**	**160**	**110**	**110**
1/f Noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	**180**	**180**	**180**	**180**	**180**	**135**	**135**
σ V_{th} matching (mV·µm) [5]	**6**	**6**	**6**	**6**	**6**	**5**	**5**
Peak F_t (GHz) [7]	**50**	**50**	**50**	**50**	**50**	**70**	**70**
Peak F_{max} (GHz) [8]	**90**	**90**	**90**	**90**	**90**	**120**	**120**
		switch to FD ro DG device					

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 46:

[1] Year of first digital product for a given technology generation as presented in overall roadmap technology characteristics (ORTC) tables. Lithographic drivers for key technologies are indicated. Year of first RF and mixed-signal product at the same technology lag the low-standby power roadmap by one year. Beyond Planar CMOS, performance RF/Analog CMOS reflect DG CMOS, Precision Analog/RF driver device color change to yellow reflecting uncertainty on device integration. The supply voltage, T_{ox}, gate length and I_{ds}, F_t, F_{max} color codes reflected the low-standby power roadmap. The logic low standby power is the driver for this. Refer to the LSTP tables in the PIDS chapter for the latest information.

[2] Nominal supply voltage, V_{dd}, SiO_2 equivalent physical CMOS gate dielectric thickness, T_{ox}, and minimum nominal gate length from low-standby power digital roadmap.

[3] Measure for the low frequency amplification of a 5× minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$. The minimum value of 30 exceeds the projected technology capability with continued scaling for the standard logic device. When this occurs, the standard logic device should be replaced with a unique device designed for specifically f or superior gain.

[4] 1/f noise spectral density, at a frequency of 1 Hz, normalized to an active emitter area of 1 μm^2.

[5] Matching specification for the NMOS transistor's threshold voltage, assuming "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity, e.g. by using dummy structures, are required. Statistical dopant fluctuations start limiting further improvement with SiO_2. Matching behavior of high-κ gate dielectrics very may be problematic. This parameter determines the lower boundary for the size of transistor in a mixed-signal circuit for a given accuracy and will limit dimensional, performance, and DC power consumption.

[6] I_{ds} for F_t of 50 GHz for a minimum transistor length. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[7] Extrapolated from 40 GHz with a 20 dB/dec slope.

[8] Peak F_{max} (measured from unilateral gain extrapolated from 40 GHz with a 20 dB/dec slope).

[9] This is the minimum transistor noise figure at 5 GHz.
[10] This device is required to achieve direct modulation of the PA for applications from 2 to 5 GHz and to support precision analog applications. With continued scaling of logic devices alternate device structures may be required to support the required specifications.
[11] Measure for the low frequency amplification of a 10× minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$.

RF AND AMS BIPOLAR DEVICES

RF and AMS bipolar devices are most frequently used in the LNA and frequency conversion transceiver and sometimes in the PA of wireless products. Technology requirements for bipolar devices used in wireless communications are driven by the need for lower power consumption, lower noise, and lower cost much in the same way as RF and AMS CMOS devices. Reduced power consumption and lower noise for bipolar devices are achieved through 1) higher F_t and F_{max}, 2) scaling of the vertical profile, and 3) scaling of the emitter width, which can bring about lower base resistance and lower noise. Reduced system level cost is achieved by higher levels of functional integration through the availability of higher breakdown transistors as described in the technology requirements table and the integration with more advanced CMOS technology generations. The very high performance levels and high dynamic range of bipolar devices can enable in the longer term new architectures for wireless products in a direct digital synthesis or software radio configuration.

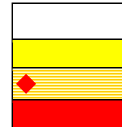
Table 47a 0.8 GHz–10 GHz RF and Analog Mixed-Signal Bipolar Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
General Analog NPN Parameters									
Emitter width (um)	**0.15**	**0.14**	**0.13**	**0.12**	**0.1**	**0.1**	**0.1**	**0.09**	**0.09**
1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz)	**3**	**3**	**2**	**2**	**2**	**1.5**	**1.5**	**1.5**	**1**
σ current matching (%·µm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
High Speed NPN (should be common to mmWave)									
Peak F_t (GHz) [V_{bc}=1V]	**200**	**230**	**265**	**300**	**350**	**370**	**385**	**400**	**420**
Peak F_{max} (GHz)	**240**	**260**	**300**	**330**	**390**	**410**	**425**	**440**	**460**
BV_{ceo}	**2**	**1.9**	**1.8**	**1.7**	**1.7**	**1.7**	**1.7**	**1.6**	**1.6**
J_c at Peak F_t (mA/µm²)	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
RF NPN									
Peak F_t (GHz) [V_{bc}=1V]	**80**	**80**	**90**	**90**	**100**	**100**	**110**	**110**	**120**
Peak F_{max} (GHz)	**150**	**160**	**170**	**180**	**190**	**200**	**210**	**220**	**230**
BV_{ceo}	**3.3**	**3.3**	**3.1**	**3.1**	**2.9**	**2.9**	**2.8**	**2.8**	**2.6**
NF_{min} (dB) at 5GHz	**0.3**	**0.28**	**0.26**	**0.24**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
I_c (µA/µm) [1] at 50GHz F_t	**43**	**37**	**28**	**22**	**16**	**15**	**14**	**13**	**12**
High Voltage NPN (Should be common to PA)									
Peak F_t (GHz) [V_{bc}=1V]	**30**	**32**	**34**	**36**	**38**	**40**	**42**	**44**	**46**
Peak F_{max} (GHz)	**100**	**110**	**120**	**130**	**140**	**150**	**160**	**170**	**180**
BV_{ceo}	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**	**8.5**
BV_{cbo} (V)	**18**	**18**	**18**	**18**	**16**	**16**	**16**	**16**	**16**

Table 47b 0.8 GHz–10 GHz RF and Analog Mixed-Signal Bipolar Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
General Analog NPN Parameters							
Emitter width (µm)	0.09	0.08	0.08	0.08	0.07	0.07	0.07
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	1	1	0.7	0.7	0.7	0.7	0.7
σ current matching (%·µm)	2	2	2	2	2	2	2
High Speed NPN (should be common to mmWave)							
Peak F_t (GHz) [V_{bc}=1V]	440	460	480	500	530	550	570
Peak F_{max} (GHz)	480	500	520	540	570	590	610
BV_{ceo}	1.5	1.5	1.4	1.4	1.3	1.3	1.3
J_c at Peak F_t ($mA/\mu m^2$)	19	20	21	22	23	24	25
RF NPN							
Peak F_t (GHz) [V_{bc}=1V]	120	130	130	140	140	150	150
Peak F_{max} (GHz)	240	250	260	270	280	290	300
BV_{ceo}	2.6	2.5	2.5	2.4	2.4	2.4	2.4
NF_{min} (dB) at 5GHz	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
I_c (µA/µm) [1] at 50GHz F_t	11	10	9	8	7	6	5
High Voltage NPN (Should be common to PA)							
Peak F_t (GHz) [V_{bc}=1V]	48	50	52	54	56	58	60
Peak F_{max} (GHz)	190	200	210	220	230	240	250
BV_{ceo}	8.5	8.5	8.5	8.5	8.5	8.5	8.5
BV_{cbo} (V)	16	16	16	16	16	16	16

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



PASSIVES

Analog MOS Capacitors for decoupling are based on the roadmap specifications for the analog precision device in the CMOS tables. As the gate oxide thickness is being scaled for this MOS transistor, capacitor density increases but leakage current becomes an issue. In the year 2010, a gate oxide thickness of 3 nm is required, but this results in unacceptable high leakage current. This might require the use of high-κ dielectrics in the MOS capacitors to reduce the leakage current to acceptable levels.

Resistors are used in all analog and mixed signal circuit blocks. Highly doped p-type polysilicon resistors are preferred in most cases for mixed signal and analog applications due to their good matching, low parasitic capacitance to the substrate and excellent temperature coefficient. These resistors consist of gate polysilicon doped with a high dose boron implant, which is normally the p-channel FET (PFET) source and drain (SD) implants. A 200–300 Ohm/square resistor is ideal for these applications. As CMOS is scaled further, the associated the shallow and lower dose SD implants result in resistances that exceed 500 Ohm/square for these devices. This may require an additional mask for analog applications in the future and lower tolerance devices with smaller resistances. These devices have an excellent temperature coefficient that is less than 100 ppm/C.

A thin-film BEOL resistor has several attractive features such as low tolerance, low parasitics, and the ability to make design changes with short lead times. These are excellent for use in RF and analog applications, especially in I/O circuits and current biasing. A typical thin film resistor is comprised of TaN, a common material in the copper BEOL process. It is integrated above Metal 1 or other upper metallization level and contacted with metal vias. These devices have excellent matching and are attractive for analog applications.

The key parameters for Metal-Insulator-Metal (MIM) Capacitors for RF applications are capacitance density, voltage linearity, leakage, matching and Q factor. Higher capacitance density is required for capacitor area scaling. The matching tolerances become smaller as the capacitance area scales down. The capacitance density value in the table indicates the value for one capacitor and does not include the stacking of two capacitors on top each other, which is sometimes done but requires doubling the mask levels and process steps. The value also is for Cu backend process, which poses significantly more challenges compared to Al backend in terms of integration and reliability.

The need for high performance on-chip monolithic spiral and multi-level spiral inductors in RF technologies recently has become increasingly important due to the technology and integration requirements of high functionality and low cost RF circuit applications. The typical interconnect scaling associated with digital circuit technologies, that is, BEOL scaling, is inconsistent with the need to keep series resistive losses low for high quality inductors. Additionally, minimizing substrate losses due to eddy currents and capacitive coupling is desired to increase Q. Integrating the inductors in the last, thick-metal levels of the BEOL and using large vias to provide a thick dielectric between the inductor and substrate help reduce these effects. Thick low-resistance metal wiring is needed for high Q applications such as in VCO circuits where high Q inductors are needed to reduce phase noise. Thick aluminum or copper inductors can be used to achieve peak Q performance of 25–30 for a 1 nH inductor at 3 GHz–5 GHz.

Accumulation and depletion mode MOS varactors offer attractive tuning ranges and Q-factors. The requirements listed in the table are for MOS varactors based on gate oxide for performance RF/analog transistors. They are updated with respect to tuning range cited in the previous 2004 ITRS Update because higher tuning ranges have been achieved with the CMOS scaling. The continuous improvement in inductor Q-factors requires the varactor Q-factor to further increase, otherwise the varactor Q-factor becomes the limiting factor for VCO performance improvements. It is not clear to what extent varactors with additional gate length reductions can achieve the required Q-factors in the range of 50 and higher and how the varactor characteristics will be affected by the introduction of high-κ dielectrics.

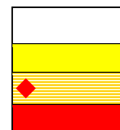
Table 48a Passives Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
ANALOG									
MOS Capacitor									
Density (fF/μm^2) [1]	**7**	**7**	**7**	**7**	**7**	**11**	**11**	**11**	**11**
Leakage (A/cm^2)	**<1e-9**	**<1e-9**	**<1e-9**	**<1e-9**	**<1e-9**	**<2e-6**	**<2e-6**	**<2e-6**	**<2e-6**
Resistor									
Thin Film BEOL									
Parasitic capacitance (fF/μm^2)	**0.03**	**0.03**	**0.03**	**0.03**	**0.05**	**0.05**	**0.05**	**0.05**	**0.08**
Temp. linearity (ppm/ºC)	**<100**	**<100**	**<100**	**<100**	**40-80**	**40-80**	**40-80**	**40-80**	**30**
1σ Matching (% μm)	**0.2**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.15**	**0.1**
Sheet resistance, Rs (Ohm/sq)	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**
P+ Polysilicon									
Parasitic capacitance (fF/μm^2)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
Temp. linearity (ppm/ºC)	**<100**	**<100**	**<100**	**<100**	**40-80**	**40-80**	**40-80**	**40-80**	**30**
1σ Matching (% μm)	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1**
Sheet resistance, Rs (Ohm/sq)	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**
RF									
Metal-Insulator-Metal Capacitor									
Density (fF/μm^2) [2]	**2**	**2**	**2**	**4**	**4**	**5**	**5**	**5**	**7**
Voltage linearity (ppm/V^2)	**<100**	**<100**	**<100**	**<100**	**<100**	**< 100**	**< 100**	**< 100**	**< 100**
Leakage (A/cm^2)	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**
σ Matching (%·μm)	**0.7**	**0.7**	**0.5**	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.3**
Q (5 GHz for 1pF)	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**
Inductor									
Q (5 GHz, 1nH) [3]	**25**	**27**	**29**	**30**	**32**	**34**	**36**	**38**	**40**
MOS Varactor									
Tuning Range [4]	**5.5**	**5.5**	**5.5**	**5.5**	**5.5**	**5.5**	**5.5**	**5.5**	**5.5**
Q (5 GHz, 0 V)	**30**	**30**	**35**	**35**	**40**	**40**	**45**	**45**	**50**
PA									
PA III-V Passives									
Inductors Q (1GHz, 5nH) [5]	**15**	**25**	**25**	**25**	**25**	**25**	**25**	**30**	**30**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**0.6**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
PA Silicon/SiGe Passives [Table 49 a&b]									
Inductors Q (1GHz, 5nH) [5]	**10**	**14**	**14**	**14**	**14**	**14**	**14**	**18**	**18**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**2**	**2**	**2**	**4**	**4**	**5**	**5**	**5**	**7**

Table 48b Passives Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
ANALOG							
MOS Capacitor							
Density (fF/μm^2) [1]	11	11	11	11	11	13	13
Leakage (A/cm^2)	<2e-6	<2e-6	<2e-6	<2e-6	<2e-6	<2e-5	<2e-5
Resistor							
Thin Film BEOL							
Parasitic capacitance (fF/μm^2)	0.08	0.08	0.08	0.08	0.08	0.08	0.08
Temp. linearity (ppm/ºC)	30	30	30	30	30	30	30
1σ Matching (% μm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Sheet resistance, Rs (Ohm/sq)	50	50	50	50	50	50	50
P+ Polysilicon							
Parasitic capacitance (fF/μm^2)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Temp. linearity (ppm/ºC)	30	30	30	30	30	30	30
1σ Matching (% μm)	1	1	1	1	1	1	1
Sheet resistance, Rs (Ohm/sq)	200–300	200–300	200–300	200–300	200–300	200–300	200–300
RF							
Metal-Insulator-Metal Capacitor							
Density (fF/μm^2) [2]	7	7	10	10	10	12	12
Voltage linearity (ppm/V²)	< 100	< 100	< 100	< 100	< 100	< 100	< 100
Leakage (A/cm^2)	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8	<1e-8
σ Matching (%·μm)	0.3	0.3	0.2	0.2	0.2	0.2	0.2
Q (5 GHz for 1pF)	>50	>50	>50	>50	>50	>50	>50
Inductor							
Q (5 GHz, 1nH) [3]	42	44	46	48	50	52	54
MOS Varactor							
Tuning Range [4]	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Q (5 GHz, 0 V)	50	55	55	60	60	60	60
PA							
PA III-V Passives							
Inductors Q (1GHz, 5nH) [5]	30	30	30	30	30	30	30
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/μm^2) [7]	2	2	2	2	2	2	2
PA Silicon/SiGe Passives [Table 49 a&b]							
Inductors Q (1GHz, 5nH) [5]	18	18	18	18	18	18	18
Capacitor Q [6]	>100	>100	>100	>100	>100	>100	>100
RF capacitor density (fF/μm^2) [7]	7	7	10	10	10	10	12

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 48 and b:
[1] This capacitance density corresponds to the gate oxide thickness for precision analog device in the CMOS table.
[2] No stacking (two capacitors on top of each other) is included. Coloring reflected MIM capacitor meeting all requirements including density, voltage linearity, leakage and matching on copper metallization.
[3] Q at 5 GHz for a single-ended 1nH inductor with a dedicated thick metal (analog metal).
[4] Defined as C_{max}/C_{min} in C-V curve of the varactor. Varactor align with performance RF device in the CMOS table.
[5] Inductor Q—quality factor of a 5nH inductor at 1 GHz achievable with the technology with a metallization suitable for handling the power requirements of the PA.
[6] Capacitor Q—quality factor of a 10 pF capacitor at 1 GHz achievable with the technology. Capacitor breakdown voltage must be rated for appropriate power amplification function.
[7] RF capacitor density—capacitor used for all other functions (matching, harmonic filtering, coupling, etc). Capacitor must have adequate breakdown for the given application. No stacking.

POWER AMPLIFIERS

Transmitted power levels of the order of tens of milliwatts to a few Watts depending on specific systems and require efficient and linear RF power amplifiers. Because of the large signal nature of PAs, they require significant ruggedness and higher breakdown voltages than available in the standard CMOS submicron technologies. In addition, because PAs are typically in battery-operated devices, a low knee voltage must also be maintained. Today, these power amplifiers are typically built as stand-alone amplifiers with either GaAs HBT, silicon LDMOS or GaAs PHEMT FET technologies. The integration of the RF power function into the silicon SOC solution requires significant device optimization and development efforts that are not just aimed at realizing the required RF functionality, but also the required isolation necessary for effective system integration.

Power management ICs are required for all but the simplest of wireless applications. This function conditions the power demands of the RF power amplifier and other wireless circuit blocks, regulates battery and charger surges; detects power levels; and provides the appropriate temperature, ruggedness, and leakage control for efficient system operation. This power management function typically is accomplished with high voltage CMOS technologies and requires very large periphery pass FET devices. It is expected that the power management function will also be integrated as part of the SOC technology instead of a separate IC within a module. The PA table includes the requirements for power management.

Some large-scale cellular baseband system providers made significant announcements in 2005 regarding the integration of multimode-multiband transceiver blocks into their baseband solutions. This integration has the potential to make radical changes in transceiver system architecture by replacing standard analog blocks with digital solutions that benefit from the high density deep-submicron CMOS characteristics.

There are minor revisions in the PA table for 2005 because in part the predictions for battery voltage reduction from 3.4 V to the 2.4 V did not occur. Through the next 2–3 years the battery voltage will remain at the same level. The RF performance of power amplifiers is greatly dictated by the battery voltage; a reduction of the voltage to 2.4 V will require significant changes in semiconductor and power management technologies.

Research results on above-IC integrated MEMS technologies suggest that these technologies have the potential of integrating large and expensive filter, switch and oscillator blocks into the silicon SOC. At this point, there are still very critical issues regarding the reliability, packaging, and high electrostatic voltage requirements of MEMS-based approaches. We don’t anticipate wide-scale usage of MEMS in integrated cellular PAs for the next 2–3 years.

The bulk of the base station semiconductor market remains at 2 GHz and below. The future market is projected to expand to higher frequencies as new applications and frequency bands are allocated. The most prominent, near term higher frequency application is WiMAX at 3.5 GHz. This application will benefit from the higher RF performance and device efficiency offered by GaAs PHEMTs. In spite of this move to higher frequencies, device cost as measured by dollars per RF Watt is projected to steadily decrease from about \$0.70/W today to less than \$0.50/W by 2008. One reason for this rapid price decrease is that a conversion from ceramic to plastic packaging is occurring. In 2005, Si LDMOS FETs are the dominant semiconductor technology, easily commanding a 95% market share with GaAs FETs picking up the rest. SiC and GaN FETs are now appearing over the technology horizon. The trend for all semiconductor device technologies is to move to higher voltage that will increase power density and reduce device size for the same output power. The reduced device size requires less complex impedance matching networks and reduces power loss and increases power efficiency. There is a trend from saturated power amplifiers to more linear power amplifiers to support the digital modulation formats of CDMA and WCDMA. For the same size devices, the available linear power is about one-half the available saturated power. But, the PAE in linear operation is always less than in saturated operation. Maximum RF output power from a single packaged device will not increase above an approximate 240 W unless there is a major change in the design of

commercial communications systems. As frequencies increase, the challenge for LDMOS will be continuing to achieve low frequency (2 GHz) performance at higher frequencies. Failing to meet this challenge will result in replacing LDMOS with more expensive technologies. GaAs FET technology offers higher frequency performance, higher efficiency, and higher power density than LDMOS but at a higher cost. A major challenge for GaAs FETs is the move to a higher operating voltage that is closer to the operating voltage of LDMOS (28V). SiC MESFET technology is much less mature than LDMOS and GaAs, but offers higher voltage operation and a higher power density. In 2005, the highest RF power SiC device is 60 W, which is one-quarter less than that available from LDMOS and GaAs. SiC MESFET technology uses a very expensive, high thermal conductivity SiC substrate. In the long-term, SiC technology will be replaced with GaN technology. GaN technology is developing. Its first products are expected by 2006 with the potential for higher power densities than LDMOS, GaAs, and SiC. GaN technology is being investigated with several substrate materials, such as SiC, sapphire, silicon, and GaN. Each of these substrate materials offers advantages and disadvantages. The major challenge for GaN technology is achieving the very high level of device reliability that has been demonstrated using LDMOS and GaAs. High-heat dissipation packaging will need to be developed to take full advantage of the potential of GaN technology.

Table 49a Power Amplifier Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Nominal Battery Voltage	**3.2**	**3.2**	**3.2**	**3.2**	**2.4**	**2.4**	**2.4**	**2.4**	**2.4**
PA Product Solutions	**Single Radio SIP [1]**		**Radio/Baseband SIP [2]**					**Radio/Baseband SIP [2]**	
PA Frequency (GHz)	**0.8–6**		**0.8-6**					**0.8-6**	
III-V HBT Transistor									
F_{max} (at V_{cc}) (GHz)	**45**	**45**	**45**	**45**	**55**	**55**	**55**	**65**	**65**
BV_{CBO} (V)	**25**	**25**	**25**	**25**	**18**	**18**	**18**	**18**	**18**
Linear efficiency (%) [1]	**52**	**52**	**52**	**52**	**55**	**55**	**55**	**55**	**55**
Area (mm^2) [2]	**2.5**	**2.5**	**2.5**	**2.5**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Cost/mm^2 (US$) [3]	**0.4**	**0.35**	**0.32**	**0.3**	**0.28**	**0.28**	**0.28**	**0.25**	**0.25**
III-V HBT Integration									
Power management [4]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [5]	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**	**E-PHEMT**
Filter [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
III-V PHEMT Transistor									
F_{max} (at V_{dd}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**	**75**	**75**
BV_{DGO} (V)	**20**	**20**	**20**	**20**	**16**	**16**	**16**	**16**	**16**
Linear Efficiency (%) [1]	**55**	**55**	**55**	**55**	**58**	**58**	**58**	**58**	**58**
PA Area (mm^2) [2]	**4**	**4**	**4**	**4**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Cost/mm^2 (US$) [3]	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**	**0.24**	**0.24**	**0.22**	**0.22**
III-V PHEMT Integration									
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [5]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Filter [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Silicon MOSFET Transistor									
T_{ox} (PA) (Å) [7]	**60**	**60**	**60**	**60**	**35**	**35**	**35**	**35**	**35**
F_{max} (at V_{dd})	**45**	**45**	**45**	**45**	**60**	**60**	**60**	**60**	**60**
BV_{DSS} (V)	**12**	**12**	**12**	**12**	**10**	**10**	**10**	**10**	**10**
Linear efficiency (%) [1]	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**
PA Area (mm^2) [2]	**6**	**6**	**6**	**6**	**4.5**	**4.5**	**4.5**	**4.5**	**4.5**
Cost/mm^2 (US$) [3]	**0.08**	**0.08**	**0.08**	**0.08**	**0.06**	**0.06**	**0.06**	**0.05**	**0.05**
Silicon MOSFET Integration									
Power management [4]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Switch [5]	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter [6]	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**
SiGe HBT Transistor									
F_{max} (GHz)	**60**	**60**	**60**	**60**	**80**	**80**	**80**	**80**	**80**
BV_{CBO} (V)	**18**	**18**	**18**	**18**	**16**	**16**	**16**	**16**	**16**
Linear efficiency (%) [1]	**50**	**50**	**50**	**50**	**55**	**55**	**55**	**55**	**55**
PA Area (mm^2) [2]	**2.5**	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**	**2**	**2**
Cost/mm^2 (US$) [3]	**0.12**	**0.12**	**0.12**	**0.12**	**0.11**	**0.11**	**0.11**	**0.11**	**0.11**
SiGe Integration									
Power management	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

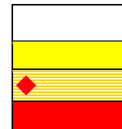
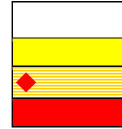


Table 49b Power Amplifier Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Nominal Battery Voltage	2.4	2.4	2.4	2.4	2.4	2.4	2.4
PA Product Solutions	Radio/Baseband SIP [2]						
PA Frequency (GHz)	0.8-6						
III-V HBT Transistor							
F_{max} *(at* V_{cc}*) (GHz)*	65	65	65	65	65	65	65
BV_{CBO} *(V)*	18	18	18	18	18	18	18
Linear efficiency (%) [1]	55	55	55	55	55	55	55
Area (mm^2*) [2]*	2.2	2.2	2.2	2	2	2	2
Cost/mm^2 *(US$) [3]*	0.25	0.25	0.25	0.25	0.25	0.25	0.25
III-V HBT Integration							
Power management [4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Switch [5]	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT	E-PHEMT
Filter [6]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
III-V PHEMT Transistor							
F_{max} *(at* V_{dd}*) (GHz)*	75	75	75	75	75	75	75
BV_{DGO} *(V)*	16	16	16	16	16	16	16
Linear Efficiency (%) [1]	58	58	58	58	58	58	58
PA Area (mm^2*) [2]*	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Cost/mm^2 *(US$) [3]*	0.22	0.15	0.15	0.15	0.15	0.15	0.15
III-V PHEMT Integration							
Power management [4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Switch [5]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Filter [6]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Silicon MOSFET Transistor							
T_{ox} *(PA) (Å) [7]*	35	35	35	35	35	35	35
F_{max} *(at* V_{dd}*)*	60	60	60	60	60	60	60
BV_{DSS} *(V)*	10	10	10	10	10	10	10
Linear efficiency (%) [1]	45	45	45	45	45	45	45
PA Area (mm^2*) [2]*	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Cost/mm^2 *(US$) [3]*	0.05	0.05	0.05	0.05	0.05	0.05	0.05
Silicon MOSFET Integration							
Power management [4]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch [5]	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Filter [6]	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
SiGe HBT Transistor							
F_{max} *(GHz)*	80	80	80	80	80	80	80
BV_{CBO} *(V)*	16	16	16	16	16	16	16
Linear efficiency (%) [1]	55	55	55	55	55	55	55
PA Area (mm^2*) [2]*	2	2	2	2	2	2	2
Cost/mm^2 *(US$) [3]*	0.11	0.11	0.11	0.11	0.11	0.11	0.11

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
SiGe Integration							
Power management	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 49a and b:
[1] Linear efficiency—power added efficiency of the final PA stage under personal communication service (PCS) CDMA (IS-95) modulation.
[2] Area—total semiconductor area necessary for the implementation of the quad-band GSM/general packet radio service (GPRS)/ Enhanced Data rates for GSM Evolution (EDGE) PA function, including matching/filtering.
[3] Cost/mm^2—approximate commercial foundry cost of the area mentioned in [4].
[4] Power management—capability of the technology to provide RF power detection/DC power management for the PA.
[5] Switch—capability of the technology to integrate cost-effectively a transmit/receive switch into the PA active die.
[6] Filter—capability of the technology to integrate high-quality band selection filters needed for the assumed PA solution; currently performed with surface acoustic wave (SAW) filter technology.
[7] T_{ox} (PA)—thickness of the MOSFET transistor in the RF power amplifier function.

Table 50a Base Station Devices Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Application frequency (GHz) [1]	**0.8–2.7**		**0.8–3.5**			**0.8–5**			
Cost ($$/Watt)	**0.7**	**0.6**	**0.5**	**0.4**		**0.3**			**0.25**
Packaging (C-Ceramic, P-Plastic)	**C/P**	**Plastic**							
Si LDMOS									
Operating voltage (V)	**<40**	**<40**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**1**	**1.2**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**
Saturated PAE (%)	**65**	**68**	**65**	**68**	**70**	**65**	**65**	**65**	**70**
Linear power (Watt)	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**	**<120**
Linear PAE (%)	**50**	**52**	**50**	**52**	**54**	**50**	**50**	**50**	**52**
GaAs FET									
Operating voltage (V)	**28**	**28**	**28**	**28**	**28**	**28**	**28**	**28**	**28**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**	**180**	**240**	**240**
Saturated power density (W/mm)	**1**	**1.2**	**1.5**	**1.5**	**1.5**	**1.8**	**1.8**	**1.8**	**1.8**
Saturated PAE (%)	**68**	**70**	**72**	**68**	**70**	**72**	**72**	**68**	**68**
Linear power (Watt)	**<60**	**<60**	**<60**	**<90**	**<90**	**<90**	**<90**	**<120**	**<120**
Linear PAE (%)	**52**	**55**	**57**	**52**	**54**	**56**	**57**	**52**	**52**
SiC FET									
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**60**	**60**	**60**	**120**	**120**	**120**	**120**	**180**	**180**
Saturated power density (W/mm)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**4**	**4**
Saturated PAE (%)	**45**	**45**	**47**	**42**	**45**	**45**	**47**	**42**	**42**
GaN FET									
Operating voltage (V)	**28**	**28**	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**60**	**60**	**120**	**120**	**120**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**3**	**3**	**4**	**4**	**5**	**5**	**5**	**5**	**5**
Saturated PAE (%)	**52**	**55**	**55**	**60**	**55**	**60**	**60**	**55**	**60**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

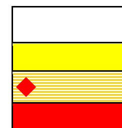
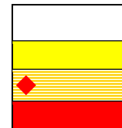


Table 50b Base Station Devices Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Application frequency (GHz) [1]	**0.8–5**						
Cost ($$/Watt)	**0.25**						
Packaging (C-Ceramic, P-Plastic)	**Plastic**						
Si LDMOS							
Operating voltage (V)	<50	<50	<50	<50	<50	<50	<50
Saturated power (Watt)	240	240	240	240	240	240	240
Saturated power density (W/mm)	1.4	1.4	1.4	1.4	1.4	1.4	1.4
Saturated PAE (%)	70	70	70	70	70	70	70
Linear power (Watt)	<120	<120	<120	<120	<120	<120	<120
Linear PAE (%)	52	52	52	52	52	52	52
GaAs FET							
Operating voltage (V)	28	28	28	28	28	28	28
Saturated power (Watt)	240	240	240	240	240	240	240
Saturated power density (W/mm)	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Saturated PAE (%)	70	70	70	72	72	72	72
Linear power (Watt)	<120	<120	<120	<120	<120	<120	<120
Linear PAE (%)	55	55	55	57	57	57	57
SiC FET							
Operating voltage (V)	48	48	48	48	48	48	48
Saturated power (Watt)	180	180	180	180	180	180	180
Saturated power density (W/mm)	4	4	4	4	4	4	4
Saturated PAE (%)	42	42	42	42	42	42	42
GaN FET							
Operating voltage (V)	48	48	48	48	48	48	48
Saturated power (Watt)	240	240	240	240	240	240	240
Saturated power density (W/mm)	5	5	5	5	5	5	5
Saturated PAE (%)	55	60	60	60	60	60	60

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 50:

[1] Application frequencies affected device saturated PAE scaling.

MILLIMETER WAVE

In the near term, which is until large volume commercial applications such as automotive radar and local multipoint distribution services (LMDS) emerge, the definition for mm-wave production in the following technology requirements tables differs substantially from that for the other Si, IV-IV, and III-V technologies. Demand for millimeter wave monolithic microwave integrated circuits (MMICs) for military, space, and specialty applications can be satisfied by modest wafer volumes in the 10 to 100 wafers /year per process or device technology (e.g., HBT, 0.5 µm HEMTs, 0.25 µm HEMTs, 0.15 µm HEMTs, and the like, in GaAs, InP, and GaN). The number of wafers per year per process or device technology depends on the product and application. For nominal wafer sizes of 100 mm and 150 mm, chip sizes of 2 mm^2 to 10 mm^2, and composite yields of 50% to 75%, this translates to tens of thousands of chips per year per process technology, which is not the millions of chips per year for Si and wireless communications chips sets. The composite yield is the line yield X DC X yield X RF yield X visual yield. This relatively low volume presents a unique challenge to mm-wave device foundries. In order to maintain a process as viable and manufacturable, a foundry needs to process a minimum of 100's of wafers per year per process technology. This minimum volume is necessary to maintain statistical process control. Smaller volumes or process variations, known as boutique processes, are possible but at the expense of overall process stability. Thus, production for millimeter wave products is defined as 100's of wafer per process technology per year under computer assisted manufacturing (CAM) and statistical process control

We divide the mm-wave technology requirements into two major device types—field effect and bipolar transistors. While the transport mechanisms and structure within each type are similar, there are vast differences in performance due to the selection of substrate material and design of the epitaxial layer stack. The major classes of millimeter wave transistors are listed in the following paragraphs.

Field effect transistors (FETs) are majority carrier devices in which electron transport is in a thin layer parallel to the wafer surface. The major types are as follows:

- MESFETs are composed of homogeneous layers in which electron transport occurs in an intentionally doped layer and are generally GaAs-based.
- HEMTs are composed of layers of different bandgap materials on a lattice-matched substrate. Carriers in HEMTs are provided by a highly doped layer and carrier transport occurs in an adjacent undoped layer, resulting in much higher mobility due to the lack of ionized charge scattering. HEMT are generally InP- and GaN-based.
- PHEMTs are composed of layers with different bandgap materials on a substrate in which the lattice constant of the layers are close, but not matched, to the lattice constant of the substrate. PHEMTs have higher mobility than HEMTs and are generally GaAs-based.
- MHEMTs are composed of layers of different bandgap materials on a substrate in which the lattice constants of the layers are mismatched to the substrate. The resulting strain is taken up by a specially designed buffer layer. MHEMTs offer the highest degree of flexibility in design and in mm-wave performance. Generally, they are made on GaAs substrates to take advantage of more mature materials and processing technologies.

HBTs are minority carrier devices in which carrier transport is perpendicular to the wafer surface. The major types are as follows:

- InP HBTs are composed of ternary and quaternary layers that contain a number of III-V elements [In, Ga, As, Sb, P] that are closely lattice matched to InP substrates. GaAs HBTs are generally used below 10 GHz.
- SiGe HBTs are composed of a single crystal mixture of Si and Ge on a Si substrate.

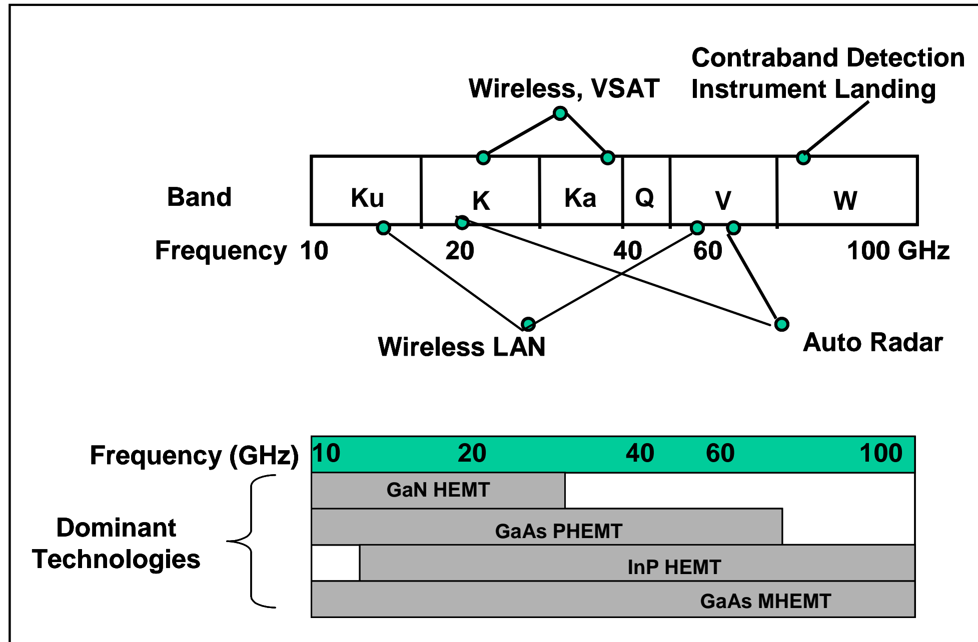


Figure 45 Millimeter Wave Commercial Applications Spanning 10 GHz to 100 GHz

Figure 45 illustrates the potential high volume commercial markets for mm-wave devices. After a major decline in the GaAs industry in 2001, the mm-wave market is likely to be dominated by automotive and WLAN applications. Figure 45 also shows the most likely scenario for deployment of device types over this frequency spectrum. GaN HEMTs may replace all other III-Vs for power applications up to 40 GHz, but there exist substantial technical challenges to be resolved. While PHEMTs have been reported at 60 GHz and even 94 GHz, it is likely that the higher mm-wave frequencies will be the domain of InP HEMTs and MHEMTs due to both higher performance and lower DC power requirements. PHEMTs will still have a role at the lower end of the spectrum due to their cost advantage, but they are likely to be replaced by the end of the decade.

InP HBTs and SiGe are ideal for high-speed logic and mixed-signal applications. These applications are due to the much better threshold control in bipolars, in which the threshold is a function of bandgap (a materials property) rather than the Schottky barrier and Fermi level that depend on processing. HBTs are also the devices of choice for low phase noise oscillators. MESFETs are likely to become obsolete for new applications in mid-decade as InP and SiGe performance advantages overtake those of MESFETs. Although the gap between InP and SiGe is closing, InP will always have the advantage of higher breakdown, while SiGe BiCMOS holds the advantage for integration density. Enhancement and depletion (ED) mode PHEMTs and MHEMTs are also candidates for high speed circuits and also offer the advantage of lower power consumption than bipolar devices.

Table 51 for mm-wave is focused on low noise and power MMICs containing HEMTs, and PHEMTs and on digital/mixed-signal circuits containing MESFETs and HBTs. While mixers, oscillators, varactors, switches, and phase shifters are as important, the technical challenges for all the devices can be embodied in the small signal (low noise) and large signal (power) functions. Other device types and passives should be included in future years.

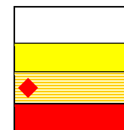
Table 51 Millimeter Wave 10 GHz–100 GHz Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
*Device Technology—FET **									
GaAs MESFET (digital mixed-signal)									
Gate length—L physical (nm)	150	150	-	-	-				
Minimum M1 pitch (nm)	680	680	-	-	-				
F_t – enhancement mode (GHz)	120	120	-	-	-				
F_t – depletion mode (GHz)	100	100	-	-	-				
BV_{GD} (1 mA/mm, V_g=0) (volts)	5 to 10	5 to 10	-	-	-				
Power delay product at gate delay-FO=1 (fJ at pS)	1.2 at 18	1.2 at 18	-	-	-				
Shortest DCFL gate delay (pS)	6	6	-	-	-				
Interconnect metal layers	5	5	-	-	-				
Interconnect metal	Al	Al	-	-	-				
Inter line dielectric constant (effective)	3.1	3.1	-	-	-				
GaAs PHEMT (low noise)									
Gate length (nm)	100	100	70	70	70	50	50		
F_t (GHz)	130	130	150	150	170	170	200		
Breakdown (volts)	7.5	7.5	7	7	6	5	5		
I_{max} (mA/mm)	700	700	600	600	600	550	550		
G_m (S/mm)	0.72	0.72	0.8	0.8	0.8	0.85	0.85		
NF (dB) at 26 GHz, 18–20 dB associated gain	2.5	2.5	2	2	2	1.8	1.8		
NF (dB) at 94 GHz, 8–10 dB associated gain	4	4	3.5	3.5	3.5	3.2	3.2		
GaAs PHEMT (power)									
Gate length (nm)	100	100	100	100	70	70	70		
F_{max} (GHz)	150	150	200	200	250	250	250		
Breakdown (volts)	11	11	9	9	7	7	7		
I_{max} (ma/mm)	750	750	850	850	900	900	900		
G_m (S/mm)	0.67	0.67	0.85	0.85	0.95	0.95	0.95		
P_{out} at 26 GHz and peak efficiency (mW/mm)	550	550	600	600	750	750	750		
Peak efficiency at 26 GHz (%)	30	30	40	40	45	45	45		
Gain at 26 GHz, at P_{1dB} (dB)***	12	12	14	14	16	16	16		
P_{out} at 94 GHz and peak efficiency (mW/mm)	300	300	350	350	350	350	350		
Peak efficiency at 94 GHz (%)	15	15	20	20	25	30	30		
Gain at 94 GHz, at P_{1dB} (dB)***	5	5	6	6	6	7	7		
*Device Technology—FET **									
InP HEMT (low noise)									
Gate length (nm)	100	100	70	70	70	50	50		
F_t (GHz)	210	210	240	240	240	260	260		
Breakdown (volts)	3.5	3.5	3	3	3	2.5	2.5		
I_{max} (ma/mm)	700	700	650	650	650	600	600		
G_m (S/mm)	1	1	1.2	1.2	1.2	1.3	1.3		
NF (dB) at 26 GHz, 20–23 dB associated gain	1.8	1.8	1.5	1.5	1.5	1.3	1.3		
NF (dB) at 94 GHz, 10–13 dB associated gain	2.5	2.5	2	2	2	1.8	1.8		

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
InP HEMT (power)									
Gate length (nm)	**150**	**100**	**100**	**100**	**70**	**70**	**70**		
F_{max} (GHz)	**200**	**220**	**260**	**260**	**260**	**300**	**300**		
Breakdown (volts)	**5**	**5**	**6**	**6**	**6**	**7**	**7**		
I_{max} (ma/mm)	**750**	**700**	**650**	**650**	**650**	**650**	**650**		
G_m (S/mm)	**0.8**	**0.9**	**0.9**	**0.9**	**1**	**1**	**1**		
P_{out} at 26 GHz and peak efficiency (mW/mm)	**400**	**400**	**450**	**450**	**450**	**500**	**500**		
Peak efficiency at 26 GHz (%)	**30**	**40**	**50**	**50**	**50**	**55**	**55**		
Gain at 26 GHz, at P_{1dB} (dB)***	**12**	**14**	**15**	**15**	**16**	**16**	**16**		
P_{out} at 94 GHz and peak efficiency (mW/mm)	**250**	**300**	**350**	**350**	**400**	**400**	**400**		
Peak efficiency at 94 GHz (%)	**25**	**40**	**40**	**45**	**45**	**45**	**45**		
Gain at 94 GHz, at P_{1dB} (dB)***	**6**	**8**	**10**	**10**	**12**	**12**	**12**		
GaAs MHEMT (low noise)									
Gate length (nm)	**100**	**100**	**100**	**70**	**70**	**50**	**50**		
F_t (GHz)	**200**	**250**	**300**	**300**	**400**	**400**	**450**		
Breakdown (volts)	**5**	**5**	**5**	**4**	**4**	**3**	**3**		
I_{max} (ma/mm)	**680**	**680**	**680**	**680**	**680**	**680**	**680**		
G_m (S/mm)	**1**	**1**	**1.1**	**1.1**	**1.2**	**1.2**	**1.2**		
NF (dB) at 26 GHz, 10–23 dB associated gain	**1.6**	**1.6**	**1.2**	**1.2**	**1**	**1**	**0.8**		
NF (dB) at 94 GHz, 10–13 dB associated gain	**2.5**	**2.3**	**2.3**	**2**	**2**	**1.8**	**1.8**		
Device Technology—FET *									
GaAs MHEMT (Power)									
Gate length (nm)		**150**	**150**	**100**	**100**	**70**	**70**		
F_{max} (GHz)		**200**	**250**	**275**	**300**	**300**	**300**		
Breakdown (volts)		**8**	**8**	**9**	**9**	**10**	**10**		
I_{max} (ma/mm)		**650**	**700**	**750**	**800**	**800**	**850**		
G_m (S/mm)		**0.75**	**0.8**	**0.85**	**0.9**	**0.95**	**1**		
P_{out} at 26 GHz and peak efficiency (mW/mm)		**600**	**650**	**700**	**750**	**800**	**850**		
Peak efficiency at 26 GHz (%)		**45**	**55**	**55**	**60**	**60**	**65**		
Gain at 26 GHz, at P_{1dB} (dB)***		**12**	**15**	**16**	**16**	**16**	**17**		
P_{out} at 94 GHz and peak efficiency (mW/mm)		**250**	**300**	**325**	**350**	**400**	**450**		
Peak efficiency at 94 GHz (%)		**25**	**30**	**35**	**40**	**45**	**45**		
Gain at 94 GHz, at P_{1dB} (dB)***		**7**	**8**	**10**	**10**	**11**	**12**		
GaN HEMT (low noise)									
Gate length (nm)			**150**	**100**	**100**	**70**	**70**		
F_t (GHz)			**100**	**100**	**120**	**150**	**200**		
Breakdown (volts)			**40**	**40**	**40**	**40**	**40**		
I_{max} (ma/mm)			**1000**	**1200**	**1500**	**1500**	**1500**		
G_m (S/mm)			**0.3**	**0.4**	**0.5**	**0.5**	**0.5**		
NF (dB) at 26 GHz, 14 dB gain			**2**	**2**	**1.5**	**1**	**0.8**		
GaN HEMT (power)									
Gate length (nm)			**150**	**100**	**100**	**70**	**70**		
F_{max} (GHz)			**100**	**100**	**150**	**200**	**200**		
Breakdown (volts)			**40**	**60**	**80**	**100**	**100**		

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
I_{max} (ma/mm)			1000	1000	1000	1500	1500		
G_m (S/mm)			0.3	0.4	0.5	0.5	0.5		
P_{out} at 26 GHz and peak efficiency (mW/mm)			5000	6000	7000	8000	10000		
Peak efficiency at 26 GHz (%)			35	40	50	60	60		
Gain at 26 GHz, at P_{1dB} (dB)***			10	12	12	13	14		
P_{out} at 44 GHz and peak efficiency (mW/mm)			2000	2000	2000	2500	2500		
Peak efficiency at 44 GHz (%)			35	35	35	40	40		
Gain at 44 GHz, at P_{1dB} (dB)***			8	8	8	9	9		
*Device Technology—HBT **									
InP HBT									
Emitter width (nm)	350	350	250	250	150	150	150		
Emitter Area (square microns)	1	0.75	0.75	0.5	0.5	0.4	0.4		
F_t (GHz)	300	300	350	350	400	400	400		
F_{max} (GHz)	300	300	400	400	450	450	450		
Breakdown (BV_{CEO}) (volts)	4	4	4	4	3	3	3		
$I_{max}/\mu m^2$ ($mA/\mu m^2$)	4	5	5	5	7	7	7		
Beta	50	50	50	50	50	50	50		
3 sigma V_{BE} (mV)	40	30	30	25	25	20	20		
Interconnect metal layers	4	4	5	5	5				
Interconnect metal	Al, Au	Al, Au	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu	Al, Au, Cu		
Barrier	PVD	PVD	IMP	IMP	IMP	IMP	IMP		
Wafer diameter (mm)	100	100	150	150	150	150	150		
SiGe HBT									
Emitter Width (nm)	150	140	130	120	100	100	100		
Peak F_t (GHz) B_{bc}=1V	200	230	265	300	350	370	385		
Peak Fmax (GHz)	240	260	300	330	390	410	425		
Breakdown (BV_{CBO}) (volts)	5.3	5	5	4.5	4.5	4.3	4.3		
Breakdown (BV_{CEO}) (volts)	2	1.9	1.8	1.7	1.7	1.7	1.7		
$I_{max}/\mu m^2$ ($mA/\mu m^2$)	10	11	12	13	14	15	16		
Beta	200	200	250	250	300	325	350		
Nf_{min} at 77 GHz (dB)	5.5	5.1	4.6	4.3	3.9	3.8	3.7		

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



* *Lithography dimensions are drawn dimensions.*
** *Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*
*** *P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

The bubble charts of Figures 46, 47, and 48 portray the projected technology trends among the various device types over the near term. In Figure 46 the PHEMT bubble represents the noise figure versus frequency for devices commercially available today. While PHEMTs are the mainstay of low noise devices in the mm-wave spectrum at present, we expect that they will be replaced for defense applications in the near term with InP HEMTs and eventually by the end of the decade with MHEMTs. Also, InP HEMTs for defense applications are expected to replace MESFETs. This projection is exhibited by the InP HEMT/MHEMT bubble region that portrays the region in the noise figure (NF) versus frequency realm of reported research results through 2005. Current R&D results project future commercial trends. Not only do InP HEMTs and MHEMTs exhibit lower noise figures, but also the required DC power dissipation is roughly one-quarter of the dissipation for equivalent NF and gain performance.

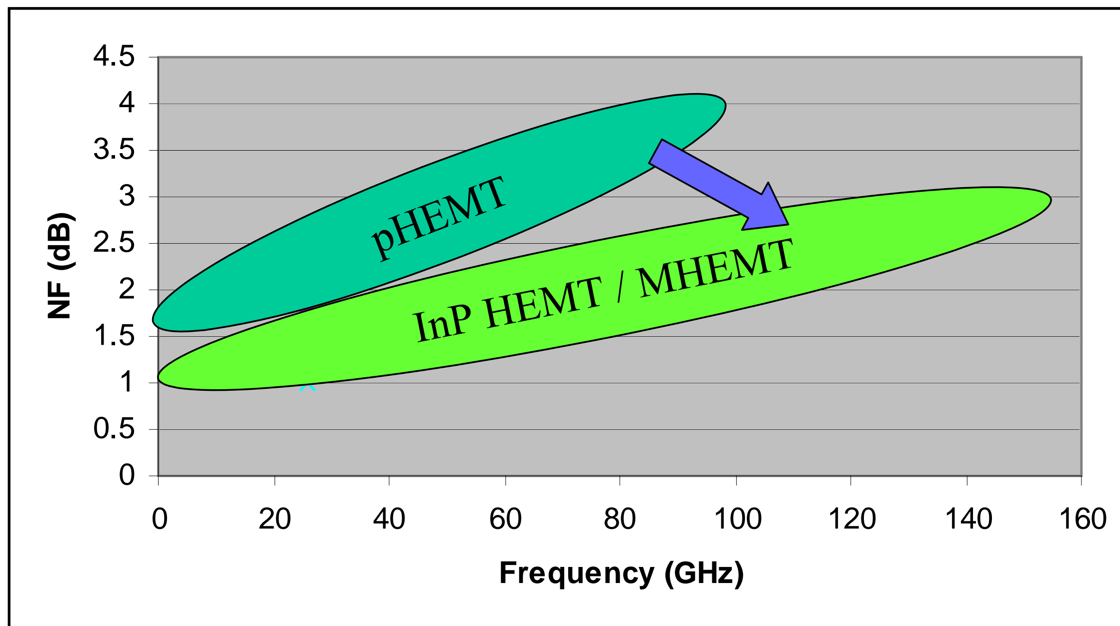


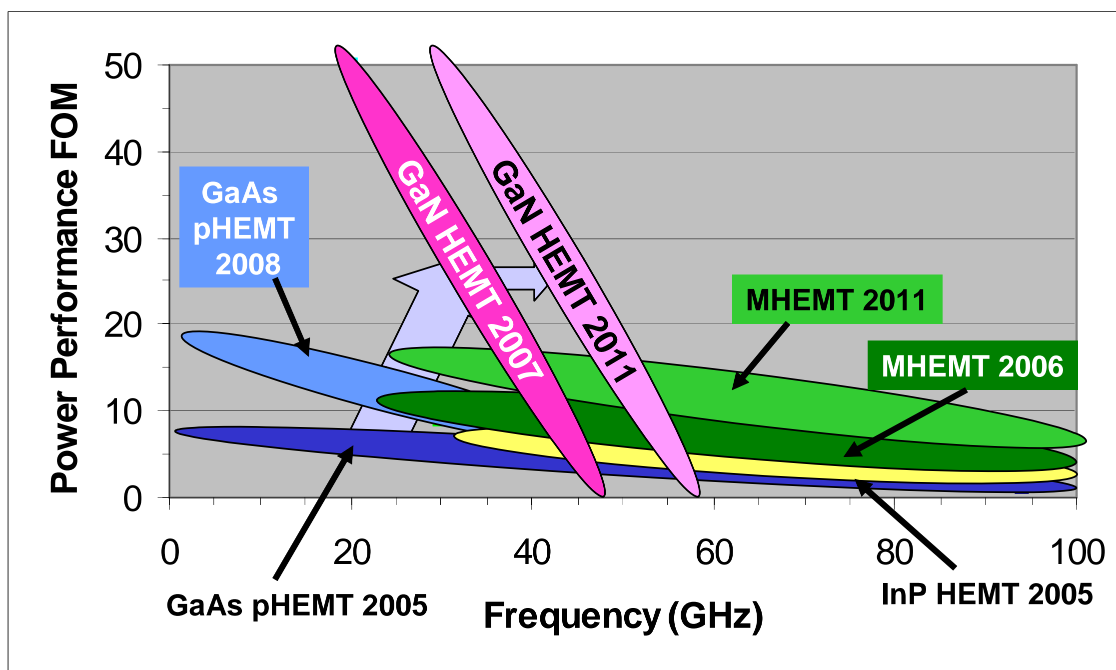
Figure 46 Low Noise Amplifiers Technology Positioning 2006–2011

Figure 47 shows the evolution of millimeter wave power performance over time. The power performance figure of merit (FOM) is MMIC power density (W/mm) times MMIC small signal (SS) gain per stage (dB) at application center frequency for a typical 10–20% bandwidth. The power bandwidth product for the different device technologies could have also been used and would have provided a similar trend. GaAs PHEMT and InP HEMT are the premier millimeter wave power devices available today in production, with GaAs PHEMT the preferred technology for frequencies less than 77 GHz. However, present day GaAs PHEMT and InP HEMT do not have the power performance to meet future systems requirements and continued technology evolution will be required to meet evolving demands.

When engineering a mm-wave power device, the engineer is faced with a dilemma. Increased power (or power density) necessitates operating devices either at higher operating voltages or high current densities. For a given device technology, in addition to the trade-off between operating voltage and current density, increasing operating voltage comes at the expense of high frequency operation or gain. As an example, GaAs PHEMTs that can operate at higher voltages compared to InP HEMTs tend to be gain-limited in the upper mm-wave frequency range. On the other hand, today's InP HEMTs that have superior high frequency gain are limited to low voltage (and subsequently low power) operation. The challenge for the device engineer is to develop a device structure that combines the best attributes of both GaAs PHEMTs (higher voltage operation) and InP HEMTs (high frequency gain).

One approach currently gaining headway is MHEMT technology, which takes advantage of bandgap engineering to create a device structure that exhibits the best compromise between the relatively high voltage operation of GaAs PHEMTs and the high gain of InP HEMTs. As shown in Figure 47, we expect power MHEMT technology to eclipse both GaAs PHEMT and InP HEMT performance in the 40 GHz to 100+ GHz frequency range and to be available for production in the 2006 timeframe.

Another promising approach is the wide bandgap semiconductor GaN. GaN HEMTs have exhibited at microwave frequencies five to ten times the power density of GaAs PHEMTs. GaN HEMTs achieve this revolutionary power performance through a combination of high current density and significantly higher operating voltage with only modest reduction in gain compared to GaAs PHEMTs. Assuming continued development within the next five years, it is projected that GaN HEMTs will become the premier and preferred device technology for mm-wave power applications, perhaps for frequencies as high as Q band frequencies.



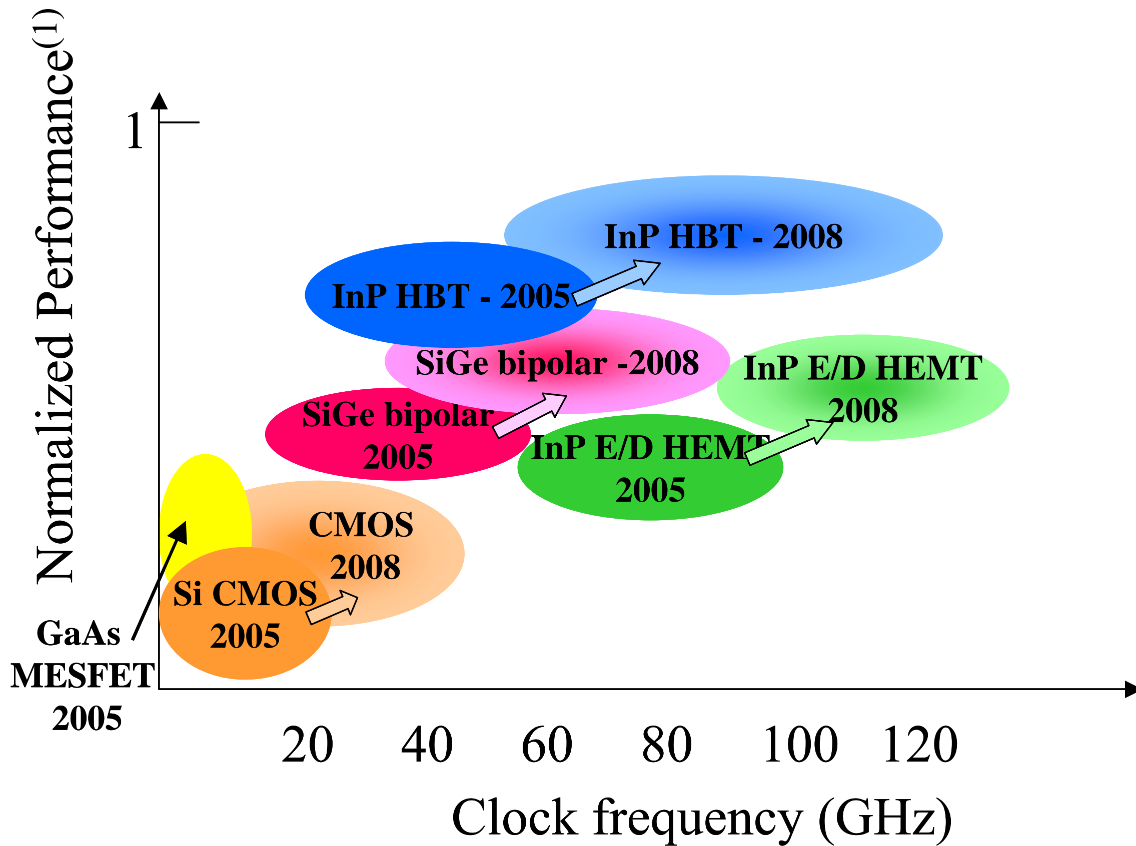
Performance figure of merit is MMIC power density (W/mm) times MMIC SS gain per stage (dB) at application center frequency (typically 10% – 20% bandwidth).

Figure 47 Evolution of Production Power Devices 2005–2011

Figure 48 shows the evolutions of mixed-signal technology for mm-wave applications. Such applications are driven by high center frequency, precise transistor matching, low noise operation, and high linearity in the under lying technology. With continuous scaling, CMOS technology is expected to address low-resolution circuits up to 10 GHz to 20 GHz. SiGe bipolars have extended this to 40 GHz, with more advanced SiGe bipolars beginning to push silicon performance out to 77 GHz, but CMOS technology will likely be limited in dynamic range because its breakdown voltage (BV_{CEO}) is less than 2V. InP HBTs are the ultimate performance technology once the core transistor technology is aggressively scaled. InP HBTs will be limited by substrate size that is now typically at 100 mm; but 150 mm wafers are being sampled. InP HEMT and GaAs MHEMT enhancement and depletion (ED) mode technology HEMTs offer higher frequency operation than InP HBTs when scaled to sub 0.1 micrometer.

ED mode HEMT technology also consumes lower power than the HBT alternative, but the threshold voltage control of the HEMT is not as good as the junction control turn-on of the HBT. The HEMT also does not have as good 1/f noise performance as the HBT.

For applications where high dynamic range is required (e.g., automotive radar), bipolar devices are often preferred due to their high linearity and low 1/f noise. The market force for advanced mixed-signal circuits will most likely drive increased wireless communications bandwidth through the real time correction and synthesis of analog signals using digital technologies. To do this, the associated digital and mixed-signal circuits must run three to ten times faster than the analog carrier frequency. While InP HBTs are predicted to operate at clock frequencies approaching 100 GHz in the near term, this technology is currently finding a niche at clock rates lower than 60 GHz where the combination of dynamic range (breakdown voltage) and high speed is required and cannot be met with SiGe. Additional opportunities exist for performing the control and routing in optical networks.



The metric for performance depends on the class of circuit. It can include dynamic range, signal-to-noise, bandwidth, data rate, and/or inverse power.

Figure 48 Mixed-signal/Ultra High-speed Digital

POTENTIAL SOLUTIONS

The 2005 potential solutions tables are divided into two main tables: one covering the 0.8 GHz–10 GHz applications and one covering 10 GHz–100 GHz mm-wave applications.

ISOLATION

As the integration density and the operation frequency increase, protection of noise sensitive analog circuits from "noisy" digital circuits will become increasingly difficult. Signal isolation is managed through a combination of substrate (e.g., high resistance), interconnect, and package solutions. Today, oxide isolation, guard rings, and buried wells (triple wells) protect circuit blocks. In the future, integrated shielding structures may be required to protect circuits and interconnects. Novel design architectures also may be employed to enhance circuit signal-to-noise performance.

As signal isolation becomes more critical for modern communication systems, a grand technique, which universally resolves different types of signal isolation issues, becomes more urgent. But, developing such a grand technique is not likely. So instead, specific solutions for certain types of noise coupling must be identified and applied. The spectral distribution of the noise significantly affects its impact on circuits. Signal isolation techniques that selectively filter the noise spectrum are cost-effective and power-effective. Any cost-effective solution addressing these problems and challenges must be compatible with the mainstream CMOS technology of the time. The Potential Solutions Table contains some analog and mixed-signal solutions for signal isolation.

RF AND AMS CMOS

In this sub-section, the potential solutions to the challenges in mixed-signal are discussed. The solutions here differ from those already reviewed for memory and logic discussed in sections of the *Process Integration, Devices, and Structures (PIDS) Chapter*. Successful mixed-signal technologies will leverage the baseline digital platform while integrating value-added features and functions. Key ingredients to successful mixed-signal integration are the addition of special higher-voltage analog precision transistors, high quality passive elements, adequate signal isolation, and compatible active devices.

With the steady improvement in high-frequency performance and decrease in speed-power product of CMOS, this technology will gain on traditional BiCMOS and bipolar implementations. Increased CMOS digital performance results in an aggressive roadmap for NF, F_t and F_{max} improvement. In addition to the obvious benefits of increased performance with scaling, technology changes may improve other device characteristics important to RF and analog circuit function. The introduction of metal gate electrodes, high permittivity gate dielectrics, and fully depleted, double-gated SOI will pose additional challenges for mixed-signal applications. Although thermal and floating-body effects and high-resistive substrate connections pose challenges, routine production of SOI microprocessors, high performance I/O interfaces, and high frequency phase-locked loop circuits demonstrate the potential for use in other analog applications. The introduction of metal gates may reduce threshold mismatch due to variations in gate doping and will increase F_{max} due to decreased gate resistance. The introduction of channel strain to increase device current should enable improvements in precision analog and RF driver performance with little or no degradation in other characteristics. Fully-depleted, dual-gate SOI has low channel doping relative to conventional CMOS structures and so may have reduced mismatch. In addition, this structure will offer reduced drain conductance with an attendant increase in voltage-gain and F_{max}. The multiple threshold voltages that enable optimization of digital power-delay will also offer design options for mixed-signal and RF applications.

The mixed-signal supply voltage continues to lag that of high-performance digital by two or more generations. A combination of multiple gate oxide thickness, multiple thresholds, and DC-DC conversion is needed to support the increased mixed-signal requirements. Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to extend the trend for lower supply voltages for mixed-signal applications. An alternative to full integration is the SIP that combines circuits made with different technologies and optimized for the desired functions. We expect that full-digital implementations in CMOS will replace most analog functions except for analog-to-digital conversion (ADC).

Good matching characteristics are critical for mixed-signal devices and for successful design of digital latches and static memory elements. Active circuit compensation techniques will compensate for the degradation of matching characteristics with device scaling.

Present scaling trends will result in substantially degraded voltage-gain even at relatively long channel lengths due to the dominant effect that pocket implants have on the variation of device threshold with drain bias. This will slow the increase in F_{max} and require additional power dissipation in analog circuits. This trend can be slowed by the introduction of asymmetric devices with no pocket implant at the drain end. In addition, the RF roadmap will drive the need for integration of asymmetrical devices (drain extensions) to increase the voltage handling capability of CMOS drivers and power management devices and possibly the use of laterally diffused channels to improve performance of high voltage devices (LDMOS).

RF AND AMS BIPOLAR DEVICES

Along with RFCMOS, SiGe has established itself as one of the key technologies of choice for cellular receivers. Its superior noise figure, gain characteristics, and state of the art 1/f noise properties allow extremely efficient and compact receiver block designs. Bipolar performance shows an aggressive roadmap for the F_t and F_{max} improvement. This improvement will be accomplished up to an F_t of about 300 GHz for bipolar devices by techniques that continue to push both vertical and lateral scaling. Vertical scaling is likely to be accomplished with evolutionary improvement in current equipment and techniques and the addition of carbon doping. Beyond F_t of about 300 GHz, it is likely that more advanced epitaxial techniques will be required, such as atomic layer epitaxy. Beyond an F_t of about 400 GHz, it is likely that additional materials and dopants will need to be introduced. Lateral scaling will borrow heavily from techniques being adopted for digital CMOS and is not likely to add any more requirements than those for scaling of digital CMOS.

PASSIVES

The trend of moving discrete passive elements from board level to chip level will continue. Solutions for achieving discrete-equivalent precision on-chip passive components are expected. Alternatively, some passives may be integrated into the printed board or package as a method of cost reduction and simplification. New high-k dielectrics can be used either to reduce integrated capacitor area or to keep the integrated capacitor area acceptable for new emerging analog and RF circuit functions. The high-k dielectrics can significantly increase the capacitance density of the MIM capacitor, MOS capacitor, and MOS varactor. The continued improvement and performance verification in linearity and matching of metal-oxide-metal (MOM) capacitor will make it an attractive low cost option for future analog and RF circuits.

Higher quality and higher density inductors can enable new functionality and circuit topology integrated on-chip and represents a significant challenge for analog and RF integrated circuits. Potential solutions for higher quality and higher density inductors include the use of thicker layers of Cu and thicker top dielectrics and the integration of magnetic materials with on-chip inductors. These may co-exist with inductors integrated in the package for the most demanding applications. Integrated resistors need low parasitic capacitance and high temperature linearity, which can be fulfilled by innovative approaches in fabrication of the integrated resistors.

Further research is needed on MOS capacitors and MOS varactors processed with high-k dielectrics. These are coupled to the availability of high-k dielectrics, respectively, for analog high precision transistors and high-speed RF transistors. The impact on the VCO phase noise of the high-k dielectric, which typically has a much higher trap density, needs sufficient research.

In order to achieve high capacitance density for RF MIM capacitors, various high-k dielectrics are being explored. This includes Ta_2O_5, HfO_2 and other high-k materials.

The key challenge is to keep the leakage current and voltage linearity low as the film thickness is reduced. One way to solve this tradeoff is to use multi-layered structures where the capacitance density and voltage linearity can be separately optimized. Whether such solutions are production worthy is yet to be seen.

When feature size is scaled down and when the stacking structure or the high-k dielectric MIM is excluded, the unit capacitance of the inter-digitated, lateral MOM capacitor can be close to or exceed that of the standard MIM capacitor. Compared with the MIM capacitor, there are no additional processing steps and cost for the inter-digitated MOM capacitor. Therefore, it is recognized as a capacitor option, especially for low-cost applications. There are tradeoffs observed between the unit capacitance and the parasitic coupling with the Si substrate. Moreover, the mismatching performance of the interdigital MOM capacitor can't be over-emphasized. However, the mismatching performance of the inter-digitated MOM capacitor can be competitive to that of the MIM capacitor by using proper structure designs.

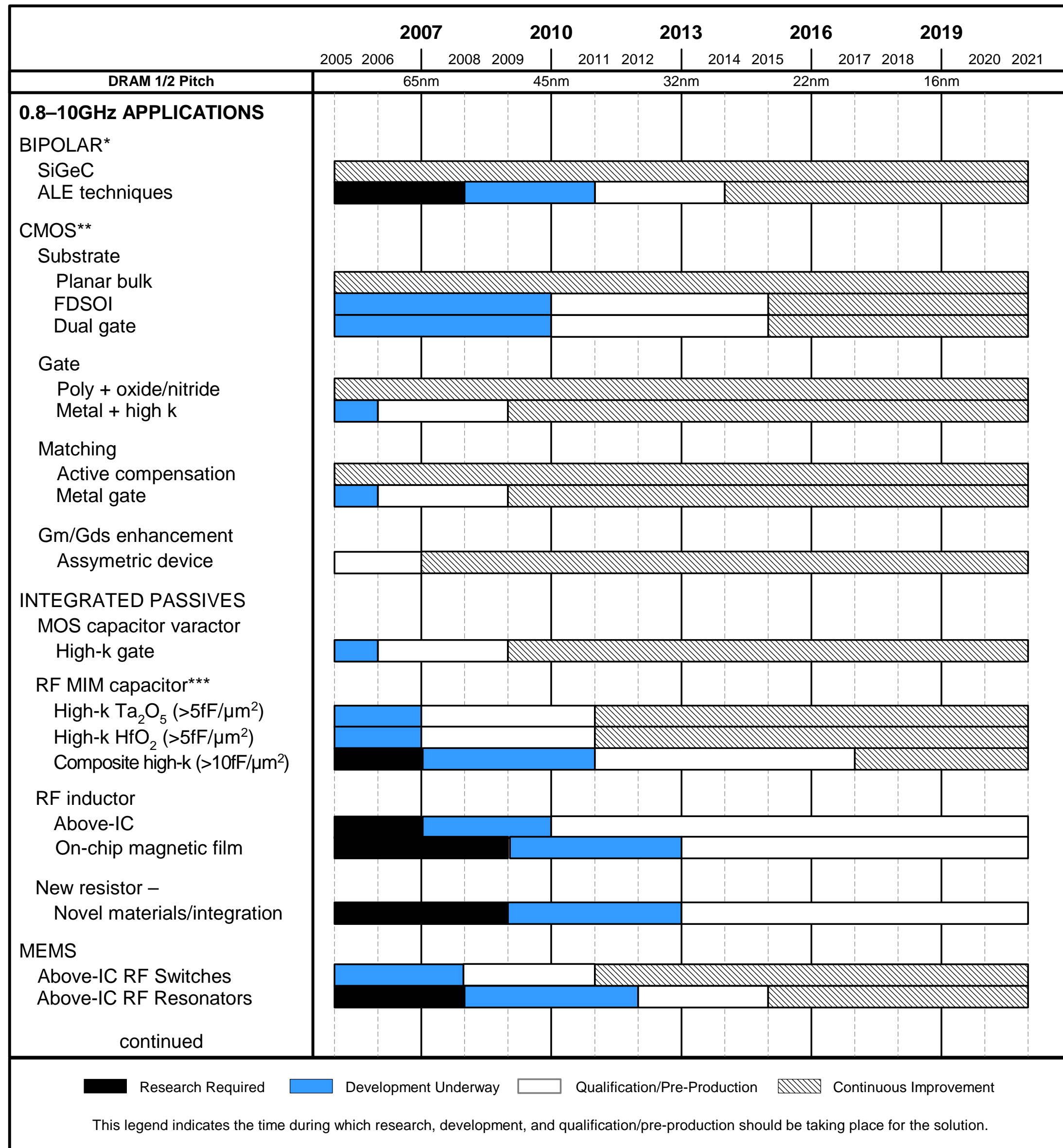
Above-passivation inductors offer high Q-factors and resonance frequencies, but require special processing. Technical feasibility has been demonstrated. Some companies have this available as a production process. The choice whether to use above-passivation inductors depends on the limited access today to such technology and the economics. The latter is assessed on a case-by-case basis. Improvements in inductance density are difficult to realize. Solutions of stacking inductors have been proposed, but add significantly to the cost and jeopardize the resonance frequency due to the high capacitive coupling between the stacked inductors. The use of magnetic materials has received some attention in the literature, such as the use of magnetic shields. However, the research in this area is not yet complete.

Increasing CMOS complexity makes it more difficult to produce stable, highly manufacturable front-end-of-line (FEOL) resistors. One solution to this problem is to provide high-resistance BEOL resistors comparable to the common p-type polysilicon resistors in the FEOL. Due to thermal affects, this can be a problem because thermal control of these devices is paramount in the BEOL to minimize electromigration. This problem needs to be addressed with new materials that provide not only good resistor parametrics for RF and analog circuits but good thermal control at high currents. This is a good area for R&D on RF and analog technologies.

POWER AMPLIFIERS

At this time, InP-based HBTs devices do not appear to have found a niche for power amplifiers below 10 GHz. However, with the continued drive for higher efficiency output stages in handsets and new applications at high frequencies, InP HBTs will become more attractive for their performance advantages in these areas. The broadband business appears to be more than adequately covered by SiGe HBTs that are actually ahead of current bandwidth requirements. If the frequency of operation for commercial radios greatly increases, then the need for InP devices will also increase.

Since the module footprint is continually decreasing while the module complexity is continually increasing, a technology capable of integrating more of the radio functions will ultimately be the technology of choice. This approach is primarily to reduce the total number of chips in a module. Two of these RF functions are filters and transmit receive (T/R) switches. If MEM switch reliability improves and their voltage requirements decrease, they can potentially offer a post-processing integration solution for both GaAs and Si technologies. Integration of filter functions also presents a challenge for inclusion in a semiconductor technology. To date, only filter bulk acoustic resonator (FBAR) technologies and MEMs resonators have appeared as possible candidates for integration.



Notes for Figure 49
** Bipolar use mainly in transceiver*
*** CMOS use in transceiver and AMS*
**** Meeting passive roadmap density and leakage w/Cu backend*

Figure 49 0.8–10 GHz Potential Solutions

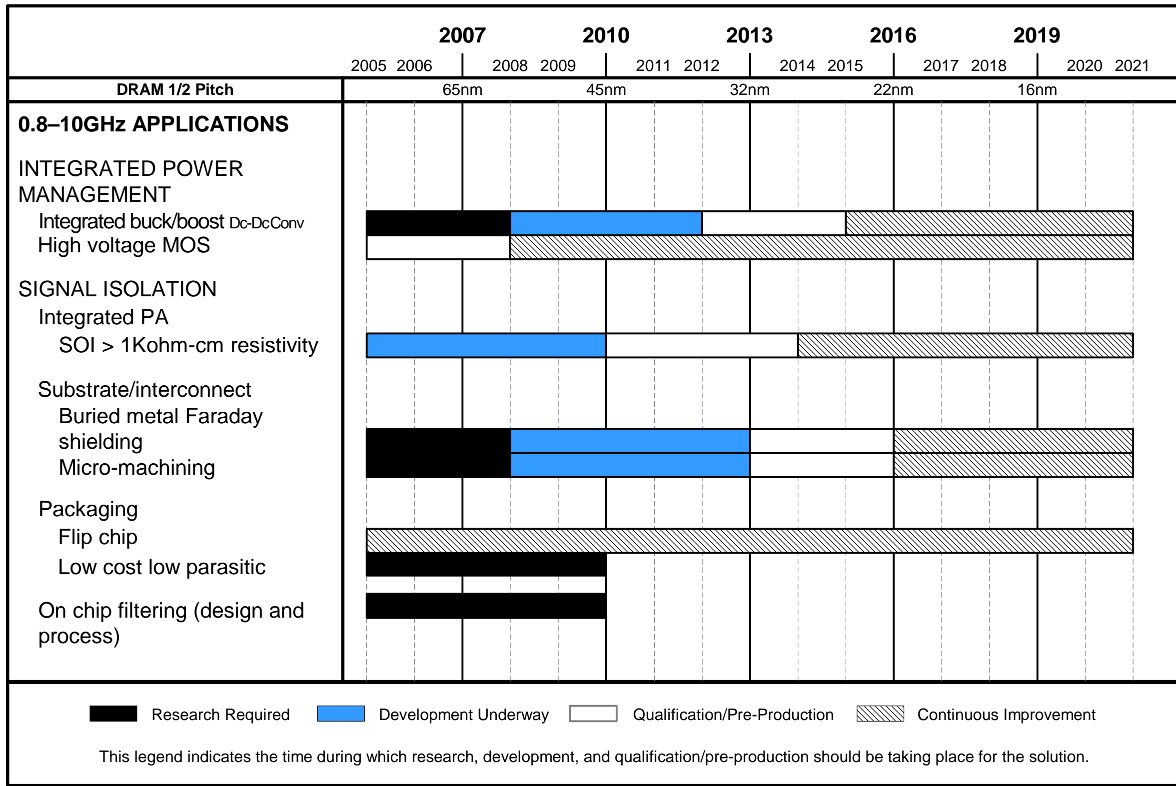


Figure 49 0.8–10 GHz Potential Solutions

MILLIMETER WAVE

Compound semiconductors must take advantage of the advances in lithography and processing equipment that are evolving now in the digital silicon industry. In order to accomplish this, wafer diameter needs to be within one or two generations of the silicon industry. Six-inch semi-insulating GaAs wafers are in production now with InP not far behind. However, the III–V industry needs to continue to push to larger wafer sizes as silicon transitions from eight to twelve-inch diameter wafers. While significant advances are being made in optical lithography tools, the cost of masks is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beam is a solution to the mask cost, but wafer through-put, which is measured in hours per III-V wafer as compared to silicon wafers per hour, needs to be increased with high current electron sources and fast alignment systems.

Uniformity, reproducibility and yield metrics for compound semiconductors lag behind Si based technologies. This is not surprising, given the much higher investment in infrastructure and research for silicon, as well as the extremely large disparity in production volume between the two. Nevertheless, as production volume in a particular compound technology rises, unit costs are found to decrease on a learning curve not unlike that of silicon.

Substrate quality is still problematic for the emerging wide bandgap devices. Research on GaN templates is continuing, but in the interim, SiC substrates will become more viable as their defect density decreases. If SiGe is to challenge other technologies for the mm-wave spectrum, then high resistivity low-loss silicon needs to be addressed.

Thermal dissipation is the major challenge for wide-bandgap III-V power devices. While GaN and SiC substrates have higher thermal conductance values compared to GaAs and InP, the 5–10× higher power densities typically present in these wide bandgap semiconductors somewhat offsets the advantage in higher thermal conductance. These circumstances make thermal dissipation a critical device design aspect. Proven techniques include thin [0.002-inch] wafers, thermal shunts, and bathtub vias. These techniques and more innovative solutions need to be applied to the wide bandgap devices.

High voltage breakdown is desirable for both mixed-signal and high-power devices. As dimensions decrease for higher frequency performance, the operating voltage suffers. This is particularly troublesome for mixed-signal devices that

require more headroom for the analog functions than for the digital functions. In this regard, InP HBTs offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe will be orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs. For power FETs, gate recessing has been used successfully to achieve higher breakdown, but this has yet to be applied to GaN. Tailoring of the vertical dimensions of the source-drain region to optimize the surface electric fields is a potential solution. Continued improvement of passivation and hot carrier effects is also needed.

Finally, high frequency performance in III-Vs is driven as much by epitaxy (vertical scaling) as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by proper engineering of the epitaxial layer stack and continued improvement in all of the III-V devices can be expected through bandgap engineering.

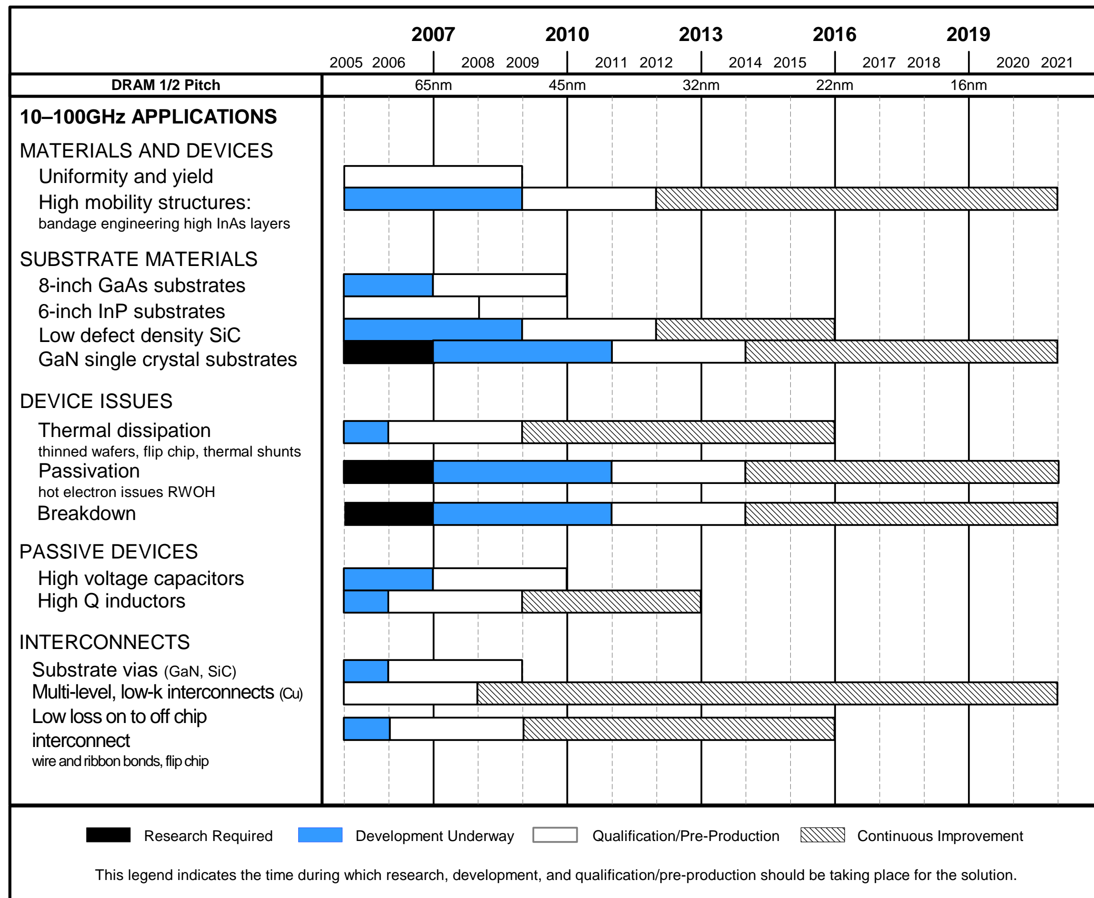


Figure 50 10–100 GHz Potential Solutions

CROSS-CUT ITWG ISSUES

Key crosscutting and liaison issues with other ITRS international technology working groups (ITWGs) are outlined below. The issues listed typically concern combinations of analog and mixed-signal devices, RF transceivers, power amplifiers, power management, and mm-wave technologies.

ASSEMBLY AND PACKAGING

- Assembly and Packaging led module roadmap that includes substrates and embedded passives
- Opportunities to include MEMs, bulk acoustic wave (BAW), switch and antenna in wireless roadmap

- Plastic packages for base station PAs, mm-wave packaging, thin packages and modules
- Thermal management

EMERGING RESEARCH DEVICES

- Analog and RF functions and performance with novel structures

FRONT END PROCESSES AND INTERCONNECTS

- Low inductance ground connection
- Suppressing electrical interference and cross-talk and increasing signal isolation
- High-Q inductors
- Substrates with low and high resistivities

MODELING AND SIMULATION

- Accurate, fast and predictive analog and RF compact models
- Computationally efficient physical models for carrier transport in compound semiconductors
- Efficient 3D modeling and simulation for mixed signal circuits
- Thermal modeling and simulations that are integrated with RF and digital design tools

SYSTEM DRIVERS AND DESIGN

- RF module and SIP drive the need for chip and package co-design, that is, radio SIP design flow
- Build cross-talk immune circuits for SOC and SIP integration

TEST

- RF, analog, and digital test for SOC system
- Reduced costs for testing RF circuits that have several functions and very high frequencies

FUTURE EMERGING RESEARCH DEVICES

Because there are few confirmed reports in the open literature of technical data on the RF and analog performance of emerging research devices, the working group cannot assess the impact of emerging research devices on RF and analog performance. Emerging research devices such as resonant tunneling devices, spin transistors, carbon nanotubes, molecular electronics, planar double-gate transistors, and 3D structures including vertical transistors are expected to present RF and AMS challenges and may also present opportunities for RF and AMS applications that demand increased performance, reliability, and functionality.

A common technical challenge for most, if not all, RF and AMS applications of emerging research devices is to understand the chemistry and physics of the electrical contacts well enough so that the RF and AMS properties are controlled and reproducible in high volumes. Also, the impacts on figures of merit such as 1/f noise, power added efficiency, linearity, bandwidth, gain, ruggedness, reliability, and signal isolation are not known. Measuring and determining the impact on figures of merit will present new areas for significant research and development. This research will exploit the additional degrees of engineering freedom that many emerging research devices offer. Two examples of additional degrees of engineering freedom are 1) controlling independently the voltage of multiple-gated devices, and 2) using an electric field applied perpendicularly to the axis of carbon nanotubes to alter their band structures.

Recent RF measurements up to 12 GHz on back-gated carbon nanotube field effect transistors (BG-CNT FETs) show that today's contact pad parasitics are very large and may be potential showstoppers and roadblocks for deploying millions to trillions of such molecular devices. Device simulations when contact pad parasitics are not included suggest good transmission properties at frequencies above 1 THz. Removing parasitics in device simulations is easy, but reducing parasitics in the laboratory is an extreme challenge. Decreasing the 100-fold difference between theory and practice for the RF performance of emerging research devices will require improved RF measurements and advanced materials research on RF contacts at the nanoscale. The conventional transmission line RF circuit models for trying to understand RF properties of emerging research devices are based on continuum concepts and may not give the optimum design strategies for improving RF performance, especially when considering the very process dependent contacts. Also, continuum concepts are not expected to be completely valid at the nanoscale. Conventional S matrix and impedance Z measurements are not appropriate for most emerging research devices, such as BG-CNT FETs, because the contacts

greatly disturb the current paths. For example, in the conventional four-probe methods to measure DC resistance, most of the electrons exit the CNT near the middle contact regions. Extracting the resistance of the entire CNT for a four-probe method becomes too convoluted. Additionally, the RF properties of contacts are problematic. RF contact parasitics are great and cause the F_t for RF CNTs to drop from the theoretical F_t of more than 1 THz to the experimental F_t of about 10 GHz or less.

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