INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

YIELD ENHANCEMENT

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YIELD ENHANCEMENT

SCOPE

Yield Enhancement (YE) is defined as the process of improving the baseline yield for a given technology generation from R&D yield level to mature yield. The definition assumes a functional baseline process for a given process technology and it's compatibility with the design of the product being fabricated. The definition reinforces the chapter focus on the yield ramp portion of the yield learning curve. The YE chapter scope is limited to wafer sort yield. The YE chapter does not address fab line yield, assembly/packaging yield, and final test yield.

The Yield Enhancement Chapter is partitioned into four focus topics: Yield Model and Defect Budget, Defect Detection and Characterization, Yield Learning, and Wafer Environment(s) Contamination Control. Key business metrics rely on the success of rapid yield ramp and the associated competencies found within these four focus topics, particularly with the introduction of 300 mm manufacturing. These competencies crosscut all process technologies, as well as the facility infrastructure, integrated circuit (IC) design, and process integration. Key messages include continued emphasis on reduction of process- and equipment-generated defects to meet defect targets for mature product yields. Significant efforts will be necessary to baseline, reduce and control yield loss associated with systematic mechanisms. Defect-to-fault and fault-to-defect mapping, kill ratios, and failure isolation techniques are also critical challenges as physical device dimensions and corresponding defect dimensions continue to shrink. There must be renewed development of defect detection, review, and classification technologies where much greater sensitivity and throughput is necessary. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and work-in-progress (WIP) data, will have to be developed to enable rapid yield learning. Specific recommendations are needed for standard monitor-wafer preparation, detection recipes, edge exclusion, test structures, short/long loops and sampling to ensure line control and yield improvement. Global, order-of-magnitude improvements in process critical fluid and gas impurity levels are not believed to be necessary in the foreseeable future. New materials and their precursors, however, introduce challenges that require continuous study.

Clarification of potential contamination from point-of-supply to point-of-process will define control systems necessary for delivered purity. There are several locations in the pathway from the original delivery package, i.e., the point of supply (POS) of a liquid or gas to the location where that material contacts the wafer, i.e., the point of process (POP), for ascertaining purity. This has led to a considerable amount of confusion and ambiguity in discussing the quality of process fluids, including the data found in Table 115. Table 108 summarizes the major fluid handling and/or measurement nodes found along the typical systems supplying process fluid. This table is an effort to create a common language for the discussion of attributes and requirements at these different node points. Further information regarding pathway nodes can be found in the supplementary materials and references, such as the Semiconductor Equipment and Materials International (SEMI) Standards.

Table 108 Definitions for the Different Interface Points

	POS *Delivery Point of Gas/Chemical Supplier*	*POD* *Outlet of Central Facility System*	*POC* *Submain or VMB/VMP Take off Valve*	*POE* *Entry to Equipment or Sub Equipment*	*POU* *Entry to the Process Chamber*	*POP* *Contact with Wafer*
Interfaces	*SEMI Standards Focus Area*	*ITRS Factory Integration Facilities Group Focus Area*		*ITRS Factory Integration Equipment Group Focus Area*		*ITRS Front End Processes, Lithography, Interconnect TWG Focus Area*
Ultrapure water	Raw water	Outlet of final filtration in UPW plant	Outlet of submain take off valve	Inlet of wet bench	Inlet of wet bench bath, spray nozzle, or connection point to piping, which is also used for other chemicals	Wafer in production
Process chemicals	Chemical drum/tote/bulk supply	Outlet of final filtration of chemical distribution unit	Outlet of VMB valve	Inlet of wet bench or intermediate tank	Inlet of wet bench bath or spray nozzle	Wafer in production
Specialty gases	Gas cylinder or bulk specialty gas systems	Outlet of final filtration of gas cabinet	Outlet of VMB valve	Inlet of equipment	Inlet of chamber (outlet of MFC)	Wafer in production
Bulk gases	Bulk gas delivered on site or gas generator	Outlet of final filtration/purification	Outlet of submain take off valve or VMB valve	Inlet of equipment/ subequipment	Inlet of chamber (outlet of MFC)	Wafer in production
Cleanroom and AMC	Outside air	Outlet of make-up air handling unit	Outlet of filters in cleanroom ceiling	Inlet to mini-environment or sub equipment	Gas/air in vicinity to wafer/substrate	Wafer/substrate in production (AMC/ SMC)

POD—point of delivery POC—point of connection POE—point of entry POU—point of use VMB— valve manifold box VMP— valve manifold post UPW—ultra pure water MFC—mass flow controller AMC—airborne molecular contamination SMC—surface molecular contamination

DIFFICULT CHALLENGES

The difficult challenges for the Yield Enhancement chapter are summarized in Table 109. The signal-to-noise ratio for defect inspection tools was identified by the community as the most important challenge for yield enhancement. Currently inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology generations. Increasing the inspection sensitivity at the same time increases the challenge to find small but yield relevant defects under a vast amount of nuisance, false defects. At the same time a low cost of ownership (CoO) of the tools demands for high throughput inspection. This is in conflict with the issue of improving the signal-to-noise ratio. The key of a successful inspection result is, besides achieved sensitivity, the ease to get to the defects of interest (DOI).

High throughput logic diagnosis capability is the top priority of challenges for the Yield Enhancement chapter. The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows to accommodate, automatic test equipment (ATE) architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

The yield enhancement community is constantly challenged by inline defect characterization and analysis, by wafer edge and bevel control and inspection and by the correlation of process variation and contamination levels to yield.

Inline elemental analysis techniques are required as alternative to energy dispersive X-ray (EDX) analysis systems. The focus of required developments is on light elements, small amount of samples due to shrinking particle size, and increasing importance of microanalysis. SEM/EDS is limited as an inline elemental analysis technique. This is due to several reasons, as follows: 1) EDS is too large for the desired scale; 2) EDS supplies insufficient chemistry information (for example, the lack of chemical state information), and 3) EDS causes e-beam damage as the insulating substrate can cause severe charging, which results in destruction of the scanning electron microscope (SEM) image resolution and

makes it difficult to know if the beam is actually on the particle. This challenge is a crosscut of yield enhancement and metrology issues.

Defects and process problems around wafer edge and wafer bevel can cause yield problems. Currently, the defect inspection of the wafer edge and the bevel as well as the wafer backside is not paid too much attention. Therefore, defect inspection concepts or technologies are either under development or have to be realized within the next few years. It is a key challenge to find the root cause inspection of wafer edge, bevel, and apex on the wafer front and backside.

Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

It will be also a challenge to keep the same yield improved rate (in yield ramp phase form 30% to 70%) in parallel with wafer volume ramp up and the mature yield level (>80%) in volume production. This is particularly true for further deep sub-micron technology generations that involve the introduction of new device structures, materials, and acceleration of yield learning. These will rely not only on high sensitive inline inspection tools for visual and invisible defects, but also powerful electrical failure analysis (EFA) and physical failure analysis (PFA) techniques to identify failure root causes. It is a requirement to enable rapid yield learning and therefore there is the need for efficient data management and test structures, and to develop parametric sensitive yield models. To shorten the feedback loop of defect excursion and yield learning cycle, a yield management system (YMS) that integrates inline metrologies, advance process control (APC), electrical parameters, work station (W/S), and manufacturing execution system (MES) is necessary. The YMS not only can provide the analysis environment for engineers, but also can send out alarm message if inline control parameters are out of control limits.

Table 109 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Signal-to-noise ratio—Increasing the inspection sensitivity at the same time increases the challenge to find small but yield relevant defects under a vast amount of nuisance, false defects. The key of a successful inspection result is, besides achieved sensitivity, the ease to get to the defects of interest (DOI).	Filtering and use of ADC is a potential solution Reduction of background noise from detection units and samples to improve the sensitivity of systems Need to improve signal to noise ratio to delineate defect from process variation Where does process variation stop and defect start?
High throughput logic diagnosis capability—The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window.	Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow Potential issues can arise due to different ATPG flows to accommodate; ATE architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die
Detection of multiple killer defects—Differentiation of multiple killer defect types is necessary at high capture rates, low cost of ownership and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity Reduction of inspection costs is crucial in view of CoO Ability to detect particles at critical size may not exist Detection of line edge roughness due to subtle process variation Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision
High aspect ratio inspection—Need for high-speed and cost-effective high aspect ratio inspection tools remains. The interim approach using e-beam inspection does not meet the requirements for throughput and low cost.	Poor transmission of energy into bottom of via and back out to detection system. To detect rapidly defects at ½× ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches, and especially defects near or at the bottoms of these features Large number of contacts and vias per wafer
Difficult Challenges < 32 nm	*Summary of Issues*
Process stability versus absolute contamination level including the correlation to yield—Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield Define a standard test for yield/parametric effect Definition of maximum process variation (control limits)
Inline defect characterization and analysis—As alternative to EDX analysis systems [1]. The focus is on light elements, small amount of samples due to particle size, and microanalysis.	The sampling probe should show minimum impact as surface damage or destruction of SEM image resolution Supply of information of chemical state and bonding especially of organics is recommended Small volume technique adapted to the scales of technology generations Capability to distinguish between the particle and the substrate signal
Wafer edge and bevel control and inspection—Defects and process problems around wafer edge and wafer bevel can cause yield problems.	Find the root cause inspection of wafer edge, bevel and apex on the wafer front and backside
Rapid yield learning requires efficient data management and suitable test structures—Enabling rapid root-cause analysis of yield-limiting conditions. With increasing process complexity and fewer yield learning cycles with each subsequent technology generation it would be impossible to achieve historic yield ramps and mature yield levels.	Development of automated, intelligent structures, analysis, and reduction algorithms that correlate facility, design, process, test, and WIP data Need of tools and methods for short yield learning cycles
Development of parametric sensitive yield models including new materials—OPC and considering the high complexity of integration. The models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology generations Address complex integration issues Model ultra-thin film integrity issues Improve scaling methods for front-end processes including increased transistor packing density

ADC—automatic defect classification
[1] Cross-link to Metrology chapter

NEEDED RESEARCH

The technology requirements and potential solutions described in this 2005 chapter call for continued cooperation between all stakeholders. For example, tool defect data is needed from semiconductor manufacturers and equipment manufacturers to specify design processes and the required equipment. Innovative algorithms for defect sourcing will be required for rapid yield learning, particularly when the electrical fault has no detectable optical or SEM image.

For high aspect ratio inspection (HARI) applications and at defect sizes below 100 nm (diameter), defect detection and characterization will be hampered by detection tools having low throughput and high cost-of-ownership. An economical solution must be found if the large risk to production inventory is to be avoided.

In order to maintain manufacturing costs while improving yield, contamination control must focus on impact at the point of process. Innovative ideas, such as local removal of undesirable contamination from a re-usable process gas or fluid, must be examined. For new thin-film materials, understanding of purity requirements for deposition chemicals is needed.

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

$$Y_{Die} = Y_S * Y_R = Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha}$$

The overall die yield of an IC process can broadly be described as a product of systematic (or gross) limited yield (Y_S) and random-defect limited yield (Y_R). The defect budget technology requirements defined in Tables 111 and 112 are based on a negative binomial yield model where Y_R is the random-defect limited yield, A is the area of the device, D_0 is the electrical fault density, and α is the cluster factor. Assumptions for the defect budget technology requirements in this revision are indicated in Table 110. The defect budget target calculation for the 2001, 2003 and 2005 Roadmaps are based on results of three studies (1997, 1999, and 2000) of particles per wafer pass (PWP) levels at SEMATECH member companies. These targets were extrapolated from median PWP value per generic process tool type and then scaled to an MPU and a DRAM-generic process-flow, respectively. Note that the defect budget targets for all process steps include wafer-handling defectivity of the process tool. In addition a 10% wafer per lot sampling rate for inspection and measurement was assumed.

$$PWP_n = PWP_{n-1} \times \frac{F_n}{F_{n-1}\left(\frac{S_{n-1}}{S_n} \right)^2}$$

This PWP extrapolation equation was used to calculate PWP budget values for each technology generation. The extrapolation takes into consideration increase in chip size, increase in complexity, and shrinking feature size. In this equation PWP is the particles per wafer pass defect density per square meter, F is the average faults per mask level (determined by the random electrical fault density (D_0) divided by number of masks at a given technology generation), S is the minimum critical defect size, and n refers to the technology generation. All PWP budget values are defined with respect to a certain critical defect size (45 nm for MPU, 40 nm for DRAM). Each entry in the PWP section of Tables 111 and 112 refers to a generic tool type used in the MPU and/or in the DRAM process flow. Since future actual tools and processes are not known, this roadmap assumes that no new process, material, or tool will be acceptable with a larger PWP budget than prior methods. This assumption needs periodic validation. This defect budgeting method tends to be a worst-case model since all process steps are assumed to be at minimum device geometry. In actuality, many processes allow process zones with more relaxed geometries. However, the same tools are used for both minimum and relaxed geometries. The costs of underestimating yield (unused capacity costs) are small and may be offset by the opportunity for additional production. The major driver for increased cost due to overestimating yield is the cost of scrapped material. Thus, a worst-case defect budgeting model is prudent.

Table 110 states the yield and the product maturity assumptions that were used in calculating electrical fault density values and PWP defect budget target values for MPUs and DRAMs, respectively. These assumptions for the most part are as defined in the 2005 *Overall Roadmap Technology Characteristics* (ORTC). Cluster parameter value returned to two from five, because the value two is more appropriate to explain the defect distribution among most fabs. Table 111 presents the random PWP defect budget targets necessary to meet the stated assumptions for a cost-performance MPU as defined in the *ORTC Tables 1a and 1b*. This MPU is assumed to have a small L1 cache, but the device consists primarily of logic transistor functionality. With respect to MPUs, this analysis assumes that the process/design improvement target factor (*ORTC Tables 1g and 1h*) for each technology generation is met. Similarly, Table 112 presents the random PWP

budget targets necessary to meet the yield assumptions stated in Table 110 for DRAMs. The electrical fault density that is used to calculate faults per mask level (which is used as input to the PWP extrapolation equation) is based on only the periphery (logic/decoder) area of the DRAM chip. This is projected in the ORTC to be 37% of chip area at the stated product maturity. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM can implement redundancy to attain the overall yield target of 85%. DRAM chip size is enlarged at the timing of the new generation product introduction, and it shrinks during the period of the same generation product manufacturing as *ORTC Tables 1c and 1d* show. So the DRAM chip size and D_0 fluctuate, but the defect budgets, derived from the chip size, do not fluctuate by adopting smaller value.

The random defect targets in Tables 111 and 112 are based on predefined technology generations, using data collected by SEMATECH member companies on 164 tools, which are divided into 30 generic tool categories. Even with targets for both memory and logic products, rarely do actual user circuit line widths and areas match the ITRS technology assumptions.

Besides continuous improvement in tool cleanliness, there are at least three other major challenges that must be addressed going forward in order to achieve acceptable yields:

1. With systematic mechanisms limited yield (SMLY) dominating the rate of yield learning, a concerted effort is required to understand, model, and eliminate SMLY detractors.
2. The impact of line edge roughness (LER) on yield needs to be understood, modeled and controlled to achieve acceptable yields for current and future technology generations.
3. The issues of particles and defects that are located not only at the front surface of a wafer but also at wafer bevel/edge portion and backside surface needs to be addressed.

Table 110 Defect Budget Technology Requirement Assumptions

Product	*MPU*	*DRAM*
Yield Ramp Phase	*Volume Production*	*Volume Production*
$Y_{OVERALL}$	**75%**	**85%**
Y_{RANDOM}	**83%**	**89.5%**
$Y_{SYSTEMATIC}$	**90%**	**95%**
Cluster Parameter	**2**	**2**

The current Defect Budgets tables are based on the survey that was carried out five year ago, so that the color tiling is not done intentionally in this 2005 revision. It is believed that the defect budgets should be re-calculated by using the latest data that will be corrected through a new survey and procedure by next revision. The Yield Enhancement ITWG will survey semiconductor manufacturing companies for defect control limits of semiconductor manufacturing equipments. Regarding the Yield Model, the Negative Binomial Model has been used. However, another technical area such as Starting Materials and Surface Preparation technologies in Front End Process is using a different model. Therefore, a discussion has been started between YE-ITWG, Starting Material sub-TWG (FEP ITWG) and Surface Preparation sub-TWG (FEP ITWG). Through this discussion, defect models used in ITRS would be unified and the YMDB table will be changed in the next revision.

Table 111a Yield Model and Defect Budget MPU Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted) [A]	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*35*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Critical Defect Size (nm)	**45**	**39**	**34**	**29.5**	**26**	**22.5**	**20**	**18**	**16**
Chip Size (mm^2) [B]	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Overall Electrical D_0 (faults/m^2) at Critical Defect Size Or Greater [C]	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**
Random D_0 (faults/m^2) [D]	**1757**	**2214**	**1395**	**1757**	**2214**	**1395**	**1757**	**2214**	**1395**
Number of Mask Levels [E]	**33**	**33**	**33**	**35**	**35**	**35**	**35**	**35**	**37**
Random Faults/Mask	**53**	**67**	**42**	**50**	**63**	**40**	**50**	**63**	**38**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 45 nm Critical Defect Size or Greater									
CMP clean	**276**	**207**	**157**	**112**	**87**	**65**	**51**	**42**	**31**
CMP insulator	**667**	**501**	**381**	**270**	**210**	**157**	**124**	**101**	**75**
CMP metal	**755**	**567**	**431**	**306**	**238**	**178**	**141**	**114**	**85**
Coat/develop/bake	**120**	**90**	**69**	**49**	**38**	**28**	**22**	**18**	**14**
CVD insulator	**594**	**446**	**339**	**241**	**187**	**140**	**111**	**90**	**67**
CVD oxide mask	**780**	**586**	**445**	**316**	**246**	**184**	**145**	**118**	**88**
Dielectric track	**189**	**142**	**108**	**77**	**60**	**45**	**35**	**29**	**21**
Furnace CVD	**338**	**254**	**193**	**137**	**106**	**80**	**63**	**51**	**38**
Furnace fast ramp	**307**	**230**	**175**	**124**	**97**	**72**	**57**	**46**	**35**
Furnace oxide/anneal	**198**	**149**	**113**	**80**	**62**	**47**	**37**	**30**	**22**
Implant high current	**264**	**199**	**151**	**107**	**83**	**62**	**49**	**40**	**30**
Implant low/medium current	**242**	**182**	**138**	**98**	**76**	**57**	**45**	**36**	**27**
Inspect PLY	**246**	**185**	**140**	**100**	**77**	**58**	**46**	**37**	**28**
Inspect visual	**264**	**199**	**151**	**107**	**83**	**62**	**49**	**40**	**30**
Lithography cell	**205**	**154**	**117**	**83**	**65**	**48**	**38**	**31**	**23**
Lithography stepper	**194**	**145**	**111**	**78**	**61**	**46**	**36**	**29**	**22**
Measure CD	**230**	**173**	**132**	**93**	**73**	**54**	**43**	**35**	**26**
Measure film	**198**	**149**	**113**	**80**	**62**	**47**	**37**	**30**	**22**
Measure overlay	**184**	**138**	**105**	**74**	**58**	**43**	**34**	**28**	**21**
Metal CVD	**360**	**271**	**206**	**146**	**113**	**85**	**67**	**54**	**41**
Metal electroplate	**187**	**140**	**107**	**76**	**59**	**44**	**35**	**28**	**21**
Metal etch	**800**	**601**	**457**	**324**	**252**	**189**	**149**	**121**	**90**
Metal PVD	**411**	**309**	**235**	**167**	**129**	**97**	**77**	**62**	**46**
Plasma etch	**728**	**547**	**416**	**295**	**229**	**172**	**136**	**110**	**82**
Plasma strip	**336**	**253**	**192**	**136**	**106**	**79**	**63**	**51**	**38**
RTP CVD	**220**	**166**	**126**	**89**	**69**	**52**	**41**	**33**	**25**
RTP oxide/anneal	**144**	**108**	**82**	**58**	**45**	**34**	**27**	**22**	**16**
Test	**57**	**42**	**32**	**23**	**18**	**13**	**11**	**9**	**6**
Vapor phase clean	**506**	**380**	**289**	**205**	**159**	**119**	**94**	**76**	**57**
Wafer handling	**23**	**17**	**13**	**9**	**7**	**5**	**4**	**3**	**3**
Wet bench	**329**	**247**	**188**	**133**	**104**	**78**	**61**	**50**	**37**

Table 111b Yield Model and Defect Budget MPU Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted) [A]	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Critical Defect Size (nm)	**14**	**12.5**	**11.5**	**10**	**9**	**8**	**7**
Chip Size (mm^2) [B]	**111**	**88**	**140**	**111**	**88**	**140**	**111**
Overall Electrical D_0 (faults/m^2) at Critical Defect Size Or Greater [C]	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**
Random D_0 (faults/m^2) [D]	**1757**	**2214**	**1395**	**1757**	**2214**	**1395**	**1757**
Number of Mask Levels [E]	**37**	**37**	**37**	**39**	**39**	**39**	**39**
Random Faults/Mask	**47**	**60**	**38**	**45**	**57**	**36**	**45**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 45 nm Critical Defect Size or Greater							
CMP clean	**24**	**19**	**16**	**12**	**9**	**7**	**6**
CMP insulator	**58**	**46**	**39**	**28**	**23**	**18**	**14**
CMP metal	**65**	**52**	**44**	**32**	**26**	**20**	**15**
Coat/develop/bake	**10**	**8**	**7**	**5**	**4**	**3**	**2**
CVD insulator	**51**	**41**	**35**	**25**	**20**	**16**	**12**
CVD oxide mask	**67**	**54**	**45**	**33**	**26**	**21**	**16**
Dielectric track	**16**	**13**	**11**	**8**	**6**	**5**	**4**
Furnace CVD	**29**	**23**	**20**	**14**	**11**	**9**	**7**
Furnace fast ramp	**26**	**21**	**18**	**13**	**10**	**8**	**6**
Furnace oxide/anneal	**17**	**14**	**12**	**8**	**7**	**5**	**4**
Implant high current	**23**	**18**	**15**	**11**	**9**	**7**	**5**
Implant low/medium current	**21**	**17**	**14**	**10**	**8**	**6**	**5**
Inspect PLY	**21**	**17**	**14**	**10**	**8**	**7**	**5**
Inspect visual	**23**	**18**	**15**	**11**	**9**	**7**	**5**
Lithography cell	**18**	**14**	**12**	**9**	**7**	**5**	**4**
Lithography stepper	**17**	**13**	**11**	**8**	**7**	**5**	**4**
Measure CD	**20**	**16**	**13**	**10**	**8**	**6**	**5**
Measure film	**17**	**14**	**12**	**8**	**7**	**5**	**4**
Measure overlay	**16**	**13**	**11**	**8**	**6**	**5**	**4**
Metal CVD	**31**	**25**	**21**	**15**	**12**	**10**	**7**
Metal electroplate	**16**	**13**	**11**	**8**	**6**	**5**	**4**
Metal etch	**69**	**55**	**47**	**33**	**27**	**21**	**16**
Metal PVD	**36**	**28**	**24**	**17**	**14**	**11**	**8**
Plasma etch	**63**	**50**	**42**	**30**	**25**	**19**	**15**
Plasma strip	**29**	**23**	**20**	**14**	**11**	**9**	**7**
RTP CVD	**19**	**15**	**13**	**9**	**7**	**6**	**5**
RTP oxide/anneal	**12**	**10**	**8**	**6**	**5**	**4**	**3**
Test	**5**	**4**	**3**	**2**	**2**	**2**	**1**
Vapor phase clean	**44**	**35**	**29**	**21**	**17**	**14**	**10**
Wafer handling	**2**	**2**	**1**	**1**	**1**	**1**	**0**
Wet bench	**28**	**23**	**19**	**14**	**11**	**9**	**7**

Notes for Tables 111a and b:
[A] As defined in the ORTC Tables 1a and 1b.
[B] As defined in the ORTC Tables 1g and 1h.
[C] Based on assumption of 75% overall volume production yield.
[D] As shown in the ORTC Tables 5a and 5b. Based on assumption of 83% Random Defect Limited Yield (RDLY).
[E] As shown in the ORTC Tables 5a and 5b.

Table 112a Yield Model and Defect Budget DRAM Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted) [A]	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Critical Defect Size (nm)	**40**	**35**	**32.5**	**28.5**	**25**	**22.5**	**20**	**17.5**	**16**
Chip Size (mm^2) [B]	**88**	**139**	**110**	**74**	**117**	**93**	**74**	**117**	**93**
Cell Array Area (%) at Production [B]	**63%**	**63%**	**63%**	**56%**	**56%**	**56%**	**56%**	**56%**	**56%**
Non-core Area (mm^2)	**32**	**51**	**41**	**32**	**51**	**41**	**32**	**51**	**41**
Overall Electrical D_0 ($faults/m^2$) at critical defect size or greater [C]	**5220**	**3288**	**4143**	**5219**	**3288**	**4143**	**5219**	**3288**	**4143**
Random D_0 ($faults/m^2$) [D]	**3517**	**2216**	**2791**	**3516**	**2215**	**2791**	**3516**	**2215**	**2791**
Number of Mask Levels [E]	**24**	**24**	**24**	**24**	**24**	**26**	**26**	**26**	**26**
Random Faults/Mask	**147**	**92**	**116**	**147**	**92**	**107**	**135**	**85**	**107**
DRAM Random Particle per Wafer pass (PWP) Budget ($defects/m^2$) for Generic Tool Type Scaled to -40 nm Critical Defect Size or Greater									
CMP clean	**1808**	**872**	**872**	**872**	**445**	**419**	**417**	**201**	**201**
CMP insulator	**1400**	**675**	**675**	**675**	**344**	**324**	**323**	**156**	**156**
CMP metal	**2145**	**1035**	**1035**	**1035**	**528**	**497**	**495**	**239**	**239**
Coat/develop/bake	**559**	**270**	**270**	**270**	**138**	**130**	**129**	**62**	**62**
CVD insulator	**1552**	**748**	**748**	**748**	**382**	**360**	**358**	**173**	**173**
CVD oxide mask	**1905**	**919**	**919**	**919**	**469**	**441**	**439**	**212**	**212**
Dielectric track	**784**	**378**	**378**	**378**	**193**	**182**	**181**	**87**	**87**
Furnace CVD	**1072**	**517**	**517**	**517**	**264**	**248**	**247**	**119**	**119**
Furnace fast ramp	**1009**	**487**	**487**	**487**	**248**	**234**	**233**	**112**	**112**
Furnace oxide/anneal	**808**	**390**	**390**	**390**	**199**	**187**	**186**	**90**	**90**
Implant high current	**939**	**453**	**453**	**453**	**231**	**218**	**217**	**105**	**105**
Implant low/medium current	**895**	**432**	**432**	**432**	**220**	**208**	**207**	**100**	**100**
Inspect PLY	**1225**	**591**	**591**	**591**	**301**	**284**	**283**	**136**	**136**
Inspect visual	**1264**	**610**	**610**	**610**	**311**	**293**	**292**	**141**	**141**
Lithography cell	**1048**	**506**	**506**	**506**	**258**	**243**	**242**	**117**	**117**
Lithography stepper	**697**	**336**	**336**	**336**	**171**	**162**	**161**	**78**	**78**
Measure CD	**1047**	**505**	**505**	**505**	**258**	**243**	**242**	**117**	**117**
Measure film	**984**	**475**	**475**	**475**	**242**	**228**	**227**	**110**	**110**
Measure overlay	**958**	**462**	**462**	**462**	**236**	**222**	**221**	**107**	**107**
Metal CVD	**986**	**476**	**476**	**476**	**243**	**229**	**227**	**110**	**110**
Metal electroplate	**750**	**362**	**362**	**362**	**185**	**174**	**173**	**83**	**83**
Metal etch	**1816**	**876**	**876**	**876**	**447**	**421**	**419**	**202**	**202**
Metal PVD	**1083**	**522**	**522**	**522**	**266**	**251**	**250**	**121**	**121**
Plasma etch	**1923**	**928**	**928**	**928**	**473**	**446**	**444**	**214**	**214**
Plasma strip	**1475**	**711**	**711**	**711**	**363**	**342**	**340**	**164**	**164**
RTP CVD	**964**	**465**	**465**	**465**	**237**	**223**	**222**	**107**	**107**
RTP oxide/anneal	**706**	**341**	**341**	**341**	**174**	**164**	**163**	**79**	**79**
Test	**138**	**66**	**66**	**66**	**34**	**32**	**32**	**15**	**15**
Vapor phase clean	**2042**	**985**	**985**	**985**	**502**	**473**	**471**	**227**	**227**
Wafer handling	**58**	**28**	**28**	**28**	**14**	**13**	**13**	**6**	**6**
Wet bench	**1463**	**705**	**705**	**705**	**360**	**339**	**337**	**163**	**163**

Table 112b Yield Model and Defect Budget DRAM Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted) [A]	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Critical Defect Size (nm)	**14**	**12.5**	**11**	**10**	**9**	**8**	**7**
Chip Size (mm^2) [B]	**74**	**117**	**93**	**74**	**117**	**93**	**74**
Cell Array Area (%) at Production [B]	**56%**	**56%**	**56%**	**56%**	**56%**	**56%**	**56%**
Non-core Area (mm^2)	**32**	**51**	**41**	**32**	**51**	**41**	**32**
Overall Electrical D_0 ($faults/m^2$) at critical defect size or greater [C]	**5219**	**3288**	**4143**	**5219**	**3288**	**4143**	**5219**
Random D_0 ($faults/m^2$) [D]	**3516**	**2215**	**2791**	**3516**	**2215**	**2791**	**3516**
Number of Mask Levels [E]	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**135**	**85**	**107**	**135**	**85**	**107**	**135**
DRAM Random Particle per Wafer pass (PWP) Budget ($defects/m^2$) for Generic Tool Type Scaled to -40 nm Critical Defect Size or Greater							
CMP clean	**201**	**103**	**100**	**100**	**53**	**53**	**51**
CMP insulator	**156**	**79**	**78**	**78**	**41**	**41**	**40**
CMP metal	**239**	**122**	**119**	**119**	**63**	**63**	**61**
Coat/develop/bake	**62**	**32**	**31**	**31**	**16**	**16**	**16**
CVD insulator	**173**	**88**	**86**	**86**	**46**	**45**	**44**
CVD oxide mask	**212**	**108**	**106**	**106**	**56**	**56**	**54**
Dielectric track	**87**	**45**	**43**	**43**	**23**	**23**	**22**
Furnace CVD	**119**	**61**	**59**	**59**	**32**	**31**	**30**
Furnace fast ramp	**112**	**57**	**56**	**56**	**30**	**30**	**29**
Furnace oxide/anneal	**90**	**46**	**45**	**45**	**24**	**24**	**23**
Implant high current	**105**	**53**	**52**	**52**	**28**	**28**	**27**
Implant low/medium current	**100**	**51**	**50**	**50**	**26**	**26**	**25**
Inspect PLY	**136**	**70**	**68**	**68**	**36**	**36**	**35**
Inspect visual	**141**	**72**	**70**	**70**	**37**	**37**	**36**
Lithography cell	**117**	**60**	**58**	**58**	**31**	**31**	**30**
Lithography stepper	**78**	**40**	**39**	**39**	**21**	**20**	**20**
Measure CD	**117**	**59**	**58**	**58**	**31**	**31**	**30**
Measure film	**110**	**56**	**55**	**55**	**29**	**29**	**28**
Measure overlay	**107**	**54**	**53**	**53**	**28**	**28**	**27**
Metal CVD	**110**	**56**	**55**	**55**	**29**	**29**	**28**
Metal electroplate	**83**	**43**	**42**	**42**	**22**	**22**	**21**
Metal etch	**202**	**103**	**101**	**101**	**53**	**53**	**51**
Metal PVD	**121**	**61**	**60**	**60**	**32**	**32**	**31**
Plasma etch	**214**	**109**	**107**	**107**	**57**	**56**	**54**
Plasma strip	**164**	**84**	**82**	**82**	**43**	**43**	**42**
RTP CVD	**107**	**55**	**53**	**53**	**28**	**28**	**27**
RTP oxide/anneal	**79**	**40**	**39**	**39**	**21**	**21**	**20**
Test	**15**	**8**	**8**	**8**	**4**	**4**	**4**
Vapor phase clean	**227**	**116**	**113**	**113**	**60**	**60**	**58**
Wafer handling	**6**	**3**	**3**	**3**	**2**	**2**	**2**
Wet bench	**163**	**83**	**81**	**81**	**43**	**43**	**41**

Notes for Tables 112a and b:
[A] As defined in the ORTC Tables 1a and 1b.
[B] As defined in the ORTC Tables 1c and 1d.
[C] Based on assumption of 89.5% (RDLY).
[D] As shown in the ORTC Tables 5a and 5b. Based on assumption of 89.5% RDLY.
[E] As shown in the ORTC Tables 5a and 5b.

DEFECT DETECTION AND CHARACTERIZATION

The ability to detect inline yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production—process research and development (PRD), yield ramp (YR), and volume production (VP)—broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabs begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the chip manufacturers just in time for each phase of the process cycle. Tools that meet the requirements for PRD are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate YR must be available several months before production begins. Finally, the ability to monitor excursions at a technology generation is needed when the product hits high yield levels.

One of the major challenges is to get to the defect of interest. The signal-to-noise ratio is therefore a very important criterion for all inspection tools. The more nuisance defects are captured the less valuable the results are as the time spend to get to the defect of interest increases through intense review.

Technology requirements are separated into unpatterned wafer inspection, patterned wafer inspection, high aspect ratio inspection, defect review, and bevel wafer inspection, as shown in Table 113. The effects of the buried patterning in post-chemical mechanical planarization (CMP) wafers makes patterned wafer inspection with grazing angle laser inspection tools approximate unpatterned inspection for the purposes of tool qualification, and are appropriate for this roadmap. Also, unpatterned inspection utilized extensively for tool qualification has implemented defect review from such scans, which has increased in importance in the last few years. Backside wafer inspection needs a defect review possibility in order to be used to the full extent. Bare wafer inspection sensitivities were adapted to reflect more the real world of then new tools purchased for sensitivity. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is treated separately from patterned wafer inspection due to special sensitivity requirements described in the Difficult Challenges section as well as note E under Table 113.

The inspection of bevel, apex, and wafer edge on the top and bottom on multilayer product wafers becomes a big challenge as increasingly more defect/process problems have their origin in those areas of the wafer. Important criteria (besides coverage of all areas, sensitivity, and speed) are ADC and optical review capability on the tool as well as a standard result file allowing SEM review.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside requirements are based on the Lithography chapter Technology Requirements table, and also defined slightly differently in the Front End Process Starting Materials table, and Surface Preparation table.

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers (defects that cannot be detected with conventional optical technologies) is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and back end of processing. Macro defects that impact large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved to match the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology generation.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The price, fab space occupied, and the throughput of defect detection tools are major contributors to their cost-of-ownership. Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table 113 have been stipulated on the basis of detecting accurately sized polystyrene latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pits pattern flaws, surface roughness, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

The definition of the wafer edge exclusion for all tools (beside the bevel inspection tool) was changed based on factory integration decision, in order to make it consistent throughout the ITRS. The ADC specification for defect review has been changed to reflect that higher accuracy and purity are more important than amount of defect classes.

Table 113a Defect Detection Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	
Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]*										
Process R&D at 300 cm^2/hr (1 "200 mm wafer"/hr)	40	35	32.5	28.5	25	22.5	20	17.5	16	*0.5 × DR*
Yield ramp at 1200 cm^2/hr (4 "200 mm wafer"/hr)	64	56	52	45.6	40	36	32	28	25.6	*0.8 × DR*
Volume production at 3000 cm^2/hr (10 "200 mm wafer"/hr)	◆80	70	65	57	50	45	40	35	32	*1.0 × DR*
Tool matching (% variation tool-to-tool) [C]	◆5	3	3	3	3	2	2	2	2	
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	2	2	
Cost of ownership ($/$cm^2$)	0.078	0.078	0.078	0.078	0.078	0.078	0.08	0.078	0.078	
High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate [D, E]										
Sensitivity without speed requirement	80	70	65	57	50	45	40	35	32	*1.0 × DR*
Process verification at 300 cm^2/hr (1 "200 mm wafer"/hr)	◆80	70	65	57	50	45	40	35	32	*1.0 × DR*
Volume manufacturing at 1200 cm^2/hr (4 "200 mm wafer"/hr)	◆80	70	65	57	50	45	40	35	32	*1.0 × DR*
CoO HARI ($/$cm^2$)	0.388	0.388	0.388	0.388	0.388	0.388	0.388	0.388	0.388	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]										
Metal film	64	56	52	45.6	40.0	36.0	32.0	28.0	25.6	*0.8 × DR*
Bare silicon and non-metal film	40	35	32.5	28.5	25	22.5	20	17.5	16	*0,5 × DR*
Wafer backside (defect size, nm) [H]	400	350	325	285	250	225	200	175	160	*5.0 × DR*
CoO ($/$cm^2$)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.004	
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	2	2	
Defect Review (Patterned Wafer)										
Resolution (nm) * [I]	2	1.8	1.6	1.4	1.3	1.125	1	0.875	0.8	*0.05 × pattern sensitivity R&D*
Coordinate accuracy (nm) at resolution [J]	800	700	650	570	500	450	400	350	320	*10 × DR*
Speed at ADR without ADC	960	1200	1200	1200	1200	1200	1200	1200	1200	
Automatic Defect Classification at Defect Review Platform [K]										
Redetection: minimum defect size (nm)	32	28	26	22.8	20	18	16	14	12.8	*0.4 × DR*
Number of defect types [L]	◆10	10	10	15	15	15	15	15	20	
Speed (defects/hours) with ADC	◆720	720	720	720	720	720	720	720	720	
Speed w/elemental (defects/hours)	◆360	360	360	360	360	360	360	360	360	
Number of defect types (inline ADC) [M]	◆10	10	10	10	10	10	10	10	10	
Wafer inspection on multilayer product wafer of top and bottom bevel, APEX and 3 mm wafer edge exclusion PSL spheres at 90% capture rate, Equivalent sensitivity (nm) [N, O]										
Sensitivity [nm] without speed requirement at 50% capture rate	◆400	350	325	285	250	225	200	175	160	*5 × DR*
Sensitivity [nm] at 100 wafer/hrs	◆2000	1750	1625	1425	1250	1125	1000	875	800	*25 × DR*
Defect classes, ADC [P]	3	5	5	5	10	10	10	10	10	
Tool matching (% variation tool-to-tool)	◆10 %	10%	10%	10%	5%	5%	5%	5%	5%	
CoO [$/300 mm wafer]	1	1	1	0.9	0.8	0.8	0.8	0.8	0.8	

**PSL—polystyrene latex (spheres utilized to simulate defects of known size during sizing calibration) ADR— automatic defect review*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

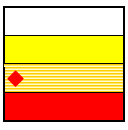
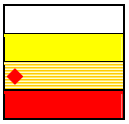


Table 113b Defect Detection Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]*								
Process R&D at 300 cm^2/hr (1 "200 mm wafer"/hr)	14	12.5	11	10	9	8	7	*0.5 × DR*
Yield ramp at 1200 cm^2/hr (4 "200 mm wafer"/hr)	22.4	20	17.6	16	14.4	12.8	11	*0.8 × DR*
Volume production at 3000 cm^2/hr (10 "200 mm wafer"/hr)	28	25	22	20	18	16	14	*1.0 × DR*
Tool matching (% variation tool to tool) [C]	2	2	2	2	2	2	2	
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	
Cost of ownership ($/$cm^2$)	0.078	0.078	0.078	0.078	0.078	0.078	0.078	
High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate [D, E]								
Sensitivity without speed requirement	28	25	22	20	18	16	14	*1.0 × DR*
Process verification at 300 cm^2/hr (1 "200 mm wafer"/hr)	28	25	22	20	18	16	14	*1.0 × DR*
Volume manufacturing at 1200 cm^2/hr (4 "200 mm wafer"/hr)	28	25	22	20	18	16	14	*1.0 × DR*
CoO HARI ($/$cm^2$)	0.388	0.388	0.388	0.388	0.388	0.388	0.388	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]								
Metal film	22.4	20.0	17.6	16.0	14.4	12.8	11.0	*0.8 × DR*
Bare silicon and non-metal film	14	12.5	11	10	9	8	7	*0,5 × DR*
Wafer backside (defect size, nm) [H]	140	125	110	100	90	80	70	*5.0 × DR*
CoO ($/$cm^2$)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	
Defect Review (Patterned Wafer)								
Resolution (nm) * [I]	0.7	0.625	0.55	0.5	0.45	0.4	0.35	*0.05 × pattern sensitivity R&D*
Coordinate accuracy (nm) at resolution [J]	280	250	220	200	180	160	140	*10 × DR*
Speed at ADR without ADC	1200	1200	1200	1200	1200	1200	1200	
Automatic Defect Classification at Defect Review Platform [K]								
Redetection: minimum defect size (nm)	11.2	10	8.8	8	7.2	6.4	5.6	*0.4 × DR*
Number of defect types [L]	20	20	25	25	25	25	25	
Speed (defects/hours) with ADC	720	720	720	720	720	720	720	
Speed w/elemental (defects/hours)	360	360	360	360	360	360	360	
Number of defect types (inline ADC) [M]	10	10	10	10	10	10	10	
Wafer inspection on multilayer product wafer of top and bottom bevel, APEX and 3 mm wafer edge exclusion PSL spheres at 90% capture rate, Equivalent sensitivity (nm) [N, O]								
Sensitivity [nm] without speed requirement at 50% capture rate	140	125	110	100	90	80	70	*5 × DR*
Sensitivity [nm] at 100 wafer/hrs	700	625	550	500	450	400	350	*25 × DR*
Defect classes, ADC [P]	10	10	10	10	10	10	10	
Tool matching (%variation tool-to-tool)	5%	5%	3%	3%	3%	3%	3%	
CoO [$/300 mm wafer]	0.8	0.7	0.7	0.7	0.7	0.7	0.7	

**PSL—polystyrene latex (spheres utilized to simulate defects of known size during sizing calibration) ADR— automatic defect review*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 113a and b:

[A] Patterned wafer scan speed is required to be at least 300 cm^2 /hour for process R&D mode, 1,200 cm^2 /hour for yield ramp mode, and, at least, 3,000 cm^2 /hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435. (Example: 3000 cm^2 /hr is about 10, 200 mm wafers and 4.3, 300 mm wafers).

[B] Patterned wafer nuisance defect rate shall be lower than 5% in all process phases. False counts in the R&D phase less than 5%, and less than 1% in the yield ramp and volume production phase. Nuisance is defined as an event indicated and a defect is present, just not the type of interest. These maybe significant and could be studied at a later date. The defect classifier must consider the defect type and assign significance. False is defined at an event is indicated, but no defect can be seen using the review optics path of the detection tool, which supports recipe setup validation.)

[C] Metric % variation tool-to-tool in number of non-matching defects/total number of defects from standard tool.

Procedure: Recipe sensitivity set on first (standard) tool with false <5. Transfer this recipe without changes and perform ten runs with a wafer containing a minimum of 30 defects.

[D] High Aspect Ration is defined as for contacts 15:1.

[E] HARI defects are already considered "killers" at any process stage, but defined at the contact/via levels for full feature size capture. Hence, minimum defect sensitivity was stipulated as 1.0× technology generation at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more is the model to be detected. If in the future, detection tools can determine size, shape, or remaining material on the order of 0.3× technology generation, this will more adequately match known experience for resistance changes. Scan speed for HARi tools have been broken out into process verification and volume production types. Process verification usually refers to SEM-type tools (but not necessarily in the future) and includes voltage contrast capability. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435.

F] Un-patterned wafer defect detection tools will be required to scan 200 (300 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually.

[G] Must meet haze and crystal originated pit (COP) requirements specified in the Front End Processes chapter Starting Materials section of the Roadmap.

[H] Sensitivity requirement agreed with Lithography TWG. Might need to be revised with implementation of EUV lithography. Optical review capability of backside results is a requirement.

[I] Resolution of defect review is defined as 0.05 × Sensitivity at pattern inspection R&D.

[J] Driver is the defect size.

[K] Assumptions: 5,000 wafer starts per week, defects per wafer based on surface preparation at front end of line (FEOL), leading to defects per hour that need review, 100% ADC.

[L] Defect classifications need to meet: Repeatability 95 %, Accuracy 90 %, Purity 90 %.

[M] Defect classifications need to meet: Repeatability 95 %, Accuracy 80 %, Purity 80 %.

[N] Review capability: optical review capability at the tool but also offline SEM review is necessary.

[O] An industry standard result file is needed also for SEM review capability. Result file containing coordinate and angular information to also allow prior level subtraction, also add images from tool in result file.

[P] The first three ADC classes to start with: chips, surface particle large, surface particle small. The fourth ADC class should be blisters.

YIELD LEARNING

Yield learning is defined as the collection and application of process and wafer knowledge to improve device yield through the identification and resolution of systematic and random manufacturing events. As seen from the yield learning technology requirements in Table 114, the key requirements for achieving historic yield ramps include the detection of ever shrinking yield-detracting defects of interest, timely identification of root causes with growing data volume, chip complexity, process complexity, and improving the yield learning rate per each cycle of learning. With increasing process complexity and longer cycle times, tools and methods are needed to increase the number of yield learning cycles for each technology generation. Also, with continuous move to smaller features and longer processes, 300 mm wafers, and new materials (low-κ, high-κ, etc.), numerous tools and methods are required to understand the entire yield detracting interactions. Use of silicon on insulator (SOI), SiGe and other new device structures and materials will further challenge yield learning.

Yield in most industries has been defined as the number of products that can be sold divided by the number of products that can be made. In the semiconductor industry, where silicon wafers act as batches for integrated circuits, the yield (Y_{total_i}) of a particular integrated circuit design product (i) can be expressed in terms of equation (1).

$$Y_{total\_i} = (Y_{line}) * (Y_{batch\_i}) \quad (1)$$

Y_{line} in equation (1) denotes the line yield, wafer yield, or survival yield. It represents the fraction wafers that survive processing through the whole manufacturing line. Y_{batch_i} denotes batch yield, chip yield or die-sort yield, which represents the fraction of integrated circuits of a particular design (i) on each wafer that are completely functional at the end of the line.

Batch yield can be expressed in terms of equation (2).

$$Y_{batch\_i} = (Y_{sys\_i}) * (Y_{random\_i}) \quad (2)$$

Y_{sys_i} in equation (2) denotes the component of batch yield that results from systematic faults. Y_{random_i} denotes the component batch yield that results from randomly distributed faults. Y_{random_i} typically be expressed as a highly non-linear function of the random fault density and the critical area of an integrated circuit design—the area in a chip that is susceptible to random faults. Y_{random_i} is frequently expressed in terms of the negative binomial law.

Historically, the semiconductor industry has been driven by batch yield in general and its random component in particular. However, the semiconductor industry tends to operate in an environment of exponentially decaying product prices, which put semiconductor manufacturers under time-to-market pressure. To a large degree, profitability is derived from an early and steep, yield ramp. The sooner a semiconductor manufacturer can generate high batch yield, the earlier the manufacturer can ramp to volume production, and the more profitable the semiconductor manufacturer's integrated circuit venture is likely to be. Improving the systematic component of batch yield, which frequently constrains batch yield in the early stages of manufacturing, can enhance profitability by enabling production at a point in time when chip prices are very high.[1] Yield learning in the early stages of manufacturing may thus differ significantly from yield learning in the later stages of manufacturing.

Also, yield learning in a foundry differs substantially from yield learning in a fabrication facility that produces a few high-volume products. The high-volume producer will be constrained by batch yield in the early stages of manufacturing. Line yield will be the limiting factor once batch yield is high and volume production has begun. By contrast, a foundry may introduce a plethora of low-volume products into a relatively mature process on a routine basis. On occasion, one lot of 300 mm wafers may provide a lifetime inventory of a particular design, which sells into a very short market window. A few chips of the design must exit the fab by a specific date. Under these circumstances, designing the circuit correctly the first time; fabricating flawless masks the first time; a rapid cycle time through the line, and a high line yield may be more important than a high batch yield.

Another recent challenge is the process of rapid yield learning on 300 mm wafers. The 300 mm semiconductor manufacturing like all other wafer size transitions has significant challenges set upon it to meet aggressive yield and cost goals. Most of these challenges are not new to 300 mm but are manifestations of old issues that occur with most new wafer size introductions. These challenges include: clean, defect-free substrates, substrate heat capacity, process uniformity, and new processing materials, all of which are just part of implementing a new substrate technology, and any of which can delay profitable yields for a technology generation cycle by months or years if not solved in planning or start-up phases of this transition.

On the positive side, generating higher yield in 300 mm manufacturing is the use of latest and greatest manufacturing tool sets. The tool sets for the most part have leveraged years of historical learning and improvement programs in their designs, making them the most sophisticated tools ever built right from the start. Also benefiting the 300 mm activities are the better process designs and simulations that are occurring before any silicon ever reaches then manufacturing floor. Process simulation has proven to be a very cost-effective and timely way to speed the rate of change. Also 300 mm manufacturing is universally being implemented with metrology needs being embedded as forethought and not an afterthought in manufacturing, as in the past. Finally, the physical potential yielding area of a 300 mm wafer is greater than 2× that of a 200 mm wafer.

Working against higher initial yields in 300 mm manufacturing are the usual challenges that seem to accompany any substrate technology transition. Along with a substrate change come new materials, specifically low-κ films that the industry wants to implement in parallel with this new substrate. It is widely believed that the single largest issue on 300 mm is uniformity across the entire wafers surface area. Uniformity issues include the usual sources of film thickness, etch profiles, and dose control. Metrology monitoring capabilities to properly cover the vast surface area of a 300 mm wafer, and its ability to recognize when non-uniform surface issues occur is also a huge challenge.

Yield Management in a 300 mm factory is going to be more closely coupled to data management then in any previous factory or technology generation currently in manufacturing. How data from all generating sources of the factory is collected, stored, compiled, and accessed is going to be more vital than in any other manufacturing environment

[1] *See for example C. Weber, D. Jensen and E. D. Hirleman, "What Drives Defect Detection Technology?" Micro, June 1998, pp. 51–72.; C. Weber, "Yield Learning and the Sources of Profitability in Semiconductor Manufacturing and Process Development," Proc. IEEE/SEMI/ASMC, Boston, Mass., May 1, 2002, pp. 324–329.*

previously conceived. In advanced manufacturing, any data generated could potentially hold the key to understanding and solving a yield issue that is identified at sort, and needs to be recorded in such a fashion as to be accessible by yield engineers if required. Accessing the raw data in such a way as to generate meaningful correlations and results is going to be a critical requirement in the 300 mm manufacturing. Data storage and consequently the user interfaces to access this data cannot be handled as an afterthought, if these factories are to be successful during the start up.

The difference in the 300 mm factories will be the sources of data. These sources will need to be greatly expanded as compared to the data sources used in 150 and 200 mm manufacturing. Specifically we are referring to the obvious inline metrology, electrical test, and sort results, but we also include detailed process equipment information,[2] front opening unified pod (FOUP) wafer position, factory environmental conditions, and delivery service,[3] along with the more advanced process state conditions that are part of a fully implemented APC solution in the factory.

Implemented APC and fault detection and classification (FDC) solutions in 300 mm will be more common than in any prior technology generation. However, these control solutions will require tremendous data transport and data processing systems to support a full-scale implementation. Managing this, which must all be done in real time to benefit the factory, is a monumental undertaking. Maintaining standards and open access systems allowing the best internal and external solutions to work together is a must.

Down stream, or rather offline analysis, of all the factories data will also require new approaches, in addition to the existing ones, to fully grasp all information that can be correlated to yield. The greatest challenge to a comprehensive data management system required for yield learning is the ability to deal with and integrate data streams that are continuous, periodic, sporadic, and interval-based such that they can all be linked through some common coupling system or user interface and be resolved by engineers. Keeping data aligned down to the wafer level or possibly the die level will require automated data matching techniques that are currently only done on an ad-hoc basis at individual desktops. For example, the simple task of aligning all wafer surface information[4] through a universal coordinate system is a requirement to be effective in yield analysis, but this is not universally implemented in most companies. It is also critical to have all data sources open and accessible by multiple user interfaces in order to maximize the effectiveness of yield engineering resources in finding problems. The best-of-breed data systems going forward will allow internal as well as multiple third party software solutions and graphical user interfaces (GUIs) to access the raw data formats, giving engineers the greatest flexibility in identifying and solving yield limiting issues. Barriers such as these must be eliminated prior to going into manufacturing 300 mm wafers if companies are expected to address yield issues in the shortest amount of time.

The rapid identification of defect and fault sources through integrated data management continues to be the essence of rapid yield learning. Table 114 presents the technology requirements for the yield learning focus topic. Learning must proceed at an accelerated rate to maintain the yield ramp from introduction to maturity within the expected timeline despite the growth in circuit complexity and the larger amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. In the face of this increased complexity, strategies and software methods for integrated data management (IDM) have been identified as critical for maintaining productivity. IDM must comprehend integrated circuit design, visible and non-visual defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the IDM system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. IDM will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as automatic defect classification (ADC) and spatial signature analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information. The technology requirements for various types of defects are described below.

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[2] State of tool repair or maintenance at time of wafer processing, components, or parts kits currently in use, operational states of sub-systems including RF power, gas flows, vacuum pressures, etc., current particle results for system are only examples.

[3] Factory data includes the obvious temperature and humidity conditions both inside, outside and in all chemical storage and usage facilities, they also include data any chemical delivery system including the specific source and quality of the chemical currently in use.

[4] Wafer surface information includes film thickness metrology, CD and alignment metrology, defects, electrical test, electrical bit-map, etc.

VISIBLE DEFECTS

Tools are needed to detect, review, classify, analyze, and source continuously shrinking visible defects.

NON-VISUAL DEFECTS

Defects that cause electrical failure, but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-visual defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance or timing; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-visual defects) will become increasing challenging. Techniques need to be developed that rapidly isolate failures and partitions them into those caused by visible defects, non-visual defects, and parametric issues.

PARAMETRIC DEFECTS

As minimum feature size decreases, the systematic mechanism limited yield (SMLY or Ys) decreases as well. A major contributor to the Ys component of yield is parametric variation within a wafer and wafer-to-wafer. Parametric defects have traditionally been referred to as "non-visual defects." However, parametric defects require separation from the "non-visual defects" for rapid sourcing.

ELECTRICAL FAULTS

As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the pattern number of a wafer times the number of process steps, forming the defect sourcing complexity factor as shown in Table 114. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity. Moreover, the soft failures caused by sporadic cross-chip timing variation will require innovative new approaches to identify the root causes since these type of failures reside between a hard spot defect failure and consistent systematic failure issue.

DATA MANAGEMENT SYSTEMS

The current practice in data management system (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient IDM is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect and fault sourcing capabilities, methods must be established for integrating workflow information (such as WIP data) with the DMS, particularly in commercial DMS systems. This will be important when addressing issues of advanced process and tool control beyond simple tool shutdown, such as lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time-based data such as that generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time-based data such that it can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

The purpose of the yield learning technologies requirements table is to provide a compact look at the impact of each new technology generation on the ability to rapidly learn and correct yield impacting events that occur during device manufacturing. The table is divided into three production phases, PRD, YR, and VP. The wafer-out volume (pcs) of each phase is a typical number of total wafers to be inspected to achieve each yield target, 30% of PRD, 70% of YR and 85% of VP. The defect sourcing complexity factor is roughly the pattern number of a wafer times the number of processing steps. It can be considered as an indicator of the "volume" of elements in completed wafers that must be inspected to achieve the yield target. Yield improvement per inspection columns will be determined in the next revision. The overall goal is to provide manufacturers and suppliers with an understanding of the factors and technologies that are available, or will be required, to facilitate rapid yield learning at current and future technology generations.

Table 114a Yield Learning Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Wafer size (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**
Number of mask levels	**33**	**33**	**33**	**35**	**35**	**35**	**35**	**35**	**35**
Number of processing steps	**543**	**556**	**570**	**583**	**596**	**610**	**623**	**636**	**650**
Process R&D at 300 mm wafer/hr, sampling rate at 100% [A]									
Patterned wafer inspection sensitivity (nm) during yield ramp	**40.0**	**35.0**	**32.5**	**28.5**	**25.0**	**22.5**	**20.0**	**17.5**	**16.0**
Wafer out volume (pcs) of yield learning to 30% at R&D [B]	**4525**	**4633**	**4750**	**4858**	**4967**	**5083**	**5192**	**5300**	**5417**
Defect sourcing complexity factor (1E15) [C]	**64**	**85**	**101**	**135**	**179**	**226**	**292**	**876**	**1071**
Yield improve % per inspection	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Yield ramp from 30% to 70% at 300 mm wafer/hr, sampling rate at 50% [A]									
Patterned wafer inspection sensitivity (nm) during yield ramp	**64.0**	**56.0**	**52.0**	**45.6**	**40.0**	**36.0**	**32.0**	**28.0**	**25.6**
Wafer out volume (pcs) of yield learning from 30% to 70% [D]	**9050**	**9267**	**9500**	**9717**	**9933**	**10167**	**10383**	**10600**	**10833**
Defect sourcing complexity factor (1E15) [C]	**25**	**33**	**40**	**53**	**70**	**88**	**114**	**342**	**418**
Yield improve % per inspection	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Yield ramp from 70% to base line (85%) at 300 mm wafer/hr, sampling rate at 20% [A]									
Patterned wafer inspection sensitivity (nm) during yield ramp	**◆80.0**	**70.0**	**65.0**	**57.0**	**50.0**	**45.0**	**40.0**	**35.0**	**32.0**
Wafer out volume (pcs) of yield learning from 70% to baseline [E]	**◆13575**	**13900**	**14250**	**14575**	**14900**	**15250**	**15575**	**15900**	**16250**
Defect sourcing complexity factor (1E15) [C]	**10**	**13**	**15**	**20**	**27**	**34**	**44**	**131**	**161**
Yield improve % per inspection	**◆TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

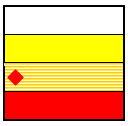
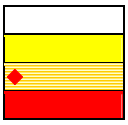


Table 114b Yield Learning Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Wafer size (mm)	**450**	**450**	**450**	**450**	**450**	**450**	**450**
Number of mask levels	**37**	**37**	**37**	**37**	**39**	**39**	**39**
Number of processing steps	**663**	**676**	**690**	**704**	**717**	**730**	**743**
Process R&D at 300 mm wafer/hr, sampling rate at 100% [A]							
Patterned wafer inspection sensitivity (nm) during yield ramp	**14.0**	**12.5**	**11.0**	**10.0**	**9.0**	**8.0**	**7.0**
Wafer out volume (pcs) of yield learning to 30% at R&D [B]	**5525**	**5633**	**5750**	**5867**	**5975**	**6083**	**6192**
Defect sourcing complexity factor (1E15) [C]	**1427**	**1825**	**2406**	**2970**	**3734**	**4812**	**6397**
Yield improve % per inspection	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Yield ramp from 30% to 70% at 300 mm wafer/hr, sampling rate at 50% [A]							
Patterned wafer inspection sensitivity (nm) during yield ramp	**22.4**	**20.0**	**17.6**	**16.0**	**14.4**	**12.8**	**11.2**
Wafer out volume (pcs) of yield learning from 30% to 70% [D]	**11050**	**11267**	**11500**	**11733**	**11950**	**12167**	**12383**
Defect sourcing complexity factor (1E15) [C]	**557**	**713**	**940**	**1160**	**1459**	**1880**	**2499**
Yield improve % per inspection	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Yield ramp from 70% to base line (85%) at 300 mm wafer/hr, sampling rate at 20% [A]							
Patterned wafer inspection sensitivity (nm) during yield ramp	**28.0**	**25.0**	**22.0**	**20.0**	**18.0**	**16.0**	**14.0**
Wafer out volume (pcs) of yield learning from 70% to baseline [E]	**16575**	**16900**	**17250**	**17600**	**17925**	**18250**	**18575**
Defect sourcing complexity factor (1E15) [C]	**214**	**274**	**361**	**446**	**560**	**722**	**960**
Yield improve % per inspection	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 114a and b:
[A]. Wafer out volume of yield learning to 30% at R&D: Assume 1/3 of total process steps are critical and need to fine tune the processes for sourcing systematic defect reduction at R&D period. One step with one lot and 25 wafers in a lot.
*[B]. Defect sourcing complexity factor: Total wafers * sampling rate* 1/ sensitivity*
*[C]. Yield improvement % by each inspection layer: Yield improvement% in R&D period * 1/defect complexity factor*
[D]. Wafer out volume of yield learning from 30% to 70%: Assume 2/3 of total process steps are possible of yield detractors and need to fine tune the processes for sourcing systematic and random defects
[E]. Wafer out volume of yield learning from 70% to base line 85%: Assume 3/3 of total process steps are possible of yield detractors and need to fine tune the processes margin for sourcing systematic and random defects

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table 115.

Wafer environment control—The wafer environment control includes the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in PODs/FOUPs. As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to effective wafer and reticle isolation deployment.

Airborne molecular contamination—Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of AMC. Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden. Acid vapors in the air have been linked with the release of boron from HEPA filters and the impact of amines on deep ultraviolet (DUV) photoresists are well known examples of AMC affecting wafer processing. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation in the cleanroom to measure AMC at the part per trillion level. Surface acoustic wave (SAW) devices and atmospheric pressure ionized mass spectroscopy (APIMS) have been used to measure low level AMC, but low cost, routine monitoring may be required as devices approach molecular dimensions. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front-end processes. Although numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures, the need for nitrogen purging of wafer environment enclosures is being investigated for critical process steps. Not all process steps will be impacted by AMC. For example, future lithography systems will require vacuum processing and are not expected to impose new AMC control requirements in the cleanroom environment. The potential for AMC to impact new processes should be considered in all process integration studies.

Process critical materials—Additional experimental investigation is required to support our understanding of impurity specifications in novel materials, such as Cu plating solutions, CMP slurries, or chemical vapor deposition (CVD) precursors to high/low-κ dielectrics and other thin film materials. Particle levels per volume have been held constant at critical particle size. Assuming a 1/×3 power law relationship, this means a cleanliness increase of approximately 2× per generation. Measurement of particles at the critical size is desirable, but monitoring of larger size particles is likely with critical particle size concentrations inferred from assumed particle size distributions.

Ultrapure water—UPW is generally considered to be 18.2 MegΩ-cm resistivity at 25°C, low ppt in metals, less than 50 ppt in inorganic anions and ammonia, less than 0.2 ppb in organic anions, and below 1 PPB total oxidizable carbon (TOC) and silica (dissolved and colloidal). Particle levels are reduced using the best available ultrafiltration technology. Bacteria are present, on surfaces and to a lesser degree in the bulk fluid, and controlled to very low levels, typically <1 colony forming unit (cfu)/L in the bulk fluid. The 2005 Roadmap values, presented in Table 115, represent typical UPW quality currently in use to manufacture the most advanced semiconductor devices and have been validated by benchmark surveys. More stringent criteria beyond 2005 are only projected where there is evidence that manufacturing process requirements demand improvements. *A discussion of the UPW requirements can be found in the supplemental material online*.

An important trend in UPW is the consideration of some parameters as process variables rather than contaminants, looking at stability more than absolute levels. Some semiconductor manufactures now treat dissolved oxygen (DO) in this way, while others still consider it a contaminant. There is some evidence to support minimizing dissolved oxygen levels for manufacturing process steps that occur in an inert atmosphere. However, since almost all water-intensive manufacturing steps generally occur in an oxygenated ambient atmosphere, there has been a small relaxation of requirements. Stability of temperature and pressure continue to be important.

Contaminant quality levels in UPW must be viewed in the context of where that quality is required and where it is to be measured. Points of measurement are referred to as the POD, point of connection (POC), POE, and POU. The POD is just after the last treatment step of the UPW system, the POE is at the tool connection point, and the POU is in the tool. The 2005 Roadmap defines UPW quality at the POE or POU as indicated in Table 115. UPW quality can change between these three locations, especially between the POE and POU, and requires particular attention to maintain quality throughout. In addition sampling techniques are critical to ensure accurate analytical results. As UPW specifications shift from the POE to the POU, sampling methods will become more difficult and costly. Most benchmark data has been collected at POD or POE and is the basis for parameters in Table 115. Where contaminant levels have been extended to POU this has been done based on engineering judgment assuming the semiconductor processing tool is well designed and operated with regard to maintaining fluid purity in accordance with applicable SEMI standards.

Ozonated UPW is not addressed in this Roadmap as it is considered a dilute process chemistry that is generally applied at the process tool. At the time of printing immersion lithography posed no special requirements for UPW other than possible degasification and additional closer temperature control, which would be done at the process tool.

UPW recycle—To promote resource optimization UPW use efficiency improvements are typically required. Cost effective technologies, including treatment and analytical methods, are needed to ensure UPW quality is maintained, as more water is recycled back through the system. A well-implemented recycle program has been shown to improve final water quality by using a "cleaner" stream for the feed, in addition to providing other benefits. Further information and requirements can be found in the *Environmental, Safety, and Health* chapter.

UPW measurement methodologies—General test methodologies for monitoring contaminants in UPW are indicated in Figure 101. Over the past few years the ITRS UPW team has benchmarked many advanced UPW systems to determine water quality. This effort has also identified the inadequacy of some measurement methodologies to quantify contaminants in UPW. The following analytical methods are not sensitive to present levels of contamination in UPW: resistivity, total oxidizable carbon, inorganic anions, and organic ions, as well as some organic species. Speciation of organics has been limited by these methods. Sensitivity of the following methods is presently adequate: viable bacteria, dissolved gasses, and metals. While particle measurement is generally not adequately sensitive at the critical dimension it may be technically sound to extrapolate particle size and concentration data to the critical dimension. Benchmarking has shown this size distribution to be unique to a particular UPW system and/or measurement technique. Each user of the Roadmap is advised to determine a particle distribution for their fab empirically. Benchmarking has indicated a log:log distribution relationship with slopes from -1 to -5. *A more complete treatment of UPW concerns is covered in the supplemental material of this chapter online*, where also *a conversion tool can be found*.

Parameter	Measured (POD/POC)	Test Method
Resistivity	Online	Electric cell
Viable bacteria	Lab	Incubation
TOC	Online	Conductivity/CO_2
Inorganic anions and NH_4+	Lab	Ion chromatography
Organic ions	Lab	Ion chromatography
Other organics	Lab	Various, e.g., ES TOF, ICP-MS
Reactive silica	Online or lab	Colorimetric
Dissolved N_2	Online	Electric cell
Total silica	Lab	ICP-MS or GFAAS
Particle monitoring	Online	Light scatter
Particle count	Lab	SEM—capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP-MS
Dissolved O_2	Online	Electric cell

ES TOF—Electro spray time of flight ICP-MS—inductively coupled plasma mass spectrometry
GFAAS—graphite furnace atomic absorption spectrometry

Figure 101 General Test Methodology for Ultrapure Water

UPW and liquid chemicals particle measurement—Problem Definition and Goals: The sensitivity limit of particle counters for UPW and liquid chemicals has not kept pace with decreases in the critical particle size (the size of particles which are thought to be detrimental to wafer yield). Measurements at the critical particle size are made difficult by the low scattering efficiency of very small particles. Low particle concentrations and small sample volumes of current particle monitors can result in large sample-to-sample variability. More sensitive particle measurement methodology with adequate measurement statistics is needed to meet projected purity goals.

The Sensitivity Problem: As of 2005, the highest sensitivity particles counter commercially available for UPW is 0.03 microns and for liquid chemicals is 0.065 microns. According to the ITRS, the critical particle size is 0.040 microns for 2005, and 0.025 microns for 2009. Past improvements in particle counter sensitivity for UPW have been accomplished by increases in laser power. While improvements in sensitivity for liquid chemical particle counters are viable, further sensitivity improvements for UPW using this approach are unlikely, due to the significant cost implications. In addition, high-cost solutions do not necessarily guarantee a production-worthy metrology tool. High initial expense coupled with increased cost of ownership impact the viability of higher sensitivity instruments. Therefore, in order to meet the ITRS goals, a mathematical extrapolation to project particle concentrations below the measurement sensitivity of available instrumentation must be utilized. This extrapolation assumes a $1/d^3$ relationship between particle counts and particle size in liquids. The further away the ITRS critical particle size gets from actual measurement capability, the higher the potential for error—error being defined as the difference in the projected value to the true value. Therefore, it is still important for the industry to develop a more sensitive method that can measure particle concentrations at greater sensitivity to validate the particle count versus particle size relationship so that the relationship can continue to be reliably used.

The Measurement Precision Problem: Statistical process control is increasingly being used to monitor the consistency of process parameters. Process variation of fluid purity can be as critical to wafer yield as the absolute purity of the fluids. Therefore, it is important that measurement methods detect sufficient number of events to ensure confidence in measured particle concentrations. Development of other statistically significant particle counting methods or a higher sample volume particle counter is needed to improve confidence in reported particle counts. The sample volume (volume of fluid measured) will determine the number of particle counts that are detected during the sample interval. *Refer to Supplemental Information link for more detail.*

Although the gas/liquid chemical section of Table 115 shows an essentially flat purity trend, there is a likelihood that specific process steps may require higher purity. Yield improvements may be achieved more by reducing variations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials.

Gases and liquid chemicals—The recommended minimum contaminant values in Table 115 represent typical gas/liquid chemical quality in use from 2005 and beyond, to manufacture the most advanced devices. In many applications, the requirements for the contaminants in these gases and/or liquid chemicals may be more relaxed. On the other hand, some manufacturers have claimed benefits from lower contaminant levels. Considering that a given process can be run successfully within a "window" defined by a range of material purity and also by ranges in other parameters (purging time, etc.), it follows that, in practice, trade-offs exist between imposed purity requirements, process throughput, etc. Pushing a process to the upper limit of its "purity window" may require significant investment of time and effort in optimizing other parameters, and the economics of pursuing that effort will depend on the environment. It may also be that benefits attributed to low contaminant levels are more attributable to the reduction in contaminant variations achieved with high-purity process gases and chemicals. Currently achievable purity levels for gases and chemicals used in semiconductor manufacturing are expected to be sufficient for multiple generations, with yield improvements being achieved more by reducing variations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials.

While purity measurements at the POP (that is, in the processing chamber itself), would provide the most direct correlation between gas or liquid quality and process performance, these measurements are often very difficult to obtain with the exception of certain fluid properties in wafer immersion baths. Examples include both particulate generation during plasma processes and wafer outgassing. The latter is the most important source of water vapor contamination in many processes, often obscuring moisture contributions from the process fluid. Measurements at the POU provide the most direct information of the quality of process fluids going directly into the process chamber, but these are also not available for many of the common processes.

Because of these difficulties, the values in Table 115 are intended to represent POE, defined as the inlet to the process tool as described in Table 108. There are sufficient measurement data on bulk gases and aqueous fluids to provide guidance with regard to POE impurity levels for many applications, although measurements on these fluids are often performed at the POS, POD, or POC. For these materials, which are relatively unreactive and delivered in large volume, the extrapolation to POE is generally very reasonable. In the case of Specialty Gases and other reactive process fluids, such extrapolation is more delicate because delivered volumes are smaller, increasing sensitivity to contamination effects, and degradation in the distribution system related to materials of construction, atmospheric contamination, thermal degradation, etc. is more likely. These factors are minimized with normal best construction and operations practices, and therefore the best guidance available is often regarding POS specification and to a lesser extent POD or POC measurements, which are interpreted as equivalent to POE. In summary, while the intention is to recommend POE purity levels for all gases, in practice, the supporting data has more often been collected at POS, POD, or POC.

The targeted levels can be reached either by bulk delivery of a fluid with requisite purity or through use of a local purifier. Care should be taken, at a minimum, to maintain the quality of the gas coming from the source, ensuring that contamination is not added downstream of the POS, as may occur due to particle generation at components, moisture outgassing, byproduct generation due to incompatible materials, etc. Particle filtration as close to the POU as possible is generally advisable for gases. For the most critical applications a local purifier may be used to enhance or ensure ultimate purity at the POU. In those cases, the prevailing approach is to seek POC levels that are adequate for the process and to view the purifier as "insurance." The challenge to the purifier is minimal, and long purifier lifetimes can normally be expected.

Liquid chemicals—Tables 115a and b summarize the purity requirements for liquid chemicals delivered to process tools. Pre-diffusion cleaning requirements drive the most aggressive impurity levels. Liquid particle level targets are shown to become purer each technology generation. Particle counters currently are capable of measuring only to 65 nm for liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes, but this will be influenced by the level of filtration utilized. The ability to accurately analyze organic, anion, and cation contamination in process chemicals is becoming more critical to successful wafer processing. With the increased use of CMP and plating chemicals, there must be a better understanding of purity requirements for the delivered chemicals. Table 115 contains only very generic comments with regard to CVD/ALD precursors. The variety of layers and the respective contaminants is enormous. Therefore, links to *ion list summary* and *precursor* tables are provided in the supplementary materials.

Bulk/specialty gases—The major bulk gases are listed separately in Table 115. Although no specific information is available that would indicate that the requirements for these gases will need to be improved for future generations in the roadmap, the table does anticipate improvements at 45 nm.

As indicated in the table, total hydrocarbons (THC) are often specified in the Bulk Gases. While not all hydrocarbons are equally detrimental, THC measurement is conveniently achieved with a flame ionization detector (FID). The FID response is roughly proportional to the number of C-atoms in a hydrocarbon, as well as its concentration, and it is usually calibrated with methane (hence the THC concentration is reported "as methane"). Atmospheric pressure ionization mass spectroscopy may also be used for THC measurement by monitoring the CH_4^+ peak or another peak (depending upon ionization conditions). The response to larger hydrocarbons will depend on the nature of the molecule and the analysis conditions, but the quantification of THC will again be typically based on calibration with methane standards. As a practical matter, for levels above 100 ppb, the straightforward FID THC measurement is recommended. APIMS will give satisfactory results to 10 ppt.

For some processes, such as advanced lithography, very small quantities of "high molecular weight/high boiling point" (e.g., C_6-C_{30}) hydrocarbons are detrimental because of increased adherence to the exposed surfaces, and potential for photochemical degradation to leave non-volatile residues on lenses, masks, mirrors, etc. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities. In order to detect such species with ultimate sensitivity, it is necessary to directly detect the relevant species and calibrate the analyzer with the appropriate standard. The methods used are analogous to those for AMC, such as TD gas chromatography (GC)/mass spectroscopy (MS) (TD = thermal desorption) or TD GC/FID, or ion mobility spectroscopy (IMS). Even these approaches may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks. For methods using adsorbent traps, it is very important to determine the trap efficiency. Using APIMS to provide real time measurement of individual hydrocarbons is possible, in principle, but calibration is difficult, because larger hydrocarbons are collisionally dissociated in the ionization process.

A compromise approach that has gained some acceptance is to use TD GC/MS and sum all peaks corresponding to C6 and higher. The instrument is usually calibrated with a multi-component standard and results are reported "hexadecane". While the quantization provided by this method is approximate, and some species may be overlooked, it does at least emphasize the heavier hydrocarbons while providing a straightforward calibration.

Applications for both O_2 and H_2 generally tolerate higher levels of N_2 contamination than other contaminants and the table reflects this observation. Requirements for critical clean dry air (CDA), lithography purge gases, and supercritical CO_2 supply are included. Whereas critical CDA may not always be conveniently or cheaply available, there is no technological barrier to its production. Analytical methods are usually the same as used for airborne molecular contamination in cleanroom air, such as bubbling through ultrapure water (for metals, sulfates, amines, etc.) or trapping on an adsorbent trap for organics. In each case, the sampler concentrates impurities so that requisite sensitivities are achieved when the sample is introduced to the analyzer (ICP-MS or ion chromatography for aqueous samples, GC-MS for desorption of organics). Such methods are time consuming by nature, and direct methods would be preferred if available. However, there is no apparent pressing need for real-time analysis. For SO_2 there are convenient on line methods, e.g., UV fluorescence.

For specialty gases, contaminant values in etchants, dopants, and deposition gases have been included in the table. Values for particulate contamination are omitted, since online monitoring of particle concentrations is not commonly practiced and the efficacy of POU particle filters is well established. Whereas there is evidence that the most demanding applications, such as low temperature epi and its cleaning gases, will continue to benefit from improvements in purity as deposition temperatures are lowered, this is expected to be reflected in wider use of the best available purity rather than substantial improvements of those levels. For both bulk and specialty gases, tighter control of purity is anticipated to be more important than improvement in absolute purity levels. This will require a shift towards statistical process control of contamination levels in gas production rather than absolute elimination of contaminants.

Novel materials—Impurity specifications for novel materials used in processing will be increasingly important. Specifications for critical materials such as novel metal oxides, CMP slurries, low/high dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied. Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements. Additional detail on the variety of thin film precursors under consideration can be found in Liquid Chemicals section of Table 115.

Design-to-process interactions—Data, test structures, and methods are needed to identify and control yield-detracting contaminants in the wafer environment, airborne and process critical materials, and ultra pure water. The need for standard test structures is critical in determining defect sources and mechanisms. Once the design process interactions are understood, device design ground rules may be established and communicated that decrease process sensitivity. Cycles of process sensitivity analysis and reduction will be critical to advancing device design and yield. Additionally, sensitivities of designs to various levels of random defects need to be considered in the design process.

Process-to-process interactions—Interactions that result in defect formation (such as thickness of photoresist and contact density can affect the level of residue inside a via/contact) between process steps may drive particular requirements to a tool or process upstream or downstream that are not necessarily germane to that tool or process. Cluster tools and wet sinks are two examples of tools that must be carefully designed to ensure that their modules do not transfer any contaminants that degrade the performance of adjacent modules. To detect, to understand, and to eliminate unwanted process interactions, process monitoring and control will play a key role. The appropriate sensors and data must be available, along with an appropriate information management system to correlate process parameters to upstream/downstream parameters and yield and provide smart, inter-tool and intra-tool statistical process control (SPC).

Table 115a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Wafer Environment Control such as Cleanroom, SMIF POD, FOUP, etc….not necessarily the cleanroom itself but wafer environment.									
Critical particle size (nm) [A]	**40**	**35**	**33**	**29**	**25**	**23**	**20**	**18**	**16**
Number of particles (/m^3) [A] [B]	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**
Airborne Molecular Contaminants in Gas Phase (pptM)) [C] [G] [M]									
Lithography (cleanroom ambient) [V]									
Total acids (as SO_4) including organic acids	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
Total bases (as NH_3)	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane)	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**
Refractory compounds (organics containing S, P, Si)	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Gate wafer environment (cleanroom/POD/FOUP ambient)									
Total metals (as Cu) [H]	**1**	**1**	**1**	**1**	**1**	**0.5**	**0.5**	**0.5**	**0.5**
Dopants [D] (front end of line only)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/week [M]*	**2**	**2**	**2**	**2**	**2**	**0.5**	**0.5**	**0.5**	**0.5**
Salicidation Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total acids (as SO_4) including organic acids	**100**	**100**	**100**	**100**	**100**	**10**	**10**	**10**	**10**
Exposed Copper Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Exposed Aluminum Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Total oxidizing species (as Cl_2)	**1000**	**1000**	**1000**	**1000**	**1000**	**500**	**500**	**500**	**500**
Reticle Exposure (Cleanroom/POD/Box ambient)									
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**TBD**	**TBD**	**TBD**	**TBD**
Total bases (as NH_3)	**2500**	**2500**	**2500**	**2500**	**2500**	**TBD**	**TBD**	**TBD**	**TBD**
General Wafer Environment (Cleanroom/POD/FOUP ambient, all areas unless specified below)									
Total acids (as SO_4) including organic acids	**1000**	**1000**	**1000**	**1000**	**1000**	**500**	**500**	**500**	**500**
Total bases (as NH_3)	**5000**	**5000**	**5000**	**5000**	**5000**	**2500**	**2500**	**2500**	**2500**
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane)	**4000**	**3500**	**3000**	**3000**	**2500**	**2500**	**2500**	**2500**	**2500**
Dopants [E] (front end of line only)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/day [M]*	**2**	**2**	**2**	**2**	**2**	**0.5**	**0.5**	**0.5**	**0.5**
Front-end processes, bare Si, total dopants added to 24-hour witness wafer, atoms/cm_2 [D] [M]	**2.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**
Front-end processes, bare Si, total metals added to witness wafer, atoms/cm_2 [F] [M]	**2.00E+10**	**2.00E+10**	**2.00E+10**	**2.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

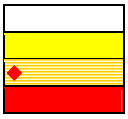


Table 115a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Process Critical Materials [G]									
Ultrapure Water [L]									
Resistivity at 25°C (MOhm-cm)	18.2	18.2	18.2	18.2	18.2	18.2	18.2	18.2	18.2
Total oxidizable carbon (ppb) POE	<1	<1	<1	<1	<1	<1	<1	<1	<1
Bacteria (CFU/liter)	<1	<1	<1	<1	<1	<1	<1	<1	<1
Total silica (ppb) as SiO_2 [P]	<0.5	<0.5	<0.5	<0.5	<0.5	<0.3	<0.3	<0.3	<0.3
Number of particles > critical size (/ml) [A] POE	◆<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
Dissolved oxygen (ppb) (contaminant based) [N] POE	<10	<10	<10	<10	<10	<10	<10	<10	<10
Dissolved nitrogen (ppm) [J]	8–12	8–12	8–18	8–18	8–18	8–18	8–18	8–18	8–18
Critical metals (ppt, each) [F]	<1	<1.0	<1.0	<0.5	<0.5	<0.5	<0.5	<0.5	<0.5
Other critical ions (ppt each) [W]	<50	<50	<50	<50	<50	<50	<50	<50	<50
Temperature stability (K) POE	± 1	± 1	± 1	± 1	± 1	± 1	± 1	± 1	± 1
Temperature gradient in K/10 minutes [U] POE for immersion photolithography	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
Liquid Chemicals [F]									
49% HF: number of particles > critical size (/ml) [A] [K]	◆<10	<10	<10	<10	<10	<10	<10	<10	<10
37% HCl: number of particles > critical size (/ml) [A] [K]	◆<10	<10	<10	<10	<10	<10	<10	<10	<10
30% H_2O_2: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
29% NH_4OH: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
100% IPA: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
49% HF: Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Pd, Pt, Ru) (ppt, each) [S]	150	150	150	150	150	150	150	150	150
49% HF: Cl (ppb, each)	10	10	10	10	10	10	10	10	10
30% H_2O_2: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [S]	150	150	150	150	150	150	150	150	150
30% H_2O_2: Br, F (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
29% NH_4OH: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [S]	150	150	150	150	150	150	150	150	150
100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Ca (ppt, each)	150	150	150	150	150	150	150	150	150
100% IPA: Cl, Br (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
100% IPA: NH_4 (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Table 115a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Liquid Chemicals [F] (continued)									
49% HF: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
30% H_2O_2: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
29% NH_4OH: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
100% IPA: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
49% HF: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
29% NH_4OH: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30% H_2O_2: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
100% IPA – Specific organic acids: formate, acetate, citrate, proprionate, oxalate (ppt, each)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
IPA: High molecular weight organics (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30%H_2O_2: resin byproducts (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: K, Ni, Cu, Cr, Co, (ppt)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
96% H_2SO_4: K, Ni, Cu, Cr, Co, (ppt)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
37% HCl: all other metals not listed in row above (ppt, each) [R]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
96% H_2SO_4: all other metals not listed in row above (ppt, each) [R]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
BEOL solvents, strippers K, Li, Na, (ppt, each)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
Planar slurries: scratching particles (/ml > key particle size) [I] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: particles>critical size (/ml) [A] [K] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: elements TBD (ppt, each) [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [A] [K] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., Trimethylsilane, Tetramethylsilane) [X]									
Metals (ppb)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
H_2O and other oxygen containing impurities (ppm)	**<10**	**<10**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**

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Interim solutions are known
Manufacturable solutions are NOT known

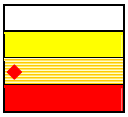

Table 115a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Bulk Gases (Contaminants, ppbv)									
N_2 (O_2, H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<1**	**<1**	**<1**	**<1**
O_2 (N_2, Ar)	**<50**	**<50**	**<50**	**<50**	**<50**	**<25**	**<25**	**<25**	**<25**
O_2 (H_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<5**
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<1**	**<1**	**<1**	**<1**
H_2 (N_2, Ar)	**<50**	**<50**	**<50**	**<50**	**<50**	**<25**	**<25**	**<25**	**<25**
H_2 (O_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<5**
He (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<5**
CO_2 (CO, H_2O, O_2, THC)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Lithography Purge Gases									
Critical clean dry air (H_2O)	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**
Critical clean dry air (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Critical clean dry air (total base as NH_3) (ppb)	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**
Critical clean dry air (NH_3 (as NH_3)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Critical clean dry air (total acid including SO_2 (as SO_4)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Critical clean dry air (SO_4 (as SO_4)) (ppb)	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**
Lithography nitrogen tool/maintenance purging gas supply (H_2O, O_2, CO_2) (ppb)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
Lithography nitrogen tool/maintenance purging gas supply (CO) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (H_2) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppbV)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Lithography nitrogen tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography nitrogen tool/maintenance purging gas supply (total acid (as SO_4) including SO_2) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography nitrogen tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppbw)	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Lithography helium tool/maintenance purging gas supply (H_2O) (ppb)	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**
Lithography helium tool/maintenance purging gas supply (O_2, CO_2) (ppb)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

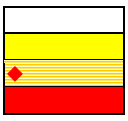

Table 115a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Bulk Gases (Contaminants, ppbv) (continued)									
Lithography helium tool/maintenance purging gas supply (CO, H_2) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography helium tool/maintenance purging gas supply (organics(molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Lithography helium tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography helium tool/maintenance purging gas supply (total acid including SO_2 (as SO_4)) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography helium tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppbw)	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Number of particles > critical size (/M^3) [A]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
Specialty Gases									
Etchants (Corrosive, e.g., BCl_3, Cl_2)									
O_2, H_2O (ppbv)	**<1000**	**<500**	**<500**	**<500**	**<100**	**100**	**100**	**100**	**100**
Critical specified metals/total metals (ppbw) [Q]	**<10/1000**	**<10/1000**	**<10/1000**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Etchants (Non-corrosive, e.g., C_2F_6, NF_3)									
O_2, H_2O (ppb)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**100**	**100**	**100**	**100**
Deposition (e.g., SiH_4, NH_3, $(CH_3)_3SiH$)									
O_2, H_2O (ppb)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**100**	**100**	**100**	**100**
Critical specified metals/total metals (ppbw) [Q]	**<10/1000**	**<10/1000**	**<10/1000**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Dopants (e.g., AsH_3, PH_3, GeH_4)									
O_2, H_2O (ppb)	**<1000**	**<500**	**<500**	**<500**	**<100**	**100**	**100**	**100**	**100**
Inerts for purging									
O_2, H_2O (ppb)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
He, H_2 cylinder carrier/purge gases (N_2, H_2O, ppb)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Manufacturable solutions exist, and are being optimized
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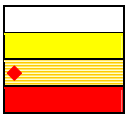

Table 115b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Wafer Environment Control such as Cleanroom, SMIF POD, FOUP, etc….not necessarily the cleanroom itself but wafer environment.							
Critical particle size (nm) [A]	**14**	**13**	**11**	**10**	**9**		
Number of particles (/m^3) [A] [B]	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**
Airborne Molecular Contaminants in Gas Phase (pptM)) [C] [G] [M]							
Lithography (cleanroom ambient) [V]							
Total acids (as SO_4) including organic acids	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
Total bases (as NH_3)	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**	**50000**
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane)	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**
Refractory compounds (organics containing S, P, Si)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Gate Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total metals (as Cu) [H]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Dopants [D] (front end of line only)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/week [M]*	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Salicidation Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total acids (as SO_4) including organic acids	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Exposed Copper Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Exposed Aluminum Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Total oxidizing species (as Cl_2)	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Reticle Exposure (Cleanroom/POD/Box ambient)							
Total acids (as SO_4) including organic acids	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total bases (as NH_3)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
General Wafer Environment (Cleanroom/POD/FOUP ambient, all areas unless specified below)							
Total acids (as SO_4) including organic acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Total bases (as NH_3)	**2500**	**2500**	**2500**	**2500**	**2500**	**2500**	**2500**
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane)	**2500**	**2500**	**2500**	**2500**	**2500**	**2500**	**2500**
Dopants [E] (front end of line only)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/day [M]*	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Front-end processes, bare Si, total dopants added to 24-hour witness wafer, atoms/cm^2 [D] [M]	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**
Front-end processes, bare Si, total metals added to witness wafer, atoms/cm^2 [F] [M]	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**	**1.00E+10**

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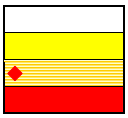

Table 115b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Process Critical Materials [G]							
Ultrapure Water [L]							
Resistivity at 25°C (MOhm-cm)	18.2	18.2	18.2	18.2	18.2	18.2	18.2
Total oxidizable carbon (ppb) POE	<1	<1	<1	<1	<1	<1	<1
Bacteria (CFU/liter)	<1	<1	<1	<1	<1	<1	<1
Total silica (ppb) as SiO_2 [P]	<0.3	<0.3	<0.3	<0.3	<0.3	<0.3	<0.3
Number of particles > critical size (/ml) [A] POE	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
Dissolved oxygen (ppb) (contaminant based) [N] POE	<10	<10	<10	<10	<10	<10	<10
Dissolved nitrogen (ppm) [J]	8–18	8–18	8–18	8–18	8–18	8–18	8–18
Critical metals (ppt, each) [F]	<0.5	<0.5	<0.5	<0.5	<0.5	<0.5	<0.5
Other critical ions (ppt each) [W]	<50	<50	<50	<50	<50	<50	<50
Temperature stability (K) POE	± 1	± 1	± 1	± 1	± 1	± 1	± 1
Temperature gradient in K/10 minutes [U] POE for immersion photolithography	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
Liquid Chemicals [F]							
49% HF: number of particles > critical size (/ml) [A] [K]	<10	<10	<10	<10	<10	<10	<10
37% HCl: number of particles > critical size (/ml) [A] [K]	<10	<10	<10	<10	<10	<10	<10
30% H_2O_2: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000
29% NH_4OH: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000
100% IPA: number of particles > critical size (/ml) [A] [K]	<1000	<1000	<1000	<1000	<1000	<1000	<1000
49% HF: Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Pd, Pt, Ru) (ppt, each) [S]	150	150	150	150	150	150	150
49% HF: Cl (ppb, each)	10	10	10	10	10	10	10
30% H_2O_2: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [S]	150	150	150	150	150	150	150
30% H_2O_2: Br, F (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
29% NH_4OH: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [S]	150	150	150	150	150	150	150
100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Ca (ppt, each)	150	150	150	150	150	150	150
100% IPA: Cl, Br (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
100% IPA: NH_4 (ppt, each)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
49% HF: All other metals not listed in row above (ppt, each) [R]	500	500	500	500	500	500	500
30% H_2O_2: All other metals not listed in row above (ppt, each) [R]	500	500	500	500	500	500	500

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

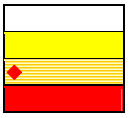

Table 115b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Liquid Chemicals [F] (continued)							
29% NH_4OH: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**
100% IPA: all other metals not listed in row above (ppt, each) [R]	**500**	**500**	**500**	**500**	**500**	**500**	**500**
49% HF: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
29% NH_4OH: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30% H_2O_2: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
100% IPA – Specific organic acids: formate, acetate, citrate, proprionate, oxalate (ppt, each)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
IPA: High molecular weight organics (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30%H_2O_2: resin byproducts (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: K, Ni, Cu, Cr, Co, (ppt)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
96% H_2SO_4: K, Ni, Cu, Cr, Co, (ppt)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
37% HCl: all other metals not listed in row above (ppt, each) [R]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
96% H_2SO_4: all other metals not listed in row above (ppt, each) [R]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
BEOL solvents, strippers K, Li, Na, (ppt, each)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
Planar slurries: scratching particles (/ml > key particle size) [I] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: particles>critical size (/ml) [A] [K] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: elements TBD (ppt, each) [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [A] [K] [O]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., Trimethylsilane, Tetramethylsilane) [X]							
Metals (ppb)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
H_2O and other oxygen containing impurities (ppm)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
Bulk Gases (Contaminants, ppbv)							
N_2 (O_2, H_2, H_2O, CO, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
O_2 (N_2, Ar)	**<25**	**<25**	**<25**	**<25**	**<25**	**<25**	**<25**
O_2 (H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
H_2 (N_2, Ar)	**<25**	**<25**	**<25**	**<25**	**<25**	**<25**	**<25**
H_2 (O_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
He (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
CO_2 (CO, H_2O, O_2, THC)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
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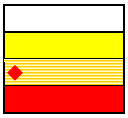

Table 115b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Bulk Gases (Contaminants, ppbv) (continued)							
Lithography Purge Gases							
Critical clean dry air (H_2O)	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**
Critical clean dry air (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Critical clean dry air (total base as NH_3) (ppb)	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**
Critical clean dry air (NH_3 (as NH_3)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Critical clean dry air (total acid including SO_2 (as SO_4)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Critical clean dry air (SO_4 (as SO_4)) (ppb)	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**
Lithography nitrogen tool/maintenance purging gas supply (H_2O, O_2, CO_2) (ppb)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
Lithography nitrogen tool/maintenance purging gas supply (CO) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (H_2) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (organics(molecular weight > benzene) normalized to hexadecane equivalent) (ppbV)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Lithography nitrogen tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography nitrogen tool/maintenance purging gas supply (total acid (as SO_4) including SO_2) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography nitrogen tool/maintenance purging gas supply (refractory compounds (Organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppbw)	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Lithography helium tool/maintenance purging gas supply (H_2O) (ppb)	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**
Lithography helium tool/maintenance purging gas supply (O_2, CO_2) (ppb)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
Lithography helium tool/maintenance purging gas supply (CO, H_2) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography helium tool/maintenance purging gas supply (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**	**<22**
Lithography helium tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography helium tool/maintenance purging gas supply (total acid including SO_2 (as SO_4)) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography helium tool/maintenance purging gas supply (refractory compounds (Organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppbw)	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Number of particles > critical size ($/M^3$) [A]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Manufacturable solutions exist, and are being optimized
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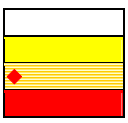

Table 115b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Specialty Gases							
Etchants (Corrosive, e.g., BCl_3, Cl_2)							
O_2, H_2O (ppbv)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Critical specified metals/total metals (ppbw) [Q]	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Etchants (Non-corrosive, e.g., C_2F_6, NF_3)							
O_2, H_2O (ppb)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Deposition (e.g., SiH_4, NH_3, $(CH_3)_3SiH$)							
O_2, H_2O (ppb)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Critical specified metals/total metals (ppbw) [Q]	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Dopants (e.g., AsH_3, PH_3, GeH_4)							
O_2, H_2O (ppb)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Inerts For Purging							
O_2, H_2O (ppb)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
He, H_2 cylinder carrier/purge gases (N_2, H_2O, ppb)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

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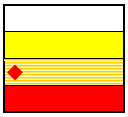

Notes for Tables 115a and b:
** Based on SEMI MF 1982-1103*[5]

*[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles. Because of instrumentation limitations, particle densities at the critical dimension < 90 nm will need to be estimated from measured densities of larger particles and an assumed particle size distribution or determined empirically and extrapolated. The particle size distribution will depend on the fluid (e.g. water, clean room air, gases), f(x)=K*1/X^n (where n=2.2 for air/gases, n varies significantly for liquids from 1 to 4, empirical determination is recommended)* [6, 7]

[B] Airborne particle requirements are based on ISO 14644-1 at "at rest".[8]

[C] Ion/species indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography projections is defined by lithography tool suppliers. Metals and organics scale as defined in the surface preparation roadmap for metallics and organics. Values listed in table are based on experience, however, all airborne molecular contaminants can be calculated as S=E(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1), N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second). The following sticking coefficients have been proposed; SO4 = 1×10¯5, NH3 = 1×10¯6, Cu = 2×10¯5. The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general, molecular weights < 250 are not considered detrimental due to the higher volatility of these compounds.*

[D] Includes P, B, As, Sb.

[E] Contaminant targets apply up to POU. POU is defined as the entry point of the wafer process chamber within the process tool; measurement of fluid purity within the tool can be difficult to impossible, however fluid purity is not expected to change through the tool's plumbing so long as proper components are selected and installed correctly. Values in the Liquid Chemicals section of this table represent typical levels that can usually be tolerated in manufacturing processes at the specified generation.

[F] Critical metals and ions may include: Al, As, Ba, Ca, Co, Cu, Cr, Fe, K, Li, Mg, Mn, Na, Ni, Pb, Sn, Ti, Zn.
Three different case studies were reviewed where the levels of Ca, Fe, and Ni in the UPW resulted in levels of problem densities (atoms/sq cm) on the wafer. These were reduced to acceptable levels by reducing the level of these elements in the UPW to levels well below 10 ppt. In only one case does the data exist that showed success by obtaining values below 0.5 ppt. In the other two, the problem existed at some level below 10 PPT (detection limit in UPW at the time). When additional ion exchange was added the problem went away. It is reasonable to assume that the ion exchange reduced the level by an order of magnitude. These results drive the 1.0 ~ 0.5 ppt values.

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[5] *SEMI MF1982-1103 (previously ASTMF 1982–99e1), "Standard Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography," SEMI.*
[6] *Cooper, D. W., "Comparing Three Environmental Particle Size Distributions," Journal of th eIES, Jan/Feb 1001, 21–24.*
[7] *Pui, D. Y. H. and Liu, B.Y.H., "Advances in Instrumentation for Atmospheric Aerosal Measurement," TSI Journal of Particle Instrumentation, Vol 4. (2), Jul–Dec 1989, 3–2.*
[8] *ISO 14644-1 Cleanrooms and Associated Controlled Environments—Part 1: Classification of Air Cleanliness.*

[G] Units on all contaminants in Table 115 are often given as ppb (or ppm or ppt, we use ppb here solely for demonstration purposes). The reader should be aware that these units of parts per billion (ppb) may be ppb by mass, volume, or molar ratios. Where not designated, the following guidelines apply: Chemicals and UPW are typically ppb by mass, gases and clean room are typically ppb by volume. In the case of the fluid acting as an ideal gas, ppb by volume is equal to ppb molar. The notable exception to the above is metals in gases that are ppb by mass.

[H] Detection of metals at the levels indicated will be dependent on sampling time and flow rate.

[I] Key particle size for scratching particles depends on mean particle size of slurry. Target level will be specific to slurry and wafer geometry sensitivity.

[J] The Dissolved Nitrogen range is solely for the physical process needs of megasonics cleaning. Processes without megasonics cleaning can ignore the line item. The concentration is process specific and needs to be determined by the end user. Factors to consider include UPW temperature and megasonic energy input at the tool. Increasing nitrogen concentration without adjusting megasonic energy input could result in over aggressive cleaning. Caution must be exercised in gas addition with regard to bubble formation, particularly in that the solubility of the gases in hot UPW is lower at higher temperature, for example N_2 saturation for UPW in equilibrium with air ranges from 15.7 ppm @ 20C to 10.7 ppm @ 70C. Other gases can be used and they may have different optimum levels. Process enhancements through chemistry associated with the other gases are outside of the scope of this chapter.

[K] As of the current year's update the finest sensitivity liquid particle sensor for chemicals is 0.065 µm. Values obtained by these particle counters are not directly comparable to the roadmap values and need to be normalized to critical particle size values in the roadmap using the equation and methods of Footnote A above. Interim solution to higher sensitivity particle counter is to collect data over longer time period to provide greater precision in the data near the threshold sensitivity of the counter.

[L] Most benchmark data has been collected at POD or POE and is the basis for parameters in Table 115. Where contaminant levels have been extended to POU this has been done based on engineering judgment assuming the semiconductor-processing tool is well designed with regards to maintaining fluid purity in accordance with applicable SEMI standards. Values in the Table are for POU unless otherwise noted.

[M] Single wafer shall be oxidized to make organic-free, then wafer shall be exposed for 24 hours and top side analyzed by TD-GC-MS with 400°C thermal desorption, and quantitation based on hexadecane external standard. TIC response factor per SEMI MF 1982-1103 (formerly ASTM 1982-99).[9] Limits determined by above method are a guideline for many organics. Note higher limits can be used for process wafers oxidized or cleaned prior to subsequent process step. Processes such as gate oxide formation, or polysilicon deposition, may be more sensitive to organics, especially high boilers such as DOP. Silicon nitride nucleation may also be more sensitive than above for some processes. Please note dopants requirement is covered in earlier section

Single wafer is first stripped with HF to yield dopant-free surface and than exposed for 24 hours. Topside of wafer is analyzed by methods known to give reliable recovery of boron. This is a guideline for dopants based on sampling in operating running fabs. Lower specifications may be required for key FEPs, especially for smaller geometries, lower thermal budgets, and for lightly doped devices. If wafers are stripped with HF or BOE immediately prior to next thermal process, then steps may become less sensitive to surface molecular dopants, and higher limits apply. Note that BEPs tend to be orders of magnitude less sensitive to dopants than FEPs.

Single wafer known to meet the ITRS FEP spec of 1E10 atoms/cm^2, from the Starting Materials table, is exposed to a clean environment for 24 hours. Subsequent analysis of top surface by vapor phase desorption (VPD)-ICP-MS or VPD-GFAA. Lower specifications may be required for key FEPs, especially for smaller geometries. If wafers are cleaned prior to the next thermal process, then air exposure during earlier steps may be less of an issue. Note that majority of environmental metallic contaminants are particles, not molecular. If total particles on wafers are kept in spec than majority of metals, most metals from the environment should be within specifications. Back-end processes (BEPs) tend to be less sensitive to metals that FEPs provided not particles. Specs of twice the incoming wafer specs are readily achievable and readily measurable in case of wafers exposed for 24 hours.

A 24-hour exposure will accentuate the contamination per wafer as wafers are often exposed too much shorter times in actual processing. The above SMC (surface molecular contamination) limits are preliminary, and no single value applies to all process steps or types of organics, dopants or metals. The SMC limits can vary substantially from process to process, and local air purification or purges may be needed to control contaminant levels.

[N] Dissolved oxygen (DO) has an effect on the etch rate of non H-passivated SiO2 and copper structures. The level in the Table is that of the most stringent. It is not expected that slightly higher levels within the same order of magnitude would have any significant effect on manufacturing processes. It is known that some fabs consider DO a process variable and operate at DO levels 3 orders of magnitude higher than stated in the Table. Etch rates as a function of DO is not a linear relationship for all materials, specifically copper etch rates are near a maximum at 300 ppb DO.

[O] Uncertain at this time what target levels might be set given the variety of chemistries used in the industry and unknown sensitivity of the wafer to particles or ionic contamination in the chemical. This parameter is identified as a potentially critical one that should be considered and work is ongoing to define the correct levels.

[P] Total Silica in UPW is a source of wafer water spots. Silica dissolved from the wafer surface is also a significant source for water spotting. The values in the Table are based on concentrations found in typical fabricators manufacturing 90 nm geometry devices. As device geometries shrink lower silica concentration requirements are expected. Research is needed to develop a clear correlation between UPW concentrations and water spots. Boron and Reactive Silica have been removed from the Table as UPW operational parameters, values of 50 ppt and 300 ppt respectively. These two species remain valuable indicators of ion exchange resin removal capacity, as they are the first two ions to leak from a mixed bed. They have been removed from the table as they are not process critical at typical UPW system concentrations.

[Q] The list of critical metals (e.g., Al, Ca, Cu, Fe, Mg, Ni, K, Si, Na) varies from process to process depending on the impact on electrical parameters such as gate oxide integrity or minority carrier lifetime as well as mobility of the metal in the substrate. The metals listed in note [G] for liquid process chemicals are of concern but the issues around metals in specialty gases are primarily around the potential for corrosion to add metal particles to the gas flow (e.g., Fe, Ni Co, P). The potential for volatile species containing metals must be considered for each specialty gas but are generally not present in the bulk gases.

[R] The following is a complete list of metal ions of concern in certain liquid chemicals: Ag, Al, As, Au, Ba, Ca, Cd, Co, Cr, Cu, Fe, K, Li, Mg, Mn, Mo, Na, Ni, P, Pb, Pd, Pt, Ru, Sb, Sn, Sr, Ti, V, W, Zn.

[S] Elements listed that are not in parentheses may cause high or some risk to device quality and may often be present in process chemicals. Elements listed that are in parentheses may cause high risk to device quality but are not typically present in process chemicals.

[T] Contamination levels are time based, ng/cm^2/week. Total contamination levels on reticles that cause problems also vary with energy exposure. These guidelines subject to change with new data currently being generated.

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[9] SEMI MF1982-1103 (previously ASTMF 1982–99e1), "Standard Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography," SEMI.

[U] This temperature stability requirement is for immersion photolithography tools, using UPW as an immersion fluid, and based upon utility requirements projected by some tool manufacturers in 2005. It represents the maximum rate of change of the temperature of the cold UPW supplied to the tool in order for the tool to maintain process required temperature stability.

[V] The photolithography AMC guidelines are based on inputs from the photolithography tool supplier. All photolithography tools should have chemical filters on the makeup air to the internals of the tools. These filters have a finite lifetime, which is dependent on the contaminant loading. Providing a chemically cleaner environment will extend the life of these filters.

[W] Other critical ions may include inorganic ions such as Fluoride, Chloride, Nitrate, Nitrite, Phosphate, Bromide, Sulfate as well as ammonium. However no reference was currently found that these ions in typical concentrations found in ultrapure water up to 50 ppt have any impact on the process. Also for organic anions such as acetate, formate, propionate, citrate, and oxalate no harmful levels have been established up to now.

[X] The variety of CVD and ALD precursors is continuously increasing as well as their applications. The contaminant types and levels vary widely due to the different chemical behavior. An overview about typical precursors is therefore given in the linked Precursor table.

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

The defect budget validation results obtained by SEMATECH in 1997, 1999, and 2000 have been used for the 2001, 2003 and 2005 revisions. Another new survey is strongly needed to validate future defect budgets. Research into better yield modeling techniques is required to address future modeling challenges. Modeling of systematic mechanisms limited yield is increasingly becoming a significant focus of yield learning experts. This is being driven by the fact that SMLY issues tend to dominate in the early yield ramp stages, and these yield ramp rates continue to accelerate. In addition, parametric limited yield issues and design to process mismatch tend to limited yield in the early ramp timeframe. Furthermore, the recent process variation caused by line edge roughness is looming ahead. The increasing dominance of non-visual defects will further complicate yield modeling and defect budgeting. Thus, defect models will need to better consider electrical characterization information, and reduce emphasis on visual analysis. This will require research into new characterization devices and methods. Interconnect process layers are a particular challenge and have been so identified in the technology requirements. Some issues include modeling the yield impacts of ultra-thin film integrity, increased process complexity, interconnect speed and transmission characteristics, and the impact of wavelength dependent defects on reticles that may or may not result in defects. This research is complicated by the lack of state-of-the-art semiconductor processing capabilities in universities and other research sources. Figure 102 illustrates a few potential solutions that may help address the technology requirements for future yield modeling.

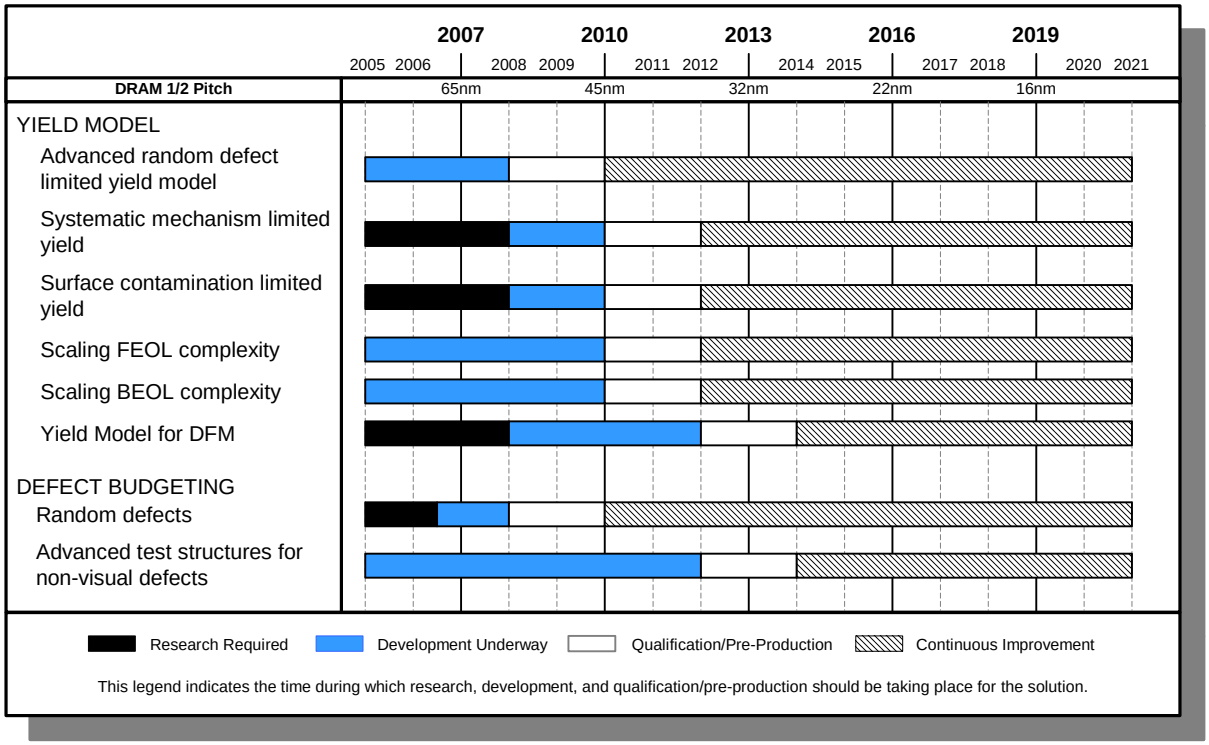

Figure 102 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION AND CHARACTERIZATION

Considerable research and development is now necessary to meet the technology requirements for advanced defect detection tools. The research and development should focus on methods to filter out the defects of interest automatically. Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. Arrayed detection schemes for parallel data acquisition from a larger area of the wafer need to be explored.

There is a lack of suitable component technologies for developing novel detection systems. Significant advancement associated with shorter wavelengths, continuous-wave lasers, detectors with higher quantum efficiency and higher

acquisition speed, suitable low-loss and low-aberration lenses, waveplates and polarizers, and robust mechanical and acousto-optic scanners are needed now to continue the economical development of optical techniques.

Potential solutions must comprehend the need for greater amounts of defect-related data, e.g., composition, shape, defect classification, and rapid decision-making. (Refer to the following section on Yield Enhancement for a comprehensive explanation of the needs in this area.) Automated defect classification, spatial signature analysis, adaptive sampling, yield-impact assessment, and other algorithmic techniques still need to be improved significantly in order to be used to its full capability. Defect detection and characterization equipment must produce more defect descriptive information for these techniques to analyze. The challenge of improved sensitivity to smaller defect sizes has moved characterization platforms inline to provide higher resolution. The trade-off between associated throughput and the provided information is crucial. Thereby, defect detection is evolving closer to the defect source. Development to integrate defect detection into process equipment must progress at faster pace to implement automated process control.

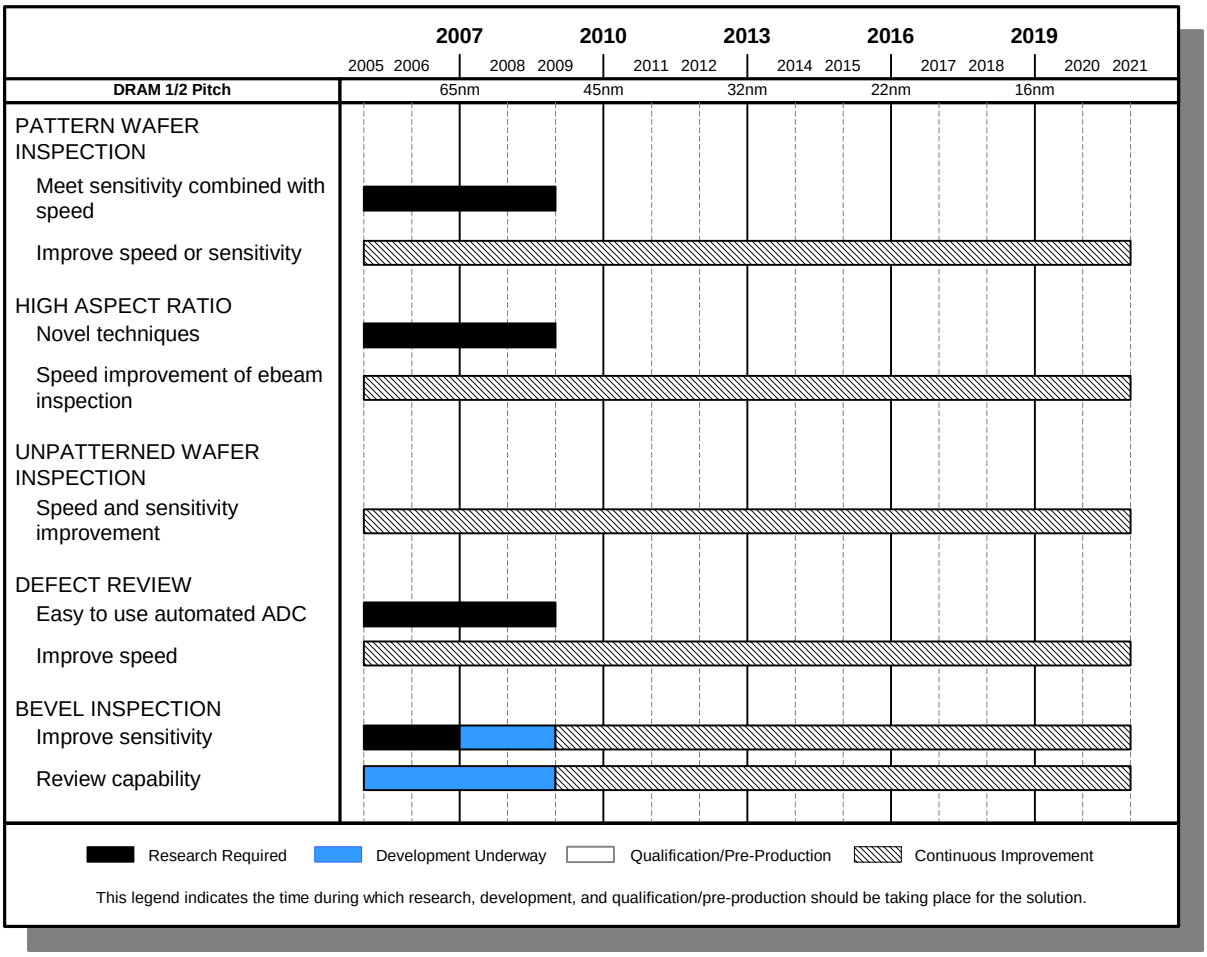

Figure 103 Defect Detection and Characterization Potential Solutions

YIELD LEARNING

As indicated by the yellow and red areas of the Yield Learning Technology Requirements table, the two areas that require highest attention are defect detection capability and capacity and rapid defect/fault sourcing. A collaborative effort between the stakeholders from device makers, metrology and information technology suppliers and academia is required to formulate and execute a strategic plan to manage defect detection capability and capacity relevant to rapid yield learning. Without such collaboration, much redundancy will continue to exist in defect management and analysis. Additional potential solutions are provided in the Yield Management System section below.

As noted above, yield-learning rate can proceed at an acceptable improvement rate in the absence of defect/fault sources. However, given the technology transfer history of our industry, numerous defect/fault sources may be anticipated after the

process technology is handed off to manufacturing by the process R&D group. There are two ways to achieve the required ramping of yield in time: 1) Reduce the total number of new defect/fault sources or mechanisms and 2) Reduce the time to source and fix each new defect/fault source or mechanism. Whereas the first approach is mostly company dependent, the second approach requires numerous tools and techniques for rapid defect/fault sourcing as shown below.

Moreover, with the continued increase in complexity of the design and fabrication process, the ability to detect and react to yield impacting trends and excursions in a timely fashion will require a larger dependence on passive data. This will be acutely true during yield ramp where maximum productivity and profit benefits will be achieved. Passive data is defined as defect, parametric, APC parameters, and electrical test data collected inline from the product through appropriate sampling strategies. The additional time required to perform experiments, such as short-loop testing, will not be readily available in the future. The time necessary to trend potential problems and/or identify process excursions will require the development of sampling techniques that maximize the signal-to-noise ratio inherent in the measured data. The goal of Yield Management System (YMS) is to identify process issues in as few samples as possible. Analysis techniques that place product data in the context of the manufacturing process provide a stronger "signal" and are less likely to be impacted by measurement noise since they comprehend various levels of process history and human experience (lessons learned). Therefore, potential solutions for rapid yield learning include the development of technologies that generate information from product data and tool-health or other in situ process measurements. Automation methods are also required that correlate product information with fabrication processes, sometimes referred to as data mining. Fundamental to the successful integration of new methods and technologies is a requirement for standards that facilitate data communications in the virtual and/or physically merged database environment.

VISIBLE DEFECTS

Although tools for sourcing visible defects are fairly well established (optical and SEM detection and review, SSA, ADC, EDX, focused ion bean (FIB)), new tools and methodologies will have to be developed to achieve adequate signal to noise ratio for differentiating real defects from background nuisance defects and to characterize the elemental composition of continuously shrinking visible defects.

NON-VISUAL DEFECTS

Affordable inspection techniques are needed that go beyond optical microscopy and offer high resolution without sacrificing throughput. To source non-visual defects, the resolution of analytical tools and techniques for electric failure analysis (EFA) and physical failure analysis (PFA) need to be improved. Technology generations below 90 nm will require the development of affordable failure analysis techniques that can extend the range of detectable defects down to the atomic level. In addition, the resolution of internal node DC micro probing for characterizing individual circuit/transistor parameters or isolating leakage paths needs to be improved. Design to process interactions that can lead to localized non-visual structural defects have to be researched and modeled. Design for testability/diagnose-ability techniques need to utilize these models to enhance the localization of a defect source.

Presently, memory array test chips and memory arrays within microprocessors are used to quickly isolate faults. This technique is likely to be extended to non-arrayed devices. Future products must be designed so that the test process can isolate failures. Design for test (DFT) and built in self test (BIST) are two methods that can aid in defect isolation. Both DFT and BIST failure pattern must map to a physical location on a circuit. Accurate fault to defect mapping models must also be developed to further assist in the defect localization process. Other test programs are needed to save failure pattern information so that it can be analyzed based on pre-determined (modeled) failure mode probabilities. All of these techniques will allow yield engineers to more quickly and precisely determine the locations and causes of circuit failures.

Along with new technologies such as optical proximity correction (OPC), and the inclusion of alternating and phase shifting elements in lithographic masks, the potential for non-defect related yield problems are likely to increase. New strategies and technologies for comparing the measured, three-dimensional die structure to the expected printed pattern based on design data will be needed to identify and rapidly correct lithographic patterning and etch problems. Interferometric optical techniques, stereo scanning electron microscopy and high throughput atomic force microscopy will be able to provide three-dimensional topological structure at critical positions across the wafer (analogous to critical dimensional metrology for line width measurements). These measurements coupled with an ability to produce a reference topology based on the expected structure from design data, will provide yield engineers with the ability to track subtle variations in physical topology that impact electrical device function. The ability to rapidly make multiple measurements across the wafer and to render and compare the physical and expected structure will be critical for improving the learning rates for non-visual structural events that impact yield.

PARAMETRIC DEFECTS

Saving more parametric data as measured on circuit testers will aid in sourcing parametric source defects. This information will allow for correlation to process data, through a variety of techniques, including spatial signature analysis. Modeling the probabilities of factors that can lead to "parametric defects" can also reduce the time it takes to source the cause. BIST techniques must be developed to identify race conditions and other failure modes that are a function of parametric variation or mismatch.

YIELD-MANAGEMENT SYSTEMS

The following key areas are necessary for meeting YMS challenges:

- Standards for data/file formats and coordinate systems
- YMS/WIP integration
- YMS methodologies for data collection, storage, archiving and purging
- YMS for advanced tool/process control

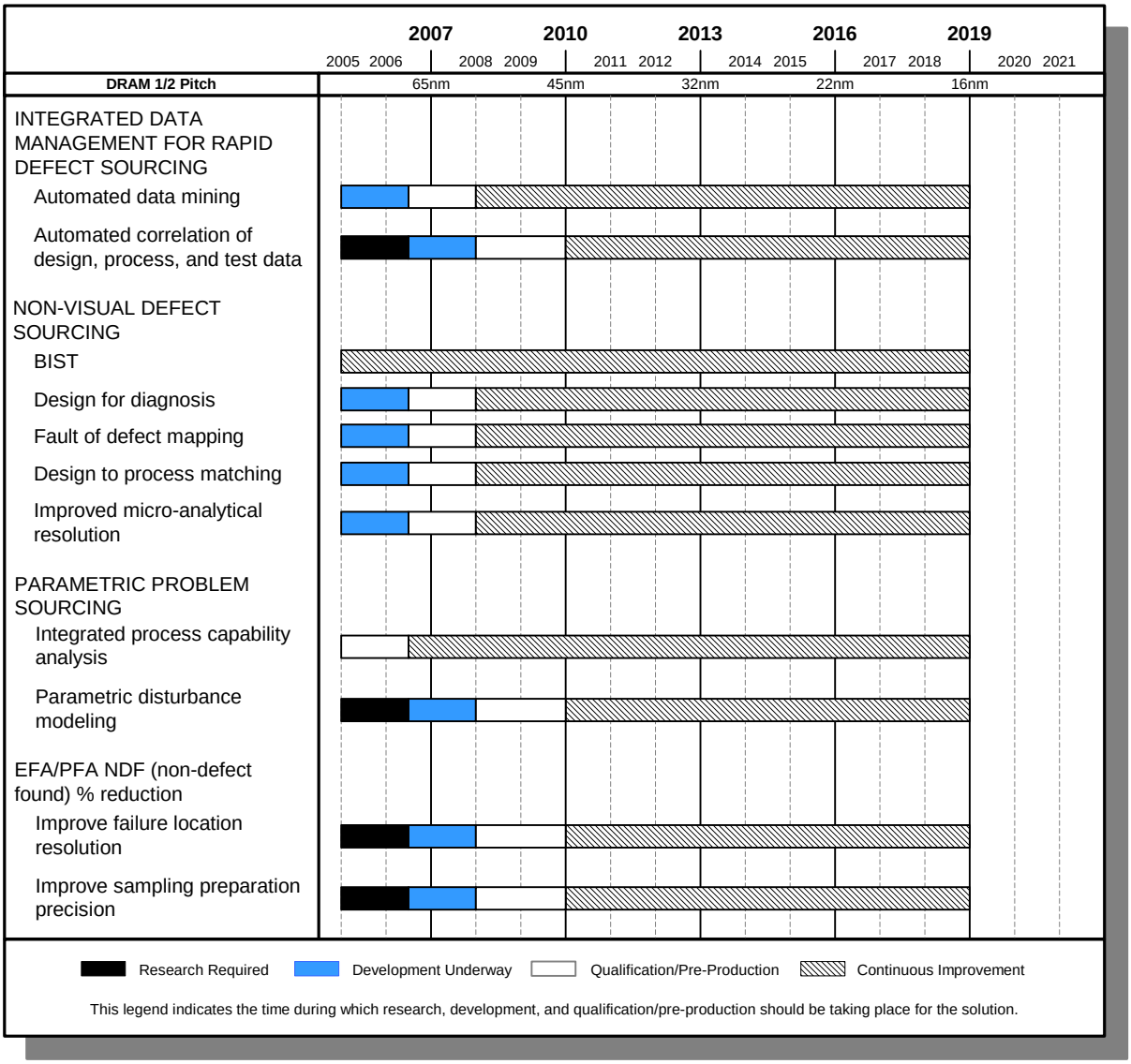

Figure 104 Yield Learning Potential Solutions

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and continue to enable cost-effective high volume manufacturing for device dimensions below 90 nm. Refer to Figure 105. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Process critical materials—Figure 105 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities.

In order to accelerate yield enhancement for processes that incorporate new materials, it is very desirable that development studies include purity data as much as is practical. Studies of new materials (e.g., for gate dielectrics) are initially concerned with basic process performance, and later with integration issues. During those stages of development contamination is a relatively minor concern. However, if no information is collected, later yield enhancement efforts proceed with inadequate technical basis. Collecting and reporting both environmental and material contamination data whenever practical will lead to long-term benefits.

UPW—UPW systems meeting specifications do not appear to be large defect drivers for current device geometries. Based on this the Roadmap does not predict that significant changes are required for future geometries. As a Roadmap priority, specific defect mechanisms related to UPW are required to drive significant changes. The current focus is to understand the impact of the tool upon water quality, specifically particles, bacteria, and dissolved gasses, as well as to identify species that are suspected to be in UPW but are below the detection limit of available measurement methods. Improved measurement methodologies are required for organics, and organic ions to specify low-level contaminants in UPW. Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water.

Chemicals—Figure 105 shows various technological areas that may be required to enhance and measure the purity of delivered chemicals to the wafer manufacturing process.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low outgassing, and non-absorbing materials development are key to effective wafer isolation deployment.

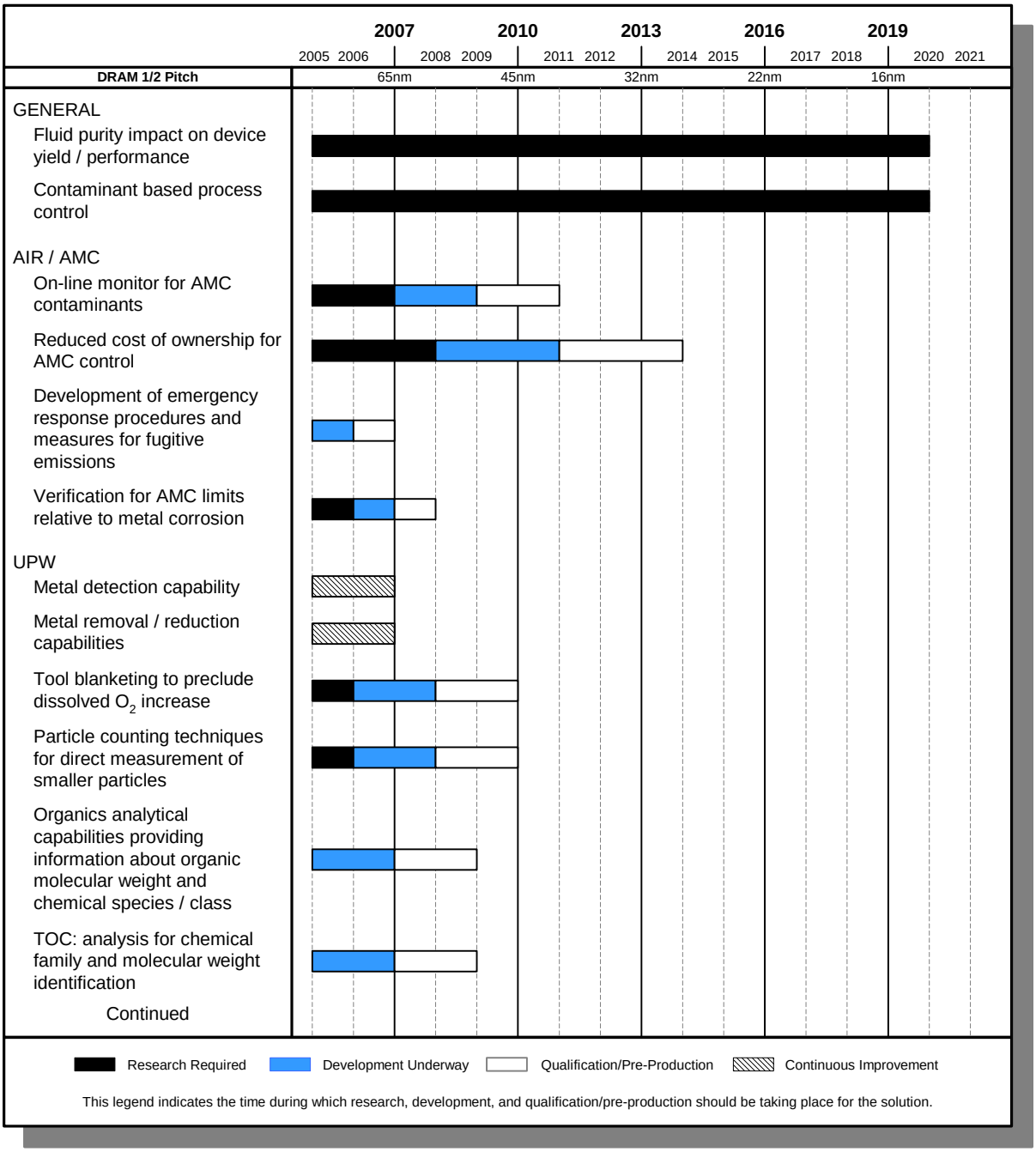

Figure 105 Wafer Environmental and Contamination Control Potential Solutions

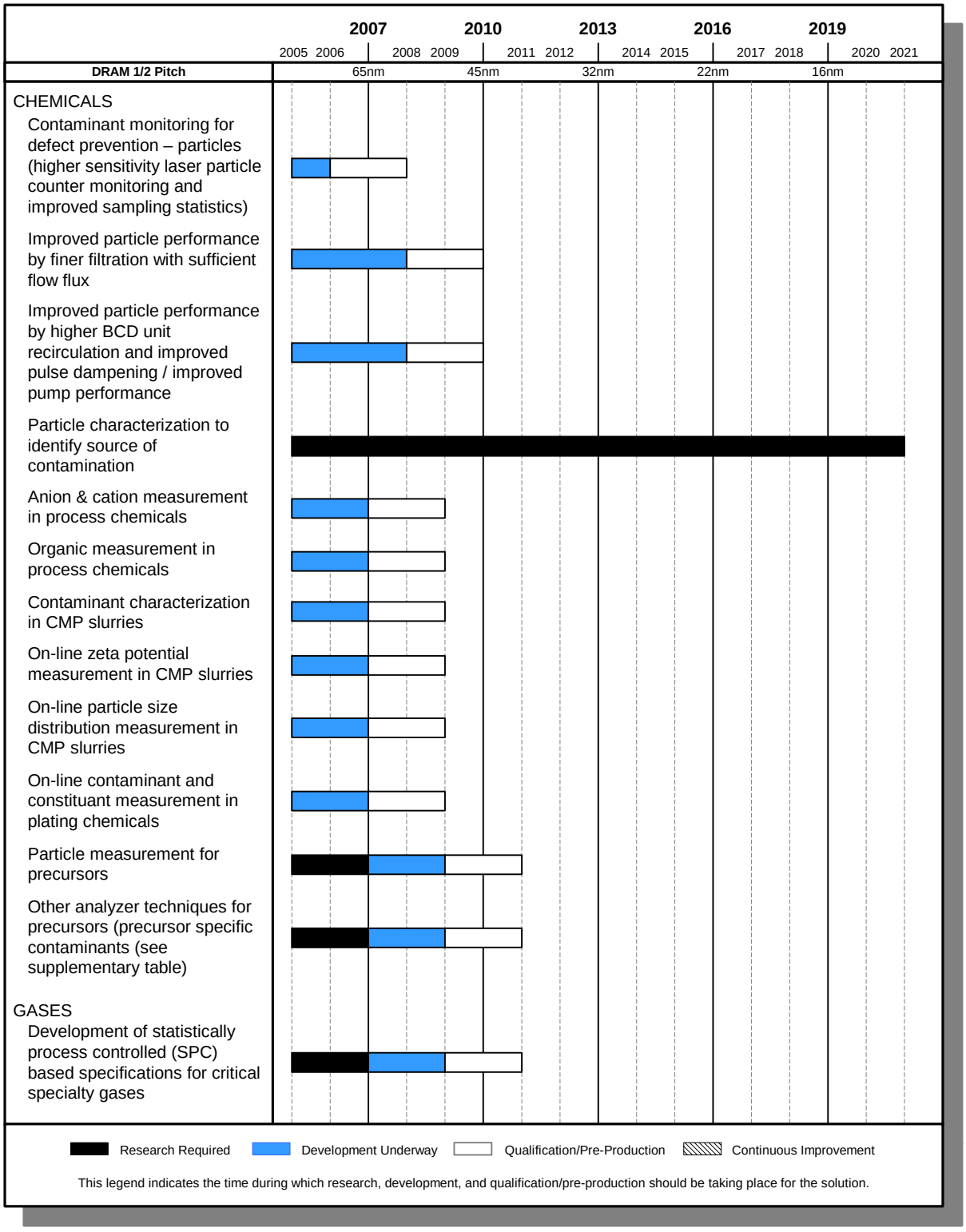

Figure 105 Wafer Environmental and Contamination Control Potential Solutions (continued)