Attachment A
Whitepaper on Semiconductor Die and Packaging

Introduction to SIA and Semiconductors

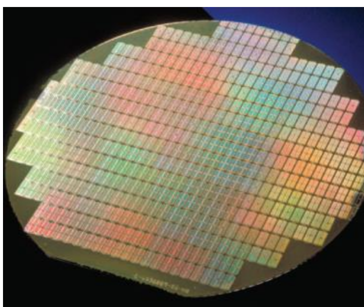
The Semiconductor Industry Association (SIA), represents U.S. leadership in semiconductor manufacturing and design. Brian Toohey, SIA president and CEO recently stated: “The U.S. semiconductor industry supports more than 1 million American jobs, drives economic growth and leads the global market, but our competitors abroad are working hard to attract the world’s top innovators and job-creators”.

In this regard, it is critical that ongoing export control reform efforts result in export control regulations that not only protect U.S. national security interests, but foster the continued growth of the U.S. semiconductor industry by recognizing that U.S. export regulations should not be applied in a manner that provides incentives resulting in the design-out of U.S. semiconductors by customers located around the world. Importantly, any such regulatory incentives to design out U.S. semiconductors would directly benefit our competitors abroad.

Semiconductor devices are the foundation of modern electronics, including computers, telephones, televisions, calculators, digital cameras and players and recorders using video media such as DVDs. Semiconductors contain numerous electrical pathways which are capable of connecting up to a billion transistors and other electronic components. These transistors store information on the semiconductors, either by holding an electrical charge or by holding little or no charge. Semiconductors also control power, battery charging, video displays, and perform other functions.

Wafer and Die

The semiconductor manufacturing process begins with a silicon wafer:



The circuit elements (transistors, resistors, and capacitors) are built in layers on the silicon wafer to produce thousands of electronic devices at tiny sizes, which together function as integrated circuits (ICs). At this stage of the manufacturing process, referred to as “fabrication”, the function of the die is fixed or determined. That is, the die is either “multipurpose” or “application specific.”

For example, the wafers containing die and/or the “bare” die for a multipurpose analog to digital converter (ADC) would be controlled under ECCNs 3A001.a.5, 3A991.c, or EAR99 depending on the performance characteristics of the die on the wafers or the “bare” die. Note 1 to 3A001 states: “The control status of wafers (finished or unfinished), in which the function has

been determined is to be evaluated against the parameters of 3A001.a." In this regard, the function of the ADC wafers and/or "bare" ADC die is converting analog signals to digital signals.

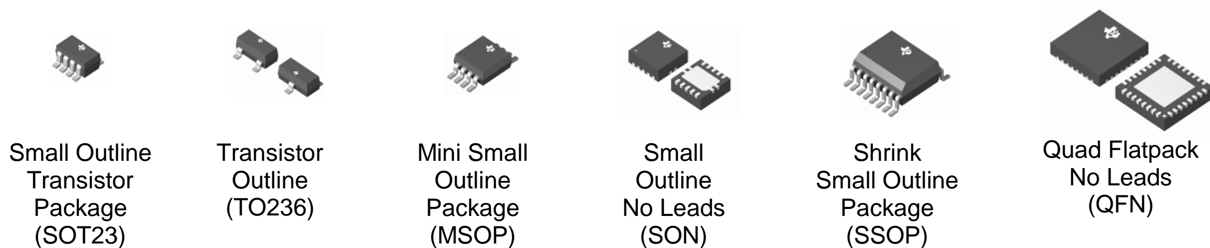
A "special purpose" die would be a die which has been customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely for a customer's networking equipment is an ASIC. Another example of an ASIC is a custom ASIC solution for a customer's digital camera.

After wafer fabrication is complete, a diamond saw cuts the wafer into individual die or chips. Nonfunctional die or chips are discarded, and the rest are generally sent on to be packaged.

In addition to complete semiconductors, a number of companies offer and sell "bare" die, such as "tested die" (TD) and known good die (KGD), to their customers. The availability of bare die provides the customer with more design-in options and enables the customer to utilize more integrated packaging for space-constrained applications. Also, if the manufacturer does not offer a die in a hermetic package, some customers may purchase the bare die and use the services of an "IC packaging foundry", such as Amkor, to encase the bare die in a hermetic package for use in harsh environments. For additional information, see **Exhibit A**.

Packaging

A semiconductor package is a metal, plastic, glass, or ceramic casing containing at least one semiconductor electronic component. The package provides protection against impact, protects against corrosion, holds the contact pins or leads which are used to connect from external circuits to the device, and dissipates heat produced in the device. Packaging can also allow the device to operate at higher temperatures, providing improved performance and reliability. The package can affect the performance characteristics of a semiconductor device, but the package does not change the function of the device. Package examples are shown below:



Small Outline Transistor Package (SOT23) | Transistor Outline (TO236) | Mini Small Outline Package (MSOP) | Small Outline No Leads (SON) | Shrink Small Outline Package (SSOP) | Quad Flatpack No Leads (QFN)

Semiconductor packaging standards may be defined by national or international industry associations such as the Joint Electron Devices Engineering Council (JEDEC), Pro Electron, or the Electronic Industries Association of Japan (EIAJ), or may be proprietary to a single manufacturer. A standard package can be used to encase any number of die having different functionalities, and is not specific to any particular part. Standard packages are widely available from a number of sources that are not engaged in the design and/or manufacture of semiconductors. Popular IC package types used in the semiconductor industry today are illustrated in **Exhibit B.**

Thousands of standard package types are offered in the commercial marketplace, with some made to industry-wide standards and others particular to an individual manufacturer. Standard packages are available in high volumes as "off-the-shelf" products and have been

commoditized. Some companies refer to standard packaging as "open tool"[1]. These packages may be used by multiple companies for several chip designs as long as they meet size and connectivity requirements.

Plastic, ceramic or metal packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Once packaged, chips are tested again to make sure they function properly and were not damaged during packaging and that the die-to-pin interconnect operation was performed correctly. Then a laser etches the chip's name and numbers on the package.

Packaging and Performance

Certain types of packages can affect the performance characteristics of a semiconductor. However, it is important to note that the package does not change the function of the die or of the completed semiconductor. The function of a semiconductor whether it is packaged in plastic, ceramic, or other forms of packaging, and irrespective of end-use is the same. Hermetic, ceramic packages have the same function irrespective of end-use and irrespective of the type of die encased therein. The same can be said regarding hermetic metal packages. See page 6 of **Exhibit C**: NSC's "Semiconductor Packaging Assembly Technology" from 1999, prior to the time NSC was acquired by TI, which notes:

> *National Semiconductor offers a wide variety of ceramic and metal can packages for through-hole and surface mount applications. These ceramic and metal can packages are offered as solutions for high reliability, high performance applications and are extensively used in military/aerospace and commercial applications. By design, a hermetic seal prevents gases and liquids from entering the package cavity where the die is mounted. Because of the package materials, hermetic packages are able to withstand higher temperatures than equivalent plastic packages.*

For example, a die encased in plastic packaging may not have the same operating temperature range as a die encased in ceramic packaging. It should also be noted, however, that when a die is encased in a ceramic package, the electrical or speed performance of the device may be degraded. In certain cases, die encased in plastic package may even have better electrical and/or speed than a die encased in a ceramic package. However, the performance capability of a standard ceramic package is the same no matter what die is encased in the standard package. The same is true for plastic packaging; the performance of the package is the same no matter what die is encased in that package. The same is true for any die used in a metal package. See **Exhibit D** for information on electronics that can operate reliably in harsh environments, including extremely high temperatures

[1] Kyocera refers to standard packages as "open tool": "Standard (open tool) products are also available for device evaluation and low volume orders" at http://global.kyocera.com/prdct/semicon/index.html NTK also refers to "open tool" for standard packages: "Beside customer tailored and "Open Tool" layouts, we also offer a product family of short time available packages" at http://www.ngk.de/en/products-technologies/technical-ceramics/ceramic-ic-packages-and-multilayer-substrates/ Spectrum Semiconductor Materials, Inc., is a distributor of packaging materials and bills itself as "the leading distributor of off-the-shelf ceramic packages". http://www.spectrum-semi.com/about/index.html

Packaging History

Most semiconductor devices are enclosed in a package to prevent damage to the chip and its fragile connecting wires. Three package types are commonly used, ceramic and metal for hermetically sealed requirements and plastic for general commercial use. Increasingly, however, plastic packages have been used in space and military end applications. Hermetically sealed parts are ones where the IC chip is enclosed in a sealed compartment to protect the chip from harsh environmental elements, such as chemicals, gases, and steam. Hermetic packages are often used in certain end applications where parts that fail due to moisture or other environmental elements are very difficult or impossible to replace.

Many IC devices are molded out of an epoxy plastic that provides adequate protection of the semiconductor device, and mechanical strength to support the leads and handling of the package. Some devices, intended for high-reliability or aerospace or radiation environments, use ceramic packages. All-metal packages are often used with high power (several watts or more) devices, since they conduct heat well and allow for easy assembly to a heat sink.

Hermetic Packages

In addition to providing connections to the semiconductor and handling waste heat, the semiconductor package must protect the "chip" from the environment, particularly the ingress of moisture. Stray particles or corrosion products inside the package may degrade performance of the device or cause failure. A hermetic package allows essentially no gas exchange with the surroundings; such construction requires glass, ceramic or metal enclosures.

Standard hermetic packages comprise a subset of standard packages and can be made of ceramic or metal (metal “cans”). These standard ceramic and metal can packages are offered as solutions for high reliability, high performance applications, including certain commercial, industrial, aerospace and military end applications. The function of the hermetic seal is to prevent gases and liquids from entering the package cavity where the die is mounted, and to help prevent damage from corrosion and moisture. Because of the package materials used in these hermetic packages, these packages are generally able to withstand higher temperatures than equivalent plastic packages.

Dual-in-Line (DIP) Packages

A common package used by the semiconductor industry is the dual in-line package (DIP or DIL), which is a device package with a rectangular housing and two parallel rows of electrical connecting pins. The package may be through-hole mounted to a printed circuit board or inserted in a socket.

For many years, beginning in the 1960s, the dual-in-line (DIP) package was the dominant IC package type, both in ceramic and plastic. The development of DIP was undertaken primarily for certain end applications, such as avionics and satellites. The DIP package, both plastic and ceramic, has been the mainstay of integrated circuit packaging for many years. The opening of the consumer electronics market required more power in a smaller package. The requirement to make better use of board space was solved through the use of surface mount packaging.

Dual-in-line packages were developed in the 1960s when the restricted number of leads available on transistor-style packages became a limitation in the use of integrated circuits. Increasingly complex circuits required more signal and power supply leads; eventually

microprocessors and similar complex devices required more leads than could be put on a DIP package, leading to development of higher-density packages.

A DIP is usually referred to as a DIP*n*, where *n* is the total number of pins. For example, a microcircuit package with two rows of seven vertical leads would be a DIP14. Common packages have as few as four and as many as 64 leads. Many analog and digital integrated circuit types are available in DIP packages, as are arrays of transistors, switches, light emitting diodes, and resistors.

The semiconductor industry uses both ceramic dual-in-line packages (CerDIP) and plastic in-line-packages (PDIP) DIP packages are usually made from an opaque molded epoxy plastic pressed around a tin-, silver-, or gold-plated lead frame that supports the device die and provides connection pins. Some types of IC are available in ceramic DIP packages, where high temperature or high reliability is required.

Variations of the DIP package include those with only a single row of pins, possibly including a heat sink tab in place of the second row of pins, and types with four rows of pins, two rows, staggered, on each side of the package. DIP packages have been mostly displaced by surface-mount package types, which avoid the expense of drilling holes in a printed circuit board and which allow higher density of interconnections.

Flat Pack Packages

A common package is the flat pack package. The original flat pack was invented by Y. Tao in 1962 while working for Texas Instruments to achieve improved heat dissipation. The dual in-line package discussed above was invented two years later. The first devices measured 1/4 inch by 1/8 inch (3.2mm x 6.4mm) and had 10 leads.

The flat package was smaller and lighter than the round TO-5 style transistor packages previously used for integrated circuits. Round packages were limited to 10 leads. Integrated circuits needed more leads to take full advantage of increasing device density. Since flat packages were made of glass, ceramic and metal, they could provide hermetic packaging for circuits, protecting them from moisture and corrosion. Flat packs remained popular for military and aerospace applications long after plastic packages became the prevalent package used for other applications.

A QFP or Quad Flat Package is a surface mount integrated circuit package with "gull wing" leads extending from each of the four sides. Socketing such packages is rare and through-hole mounting is not possible. Versions ranging from 32 to 304 pins with a pitch ranging from 0.4 to 1.0 mm are common.

The QFP component package type became common in Europe and United States during the early nineties, even though it has been used in Japanese consumer electronics since the seventies. The semiconductor industry uses both ceramic quad flat packs (CQFP) and plastic quad flat pack packages (PQFP). See Exhibit E - Kyocera Ceramic Quad Flat Packages. Kyocera not only offers CQFP packages, but the company also “offers a wide variety of [other] standard packages”. See **Exhibit F –** Packages and Lids for Evaluation (Standard Product Lists).

A package related to QFP is the leadless chip carrier (LCC) which is similar to the QFP but has pins with larger pitch, 1.27 mm (or 1/20 inch), curved up underneath a thicker body to

simplify socketing (soldering is also possible). LCC packages are commonly used for NOR Flash memories and other programmable components. The semiconductor industry uses both ceramic leadless chip carriers (CLCC) and plastic leadless chip carriers (PLCC).

Metal Packages

As is the case with plastic and ceramic packages, there are also a number of different standard metal packages. TO-3 is a designation for a standardized metal semiconductor package used for transistors and some integrated circuits. The “TO” element stands for "transistor outline" and refers to a series of technical drawings produced by JEDEC.

The TO-3 metal can package is commonly used for power transistors, silicon-controlled rectifiers, and, occasionally, integrated circuits. The semiconductor die component is mounted on a metal plate with a metal can crimped on top of it, providing good heat conduction and durability. TO-3 packages usually have two leads, the case being the third connection, though devices with four leads exist and more leads are possible. The leads pass through the metal base plate and are sealed with glass. The metal case is connected to the internal device. The TO-3 case has two mounting holes. The design originated at Motorola in approximately 1955.

The metal package can be attached to a heat sink, making it suitable for devices dissipating several watts of heat. Thermal compound is used to improve heat transfer between the device case and the heat sink. Since the device case is one of the electrical connections, an insulator may be required to electrically isolate the component from the heatsink. Insulating washers may be made of mica or other materials with good thermal conductivity.

Advantages of metal packages include the fact that they can be used in high-power and high-current applications where equivalent components of other cases may be susceptible to damage. In addition, almost all surfaces are metal for better heat conduction and durability. The metal-glass seal is hermetic to protect the semiconductor from liquids and gases. However, there are also certain disadvantages, such as being more costly than plastic encapsulated components with similar ratings and the component size and lead placement makes soldering to a circuit board difficult.

Common components that use the TO-3 package include common voltage regulators such as the LM317, voltage regulator and the LM340, voltage regulator.

TO-5 is a designation for a standardized metal semiconductor package used for transistors and some integrated circuits. The typical TO-5 package has a base diameter of 8.9mm, a cap diameter of 8.1mm, and a cap height of 6.3mm. Different manufacturers have different tolerances, and the actual form factor may vary slightly, depending on function. The tab on the metal can usually marks the last pin-number, for example 8 on a typical operational amplifier and the pin numbers count upwards counter clock-wise

TO-18 is a designation for a style of transistor metal case. The case is therefore more expensive than the similarly sized plastic TO-92 package. The name is from JEDEC, signifying *Transistor Outline Package, Case Style 18*. The 3-lead TO-18 is used for transistors and other devices using no more than three leads. Variants for diodes, photodiodes and LEDs have only two leads. Light-sensitive or light-emitting devices have a transparent window, lens, or parabolic reflectors in the top of the case rather than a sealed, flat top. For example, diode lasers such as those found in CD players may be packaged in TO-18 cases with a lens.

Application Specific Integrated Circuits (ASICs)

An application-specific integrated circuit (ASIC) is a kind of integrated circuit that is specially built for a specific application or purpose. Compared to a programmable logic device or a standard logic integrated circuit, an ASIC can improve speed because it is specifically designed to do one thing and it does this one thing well. It can also be made smaller and use less electricity. The disadvantage of this circuit is that it can be more expensive to design and manufacture, particularly if only a few units are needed.

In the mid-1980s, a designer would choose an ASIC manufacturer and implement their design using the design tools available from the manufacturer. While third-party design tools were available, there was not an effective link from the third-party design tools to the layout and actual semiconductor process performance characteristics of the various ASIC manufacturers. Most designers ended up using factory-specific tools to complete the implementation of their designs. A solution to this problem, which also yielded a much higher density device, was the implementation of standard cells. Every ASIC manufacturer could create functional blocks with known electrical characteristics, such as propagation delay, capacitance and inductance, that could also be represented in third-party tools. Standard-cell design is the utilization of these functional blocks to achieve very high gate density and good electrical performance.

Standard-cell design uses the manufacturer's cell libraries that have been used in potentially hundreds of other design implementations and therefore are of much lower risk than full custom design. Standard cells produce a design density that is cost effective, and they can also integrate IP cores and SRAM (Static Random Access Memory) effectively, unlike Gate Arrays.

An ASIC can be found in almost any electronic device and its uses can range from custom rendering of images to sound conversion. Because ASICs are all custom-made and thus only available to the company that designed them, they are considered to be proprietary technology.

Index of Exhibits:

Exhibit A – TI Bare Die Solutions; ADI Semi Dice, wafer & Die Products
Exhibit B - Package Diversity
Exhibit C – NSC's "Semiconductor Packaging Assembly Technology"
Exhibit D - High-Temperature Electronics Pose Design and Reliability Challenges).
Exhibit E - Kyocera Ceramic Quad Flat Packages
Exhibit F - Kyocera Packages And Lids for Evaluation (Standard Product Lists)