INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2001 EDITION

INTERCONNECT

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INTERCONNECT

SCOPE

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap highlights a continued change to new materials, now being introduced at an unprecedented pace. In 2001, these materials introductions continue, but a solution must be found for the problem associated with increases in conductor resistivity (for more detail, a link is provided to the supplemental material regarding *conductor resistivity*). Further, although the technical product driver for the smallest feature size remains the dynamic memory chip, an emerging classification of chips, system-on-a-chip, or SoC, will challenge microprocessors for increased complexity and decreased design rules. Managing this rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes. The Interconnect Technology Requirements tables have been updated to reflect the new 2001 node accelerations for both MPU and DRAM.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant predicted by the ITRS is now firmly on track. Fluorine doped silicon dioxide ($\kappa = 3.7$) was introduced at the 180 nm technology node and there will undoubtedly be insulating materials with $\kappa = 2.6–3.0$ introduced at the 130 nm node. Since the development and integration of these new low κ materials is rather time invariant, κ values will translate to lower technology nodes with the roadmap acceleration. The κ values of the bulk dielectric materials are defined in the dielectric potential solutions figure and the range of effective κ values for the integrated dielectric stack is listed in the technology requirements tables. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge. (For a more thorough explanation, access the link to the *calculation of the effective κ for various integration schemes*.)

The conductor, barrier, and nucleation potential solutions have been grouped into sections for local, intermediate and global wiring levels, as well as passive devices. Atomic layer deposition (ALD), characterized by excellent conformality and thickness control, is receiving attention for applications in the deposition of barriers, nucleation layers and high κ dielectric materials. Other additions to conductor potential solutions include novel process tools that combine Cu electrochemical deposition (ECD) and planarization. This is particularly relevant for thick metal films used for either global wiring or inductors. Doped Cu has also emerged as a potential solution for improved Cu reliability, but this needs to be balanced against the increased Cu resistivity that occurs. Increases in Cu resistivity due to electron scattering effects will become an important factor in the long term, and is also an area of focus. Links to *expanded references to ALD* are included as supplemental material.

Figure 43 covers etch, strip, and cleans potential solutions, acknowledging the increased integration challenges of these steps. For example, the etch solution for a dual-Damascene structure with and without an embedded trench etch stop are different. Requirements for pre-etch and post-etch clean, which might utilize novel approaches such as super critical CO_2, have been expanded. Plasma (HDP) etch has been de-emphasized in this Roadmap.

Planarization potential solutions contain a more detailed discussion of chemically enhanced planarization (CEP). One of the primary integration challenges with low κ materials is adhesion failure of barrier or capping materials with the dielectric during planarization. Porous low κ materials are even more problematic and are therefore one of the key focus areas for planarization development efforts. A more detailed *schematic on the dishing/erosion/thinning metrics* shown in the technology requirements tables is found in the supplemental material link.

DIFFICULT CHALLENGES

Table 61 highlights and differentiates the five key challenges in the near term (≥ 65 nm) and long term (< 65 nm). In the near term, the most difficult challenges for interconnect include the rapid introduction and integration of new materials and processes, dimensional control, physical/electrical reliability of interconnect structures, and interconnect processes with low or no device impact. The introduction of new low κ dielectrics, chemical vapor deposition (CVD) metal/barrier/seed layers, and additional elements for SoC, provide significant process and process integration challenges. Interfaces, contamination, adhesion, mechanical stability, electrical parametrics, and thermal budget, confounded by the number of wiring levels for interconnect, ground planes and passive elements, create a difficult-to-manage complexity.

Table 61 Interconnect Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥65 nm / THROUGH 2007	*SUMMARY OF ISSUES*
Introduction of new materials*	The rapid introduction of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Integration of new processes and structures*	Combinations of materials and processes used to fabricate new structures create integration complexity.
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Attaining dimensional control	Three-dimensional control (3D CD), with its associated metrology, of interconnect features is necessary for circuit performance and reliability. The multiplicity of levels combined with new materials, reduced feature size and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
FIVE DIFFICULT CHALLENGES <65 nm / BEYOND 2007	*SUMMARY OF ISSUES*
Dimensional control and metrology	Multi-dimensional control and metrology of interconnect features is necessary for circuit performance and reliability.
Patterning, cleaning, and filling high aspect ratios features	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low κ dual-Damascene metal structures and DRAM.
Integration of new processes and structures	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Continued introductions of new materials and size effects	Further introductions of materials/processes are expected. Microstructure and dimensional effects become important when Cu/low κ interconnect is extended to smaller features.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*

Dimensional control is a key challenge for present and future interconnect technology generations. The dominant architecture, Damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for inline monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional

control, a challenge now, will become even more critical as new materials, such as porous low κ dielectrics and CVD metals, play a role at the tighter pitches and higher A/R (aspect ratio) of intermediate and global levels. At the 45 nm node, feature size effects, such as electron surface scattering, will increase the effective resistivity and new conductor technologies may be required. Cu and low κ will continue to find applications in future chip generations, but for global wiring, new interconnect solutions incorporating RF or optical propagation will be required, bringing even more material and process integration challenges.

Feature size reduction, new materials, and Damascene structures all challenge metrology for on-chip interconnect development and manufacture. Critical dimension measurements are needed for very high aspect ratio features and ultra-thin barriers. Methods must be developed to accommodate the increased complexity of the wiring levels of future chips. Other metrology challenges include measuring resistivity and dielectric constant at high frequency, adhesion and mechanical properties.

TECHNOLOGY REQUIREMENTS

To adequately describe the wiring needs of interconnect, near term (2001–2007) and long term (2010–2016) technology requirements and potential solutions are addressed for two specific classes of products: high performance microprocessors (HP MPU) and dynamic memory (DRAM [Tables 62–63]. For MPUs, local, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a hierarchical scaling methodology that has been broadly adopted. Implementation of copper and low κ materials allows scaling of the intermediate wiring levels and minimizes the impact on wiring delay. Local wiring levels are relatively unaffected by traditional scaling. RC delay, however, is dominated by global interconnect and the benefit of materials changes alone is insufficient to meet overall performance requirements. Figure 35 shows the delay of local and global wiring in future generations. Repeaters can be incorporated to mitigate the delay in global wiring but consume power and chip area.

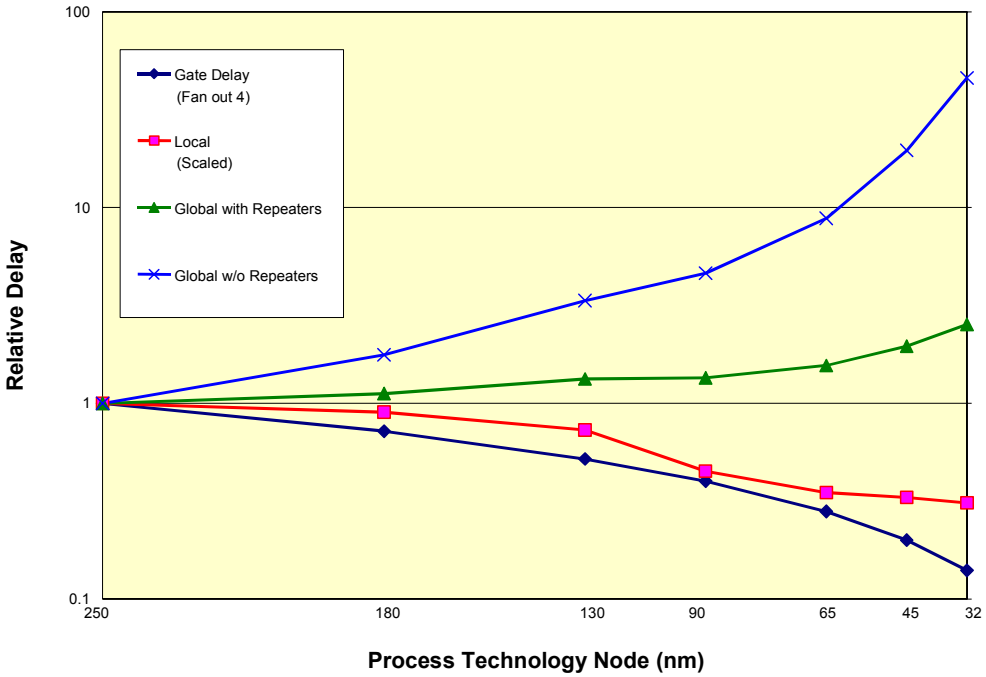


Figure 35 Delay for Local and Global Wiring versus Feature Size

In the long term, new design or technology solutions (such as co-planar waveguides, free space RF, optical interconnect) will be needed to overcome the performance limitations of traditional interconnect. Inductive effects will also become increasingly important as frequency of operation increases, and additional metal patterns or ground planes may be required for inductive shielding. As supply voltage is scaled or reduced, crosstalk has become an issue for all clock and signal wiring levels; the near term solution adopted by the industry is the use of thinner metallization to lower line-to-line

capacitance. This approach is more effective for the lower resistivity copper metallization, where reduced aspect ratios (A/R) can be achieved with less sacrifice in resistance as compared with aluminum metallization. The 2001 Roadmap continues to reflect the design trend featuring reduced aspect ratios (as an alternative means of reducing capacitance) and less aggressive scaling of dielectric. The latter change expands the development window to address the difficulty in integrating low κ dielectrics into a Damascene architecture.

MPUs utilize a high number of metal layers; designers are adopting a hierarchical wiring approach with steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. Refer to Figure 36.

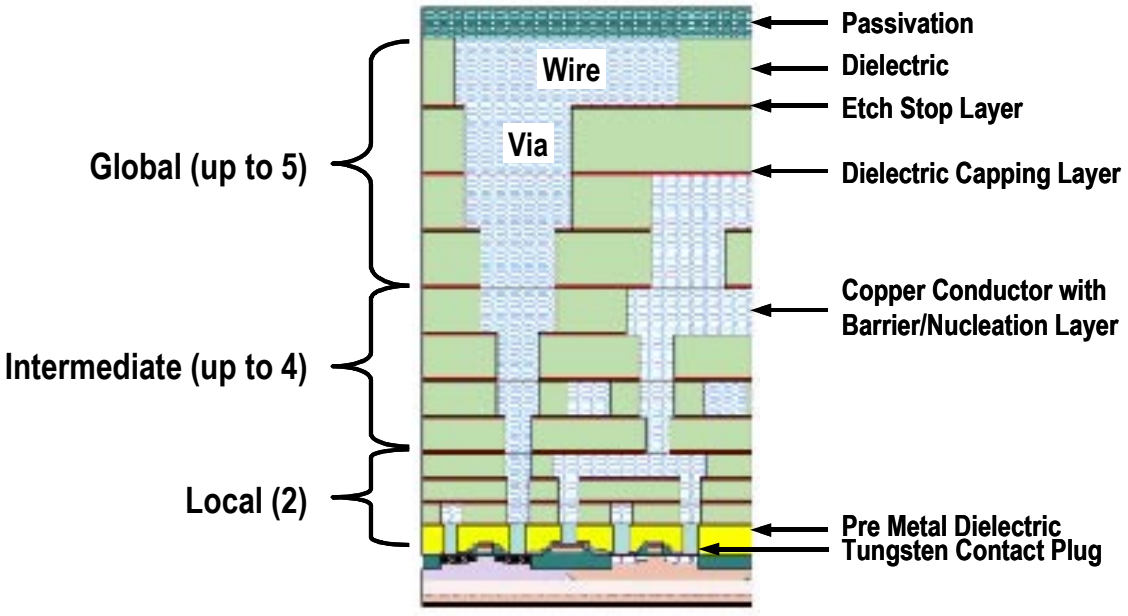


Figure 36 Cross-section of Hierarchical Scaling

To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified solely to meet performance requirements. Copper wire aspect ratios are lower than those for Al, which provides for a reduction in line-to-line capacitance and crosstalk but leads to higher wire resistance. Aspect ratios of features at the global levels will be comparable for both copper and aluminum conductor solutions, to minimize delay. Refer to Table 62a and b. More information regarding *optional levels* is provided through a link to supplemental files.

Table 62a MPU Interconnect Technology Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU/ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Number of metal levels	8	8	8	9	10	10	10
Number of optional levels—ground planes/capacitors	**2**	**2**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2)—active wiring only, excluding global levels [1]	**4086**	**4843**	**5788**	**6879**	**9068**	**10022**	**11169**
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	**1.22**	**1.03**	**0.86**	**0.73**	**0.55**	**0.50**	**0.45**
Jmax (A/cm^2)—wire (at 105°C)	**9.6E5**	**1.1E6**	**1.3E6**	**1.5E6**	**1.7E6**	**1.9E6**	**2.1E6**
Imax (mA)—via (at 105°C)	**0.32**	**0.29**	**0.27**	**0.24**	**0.22**	**0.20**	**0.18**
Local wiring pitch (nm)	**350**	**295**	**245**	**210**	**185**	**170**	**150**
Local wiring A/R (for Cu)	**1.6**	**1.6**	**1.6**	**1.7**	**1.7**	**1.7**	**1.7**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**28**	**24**	**20**	**18**	**16**	**14**	**13**
Intermediate wiring pitch (nm)	**450**	**380**	**320**	**265**	**240**	**215**	**195**
Intermediate wiring dual Damascene A/R (Cu wire/via)	**1.6/1.4**	**1.6/1.4**	**1.7/1.5**	**1.7/1.5**	**1.7/1.5**	**1.7/1.6**	**1.8/1.6**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**36**	**30**	**27**	**23**	**20**	**18**	**18**
Minimum global wiring pitch (nm)	**670**	**565**	**475**	**460**	**360**	**320**	**290**
Global wiring dual Damascene A/R (Cu wire/via)	**2.0/1.8**	**2.0/1.8**	**2.1/1.9**	**2.1/1.9**	**2.2/2.0**	**2.2/2.0**	**2.2/2.0**
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 µm wide wire	**67**	**57**	**50**	**48**	**40**	**35**	**32**
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**40**	**34**	**30**	**29**	**24**	**21**	**19**
Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**16**	**14**	**12**	**10**	**9**	**8**	**7**
Interlevel metal insulator —effective dielectric constant (κ)	**3.0-3.6**	**3.0–3.6**	**3.0–3.6**	**2.6–3.1**	**2.6–3.1**	**2.6–3.1**	**2.3–2.7**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	**<2.7**	**<2.7**	**<2.7**	**<2.4**	**<2.4**	**<2.4**	**<2.1**

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow–Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

Notes for Table 62a and b

[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semiglobal wiring levels are populated. The wiring lengths for each level are then summed to calculate the total inteconnect length per square centimeter of active area.

[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.

[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity

Table 62b MPU Interconnect Technology Requirements—Long-term

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*45*	*32*	*22*
MPU/ASIC ½ PITCH (nm)	*45*	*32*	*22*
MPU PRINTED GATE LENGTH (nm)	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*18*	*13*	*9.0*
Number of metal levels	**10**	**11**	**11**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**
Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	**16063**	**22695**	**33508**
FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	**0.31**	**0.22**	**0.15**
Jmax (A/cm^2)—wire (at 105°C)	**2.7E6**	**3.3E6**	**3.9E6**
Imax (mA)—via (at 105°C)	**0.10**	**0.07**	**0.04**
Local wiring pitch (nm)	**105**	**75**	**50**
Local A/R (for Cu)	**1.8**	**1.9**	**2.0**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**5**	**4**	**3**
Intermediate wiring pitch (nm)	**135**	**95**	**65**
Intermediate wiring dual Damascene A/R (Cu wire/via)	**1.8/1.6**	**1.9/1.7**	**2.0/1.8**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**12**	**9**	**7**
Minimum global wiring pitch (nm)	**205**	**140**	**100**
Global wiring dual-Damascene A/R (Cu wire/via)	**2.3/2.1**	**2.4/2.2**	**2.5/2.3**
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 µm wide wire	**24**	**17**	**13**
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**14**	**10**	**8**
Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**5**	**3.5**	**2.5**
Interlevel metal insulator—effective dielectric constant (κ)	**2.1**	**1.9**	**1.8**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	**<1.9**	**<1.7**	**<1.6**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

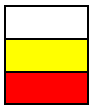


Table 63a DRAM Interconnect Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Number of metal levels	3	3–4	4	4	4	4	4
Contact A/R—stacked capacitor	11.4	11.9	12.4	13.0	13.6	14.3	15.2
Local wiring pitch (nm) non-contacted	260	230	200	180	160	150	130
Specific contact resistance (Ω-cm^2)	1.5E-7	1.3E-7	1.0E-7	8.0E-8	7.0E-8	6.0E-8	5.0E-8
Specific via resistance (Ω-cm^2)	2E-9	1.4E-9	1.0E-9	9.0E-10	7.0E-10	6.0E-10	5.0E-10
Conductor effective resistivity ($\mu\Omega$-cm)	3.3	3.3	3.3	2.2	2.2	2.2	2.2
Interlevel metal insulator—effective dielectric constant (κ)	4.1	3.0–4.1	3.0–4.1	3.0–4.1	3.0-4.1	2.6–3.1	2.6–3.1

Table 63b DRAM Interconnect Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (nm)	45	32	22
MPU/ASIC ½ PITCH (nm)	45	32	22
MPU PRINTED GATE LENGTH (nm)	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	18	13	9.0
Number of metal levels	4	4	4
Contact A/R—stacked capacitor	16.1	19.3	23.2
Local wiring pitch (nm) non-contacted	90	64	44
Specific contact resistance (Ω-cm^2)	4.0E-8	2.0E-8	1.0E-8
Specific via resistance (Ω-cm^2)	5E-10	3E-10	1.0E-10
Conductor effective resistivity ($\mu\Omega$-cm)	2.2	2.2	2.2
Interlevel metal insulator—effective dielectric constant (κ)	2.3–2.7	2.3–2.7	2.1

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

DRAM interconnect technology reflects the most aggressive metal pitch and highest aspect ratio contacts and will continue to provide the most significant challenges in dimensional control and defect management (refer to Table 63). The introduction of low κ dielectric materials at the 115 nm ½ pitch and copper at the 90 nm ½ pitch is required to meet the performance of high speed memory products. However, the pricing sensitivity of the marketplace may delay introduction if cost savings associated with copper are not realized. This suggests that capability for aluminum processing must be continuously improved and extended.

Damascene processing flows dominate MPU/ASIC fabrication methodologies and usage in DRAM is expected to broaden. Figure 37 illustrates several typical interlevel dielectric (ILD) architectures available to create the interconnect wiring levels. While current copper Damascene processes utilize physical vapor deposited (PVD) Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited Cu (ECD) to the 22 nm generation but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of Damascene

features. Surface segregated, CVD, ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required.

Near-term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for decoupling and metal insulator metal (MIM) capacitors and materials with high remanent polarization for ferroelectric memories. The thermal, mechanical, and electrical properties of these new materials present a formidable challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials will be required that have sufficient optical contrast to serve as low-loss waveguides.

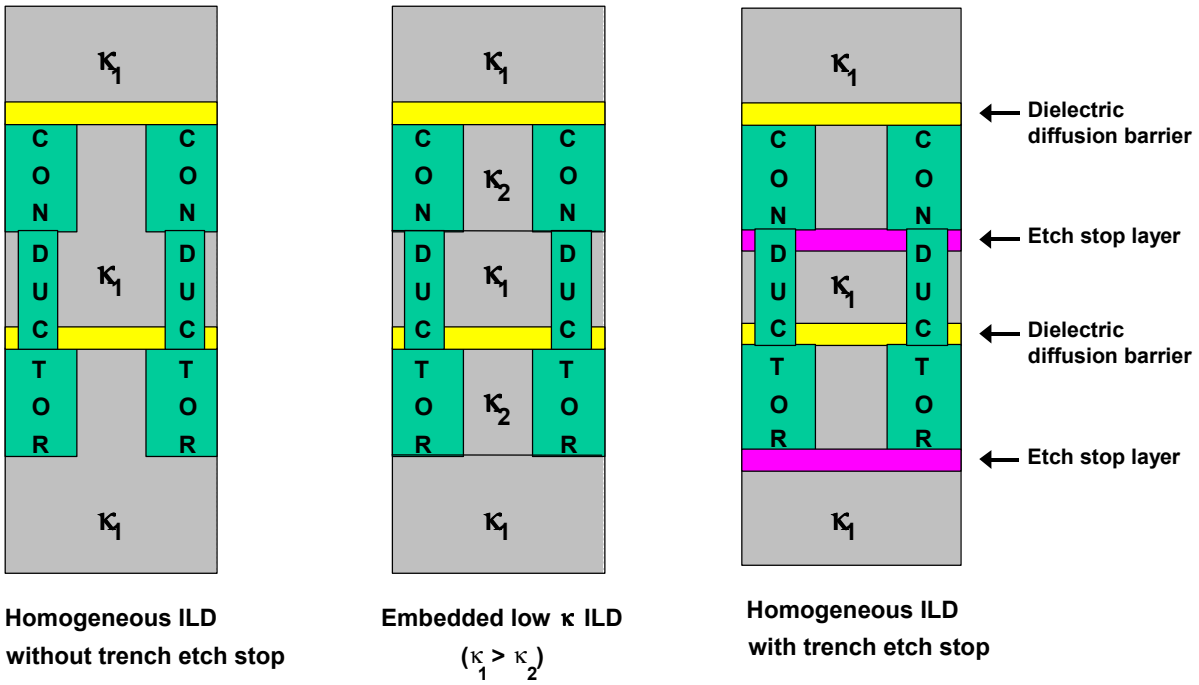


Figure 37 Typical ILD Architectures

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long-term solution. For copper CMP, minimization of erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Planarization processes (with associated end-point) that are compatible with low κ dielectrics that may have low density and poor mechanical strength must be developed. Improvements in post-CMP clean will be critical in achieving the low defect densities required for future devices. Etch, resist strip, and post-etch cleans must be developed that maintain the desired selectivity to etch stop layers and diffusion barriers, but which do not degrade low κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

POTENTIAL SOLUTIONS

DIELECTRIC POTENTIAL SOLUTIONS

The *1999 ITRS* indicated the need for a substantial change in the dielectric materials used in ICs and the 2001 Roadmap will substantiate the occurrence of this change. All ranges of material permittivity (from $\kappa > 100$ to $\kappa < 2$) are under discussion and development with materials having $\kappa > 20$ and $\kappa < 3$ being commercially implemented in 2001. The κ values in this document are bulk film permittivity values unless otherwise indicated. Effective values, κ_{eff}, are defined later. The following three overall dielectric challenges remain valid throughout the 15-year scope of this roadmap:

- Development and integration of high κ materials and processes to achieve the maximum permittivity for stand-alone memory applications, decoupling and (MIM) capacitors for MPU/ASICs and system-on-a-chip (SoC)
- Development and integration of low κ materials and processes to achieve the minimum possible permittivity (κ_{eff}) primarily for Cu dual-Damascene technology
- Development and integration of new materials for emerging technologies to replace conventional wiring with alternatives, such as RF and optical interconnect.

Higher κ materials will be targeted for BEOL decoupling capacitors in logic and SoC beginning at the 130 nm node. The driver of increased permittivity to support a conservation of interconnect real estate must be balanced with compatibility requirements of these higher κ materials with the evolving BEOL process technologies. The primary focus will be on thermal, mechanical, and stress properties of these films. Topographical challenges associated with multi-layer capacitor structures may require CMP development. The technical requirements of these materials consist of frequency invariance of permittivity matched to the device operating needs, low electrical leakage, *I-V* linearity and available/compatible electrode materials. CVD tantalum oxide is the most widely used of the commercially implemented high κ materials, with multiple supplier support. Development of aluminum oxide (MIM) structures continues. Perovskites (BST, PZT) still require additional development to reduce process temperatures while achieving higher permittivity values.

Low κ FSG (κ=3.7) materials have been in production since the 250 nm node, and were introduced into the 180 nm node with Cu dual Damascene. The measurable performance benefit derived from FSG, spurred the aggressive introduction of lower κ materials (κ<3.0) at the 130 nm node, with organic spin-on-polymers (SOP) and both spin-on and PECVD inorganic/organic hybrid materials. These materials have been commercially implemented as monolithic dielectric layers, dual layers with an intermediate etch stop layer and as hybrid dielectric layers with USG at the via level. The most challenging integration modules are dielectric etch, integrated clean, CMP, and packaging.

Lower κ dielectric materials (κ<2.5) are in development. Integration efforts focus on solving the problems of these reduced density materials with their compromised thermal and mechanical properties. This inevitable trend in density reduction is most troublesome for CMP and packaging. Although incorporation of fluorine into low κ materials reduces dielectric constant approximately 10%, further reductions in FSG were found to be incompatible with refractory metal liner materials; the use of fluorine-containing ULK and ELK materials must therefore be carefully considered. The ideal ultra-low κ material (κ<2.5) will have a closed pore structure and uniformly distributed pores with a maximum pore size, tied to, and decreasing with, technology node. A tight pore size distribution is also desirable.

The effective permittivity encountered by the signal in the interconnect structure is the most important parameter, and this has as much to do with the integration scheme as the permittivity of the bulk interlayer dielectric. Each material in the ILD stack contributes to the κ_{eff} (etch stop, Cu capping layer and hard mask (s). Novel integration schemes may still be required, in addition to these ultra low κ materials, to realize a κ_{eff} of 2.0 or less.

RF and optical interconnect are the leading technologies poised to replace conventional wiring and alleviate the global interconnect problem. Oxide-based optical interconnects are a logical step, but current deposition technologies are incapable of producing material of sufficient quality for direct implementation. Transition metal purity and hydroxol content must improve by several orders of magnitude, in some cases, to meet acceptable loss targets. The challenge for polymeric materials will be achievement of sufficient refractive index contrast between core and cladding layers to ensure low loss at small radius turns. The conversion efficiencies (electron to photon and photon to electron) still need to be significantly improved for insertion at design frequencies greater than 10 GHz. One advantage of optical interconnects is the application of wavelength and frequency multiplexing of signals simultaneously on the same interconnect. Local (on chip) RF is also being explored.

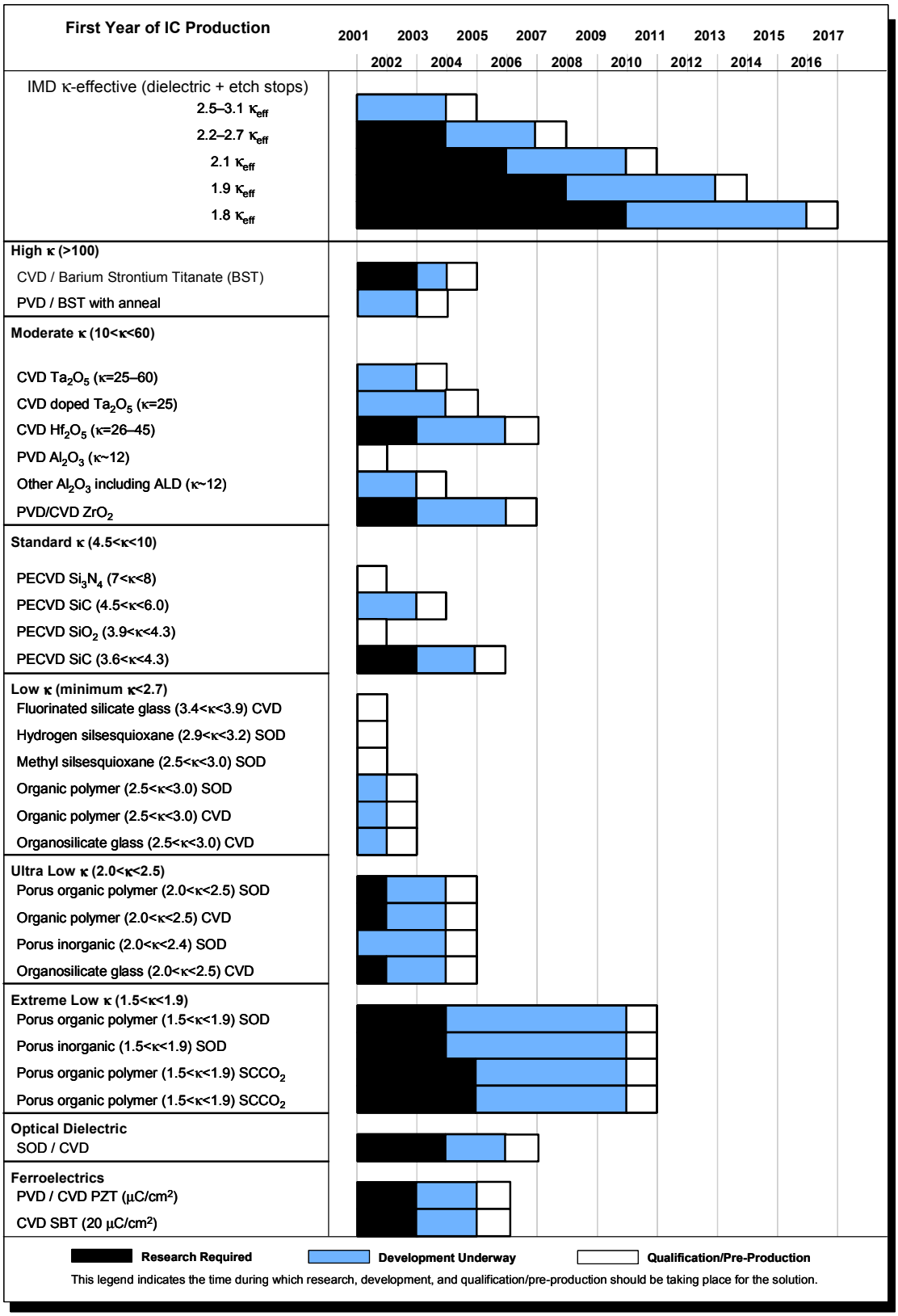


Figure 38 Dielectric Potential Solutions

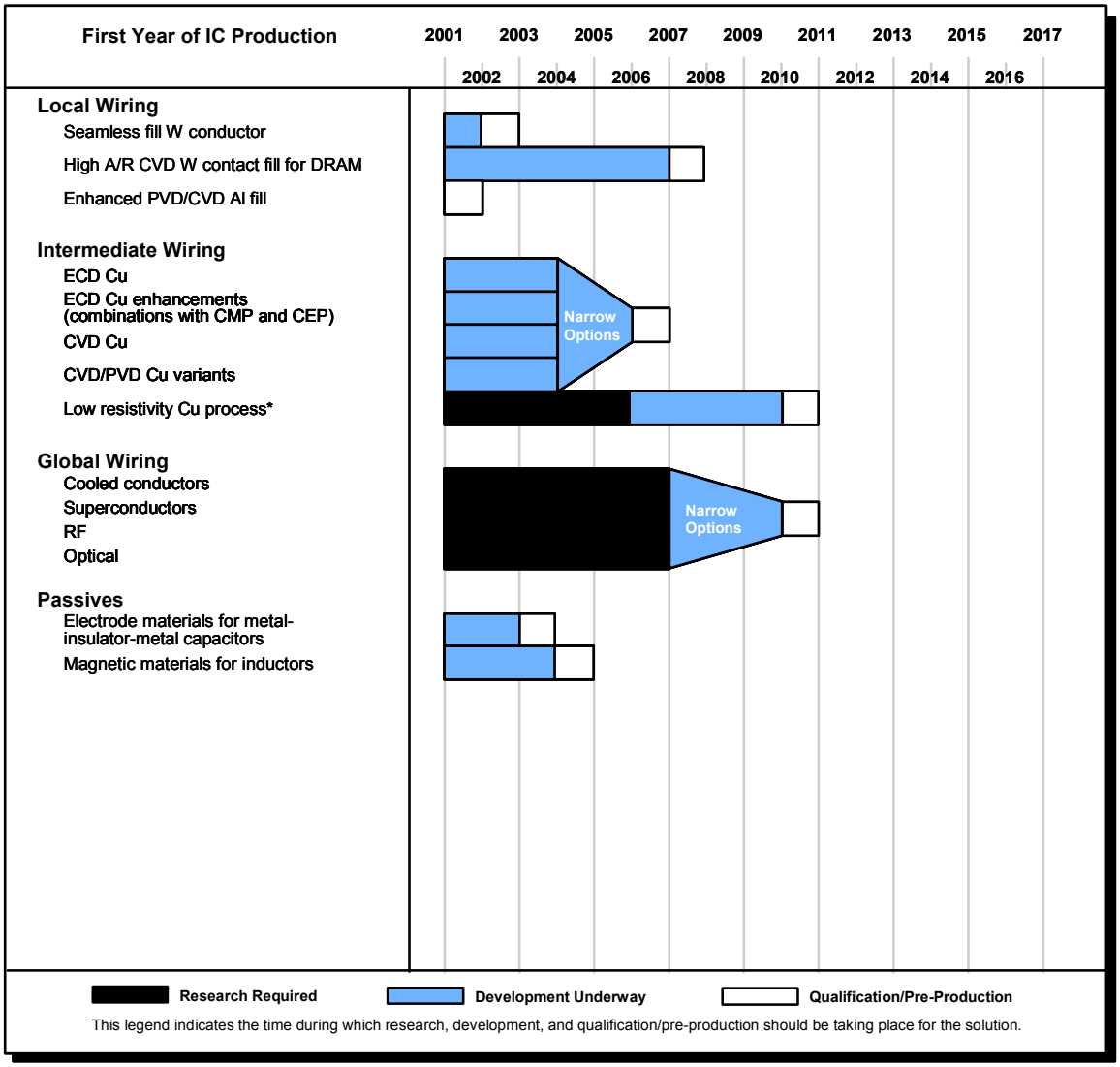
CONDUCTOR POTENTIAL SOLUTIONS

Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, ASICs and DRAMs. ALD, in conjunction with CVD techniques, will be utilized first in the W deposition area to accomplish a seamless W fill. These same techniques, with more emphasis on ALD, need to be employed to accomplish W fill of high aspect ratio (15:1 in 2007) contacts for stacked capacitor DRAM designs. Other materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts, which are projected to have aspect rations greater than 20:1 by 2016. Aluminum may continue to be used for local wiring. Enhanced CVD/PVD flow techniques may also be utilized for Damascene architectures. Cu will also be used for local wiring levels and these will be the first to be impacted by the size effects that will increase Cu resistivity toward the end of the period covered by the 2001 ITRS.

Cu will be the preferred solution for the intermediate wiring levels in microprocessors and ASICs and electrochemical deposition will continue to dominate the market in the near term. CVD Cu fill may become competitive as a fill technology if the same "superfilling" behavior and microstructure characteristic of ECD can be achieved. At the intermediate wiring pitches predicted for the long-term years of this Roadmap, size effects will also increase Cu resistivity for intermediate wiring levels. This is much more problematic since intermediate wiring traverses longer lengths and is much more likely to impact performance than local wiring. Cu interfaces, microstructures and impurity levels will be engineered to alleviate the impact of this resistivity rise for a few additional technology generations.

Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. However, scaling at each technology generation has the largest impact on global wiring levels that nominally traverse lengths on the order of the die size. This problem is currently being addressed by the judicious use of repeaters, or by oversized drivers, which impact both chip size and power. Future potential solutions include RF, optical, cooled conductors and superconductors, which are expected to be introduced into manufacturing at the beginning of the long-term years of this Roadmap.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of metal-insulator-metal (MIM) capacitors to improve yield and reliability. Both Al and Cu are currently in use for standard spiral inductors, but in the future various magnetic materials may emerge with different inductor designs to reduce the area of these devices.



**Cu process with optimized interfaces, microstructure and impurities to alleviate resistivity rise at small critical dimensions*

Figure 39 Conductor Potential Solutions

BARRIER POTENTIAL SOLUTIONS

Ti/TiN will continue to be used as the contact and for barrier materials for high aspect ratio contacts (e.g., DRAM stacked capacitor) filled with W conductor. Long throw and ionized PVD, as well as CVD and ALD techniques, will be developed as potential solutions in this area. In addition, surface treatments of the TiN with SiH_4 and other gaseous species will be used to enhance nucleation of the subsequently deposited CVD or ALD W film.

The barrier materials used for Cu wiring will continue to be selected from the nitrides and silicon nitrides of Ta, Ti, and W. Long throw, ionized PVD and CVD deposition will continue to be the predominate solutions. However, ALD deposition methods will emerge as the dominant solutions because of their superior conformality and improved thickness control. In addition, elimination of deposited barriers may be possible through *in situ* treatment of the etched low κ dielectric sidewall to form an effective barrier to Cu diffusion. Barriers will undoubtedly be a key focus area toward the long term years of this Roadmap, since engineering the smoothness and other properties of the Cu barrier interface will be key to ameliorating the expected Cu resistivity increase due to electron scattering effects.

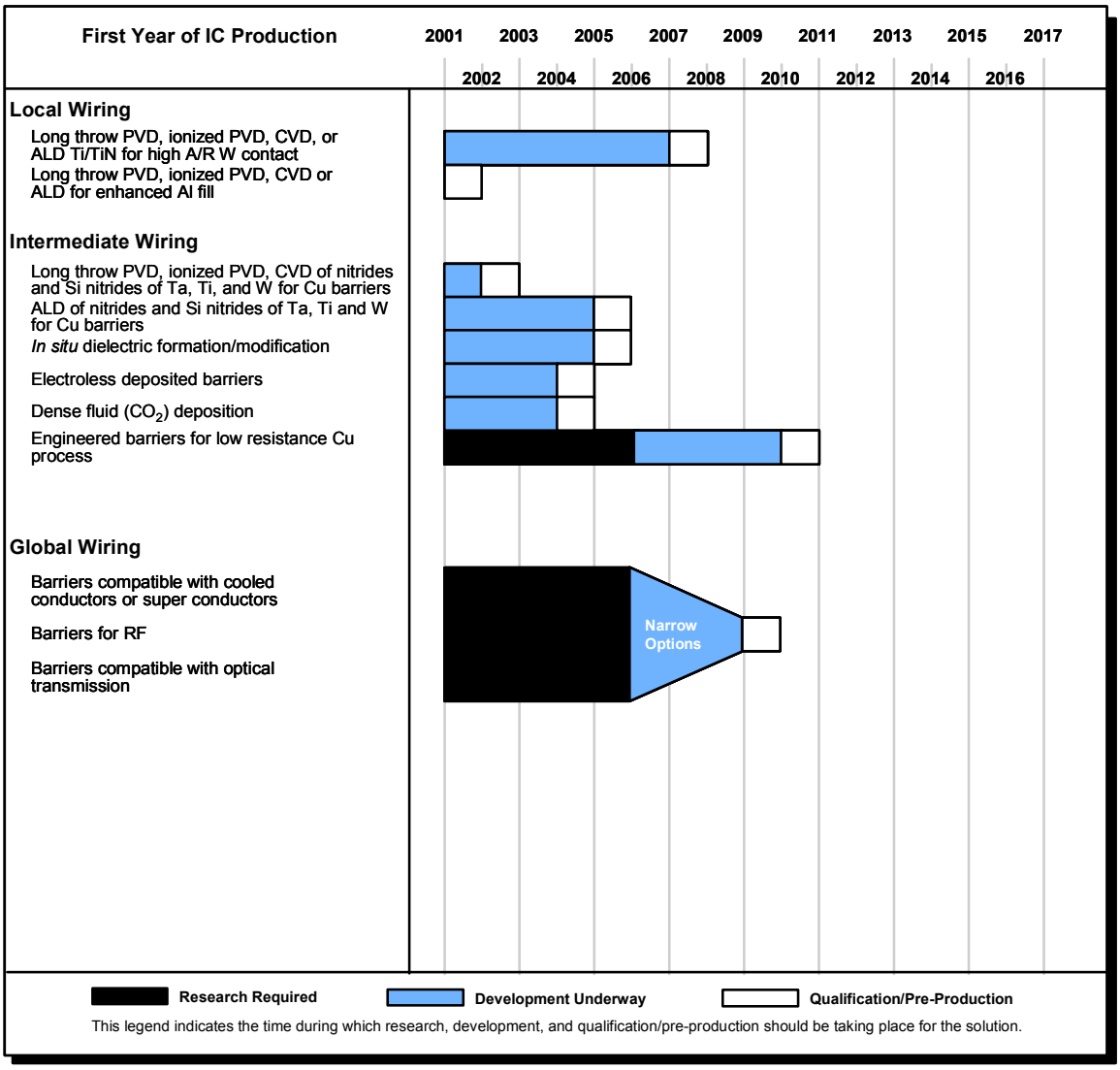


Figure 40 Barrier Potential Solutions

NUCLEATION POTENTIAL SOLUTIONS

PVD Cu deposited through either long throw or various ionized PVD techniques continues to be the dominant nucleation layer for ECD Cu. Since these PVD techniques yield marginal coverage on next generation dual Damascene structures, electroless and ECD Cu seed layer repair are being developed as nucleation solutions over the next few years. As a more extendible solution to the issue of seed conformality in high aspect ratio structures, electroless Cu seed, direct ECD plating on barriers—such as seedless ECD, CVD Cu seed, and enhanced PVD seeds—are being pursued. These are expected to emerge and be ready for manufacturing by the 65 nm technology node. Figure 41 shows the nucleation potential solutions chart.

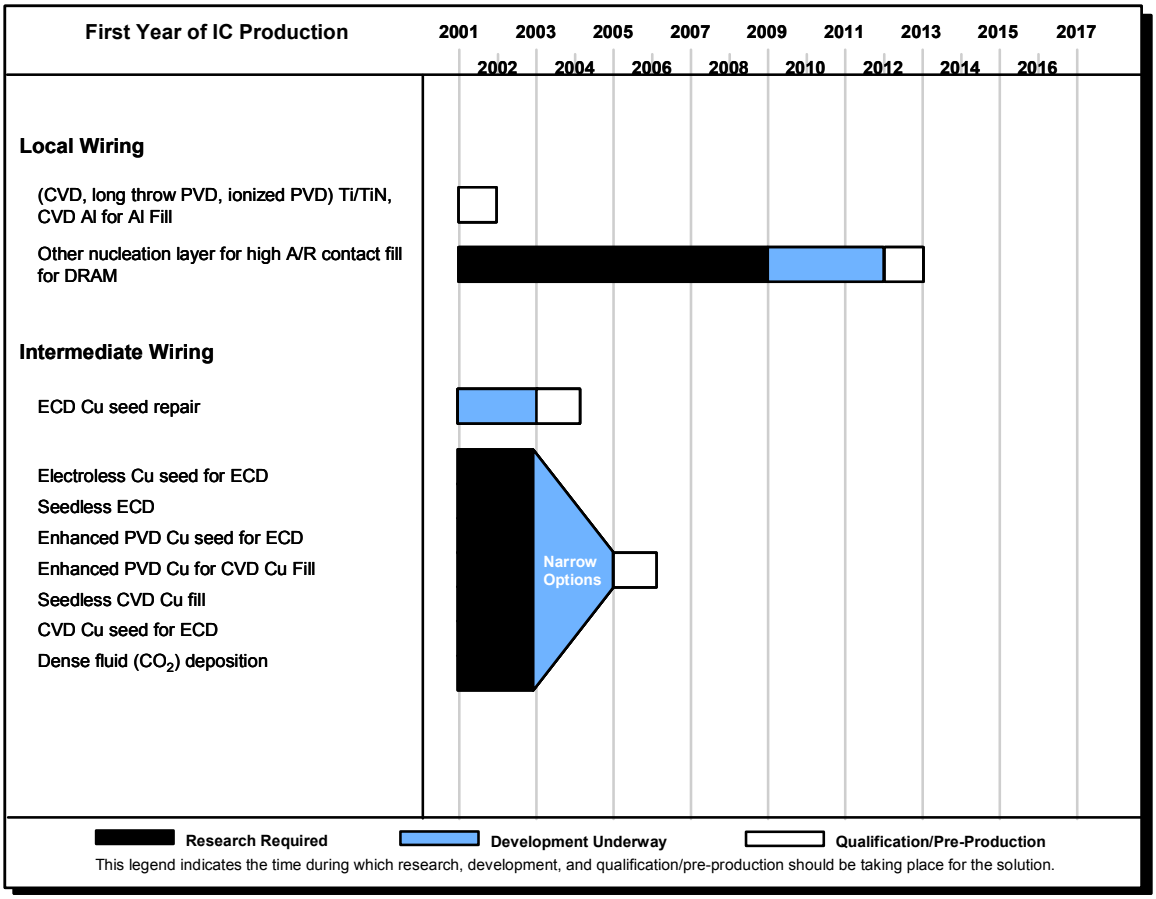


Figure 41 Nucleation Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Planarization continues to be a critical and enabling step for interconnect technology. As the materials comprising the interconnects become less conventional and the demands on planarization tolerances become more exacting, the planarization processes themselves become more closely coupled to the choice of an integration scheme. Chemical-mechanical polishing remains the leading planarization technology in current and future manufacturing.

The CMP of silicon dioxide for ILD and pre-metal dielectrics and CMP of tungsten for plugs/local interconnect will remain a requirement for the foreseeable future. The accelerating industry movement to Cu Damascene technology has resulted in the need for Cu CMP processes that address advanced material requirements spanning three technology nodes: Cu/SiO_2, Cu/low κ dielectrics, and Cu/ultra-low κ dielectrics. Each of these BEOL material sets brings new metal planarization challenges. Among these is the need to reduce the mechanical forces applied to the wafer during CMP, in order to prevent adhesive/cohesive failures in the dielectric, due to the reduced mechanical strength of many porous ULK dielectrics. Although this problem can be alleviated through integration choices, an effective dielectric constant performance penalty is likely.

As minimum wire dimensions scale with each new technology node, the primary influence that planarization has on control of wire thickness becomes increasingly important. Thinning of the local and intermediate Cu wiring at minimum pitch is a result of pattern erosion during CMP. Thinning of the global wiring results from both pattern erosion and dishing of the individual wires. With the projected scaling of wire thickness, it is likely that Cu thinning due to CMP must be limited to less than 10% of the nominal thickness for any interconnect level. For the wide global features, Cu dishing from CMP results in localized non-planarity, leading to conductive defects at subsequent interconnect layers. Tighter control of metal planarization will need to be addressed by improvements in all facets of CMP, including tools (end point, removal non-uniformity, process parameters), slurries (selectivity), and pads (planarization lengths).

Related links are provided for *thinning of the local and intermediate Cu wiring at minimum pitch*; thinning of the *global wiring from both pattern erosion and dishing of the individual wires*, and *wide global features and Cu dishing from CMP*.

Development will continue in alternative metal planarization techniques, sometimes referred to as Chemically Enhanced Planarization (CEP) and the similar spin-etch planarization (SEP). These two approaches use controlled chemical etching of metals to avoid some of the disadvantages associated with CMP processing, such as dielectric erosion. They may also employ electrochemical and diffusion-controlled chemical reactions for planarizing. Combining CEP/SEP with conventional CMP may be particularly useful for productivity enhancements and compatibility with weak/porous dielectrics.

Planarization tools for metal CMP must evolve so that Cu can be polished in the advanced dielectrics. The current breed tools all control relative speed and distributed force to the wafer surface, with techniques to enhance cross-wafer slurry transport. Various polish endpoint detection techniques are used, with inline dielectric thickness metrology as an available option. Integrated wafer cleaning is a popular architecture for metal planarization tools. It is important that future tools be designed for processing Cu in low κ and ultra low κ dielectrics. In addition to the above features, the next generation tool for manufacturing may include tribological metrology to measure frictional forces, and *in situ* (or inline) metrology for dielectric and metal thickness, planarity, defects/residuals, and reliable full-wafer endpoint detection for both Cu and barrier films. These features will enable a machine-tunable, radially uniform, polish and allow an improved implementation of automatic process control (APC). The polisher is likely to have fully integrated slurry metrology and to incorporate a number of "green tool" features. Beyond the next generation, the futuristic CMP tool may be specifically designed to operate in a low-shear-force region of the CMP process space. This may require novel tool designs. Tribological metrology may be fully integrated for active force control. Metrology and active control of the wafer surface temperature may become important to control the polishing chemical reaction. Tools may have the capability of precision "point-of-use" slurry mixing, and a green tool design should be well established.

Advances in CMP consumables will share equal importance with tools in enabling future metal planarization. The attention focused on polishing slurries has resulted in significant improvements in their performance. Producing slurries with controlled selectivities for Cu/barrier/dielectric has allowed the user to engineer the polish sequence for minimal Cu thinning. At the same time, attention must be paid to the slurries' role in creating scratch and residual defects on the Cu wires and dielectric surfaces, and corrosion of the Cu wires. The RMS roughness of the polished Cu surface may become important, as interface scattering effects start to influence the conductivity of small wires. The advent of solids-free CMP chemistries for Cu may improve manufacturing margin through improved selectivity and dishing control, two areas that may also be addressed by fixed-abrasive pads. Development of new abrasive materials with engineered chemical-physical properties and engineered pad materials both may lead to enhanced precision in the metal polishing process. What is demonstrated by these consumable innovations is the less explored regions of CMP process space (both *chem-* and *mech-*) that may hold answers to problems of metal planarization in the future. A materials pathway to a low shear force metal polish is a potential solution. For CMP consumables it is expected that a path of continuous improvement will be taken.

Post-CMP wafer cleaning will likely become more closely integrated with the metal planarization process. With respect to tools, the combined polisher/cleaner for Cu CMP is common in manufacturing. The brush scrubber, in combination with megasonic and chemical treatments, is currently favored. The chemistries employed for cleaning are now formulated for metal applications, and in the future may need to be tailored for the specific slurry and CMP process with which they are used. Since the chemical characteristics of the cleanable defects are more and more determined by the slurry used and the polishing byproducts, closer collaboration between the slurry providers, chemical providers, and end user will be required. Metal corrosion remains a concern, as it is often tied to the specifics of the metals deposition. Development will continue on alternative cleaning technologies.

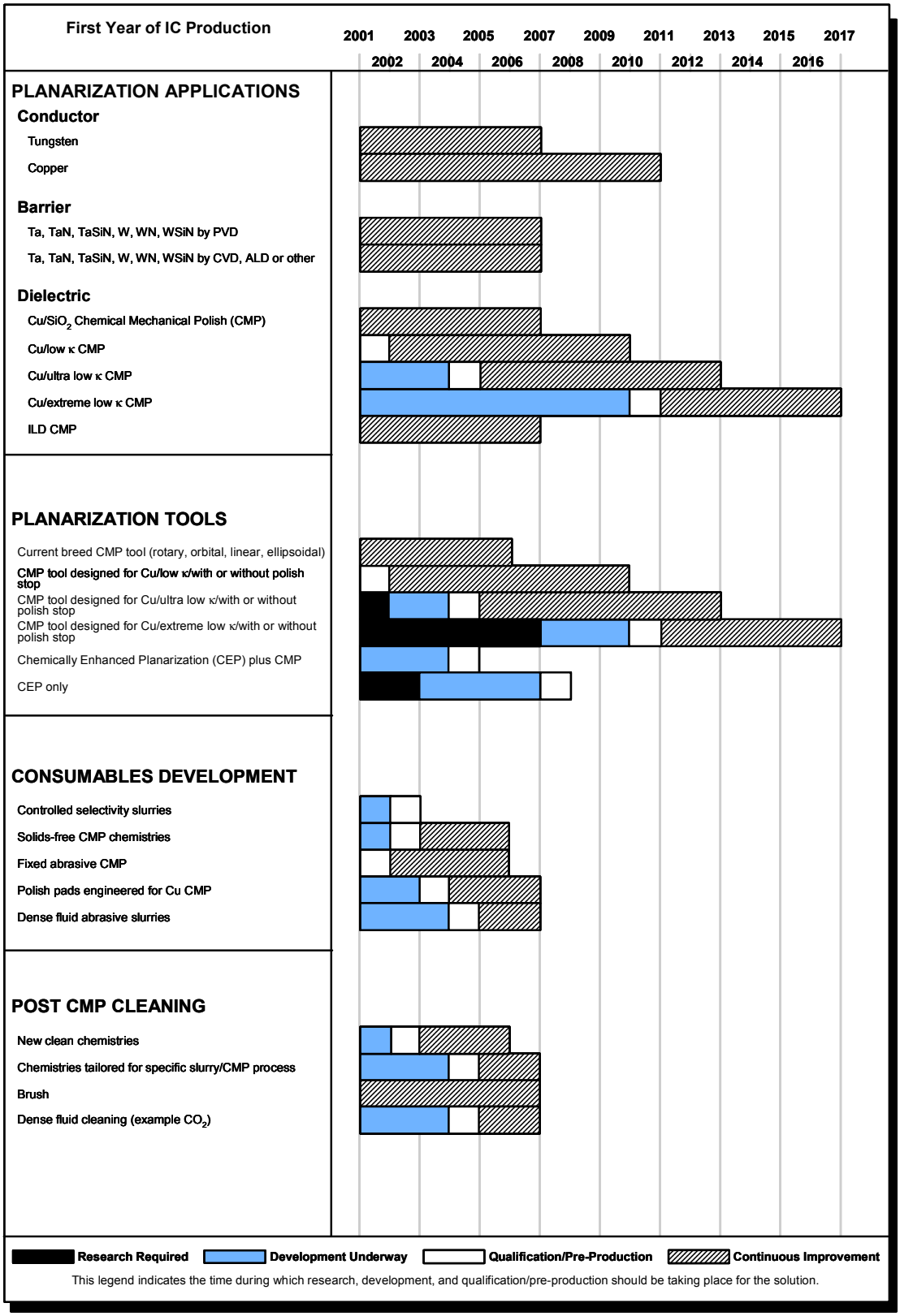


Figure 42 Planarization Potential Solutions

ETCH, STRIP, AND CLEAN POTENTIAL SOLUTIONS

Plasma etching of interconnect structures will be required throughout the ITRS forecast period, as shown in Figure 43. Subtractive metal etch, the standard for pattern transfer for many decades, will continue to be used for DRAM until at least 100 nm half pitch; there may also be applications in logic products with copper wiring that include aluminum at the packaging interface. RIE etch of high A/R aluminum conductors for DRAM at 90 nm and below is expected to be extremely difficult and will require continued development by tool suppliers, for those manufacturers who do migrate to Cu. High aspect ratio W contacts for Al DRAM technologies may see an additional challenge with the incorporation of low κ materials requiring new development in sidewall passivation chemistries. Contact/via etch for all product classes will extend to 22 nm. Damascene and dual Damascene approaches will be utilized with copper conductors.

The Reactive Ion Etching (RIE) process will continue to be applied to an increasing diversity of materials. New material introductions for BEOL ILD materials, capacitor structures (electrode and storage materials) as well as Cu capping or barrier materials. Development of needed etch capability must be timed to match the permittivity trend in the dielectric potential solutions roadmap. There is no strong drive for novel plasma source technology development but rather a focus on etch and passivation chemistry strategies required for multi component materials and integration stack configurations. Porous materials are particularly sensitive to distortion, and geometric control and aspect-ratio-dependent etching effects (ARDE) must be minimized. Etch processes must not introduce electrical, chemical, or physical damage, for the 65 nm node, new processes such as neutral stream, are a potential solution.

Many new interconnect materials are associated with the ILD, capacitors and their electrodes, barriers, hard mask and capping layers and top and bottom antireflection layers. The BEOL ILD will introduce increasing organic content coincident with the simultaneous increase in porosity to reduce dielectric constant. This hybridization of the ILD material, now containing both organic and inorganic functionality, must meet the dual challenges of minimizing the effective κ of the stack with the use of a reduced κ etch stop and capping materials as well as the selectivity needs. Cu barrier and capping layer improvements will introduce several new classes of materials which maybe be multi-component in nature, likely amorphous, and continually thinner to address lower κ_{eff} targets. These Cu cap layers represent the etch stop material at the bottom of the high aspect ratio dual Damascene contact that must offer continual higher selectivity to the low κ ILD etch chemistry to address this projected thinning.

Emerging capacitor materials and novel electrode materials will create challenging etching requirements. Multi-component capacitor materials will require significant etch chemistry development. Coupled with the use of noble metal electrode materials, there may be a requirement for different plasma etch chemistries incorporated on the same etch platform.

These interconnect materials create new cleaning challenges associated with surface preparation and post-etch residue removal. Cleaning technology encompassing dry, semi-dry, wet and combinations will be required. Wet cleans, effective for metallic removal, will be incorporated on platforms with more dilute chemistries, and point of use generation and dispense. Semi-dry modifications of wet cleans, those that utilize aqueous ammonia and ozonated water or acids, will also move away from batch to single wafer with the same point of use needs. Dry cleaning methods are likely to be used for surface preparation or "conditioning" prior to deposition but are inefficient for removing elevated concentrations of metallic elements.

Damascene structures will force a change in photoresist stripping and subsequent cleaning. The complete move from wet to plasma or dry etching is not possible for the subsequent cleans/strips. Oxygen-based chemistries are often used for etching organic low κ dielectrics for trench, via and contact steps. Unfortunately, dry processes, generally used to remove organic materials, may be insufficient to remove residues and particles from structures with high aspect ratios without attacking the low κ dielectrics or copper barrier structures. Wet chemicals or other techniques, including the use of supercritical or dense fluids, can be effective and may be necessary. These fluids, especially when combined with surfactants or co-solvents, can be particularly effective in high A/R features for cleaning and stripping.

Alternative stripping gases, such as hydrogen-reducing chemistries, might be needed for porous silicon oxide or similar low κ materials. Cryogenic aerosol technologies which create ice crystals from cooled argon or nitrogen can be effective for particulate removal and are environmentally benign. High κ materials and capacitor electrodes which might contain barium strontium titanate or ruthenium, etc., have their own unique set of challenges. The most promising hybrid approaches will combine multiple technologies in gas phase and liquids to meet both surface preparation, cleaning and

stripping requirements. Other issues that will affect the future development of these technologies include finding new chemistries that are compatible with ESH mandates, selectivity needs, and electrical requirements.

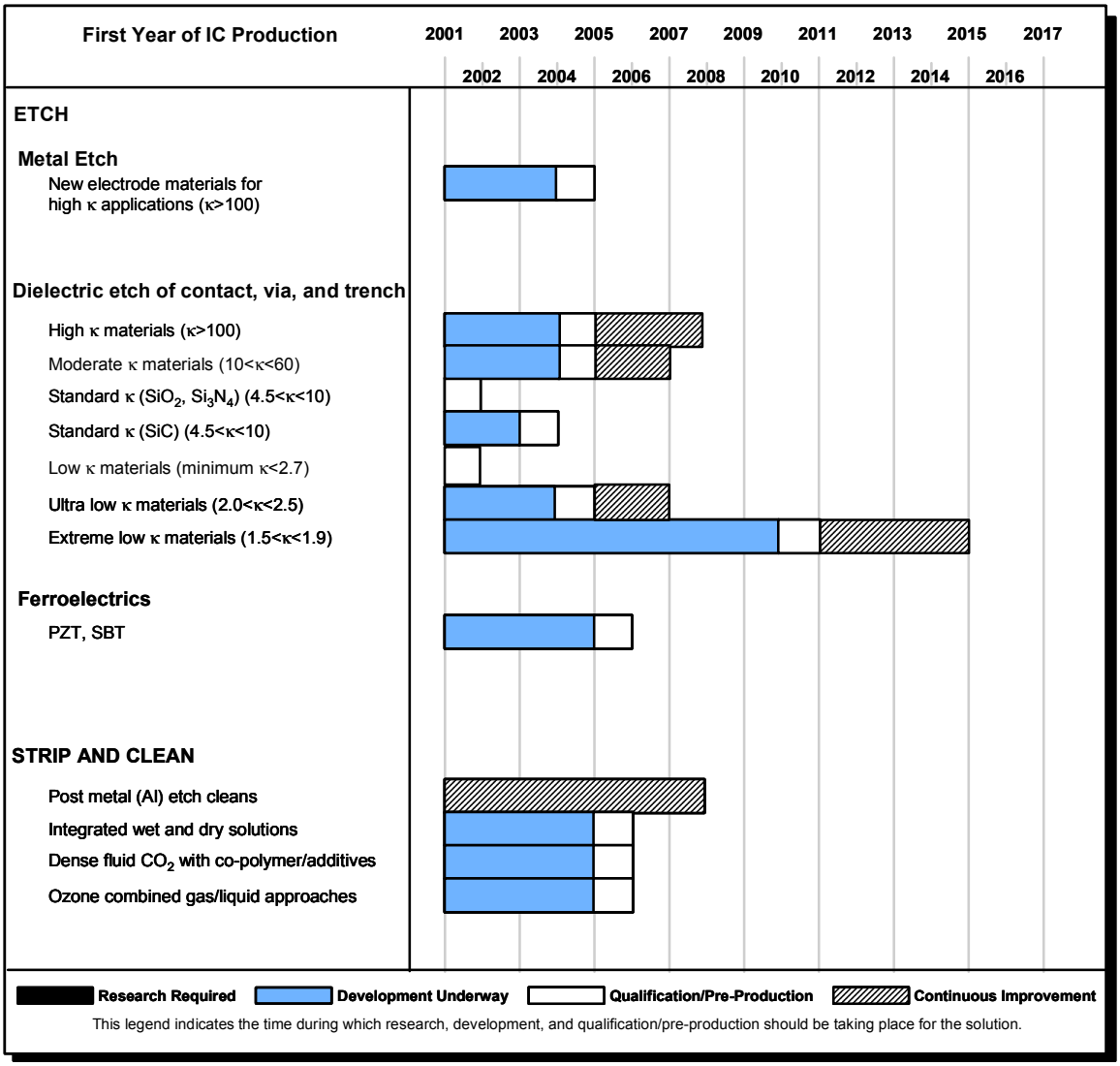


Figure 43 Etch, Strip, and Clean Potential Solutions

RELIABILITY

The semiconductor industry move to copper metallization promises significant improvements in interconnect current-carrying capacity and high-temperature operation, but presents numerous new material integration and reliability challenges. Since copper readily diffuses into silicon and most dielectrics, it must be encapsulated with metallic (such as Ta, TaN) or dielectric (such as SiN, SiC) diffusion barriers to prevent electrical leakage between metal wires and degradation of transistor performance. Cu diffusion is also greatly enhanced by electric fields imposed between adjacent wires during device operation, and absolute barrier integrity is crucial to long term device reliability. As barrier thickness scales with metal width to meet effective resistivity goals, copper containment becomes increasingly more problematic, and eventually new copper passivation techniques and/or diffusion-resistant dielectrics are needed to provide "zero thickness" solutions.

Copper, unlike aluminum, has no self-passivation layer. Therefore, surface diffusion is expected to dominate electromigration behavior, and material interfaces will play a key role in determining overall reliability. Maintaining the mechanical and electrical integrity of dielectric and metal barriers, particularly at their critical corner juncture, will also be essential to prevent catastrophic copper diffusion between metal leads. CVD copper barriers and seed layers, while providing scaling relief, bring additional integration concerns, and the impact of texture and intermixed CVD/ECD copper layers must be understood.

Damascene structures may change the approach to photoresist stripping and subsequent cleaning for interconnect layers. The use of hard mask materials and oxygen-based chemistries for etching organic low κ dielectrics enables *in situ* stripping of the photoresist during the trench, contact or via etch steps. Dry stripping alone may be insufficient to remove residues and particles from structures with high aspect ratios without attacking the low κ dielectrics or copper and its barriers. The implementation of porous silicon oxide or similar low κ materials may allow the continued use of traditional oxygen-based stripping processes, but the detailed reliability implications of this combination of processes and materials will need to be understood. All of these unit processes bring their own specific yield loss mechanisms as well as susceptibility to longer term reliability problems.

The integration of new low κ dielectrics needed for performance enhancement bring numerous reliability concerns that include thermally or mechanically-induced cracking or adhesion loss, poor mechanical strength, moisture absorption, time-dependent behavior, texture effects, and poor thermal conductivity. The typical thermal conductivity of low κ dielectrics is less than one third that of oxide, leading to higher metal wire temperatures and enhanced electromigration. Bi-layer or embedded oxide/low κ dielectric schemes may be required to enhance the mechanical strength and heat dissipation of future low κ dielectric systems.

The lessened mechanical strength of low κ dielectrics and anticipated higher temperature operation of some of the copper interconnects will drive the need for novel packaging techniques and structures. These, combined with the move to higher packaging process temperatures and migration to Pb-free solders, will provide new reliability challenges for the research and development community to resolve. Expanding use of advanced technology in assembly, such as area-array bumps, need to be considered and integrated with circuit, material, and process selections in order to maintain product reliability in the future. This is especially important to encompass low κ dielectrics and assembly-related process steps, so that steps such as under-bump fill, integrate with low κ.

Computer-aided design (CAD) tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- Wire length
- Current densities expected for the currents required by the circuit
- Calculated local operating temperature, which includes the effects of Joule heating in the circuit and elsewhere

These tools will need to become an integral part of the circuit designer's tool set to aid in the prediction of product reliability before processing begins and to develop solutions that anticipate technology and thereby accelerate their introduction.

Continuing research is needed to fully understand the multi-variable nature of copper and low κ interconnect reliability and provide accurate models for designed-in reliability. The fundamental limits of copper metallization must also be explored to assess technology extendibility, especially to feature sizes where electron surface scattering effects become a significant contributor to resistivity (< 45 nm for Cu).

It is expected that one or more alternate interconnect approaches, such as optical interconnects, package intermediated interconnects, 3D interconnects, or microwave interconnects will begin to be used within the next five years. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

SYSTEMS AND PERFORMANCE ISSUES

INTERCONNECT PERFORMANCE

The adequacy of near-term interconnect technologies (copper wires and low κ dielectrics) to continue meeting the performance requirements for ICs fabricated for succeeding technology nodes varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. For a constant span of gates (such as 40 gates), the signal delay time for local wires is typically a small fraction of a clock cycle, and is expected to decrease at a rate similar to the reduction of the gate propagation delay as a function of technology scaling. This trend is expected to continue down to the 65 nm or 45 nm nodes, at which point the signal delay for local wires will begin to increase. The delay for intermediate wires in terms of half the perimeter of a functional block will grow only slightly with technology scaling. Conversely, crosstalk and noise for local wires (and some intermediate wires) are expected to increase with decreasing wire pitch. These trends are a strong function of design strategy, and should be considered in that context.

It has been shown by several researchers that the global interconnect performance needed for future generations of ICs cannot be achieved even with the most optimistic values of metal resistivity and dielectric constant. The signal delay time for global wires will continue to increase with technology scaling primarily due to the increasing resistance of the wires and their increasing lengths (delay for a non-repeated wire increases with the square of wire length). Power distribution at constant voltage through equipotential wires to all V_{dd} bias points requires increasingly lower resistance global wires to avoid the voltage drop problem. The increasing power supply current, related to the decreasing V_{dd}, causes an increased voltage drop between power supply and the bias point for fixed global wire resistance. Consequently, this requirement demands increasingly lower resistance paths from the power supply to the V_{dd} bias points. This need is being partially addressed by the introduction of ball-grid-array packaging technology that distributes power feeds across the area of the chip, eliminating much of the on-chip lateral power feeds through relatively high-resistance global wires. Interconnect nets for distributing clock signals and power can dissipate up to 40-50 % of the power on the chip, which may exceed 120 Watts.

SYSTEM LEVEL INTEGRATION

System level integration encompasses the physical and functional assembly of a system's macro functions to achieve its desired operating characteristics. Assembly of individual functional components (such as bare chip or block functions on a single chip) into the system must encompass all the performance and reliability requirements imposed on the system. For interconnect, the requirements are currently met through the distinctly separate functions of on-chip interconnect, packaging and board-level technologies. It is now widely conceded that technology alone (in the short term, and probably not in the long term) cannot solve the on-chip global interconnect problem with current design methodologies. Rather, the current view is that design, process technology, packaging, and board construction will all need to come together to provide an optimized integrated system level solution for interconnect requirements.

The current projection for evolution of interconnect is that in the short term interconnect delay problems in new ICs will be met by circuit design within the constraints of planar technology with special attention to minimizing the lengths of critical paths. This will be done in concert with a substantial push in Cu-low κ technology, as well as more innovative

packaging and board approaches, to minimize the changes needed in design architectures while still meeting the continued advances in performance projected by the ITRS. In the intermediate term, Cu-low κ will be pushed to its limits, and new design architectures as well as chip-package co-design will be achieved with new CAD tools to significantly facilitate needed performance advances. Beyond these extrapolations of current practices, radically new design, packaging, and technology options will be needed.

Many changes are envisioned to meet the needs for advanced interconnect. Among the design options being considered are items such as non-synchronous clocking, interconnect-centric architectures and design tools, and interconnect-aware verification and analysis. The packaging community is expected to impact the global interconnect problem in the near term with optimized co-design of the chip and package interconnects. This approach will lead naturally to the total optimized system in a single package (SIP). The SIP approach can provide many unique capabilities for interconnect, including transfer of high-speed clocks and signals to thick package leads to minimize RC delay and use of specialized chips for interconnect functions. In the longer term, innovations such as wafer-scale packaging and package intermediated intra- and inter-chip interconnects will be needed to assist in alleviating the interconnect problem. Many new technology options are currently envisioned beyond the immediate Cu-low κ and IC/package redesign. These may include microwave interconnects, package-mediated interconnects (such as multi-chip packages, active substrate packages, etc.), RF package coupled interconnects, 3D ICs, optical interconnects, and nanotubes. Other futuristic approaches such as self-assembled interconnects and quantum communications via spin are intriguing concepts, but will require major innovations to be useful in circuit applications.

Each of the higher system level approaches listed above has the potential to minimize the problems associated with global interconnect. Research and development in all of these areas is needed to ensure timely availability of these future options

NEW INTERCONNECT CONCEPTS

The need for new interconnect concepts, *beyond the traditional metal/dielectric system,* was pointed out dramatically during the 1997 roadmap development. It was realized that the continued push to smaller geometries, higher frequencies, and larger chip sizes rapidly resulted in an incompatibility between interconnect needs and projected interconnect performance. Further analysis has shown that the problem is primarily with global interconnects, and for this case the traditional metal/dielectric interconnect systems will not meet advanced roadmap requirements using even the most optimistic estimates of resistance and dielectric constants. This recognition has led to investigations into new interconnect concepts to continue IC technology along the Moore's law curve. The totality of new concepts that have been identified as possible resolutions to global interconnect issues is extensive and a few options and some of their critical issues are described.

DESIGN OPTIONS

Minimization of global interconnect length through design modifications is the quickest means of circumventing global interconnect shortcomings. Although this may seem simple to implement, there are several significant obstacles. The most difficult obstacle is that when design modifications to minimize global interconnect lengths are described, few automated design tools are available that can use these ideas to optimize performance. Also, when tools are available, the models of interconnect performance are generally complex and slow to execute, and are therefore not compatible with the rapid iterations needed for design optimization. Without significant innovations in design tools and design technology, these limitations will cause significant segments of high performance designs to be customized, resulting in poor design productivity. Alternative approaches have been proposed that eliminate the need for global interconnect, such as moving to non-synchronous designs. However, such approaches incur additional complications at the system design level, and may also suffer from design tool shortfalls. It is imperative that researchers continue to study design options.

PACKAGING INTERMEDIATED INTERCONNECTS

One option for reducing the global interconnect problem is to move some of the interconnects from the primary chip to thicker metallization and higher performance levels on the package, or on a supplementary chip designed to carry only interconnects. These signals would then be transferred back to the primary chip at an appropriate point. In some cases, a "sea of leads" approach might be used to provide major density increases in I/O to benefit not only global interconnect, but at the same time, power and ground connections. These approaches offer many significant opportunities, but are subject to critical potential shortcomings in cost and reliability. The additional interconnects from the primary chip to the board, and the cost of a supplementary chip and its interconnects, bring significant liabilities to this approach. Creative

research is needed to provide new implementations of this approach that will circumvent the inherent cost and reliability limitations.

RF/MICROWAVE INTERCONNECTS

A relatively radical alternative to the usual metal/dielectric interconnect option is to use electromagnetic transmission of signals from one part of a chip to another. This option essentially takes the form of a LAN on a chip, with transmitters and receivers combining antennas and appropriate signal generation and signal detection circuitry. Transmission in this case has been proposed to be a "free-space transmission" through the package and IC structures, as well as being capacitively coupled through a waveguide in the package lid. The transmission has been proposed as a sinusoidal signal or as a coded signal, depending on the specific system concept employed. Each option has its own particular advantages and disadvantages, as well as its own unique requirements. This approach has the advantage of being relatively easily implemented using available projected technology, but requires significant design effort and chip real estate for the transmission and reception elements. The basic concepts of this approach to global interconnects have been demonstrated, but significant research is required in order to identify the optimum system concept and to minimize overhead design and chip real estate needs in implementation.

OPTICAL INTERCONNECTS

Optical interconnects are considered a primary option for replacing the conductor/dielectric system for global interconnects. The optical approach has many variants, the simplest perhaps having emitters off-chip and only free space waveguides and detectors in top layers on-chip. Progressively more complex options culminate in monolithic emitters, waveguides, and detectors. The optical interconnect option has many advantages, but also has several clear areas requiring significant research. The decisions on which signals to include in optical communications and which remain in conventional metal dielectric, and the choice of on-chip optical emitters, are significant. In the case of optical interconnects, it is easy to assume that this solution will meet speed requirements because the signal travels at "the speed of light." However, to define the total interconnect system for this approach it is necessary to consider the delays associated with rise and fall times of optical emitters and detectors, the speed of light, losses in the optical waveguides (if used), the signal noise due to coupling between waveguides, and a myriad of other details of this approach. Critical issues for optical interconnect are not only the technology to provide optical signaling, but also the appropriate design tools to optimally design the emitters, waveguides, and detectors.

3D INTERCONNECTS

3D interconnects have been proposed as one of the most promising solutions for achieving high density device packaging and interconnects. Multiple levels of active devices are stacked on top of one another to minimize the distance required for interconnects. The stacked layers may be separate chips with innovative "through wafer" contacts, or multiple stacks of active devices. One advantage of this method is that it can be used not only to minimize the distance that global interconnects must span, but also to provide integrated repeaters within the 3D layers to facilitate high-speed signal transmission. This approach takes many forms and opens many new areas of research. Among these area are critical alignment tolerances, material performance and compatibility issues, and heat management issues. Of these, heat extraction from within the multiple levels is a new key problem. Commercial viability of this approach hinges on research into these and many other issues.

RADICAL SOLUTIONS

In addition to the aforementioned options for global interconnect solutions, there are several more radical options that may offer unique advantages. These radical alternatives include nanotubes, spin coupling, and molecular interconnects. Nanotubes of various constructions are most often noted. Recent measurements have shown that nanotubes can have high conductivity based on ballistic transport. In addition, recent experimental programs have shown the ability to grow nanotubes at designated locations by using specialized seed sites. The ability to connect nanotubes from site to site has also been demonstrated. Although many important features of radical solutions to the interconnect problem have been realized, there is still much research to be done to make these approaches viable. There is also a critical need for truly creative approaches that will provide the defined roadmap capabilities while meeting the difficult challenges of cost and manufacturability.

The discussions above have described several *new concepts* for providing interconnect solutions compatible with the increasing requirements needed to continue the progression of IC technology. Although several independent approaches

are described, it is expected that the solutions used will be different for different applications, and that the ultimate solutions will require a combination of several approaches.

CROSSCUT ISSUES

In response to the magnitude and difficulty of solving the global interconnect problem, the interconnect community has begun not only a significant effort to push Cu-low κ to its limits, but also to explore radical alternatives that may require fundamental changes in design and packaging methodologies. At the same time, the design, packaging, and modeling and simulation communities have started significant efforts to alter their approaches to address the global interconnect problem. Possible solutions range from relatively minor modification of existing technology, to radical alternatives to existing methodologies. In this case it is critical that the entries in the ITRS technology requirements tables comprehend needs generated by advances in all areas. It is also critical that the design, packaging, and modeling and simulation communities are appraised of common needs envisioned by the interconnect community. The following paragraphs discuss some of these needs.

DESIGN

The most promising near-term solution (available in the next few years) anticipated for the global interconnect problem is design modifications to reduce the length of metal lines, combined with advances in Cu-low κ metallization. Continuous improvement in Cu-low κ performance is critical in order to maximize the size of circuit blocks that can be used without major design changes. Simple design solutions are currently being implemented in many companies. However, fundamental changes in design methodology, and solutions to difficult challenges in electronic design automation tools and techniques need to be researched and implemented to fully exploit the advantages available from design alternatives. Meeting the roadmap challenges and providing the time to implement further technology solutions requires changes.

Close coordination between design and interconnect technology teams is imperative to ensure correct resource investments in these areas. Specific needs of the interconnect community from the design community are modifications of design methodologies to compensate for the increasing importance of inductance and crosstalk, as well as increased power dissipation. Joule heating and current crowding in complex wiring systems must be carefully assessed as current densities rise. While selective use of repeaters can optimize critical speed paths, new design architectures are needed to mitigate global delay. Closer coupling between process capability, manufacturing variability, technology modeling, synthesis, physical design, and design verification will be required to meet the ITRS density, performance, and reliability challenges for interconnects. Design and interconnect must coordinate a critical review of the accuracy of needed interconnect technology parameters, as a function of technology nodes, in light of design advances. In addition, a close communication path to design must be established to assess the impact of interconnect technology advances and technology projections on predicted device performance, design, and layout. Refer to the *Design* chapter.

MODELING AND SIMULATION

Modeling and Simulation is a key resource for all of the technology areas working on the global interconnect problem. The modeling and simulation capabilities needed range from high level predictions of interconnect impact on IC layout and electrical behavior to prediction of physical structure of new low κ dielectrics and other more exotic interconnect materials. In all of these cases, modeling and simulation needs to provide sufficiently accurate predictions to eliminate the need (and cost) of running extensive experiments. These needs run from predictive capability within experimental error for relatively mature technology to accurate identification of restricted parameter ranges for experiments verifying that specific physical models provide reasonable representations of experimental results. The modeling and simulation needs in interconnect, as in many other technology areas, are becoming much more stringent because of the wider number of parameters that must be included. For example, the change to low κ dielectrics with low thermal conductivity have placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development. Specific interconnect needs from modeling and simulation are as follows: tools for interconnect performance prediction (including reliability and high frequency effects) for complex structures with hierarchical capability to trade speed and accuracy to meet specific applications; tools and methodology to connect product and process design in an integrated flow to meet target specifications or identify deficiencies; and materials modeling capability to predict structure, physical and electrical performance from atomic and molecular information. See the *Modeling and Simulation* chapter.

ASSEMBLY AND PACKAGING

Packages have traditionally been used to protect the IC chip from the environment, and to provide robust connections to the chip from the outside world. Recent moves to higher frequencies, higher power, lower power supply voltages, and larger pin count devices have caused packages to become a major factor in determining total device performance. These changes, compounded by the global interconnect problem, are forcing a broader view of packaging. This view has resulted in discussion of alternatives such as optimizing the package-chip system performance and allowing the package to be used as an intermediary in the transfer of signals from one part of the chip to another. Specific areas needing coordinated effort between packaging and interconnect include modeling and simulation capabilities that comprehend both package and on-chip interconnect for very high frequency and very high transient power signals. Such conditions ensure that changes in on-chip interconnect to Cu-low κ are not compatible with mechanical performance requirements in assembly and packaging, and developing innovative packaging structures and methodology that will assist in eliminating the global interconnect problem. Refer to the *Assembly and Packaging* chapter.

METROLOGY

Copper Damascene process technology continues in both research and development as the first low κ materials move into production. It is useful to note that although the goal of metrology is measurement of patterned wafers, most available methods are used on blanket wafers or test structures. Two new measurement needs have been added to the Interconnect Metrology roadmap— the measurement of voids in copper lines and the determination of pore size distribution in porous low κ materials.

The Interconnect Metrology section of the *Metrology* chapter describes the critical metrology challenges in more detail., such as measurement of complex material stacks and interfacial properties including physical and electrical properties, and determination of manufacturing metrology when device and interconnect technology remain undefined.

YIELD ENHANCEMENT

As the wiring density and number of interconnect levels increases, improvements in defect detection and reduction are required to maintain product yield. Real-time detection and analysis of defects is also required for yield improvement and process control to maintain factory product flow. Defects associated with high aspect ratio Damascene structures will be difficult to identify in patterned multi-layer low κ dielectrics. New techniques for defect detection and analysis, as well as improved defect reduction approaches, will be required to support future interconnect manufacturing processes (see *Yield Enhancement* chapter).

ENVIRONMENT, SAFETY, AND HEALTH

Interconnect technologies carry unique environmental, safety, and health (ESH) challenges (see Table 64). The performance-driven need for new materials (low κ dielectrics, high κ dielectrics, copper conductors and barriers, and others) and processes (electrochemical deposition, CVD metal/dielectric deposition, Cu/barrier CMP, low κ/high κ etch/clean, and others) brings numerous ESH concerns, especially considering the rapid pace of insertion. Continuous improvement is needed in methods for treating and recycling CMP slurries and copper electrochemical deposition baths. Both wet and dry processes will continue and require appropriate abatement; the introduction of new metal and dielectric materials adds to these ESH challenges. Closed-loop control and replenishment are potential solutions for wet processes. The new materials, precursors, and processes that will be required for future low κ dielectrics and CVD conductor/barrier depositions must also be carefully screened for ESH issues during the early phase of development. Reaction product emissions, health and safety properties, materials compatibility with equipment and other chemical components, flammability and reactivity must be predetermined to ameliorate ESH impact. The industry must also strive to reduce chemical emissions and waste (copper plating solutions, CMP slurries, acids/solvents, PFCs, water use) through process optimization, use of alternative chemistries, recycling, and/or abatement. (Refer to the *ESH* chapter.)

Table 64 Interconnect ESH Needs and Potential Solutions

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
Advanced metallization and dielectric materials	Utilize lowest ESH impact deposition processes Increased chemical utilization efficiency	Use lowest ESH impact solvents for spin-on processes Develop "zero waste" deposition methods Identify ESH issues with CVD precursors Develop safe precursor delivery systems Develop emissions models for vapor phase systems Utilize lowest ESH impact process chemistries for CVD Improve chemical utilization efficiency through endpoint detection and reactor design
Planarization	Lowest volume of chemicals and water used and disposed in CMP and post-CMP cleans processes Utilize lowest ESH impact chemistries for CMP and post-CMP cleans processes Low-energy and low-chemical consumption methods for removal of Cu from wastewater Water reclaim and reuse	Decrease amount of slurry required for CMP Develop slurry recycling methods Develop alternatives to slurry-based CMP processes Develop non-chemical consuming planarization methods Reduce water consumption Develop more efficient techniques for post-CMP rinsing Develop water recycling systems to reuse CMP and post-CMP wastewater Develop lowest ESH impact CMP and post CMP cleans chemistries
Electrochemical deposition of Cu	Reduce generation and handling of hazardous waste Lowest ESH impact process chemistries Reduce employee exposure to chemicals	Extend Cu plating bath life using monitoring and replenishment Develop techniques for bath recycle Minimize quantity of rinse water Develop and utilize lowest ESH impact plating chemistries Develop "zero waste" copper deposition processes Design process tools which minimize exposure to chemicals
Plasma processes	Lowest ESH impact process chemistries Reduce power consumption	Optimize chamber clean and etch processes to increase utilization efficiency of PFCs Develop low CoO abatement and recycle systems for PFCs Develop lowest ESH impact alternative etch chemistries and chamber cleaning processes that do not emit high global warming potential by-products (PFCs) Develop predictive plasma emissions models Monitor and optimize tool systems (energy-efficient pumps, idle energy usage, recycle waste heat) Reduce RF plasma energy consumption and develop alternate low-energy plasma generating systems Develop new heat transfer methodologies in vacuum systems

CONCLUSION

Managing the rapid rate of materials introduction and the concomitant complexity represents the overall interconnect challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. The delay associated with global wiring and the management of crosstalk and noise must be addressed with increased development activity. System-on-a-chip may alter the picture or technology timing because chip functionality can be traded for scaled density in the marketplace. Ultimately, interconnect innovation with optical, RF, or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.