# INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

## 2001 EDITION

# LITHOGRAPHY

## Table of Contents

**Scope** ........ 1
**Difficult Challenges** ........ 1
**Lithography Technology Requirements** ........ 3
**Potential Solutions** ........ 14
**Crosscut Needs and Potential Solutions** ........ 16
Environment, Safety, and Health ........ 16
Yield Enhancement ........ 16
Metrology ........ 16
Modeling & Simulation ........ 16

## List of Figures

Figure 34 Lithography Exposure Tool Potential Solutions ........ 15

## List of Tables

Table 56 Lithography Difficult Challenges ........ 2
Table 57a Lithography Technology Requirements—Near-term ........ 4
Table 57b Lithography Technology Requirements—Long-term ........ 5
Table 58a Resist Requirements—Near-term ........ 6
Table 58b Resist Requirements—Long Term ........ 6
Table 58c Resist Sensitivities ........ 6
Table 59a Optical Mask Requirements ........ 8
Table 59b EUVL Mask Requirements ........ 10
Table 59c EPL Mask Requirements ........ 12
Table 60 Lithography Modeling & Simulation Needs and Potential Solutions ........ 17

# LITHOGRAPHY

## SCOPE

In 2001 and beyond, lithographers are confronted with two sets of challenges. The first is a consequence of the difficulties inherent in extending optical methods of patterning to physical limits, while the second follows from the need to develop entirely new, post-optical lithographic technologies and implement them into manufacturing. Not only is it necessary to invent technical solutions to very challenging problems, it is critical that die costs not be increased because of the new methods. Each new generation of lithographic technology requires advances in all of the key elements of the following lithography infrastructure:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask making equipment, and materials
- Metrology equipment for critical dimension (CD) measurement, overlay control, and defect inspection

This chapter provides a 15-year roadmap defining lithography's difficult challenges, technology requirements, and potential solutions. Additionally, this chapter defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for Environment, Safety, and Health (ESH); Yield Enhancement; Metrology; and Modeling and Simulation.

Since the earliest days of the microelectronics industry, optical lithography has been the mainstream technology for volume manufacturing, and it is expected to continue as such through the 65 nm node, through the application of resolution enhancement techniques such as off-axis illumination (OAI), phase shifting masks (PSM) and optical proximity corrections (OPC). In addition to resolution enhancement techniques, wavelength reductions (248 nm→193 nm→157 nm) and lenses with increasing numerical apertures and decreasing aberrations will be required to extend the life of optical lithography.

The requirements of the 45 nm node and beyond are viewed as beyond the capabilities of optical lithography. Extension of the Roadmap will require the development of next-generation lithography (NGL) technologies, such extreme ultraviolet lithography (EUV) and electron projection lithography (EPL). Because next generation lithographies will require the development of substantially new infrastructure, the costs of these technologies will put great pressure on manufacturing costs.

## DIFFICULT CHALLENGES

The ten most difficult challenges to the continued shrinking of minimum feature sizes are shown in Table 56. Mask-making capability and cost escalation continue to be critical to future progress in lithography and will require continued focus. As a consequence of aggressive Roadmap acceleration—particularly the MPU gate linewidth (post etch), and increased mask error factors (MEFs) associated with low $\kappa_1$ lithography—mask linewidth control is falling behind the requirements of the chipmakers. For example, in the 1997 roadmap the 70nm node requirements showed 4× masks needing 9 nm of CD control for isolated lines and 14 nm for contacts. The current requirements are 3.4 nm for isolated lines and 4.3 nm for contacts assuming mask error factor (MEF) values of 1.4 and 3.0 respectively. Mask equipment and process capabilities are in place for manufacturing masks with complex Optical Proximity Corrections (OPC) and phase-shifting (PSM), while mask processes for post-193 nm technologies are in research and development. Mask damage from electrostatic discharge (ESD) has long been a concern, and it is expected to be even more problematic as mask feature sizes shrink. Furthermore, masks for 157 nm lithography will be kept in ambient atmospheres nearly free of water, so the risk of ESD damage to masks will increase. A cost-effective pellicle solution has not yet been identified for 157 nm masks, further complicating mask handling for lithography at that wavelength.

While lithography has long contributed significantly to over-all semiconductor manufacturing costs, there is even greater concern going forward regarding cost control and return-on-investment (ROI). Because lithography tool throughput is reduced with larger wafers, the fraction of total wafer costs resulting from lithography may increase from the transition to 300 mm wafers. These issues of masks and lithography costs are relevant to optical, as well as next-generation

lithography. To be extended further, optical lithography will require new resists that will provide both good pattern fidelity when exposed with short wavelengths (193 nm and 157 nm), and improved performance during etch. New optical materials for lenses, such as $CaF_2$, will also be needed, beginning with 193 nm (ArF) lithography. Inadequacies in performance and supply in resists and $CaF_2$ have already led to a slowdown in the pace of advances in lithography.

Process control, particularly for overlay and linewidths, also represents a major challenge. It is unclear whether metrology, which is fundamental to process control, will be adequate to meet future requirements as needed for both development and volume manufacturing. Resist line edge roughness (LER) is becoming significant, as gate linewidth control becomes comparable to the size of a polymer unit. Next-generation lithography will require careful attention to details as the exposure tools are based upon approaches that have never been used before in manufacturing. These tools must be developed and proven to be capable of meeting the reliability and utilization requirements of cost-effective manufacturing.

*Table 56 Lithography Difficult Challenges*

| *Five Difficult Challenges ≥ 65 nm Through 2007* | *Summary of Issues* |
|---|---|
| Optical mask fabrication with resolution enhancement techniques for ≤ 90 nm and development of post-optical mask fabrication | Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as registration, CD control, defectivity, and 157 nm films; defect free multi-layer substrates or membranes)<br>Development of equipment infrastructure (writers, inspection, repair, metrology) for a relatively small market |
| Cost control and ROI | Achieving constant/improved ratio of tool cost to throughput over time<br>Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, such as low-cost masks<br>Achieving ROI for all segments of the industry (chipmakers, equipment and material suppliers, and infrastructure) with sufficient lifetimes for the technologies, especially single node solutions at 90 nm and below |
| Process control | Development of processes to control gate linewidths to nearly 3 nm, 3 sigma<br>Development of new and improved alignment and overlay control methods independent of technology option for < 25 nm overlay |
| Resists for ArF and $F_2$ | Outgassing, LER, SEM-induced CD changes, etch resistance, and defects as small as 40 nm |
| $CaF_2$ | Yield, cost, quality |
| *Five Difficult Challenges < 65 nm Beyond 2007* | |
| Mask fabrication and process control | Development of commercial mask manufacturing processes to meet requirements of Roadmap options (defect-free NGL masks, such as EUV multi-layer masks or EPL membranes and stencil masks)<br>Development of equipment infrastructure (writers, inspection of substrates, blanks and patterned masks, repair, metrology) for a relatively small market<br>Development of mask process control methods to achieve critical dimensions, image placement, and defect density control below the 65 nm node |
| Metrology and defect inspection | Capability for measuring critical dimensions down to 9 nm and metrology for overlay down to 9 nm, and patterned wafer defect inspection for defects < 40 nm |
| Cost control and ROI | Achieving constant/improved ratio of tool cost to throughput over time<br>Development of cost-effective post-optical masks including an affordable ASIC solution, such as low-cost masks<br>Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) with sufficient lifetimes for the technologies, especially single node solutions at 45 nm and below |
| Gate CD control improvements; process control; resist materials | Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness<br>Development of new and improved alignment and overlay control methods independent of technology option to < 9 nm overlay |
| Tools for mass production | Post optical exposure tools capable of meeting requirements of the Roadmap |

## LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Table 57a and b)
- Resist Requirements (Table 58a, b, and c)
- Mask Requirements (Table 59a, b, and c)

Because of the relative immaturity of new lithography technologies—ArF, $F_2$, and NGL—and the need for additional development, the pace at which half-pitch will shrink is expect to return to a 50% reduction every three years. Because of the particular challenges associated with imaging contact holes, contact hole size after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gates. This is important to comprehend in the Roadmap, because contacts have very small process windows and large mask error factors, and minor changes in the contact size have large implications for mask CD control requirements. Small MPU gates after etch are pursued aggressively and create significant challenges for metrology and process control.

Photoresists need to be developed that provide good pattern fidelity, good linewidth control, and low defects at several new wavelengths. Each of the 130 nm, 90 nm and 65 nm nodes could involve the introduction of a new wavelength or non-optical lithography, so each node will require the development of an entirely new resist platform. As feature sizes get smaller, defects and polymers will have comparable dimensions with implications for filtering of resists.

The masks for all next-generation lithographies are radically different from optical masks, and no NGL technology can support a pellicle. Because the requirements for NGL masks are substantially different than those for optical lithography, separate tables have been included for Optical, EUV, and EPL masks (Table 59a, b, and c, respectively). These masks have tight requirements for linewidth control and registration, because they will be applied at the 65 nm and beyond. EUV masks must also have very tight flatness control, and there are additional requirements for various parameters associated with reflectivity of EUV masks. EPL masks are comprised of thin membranes, and have special requirements. NGL masks, being different in form from optical masks, will also require the development of new defect inspection capabilities. Solutions for protecting the masks from defects added during storage, handling and use in the exposure tool need to be developed and tested, because there are no known pellicle options for NGL masks. These very different NGL mask requirements can be expected to exacerbate, rather than relieve, the high costs associated with masks that are already being encountered with optical masks.

*Table 57a Lithography Technology Requirements—Near-term*

| YEAR OF PRODUCTION | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 |
|---|---|---|---|---|---|---|---|
| *DRAM* | | | | | | | |
| *DRAM ½ Pitch (nm)* | 130 | 115 | 100 | 90 | 80 | 70 | 65 |
| *Contact in resist (nm)* | 165 | 140 | 130 | 110 | 100 | 90 | 80 |
| *Contact after etch (nm)* | 150 | 130 | 115 | 100 | 90 | 80 | 70 |
| *Overlay* | 46 | 40 | 35 | 32 | 28 | 25 | 23 |
| *CD control (3 sigma) (nm)* | 15.9 | 14.1 | 12.2 | 11.0 | 9.8 | 8.6 | 8.0 |
| *MPU* | | | | | | | |
| *MPU ½ Pitch (nm)* | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| *MPU gate in resist (nm)* | 90 | 70 | 65 | 53 | 45 | 40 | 35 |
| *MPU gate length after etch (nm)* | 65 | 53 | 45 | 37 | 32 | 28 | 25 |
| *Contact in resist (nm)* | 165 | 140 | 122 | 100 | 90 | 80 | 75 |
| *Contact after etch (nm)* | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| *Gate CD control (3 sigma) (nm)* | 5.3 | 4.3 | 3.7 | 3.0 | 2.6 | 2.4 | 2.0 |
| *ASIC/LP* | | | | | | | |
| *ASIC/LP ½ Pitch (nm)* | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| *ASIC/LP gate in resist (nm)* | 130 | 107 | 90 | 75 | 65 | 53 | 45 |
| *ASIC/LP gate length after etch (nm)* | 90 | 80 | 65 | 53 | 45 | 37 | 32 |
| *Contact in resist (nm)* | 165 | 140 | 122 | 100 | 90 | 80 | 75 |
| *Contact after etch (nm)* | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| *CD control (3 sigma) (nm)* | 7.3 | 6.5 | 5.3 | 4.3 | 3.7 | 3.0 | 2.6 |
| *Chip size ($mm^2$)* | | | | | | | |
| *DRAM, introduction* | 390 | 308 | 364 | 287 | 454 | 359 | 568 |
| *DRAM, production* | 127 | 100 | 118 | 93 | 147 | 116 | 183 |
| *MPU, high volume at introduction* | 280 | 280 | 280 | 280 | 280 | 280 | 280 |
| *MPU, high volume at production* | 140 | 140 | 140 | 140 | 140 | 140 | 140 |
| *MPU, high performance* | 310 | 310 | 310 | 310 | 310 | 310 | 310 |
| *ASIC* | 800 | 800 | 572 | 572 | 572 | 572 | 572 |
| *Minimum field area* | 800 | 800 | 572 | 572 | 572 | 572 | 572 |
| *Wafer size (diameter, mm)* | 300 | 300 | 300 | 300 | 300 | 300 | 300 |

*White–Manufacturable Solutions Exist, and Are Being Optimized*

*Yellow--Manufacturable Solutions are Known*

*Red–Manufacturable Solutions are NOT Known*

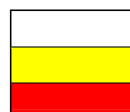


*Table 57b Lithography Technology Requirements—Long-term*

| YEAR OF PRODUCTION | 2010 | 2013 | 2016 |
|---|---|---|---|
| DRAM | | | |
| DRAM ½ Pitch (nm) | 45 | 32 | 22 |
| Contact in resist (nm) | 55 | 40 | 30 |
| Contact after etch (m) | 50 | 35 | 25 |
| Overlay | 18 | 13 | 9 |
| CD control (3 sigma) (nm) | 5.5 | 3.9 | 2.7 |
| MPU | | | |
| MPU ½ Pitch (nm) | 45 | 32 | 22 |
| MPU gate in resist (nm) | 25 | 18 | 13 |
| MPU gate length after etch (nm) | 18 | 13 | 9 |
| Contact in resist (nm) | 50 | 37 | 27 |
| Contact after etch (nm) | 45 | 32 | 22 |
| CD control (3 sigma) (nm) | 1.5 | 1.1 | 0.7 |
| ASIC/LP | | | |
| ASIC/LP ½ Pitch (nm) | 45 | 32 | 22 |
| ASIC/LP gate in resist (nm) | 32 | 22 | 16 |
| ASIC/LP gate length after etch (nm) | 22 | 16 | 11 |
| Contact in resist (nm) | 50 | 37 | 27 |
| Contact after etch (nm) | 45 | 32 | 22 |
| CD control (3 sigma) (nm) | 1.8 | 1.3 | 0.9 |
| Chip size ($mm^2$) | | | |
| DRAM, introduction | 563 | 373 | 186 |
| DRAM, production | 181 | 239 | 238 |
| MPU, high volume at introduction | 280 | 280 | 280 |
| MPU, high volume at production | 140 | 140 | 140 |
| MPU, high performance | 310 | 310 | 310 |
| ASIC | 572 | 572 | 572 |
| Minimum field area | 572 | 572 | 572 |
| Wafer size (diameter, mm) | 300 | 450 | 450 |

*Note: The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one year earlier. Development capability must be available 2–3 years earlier.*

*White–Manufacturable Solutions Exist, and Are Being Optimized*

*Yellow--Manufacturable Solutions are Known*

*Red–Manufacturable Solutions are NOT Known*

*Notes for Table 57a and b*

*[1] The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists, and masks for manufacturing must be available one year earlier. Development capability must be available two–three years earlier.*

*[ 2] Linewidth variations are based on linewidth deviations from target dimensions for all critical features for a given product. For example, for microprocessors these would be the gate features critical to circuit performance. This total linewidth variation includes contributions from errors within each exposure field for features of various orientations and with varying pitch. Variations also include contributions from linewidth changes across individual wafers and from wafer-to-wafer. The variances of the final dimensions after etch are assumed to result 2/3 from variance of the linewidths in resist and 1/3 from the etch process. It is assumed that the allowable variations in linewidth are +/-15% of the final, etch feature size for DRAMs and ASICS and +/-10% for MPUs..*

*Table 58a Resist Requirements—Near-term*

| Year of Production | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm)* | 130 | 115 | 100 | 90 | 80 | 70 | 65 |
| *MPU / ASIC ½ Pitch (nm)* | 150 | 130 | 107 | 90 | 80 | 70 | 65 |
| *MPU Printed Gate Length (nm)* | 90 | 75 | 65 | 53 | 45 | 40 | 35 |
| *MPU Physical Gate Length (nm)* | 65 | 53 | 45 | 37 | 32 | 28 | 25 |
| *Resist Characteristics ** | | | | | | | |
| Resist meets requirements for resolution and CD Control (nm, 3 sigma) ** | **7** | **6** | **5** | **5** | **4** | **4** | **3** |
| Resist thickness (nm, imaging layer) *** | **300–450** | **250–400** | **200–400** | **170–320** | **150–280** | **140–250** | **140–220** |
| Ultra thin resist thickness (nm)**** | **x** | **x** | **130–200** | **100–150** | **100–150** | **100–150** | **100–150** |
| PEB temperature sensitivity (nm/C) | **4** | **3** | **2.5** | **2** | **2** | **1.5** | **1.5** |
| Backside particles (particles/m$^2$ at critical size, nm) | **2500 @ 200** | **2000 @ 200** | **2000 @ 150** | **2000 @ 150** | **1500 @ 100** | **1500 @ 100** | **1500 @ 100** |
| Defects in spin-coated resist films† #/cm$^2$ (size in nm) | **0.02<br>70** | **0.02<br>65** | **0.02<br>60** | **0.01<br>55** | **0.01<br>50** | **0.01<br>45** | **0.01<br>40** |
| Defects in patterned resist films, gates, contacts, etc. #/cm$^2$ (size in nm) | **0.08<br>70** | **0.07<br>65** | **0.07<br>60** | **0.06<br>55** | **0.05<br>50** | **0.04<br>45** | **0.04<br>40** |
| Line Edge Roughness (nm, 3 sigma) <5% of CD, 3 sigma, single side | **7** | **6** | **5** | **4** | **4** | **3** | **3** |

*Table 58b Resist Requirements—Long Term*

| Year of Production | 2010 | 2013 | 2016 |
|---|---|---|---|
| *DRAM ½ Pitch (nm)* | 45 | 32 | 22 |
| *MPU / ASIC ½ Pitch (nm)* | 50 | 35 | 25 |
| *MPU Printed Gate Length (nm)* | 25 | 18 | 13 |
| *MPU Physical Gate Length (nm)* | 18 | 13 | 9 |
| *Resist Characteristics ** | | | |
| Resist meets requirements for resolution and CD Control (nm, 3 sigma) ** | **2** | **1** | **1** |
| Resist thickness (nm, imaging layer) *** | **120–160** | **80–140** | **50–80** |
| Ultra thin resist thickness (nm)*** | **80–120** | **60–100** | **40–60** |
| PEB temperature sensitivity (nm/C) | **1.5** | **1** | **1** |
| Backside particles (particles/m$^2$ at critical size, nm) | **1000 @ 50** | **1000 @ 50** | **500 @ 50** |
| Defects in spin-coated resist films #/cm$^2$ (size in nm) | **0.01<br>30** | **0.01<br>20** | **0.01<br>10** |
| Defects in patterned resist films for gates, contacts, etc. #/cm$^2$ (size in nm) | **0.03<br>30** | **0.01<br>20** | **0.01<br>10** |
| Line Edge Roughness (nm, 3 sigma) <5% of CD, 3 sigma, single side | **2** | **1** | **1** |

*White–Manufacturable Solutions Exist, and Are Being Optimized*
*Yellow--Manufacturable Solutions are Known*
*Red–Manufacturable Solutions are NOT Known*

*Table 58c Resist Sensitivities*

| Exposure Technology | Sensitivity |
|---|---|
| *248nm* | **20–50 mJ/ cm$^2$** |
| *193nm* | **10–40 mJ/ cm$^2$** |
| *157nm* | **2–20 mJ/ cm$^2$** |
| *X-ray @ 1nm* | **50–100 mJ/ cm$^2$** |
| *Extreme Ultraviolet @ 13.5nm* | **2–25 mJ/ cm$^2$** |
| *Electron Beam Projection @ 100kV ******* | **2–10 uC/ cm$^2$** |
| *E-beam Direct Write @ 50kV ******* | **5–10 uC/ cm$^2$** |
| *Ion Beam Projection* | **0.2–2.0 uC/ cm$^2$** |

****** Linked with resolution*

*Notes for Table 58a and b:*

*Exposure Dependent Requirements*

* *Resist sensitivity is treated separately in the second resist sensitivities table (separate sheet).*

** *Indicates whether the resist has sufficient resolution, CD control, and profile to meet the device resolution and CD control values.*

*** *Resist thickness is determined by the aspect ratio range of 3:1 to 4:1, limited by pattern collapse.*

**** Upper thickness limit for ultrathin resist (UTR) is determined by the opacity to the incident radiation from the *exposure tool*

***** *Linked with resolution*

*† Defects in coated films are those detectable as physical objects, such as pinholes, that may be distinguished from the resist film by optical detection methods.*

*Other requirements:*

*A. Need for a positive tone resist and a negative tone resist will depend upon critical feature type and density.*

*B. Feature wall profile should be 90 ± 2 degrees.*

*C. Thermal stability should be ≥ 130°C.*

*D. Etching selectivity should be > that of poly hydroxystyrene (PHOST).*

*E. Upon removal by stripping there should be no detectible residues.*

*F. Sensitive to basic airborne compounds such as amines and amides. Clean handling space should have <1000 pptM of these materials.*

*G. Metal contaminants < 5 ppb.*

*H. Organic material outgassing (molecules/cm$^2$-sec) while in the 157nm lithography tool(under the lens) for 2 minutes<1e12. Values for electron projection and EUV lithographies are being determined and a preliminary estimate for EUV is <1e15.*

*I. Si species outgassing (molecules/cm$^2$-sec) while in the 157 nm lithography tool for 2 minutes <1e8. Values for electron projection and EUV lithographies are being determined.*

*Table 59a Optical Mask Requirements*

| YEAR OF PRODUCTION | 2001 130nm | 2002 115nm | 2003 100nm | 2004 90nm | | 2005 80nm | | 2006 70nm | | 2007 65nm | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Wafer minimum half pitch (nm) [A] | 130 | 115 | 100 | 90 | 90 | 80 | 80 | 70 | 70 | 65 | 65 |
| Wafer minimum line (nm, in resist) | 90 | 75 | 65 | 53 | 53 | 45 | 45 | 40 | 40 | 35 | 35 |
| Wafer minimum line (nm, Post Etch) | 65 | 53 | 45 | 37 | 37 | 32 | 32 | 30 | 30 | 25 | 25 |
| Overlay | 45 | 40 | 35 | 32 | 32 | 28 | 28 | 25 | 25 | 23 | 23 |
| Wafer minimum contact hole (nm, Post Etch) [A] | 150 | 130 | 115 | 100 | 100 | 90 | 90 | 80 | 80 | 70 | 70 |
| Magnification [B] | 4 | 4 | 4 | 4 | 5 | 4 | 5 | 4 | 5 | 4 | 5 |
| Mask minimum image size (nm) [C] | 360 | 300 | 260 | 212 | 265 | 180 | 225 | 160 | 200 | 140 | 175 |
| Mask OPC feature size (nm) Clear [D] | 260 | 230 | 200 | 180 | 225 | 160 | 200 | 140 | 175 | 130 | 163 |
| Mask OPC feature size (nm) Opaque [D] | 180 | 150 | 130 | 106 | 133 | 90 | 113 | 80 | 100 | 70 | 88 |
| Image placement (nm, multi-point) [E] | 27 | 24 | 21 | 19 | 24 | 17 | 21 | 15 | 19 | 14 | 17 |
| CD uniformity (nm, 3 sigma) [F] @ | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 |
| Isolated lines (MPU gates) Binary | 7.4 | 6.1 | 5.1 | 4.2 | 5.3 | 3.7 | 4.6 | 3.4 | 4.3 | 2.5 | 3.1 |
| Isolated lines (MPU gates) ALT | 10.4 | 8.5 | 7.2 | 5.9 | 7.4 | 5.1 | 6.4 | 4.8 | 6.0 | 4.0 | 5.0 |
| Dense lines DRAM half pitch) | 10.4 | 9.2 | 8.0 | 7.2 | 9.0 | 6.4 | 8.0 | 5.6 | 7.0 | 4.2 | 5.2 |
| Contact/vias | 8.0 | 6.9 | 6.1 | 5.3 | 6.7 | 4.8 | 6.0 | 4.3 | 5.3 | 3.2 | 4.0 |
| Linearity (nm) [G] | 19.8 | 17.5 | 15.2 | 13.7 | 17.1 | 12.2 | 15.2 | 10.6 | 13.3 | 9.9 | 12.4 |
| CD mean to target (nm) [H] | 10.4 | 9.2 | 8.0 | 7.2 | 9.0 | 6.4 | 8.0 | 5.6 | 7.0 | 5.2 | 6.5 |
| Defect size (nm) [I] * | 104 | 92 | 80 | 72 | 90 | 64 | 80 | 56 | 70 | 52 | 65 |
| Substrate form factor | 152 x 152 x 6.35 mm | | | | | | | | | | |
| Blank Flatness (nm) | 250 | 250 | 200 | 180 | 280 | 160 | 250 | 140 | 220 | 130 | 200 |
| Transmission uniformity to mask(pellicle and clear feature) (+-% 3sigma) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Data volume (GB) [J] | 64 | 96 | 144 | 216 | 216 | 324 | 324 | 486 | 486 | 729 | 729 |
| Mask design grid (nm) [K] | 8 | 8 | 4 | 4 | 5 | 4 | 5 | 4 | 5 | 4 | 5 |
| Attenuated PSM transmission mean deviation from target (+/- % of target) [L] | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 | 4 | 4 |
| Attenuated PSM transmission uniformity (+/-% of target) [M] | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Attenuated PSM phase mean deviation from 180o (+/- degree) | 4 | 4 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Alternating PSM phase mean deviation from 180o (+/- degree) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 |
| Alternating PSM phase uniformity (+/- degree) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 |
| Mask materials and substrates | Absorber on fused silica, except for 157nm optical which will be absorber on modified fused silica square with pellicles *157nm has no known cost-effective pellicle solution* | | | | | | | | | | |
| (Exposure tool dependent) | Primary PSM choices are attenuated shifter and alternating aperture | | | | | | | | | | |

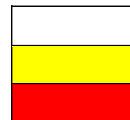
*The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.*

**180 degree phase defects are 70% of number shown*

*White–Manufacturable Solutions Exist, and Are Being Optimized*

*Yellow–Manufacturable Solutions are Known*

*Red–Manufacturable Solutions are NOT Known*



*Notes for Table 59a—Optical Mask requirements*

[A] *Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)*

[B] *Magnification—Lithography tool reduction ratio, N:1*

[C] *Mask Minimum Image Size—The nominal mask size of the smallest primary feature to be transferred to the wafer (Commonly equivalent to wafer minimum feature size times the reduction ratio.)*

[D] *Mask OPC Feature Size—The minimum width of isolated non-printing features on the mask.*

[E] *Image Placement—The maximum component deviation (x or y) of the array of the images centerline relative to a defined reference grid.*

[F] *CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the Mask Feature. For table simplicity the roadmap numbers normalize back to one dimension.* $\sqrt{AREA} - \sqrt{TARGET\ AREA}$

[G] *Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than half the primary feature size and less than five times the primary feature size.*

[H] *CD Mean to Target—The maximum difference between the average of the measured feature sizes and the intended feature size (design size). Applies to a single feature size and tone.* $\Sigma(Actual\text{-}Target)/Number\ of\ measurements$.

[I] *Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The Mask Defect Size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.*

[J] *Date Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.*

[K] *Mask Design Grid—Wafer design grid times the mask magnification.*

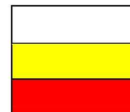
[L] *Transmission—Ratio of the fraction of light passing through an attenuated PSM layer and the mask blank with no opaque films expressed in a percent.*

[M] *Phase—Change in optical path length between two regions on the mask expressed in degrees.*

*Table 59b EUVL Mask Requirements*

| YEAR OF PRODUCTION | 2006<br>70nm | 2007<br>65nm | 2010<br>45nm | 2013<br>32nm | 2016<br>22nm |
|---|---|---|---|---|---|
| Wafer minimum half pitch (nm) [A] | 70 | 65 | 45 | 32 | 22 |
| Wafer minimum line (nm, in resist) | 40 | 35 | 25 | 18 | 13 |
| Wafer minimum line (nm, Post Etch) | 30 | 25 | 18 | 13 | 9 |
| Overlay | 25 | 23 | 18 | 13 | 9 |
| Wafer minimum contact hole (nm, after etch) | 80 | 70 | 50 | 35 | 25 |
| *Generic Mask Requirements* | | | | | |
| Magnification [B] | 4 | 4 | 4 | 4 | 4 |
| Mask minimum image size (nm) [C] | 160 | 140 | 100 | 72 | 52 |
| Image placement (nm, multi-point) [D] | 15 | 14 | 11 | 8 | 6 |
| *CD Uniformity (nm, 3 sigma) [E]* | | | | | |
| Isolated lines (MPU gates) | 4.5 | 4 | 2.5 | 2 | 1 |
| Dense lines DRAM (half pitch) | 11 | 10 | 7 | 5 | 3.5 |
| Contact/vias | 12.5 | 11 | 8 | 5.5 | 4 |
| Linearity (nm) [F] | 11 | 10 | 7 | 5 | 3.5 |
| CD mean to target (nm) [G] | 5.5 | 5 | 3.5 | 2.5 | 1.5 |
| Defect size (nm) [H] | 55 | 50 | 35 | 25 | 15 |
| Data volume (GB) [I] | 324 | 486 | 1644 | 5550 | 18736 |
| Mask design grid (nm) [J] | 4 | 4 | 4 | 4 | 4 |
| *EUVL-specific Mask Requirements* | | | | | |
| Substrate defect size (nm) [K] | 39 | 37 | 32 | 27 | 23 |
| Mean peak reflectivity | 65% | 65% | 66% | 67% | 67% |
| Relative reflectivity uniformity of the mask (% 3sigma) [L] | 1.5% | 1.3% | 0.9% | 0.7% | 0.5% |
| Peak reflectivity uniformity (% 3sigma absolute) | 0.69% | 0.61% | 0.42% | 0.33% | 0.24% |
| Reflected centroid wavelength uniformity (nm 3sigma) [M] | 0.06 | 0.05 | 0.05 | 0.04 | 0.03 |
| Minimum absorber sidewall angle (degrees) | 85 | 85 | 85 | 85 | 85 |
| Absorber sidewall angle tolerance (± degrees) | 1 | 1 | 0.75 | 0.5 | 0.5 |
| Absorber LER (3sigma nm) [N] | 5 | 4 | 3 | 3 | 3 |
| Mask substrate flatness (nm peak-to-valley) [O] | 80 | 75 | 50 | 45 | 30 |
| Maximum aspect ratio of absorber stack | 1 | 1.1 | 1.3 | 1.5 | 1.7 |
| Substrate form factor | 152 × 152 × 6.35 mm | | | | |
| Strategy for protecting mask from defects | Removable pellicle and thermophoresis during exposure | | | | |

*White–Manufacturable Solutions Exist, and Are Being Optimized*
*Yellow--Manufacturable Solutions are Known*
*Red–Manufacturable Solutions are NOT Known*



*Notes for Table 59b—EUV Mask requirements:*

*EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.*

*[A] Wafer Minimum Feature Size-Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)*

*[B] Magnification-Lithography tool reduction ratio, N:1*

*[C] Mask Minimum Image Size-The nominal mask size of the smallest primary feature to be transferred to the wafer (Commonly equivalent to wafer minimum feature size times the reduction ratio.)*

*[D] Image Placement-The maximum component deviation (x or y) of the array of the images centerline relative to a defined reference grid.*

*[E] CD Uniformity-The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the Mask Feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt(AREA) - sqrt(TARGET AREA)*

*[F] Linearity-Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than half the primary feature size and less than five times the primary feature size*

*[G] CD Mean to Target-The maximum difference between the average of the measured feature sizes and the intended feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.*

*[H] Defect Size-A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The Mask Defect Size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.*

*[I] Date Volume-This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.*

*[J] Mask Design Grid-Wafer design grid times the mask magnification.*

*[K] Substrate Defect Size-the minimum diameter spherical defect on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.*

*[L] Relative reflectivity uniformity includes errors in effective reflectivity due to peak reflectivity uniformity, centroid wavelength uniformity, and centered wavelength accuracy.*

*[M] Includes variation in centroid wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.*

*[N] Line edge roughness (LER) is defined a roughness 3sigma one-sided for spatial period < minimum linewidth*

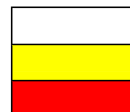
*[O] Mask Substrate Flatness-Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge and or bow that are compensable by the mask mounting and leveling method in the exposure tool.*

*Table 59c EPL Mask Requirements*

| *Year of Production* | *2006*<br>*70nm* | *2007*<br>*65nm* | *2010*<br>*45nm* | *2013*<br>*32nm* | *2016*<br>*22nm* |
|---|---|---|---|---|---|
| Wafer minimum half pitch (nm) [A] | **70** | **65** | **45** | **32** | **22** |
| Wafer minimum line (nm, in resist) | **40** | **35** | **25** | **18** | **13** |
| Wafer minimum line (nm, Post Etch) | **30** | **25** | **18** | **13** | **9** |
| Overlay | **25** | **23** | **18** | **13** | **9** |
| Wafer minimum contact hole (nm, after etch) | **80** | **70** | **50** | **35** | **25** |
| Magnification [B] | **4** | **4** | **4** | **4** | **4** |
| Mask minimum image size (nm) [C] | **112** | **98** | **70** | **50** | **36** |
| Non-linear image placement error in sub-field (nm, multi-point) [D] | **11** | **10** | **7** | **5** | **3** |
| *Generic mask requirements* | | | | | |
| Isolated lines (MPU gates) [E] | **4.5** | **4** | **2.5** | **2** | **1** |
| Dense lines DRAM half pitch) [E] | **11.5** | **10.5** | **7.5** | **5** | **3.5** |
| Contact/vias [E] | **13** | **11.5** | **8** | **5.5** | **4** |
| Linearity (nm) [F] | **11** | **10** | **7** | **5** | **3.5** |
| CD mean to target (nm) [G] | **6** | **5.5** | **4** | **2.5** | **1.5** |
| Pattern corner rounding (nm) | **45** | **40** | **28** | **18** | **15** |
| Defect size (nm) [H] | **55** | **50** | **35** | **25** | **15** |
| Data volume (GB) [I] | **324** | **486** | **1644** | **5550** | **18736** |
| Mask design grid (nm) [J] | 4 | **4** | **4** | **4** | **4** |
| *EPL-specific mask requirements* | | | | | |

| *Mask type* | ***Membrane [N]*** | ***Stencil [O]*** | ***Membrane*** | ***Stencil*** | ***Membrane*** | ***Stencil*** | ***Membrane*** | ***Stencil*** | ***Membrane*** | ***Stencil*** |
|---|---|---|---|---|---|---|---|---|---|---|
| Clear area transmission factor [K] | **50%** | **100%** | **50%** | **100%** | **50%** | **100%** | **70%** | **100%** | **70%** | **100%** |
| Membrane thickness uniformity (3 sigma %) [L] | **1.0%** | **N/A** | **1.0%** | **N/A** | **1.0%** | **N/A** | **1.0%** | **N/A** | **1.0%** | **N/A** |
| Pattern sidewall angle (degrees) | **90** | **90** | **90** | **90** | **90** | **90** | **90** | **90** | **90** | **90** |
| Pattern sidewall angle tolerance (+ degrees) | **0.2** | | **0.2** | | **0.2** | | **0.2** | | **0.2** | |
| Scatterer/stencil LER ( 3sigma nm) [M] | **5** | | **4** | | **3** | | **3** | | **3** | |
| Mask substrate flatness (micron peak-to-valley) | **10** | | **10** | | **5** | | **5** | | **4** | |
| Mask flatness within a sub-field (micron peak-to-valley) | **1** | | **1** | | **1** | | **1** | | **1** | |
| Maximum mask resistivity (ohm-cm) | **20** | | | | | | | | | |
| Substrate form factor | **200 mm diameter, 0.725 mm thick** | | | | | | | | | |
| Strategy for protecting mask from defects | **Periodic inspection and cleaning as needed** | | | | | | | | | |

*White–Manufacturable Solutions Exist, and Are Being Optimized*
*Yellow--Manufacturable Solutions are Known*
*Red–Manufacturable Solutions are NOT Known*



*Notes for Table 59c—EPL Mask requirements*

*EPL masks have hundreds of subfields (~1 by 1 mm), and each subfield corresponds to a membrane surrounded by Si struts*
*[A] Wafer Minimum Feature Size-Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)*
*[B] Magnification-Lithography tool reduction ratio, N:1*
*[C] Mask Minimum Image Size—The nominal mask size of the smallest primary feature to be transferred to the wafer (Commonly equivalent to wafer minimum feature size times the reduction ratio.)*
*[D] Nonlinear image placement error in sub-field-The three sigma non-linear deviation (x or y) of the images in a sub field relative to a defined reference grid. Please note that a sub field is 1mm X 1mm on the mask. The non-linear error component can be obtained by calculation.*
*[E] CD Uniformity-The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the Mask Feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt(AREA) - sqrt(TARGET AREA)*
*[F] Linearity-Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than half the primary feature size and less than five times the primary feature size*
*[G] CD Mean to Target-The maximum difference between the average of the measured feature sizes and the intended feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.*
*[H] Defect Size-A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The Mask Defect Size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.*
*[I] Date Volume-This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.*
*[J] Mask Design Grid-Wafer design grid times the mask magnification.*
*[K] Percentage of current incident on a clear area on the mask relative to that arriving at wafer through the axial back focal plane aperture of the projection optics of the exposure tool (for NA of 6 - 8 mRAD)*
*[L] Membrane Thickness Uniformity - The three sigma variation of membrane thickness over a subfield. Note that a subfield is a 1x1 mm area.*
*[M] Line edge roughness (LER) is defined a roughness 3sigma one-sided for spatial period < minimum linewidth*
*[N] Membrane masks have patterned scattering layers on each membrane.*
*[O] Stencil masks have patterns etched through the membranes in each subfield*

## POTENTIAL SOLUTIONS

The lithography potential solutions are presented in Figure 34. Optical lithography is the mainstream approach through the 90 nm node, with NGL possibly appearing by the 65 nm node. For critical layer imaging, optical lithography is represented by three wavelengths—248 nm, 193 nm, and 157 nm. Currently, only 248 nm lithography has a mature infrastructure. Significant improvements in 193 nm resists and $CaF_2$ are needed for mainstream application of 193 nm lithography, and 157 nm lithography is still in early development.

The post-optical or next-generation lithography (NGL) alternatives are all candidates at and below 65 nm. Of the possible NGL technologies, multiple regions consider EUV, EPL, and maskless (ML2) lithography as potential successors to optical lithography. There are activities taking place in other lithographic technologies, such as ion projection lithography (IPL), proximity x-ray lithography (PXL), and proximity electron lithography (PEL), but these activities are confined largely to single regions.

Although many technology approaches exist, the industry is limited in its ability to fund the development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions among government, industry, and universities are absolutely necessary to narrow the options for these future generations.

The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities that are necessary for continued adherence to Moore's Law. This shift will drive major changes throughout the lithography infrastructure and require significant resources for commercialization. These development costs must necessarily be recovered in the costs of exposure tools, masks, and materials.

Direct write lithography has been applied to niche applications in development and low volume ASIC production, but could expand its role. Breakthroughs in direct-write technologies that achieve high throughput will be a significant paradigm shift. It will eliminate the need for masks, offering inherent cost and cycle-time reduction. Other technologies that eliminate the need for masks and resist would likewise constitute a paradigm shift. Maskless lithography (ML2) is currently in the research phase, and many significant technological hurdles will need to be overcome for ML2 to be viable for cost-effective semiconductor manufacturing.

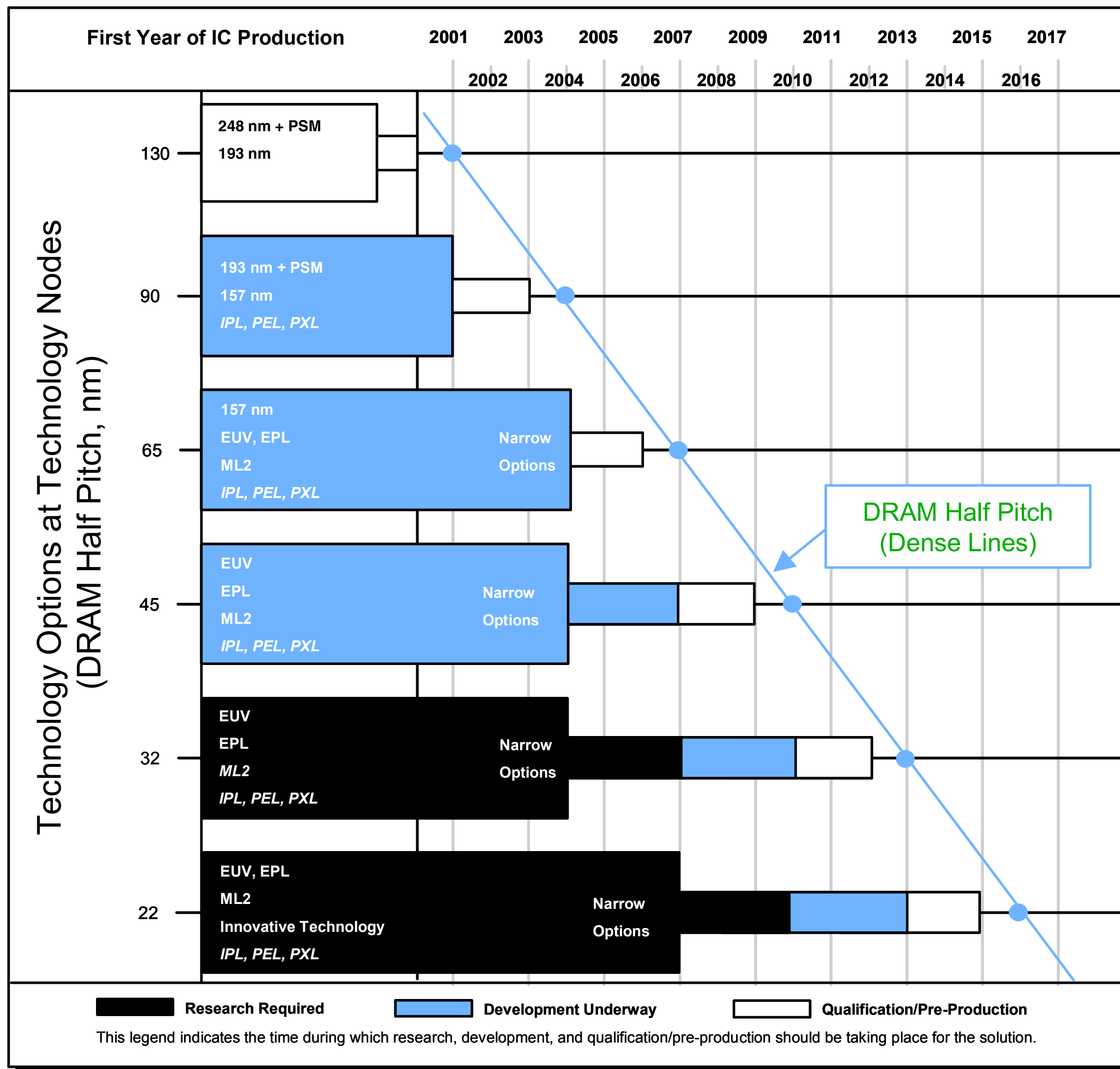



*Figure 34 Lithography Exposure Tool Potential Solutions*

*Technologies shown in italics have only single region support.*

*EUV—extreme ultraviolet*

*EPL—electron projection lithography*

*ML2—maskless lithography*

*IPL—ion projection lithography*

*PXL—proximity x-ray lithography*

*PEL—proximity electron lithography*

## CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions involving Lithography, ESH, Yield Enhancement, Metrology, and Modeling & Simulation are outlined in this section.

### ENVIRONMENT, SAFETY, AND HEALTH

The recent discussion over the continued use of perfluorooctyl sulfonates (PFOS) in photochemicals has shown that long- and commonly-used materials can have safety issues that are being understood only recently. The introduction of new technologies necessarily means the use of materials and chemicals whose safety and environmental implications are even less well known. Practices for use and disposal of the chemicals utilized in lithography must continue with careful regard for the safety of workers and their environment. Refer to the *Environment, Safety, and Health* chapter.

### YIELD ENHANCEMENT

Yield enhancement is expected to become a major challenge, as critical defect sizes become smaller than the limits of optical detection. Non-optical methods of defect detection have yet been demonstrated to have the acquisition rates required for controlling defects in semiconductor manufacturing. Filtration technology is another concern, because filters with pore sizes less than 50 nm do not exist for filtering photoresist materials, and this capability will be needed for the 65 nm node and beyond. Filtration methods applicable at the point-of-use will continue to be needed, and solutions will need to be consistent with this requirement.

### METROLOGY

The rapid advancement of lithography technology and resultant decrease in feature dimensions continues to challenge wafer and mask metrology capability. The existing precision of critical dimension measurement tools does not meet even the somewhat relaxed 20% measurement precision to process tolerance metric at the most advanced technology node. Precision includes measurement tool variation from short- and long-term tool variation as well as tool-to-tool matching. Wafer and mask CD technology is evolving to meet the need for 3D measurements. Potential solutions for near-term CD measurements include CD-scanning electron microscopy, scatterometry, and scanned probe microscopy. A key new requirement is measurement of line edge roughness (LER). Measurement precision for LER must be smaller (better) than that needed for linewidth.

Overlay metrology is also challenged by future technology generations. Traditional overlay test structures do not capture all possible overlay errors that can occur during use of phase shift and optical proximity correction masks.

The complete discussion of Lithography Metrology is located in the Lithography Metrology and Microscopy sections of the *Metrology* chapter. The Lithography Metrology Technology Requirements and Potential Solutions is also presented in that chapter.

### MODELING & SIMULATION

Lithography modeling and simulation needs have been divided into four areas; resist modeling; overlay; defect simulation; and lithography technology and techniques. The modeling and simulation needs for these areas are summarized in Table 60 below and are briefly discussed in the lithography section of the *Modeling and Simulation* chapter.

*Table 60 Lithography Modeling & Simulation Needs and Potential Solutions*

| *KEY AREAS* | *SUMMARY OF NEEDS* | *POTENTIAL SOLUTIONS* |
|---|---|---|
| Resist Modeling | Chemically amplified resists<br>Post exposure bake<br>Diffusion<br>Line edge roughness<br>Surface interaction | Develop methodology for calibrating models on production tooling<br>Validate models across multiple features, sizes and pitches for 2D and 3D profiles |
| | Thin and multilayer resists<br>Link litho to etch - uniformity<br>Surface interactions | Extend models to emerging materials and techniques (optical, EPL and EUVL)<br>Integrate dry etch modeling into lithography simulation |
| | Molecular level modeling<br>Diffusion (model generation)<br>Post exposure bake (model generation)<br>Line edge roughness<br>Stochastic shot noise | Establish mechanism-based models from basic studies on model materials |
| Overlay | Models for alignment signals | Establish techniques to calibrate, model and optimize overlay on product tooling |
| | Feature size dependent pattern placement | Tools for optical system level calculation of pattern position and application of correction techniques |
| | 45 nm node (and EUVL) | Extend current models to future technology nodes and emerging lithography |
| Defect simulation | Sort killer and non-critical defects | Model defect printability from masks through final product |
| Lithography technology, techniques and issues | Phase shift lithography<br>High numerical aperture effects<br>Surface roughness; scattering<br>EUVL<br>ML2, EPL and other emerging lithographies | Full system level simulation of lithography tools with emphasis on balancing tradeoffs and optimizing performance (resolution, aberrations, throughput, masks, and material inhomogeneities) on product<br>Simulation based assessment of emerging lithographies |