INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2001 EDITION

METROLOGY

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METROLOGY

Metrology is an essential enabler if the industry is to continue on a two-year schedule for introduction of new technology generations. The reduction of feature size drives the timeline for metrology solutions for new materials, process, and structures. Metrology accelerates yield improvement at every stage of manufacturing. It enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The increasing diversity of chip types will spread already limited metrology resources over a wider range of challenges. The metrology community including suppliers, chip manufacturers, consortia, and research institutions must provide cooperative research, development, and prototyping in order to meet the ITRS timeline. *The forefront developments in measurement technology must be commercialized in a timely manner.* The feature sizes a decade away in the 2001 Roadmap will greatly challenge all measurements.

The near term challenges for metrology revolve around the need for controlling scaling as well as new materials and processes used for gate stack, ultra-shallow junctions, and copper/low κ interconnect. Beyond the electrical and physical metrology for high and low κ dielectric films, metrology for pore size distribution and voids in copper lines are added to the critical needs. The increasing emphasis on active area measurements instead of test structures in scribe (kerf) lines places new demands on metrology. Long-term needs are difficult to address due to the lack of clarity of device design and interconnect technology. The selection of a replacement for copper interconnect remains a research challenge. Although materials characterization and some existing in-line metrology apply to new device and interconnect structures, development of manufacturing capable metrology requires a more certain knowledge of materials, devices, and interconnect structures.

All areas of measurement technology (especially those covered in the Defect Reduction Technologies Roadmap) are being combined with computer integrated manufacturing (CIM) and data management systems for information-based process control. Although Integrated Metrology still needs a universal definition, it has become the term associated with the slow migration from offline to inline and *in situ* measurements. The combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

Metrology tool development requires access to new materials and structures if it is to be successful. This requires a greater attention to expanding close ties between metrology development and process development. When the metrology is well matched to the process tools and processes, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

SCOPE

The metrology topics covered in the 2001 *Metrology* roadmap are microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; *in situ* sensors and cluster stations for process control; reference materials; correlation of physical and electrical measurements; and packaging. These topics are reported in the following sections: Metrology for *Processes Facing Statistical Limits*; *Microscopy*; *Lithography Metrology*; *Front End Processes Metrology*; *Interconnect Metrology*; *Materials and Contamination Characterization*; *Reference Materials*; *Metrology Integration*; and *Packaging Metrology*.

International cooperation on the development of new metrology technology and standards will be required. Both metrology and process research and development organizations must work together with the industry including both the supplier and IC manufacturer. Metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. Despite the existence of standardized definitions and procedures for metrics, individualized implementation of metrics such as measurement precision to tolerance (P/T) ratio is typical.[1] The P/T ratio for evaluation of automated measurement capability for use in statistical process control relates the measurement variation (precision) of the metrology tool to the product specification limits. Determination of measurement tool variations is frequently carried out using reference materials that are not representative of the product or process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. It is also possible that the sensitivity of the instrument could be insufficient to detect small but

unacceptable process variations. There is a need for a metric that describes the resolution capability of metrology tools for use in statistical process control. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio. However, because the type of resolution depends on the process (e.g., thickness requires spatial resolution while levels of metallics on the surface require resolution of atomic percent differences), topic-specific metrics may be required. A new need is for standardized approach to determination of precision when the metrology tool provides discrete instead of continuous data. This situation occurs, for example, when significant differences are smaller than the instrument resolution. See for example, *SEMI E89-0999 Guide For Measurement System Capability Analysis* [1]

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for metrology should decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 65 nm node. Metrology needs after 2007 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect materials will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 96 presents the ten major challenges for metrology.

1 SEMI E89-0999 Guide For Measurement System Capability Analysis

Table 96 Metrology Difficult Challenges

Five Difficult Challenges ≥65 nm, Through 2007	*Summary of Issues*
Factory level and company wide metrology integration for real time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are void detection in copper lines and pore size distribution in patterned low κ dielectrics.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers. High frequency dielectric constant measurements advances need to continue.
Measurement test structures and reference materials.	Scribe lines are shrinking and correlation to variation of chip properties is difficult. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between scribe line measurement and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate stable reference materials.
Five Difficult Challenges < 65 nm, Beyond 2007	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for Damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.
Statistical limits of sub-65 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters is needed to replace inspection, reduce process variation, control defects, and reduce waste.*

TECHNOLOGY REQUIREMENTS

Selected measurement requirements for metrology tools are listed in Tables 97–101. The microscopy resolution refers to the ability of a CD measurement tool to distinguish between lines that differ in width. The spatial resolution requirements for 2- and 3-dimensional (2D and 3D) dopant profiling are based on the requirements of Modeling & Simulation. Meeting 2D dopant profiling requirements will be difficult, and methods with slightly less spatial resolution may provide useful information. Measurement accuracy for all metrology requires appropriate reference materials.

Table 97a Metrology Technology Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*DRIVER*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
Microscopy								
Inline, nondestructive microscopy resolution (nm) for P/T=0.1	**0.65**	**0.53**	**0.45**	**0.37**	**0.32**	**0.3**	**0.25**	*MPU GATE*
Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	**11.4**	**11.9**	**12.4**	**13**	**13.6**	**14.3**	**15.2**	
Materials and Contamination Characterization								
Real particle detection limit (nm) [B]	**65**	**53**	**45**	**37**	**32**	**30**	**25**	*D1/2*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**43**	**35**	**30**	**24**	**21**	**20**	**17**	*D1/2*
Specification limit of total surface contamination for critical COI surface materials (atoms/cm^2) [C]	**5.0E+09**	**5.0E+09**	**5.0E+09**	**5.0E+09**	**5.0E+09**	**5.0E+09**	**5.0E+09**	*MPU GATE*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.0E+08**	**5.0E+08**	**5.0E+08**	**5.0E+08**	**5.0E+08**	**5.0E+08**	**5.0E+08**	*MPU GATE*

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Notes for Table 97a and b:

[A] *Metal and via aspect ratios are additive for dual-Damascene process flow.*

[B] *This value depends on surface microroughness and layer composition.*

[C] *The requirements for metal contamination have been changed based on less stringent requirements found in Front End Processes chapter Surface Preparation Technology Requirements table, Note F.*

Table 97b Metrology Technology Requirements—Long-term

YEAR OF PRODUCTION	*2010*	*2013*	*2016*	*DRIVER*
DRAM ½ PITCH (nm)	*45*	*32*	*22*	
MPU / ASIC ½ PITCH (nm)	*45*	*32*	*22*	
MPU PRINTED GATE LENGTH (nm)	*25*	*18*	*13*	
MPU PHYSICAL GATE LENGTH (nm)	*18*	*13*	*9*	
Microscopy				
Inline, nondestructive microscopy resolution (nm) for P/T=0.1	**0.18**	**0.13**	**0.09**	*MPU*
Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	**16.1**	**19.3**	**23.2**	*D1/2*
Materials and Contamination Characterization				
Real particle detection limit (nm) [B]	**18**	**13**	**9**	*D1/2*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**12**	**9**	**6**	*D1/2*
Specification limit of total surface contamination for critical COI surface materials (atoms/cm^2) [C]	**5.0E+09**	**5.0E+09**	**5.0E+09**	*D1/2*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.0E+08**	**5.0E+08**	**5.0E+08**	*D1/2*

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

[A] *Metal and via aspect ratios are additive for dual-Damascene process flow.*

[B] *This value depends on surface microroughness and layer composition.*

[C]

MEASUREMENTS FOR PROCESSES FACING STATISTICAL LIMITS AND PHYSICAL STRUCTURES REACHING ATOMIC DIMENSIONS

As the dimensions of integrated circuit devices continue to shrink, the finite dimensions of the atoms within the structures will lead to statistical variations in critical dimensions and thus device properties. Furthermore, as dimensions of structures continue to shrink, the physical properties will deviate from the bulk properties because of quantum mechanical and mean free path effects. For instance, the lattice spacing of silicon atoms in a 35 nm gate represents about 1% of the gate length. The effects of statistical variations may be even more pronounced in gate dielectric structures composed of multi-layers of different components, each only several atoms thick. The engineering of such structures must take these statistical variations of dopant atoms and intrinsic defects and the quantum mechanical effects of confined structures into account to obtain sufficiently uniform device and circuit performance for large-scale integration.

Advances in interconnect technology are introducing conductor materials such as copper that must be excluded from the semiconductor itself and low κ interconnect structures. Process and process modeling advances are required to deposit barrier layers of the order of only a few atomic layers that are pin hole-free. Metrology must be developed to ensure the integrity of barrier layers. As the conductor cross-section shrinks to the order of the mean free path of electrons, the bulk conductivity model no longer applies.

Several issues challenge measurement of transistor structures. Metrology of gate dielectric structures requires a practical standardized model of the quantum mechanical effects at the silicon – dielectric interface and gate – dielectric interface. Stochastic modeling strategies will be required to supplement deterministic (continuum) modeling techniques that have been used thus far. Significant advances in two- and three-dimensional dopant profiling metrology will be required to validate modeling. Mechanical stress changes the transport properties of transistors, and this can be either advantageous or detrimental. Metrology and modeling needs to be developed to manage stress effects.

These and other statistical variations in real materials and structures are independent of measurement uncertainties, and will add quadratically to the total uncertainty to the total uncertainty of the values of measured quantities. In addition, they must be taken into account in circuit and process design in ways that are not yet envisioned. It appears that the measurement uncertainties of a number of parameters specified for future device generations elsewhere in the Roadmap cannot be met for fundamental physical reasons having little to do with metrology *per se*.

MICROSCOPY

Microscopy is used in most of the core technology processes where two-dimensional distributions, i.e., digital images of the shape and appearance of integrated circuit (IC) features reveal important information. Usually, imaging is the first, but many times the only one step in the "being able to see it, measure it, and control it" chain. Microscopes typically employ light, electron beam, or scanned probe methods. Beyond imaging, online microscopy applications include critical dimension (CD) and overlay measurements along with defect/particle detection, review and auto-classification. Because of the high value and quantity of wafers, the need for rapid, non-destructive, inline imaging and measurement is growing. Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques and networked measurement tools will be needed to meet the requirements of near future IC technologies. Microscopy techniques and measurements based on them must serve the technologists better giving fast, detailed, adequate information on the processes in ways that help to establish process control in a more automated manner.

Scanning Electron Microscopy (SEM)—continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 90 nm generation. New inline SEM technology, such as the use of ultra-low voltage electron beams (<250 eV) may be required for overcoming image degradation due to charging, contamination, and radiation damage of the sample surface, while maintaining adequate resolution. Alternative paths should also be sought. SEM images carry more information that is currently being used, therefore it is important to develop measurement methods that reveal and express the needed information. Measured and modeled image and line-scan libraries and fast and accurate comparative techniques are likely to gain importance in process development. Improving the resolution of the SEM by the reduction of spherical aberration leads to an unacceptably small depth of field; consequently non-traditional SEM imaging techniques such as the implementation of nano-tips, "confocal-like" SEM imaging and electron holography need to be developed, if they can prove to be production-worthy methodologies. Refer to the *supplementary material for more details on Microscopy*.

Obtaining the most information from the SEM image requires a greater understanding of the imaging process. This is obtained through modeling. There is a need to improve and extend the modeling of the signal generation process by including the effects of sample charging and the role of the instrument electronics. A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and the deposition of charge in gate structures, sets a fundamental limit to the utility of all microscopies relying on charged particle beams.

Determination of the real 3D shape for sub-90 nm contacts/vias, transistor gates, interconnect lines or Damascene trenches will require continuing advances in existing microscopy and sample preparation methods. Cross sectioning by FIB and lift-out for imaging in a TEM or a STEM has been successfully demonstrated.

Scanning probe microscopy (SPM)—may be used to calibrate CD-SEM measurements. Stylus microscopes offer 3D measurements that are insensitive to the conductivity of the material scanned. Flexing of the stylus degrades measurements, however, when the probe is too slender. The stylus shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High stiffness probe materials, such as carbon nano-tubes, may alleviate this problem.

Far-field optical microscopy—is limited by the wavelength of light. Deep ultra-violet sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of defects is needed. Optical microscopes will continue to have application in the inspection of large features, such as solder bump arrays for multi-chip modules.

For *defect detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes. High speed scanning has been demonstrated with arrayed SPMs, (that might be faster than SEMs) but issues associated with stylus lifetime, uniformity, characterization, and wear need to be addressed. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput and operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs.

LITHOGRAPHY METROLOGY

Lithography metrology continues to be challenged by rapid advancement of patterning technology. Critical dimension measurement capability does not meet precision requirements which comprehend measurement variation from individual tool reproducibility and tool to tool matching. As indicated in the introduction, reproducibility includes repeatability, variation from reloading the wafer, and long term drift. CD measurement must be extended to line shape determination. The determination of etch bias (the difference in CD before and after etch) remains a difficult challenge. . Electrical CD measurements provide a monitoring of gate and interconnect linewidth, but only after the point where reworking the wafers is no longer possible. Overlay measurements are challenged by phase shift and optical proximity correction masks, and the use of different exposure tools for metal trench and via will compound the difficulty.

Although a number of potential solutions for CD measurement exist, there is no single method that meets every measurement requirement. CD-SEM continues to be used for wafer and mask measurement of lines and via/contact. A considerable effort has been aimed at overcoming electron beam damage to photoresist used by 193 nm exposure and that will continue when 157 nm exposure tools are introduced. Although software that detects changes in line profile based on comparison to a golden linescan is available, software for 3D line shape determination from top down CD-SEM images remains in development. CD-SEM capable of e-beam tilt could set the path towards line shape evaluation concurrent to CD measurements. Developments in electron beam source technology that improve resolution and precision are being tested. CD-SEM is facing an issue with poor depth of field unless a new approach to SEM based CD measurement is found. Scatterometry has moved into manufacturing, and does provide line shape metrology. Here, we use the term scatterometry to refer to single wavelength – multi angle optical scattering and to multi-wavelength – single angle varieties. The next step is for the development of scatterometry for contact and via structures. Because scatterometry measurements typically provide discretized data, CD variation is determined in set linewidth steps. Therefore, a standardized approach to determination of precision is required for discretized data. Scatterometry has been proposed as a candidate for integration into lithography track systems. The use of "feed forward" control concepts must be extended to lithography metrology taking data from resist measurements and controlling subsequent processing, such as etch, to improve product performance. The use of overlay measurement equipment for CD control has also been reported. This method is based on the fact that the change in linewidth also effect the length of the photoresist lines which can then be measured using the optical microscope of the overlay system. A special test structure with arrays of line and arrays of spaces is required. CD-AFM measurements are an excellent means of verifying line shape and calibrating CD measurements. New probe tip technology and 3-D tilt-able cantilever is required if CD-AFM is to be applied to dense line measurement below 90 nm node. Focus – Exposure correlation studies can be done using all of the above methods as well as by the dual beam FIB (SEM plus focused ion beam) where there is an immediate correlation with line shape. Electron holography has been proposed as a long term CD measurement technology.

Line edge roughness (LER) was recently correlated to an increase in transistor leakage current but not to changes in drive current.(2) Therefore, LER has been added as a measurement requirement. It is important to note that the precision requirement for LER are several years ahead of those required for CD as indicated below. Presently, there is no standard method of determining line edge roughness. [2]

Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with scanning probe microscopy (SPM). The need for new target structures has been

[2] *K. Patterson, J.L. Sturtevant, J. Alvis, N. Benavides, D. Bonser, N. Cave, C. Nelson-Thomas, B. Taylor, K. Turnquest, Experimental Determination of the Impact of Polysilicon LER on sub-100 nm Transistor Performance, In Metrology, Inspection, and Process Control for Microlithography XV, SPIE Vol 4344, 2001, pp 809-814*

suggested as a means of overcoming the issues associated with phase shift mask and optical proximity mask alignment errors not detectable with traditional targets. Overlay for on-chip interconnect will continue to be challenging. The use of chemical mechanical polishing for planarization degrades target structures. Thus as requirements for tighter overlay control are introduced, the line edge of overlay targets in interconnect are roughened. The low κ materials used as insulators will continue to make overlay more difficult especially as porous low κ move into manufacturing.

The Lithography Metrology Requirements Tables are divided into wafer and mask requirements. The mask metrology requirements are further divided into the needs for each type of exposure technology : optical, EUV, and electron projection

Table 98a Lithography Wafer Metrology Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Wafer gate CD control*	6.5	5.3	4.5	3.7	3.2	2.8	2.5
Wafer dense line CD control*	13	11.5	10	9	8	7	6.5
Wafer contact CD control*	15	13	11.5	10	9	8	7
Line Edge Roughness control*	4.5	3.9	3.3	2.7	2.4	2.1	1.8
Wafer CD metrology tool precision* (P/T=.2 for isolated lines**)	1.3	1.1	0.9	0.75	0.65	0.56	0.5
Wafer CD metrology tool precision* (P/T=.2 for dense lines**)	2.6	2.3	2	1.8	1.6	1.4	1.3
Wafer CD metrology tool precision* (P/T=.2 for contacts**)	3	2.6	2.3	2	1.8	1.6	1.4
Wafer CD metrology tool precision* (P/T=.2 for LER**)	0.9	0.78	0.66	0.54	0.48	0.42	0.36
Maximum CD measurement bias (%)	10	10	10	10	10	10	10
Wafer overlay control (nm)	65	58	52	45	42	38	35
Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	6.5	5.8	5.2	4.5	4.2	3.8	3.5

** All precision values are 3 Sigma in nm and include metrology tool to tool matching*

*** Measurement tool performance needs to be independent of target shape, material, and density*

LER—Local linewidth variation (3 Sigma total, all frequency components included, both edges) evaluated along a distance equal to four technology nodes"

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Table 98b Lithography Metrology Technology Requirements—Long-term

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*45*	*32*	*22*
MPU PRINTED GATE LENGTH (nm)	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*18*	*13*	*9*
*Wafer gate CD control**	**1.8**	**1.3**	**0.9**
*Wafer dense line CD control**	**4.5**	**3.2**	**2.2**
*Wafer contact CD control**	**5**	**3.5**	**2.5**
*Line Edge Roughness control**	**1.3**	**0.9**	**0.65**
Wafer CD metrology tool precision (P/T=.2 for isolated lines**)*	**0.36**	**0.26**	**0.18**
Wafer CD metrology tool precision (P/T=.2 for dense lines**)*	**0.9**	**0.64**	**0.44**
Wafer CD metrology tool precision (P/T=.2 for contacts**)*	**1**	**0.7**	**0.5**
Wafer CD metrology tool precision (P/T=.2 for LER**)*	**0.26**	**0.18**	**0.13**
Maximum CD measurement bias (%)	**10**	**10**	**10**
Wafer overlay control (nm)	**18**	**13**	**9**
Wafer overlay output metrology precision (nm, 3 sigma) P/T=.1*	**1.8**	**1.3**	**0.9**

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Table 99a Lithography Metrology (Mask) Technology Requirements: Optical—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Wafer gate CD control*	6.5	5.3	4.5	3.7	3.2	3	2.5
Wafer overlay control*	45	40	35	31	28	27	26
Wafer contact CD control*	15	13	11.5	10	9	8	7
Mask minimum image size (at 4×, nm)	360	300	260	220	200	180	160
Optical Section							
Minimum OPC size (opaque at 4×, nm)	180	150	130	110	100	90	80
Image placement (multipoint at 4×, nm)	27	24	21	19	17	17	16
CD Uniformity (3 Sigma at 4×, nm)							
Isolated lines (MPU gates), binary	8.6	7.4	6.3	5.7	5.1	4.6	3.5
Isolated lines (MPU gates), alternated	12	10.4	8.8	8	7.2	6.4	5.6
Dense lines (DRAM half-pitch)	10.4	9.2	8	7.2	6.4	5.6	4.2
Contact/Vias	8	6.9	6.1	5.3	4.8	4.3	3.2
Mask image placement metrology (precision, P/T=0.1)	2.7	2.4	2.1	1.9	1.7	1.7	1.6
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, binary**)	1.8	1.5	1.3	1.1	1	0.9	0.7
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, alternated**)	2.4	2.1	1.75	1.6	1.45	1.3	1.15
Mask CD metrology tool precision* (P/T=0.2 for dense lines**)	2.1	1.85	1.6	1.45	1.3	1.15	0.85
Mask CD metrology tool precision* (P/T=0.2 for contact/vias**)	1.6	1.4	1.2	1.05	0.95	0.85	0.65
Specific requirements							
Alternated PSM phase mean deviation	2	2	2	2	2	1	1
Phase metrology precision, P/T=0.2	0.4	0.4	0.4	0.4	0.4	0.2	0.2
Alternated PSM phase uniformity (±degrees)	2	2	2	2	2	1	1
Phase uniformity metrology precision, P/T=0.2	0.4	0.4	0.4	0.4	0.4	0.2	0.2

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Table 99b Lithography Metrology (Mask) Technology Requirements: EPL—Near and Long-term

YEAR OF PRODUCTION	*2006*	*2007*	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*70*	*65*	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*70*	*65*	*45*	*32*	*22*
MPU PRINTED GATE LENGTH (nm)	*40*	*35*	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*28*	*25*	*18*	*13*	*9*
Wafer gate CD control*	3	2.5	1.8	1.3	0.9
Wafer overlay control*	27	26	18	13	9
Wafer contact CD control*	8	7	5	3.5	2.5
Mask minimum image size (at 4×, nm)	180	160	112	80	60
EPL					
Minimum stitching feature size (nm)	90	80	56	40	30
Image placement error (nm, multipoint)	17	16	11	8	6
Complementary mask pair placement error (nm, multipoint) for stencil mask	15	14	10	7	5
Metrology stitching precision (3 sigma, P/T=0.1)	9	8	5.6	4	3
Mask image placement metrology precision (3 sigma, P/T = 0.1)	1.7	1.6	1.1	0.8	0.6
Complementary mask pair metrology precision (3 sigma, P/T = 0.1)	1.5	1.4	1	0.7	0.5
CD Uniformity (3 Sigma at 4× nm)					
Isolated lines (MPU gates)	7	6	4	3	2
Dense lines (DRAM half-pitch)	11	10	7	5	3.5
Contact/Vias	10.5	9.5	8	5.5	4
Mask CD metrology tool precision* P/T=0.2 for isolated lines**	0.7	0.6	0.8	0.6	0.4
Mask CD metrology tool precision* P/T=0.2 for dense lines**	1.1	1	1.4	1	0.7
Mask CD metrology tool precision* P/T=0.2 for contact/vias**	1.05	0.95	1.6	1.1	0.8
Specific requirements					
Clear area transmission uniformity (3 Sigma %) for membrane	1%	0.90%	0.70%	0.60%	0.50%
Energy loss (delta E/E) (%) for membrane	0.09%	0.08%	0.07%	0.05%	0.04%
Scatterer sidewall angle tolerance (degrees)	0.5	0.5	0.5	0.5	0.5
Scatterer/stencil LER (3 Sigma, nm)	5	4.5	3	2	1.5
Metrology transmission uniformity precision (P/T=0.2, %)	0.20%	0.18%	0.07%	0.06%	0.05%
Energy loss metrology precision (3 sigma, P/T = 0.1)	0.009%	0.008%	0.007%	0.005%	0.004%
Sidewall angle metrology precision (3 sigma, P/T = 0.2)	0.1	0.1	0.1	0.1	0.1
LER metrology precision (3 sigma, P/T=0.2)	1	0.9	0.6	0.4	0.3

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Table 99c Lithography Metrology (Mask) Technology Requirements: EUV—Near and long-term

YEAR OF PRODUCTION	*2006*	*2007*	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*70*	*65*	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*70*	*65*	*45*	*32*	*22*
MPU PRINTED GATE LENGTH (nm)	*40*	*35*	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*28*	*25*	*18*	*13*	*9*
EUV					
Image placement error (nm, multipoint)	17	16	11	8	6
CD Uniformity (3 Sigma at 4X, nm)					
Isolated lines (MPU gates)	7	6	4	3	2
Dense lines (DRAM half-pitch)	11	10	7	5	3.5
Contact/Vias	12.5	11	8	5.5	4
Mask CD metrology tool precision* P/T=0.2 for isolated lines**	0.7	0.6	0.8	0.6	0.4
Mask CD metrology tool precision* P/T=0.2 for dense lines**	1.1	1	1.4	1	0.7
Mask CD metrology tool precision* P/T=0.2 for contact/vias**	1.25	1.1	1.6	1.1	0.8
Specific Requirements					
Mean peak reflectivity	65%	65%	66%	67%	67%
Peak reflectivity uniformity (3 Sigma %)	0.69%	0.61%	0.42%	0.33%	0.24%
Absorber sidewall angle tolerance (degrees)	1	1	0.75	0.5	0.5
Absorber LER (3 Sigma, nm)	5	4.5	3	2	1.5
Mask substrate flatness (peak-to-valley, nm)	70	65	50	45	35
Metrology mean peak precision (P/T=0.2, %)	1.30%	1.30%	1.30%	1.30%	1.30%
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)	0.13%	0.12%	0.08%	0.06%	0.05%
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)	0.2	0.2	0.15	0.1	0.1
Absorber LER metrology precision (3 sigma, P/T=0.2)	1	0.9	0.6	0.4	0.3
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)	14	13	10	9	7

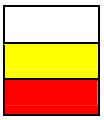
**All precision values are 3 Sigma in nm and include metrology tool to tool matching*

*** Measurement tool performance needs to be independent of target shape, material and density*

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



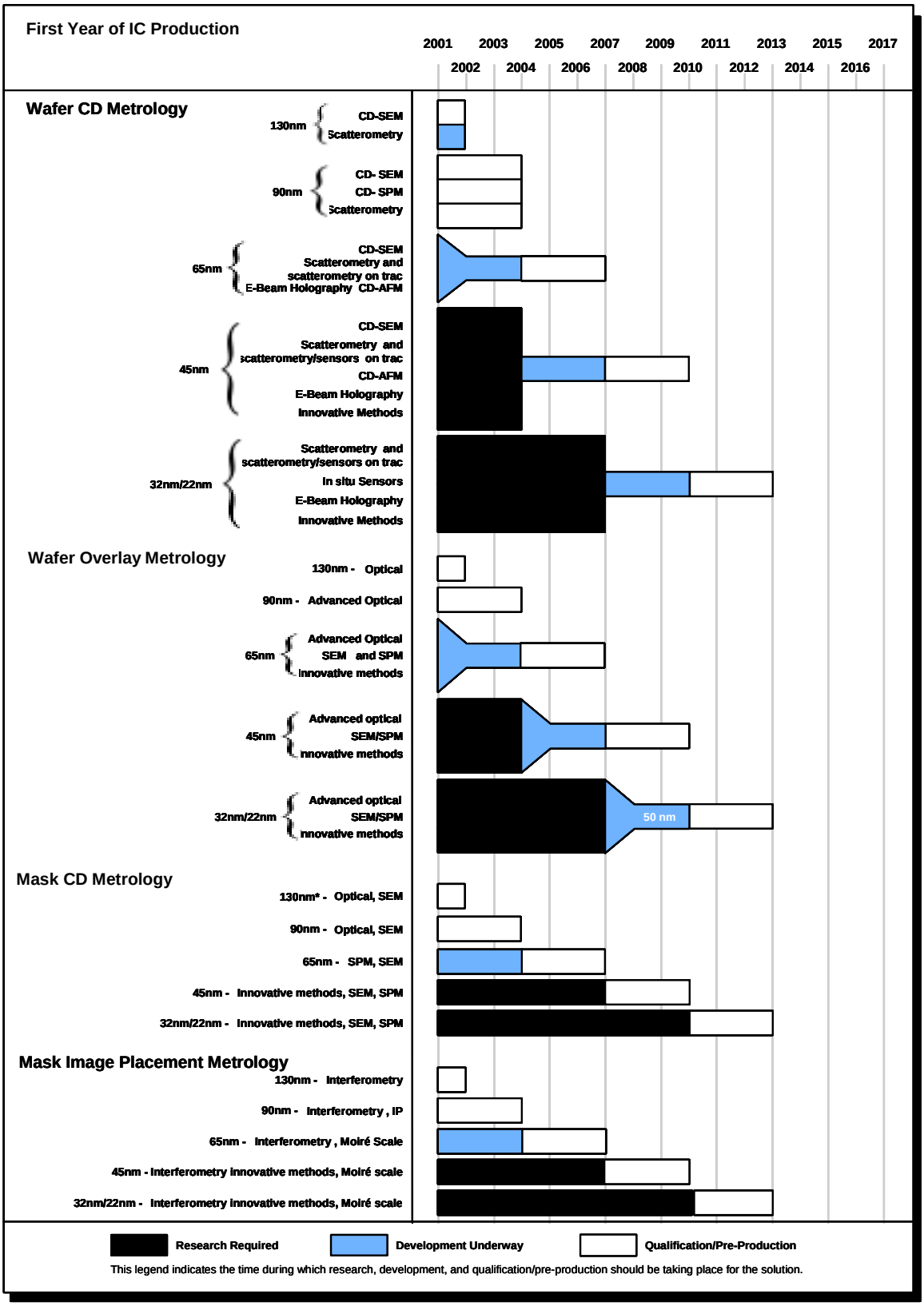


Figure 61 Lithography Metrology Potential Solutions

FRONT END PROCESSES METROLOGY

The accelerated introduction of new technology generations requires accelerated advancements of metrology for transistor development and fabrication. In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front end plasma etch technologies are covered. Process integration issues such as the need to control leakage current and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Metrology requirements for Front End Processes are shown in Table 100a and b, and the Potential Solutions are shown in Figure 62.

Table 100a Front End Processes Metrology Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65	
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65	
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35	
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	1×10^{10}	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	*
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	1×10^{9}	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	*
High-performance logic EOT equivalent oxide thickness (EOT) nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	M GATE
Low operating power logic EOT	2	1.8	1.6	1.4	1.2	1.1	1	
± 3σ dielectric process range (EOT) (nm)	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	
EOT measurement precision 3σ(nm) [B]	0.0052	0.0048	0.0044	0.0036	0.0032	0.0028	0.0024	MPU HIGH-PERFORMANCE
DRAM capacitor structure	Cyl.	Pedestal	Pedestal	Pedestal	Pedestal	Pedestal	Pedestal	D½
DRAM capacitor electrodes	MIS	MIM	MIM	MIM	MIM	MIM	MIM	
DRAM capacitor dielectric material	Ta_2O_5	Ta_2O_5	bb	Ta_2O_5	Not BST??	BST	Epi-BST	
DRAM capacitor dielectric constant	>22	>50	>50	>50	>250	>250	>700	
Equivalent oxide thickness (EOT) (nm)	3	0.95	0.95	0.95	0.45	0.45	0.15	
DRAM capacitor dielectric physical thickness (nm) ±3 σ process range	11.5 ±4%	12.2 ± 4%	12.2 ± 4%	12.2 ± 4%	28.7 ± 4%	28.7 ± 4%	27.2 ± 4%	D½
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.046	0.049	0.049	0.049	0.11	0.11	0.11	D½
Dopant concentration (atoms/cm^3) Dopant atom Metrology for junction depth of (nm)	3×10^{18} P, As, B 27	4×10^{18} P, As, B 22	4×10^{18} P, As, B 19	5×10^{18} P, As, B 15	6×10^{18} P, As, B 13	7×10^{18} P, As, B 12	8×10^{18} P, As, B 10	MPU
Lateral Steepness of dopant profile (nm/decade)	5.1	4.7	4.25	4	3.8	3.5	3.3	
Lateral/depth spatial resolution for 2D / 3D dopant profile (nm)	4.1 / 5.2	2	2	3.9 / 4.0	1.5	1.5	2.6 / 2.0	*
At-line dopant concentration precision (across concentration range) [D]	5%	4%	4%	4%	3%	3%	2%	*

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Table 100b Front End Processes Metrology Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016	DRIVER
DRAM ½ PITCH (nm)	45	32	22	
MPU / ASIC ½ PITCH (nm)	45	32	22	
MPU PRINTED GATE LENGTH (nm)	25	18	13	
MPU PHYSICAL GATE LENGTH (nm)	18	13	9	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	< 1 × 10 ^{10}	< 1 × 10 ^{10}	< 1 × 10 ^{10}	
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	< 1 × 10 ^{9}	< 1 × 10 ^{9}	< 1 × 10 ^{9}	
High- performance logic EOT [A] equivalent oxide thickness (EOT) nm	0.5–0.8	0.4–0.6	0.4–0.5	MPU
Low operating power logic EOT	0.9	0.8	0.6	
± 3σ process range (EOT) (nm)	± 4%	± 4%	± 4%	
Logic dielectric measurement precision 3σ (nm) [B]	0.002	0.0016	0.0016	MPU HIGH - PERFORMANCE
DRAM capacitor structure dielectric material process control requirements	Pedestal MIM epi-BST	Pedestal MIM ???	Pedestal MIM ???	D ½
(Dielectric constant)	>700	>1500	>1500	
Equivalent oxide thickness (nm)	0.15	0.06	0.043	
DRAM capacitor dielectric physical thickness (nm) ±3σ process range [C]	27.2 ± 4%	23 4%	16.4 4%	D ½
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ)	0.11	0.092	0.066	D ½
Dopant concentration (atoms/cm^3) Dopant atom	1.4 x 10^{19} P, As, B	2.0 x 10^{19} P, As, B	? x 10^{19} P, As, B	
Metrology for junction depth of (nm)	7	5	4	
Lateral Steepness of dopant profile (nm/decade)	2.7	1.9	1.6	
Lateral/depth spatial resolution for 2D / 3D dopant profile (nm)	2.2 / 2.0	1.5 / 1.4	1.0 / 1.2	
At-line dopant profile concentration precision (across concentration range) [E]	2%	2%	2%	

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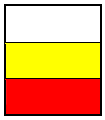
Red—Manufacturable Solutions are NOT Known



Notes for Table 100a and b:

[A] The use of SOI wafers requires metrology development.

[B] Precision calculated from P/T=0.1=6×precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as Ta_2O_5 will be used at and after the 70 nm logic node and possibly at the 100 nm node. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\varepsilon_{high\ \kappa}/\varepsilon_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick Ta_2O_5 (κ= ~25) layer has a 1 nm equivalent oxide (κ=3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.

[C] In the case of MIS structure, physical thickness, t_{diel} , is calculated using the equation of $t_{diel}=(t_{eq.ox}\text{-}1\ nm)_{diel}\ \varepsilon_{high\ \kappa}/3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, t_{diel} is calculated using the equation of $t_{diel}= t_{eq.ox}\ \varepsilon_{high\ \kappa}/3.9$. Here $t_{eq.ox}$ is equivalent oxide thickness, and t_{diel} is dielectric constant of the dielectric material.

[D] High precision measurements with low systematic error are required.

Starting materials —Metrology continues to play an indispensable role in the cost-effective specification of polished, epitaxial and SOI silicon wafers to obtain optimal integrated circuit performance. Key metrology issues include (1) particle and surface defect detection, (2) reductions in edge exclusion, and (3) flatness. Gate oxide integrity (GOI) is becoming less of an issue as gate oxide thickness decreases. Improved tools are required to both size and distinguish different types of localized light scatterers, including particles and crystal originated pits. In addition, new methods may be required for detection and identification of LLSs less than 50–70 nm in size. Metrology for the measurement of wafer parameters within 2 mm of the wafer edge by 2003 is a significant challenge. A key issue addresses the beam or critical probe size in relation to the wafer edge exclusion region. Lithography continues to be the gateway for the successful fabrication of ICs. Standardized metrology for measuring the site flatness under scanning stepper conditions is required for meaningful characterization of the wafer in order to ensure sufficient quality during subsequent patterning operations. Characterization of wafer nanotopography (front-surface features in the 0.2–20 mm spatial wavelength range) is becoming a starting materials requirement in relation to both lithography and CMP for STI. More information can be found in the Starting Materials section of the *Front End Processes* chapter.

Silicon-On-Insulator (SOI) is entering the mainstream of IC device applications, and this is expect to grow further along the Roadmap. An expectation has been that the materials specifications for polished silicon substrates would be transferred to SOI specifications. However, the underlying insulator structure in SOI negatively affects many of the metrology capabilities used for polished silicon substrates. Thus, there is an inability to measure and control SOI material properties at the level desired. This leads to a major challenge for SOI metrology, one that the metrology community must address soon. For more details on these metrology challenges see the FEP section on Starting Materials.

Surface preparation—In situ sensors for particles, chemical composition, and possibly for trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Yield Enhancement* chapter. Particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter.

Thermal/thin films—The transition from silicon dioxide to silicon oxynitride and then to alternate materials with higher dielectric constants remains a key metrology challenge. Near term metrology development will continue to focus on control of nitrogen content and profile by extension of ellipsometry and electrical (capacitance–voltage and current–voltage) methods. Development of metrology for high κ materials needs to continue and metrology for the interface layer remains a difficult challenge. The FEP roadmap shows the first use of high κ in low power devices in 2004 preceding its use for high-performance devices. Potential solutions that enable interfacial control include in-line optical metrology that extends either into the infra-red and/or the ultra-violet wavelength range. Continued development and standardization of electrical testing at high frequencies and new methods for dielectric reliability testing are required. Higher κ electrical testing by traditional capacitor and transistor structures, Hg-probe type capacitor testing, and non-contact, corona discharge methods are all under development. There is considerable evidence that the dielectric properties of transistor and capacitor dielectric films after deposition are different from those subsequent to thermal processing, and this complicates comparison of electrical and physical methods. Correlation must improve. Application of materials characterization methods such as scanning transmission electron microscopy and x-ray reflectivity to higher κ materials as well as methods for controlling Ge in SiGe channels are discussed in the *Materials and Contamination Characterization* section of this Metrology chapter.

FERAM—Although the thickness of the dielectric films are 100 to 200 nm, optical models for in-line film thickness measurement of the metal oxides must be developed when a new materials set is used. The main metrology need is for fatigue testing of the capacitor structures at 10^{16} read write cycles and above.

Doping technology—Improved inline process measurements to control active dopant implants is required beyond 180 nm. Presently, 4-point probe measurement is used for high dose implant and thermally modulated optical reflectance is used for low-dose implant process control. Both methods require improvement, and a new technique that provides direct *in situ* measurement of dose, dopant profile, and dose uniformity would allow real time control. New methods for control of B, P, and As implants are also needed, and an in-line electron microprobe system optimized for B, P, and As x-ray fluorescence based dose measurement has recently been introduced. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of new, non-destructive measurement methods such as carrier illumination (an optical technology) are under evaluation. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology.

VERTICAL STRUCTURES

The control of vertical features and structures, like for example sidewall angle and vertical gates will become more important not only for process development but also in production control. Special process conditions, like micro loading effects in etch processes, will require to perform measurements directly on product rather than on test structures or test wafers. Major efforts in metrology tool development are required to meet these requirements. New techniques like 3D SEM, CD AFM or 3D modeling of scatterometry data need further development to meet a sufficient level of maturity for process control.

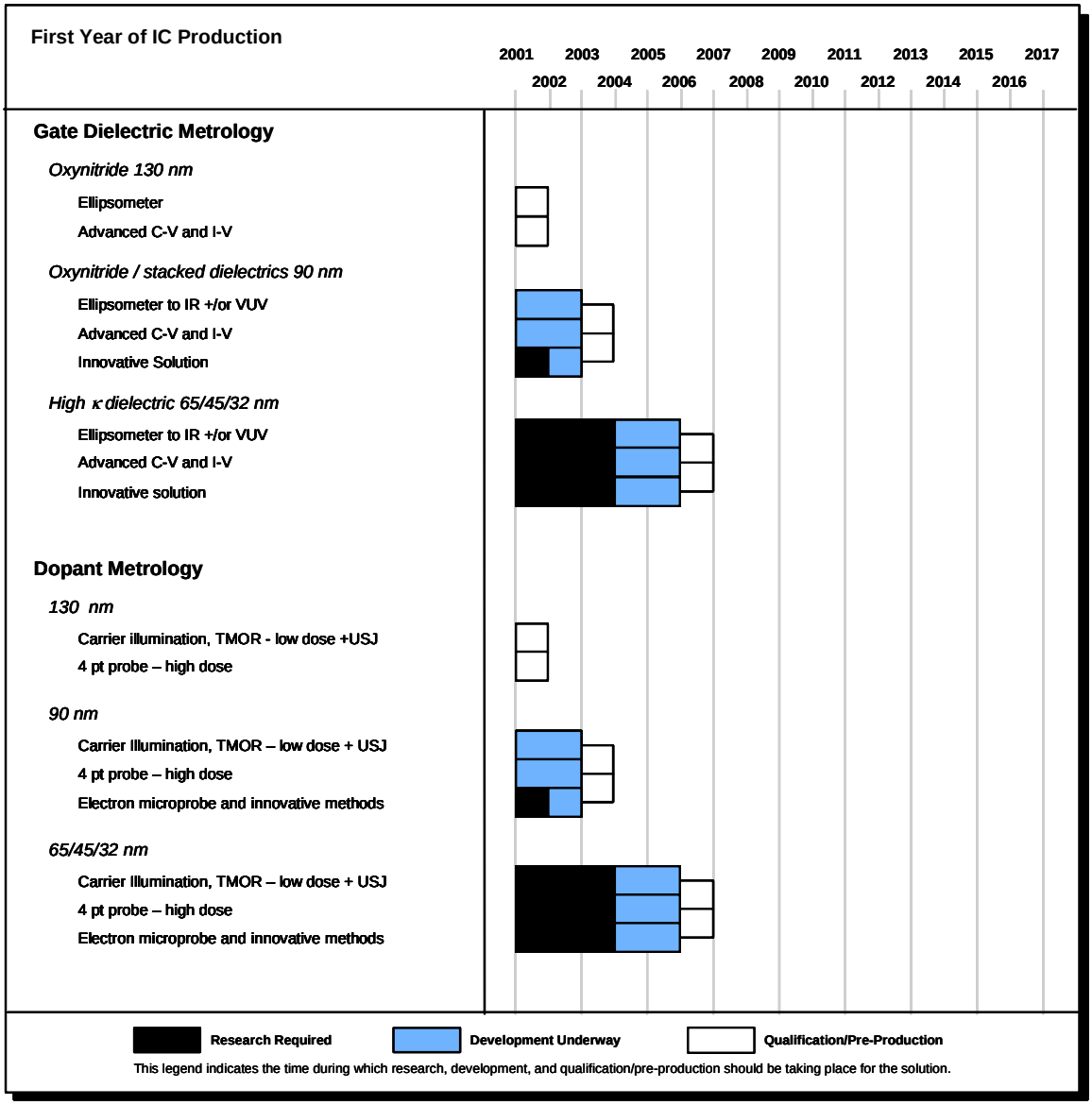


Figure 62 Front End Processes Metrology Potential Solutions

TMOR—thermally modulated optical reflectance
USJ—ultra shallow junctions

INTERCONNECT METROLOGY

Metrology for improving low κ / copper Damascene interconnect processing requires rapid development to meet near term needs. This includes new barrier and low κ materials and processes. Longer term metrology needs are dependent on

new interconnect technologies. Manufacturing experience has shown that voids in copper lines have not been eliminated, yet, by process improvements. Metrology for in-line control of bath chemistry must be implemented and metrology for the statistical detection of voids in patterned copper must be developed. Metrology must also be developed for improved control of porous low κ processing including statistical distribution of pore size and better control for planarization. The accelerated reduction in feature size makes development of metrology for high aspect ratio features a greater challenge for on-chip interconnect development and manufacture. Critical dimension measurements are also a key enabler for development of interconnect processes. CD metrology must be extended to very high aspect ratio structures made from porous dielectric materials and requires 3D information for trench and via/contact sidewalls. These measurements will be further complicated by the underlying multi film complexity.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline measurements for interconnect structures are made on simplified structures or monitor wafers and are often destructive.. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Metrology requirements for Interconnect are shown in Table 101 and the potential solutions are shown in Figure 63 below. The new measurement requirements for void detection in copper lines and killer pores in low κ appears to be difficult or impossible to meet. The need is to have a rapid, in-line observation of very small number of voids/larger pores. The main challenge is the requirement that the information be a statistically significant determination at the percentage specified in Table 101.

Table 101a Interconnect Metrology Technology Requirements—Near Term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*Driver*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
Planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm)	**25 × 32**	**250**	**250**	**25 × 36**	**200**	**200**	**25 × 40**	*MPU*
Measurement precision (nm)	**250 ± 25**			**200 ±20**			**175 ±17**	
Measurement of deposited barrier layer at thickness (nm) / Process range (± 3σ) precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	**18 10% 0.06**	**15 10% 0.05**	**13 10% 0.043**	**11 10% 0.037**	**10 10% 0.033**	**9 10% 0.03**	**8 10% 0.026**	***MPU***
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**28**	**24**	**20**	**18**	**16**	**14**	**13**	***MPU***
Void size for 1 % voiding in copper lines	**32.5**	**28.75**	**25**	**22.5**	**20**	**17.5**	**16.25**	***MPU***
Detection of killer pore at (nm) size	**6.5**	**5.75**	**5**	**4.5**	**4**	**3.5**	**3.25**	***MPU***
Measure interlevel metal insulator bulk / effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× local clock frequency (GHz) [B]	**2.7 3.0–3.7 1.7**	**2.7 3.0–3.7 2.3**	**2.7 2.9–3.5 3.1**	**2.2 2.5–3.0 4**	**2.2 2.5–3.0 5.2**	**2.2 2.5–3.0 5.6**	**1.7 2.0–2.5 6.7**	***MPU***

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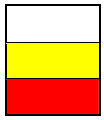


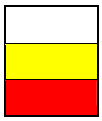
Table 101b Interconnect Metrology Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016	DRIVER
DRAM ½ PITCH (nm)	45	32	22	
MPU / ASIC ½ PITCH (nm)	45	32	22	
MPU PRINTED GATE LENGTH (nm)	25	18	13	
MPU PHYSICAL GATE LENGTH (nm)	18	13	9	
Planarity requirements: lithography field (mm × mm)/ planarity for minimum interconnect CD (nm) / measurement precision	25 × 44 175 ±17	25 × 52 175 ±17	175 ±17	MPU
Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ(nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	7 10% 0.023	5 10% 0.017	4 10% 0.013	MPU
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% X height, 50% areal density, 500 μm square array	5	4	3	MPU
Void size for 1 % voiding in copper lines	11.25	8	5.5	MPU
Detection of killer pore at (nm) size	2.25	1.6	1.1	MPU
Measure interlevel metal insulator bulk / effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× clock frequency (GHz) [B]	1.6 2.0 11.5	<1.6 1.9 19.3	1.5 1.7 28.7	MPU

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Notes for Table 101a and b:

[A] Roadmap predicts barrier for 35 nm technology node will be formed by reactive processes in metal or dielectric or both instead of by deposition.

[B] Minimum effective dielectric constant is listed. Due to divergence of DRAM and logic requirements, minimum listed number is associated with logic requirements. The development of a measurement technique for low κ dielectric constant and anisotropy is nearly complete up to 40 GHz. Technology transfer to industry will take place from 1999 to 2000.

LOW κ METROLOGY NEEDS

Control of porous material properties continues to be a challenge. Detection of large, "killer, pores in patterned low κ has been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap. Pore size distribution has been characterized off-line by small angle neutron scattering, positron annihilation, and x-ray scattering. Recently, a combination of gas absorption and ellipsometry have been proposed as a potential in-line measurement of pore size. This method needs industry wide evaluation. High frequency measurement of low κ materials and test structures has been developed up to 40 GHz. Equipment, procedures, and test structures materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials need to be reduced to practice and applied to low κ interconnect

Dielectric thinning during chemical mechanical polishing technology must be controlled, and available flatness metrology further developed to for patterned wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations are developing flatness tests that provide the information required for statistical process control that is useful for lithographic processing.

Interconnect specific CD measurement procedures must be further developed for control of etch processes. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capabilities of current in-line CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels. Furthermore, scatterometry must be extended to contact and via structures.

The increase in clock frequency is predicted to occur at a faster pace than in the 1999 ITRS. Continued development of high frequency testing of interconnect structures must occur. This capability must characterize the effects of clock harmonics (5× to 10× base frequency), skin effects, and crosstalk.

CONDUCTOR METROLOGY

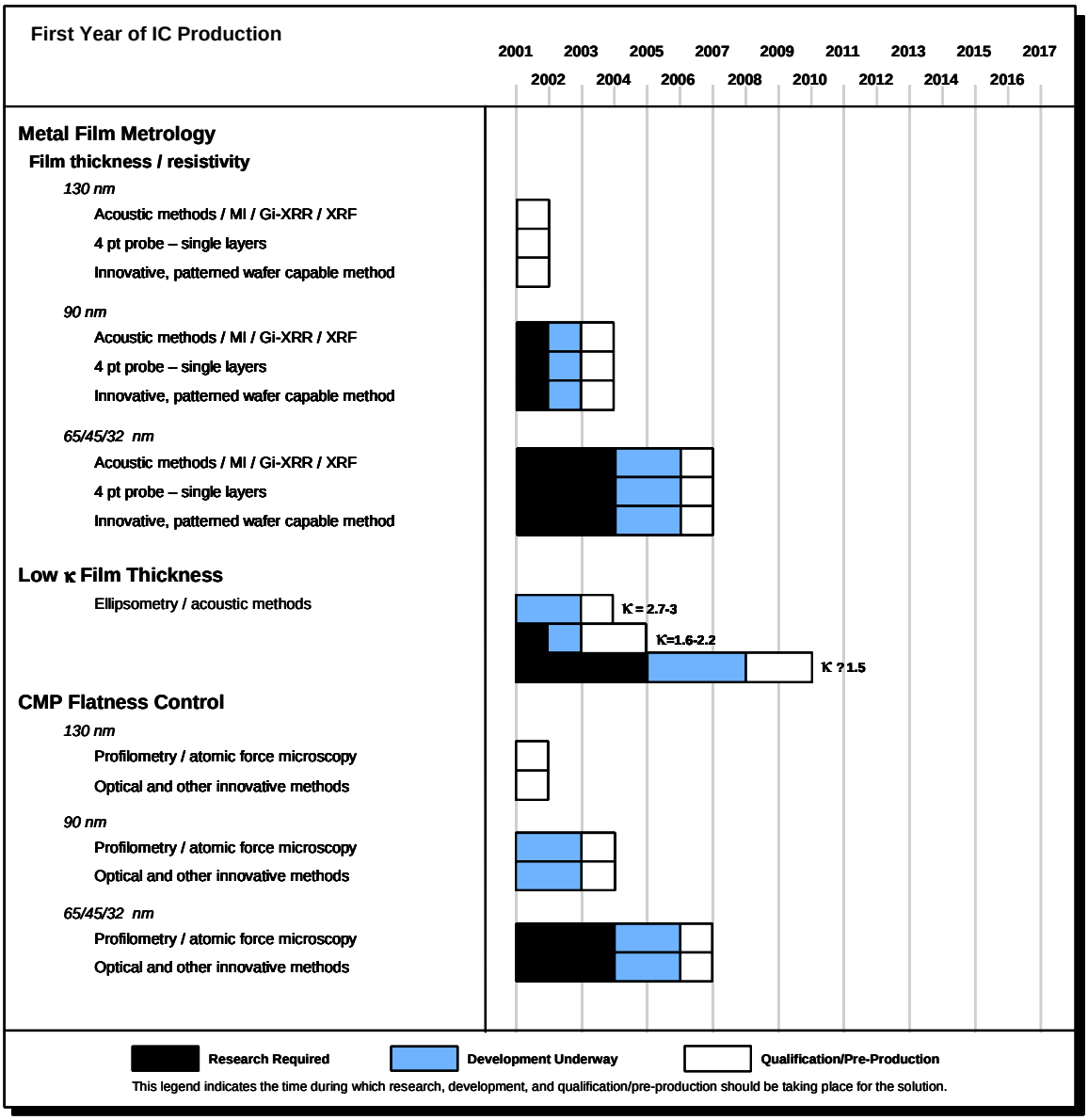
Copper electroplating systems need quantitative determination of the additives, byproducts and inorganic contents in the bath to maintain the desired properties in the electroplated copper film. Process monitoring requires *in situ* measurements of additives, byproducts and inorganic content that result from bath aging.

Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid Chromatography can be used to quantitative measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for the monitoring of inorganics.

Interconnect technical requirements indicate that barrier layers for future technology will be <6 nm thick. If a process window of 20% total thickness variation is assumed, then measurement precision (6σ) must be ≤ 0.12 nm, which is beyond current capabilities. Metrology for fabricated metal lines must be extended from determination of barrier and seed copper thickness on blanket films to patterned structures and detection of voids in copper lines. A metric for copper void content has been proposed in the Interconnect Roadmap and in line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, spatially resolved (for product wafers) multi-layer thickness measurements. Current film thickness methods such X-ray fluorescence, optical reflectivity, ellipsometry, profilometry, and microbalance do not meet this goal. New methods for measuring multiple film layers in production using laser stimulation of acoustic and thermal waves at this time require test structures in the scribe region between chips.

Post CMP processes for interconnect structures require measurement of dishing and erosion in the copper lines. Current optical and acoustic techniques have been explored, but need to address the statistical sampling requirements for the accurate detection of dishing and erosion on a manufacturing environment.

Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.



MI – Metal Illumination, GI-XRR—grazing incidence X-ray reflectivity, XRF – x-ray fluorescence

Figure 63 Interconnect Metrology Potential Solutions

MATERIALS AND CONTAMINATION CHARACTERIZATION

The rapid introduction of new materials, reduced feature size, new device structures, and low temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility.

Often, offline methods provide information that inline methods cannot. For example, transmission electron microscopy (TEM) and scanning TEM, especially those capable of annular dark field (ADF) imaging, provide the highest spatial or cross-sectional characterization of ultra thin films and interfacial layers. ADF-STEM systems equipped with X-ray detection and electron energy loss instrumentation have provided new information about interface chemical bonding. High-performance secondary ion mass spectrometry (SIMS), and its variant time-of-flight (TOF) SIMS, provide

contamination analysis of surfaces and thin film stacks. Grazing incidence X-ray reflectivity provides measurement of thin film thickness and density, while grazing incidence X-ray diffraction provides information about the crystalline texture of thin films. The importance of using diffuse scattering in addition to specular scattering during XRR seems to be critical to building interfacial models from XRR that can be compared to interfacial models from other methods such as TEM/STEM, SIMS, and ion backscattering. Field emission Auger electron spectroscopy (FE-AES) provide composition analysis of particulate contamination down to less than 20 nm in size. Offline characterization of physical properties such as void content and size in porous low κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials. Many of these tools are now available for full wafers up to 300 mm in diameter. Some of these tools are transitioning from offline to inline as combination defect review and analysis tools such as FE-AES and dual-beam focused ion beam (FIB).

Continued development of TEM and STEM imaging capability is required. Several technologies are being applied to materials and process development for critical areas such as high and low κ. Interfacial imaging has been greatly improved by the ADF detector for STEM imaging. The key to the STEM mode is the ability to do materials characterization in an area close to the size of the finest focus of the electron beam. ELS can be done in an area with a diameter of approximately 0.2 nm. With this greatly improved spatial localization, electron energy loss (ELS) characterization can be used to characterize interfacial regions such as the interface between high κ and silicon substrate. STEM with ADF imaging and ELS is just beginning to move into manufacturing support. Advances in image reconstruction software have also improved image resolution and thus interfacial imaging. Several improvements in TEM/STEM technology are in early stages of development, and this development should move into commercialized products as soon as possible. These include lens aberration correction and monochromators for the electron beam.

Promising new technology such as high-energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. Beta site systems are now being tested.

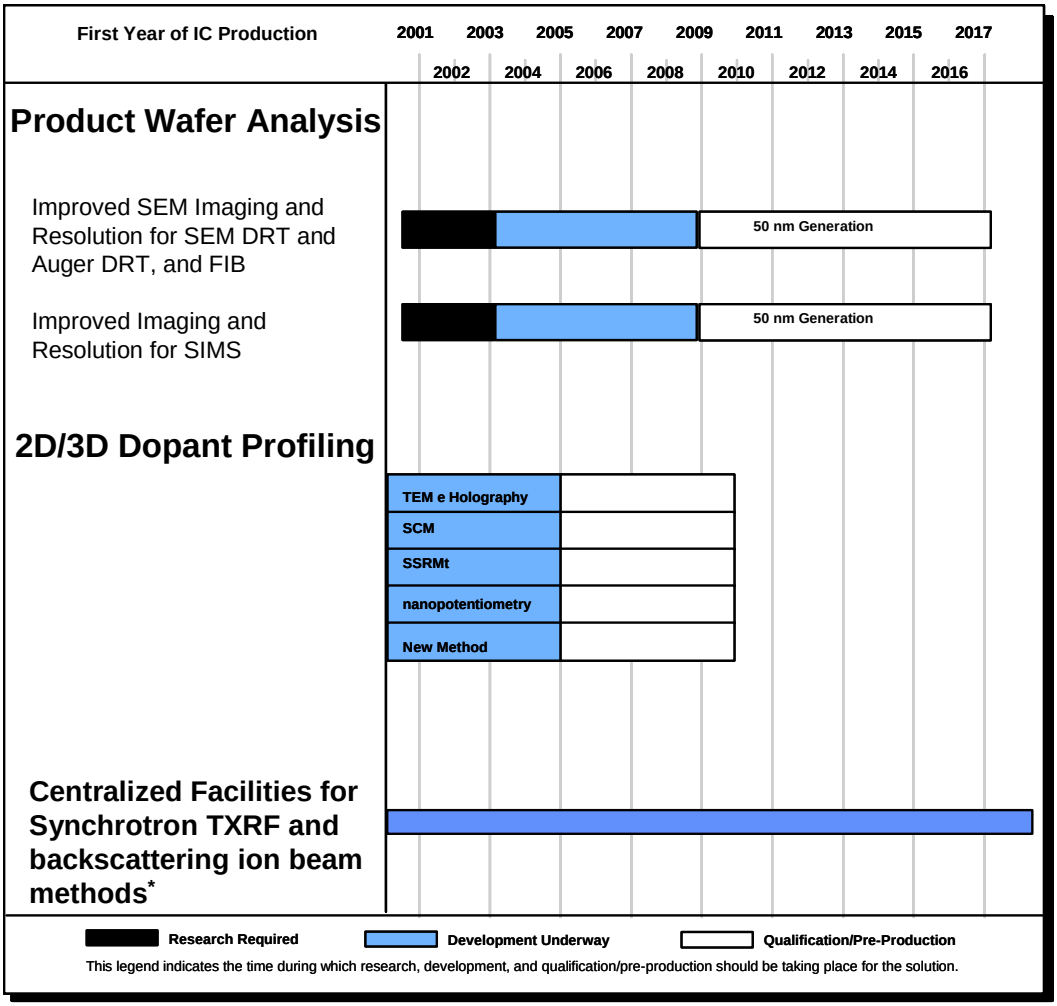
Contamination characterization methods continue to develop better detection limits and improved automation. Surface contamination on silicon wafers is often analyzed by Total Reflection X-ray Fluorescence (TXRF) and Vapor Phase Decomposition (VPD) collection based methods. VPD collection is followed by either TXRF, inductively coupled plasma mass spectrometry (ICP-MS), or atomic adsorption spectroscopy (AAS). Another approach to contamination control is being developed for *in-line* measurement. Real time sampling of wet chemical baths has been added to a mass spectrometry based detection system for measurement of trace contamination in the bath solutions. Refer to the *supplemental link for more details on TXRF*.

While these and other offline characterization tools provide critical information for implementing the Roadmap, there are still many challenges. Characterization of the high κ gate stacks to be used will be very difficult due to for example the layer-layer chemical intermixing and structure, interface roughness, and matrix-induced effects on some analytical probes and signals. In addition, as the device feature size continues to shrink, the applicability of characterizing planar structures as representative of the device feature becomes more questionable. Furthermore, the ongoing scaling make the analysis of contamination in high aspect ratio structures even more difficult.

The introduction of new materials will raise new challenges in contamination analysis, such as happened with copper metallization where the very real possibility of cross contamination has led to the need to measure bulk copper contamination down to the order of 10^{10} atoms/cm^3 and surface copper contamination even in the edge exclusion region, all because of the high diffusivity properties of this deleterious metal. The device shrinks are also tending to lower the thermal budgets of the process, so that the behavior of metal contamination and how to reduce its negative effects are changing the characterization needs. For example, low temperature processing is changing which surface contamination elements, and at what levels, need to be controlled, and therefore measured. A key example is the role of surface calcium on very thin gate oxide integrity, and the difficult challenge of measuring this surface element at the 10^8 atoms/cm^3 level. Traditional methods such as vapor phase decomposition ICPMS can have day-to-day BLANK limitations at this level. In addition, the low temperature processing is changing how the gettering of metal contamination is achieved. This change leads to challenges on how to characterize material properties to insure proper gettering.

Lastly, the introduction of new device structures, such as vertical gate and replacement gate, is expected to create new and unforeseen challenges for characterization. Also, as entirely new device materials are introduced or integrated, such as SiGe, compound semiconductors, FeRAM, MRAM, optoelectronics, and photonic crystals, unexpected challenges for

materials characterization and contamination analysis will arise. Double crystal diffraction, SIMS, and spectroscopic ellipsometry have been applied to characterization of Ge content in SiGe.



Backscattering ion beam methods refers to unique capabilities such as medium energy ion scattering, heavy ion back scattering, and other methods that are not available commercially.

Figure 64 Materials and Contamination Potential Solutions

REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar tools at different locations (internally or externally), or between model and experiment. Reference materials can be obtained from a variety of sources and come in a variety of forms and grades. Depending on the source, they may be called certified reference materials (CRM), consensus reference materials, NIST Traceable Reference Materials (NTRM®[3]) or Standard Reference Materials (SRM®*).

NIST has maintained its position as one of the leading internationally acceptable national authorities of measurement science in the semiconductor industry. NIST has also recognized the difficulty of keeping pace with the IC industry through the traditional method of need identification, instrumentation and technique development, and the development of SRMs. Several approaches allow the industry to supplement NIST's ability to supply reference materials. Commercial suppliers can submit calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark for the

[3] *These acronyms are registered trademarks of NIST.*

series of artifacts checked by NIST.[4] Another approach is the development of consensus reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM. There are several technical requirements related to reference materials and certification, as follows:

- Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be smaller than the desired calibration uncertainty.
- Reference materials may be difficult to manufacture with the desired attributes; frequently it is necessary to use specialized manufacturing techniques in short runs to obtain the samples to be measured and certified.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.
- Uncertainties in the certified value of the reference material must be less than 1/4 of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy better than 1/4 of the requirement; accuracy includes both bias and variability considerations.
- Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.

It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process tool development. Each type of reference material has its own set of difficult challenges, involving different combinations of the challenges described above.

METROLOGY INTEGRATION

Since the 1999 ITRS, the move to integrate metrology has proceeded although more slowly than expected. Metrology tool suppliers have introduced measurement stations that can be used a cluster station or be attached to a process tool. Typically, these stations are referred to as "Integrated Metrology" stations. Standardization of the hardware and communications protocols is underway, but requires significant effort to complete. One key issue is the flexibility of process tools to use Integrated Metrology Stations selected by the IC manufacturer. As 300 mm fabrication facilities become more common, integration of metrology is expected to be a key method of reducing use of test wafers and reducing wafer scrap. Traditional stand-alone, in-line metrology systems are often considered to have better capability than the integrated metrology, and may be used to monitor "Integrated Metrology Stations and *in situ* sensors. The Factory Integration Roadmap contains additional discussion of metrology Integration. A link is provided to show *key sensor technology requirements.*

As IC complexity increases and required measurement resolution shrinks, both data volumes and data rates will increase dramatically. This raw data must be converted into useful information to facilitate process control and defect reduction. To accomplish this, metrology data must be integrated into factory and enterprise-level-information systems so that it may be associated both with other data and with wafer tracking information.

There is a clear need for factory modeling of the cost effectiveness of sensors and Integrated Metrology, particularly with respect to queuing time in 300mm manufacturing. The manner in which metrology integration occurs will be greatly influenced by the implementation of advances in technology and the availability of these factory models. These include (1) introduction of advanced proximity correction and phase-shift mask technology; (2) the ramp of 193 nm, 157 nm, and next-generation lithography; (3) integration of copper and low κ interconnect processes; (4) the introduction of exotic high κ and SiGe materials; and (5) the shift from 200 mm to 300 mm wafers in high-volume production.

Physical, electrical, and parametric defects found with inspection tools must be correlated with data from other inspection tools and blended seamlessly with physical and parametric data from metrology tools. For example, CD and defect data on the reticle must be compared with CD and defect data on the wafer. This requires efficient communication between the mask supplier, pilot line, and high-volume factories. Also, bare-wafer nanotopography and defect data must be compared with yield losses on device wafers, requiring an information link between silicon suppliers and their customers. At the factory level, control of transistor drive and leakage currents will require correlation of gate length, gate width, dielectric

[4] *Use of the NTRM mark on a subsequent series of artifacts, even of the same type, requires additional verification testing by NIST.*

thickness, and dielectric constant across multiple process areas. The process cells in each area must produce nominally identical wafer states. In addition, metrology in one factory must be linked to other factories producing the same device, most of which will use "copy exactly," "copy intelligently," or "wafer-state matching" strategies.

One form of metrology integration is found in advanced process control (APC). APC applies model-based or proportional process control to reduce process variation, reduce send-ahead and tool monitor wafers, shorten learning cycles and response-times, enable better tool matching in high-volume production, improve overall equipment effectiveness, shorten development times, and ease process transfer from pilot line to factory. Due to the increasing challenge of controlling transistor characteristics as design rules shrink, future implementations of advanced process control will rely on factory-wide frameworks that allow integration of metrology data from lithography, etch, thin-film, and CMP areas. An industry-standard framework of computer integrated manufacturing (CIM) and APC will be required to support "single-wire" integration with the factory MES. In addition, frameworks will manage the complex interactions required for control in different manufacturing contexts (e.g., logic, memory, and foundry), and create a common interface for control applications. Control applications will need the bandwidth to utilize multiple data inputs from stand-alone, clustered, integrated, and in-situ metrology tools. Meeting the roadmap will eventually require that process corrections be made on a lot-to-lot, wafer-to-wafer, field-to-field, and site-to-site basis. This level of granularity will require APC-enabled process tools, with improved access to data and to the inputs required for process adjustment.

PACKAGING METROLOGY

Assembly and Packaging will continue to play a significant and increasing role in the size, performance and cost of future electronic systems. This section summarizes the metrology challenges associated with assembly and packaging. This is not an exhaustive summary, but rather attempts to highlight the most critical areas of interest.

Measurement of the stress / strain / fracture, adhesion, moisture content, materials uptake of the packaging materials continues to be a key metrology need. A new set of requirements involves the effect of the low κ material used for on-chip interconnect on packaged chip reliability. The packaging process itself imparts mechanical loading and vibration which can result in failures such as delamination of the on-chip interconnect layers. Thus packaging activities are dependent on the strength and interfacial adhesion of low κ materials in the chip.

Accelerated failure test methods representative of the application—Temperature cycling, chemical exposure, and shock and vibration are techniques that are used to accelerate the onset of failures with a view to validate the failure mechanism, and to qualify and improve the lifetime and successful operation of the product. We need to continue to ensure through test, measurement and modeling, that these acceleration methods lead to the same kinds of failures that are found in the product in its daily usage.

Measurement and modeling of interfaces—The performance, reliability, and cost of assembly and packaging are driven by our understanding of interfaces between chip and package and inside the chip, and our ability to measure and control them. For examples, the interfacial behavior of the die attach materials, mold compounds, encapsulations, adhesives, underfills, and thermal compounds are important issues. The mechanical stresses imparted on the chip can cause failure of the low κ materials used for on-chip interconnect. Our ability to accurately measure and predict interface performance will remain a key to future cost effective developments.

Refinement and validation of thermal and mechanical simulation models of packages and assemblies—We continue to push the cooling and mechanical limits of electronic products. Complete thermal and mechanical modeling, validated with measurements, is needed. This includes flow characteristics, interfacial properties, fracture mechanics, and the thermo-mechanical behavior of packages and assemblies. The validation also highlights the need for better systems and measurement techniques to locate and measure properties, defects and failures.

Material parameters—The measurement, collection and dissemination of the fundamental properties, for example, sizes, thicknesses, and temperatures of interest, of packaging materials requires constant improvement. They will also include thermal conductivity, electrical conductivity, dielectric constant and loss factor, stress/strain functions, specific heat, and micromechanical and dimensional stability over the temperature and stress ranges relevant to the application.

Material application control—The application of solders, solder alternatives, underfills, encapsulants, attachment materials, and others in the manufacture of packages and bumped chips continues to push the limits in many areas. They may include the quantity control, quality control, thickness, uniformity, voiding, thermal, and electrical and mechanical properties. Refinement in the online measurement of these parameters is needed to replace inspection, reduce process variation, control defects, and reduce waste.