INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2001 EDITION

TEST AND TEST EQUIPMENT

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TEST AND TEST EQUIPMENT

SCOPE

The 2001 Test Roadmap has been expanded from 1999 to address more of the equipment that impacts the manufacturing test process. Burn-in, wafer probe, component handler, and probe card technology trends are covered for the first time to begin to address the overall process flow beyond the challenges of the test equipment alone. In the area of test challenges, System-on-Chip (SOC) content contributed by the Japan Region is included in the supplementary material for the test chapter. The content of these areas is expected to grow and mature with future roadmap revisions.

The organization of the chapter follows that of the 1999 roadmap revision. Test technology requirements are divided into sections by key device under test market segments and design attributes, as these are the primary drivers that drive test decisions. In addition, several areas of difficult challenges are expanded to provide additional insight into the need for technology development.

DIFFICULT CHALLENGES

COST AND DESIGN FOR TEST

Test cost per unit and test equipment capital cost considerations continue to dominate manufacturing test methodology decisions. The search for low-cost equipment solutions for Design-for-Test (DFT) enabled designs that began many years ago has recently generated significant industry momentum. However, several trends limit the application of DFT techniques. System-on-chip (SOC) designs are breaking the traditional barriers between digital, analog, RF, and mixed-signal test equipment capability requirements, resulting in a trend toward highly configurable, one-platform-fits-all test solutions. Increasing demand for bandwidth and constant or shrinking final package form-factor are driving wide proliferation of high-speed serial protocols for off-chip communication. The analog nature of these interfaces and demand for device interoperability drive extensive at-speed parametric test requirements into the manufacturing environment. Finally, DFT-based test approaches require continued research to increase coverage of actual process defects through development of advanced methodologies to apply patterns based on existing fault models to designs, and identification of novel fault models. While DFT-based test methodologies are feasible in these areas, it is expected that DFT technology will continue to lag leading-edge device performance and complexity.

DFT techniques have been known for many years, but are only just becoming an industry-wide practice. Some have asked why this old technology is suddenly so crucial in today's products. For many years at-speed functional test has provided a robust methodology for high-volume manufacturing to achieve the required outgoing quality levels. It can be argued that this method is reaching its limits for several reasons, not the least of which are test development resources, manufacturing yield loss, and cost. Even if it were an affordable process to upgrade or replace manufacturing test equipment with each increase in device performance, it has proven to be impossible to avoid the resource requirements for manual test writing in the functional test environment. Test content generation may require tens of person years for highly complex designs. DFT techniques like scan and Built-in Self Test (BIST) either enable test content to be generated automatically or reduce the test content generation effort, thus drastically reducing the manual test writing task. For highly integrated devices, DFT is required to provide re-use of test collateral and avoid a geometric or exponential growth of the test development & validation effort.

With all of the industry momentum towards DFT-based designs to lower product test cost, does functional test really go away? As technology evolves, functional test equipment costs have decreased over time for a constant performance window. Test will continue to leverage the functional test methodology as one opportunity to obtain the coverage required to guarantee outgoing product quality. However, it is expected that DFT will be used when needed to limit the functional test performance envelope in production by reducing input/output (I/O) data rate requirements, enabling low pin count testing, and reducing the dependence on expensive instruments. DFT will enable manufacturers to step off the test equipment technology treadmill associated with functional test.

2 Test and Test Equipment

Fundamental research is needed to further our understanding of the fault detection environment and to identify advanced methods for applying patterns based on fault models that result in improved detection of static and dynamic defects in leading-edge semiconductor process technologies. After many years of analysis of the defect detection capabilities of test sets derived from or graded by different fault models, the single stuck-at fault model remains the most widely used model for quantifying the quality of test sets. This methodology, when used in a low-speed scan environment, has proven to be sufficient to detect most static process defects; however, more advanced vector application techniques and novel fault models are required to detect defects that only affect dynamic circuit behavior. Use of the transition and path delay fault models is growing; however, deep sub-micron circuit sensitivities and the declining capability of IDDQ testing for devices with high background current drive the need to augment with additional coverage from other fault types such as opens and bridges. Methods based on these and other novel fault models must enable high-fault coverage through heuristics that manage test pattern generation time and test equipment vector memory requirements.

As design transistor count and the application of test patterns based on advanced fault models grow, the associated scan-based DFT test data volume will experience an associated growth. It is expected that the available bandwidth at the device interface for transfer of test data will grow slower than the test data volume. This trend has a direct negative impact on production test time, and therefore manufacturing cost. Increased penetration of BIST techniques into test bandwidth limited designs will be required to manage the test data volume growth through on-chip generation of a subset of test patterns.

DFT methodologies for analog and mixed-signal test are in the early stages of development and represent a significant challenge for the industry. This is complicated by the fact that quality mixed-signal testing may be dependent on the type of application, not just the type of circuit. The trend toward higher integration with complex analog circuits drives the business need for cost-effective manufacturing test solutions. Research has begun and must continue with an increased emphasis on technology transfer to industry test applications.

The *1999 ITRS* provided the first focused requirements definition for a low-cost tester for DFT-enabled designs. The *2000 Update* contained a significant refresh of this information to clarify the requirements and reduce industry confusion in interpretation of the content. The extensive collaboration between semiconductor manufacturers and test equipment suppliers during the process of generating these requirements has demonstrated that the highly custom DFT methodologies used in individual designs converge toward a common set of tester building blocks. This significant conclusion builds confidence that a generic DFT tester capability can be designed and configured to meet the needs of the industry, rather than a series of custom point solutions.

However, in the device debug and characterization world, at-speed functional and analog test will continue to serve as a primary vehicle for root cause of design and process errors and marginalities. Traditional test equipment based methodologies are required to correlate DFT-based results to end-use environment conditions. It is expected that this equipment will not proliferate into manufacturing, but rather be used to prove manufacturing capability on lower cost high-volume testers. This represents a significant challenge to the industry, should this trend continue it would result in a reduction of the total available market for the most complex, development intensive test equipment. New methodologies for design debug and characterization must be identified to avoid rising equipment costs.

High-speed serial interfaces have been used in the communications market segment for many years. While the communications market will maintain a significant frequency lead, high-speed serial protocols will penetrate the Application Specific Integrated Circuit (ASIC) and SoC markets to support a broad range of consumer applications. This trend brings a complex test problem, previously limited to the high-speed networking environment, into the mainstream. Key learning from this market segment indicate the need to execute extensive jitter tolerance and jitter transfer testing, among others, on these interfaces. Such testing is done today in the analog domain through a rack and stack or mixed-signal tester approach. These solutions carry significant manufacturing cost considerations due to test time and equipment capital cost, and support a relatively limited number of high-speed serial ports on a single device. As these interfaces proliferate to many ports on a single device, the traditional analog test approach will fail due to the scalability of analog instrumentation. As the frequency of these interfaces continues to increase, alternative methods will need to be developed to enable manufacturing test.

Increasing pressure on consumer products for final product form factor and battery life is driving significant levels of single chip integration, blurring the lines between design types. The advent of SOC designs makes it difficult to determine whether analog circuits have been added to a fundamentally digital design (Big D / Little A) or logic circuits have been added to a fundamentally analog design (Big A / Little D). Analog complexity may vary from relatively low performance

baseband up to and including multi-gigahertz radio frequency (RF) applications. In addition to logic and analog circuitry, a true SOC design may contain a significant amount of embedded volatile and/or non-volatile memory. The combination of these circuits on a single die compounds the test complexities and challenges for devices that fall in an increasingly commodity market. Fundamental innovation in DFT and test equipment architecture is needed to balance the long test time demands of memory test with the complexities of logic and analog circuit testing. In addition, large SOC designs will be constructed from reusable mixed technology design blocks; a highly structured DFT approach will be required to enable high test coverage and test collateral reuse for embedded design blocks.

MULTI-DIE PACKAGING

Integration of customer driven "options" such as large memory arrays, while maintaining small product form factor is driving demand for multi-die packaging. Mixed technology multi-die packaging carries similar challenges as an SOC device with the added complication that the DFT opportunity is at risk because the individual die may come from different design teams or even different manufacturers. Additionally, several different test strategies, each optimized for particular technologies and normally handled individually on specialized testers, could come together in one package challenging test methods and test equipment capability. Multi-die package component yield is the product of the individual die yields and the packaging yield. This drives the desire for known-good die (KGD) from wafer probe to minimize the yield impact on the integrated multi-die packages at component test. KGD dramatically increases wafer probe defect detection requirements and challenges existing wafer probe and burn-in acceleration methodologies. Growing demand for multi-die packaging drives increased interest in enhanced wafer level test and burn-in capability and will likely lead to development of novel manufacturing process flows to maximize throughput and yield.

STANDARDS

The growing diversity of circuit types within a single die and/or package will drive an associated increase in the complexity of the manufacturing test flow. Test development standards are needed to efficiently move test content between test equipment platforms. Software tools to automate test content generation and adoption of test software standards are needed. Tools capability for digital logic designs has reached a relative level of maturity; focus is needed to bring similar capabilities to the analog domain. Today's environment of platform-unique supplier software solutions and home-grown tools for equipment programming, automation, and customization will drive unacceptable growth in test development engineering and factory integration effort. Automation of common tasks and decreasing test platform integration time demand a focus on standards to enable more efficient use of resources in line with shrinking product development lifecycles.

MODELING AND SIMULATION

As device pin count, I/O frequency, analog requirements, and power demand increase, the interface between the tester and the device-under-test (DUT) becomes increasingly complex. The worst-case combination of these characteristics requires that all instruments be physically located as close to the DUT as possible to minimize path parasitics – trade-offs will be required. Complex simulation capability is needed to allow optimization of interface layout routing and geometries versus instrument location and path performance. Simulations require detailed models of the test equipment instrument, electrical delivery path, probe card or loadboard and contactor, and the DUT. Such simulations are needed to guarantee signal and power performance at the die.

Commodity DRAM bit density growth drives an associated increase in production test throughput to maintain cost parity. Simple extensions to test parallelism will not be sufficient and may be limited by increasing DUT interface speed and accuracy requirements. Multi-bit testing, BIST, and Built-in Self Repair (BISR) will be essential to enable production throughput and yield.

Test process implementation decisions will continue to be driven by the constant trade-off between product test cost and test effectiveness. Cost pressure will continue for high performance digital and analog test equipment to manage leading edge design test requirements during the DFT technology development phase or for designs that do not lend themselves to extensive DFT solutions. Use of DFT will continue to grow with the purpose of moving test complexity on-chip and thus reducing the capability requirements, and therefore cost, of manufacturing test equipment.

Increasing device complexity in terms of transistor count, interface frequency, power consumption, and integration of diverse circuit type will drive significant challenges within the test community in the future. In the near term these

challenges center on the abilities to provide test access through highly structured DFT methodologies and to deliver high performance signals to the device through the test equipment interface. Long-term challenges lie in test equipment-to-device interfaces, advanced test methodologies, and failure diagnosis. The challenges below in Table 19 are defined in priority order.

Table 19 Test and Test Equipment Difficult Challenges—Near-term

FIVE DIFFICULT CHALLENGE ≥65 nm / THROUGH 2007	*SUMMARY OF ISSUES*
High Speed Device Interfaces	A major roadblock will be the need for high-frequency, high pin count probes and test sockets; research and development is urgently required to enable cost-effective solutions with reduced parasitic impedance. High speed serial interface speed and port count trends will continue to drive high speed analog source/capture and jitter analysis instrument capability for characterization. DFT/DFM techniques must be developed for manufacturing. Device interface circuitry must not degrade equipment bandwidth and accuracy, or introduce noise; especially for high-frequency differential I/O and analog circuits.
Highly Integrated Designs	Highly structured DFT approaches are required to enable test access to embedded cores. Individual cores require special attention when using DFT and BIST to enable test. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits. DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Reliability Screens	Existing methodologies are limited (burn-in versus thermal runaway, IDDQ versus background current increases). Research is required to identify novel infant mortality defect acceleration stress conditions
Manufacturing Test Cost	Test cell throughput enhancements are needed to reduce manufacturing test cost. Opportunities include massively parallel test, wafer-level test, wafer-level burn-in, and others. Challenges include device interfacing/contacting, power and thermal management. Device test needs must be managed through DFT to enable low-cost manufacturing test solutions; including reduced pin count test, equipment reuse, and reduced test time. Automatic test program generators are needed to reduce test development time. Test standards are required to enable test content reuse and manufacturing agility.
Modeling and Simulation	Logic and timing accurate simulation of the ATE, device interface, and DUT is needed to enable pre-silicon test development and minimize costly post-silicon test content development/debug on expensive ATE. High performance digital and analog I/O and power requirements require significant improvements to test environment simulation capability to ensure signal accuracy and power quality at the die. Equipment suppliers must provide accurate simulation models for pin electronics, power supplies, and device interfaces to enable interface design.

Table 19 Test and Test Equipment Difficult Challenges—Long-term

FIVE DIFFICULT CHALLENGES <65 nm / BEYOND 2007	SUMMARY OF ISSUES
DUT to ATE interface	Probing capability for optical and other disruptive technologies. Support for massively parallel test—including full wafer contacting. Decreasing die size and increasing circuit density are driving dramatic increases in die thermal density. This problem is further magnified by the desire to enable parallel test to maximize manufacturing throughput. New thermal control techniques will be needed for wafer probe and component test. DFT to enable test of device pins not contacted by the interface and test equipment.
Test Methodologies	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends. Logic BIST techniques must evolve to support new fault models, failure analysis, and deterministic test. EDA tools for DFT insertion must support DFT selection with considerations for functionality, coverage, cost, circuit performance and ATPG performance.
Defect Analysis	Defect types and behavior will continue to evolve with advances in fabrication process technology. Fundamental research in existing and novel fault models to address emerging defects will be required. Significant advances in EDA tools for ATPG capacity and performance for advanced fault models and DFT insertion are required to improve efficiency and reduce design complexities associated with test.
Failure analysis.	Realtime analysis of defects in multi-layer metal processes are needed. Failure analysis methods analog devices must be developed and automated. Transition from a destructive physical inspection process to a primarily non-destructive diagnostic capability. Characterization capabilities must identify, locate, and distinguish individual defect types.
Disruptive device technologies	Develop new test methods for MEMS and sensors. Develop new fault models for advanced/disruptive transistor structures.

TEST TECHNOLOGY REQUIREMENTS

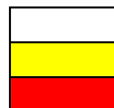
POTENTIAL YIELD LOSSES

Manufacturing yield loss associated with the at-speed functional test methodology is related to the growing gap between ATE performance and the ever increasing device I/O speed as shown in the *Overall Roadmap Technology Characteristics (ORTC) tables*. Increasing microprocessor and ASIC I/O speeds require increased accuracy for proper resolution of timing signals. While semiconductor off-chip speeds have improved at 30% per year, tester accuracy has improved at a rate of 12% per year. Typical headroom offered by testers five times faster than device speeds in the 1980s have disappeared. If the current trends continue, tester timing errors will approach the cycle time of the fastest devices. In 2001, yield losses due to tester inaccuracy are becoming a problem when using a traditional functional test methodology as shown in Table 20.

Table 20 Yield Versus Test Accuracy

YEAR		2001	2002	2003	2004	2005	2006	2007
Chip-to-Board Bus Frequency - High Performance	*MHz*	**1700**	**1870**	**2057**	**2262**	**2488**	**2737**	**3011**
Device period	*ps*	**588**	**535**	**486**	**442**	**402**	**365**	**332**
Overall ATE accuracy (OTA)	*ps*	**200**	**176**	**155**	**136**	**120**	**106**	**93**
Overall device accuracy requirement (5% target)	*ps*	**29**	**27**	**24**	**22**	**20**	**18**	**17**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow--Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



These potentially severe yield losses must be mitigated by the use of alternative test methods to at-speed functional test. DFT methodologies must mature to provide coverage of the "collateral" defects identified by at-speed functional test vectors through advanced pattern application methods and novel fault models. These methods alleviate the risk of yield loss on leading edge designs due to tester timing accuracy and provide additional benefit in reduction of tester to device interface complexity.

AUTOMATED TEST EQUIPMENT COST

ATE cost has traditionally been measured using a simple cost-per-digital pin approach. Although this is a convenient metric it is misleading because it ignores base system costs associated with equipment infrastructure and central instruments as well as the beneficial scaling that occurs with increasing pin count. Therefore, it is suggested that using the following equation for each tester segment would be a more useful way to present and evaluate the ATE cost roadmap:

$$\text{Tester Cost} = b + \Sigma(m * x)_n$$

In this equation b = base cost of a test system with zero pins, m = incremental cost per pin, and x = number of pins. Note that b scales with capability, performance, and features, while m depends on memory depth, features, and analog capability. The base cost b does vary by tester segment; however, at the present time it does not take into account special power requirements, such as for multi-site testing. The summation addresses mixed configuration systems that provide different test pin capability (i.e., analog, RF, etc.). Costs for factor b and m are expected to decrease over time for equivalent performance points. Refer to Table 21

Table 21 ATE Cost Parameters

TESTER SEGMENTS	*b*	*m*	*x*
	BASE COST	*INCREMENTAL COST PER PIN*	*PIN COUNT*
	K$	*$*	
High-performance ASIC / MPU	**250–400**	**2700–6000**	**512**
Mixed-signal	**250–350**	**3000–18,000**	**128-192**
DFT Tester	**100–350**	**150–650**	**512-2500**
Low-end Microcontroller / ASIC	**200–350**	**1200–2500**	**256-1024**
Commodity Memory	**200+**	**800–1000**	**1024**
RF	**200+**	**~50,000**	**32**

BEYOND PRICE PER PIN

ATE cost is one element of the overall cost of manufacturing test, although it has historically comprised a very large percentage. As with the silicon fabrication and package assembly portions of the semiconductor manufacturing process, the total cost of operation for wafer sort and final test include the cost of associated manufacturing cell equipment, materials, labor, floorspace, equipment support, and manufacturing cell efficiency. Since the publication of the *1997 NTRS*, there has been a great deal of emphasis placed on test cost by ATE suppliers, semiconductor companies, and even EDA vendors.

The *1997 NTRS* and *1999 ITRS* used the graph shown in Figure 19 to describe the test cost challenge due to equipment capital cost. This model was originally based on test cost trends in the high performance microprocessor product segment and has been inappropriately applied to the broad market. The original model projected test cost forward based on the assumption that historical trends continued into the future. These trends included constant tester per-pin capital cost per product generation and increasing device test times associated with the device transistor count trends. In the years since publication of this cost model, significant effort has been applied to change the historical trends and begin to push the test cost model trend downward.

Changing these historical trends has been a joint effort between the ATE and Semiconductor Manufacturing industries. Equipment costs have begun to trend downward due to the combination of equipment cost improvement and reduction in equipment capability requirements. In addition, Semiconductor Manufacturers have placed increased emphasis on manufacturing cell throughput, increasing the use of parallel test and reducing device test time. This has resulted in an overall reduction of the impact of equipment capital cost on the overall cost of test.

However, these gains have been seen in some market segments while others continue to struggle. The relative high cost of analog and RF test instruments and the long test times associated with testing of these circuits remains a key challenge. For products in some market segments, test may account for more than 70% of the total manufacturing cost – test cost does not directly scale with transistor count, die size, device pin count, or process technology.

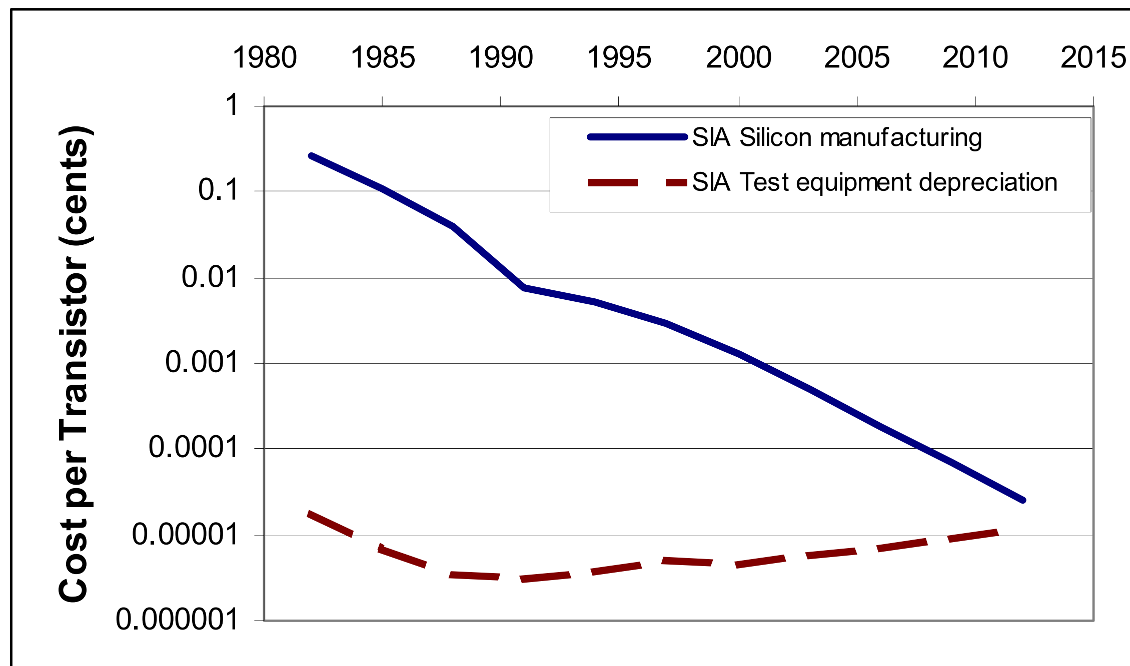


Figure 19 1997 Microprocessor Cost of Test Trend Model

IMPORTANT TRENDS

DFT has been used early in the design process to ensure test coverage and reduce test development time. Initial resistance by the design community to consider testability early in the design process has been easing over time and may be further aided as the ATE and EDA environments begin to converge in the near term. To lower test cost it is critical to use DFT methodologies to enable use of lower cost lower capability equipment, enable reuse of existing equipment, and enable higher manufacturing throughput. BIST and DFT are mainstream in high-end digital logic designs, penetration into analog and SOC designs will begin in earnest over the near term. Key to success will be the availability of low-cost equipment built to take advantage of the benefits offered by design testability features.

TEST AND YIELD LEARNING

In addition to differentiating salable product from defective and premium sorts from standard ones, test provides another major service for the semiconductor industry. Today the best tool for analysis of failure mechanisms in the manufacturing process is the test equipment. Time-to-yield, time-to-quality, and time-to-market are all gated by test. The feedback loop derived from the test process is the only way to analyze and isolate many of the defects in today's processes. Similarly, test is the main source of feedback regarding unacceptable parametric variations and design-process interactions. Test must continue to support cost-effective process measurements, defect isolation and failure root cause determination. The emergence of complex microprocessors as technology leaders in place of RAM devices is making these goals harder to realize.

The migration of CMOS technology towards 65 nm feature sizes will severely challenge the traditional failure analysis process. Hardware-based physical failure analysis, comprising the steps of fault localization, deprocessing, and physical characterization/inspection, will remain an important process; however, alternatives are needed. The need for alternatives is driven by such factors as increased circuit sensitivity to failure, which requires finding smaller, more subtle defects; tighter pitches, which require greater spatial resolution; and increasing numbers of metal layers, which along with flip-chip packaging force the use of backside analysis. These factors will combine to make the physical failure analysis process too slow and difficult to be relied upon as a routine analysis procedure. A key alternative/supplement to traditional hardware-

based fault localization is software-based fault localization, the need for which is especially acute and requires major breakthroughs. As the challenges to physical failure analysis techniques become more severe, signature analysis techniques for mapping from rapidly gathered data, such as product-level electrical behavior or in-line or test-structure measurements, to the underlying physical cause must also be developed. Such developments, if proven successful, will relegate physical failure analysis to a sampling/verification role.

To play even a sampling/verification role, physical failure analysis needs improvements to existing tools/techniques to keep pace with technology and, in some cases, requires new breakthrough techniques. In addition, new and improved hardware fault localization tools are needed to support and supplement software-based fault localization. Developments in software-based fault localization and signature analysis, especially, demand major shifts in capability, driven by drastic changes in analytical method. They require major efforts of industry, academia, and the national laboratories, as well as the analytical equipment suppliers. These needs are further detailed in the following prioritized list.

1. *Software-based fault localization methodologies and tools—*Such tools and methodologies are needed to handle diagnostics for fails detected by all major test methodologies, such as scan-based and BIST-based voltage test, functional, IDDQ and AC (delay) test. Methods are also needed to handle core-based designs, analog circuits, and varied design methods, including high-performance methods using dynamic logic and low power methods. Localization of AC or performance fails is especially important. These tools should be able to locate defects to single transistors or to sections of conductor no longer than 10µm. They must also handle all realistic physical defects, including resistive bridges, resistive contacts/vias and opens. Methods to diagnose problems related to parametric (non-defect) failure mechanisms must also be developed. DFT techniques such as BIST must be designed to support the necessary data gathering. IDDQ measurement devices need to support the accuracy levels required by diagnostics. Tester response data capture capabilities and data management systems must meet the demands of these methodologies. Specifically, ATE should allow for unlimited collecting of scan data at the model scan vector rates predicted in Table 28 for DFT testers, e.g., 50MHz in 2001. The diagnostic data collection should not add significantly, e.g., more than a few seconds, to overall test time.
2. *Hardware-based fault localization tools to complement and supplement those above as appropriate—*The spatial resolution of these techniques is predominantly fixed at about 0.5 µm by the near infrared light used for imaging and overlay (e.g., Picosecond Imaging Circuit Analysis [PICA], Thermally-Induced Voltage Acceleration [TIVA], etc.). Since no other method exists for backside imaging, this constraint must be dealt with by integrating hardware based fault isolation tools with improved computer aided design (CAD) capability for overlay and signal tracing. ATE and DFT must support the needs of these tools, e.g., to loop efficiently through a subset of the test vectors for PICA analysis.
3. *Non-destructive inspection techniques beyond optical microscopy (e.g., X-ray tomography)* that offer high resolution without sacrificing throughput and without subjecting subtle defects to potentially destructive chip delayering processes.
4. *Signature analysis techniques* to significantly reduce or eliminate the need for physical failure analysis. Statistical methods are needed first to select failing die of a particular class to accurately pre-sort and prioritize input to physical failure analysis. In the longer term, methods must be developed to point to root cause based on test information without resorting to physical failure analysis. A key enabling technology is characterization test methods that distinguish defect types from one another. Integration of electrical characterization with layout data and test-structure/in-line test results are also key capabilities. Data management strategies are required to collect consistent data across multiple products containing the same cores.
5. In the area of *deprocessing, wet and dry delayering processes for new films*, focused ion beam cross-sectioning, milling and deposition capabilities and depackaging processes require advancement. In the area of *inspection/defect characterization*, SEM and acoustic microscope resolution, X-ray radiography resolution, E-beam test resolution and robustness to crosstalk and internal DC micro-probing capabilities need to be improved for characterizing individual circuit or transistor parameters or isolating leakage paths.

The following is a list of potential opportunities to address the revolutionary needs for test and yield-learning:

- Improvements in fault localization techniques based on matching tester pass/fail response to expected response, including those based upon voltage-test results and IDDQ test results
- Integrating layout-based likelihood of defect occurrence information and/or in-line test results into fault localization

- Localization using multiple physical measurement points, e.g., triangulating defect current source using measurements at multiple points on the supply grid
- Fault-distinguishing, diagnosis-oriented test generation
- DFT/BIST/ATE architectures to facilitate diagnostic data collection
- Continuous improvements in non-invasive techniques for monitoring timing-varying signals during chip operation, such as Laser Voltage Probe (LVP) and Picosecond Imaging Circuit Analysis (PICA)
- Characterization methods based on product level electrical measurements, such as functional speed or IDDQ, versus test conditions, such as voltage or temperature
- Tighter coupling between design tools, especially timing tools, and diagnosis
- Integration of process-monitoring test structure information into diagnostics

IDDQ TESTING

Normal background leakages (both the amplitude and variability) are increasing to the point where IDDQ testing as it has historically been practiced will face difficulty in the future. IDDQ testing must change to continue to enable defect detection. Alternative solutions must be developed to provide the same benefits in the face of the rising background leakage currents of future technologies. IDDQ provides a rich source of information about a manufactured chip and in many cases today plays a vital role in both defect detection and characterization.

The Table 22 shows projected IDDQ values for performance-oriented products in future technologies. These values should not be precisely interpreted; instead they are meant to provide relative values as technology scales. These numbers may be significantly lower (e.g., three orders of magnitude) for low-power technologies. These ranges are derived from the maximum device I_{off} (from 2001 ITRS *Process Integration* chapter, Logic Technology Requirements Tables [high performance, low operating power, and low standby power tables]), transistor counts (from *ORTC, Table 1g-1h*), typical W/L ratios, and assuming a percentage of off transistors. It is assumed that the IC is designed appropriately to enable IDDQ testing.

Table 22 Projected Performance-Oriented IC IDDQ Values

YEAR	MAXIMUM IDDQ
2001	**30–70 mA**
2003	**70–150 mA**
2005	**150–400 mA**
2008	**400 mA–1.6 A**
2011	**1.6–8 A**
2014	**8–20 A**

Note—all table values assume 25°C

Not only are IDDQ values projected to increase in magnitude, but also the variability of IDDQ (for a given technology and product) is expected to be high. For example, although the IDDQ values in Table 22 represent the maximum, typical values could be significantly lower. It is important to better understand the components of this variability and to develop new test techniques so that this variability can be tolerated.

Below is a list of potential opportunities (both test methods and design-for-test techniques) for continuous use of IDDQ testing.

- Use of "Delta IDDQ" or "IDDQ Ratios" test methods
- Substrate biasing to control V_t
- Processing changes to have higher V_t (either for all devices or selected ones) or lower V_t variance
- IDDQ testing at low temperature
- Power supply partitioning at chip level and use of multiple power sources

- Use of large "footer" devices that limit leakage currents in the transistor path
- IDDQ measurements for multiple V_{dd} voltages
- Transient and charged-based I_{dd} techniques
- IDDQ limits determined based on comparisons with neighboring die
- IDDQ limits determined as a function of other parametric measurements (e.g., speed)
- IDDQ measured simultaneously on a set of power supply pads
- Built-in IDDQ sensors (potentially self-calibrating) or other on-chip measurement aids

IDDQ has been an important failure analysis and characterization technique. Physical failure analysis relies on IDDQ for defect localization and defect type identification. In addition, there is important information about defective circuit behavior in the relationship between IDDQ and conditions such as temperature, voltage, and circuit state. As IDDQ goes up, however, some loss of diagnostic effectiveness using traditional techniques is possible.

There is also a need to improve the rate at which IDDQ measurements can be performed. Test equipment improvements or supported test fixture aids are preferred. Furthermore, IDDQ measurement resolution and accuracy at high currents must improve—particularly for emerging “signature-based” techniques.

HIGH-FREQUENCY SERIAL COMMUNICATIONS

Recently, the use of gigabit serial input/output buffers has grown beyond the original long-haul voice and data communication market segment. Serial communication interfaces are being widely adopted into back plane applications, short and long-haul communications, mass storage access networking, and computer peripherals. The rapid deployment of gigabit-rate serializer and deserializer (SerDes) in ASICs and other ICs for applications (such as SONET/SDH, Gigabit Ethernet, Fiber Channel, Serial ATA, Infiniband, FlatPanel, Link, and source synchronous rapid IO) presents many challenges for ATE.

At the present time, testing the functionality of high-performance serial interfaces must be done by using expensive, stand-alone pattern-generators and bit-error-rate detectors. Excessive test time and cost makes this approach impossible for volume production. Without proper test methodology and equipment available, many IC manufacturers are forced to use very primitive testing techniques (such as loopback or golden device) with reduced fault coverage. In the near term there is an urgent need for ATE manufacturers to design multi-port, gigabit rate instruments and integrate them into test systems, including control software. However, development of effective DFT methodologies is required to reduce manufacturing test cost and enable efficient testing for high port count devices. Table 23a and b show the technology requirements for high-frequency serial communications test.

IMPORTANT AREAS OF CONCERN

1. *Frequency*—The frequency of Si CMOS and BiCMOS serial communication devices, such as SONET, Gigabit Ethernet, and Fiber Channel, is rapidly exceeding 2.5 Gbits/s and approaching 3.125 Gbits/s in 2001. With the deployment of SiGe technology, the current stand-alone 10 Gbits/s serial ports will be integrated into CMOS ASICs as early as 2002. Concurrently, SiGe, GaAs and InP technologies continue to lead the way into the 40Gbits/s domain. As predicted in the *Test* chapter of the *1999 ITRS*, development efforts have been intensified for high-speed, low-voltage swing, low-timing skew, differential source, and capture instruments yet equipment capability continues to lag leading edge interface performance.
2. *Port Count*—The lower threshold voltages of CMOS (0.7V) and SiGe (0.8V) technologies compared to GaAs (1.4V) technology have made low-power gigabit IO a reality by using 1.5V–1.8V power supplies. Low power enables massive integration into ASICs and SOCs. Currently in 2001, ASICs with 20–80 pairs of multi-gigabit transmitters and receivers are being produced by several IC makers. This port count will exceed 100 pairs in 2002. With such a high port count, the traditional rack-and-stack approach with stand-alone instruments becomes impractical. A multi port ATE solution is required to handle so many serial ports on a single device.
3. *Cost Factor*—Traditionally, most multi-gigabit transceivers were designed as high-performance, high-priced, and high-margin devices with a low level of integration and relatively low production volume. With the introduction of low-cost, low-power CMOS/SiGe macro cells, gigabit transceivers have become valued additions to many high volume and low priced (even commodity) devices. In addition to high port count, a cost-efficient ATE solution that

can test all serial ports concurrently is essential for production. The constant trade-off between performance and integration level results in the separation of SerDes devices into two categories: high-performance-level serial transceivers and high-integration-level serial macro-cells. The test method for each type should be selected with cost in mind. The economies of high-performance SerDes products typically allow a more traditional equipment instrument-based test approach. But reliable DFT features or other low-cost test techniques are critical for large port count SerDes deployment.

4. *Jitter Measurement*—The jitter generated by the transmitter is the key parameter to guarantee transmitter quality. Currently, jitter measurement capability on ATE is in its infancy—there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth, and test time requirements for high performance interfaces. For the dominant 2.5 Gbit/s data rate in 2001, it is normal for a 2.5 Gbps SerDes to have a peak-to-peak jitter lower than 40ps, which requires instruments with <5ps peak-to-peak jitter noise floor. A digital signal of 2.5Gbit/s has a frequency spectrum up to 8~10GHz, associated jitter measurement instruments must provide this analog bandwidth to avoid adding erroneous data-dependent jitter to the measurement. Most existing instruments for jitter measurements take more than 20 seconds to capture jitter from a high-speed data stream. Although it is faster to measure jitter based on the device clock, many of these designs do not provide direct access to the internal clock. In that case, jitter can only be measured from the data stream. Since routing of such a high frequency clock is impractical in most cases, a DFT approach to measure the jitter on chip is preferred. This is yet to be developed in the multi-gigabit domain.
5. *Jitter Injection*—Jitter tolerance measures the level of jitter on the input signal that the receiver can tolerate before communication quality in terms of bit-error-rate (BER) is degraded. This is a key specification for receiver (Rx) noise immunity. To conduct a jitter tolerance test, jitter must be deliberately injected into the data stream in a controlled fashion. Currently, there is no integrated ATE solution that has this capability in the speed range required by today's high performance designs.
6. *Asynchronous and Low Jitter Clocking*—A jitter generation test measures the jitter out of a device or system in the absence of any input jitter. To conduct this test, input jitter must be minimized. This implies that a high-quality, low-jitter clock is needed. Typically, the clock generated by a standard tester digital channel contains too much jitter for effective measurement of jitter generation for gigabit SerDes. To accurately measure the jitter generated from the device, the reference clock provided to the SerDes needs to be of very low jitter (for example <5ps rms). Such clock sources are becoming available as special pin card options. Asynchronous interface testing requires the capability for these special pin cards to run at a different rate, independent from the tester. For SerDes embedded in large ASICs, asynchronous testing is needed to identify on-chip crosstalk and ground bounce problems.
7. *Non-deterministic Phase*—Most receivers in serial communication use clock and data recovery circuits (CDR) to extract the clock from a data stream. The phase of the recovered data is not necessarily fixed from part to part, or even from one reset to the next. Highly flexible timing and clocking schemes are required to accommodate clock recovery latency variation, phase alignment, and frame alignment.
8. *DFT*—Basic DFT for SerDes modules relies on internal serial and parallel loopback. Additional DFT including a built-in Pseudo-Random-Bit-Sequence (PRBS) generator and a bit-error (BER) checker are required to provide increased defect coverage. When used in conjunction with serial internal/external loopback these features provide at-speed functional test without the need for external stimulus and capture instruments. Innovative research for DFT techniques for jitter generation and jitter tolerance testing is needed.

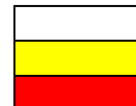
Table 23a High Frequency Serial Communications Test Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
High–performance-level serial transceivers							
Serial data rate (Gbits/s)	**10**	**10**	**40**	**40**	**40**	**40**	**40**
Maximum reference clock speed (MHz)	**667**	**667**	**2500**	**2500**	**2500**	**2500**	**2500**
High-integration-level backplane and computer I/O							
Serial data rate (Gbits/s) Production	**2.5**	**3.125**	**3.125**	**10**	**10**	**40**	**40**
Introduction	**3.125**	**—**	**10**	**—**	**40**	**—**	**—**
Maximum port count at Production frequencies	**20**	**100**	**200**	**100**	**200**	**100**	**200**
at Introduction frequencies	**—**	**—**	**20**	**—**	**20**	**—**	**—**
Maximum reference clock speed (MHz) Production	**166**	**166**	**166**	**667**	**667**	**2500**	**2500**
Introduction	**—**	**—**	**667**	**—**	**2500**	**—**	**—**

Table 23b High Frequency Serial Communications Test Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
High–performance-level serial transceivers			
Serial data rate (Gbits/s)	**40**	**80**	**80**
Maximum reference clock speed (MHz)	**2500**	**5000**	**5000**
High-integration-level backplane and computer I/O			
Serial data rate (Gbits/s)	**40**	**40**	**40**
Maximum port count	**200**	**200**	**200**
Maximum reference clock speed (MHz)	**2500**	**2500**	**2500**

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known



High-performance ASIC Test Requirements

High-performance ASIC test requirements, Table 24a and b, illustrate the demands that automatic test equipment (ATE) manufacturers must meet in terms such as pin count and frequencies in order to test the digital portions of today's ASICs. It is unlikely that ATE will ever be required to meet all of these demands on all pins simultaneously. For example, the highest off-chip data frequencies will probably occur on a relatively small number of high frequency serial interfaces operating at 1.25, 2.5, 10, or 40GHz rates, while the majority of device pins will operate at the lower frequencies shown in the tables. It is expected that integration of high-frequency serial differential I/O buffers will result in a slowing of the device pin count growth trend to approximately 3000 by the year 2016.

The off-chip frequencies shown in the tables are for signal pins other than the high-frequency serial interface pins. For example, data may enter the ASIC on a broad bus at 156 Mbps, and exit on a narrow bus at 2.5 Gbps.

The number of externally stored, non-scan test vectors has not been shown. This number is typically around 32M in 2001, and could climb toward 1000M in the future if not constrained. Since external high-speed memory for test vectors can greatly increase the cost of ATE and result in manufacturing cell throughput reduction due to long vector load times, there

is an urgent need for DUT designs incorporating DFT and BIST in the near future. This has been incorporated in the DFT tester section.

High-frequency clocks are often generated on-chip using phase-locked-loop (PLL) oscillators. These are stimulated by clock signals from the ATE at much lower frequencies, but are required to have very low jitter. Typically a special tester clock pin is needed to provide jitter on the order of 10ps RMS with an accuracy of ±20ppm for SONET, and ±100ppm for other serial communications systems.

Today's ASICs are rapidly transforming into SOC designs that incorporate intellectual property (IP) such as memories and analog circuits. Therefore the test requirements contained in Table 24a and b should be combined with the mixed-signal and memory test and high frequency serial requirements when determining ATE requirements.

Table 24a High Performance ASIC Test Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Off-chip data freq. MHz NRZ (see note).	**800**	**900**	**1000**	**1100**	**1200**	**1300**	**1400**
Overall timing accuracy (% period)	**± 5**	**±5**	**±5**	**± 5**	**±5**	**±5**	**±5**
Special clock pin RMS jitter ps	**10**	**10**	**5**	**5**	**5**	**5**	**5**
Signal pk-pk range V	**1.2–3.3**	**1.2–3.3**	**0.9–3.3**	**0.9–2.5**	**0.8–2.5**	**0.7–2.5**	**0.6–2.5**
Power/device. DC with heat sink W	**130**	**140**	**150**	**160**	**170**	**170**	**170**
Tester cost per high-frequency signal pin $K	**1–4**	**1–3**	**1–3**	**1–3**	**1–3**	**1–3**	**1–3**
Maximum number of I/O signal pads. *Power and ground could double the number of pads for wafer test.*	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**

NRZ—nonreturn-to-zero waveform (NRZ rates are often referred to as Mbits/s)

Table 24b High Performance ASIC Test Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
Off-chip data freq. MHz NRZ (see note).	**1500**	**1800**	**2000**
Overall timing accuracy (% period)	**±5**	**±5**	**±5**
Special clock pin. RMS jitter ps	**2**	**2**	**2**
Signal pk-pk range V	**0.6–2.5**	**0.6–2.6**	**0.6–2.7**
Power/device. DC with heat sink W	**180**	**190**	**200**
Tester cost per high-frequency signal pin $K	**2–4**	**3–4**	**4–4**
Maximum number of I/O signal pads. *Power and ground could double the number of pads for wafer test.*	**2400**	**2700**	**3000**

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

HIGH-PERFORMANCE MICROPROCESSOR TEST REQUIREMENTS

With the focus to shift microprocessor test content from a pure at-speed functional test approach to a more diverse test suite encompassing DFT and BIST techniques many of the traditional manufacturing test challenges are changing. Traditional challenges such as data rate and timing accuracy are being replaced by characteristics like test data volume and power and thermal management. This is not to say that the traditional challenges associated with scaling of at-speed functional test are going away, but rather that there is a shifting emphasis on these parameters to the post-silicon device debug and validation environment. DFT methods have begun to minimize the impact of key test limitations associated with tester data rate and accuracy scaling.

As a result, the microprocessor trends shown in Table 25a and b more accurately reflect post-silicon efforts than manufacturing need. Manufacturing challenges associated with DFT methodologies are covered in the DFT tester section.

This basic shift in test methods will have a dramatic impact on the industry over the near term. It is not clear today how the leading-edge equipment required for post-silicon debug and validation will be economically viable provided increasing development resources and declining equipment demand.

Over the near term it is expected that equipment capability will scale to match device parameters like data rate and power consumption. Timing accuracy requirements will demand new approaches to specification definition and calibration methodologies. It is unclear whether test equipment design innovation will find answers to the nagging issues of timing accuracy and adaptation to emerging interface protocols over the long term. However, it is clear that functional test will not be possible without the intervention of novel technologies as the available timing margin will be overtaken by timing inaccuracies.

Algorithmic Pattern Generator (APG) capabilities are still required for testing of embedded memory on a microprocessor. However with the advent of BIST for most large arrays, APG performance scaling has essentially frozen at 1999 levels even as the total number of embedded memory bits continues to increase.

Significant progress has been made within the last two years to address the growing concerns around power supply bandwidth and dynamic response to current demand transients. Continued research in this area and in alternative methods will be required to address future requirements.

Table 25a High Performance Microprocessor Test Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Pin count							
Pin count I/O signal channels (maximum pins) [1]	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Pin count power and ground (maximum pins)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**

Table 25a High Performance Microprocessor Test Requirements—Near-term (continued)

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Busses							
Clock input frequency (MHz) [2]	1066	1200	1200	1200	1200	1200	1200
Clock accuracy (ps) [3]	47	42	42	42	42	42	42
Off-chip bus data rate (Mbits/s)	800	1200	1600	2400	3200	4800	6400
Accuracy OTA (ps)	63	42	31	21	16	10	8
Bi-directional I/O	Yes	Yes	No	No	No	No	No
Uni-directional I/O	No	No	Yes	Yes	Yes	Yes	Yes
Source synchronous	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Differential	No	No	Yes	Yes	Yes	Yes	Yes
Self clocked	No	No	No	No	Yes	Yes	Yes
Embedded memory (Mbits)	256	512	1024	2048	4096	4096	8192
APG frequency (MHz)	200	200	200	200	200	200	200
Algorithmic pattern generator (#X, Y addresses)	16	16	16	16	16	16	16
Algorithmic pattern generator (#Z addresses)	4	4	4	4	4	4	4
Power Supplies							
High current power supply voltage range (volts) [4]	1.3–2.5	1.1–2.5	0.9–2.0	0.9–2.0	0.9–2.0	0.7–1.8	0.7–1.8
Low current power supply voltage range (volts)	1.3–3.3	1.1–3.3	0.9–3.3	0.9–3.3	0.9–3.3	0.7–3.3	0.7–3.3
Power supply accuracy (% of programmed value AC+DC)	10	10	10	10	10	10	10
High current power supply maximum current (A)	95	115	146	150	154	204	211
Patterns							
Vector memory (Meg–vectors per pin)	64	128	128	256	256	512	512
Vector memory load time (minutes)	15	15	15	15	15	15	15
Independent pattern management (# of patterns)	>1000	>1000	>1000	>1000	>1000	>1000	>1000
Reliability							
MTBF (hours)	1150	1208	1268	1331	1398	1468	1541
MTTR (hours)	1	1	1	1	1	1	1
Availability (%)	98	98	99	99	99	99	99
Setup time (hours)	0.4	0.4	0.3	0.3	0.2	0.2	0.2

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

Notes for Table 25a and b:

[1] Maximum pin count is for debug tester purposes. Debug testers typically utilize the higher pin counts.

[2] Tester should be capable of handling RAMBUS type of date rates and protocols. Characterization testers need to meet full data rate requirements. Production tester accuracy of measurement of "output-to-output" will be critical.

[3] The tester needs to supply the clock as a bypass.

[4] The power supply should be capable of handling 6000 µF, and current switching of 2× maximum current. The circuit can wakeup between 1–20 cycles of the CPU clock.

Table 25b High Performance Microprocessor Test Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
Pin count			
Pin count I/O signal channels (maximum pins) [1]	**1280**	**1408**	**1472**
Pin count power and ground (maximum pins)	**2560**	**2816**	**2944**
Busses			
Clock input frequency (MHz) [2]	**1200**	**1200**	**1200**
Clock accuracy (ps) [3]	**42**	**42**	**42**
Off-chip bus data rate (Mbits/s)	**9600**	**14400**	**21600**
Accuracy OTA (ps)	**5**	**3**	**2**
Bi-directional I/O	**No**	**No**	**No**
Uni-directional I/O	**Yes**	**Yes**	**Yes**
Source synchronous	**Yes**	**Yes**	**Yes**
Differential	**Yes**	**Yes**	**Yes**
Self clocked	**Yes**	**Yes**	**Yes**
Embedded memory (Mbits)	**16384**	**16384**	**16384**
APG frequency (MHz)	**200**	**200**	**200**
Algorithmic pattern generator (#X, Y addresses)	**64**	**64**	**64**
Algorithmic pattern generator (#Z addresses)	**16**	**16**	**16**
Power Supplies			
High current power supply voltage range (volts) [4]	**0.7–1.8**	**0.5–1.5**	**0.5–1.5**
Low current power supply voltage range (volts)	**0.7–3.3**	**0.5–3.3**	**0.5–3.3**
Power supply accuracy (% of programmed value AC+DC)	**10**	**10**	**10**
High current power supply maximum current (A)	**231**	**354**	**388**
Patterns			
Vector memory (meg–vectors per pin)	**1024**	**4096**	**4096**
Vector memory load time (minutes)	**15**	**15**	**15**
Independent pattern management (# of patterns)	**>1000**	**>1000**	**>1000**
Reliability			
MTBF (hours)	**1722**	**2038**	**2344**
MTTR (hours)	**1**	**1**	**1**
Availability (%)	**99**	**99**	**99**
Setup time (hours)	**0.2**	**0.2**	**0.2**

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

LOW-END MICROCONTROLLER TEST REQUIREMENTS

Low-cost microcontrollers continue to thrive in today's competitive market. Sales of 8-bit microcontrollers alone almost reached the $10B mark in 2000. The need for connectivity in both the wired and wireless arena have driven the development of many new building blocks for the microcontroller, including USB, TCP/IP, and RF interfaces. Lower flash memory costs are resulting in a move from the traditional mask ROM to integration of flash memory technology. Current applications utilizing microcontrollers include household appliances, entertainment devices, games, motor controllers, and security systems.

The difficult challenges for microcontroller testing are in the area of "test cost" and the increasing integration level. Test requirements for microcontrollers are rapidly merging with SOC requirements. The increasing level of integration results in microcontrollers receiving an insertion on a mixed-signal tester or being moved onto the new SOC type of testers. Table 26a and b shows the test characteristics that are unique to testing of microcontrollers.

Table 26a Low-end Microcontroller Test Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Tester Characteristics							
Overall timing accuracy (% of period)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
RMS clock jitter (ps)	**100**	**75**	**75**	**50**	**50**	**50**	**40**
External test vectors (M) [1]	**8**	**12**	**12**	**12**	**12**	**16**	**16**
Tester cost range ($K/per pin)	**1.0–4**	**1.0–3**	**0.8–3**	**0.8–3**	**0.6–3**	**0.6–3**	**0.4–2.5**
Reliability–MTBF (hrs)	**2500**	**3000**	**5000**	**6000**	**7000**	**8000**	**9000**
DPS maximum voltage (V)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Maximum DPS in tester	**32**	**48**	**48**	**64**	**64**	**64**	**64**
Maximum devices for parallel testing [2]	**32**	**32**	**48**	**48**	**48**	**64**	**64**
Maximum tester pins	**1024**	**1024**	**1536**	**1536**	**1536**	**2048**	**2048**

Notes for Table 26a and b:

[1] Without BIST or DFT. number will be smaller if acceptable BIST and/or DFT solutions are developed

[2] This category is for parallel testing of microcontrollers, and is not to be confused with parallel testing of memories

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

Table 26b Low-end Microcontroller Test Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (NM)	45	32	22
MPU / ASIC ½ PITCH (NM)	45	32	22
MPU PRINTED GATE LENGTH (NM)	25	18	13
MPU PHYSICAL GATE LENGTH (NM)	18	13	9
Tester Characteristics			
Overall timing accuracy (% of period)	4	4	3
RMS clock jitter (ps)	40	30	25
External test vectors (M) [1]	16	16	24
Tester cost range ($K/per pin)	0.3–2.5	0.3–2.0	0.2–2.0
Reliability–MTBF (hrs)	10K	12K	15K
DPS maximum voltage (V) [2]	8	8	8
Maximum DPS in tester	64	96	128
Maximum devices for parallel testing	64	96	128
Maximum tester pins	2048	3K	4K

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

MIXED-SIGNAL TESTING

The trend toward more system functionality on a single piece of silicon will increasingly blur the lines between traditional digital, analog, RF/microwave and mixed-signal devices. This trend will drive test equipment toward a single platform solution that can test any device structure on a single piece of silicon. The digital requirements for mixed-signal test equipment are equivalent to those for purely digital chips and are shown in the tables for the associated market segment. Consequently, ATE must be modular and expandable across the entire spectrum from digital-only to the full integration of high performance analog/RF/microwave instruments. The analog test issues and test technology limiters are higher bandwidth, higher direct conversion sampling rates, higher dynamic range, lower noise floors and seamless integration of digital and analog instruments.

The mixed-signal test equipment requirements in Table 27a and b focuses on test instruments rather than specific IC device applications. Current Analog/RF/Microwave testing methodologies require performance-based measurements (i.e., using external outside-the-chip instruments); therefore, instrument needs reflect the increasing device performance predicted in the process and packaging technology roadmaps. The complexity of applications is also forcing specialized instrument designs focused on a particular device application. This complexity increases the number of instruments in a given test system, which increases cost and creates significant configuration-management issues for equipment that must be shared across multiple products. This trend of increasing instrument numbers, complexity, and performance is expected to continue but can not be allowed to drive up the cost of test.

Analog DFT techniques are enabling each element in an analog chain to be tested independently reducing the requirement for complex functional tests and improving test reuse. No proven alternative to performance-based analog testing exists and more research in this area is needed. Analog BIST has been suggested as a possible solution and area for more research. The current state of analog DFT lies mainly in loopback techniques and direct access test methodologies. Fundamental research is needed to identify DFT techniques that enable reduction of test instrument complexity or elimination of the need for external instrumentation.

IMPORTANT AREAS OF CONCERN

1. The analog/RF/microwave signal environment seriously complicates load board design and test methodology. Noise, crosstalk, signal mixing, load board design, and ATE software issues will dominate the test development process and schedule.
2. Gigabit/second (2.5 to 10Gb/s) serial ports are being used for off-chip communication. These ports may be used on a single ICs along with mixed-signal functions. Test requirements for these ports can be found in the High Frequency Serial section.
3. Parallel test of all analog functions is needed to reduce test time, increase manufacturing cell throughput, and reduce test cost. This requires multiple instruments with fast parallel execution of DSP test algorithms (FFTs etc). Parallel test has been used for many years to test Memory and high volume Digital Devices but not to a large enough extent on mixed-signal devices. Also, multiple analog functions on a single chip (such as dual, quad, octal, etc., for LAN ports) must be tested simultaneously.
4. Better software tools that apply to more than one test equipment vendor are needed. Tools are required for digital and mixed-signal vector generation, circuit simulation of the device's analog circuitry along with the load board and the test instruments, and rapid mixed-signal test program generation. Currently, mixed-signal test programs are manually generated; automatic test program generators are widely used for generating digital test.

Table 27a Mixed-signal Test Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Low Frequency Source and Digitizer							
BW * (MHz)	**15**	**22**	**30**	**40**	**50**	**60**	**60**
Fs** (MS/s***)	**5**	**7**	**10**	**13**	**16**	**20**	**20**
Resolution (bits)	**20–23**	**20–23**	**20–23**	**24**	**24**	**24**	**24**
Noise floor (dB/RT Hz)	**-160**	**-160**	**-160**	**-165**	**-165**	**-165**	**-165**
High Frequency Waveform Source							
Level V (pk–pk) Accuracy (+/-)	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**
BW (MHz)	**1600**	**2400**	**3200**	**4000**	**4800**	**6000**	**7000**
Fs (MS/s)	**3500**	**5000**	**7000**	**8500**	**10000**	**12000**	**15000**
Resolution (bits) AWG/Sine†	**10/14**	**10/14**	**10/14**	**10/14**	**10/14**	**10/14**	**10/14**
Noise floor (dB/RT Hz)	**-145**	**-145**	**-150**	**-150**	**-155**	**-155**	**-155**
High Frequency Waveform Digitizer							
Level V (pk–pk) Accuracy (+/-)	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**
BW (MHz) (undersampled)	**2000**	**3000**	**4000**	**5200**	**6400**	**8000**	**9200**
Fs (MS/s)	**200**	**300**	**400**	**520**	**640**	**800**	**920**
Resolution (bits)	**12**	**12**	**12**	**12**	**14**	**14**	**14**
Noise floor (dB/RT Hz)	**-145**	**-145**	**-150**	**-150**	**-155**	**-155**	**-155**

Table 27a Mixed-signal Test Requirements—Near-term (continued)

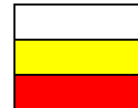
YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Time Measurement							
Jitter measurement (ps RMS)	3	2	2	1	1	1	1
Frequency measurement (MHz)	660	1320	1320	1320	2640	2640	2640
Single shot time capability (ps)	100	75	75	75	50	50	50
RF/Microwave Instrumentation							
Source BW (GHz) Accuracy (+/-dB)	10 0.2	14 0.2	14 0.2	18 0.2	18 0.1	18 0.1	18 0.1
Source phase noise low frequency Close-In 1KHz (dBc/Hz)	130	136	136	136	136	136	136
Source phase noise high frequency Wideband 10MHz (dBc/Hz)	160	166	166	166	166	166	166
Receive BW (GHz)	10	14	14	14	18	18	18
Receive noise floor (dBm/Hz)	-160	-160	-160	-166	-166	-166	-166
Receive dynamic range SFDR (dBc) ‡	110	130	140	140	140	160	160
Special Digital Capabilities							
D/A and A/D digital data rate (MB/s)	300	400	520	640	800	920	1040
Sample clock jitter (< ps RMS)	1.5	1	0.5	0.25	0.2	0.15	0.1

BW—Bandwidth *Fs—Sample rate* *MS/s—Megasamples/second*

† AWG/Sin—Arbitrary waveform generation/sine wave *‡ SFDR—Spurious free dynamic range*

§ MB/s—Megabits/second

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



Definitions for Table 27a and b:

Low Frequency Source And Digitizer—This is the basic, minimum, instrument set of any mixed-signal tester. Telecommunications, advanced audio and wireless baseband will drive these specifications. Differential inputs/outputs are needed.

High Frequency Waveform Source—Disk drive read channels (PRML) will drive sample rate and bandwidth. Local area network (LAN) devices will drive sample rate, bit resolution and amplitude accuracy. Differential outputs are needed.

High Frequency Waveform Digitizer—An undersampled (down conversion, track-and-hold, etc) bandwidth is shown. The sample rates and bit resolutions are for a direct conversion digitizer, which is usually preceded by the undersampler. PRML and LAN devices will drive digitizer specifications. Differential inputs are needed.

Time Measurement—Phase Lock Loops (PLLs), which are increasingly being embedded in new designs, will require Jitter and Frequency measurements. A specialized class of instruments will have to be developed to make these measurements efficiently and accurately.

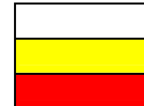
RF/Microwave Instrumentation—Single chip RF/digital/baseband/audio devices will require RF instruments such as modulated carrier sources and low noise receivers or down converters.

Special Digital Capabilities—For converter testing, the ability to source a digital word to a D/A and capture a digital word from an A/D.

Table 27b Mixed-signal Test Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm))	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
Low Frequency Source and Digitizer			
BW * (MHz)	**60**	**60**	**60**
Fs** MS/s***	**20**	**20**	**20**
Resolution (bits)	**24**	**24**	**24**
Noise floor (dB/RT Hz)	**-165**	**-165**	**-165**
High Frequency Waveform Source			
Level V (pk–pk) Accuracy	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**
BW (MHz)	**7000**	**7000**	**7000**
Fs (MS/s)	**15000**	**15000**	**15000**
Resolution (bits) AWG/Sine†	**10/14**	**10/14**	**10/14**
Noise floor (dB/RT Hz)	**-155**	**-155**	**-155**
High Frequency Waveform Digitizer			
Level V (pk–pk) Accuracy	**4** **0.5%**	**4** **0.5%**	**4** **0.5%**
BW (MHz) (undersampled)	**10000**	**10000**	**10000**
Fs (MS/s)	**1000**	**1000**	**1000**
Resolution (bits)	**14**	**14**	**14**
Noise floor (dB/RT Hz)	**-155**	**-155**	**-155**
Time Measurement			
Jitter measurement (ps RMS)	**1**	**1**	**1**
Frequency measurement (MHz)	**3000**	**3000**	**3000**
Single shot time capability (ps)	**30**	**30**	**30**
RF/Microwave Instrumentation			
Source BW (GHz)	**36**	**36**	**36**
Source phase noise low frequency Close-In 1KHz (dBc/Hz)	**140**	**140**	**140**
Source phase noise high frequency Wideband 10MHz (dBc/Hz)	**166**	**166**	**166**
Receive BW (GHz)	**36**	**36**	**36**
Receive noise floor (dBm/Hz)	**-166**	**-166**	**-166**
Receive dynamic range SFDR (dBc) ‡	**160**	**160**	**160**
Special Digital Capabilities			
D/A and A/D data rate (MB/s) §	**1200**	**1200**	**1200**
Sample clock jitter (< ps RMS)	**0.1**	**0.1**	**0.1**

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known



EQUIPMENT FOR TESTING DEVICES DESIGNED WITH DFT

The use of DFT is showing a rapid growth trend across the semiconductor industry. The reasons for this growth are many. DFT can greatly shorten test development cycle times, improve fault coverage, access multiple internal circuits in an SoC through a common subset of pins, test high performance circuits with medium performance interfaces, facilitates massively parallel testing, and more. Except for a few isolated point solutions, most structural (DFT) testing to-date has been performed on conventional digital ATE. This has the unfortunate consequences of exceeding the test requirements in some areas and being sub optimal in others. This means that many devices utilizing DFT are paying a higher cost of test than necessary. Therefore, a need has arisen for the development of specialized ATE, targeted at this "new" class of DFT savvy devices.

Table 28 indicates the industry trends over the next seven years. The data represented is a composite of the projected requirements from various semiconductor manufacturers. There are slightly divergent requirements across the semiconductor industry due to a number of different factors:

1. DFT is still a maturing technology and thus, not consistently implemented across the industry.
2. There are different deployment strategies dependent on device technologies and manufacturing flows.
3. There is a need to support various levels of "legacy" test methodologies for older product families.

Therefore it is important to note that these tables should not be construed as a "specification." It is not expected that any single configuration would satisfy all DFT applications.

*Table 28 DFT-BIST Device Test Requirements—Near-term***

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65	
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65	
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35	
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25	
Number of parallel sites	**32**	**32**	**64**	**64**	**128**	**128**	**128**	COST
Scan data volume(Giga-pin-vectors available per site)	**6**	**6**	**12**	**12**	**16**	**16**	**16**	LOGIC DENSITY
Scan pin (available per site / system)	**256/1K**	**256/1K**	**256/2K**	**256/2K**	**256/4K**	**256/4K**	**256/4K**	LOGIC DENSITY
Scan vector rate (MT or MHz)	**50**	**100**	**100**	**200**	**200**	**200**	**200**	TEST TIME
"Full function" pin (available per site / system)	**128/256**	**128/256**	**128/512**	**128/512**	**128/512**	**128/512**	**128/512**	TEST TIME
Functional vector depth (M-Vectors)	**16**	**16**	**16**	**16**	**16**	**16**	**16**	LOGIC DENSITY
Functional data rate (MHz)	**100**	**100**	**100**	**200**	**200**	**200**	**200**	TEST TIME
"Reduced function" pin (available per site / system)(DC only)	**3K/4K**	**3K/4K**	**3K/4K**	**4K/5K**	**4K/5K**	**5K/6K**	**5K/6K**	I/O DENSITY
Clock pins (available per site / system)	**4/32**	**4/32**	**4/64**	**4/64**	**4/128**	**4/128**	**4/128**	CLOCK DOMAINS
Clock frequency (MHz)	**200**	**200**	**400**	**400**	**400**	**800**	**800**	ON-CHIP CLOCK RATE
Power supplies (available per site / system)	**8/32**	**8/32**	**8/64**	**8/64**	**8/128**	**8/128**	**8/128**	LOGIC DENSITY

*Table 28 DFT-BIST Device Test Requirements—Near-term (continued)***

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	DRIVER
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65	
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65	
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35	
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25	
Support for options								SoC
High-speed clock (differential pairs)	yes	yes	yes	yes	yes	yes	yes	
Signature compression	yes	yes	yes	yes	yes	yes	yes	
Algorithmic pattern generation	yes	yes	yes	yes	yes	yes	yes	
Low-frequency source and digitizer	yes	yes	yes	yes	yes	yes	yes	
High-frequency source and digitizer	yes	yes	yes	yes	yes	yes	yes	
Time measurement unit	yes	yes	yes	yes	yes	yes	yes	
ADC/DAC	yes	yes	yes	yes	yes	yes	yes	
RF source	no	no	yes	yes	yes	yes	yes	
High power	yes	yes	yes	yes	yes	yes	yes	
IDDQ	yes	yes	yes	yes	yes	yes	yes	

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

Definitions for Table 28:

Parallel Sites—Parallel testing of devices is a common technique for reducing the effective cost of test per device by testing multiple devices with a single tester. The number of devices that can be tested in parallel will be necessarily limited by the tester's available physical resources, however there should be no "logical" limit imposed by the hardware or software architecture. A common concern with these tables in the past has been the total number of pins that seem to be indicated by multiplying all of the numbers together, however this is not the intent. The total number of pins available on a given tester should be consistent with the current state-of-the-art for pin densities.

Scan Data Volume—The total number of bits shifted into the scan input pins plus the total number of bits shifted out of scan output pins. It is the total number of scan-able elements in a device multiplied by the total number of scan-loads plus the scan-unloads. A single bit shifted into a single device pin or shifted out of a single device pin can be defined as pin-vector (a tester architecture neutral unit).

Scan Pin—The maximum number of scan input pins and scan output pins. This number does not necessarily include the pins required for scan control.

Scan Vector Rate—The maximum shift rate for scan data input pins and scan data output pins (expressed in MegaTransfers per second (MT)).

"Full Function" Pin—Full Function pins are backed by drive and receive resources containing the full functionality of a traditional ATE system pin. These resources may include, but are not necessarily limited to, precision timing accuracy, flexible waveform capability, high vector rates, programmable drive/receive thresholds, parametric measurement capability, etc. These "Full Function" pins are used to test the DUT via a traditional ATE approach utilizing device primary I/O pins which may include, but are not limited to the following functions: clock, input, output, bi-directional, and reference level bias (fixed state controlled by ATE pin electronics). In addition, the full function pins should be capable of scan (either within the limits of "Full Function" pin memory depth or with access to the scan memory).

Functional Vector Depth—The total number of vectors required to test a particular device. In this context, it refers to the total number of individual states (e.g., "0," "1," "H," "L," "X," "Z," etc.) applied to or received from a single device pin.

Functional Data Rate – The maximum rate of application of vectors to the data pins of the device.

"Reduced Function" Pin—Reduced Function pins are backed by low-cost resources containing limited digital drive/receive capability (e.g. static vectors are vectors that remain static for the duration of a particular test or subtest), no waveform capability, very little vector depth, etc. These pins will typically have programmable drive/receive thresholds, and parametric measurement capability.

Clock Pin—These single-ended clock pins function at higher frequencies and higher accuracies than the scan and functional data pins. These clocks are used for functional testing at the functional data rate, as well as, AC scan (shift slow – sample fast) and BIST, to facilitate high performance testing on DFT testers.

Clock Frequency—The maximum frequency attainable from the standard clock source. The accuracy and skew for the clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.

Power Supplies—ATE device power supplies provide programmable voltage (or current) levels during testing. The most typical application is to apply voltage and current to a device's primary power connections such as V_{cc} or V_{dd}. Other uses include reference voltage sources for device pins, termination voltages for external loads, and current sourcing during test. Device power supplies may be used in forcing either current or voltage while measuring the resulting voltage or current. Common feature include programmable clamps, measurement trigger/capture controlled by the tester's pattern generator, and switch-able output voltage ranges controlled by the pattern generator. Supplies should be gang-able for flexibility.

Support for Options—There will always be a need to support options. This is driven by the need to support legacy devices in the Functional-to-Structural transition phase, as well as, for devices with mature DFT and some mixed-signal or extended performance requirements. The remaining line items in this table try to predict the need and performance requirements of some of the more typical of these options in the future. There are a number of analog options – these have been specifically identified, though this may not be a comprehensive list.

High-Speed Clock Pin—The high-speed clock pins function at higher frequencies and higher accuracies than the "standard" clock source. The high-speed clocks should support both single-ended operation and differential clock pairs. The maximum frequency required for this clock option is 800MHz through 2003, rising to 1.4GHz in 2004. The accuracy and skew for the high frequency clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.

Signature Compression—Integrating Linear Feedback Shift Registers (LFSRs) with the scan channels on the DFT tester can dramatically reduce scan data volume and test time. Pseudo Random Pattern Generators (PRPGs) can be used to minimize the amount of scan-in stimuli that need to be stored in the scan buffer. Single Input Signature Registers (SISRs) can be used to compress scan-out measures. The PRPGs and SISRs should be integrated with the scan channels such that an individual scan cycle can interact with either its LFSR / SISR or scan channel. The LFSRs / SISRs should have programmable polynomials. The LFSRs/ SISRs should be capable of having their states seeded, reset, and observed under pattern op-code control and from states stored in pattern memory.

Algorithmic Pattern Generation—Memory pattern sequences are generally repetitive and can, therefore, be generated algorithmically. Algorithmic Pattern Generator functionality should be integrated with other tester pattern sources to allow operation concurrently with stored stimulus/response test patterns.

Low Frequency Source/Digitizer—The ability to generate and digitize a differential analog waveform, such as a ramp or sine wave. Generally, 18-bit resolution up to 100KHz.

High Frequency Source/Digitizer—The ability to generate and digitize a differential analog waveform, such as a ramp or sine wave. Generally, 12-bit resolution up to 10MHz.

Time Measurement—Ability to measure a time interval or frequency.

RF Source—As Radio Frequency functions find their way onto more and more SoCs and appropriate DFT sampling methodologies are developed for RF, there will be a need for external resources to generate clean, high frequency sine waves. The frequency requirements of these resource will be in the 100MHz to 6GHz range.

High Power—Some devices consume very high power (>75W), during tests. High-current device power supplies must deliver accurate voltage and respond quickly to load changes (on the order of 1–2µs). In addition, significant current is applied through the tooling fixture and contactors or probe needles. There may be 1000s of device power pins in extremely tight physical density. The power supply must be capable of performing integrity tests that detect discontinuities such as power shorts to prevent damage to expensive test fixtures. In general, flexible user control of fast-acting safety/error, clamping, and shutdown hardware features becomes more important in high power delivery.

SEMICONDUCTOR MEMORIES TEST REQUIREMENTS

It is expected that memory density will continue to grow at an exponential rate. Semiconductor memories will continue to be the test vehicle for the development of new process technologies. DRAM will continue to be the leading devices to define the process technology, design and test. Refer to Tables 29 through 31.

COMMODITY DRAM TESTING

DRAM bit density will continue to quadruple every two years in the short-term; however, in the long-term this trend will slow and DRAM bit density will quadruple every three years. Increasing memory size will cause test to become a manufacturing bottleneck due to increasing device test time and decreasing manufacturing cell throughput. Redundancy is necessary for commodity DRAMs. To enhance test productivity, new test-oriented architectures will be required. Multi-bit testing, BIST, and built-in self-repair (BISR) will be essential to maintain the production throughput and yield.

A considerable parallelism in test from the automatic tester equipment will be required. The number of devices simultaneously tested refers to the packaged devices tested at-speed. In the realm of above 2 GHz, there is a bottleneck with the device exterior and the interface such as signal transmission method, socket, probing, and handling. Because of required timing accuracy and test/device interface components, exceeding beyond 64 devices per test head is a challenge.

The primary fault models for DRAMs will continue to be cell stuck-at, multi-cell coupling, decoder open, and data retention faults. For 100 nm feature size and below, in-line defect detection will be necessary for product development. With inline defect monitoring, processing of defective wafers will be avoided and test time for wafer sort and package-level test will be maintained.

Table 29a Commodity DRAM Test Requirements—Near-term

Year of Production		*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)		*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)		*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU Printed Gate Length (nm)		*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU Physical Gate Length (nm)		*65*	*53*	*45*	*37*	*32*	*28*	*25*
DRAM capacity (Gbits):	R&D	**2**	—	**4**	—	**8**	—	**16**
	Mass Production	**0.512**	—	**1**	—	**2**	—	**4**
DRAM data rate (GHz):	R&D	**1.3**	—	**1.6**	—	**2**	—	**2.4**
	Mass Production	**1**	—	**1.3**	—	**1.6**	—	**2**
DRAM access time (ns):	R&D	**2**	—	**1**	—	**0.5**	—	**0.3**
	Mass Production	**4**	—	**2.5**	—	**2**	—	**1**
DRAM bit width/device (Mass Production)		**16**	—	**16**	—	**16**	—	**16**
Tester data rate (GHz):	R&D	**1.3**	—	**1.6**	—	**2**	—	**2.4**
	Mass Production	**1**	—	**1.3**	—	**1.6**	—	**2**
Overall timing accuracy (ps):	R&D	**60**	—	**50**	—	**40**	—	**30**
	Mass Production	**80**	—	**60**	—	**50**	—	**40**
Simultaneous testing (devices/test head)		**32/64**	—	**64**	—	**64**	—	**128**
Test channels (Mass Production)		**1200* 2300****	**—**	**1200* 2300****	**—**	**2300**	—	**2300**

** Assuming SDRAM with 32 devices/station, Driver 800, I/O 640*

*** Assuming RAMBUS with 32 devices/station, Driver 480, I/O 640; 2 64 devices/station, Driver 960, I/O 1280*

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

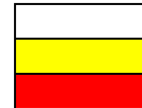
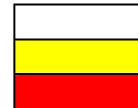


Table 29b Commodity DRAM Test Requirements—Long-term

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*45*	*32*	*22*
MPU PRINTED GATE LENGTH (nm)	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*18*	*13*	*9*
DRAM capacity (Gbits): R&D	**64**	**256**	**1024**
Mass Production	**16**	**64**	**256**
DRAM data rate (GHz): R&D	**3.0**	**3.6**	**4.2**
Mass Production	**2.4**	**3.0**	**3.6**
DRAM access time (ns): R&D	**0.2**	**0.15**	**0.1**
Mass Production	**0.8**	**0.5**	**0.3**
DRAM bit width/device (Mass Production)	**32**	**32**	**32**
Tester data rate (GHz): R&D	**3.0**	**3.6**	**4.2**
Mass Production	**2.4**	**3.0**	**3.6**
Overall timing accuracy (ps): R&D	**25**	**20**	**18**
Mass Production	**30**	**25**	**20**
Simultaneous testing (Devices/test head)	**128**	**256**	**256**
Test channels (Mass Production)	**3500***	**3500***	**3500***

Assuming RAMBUS with 64 devices/station, Driver 960, I/O 2560

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



COMMODITY FLASH TESTING

There are a variety of Flash I/O bus types with the most common being non-multiplexed, Address/Data multiplexed, Address/Address/Address/Data multiplexed, serial, synchronous burst and SDRAM-like. Further proliferation of bus types is expected due to the customization of flash for applications. Bus width is presently 8-bit and 16-bit but 32-bit widths are on the horizon.

Flash is commonly used in battery powered embedded applications thus test equipment must provide a means of measuring low levels of current or energy. Supply voltage requirements of Flash have been dropping slowly over time, but the need for internal test mode voltages that are 3–5 times the external supply requirements is expected to continue. Increased absolute accuracy of supply voltages will be required in the future due to the trend toward lower voltages, but is expected to remain constant as a relative percentage. I/O voltage decreases are pushing the operation limits of standard tester load circuits, new methods will be required in the future.

Wafer test generally does not require the performance of package test, but error detection, error analysis, and redundancy processing is required.

Stacking of various types of Flash and other memory or logic components in a single package has become standard and is expected to continue. Stacked packaging has complicated the package test requirements and increased the per package pin count. Many Flash components contain an embedded controller for program/erase control, enabling feature additions that require additional logic or analog test capability. Logic test capability is reflected in the table.

Data and clock rates for flash will increase, but there is expected to be a wide variability in the requirements based upon the end application. Table 30a and b reflects only the high-end trend.

Table 30a Commodity Flash Memory Test Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*Driver*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
MPU Printed Gate Length(nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
Device Characteristics								
Density (megabits): volume production	**64**	**128**	**128**	**256**	**256**	**512**	**512**	
Density (megabits): lead density	**512**	**512**	**1024**	**1024**	**2048**	**4096**	**4096**	
Data width (bits)	**32**	**32**	**32**	**32**	**32**	**32**	**32**	
Simultaneously tested devices (wafer test)	**64**	**64**	**64**	**128**	**128**	**128**	**128**	
Simultaneously tested devices (package test)	**64**	**64**	**64**	**128**	**128**	**128**	**128**	
Power Supplies								
Power supply voltage range	**0.6–5.5**	**0.6–5.5**	**0.6–5.5**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	
Power supply accuracy (% of programmed value)	**5**	**5**	**5**	**5**	**5**	**5**	**5**	
Maximum current (MA)	**200**	**200**	**300**	**300**	**300**	**300**	**300**	
Programming power supply voltage range (V)	**0.6–10.0**	**0.6–10.0**	**0.6–10.0**	**0.6–10.0**	**0.6–10.0**	**0.6–10.0**	**0.6–8.0**	
Pattern Generator								
Tester channels per test site [1]	**64**	**64**	**64**	**64**	**64**	**64**	**64**	
Vector depth (millions)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	
Scan vector depth (millions) [2]	**2**	**4**	**4**	**4**	**4**	**4**	**4**	*On-chip or multi-chip logic*
APG addresses [3]	**48**	**48**	**48**	**48**	**48**	**48**	**48**	
Timing								
Maximum data rate (MHz)	**80**	**100**	**125**	**133**	**166**	**166**	**166**	
Accuracy OTA (ns)	**0.75**	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**	**0.5**	
Cost								
Tester cost per pin ($) [4] [5]	**1000**	**950**	**903**	**857**	**815**	**774**	**735**	
Reliability								
MTBF (hours) [6]	**3000**	**3150**	**3308**	**3473**	**3647**	**3829**	**4020**	
MTTR (hours)	**1**	**1**	**1**	**1**	**1**	**1**	**0.5**	
Availability (%)	**99**	**99**	**99.5**	**99.5**	**99.5**	**99.5**	**99.5**	
Setup time (hours)	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

Notes for Table 30a and b:

[1] The number represents the maximum number of tester channels needed for a single device under test. Multiple die stacked in a single package will increase this requirement

[2] Separate scan-in and scan out.

[3] Total addresses may be distributed in either two (X,Y) or three (X, Y, Z) fields

[4] Overall tester cost is: (per pin cost) x (number of channels) x (number of simultaneously tested).

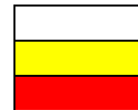
[5] Tester cost per pin decreases 5% per year.

[6] MTBF increases 5% per year.

Table 30b Commodity Flash Memory Test Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016	DRIVER
DRAM ½ PITCH (nm)	45	32	22	
MPU / ASIC ½ PITCH (nm)	45	32	22	
MPU PRINTED GATE LENGTH (nm)	25	18	13	
MPU PHYSICAL GATE LENGTH (nm)	18	13	9	
Device Characteristics				
Density (megabits): volume production	**2048**	**4096**	**8192**	
Density (megabits): lead density	**16384**	**65536**	**131072**	
Data width (bits)	**32**	**32**	**32**	
Simultaneously tested devices (wafer test)	**256**	**256**	**256**	
Simultaneously tested devices (package test)	**256**	**256**	**256**	
Power Supplies				
Power supply voltage range	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	
Power supply accuracy (% of programmed value)	**5**	**5**	**5**	
Maximum current (MA)	**300**	**300**	**300**	
Programming power supply voltage range (V)	**0.6–8.0**	**0.6–8.0**	**0.6–8.0**	
Pattern Generator				
Tester channels per test site [1]	**72**	**72**	**72**	
Vector depth (millions)	**2**	**2**	**2**	
Scan vector depth (millions) [2]	**8**	**8**	**8**	ON-CHIP OR MULTI-CHIP LOGIC
APG addresses [3]	**48**	**48**	**48**	
Timing				
Maximum data rate (MHz)	**200**	**250**	**300**	
Accuracy OTA (ns)	**0.3**	**0.2**	**0.1**	
Cost				
Tester cost per pin ($) [4] [5]	**630**	**540**	**463**	
Reliability				
MTBF (hours) [6]	**4654**	**5388**	**6237**	
MTTR (hours)	**0.5**	**0.5**	**0.5**	
Availability (%)	**99.5**	**99.5**	**99.5**	
Setup time (hours)	**0.2**	**0.2**	**0.2**	

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known



EMBEDDED DRAM AND FLASH TESTING

In the near-term, the number of embedded DRAM bits will double in every two years; in the long-term this growth will slow to double every three years. The major concern in the merged logic-DRAM design in a dual-gate process will be array noise and sense-amp imbalance. For the 100 nm node and below, in-line defect detection will be necessary for product development. With in-line defect monitoring, processing of defective wafers will be avoided and test time for wafer sort and package level test will be maintained.

Embedded Flash memory bits will grow exponentially in the near term; however, in the long-term embedded flash memory bits will double every two years. It is expected that embedded flash memories will transition to use a multi-bit cell architecture. More and more ICs will include both DRAM and flash memories. Oxide reliability, sense-amp imbalance, and oxide-nitride-oxide (ONO) scaling will be the major concerns in flash memories from 2003 and onwards. Refer to Table 31a and b.

To enhance test productivity, new test oriented architectures will be required. Built-in self-test and built-in self-repair will be essential to test embedded DRAM and embedded Flash memories and to maintain production throughput and yield. The primary test algorithms for Flash memories will continue to be Read-disturb, Program-disturb, and Erase-disturb while March tests with all data background will be essential for embedded DRAM.

Considerable parallelism in test will be required to maintain test throughput in the face of rising memory densities. It is expected that by the year 2003 and onwards, test will become cost-effective in double insertion of devices rather than testing both logic and embedded memories on the logic tester. In double insertion, embedded Flash and DRAMs will be tested and repaired on the memory tester, while the logic blocks will be tested on the logic tester. Embedded SRAM test requirements are captured in the High Performance Microprocessor section of the roadmap.

Table 31a Embedded Memory (DRAM and Flash) Test Requirements—Near-term

<table>
<tr><td>YEAR OF PRODUCTION</td><td>2001</td><td>2002</td><td>2003</td><td>2004</td><td>2005</td><td>2006</td><td>2007</td></tr>
<tr><td>DRAM ½ PITCH (nm)</td><td>130</td><td>115</td><td>100</td><td>90</td><td>80</td><td>70</td><td>65</td></tr>
<tr><td>MPU / ASIC ½ PITCH (nm)</td><td>150</td><td>130</td><td>107</td><td>90</td><td>80</td><td>70</td><td>65</td></tr>
<tr><td>MPU PRINTED GATE LENGTH (nm)</td><td>90</td><td>75</td><td>65</td><td>53</td><td>45</td><td>40</td><td>35</td></tr>
<tr><td>MPU PHYSICAL GATE LENGTH (nm)</td><td>65</td><td>53</td><td>45</td><td>37</td><td>32</td><td>28</td><td>25</td></tr>
<tr><td colspan="8">Embedded DRAM</td></tr>
<tr><td colspan="8">Embedded DRAM size (Mbits)</td></tr>
<tr><td>R&D</td><td colspan="2">64</td><td colspan="2">128</td><td colspan="2">256</td><td>512</td></tr>
<tr><td>Mass Production</td><td colspan="2">32</td><td colspan="2">64</td><td colspan="2">128</td><td>256</td></tr>
<tr><td>Failure concerns</td><td colspan="2">Particle defects; data retention</td><td colspan="2">Particle defects; array noise; data retention</td><td colspan="2">Particle defects; array noise; sense-amp imbalance</td><td>Particle defects; array noise; sense-amp imbalance</td></tr>
<tr><td>Wafer level test</td><td colspan="2">Single insertion</td><td colspan="2">Double insertion</td><td colspan="2">Double insertion</td><td>Double insertion</td></tr>
<tr><td>Usage of on-chip test</td><td colspan="2">50% BIST
100% BISR</td><td colspan="2">100% BIST
100% BISR</td><td colspan="2">100% BIST
100% BISR</td><td>100% BIST
100% BISR</td></tr>
<tr><td colspan="8">Embedded Flash</td></tr>
<tr><td colspan="8">Embedded Flash size (Mbits)</td></tr>
<tr><td>R&D</td><td colspan="2">16</td><td colspan="2">32</td><td colspan="2">64</td><td>128</td></tr>
<tr><td>Mass Production</td><td colspan="2">4</td><td colspan="2">16</td><td colspan="2">32</td><td>64</td></tr>
<tr><td colspan="8">Embedded mixed memory size (Mbits)</td></tr>
<tr><td>Flash</td><td colspan="2">1</td><td colspan="2">4</td><td colspan="2">16</td><td>32</td></tr>
<tr><td>DRAM</td><td colspan="2">4</td><td colspan="2">16</td><td colspan="2">32</td><td>32</td></tr>
<tr><td>Failure concerns</td><td colspan="2">Oxide defects; # of erase cycles</td><td colspan="2">Oxide defects; ONO scaling</td><td colspan="2">Oxide defects; ONO scaling; over erase</td><td>Oxide defects; ONO scaling; over erase</td></tr>
<tr><td>Wafer level test</td><td colspan="2">Single insertion</td><td colspan="2">Single insertion</td><td colspan="2">Double insertion</td><td>Double insertion</td></tr>
<tr><td>Usage of On-chip test</td><td colspan="2">50% BIST
100% BISR</td><td colspan="2">100% BIST
100% BISR</td><td colspan="2">100% BIST
100% BISR</td><td>100% BIST
100% BISR</td></tr>
</table>

Number of bits in mass production is approximately 50% of number of bits in R&D

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 31b Embedded Memory (DRAM and Flash) Test Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (nm)	45	32	22
MPU / ASIC ½ PITCH (nm)	45	32	22
MPU PRINTED GATE LENGTH (nm)	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	18	13	9
Embedded DRAM			
Embedded DRAM size (Gbits)			
R&D	**1**	**2**	**4**
Mass Production	**0.512**	**1**	**2**
Failure concerns	**Particle Defects, Array Noise, Sense-amp Imbalance**	**Particle Defects, Array Noise, Sense-amp Imbalance**	**Particle Defects, Array Noise, Sense-amp Imbalance**
Wafer level test	**In-line Defect Detection, Double Insertion**	**In-line Defect Detection, Double Insertion**	**In-line Defect Detection, Double Insertion**
Usage of on-chip test	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**
Embedded Flash			
Embedded Flash size (Mbits)			
R&D	**256**	**512**	**1024**
Mass Production	**64**	**128**	**256**
Embedded mixed memory size (Mbits)			
Flash	**64**	**128**	**256**
DRAM	**64**	**128**	**256**
Failure concerns	**Oxide Defects, ONO Scaling, Sense-amp Imbalance**	**Oxide Defects, ONO Scaling, Sense-amp Imbalance**	**Oxide Defects, ONO Scaling, Sense-amp Imbalance**
Wafer level test	**In-line Defect Detection, Double Insertion**	**In-line Defect Detection, Double Insertion**	**In-line Defect Detection, Double Insertion**
Usage of On-chip test	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**

Number of bits in mass production is approximately 50% of number of bits in R&D

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

RELIABILITY TECHNOLOGY REQUIREMENTS

BURN-IN REQUIREMENTS

Burn-in faces many of the same electrical and mechanical challenges as noted in other sections of this chapter. In addition, some limitations of the burn-in process create constraints not found in the Test arena. These are covered in the Table 32a and b below.

Burn-in is moving from functional to structural test in response to the high I/O count, high speed, and high complexity of newer device technologies. Scan and BIST capabilities, both on the device and on the system, are needed to ensure that

future generations of burn-in are feasible and cost-effective. A positive byproduct of this trend will be the increasing use of the burn-in process for massive parallel test for devices in some market segments. Because of the trend toward Scan, burn-in requires the same test pattern generation / conversion capabilities as needed for Test. It is possible that the testers discussed in the DFT Test Roadmap section will play a role in future burn-in environments.

Device electrical test needs will drive burn-in requirements toward deeper vector memories, faster clocks and signals, both lower and higher voltages, more accurate power supplies, and analog stressing capabilities. At the same time, physical and economic limitations of the existing burn-in environment will constrain vector widths, clock and signal speeds, and power delivered to the device. These limitations will drive changes in the way burn-in is performed. As device bias voltages become smaller, traditional voltage and temperature acceleration factors will no longer scale sufficiently, requiring research into novel acceleration methodologies to identify and eliminate failure mechanisms.

At the wafer level, several different solutions are now available for burn-in. This technology is driven primarily by the need for known good die, as the wafer level burn-in process is not yet mature enough to serve as a generic replacement for package level burn-in. Requirements in wafer level burn-in include effective contacting, a match of coefficients of thermal expansion between the wafer and the contact interface, the ability to interface with larger wafer sizes (300 mm and beyond), electrical isolation of bad die to prevent damage to the system or wafer, and reliable contacts to tens of thousands of points on the wafer. At the package level, contacting technology will be driven by finer pitch, higher pin counts, higher speeds, and strip / panel level testing.

Increasing power requirements for high-end microprocessors and ASIC devices have resulted in a market for active thermal control on individual devices. Present solutions offer the capability to control the individual device heat generation, but the need exists for a more cost-effective approach.

All of the above requirements ultimately affect the overall cost of burn-in. Whereas traditional dynamic burn-in could be expected to cost between $0.0005 and $0.02 per device hour in the system (system cost plus board cost, divided by devices per system), Test During Burn-in and Wafer Level Burn-in systems range from $0.005 to $0.2 per device hour, while active thermal management systems can cost as much as $0.25 per device hour.

Table 32a Burn-in Requirements—Near-term

YEAR OF PRODUCTION	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
High Performance ASIC							
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**25**	**50**	**50**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–4.0**	**0.7–4.0**	**0.7–3.3**	**0.7–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**
Power dissipation (W per DUT)	**130**	**140**	**150**	**150**	**200**	**200**	**200**
Maximum number of signal I/O	**384**	**384**	**384**	**384**	**384**	**384**	**384**
High Performance Microprocessor							
Clock input frequency (MHz)	**150**	**200**	**200**	**250**	**250**	**250**	**250**
Off-chip data frequency (MHz)	**33**	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–4.0**	**0.7–3.5**	**0.7–3.5**	**0.5–3.5**	**0.5–3.5**	**0.5–3.5**	**0.5–3.5**
Power dissipation (W per DUT)	**150**	**200**	**200**	**250**	**300**	**300**	**300**
Maximum current (A)	**75**	**150**	**150**	**300**	**300**	**300**	**300**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**	**128**

Table 32a Burn-in Requirements—Near-term (continued)

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Low-End Microcontroller							
Clock frequency (MHz)	**25**	**100**	**200**	**300**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**25**	**40**	**50**	**60**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–12.0**	**0.7–12.0**	**0.7–12.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**
Power dissipation (W per DUT)	**3**	**5**	**5**	**10**	**10**	**10**	**10**
Maximum number of signal I/O	**32**	**32**	**32**	**32**	**32**	**32**	**32**
Mixed-Signal							
Clock input frequency (MHz)	**150**	**200**	**200**	**250**	**250**	**250**	**250**
Off-chip data frequency (MHz)	**33**	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–65.0**	**0.7–65.0**	**0.7–100**	**0.7–100**	**0.5–500**	**0.5–500**	**0.5–500**
Power dissipation (W per DUT)	**50**	**50**	**75**	**75**	**150**	**150**	**150**
Maximum current (A)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Analog signal peak-to-peak voltage range (V)	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**
Commodity Memory							
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**30**	**30**	**30**	**50**	**50**	**50**	**50**
Power supply voltage range (V)	**0.6–6.0**	**0.6–6.0**	**0.6–6.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**
Programming power supply voltage range (V)	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–8**
Power dissipation (W per DUT)	**2**	**5**	**10**	**15**	**20**	**20**	**20**
Maximum number of signal I/O	**18**	**36**	**36**	**72**	**72**	**72**	**72**
DFT / BIST Requirements							
Scan pin count (per DUT)	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Scan vector memory depth (megavectors)	**64**	**128**	**256**	**256**	**256**	**256**	**256**
Scan vector frequency (MHz)	**33**	**75**	**75**	**75**	**75**	**75**	**75**

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

Table 32b Burn-in Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
High Performance ASIC			
Clock input frequency (MHz)	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–2.5**	**0.5–2.5**	**0.4–2.5**
Power dissipation (W per DUT)	**200**	**225**	**250**
Maximum number of signal I/O	**384**	**384**	**384**
High Performance Microprocessor			
Clock input frequency (MHz)	**250**	**250**	**250**
Off-chip data frequency (MHz)	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–3.0**	**0.5–2.5**	**0.5–2.5**
Power dissipation (W per DUT)	**300**	**300**	**300**
Maximum current (A)	**300**	**300**	**300**
Maximum number of signal I/O	**128**	**128**	**128**
Low-End Microcontroller			
Clock frequency (MHz)	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–10**	**0.5–10**	**0.5–10**
Power dissipation (W per DUT)	**20**	**20**	**20**
Maximum number of signal I/O	**32**	**32**	**32**
Mixed-Signal			
Clock input frequency (MHz)	**250**	**250**	**250**
Off-chip data frequency (MHz)	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–500**	**0.5–1000**	**0.5–1000**
Power dissipation (W per DUT)	**150**	**150**	**150**
Maximum current (A)	**30**	**30**	**30**
Maximum number of signal I/O	**128**	**128**	**128**
Analog signal peak-to-peak voltage range (V)	**±10V**	**±10V**	**±10V**
Commodity Memory			
Clock input frequency (MHz)	**400**	**400**	**400**
Off-chip data frequency (MHz)	**50**	**50**	**50**
Power supply voltage range (V)	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**
Programming power supply voltage range (V)	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**
Power dissipation (W per DUT)	**20**	**20**	**20**
Maximum number of signal I/O	**72**	**72**	**72**
DFT / BIST Requirements			
Scan pin count (per DUT)	**128**	**128**	**128**
Scan vector memory depth (megavectors)	**256**	**256**	**256**
Scan vector frequency (MHz)	**75**	**75**	**75**

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

MATERIAL HANDLING TECHNOLOGY REQUIREMENTS

Wafer probe and component test handling equipment face significant technical challenges in each market segment. Common issues on both platforms include thermal management, higher parallelism and increasing capital equipment cost. In 2001 this section is intended to introduce the key challenges facing material handling equipment over the next several years. In future versions of the roadmap this section will be enhanced to provide more detailed direction to the industry in the form of trends and difficult challenges.

Specific to wafer probe the technical trends affecting this equipment include fab process technology, increasing probe count, decreasing probe pitch/diameter and evolving probe tip geometries. These trends translate into challenges in the areas of DUT thermal management, wafer placement accuracy under load, chuck electrical isolation, and probe to pad alignment (PTPA) complexity.

Component test handling unique challenges include increasing power requirements, increasing pin count, reduced pitch, reduced packaging thickness/rigidity and surface mount components. These trends translate into requirements for active thermal control during test, higher socketing force, improved placement accuracy, and complex custom tooling. In addition, device sensitivity to ESD and EMI requires enhanced closed loop ESD solutions, exotic tooling materials, and DUT shielding.

Ultimately these issues are increasing cost of wafer probers and component test handlers, while structural and functional test equipment cost continue to decrease. Over the next several years, material handling equipment solutions will be required to meet increasing product requirements under increasing cost pressures.

DEVICE INTERFACE TECHNOLOGY REQUIREMENTS

As device analog and digital I/O bandwidth and power demands increase there is an associated requirements for high performance power and signal delivery. These requirements drive challenges for the assemblies used to interface the test equipment to the device-under-test. The highest performance interfaces require complete power and signal path modeling from the source instrument to the die, requiring accurate simulation models of the test instrument, path, probe or socket, and die. To further complicate matters, shrinking die and package geometries further complicate these interfaces with decreasing pitch and increasing pin count mechanical requirements.

For reference, the *2001 Update of the Probing Roadmap* from the Semiconductor Technology Roadmap of Japan (STRJ) published by the Japan Electronics and Information Technology Industries Association (JEITA) is included as a part of the supplemental material.

PROBE CARDS

Wafer probe technologies face complex electrical and mechanical challenges driven by product specifications, test implementation requirements, test productivity goals, and reduced test cost demands. Across the device spectrum, these challenges include: higher frequency response (bandwidth), rising pin counts across tighter pitches and smaller pads/bumps, increasing switching currents (di/dt), alternative pad/bump metallurgies and increasing test parallelism. Research and development of new or improved probe technologies is required to meet these challenges to ensure that the basic probing requirement of ensuring reliable, sound and cost-effective electrical contact to the device(s) under test (DUT) is achieved.

TRENDS AFFECTING PROBE CARD TECHNOLOGIES

Along with addressing the key challenges listed below, research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment.

The continuing volume growth (share of market) of bumped devices, often with I/Os in area arrays, points to the escalating demand for “vertical” style probe card technologies, with a rising need in multi-DUT configurations as well.

Increasingly, manufacturing test of devices is moving to parallel test. For some product groups (e.g., memory), current wafer probe technologies handle parallel testing of 32, 64 and even 128 devices. Probe technologies capable of further

increases in parallelism, including up to full wafer (up to 300mm), are needed to drive test costs lower. For some high pin count products, e.g. ASICS, parallel probing requirements are emerging.

Wafer probe electrical models that integrate models of other elements in the path from tester to DUT will be required of probe card suppliers. These models will be needed to conduct simulations of increasingly complex automated test equipment (ATE) to DUT interface networks to optimize performance at the DUT.

As new or advanced probe technologies are entering the marketplace, issues of single-sourcing, order to delivery time, probe lifetime, application support, and reparability are important and essential considerations in the selection of a probe card for use in volume production.

Table 33 Probe Card Difficult Challenges—Near-term

CHALLENGE	***ISSUE / GOAL***
High Frequency Probing	Traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40GHz.
Geometry	Probe technologies to support peripheral fine pitch probe of 44 µm, and peripheral staggered pad probes at effective pitches of 30/60. Fine pitch vertical probe technologies to support 100 µm pitch solder bump and staggered pad devices Reduction of pad damage at probe commensurate with pad size reductions (or better) Alternative probe technology for 3 on 6 mil. pitch dense array (vertical probe; bumped device) Increasing probe array planarity requirements in combination with increasing array size
Parallel Test	Need a probe technology to handle the complexity of System On Chip (SoC) devices while probing more than one device. Current probe technologies have I/O limitations for bumped device probes
Probing at Temperature	Reduce effects on probes for non-ambient testing -40 to 150°C; especially for fine-pitch devices
Product	Probe technologies to direct probe on copper bond pads including various oxidation considerations Probe technologies for probing over active circuitry (including flip-chip) Reduction of probe force requirements to eliminate die damage
Probe Cleaning	Development of *in situ* cleaning mediums/methods, particularly for fine pitch, multi-DUT and non-traditional probes Reduction of cleaning requirements while maintaining electrical performance to increase lifetime
Cost and Delivery	Fine pitch or high pin count probe cards are too expensive and take too long to build. Time and cost to repair fine pitch or high pin count probe cards is very high. The time between chip design completion ("tape-out") and the availability of wafers to be probed is less than the time required to design and build a probe card in almost every probe technology except traditional cantilever. Space transformer lead times are too long, thus causing some vertical probe technologies to have lengthy lead-times.
Probe Metrology	Tools are required that support fine pitch probe characterization and pad damage measurements. Metrology correlation is needed—repair versus on-floor usage

POTENTIAL SOLUTIONS

Figure 20 shows the high level Potential Solutions for Test and Test Equipment.

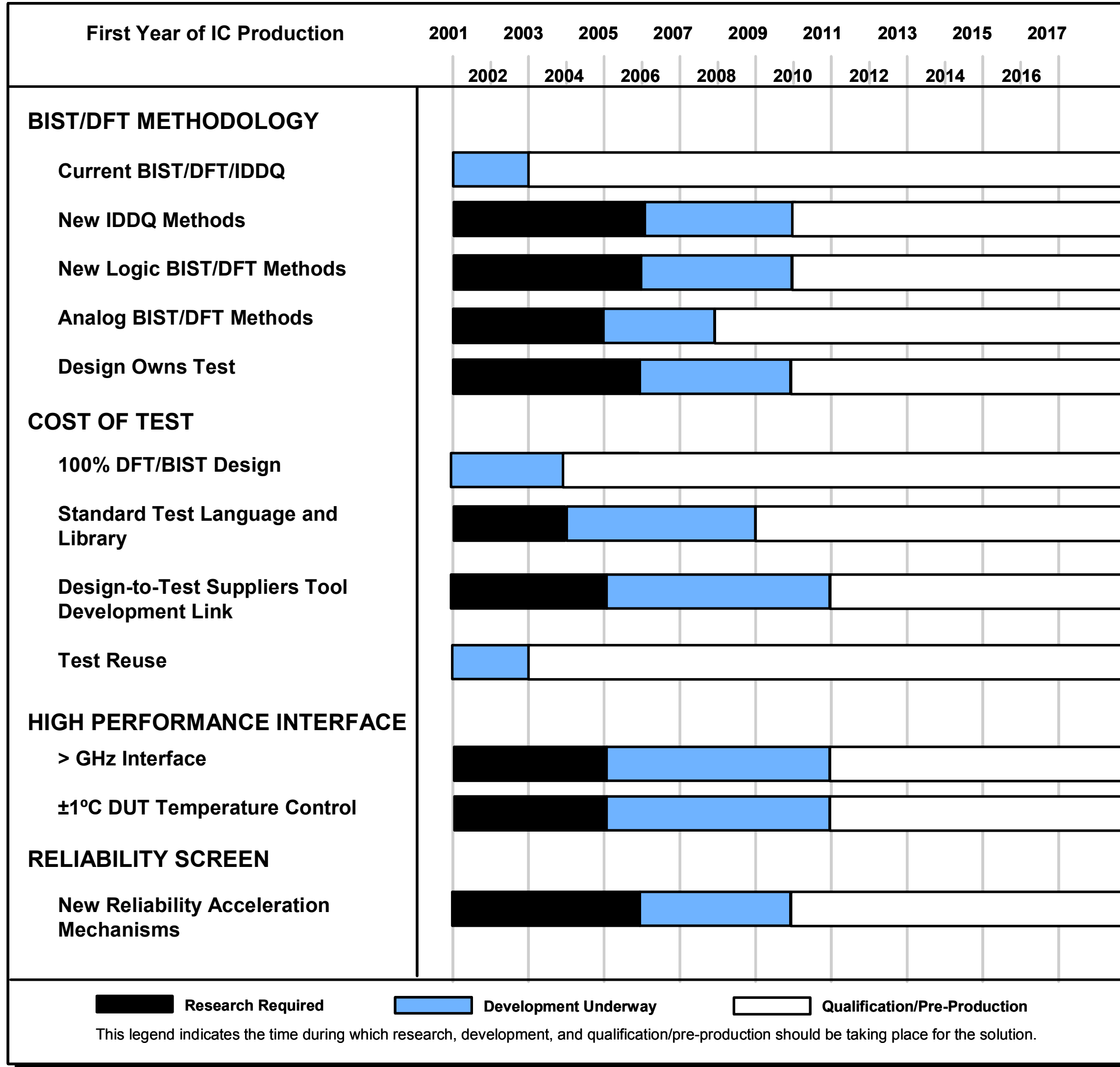


Figure 20 Test and Test Equipment Potential Solutions