INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2001 EDITION

YIELD ENHANCEMENT

Table of Contents

Scope 1
Difficult Challenges 1
  Needed Research 2
Technology Requirements 3
  Yield Model and Defect Budget 3
  Defect Target Calculator 6
  Defect Detection and Characterization 7
  Yield Learning 10
    Visible Defects 10
    Non-visual Defects 10
    Parametric Defects 10
    Electrical Faults 11
    Data Management Systems 11
  Wafer Environmental Contamination Control 14
Potential Solutions 19
  Yield Model and Defect Budget 19
  Defect Detection and Characterization 21
  Yield Learning 23
    Visible Defects 23
    Non-visual Defects 23
    Parametric Defects 24
    Electrical Faults 24
    Data Management Systems (DMS) 24
  Wafer Environmental Contamination Control 25

List of Figures

Figure 56 General Test Methodology for Ultrapure Water 15
Figure 57 Yield Model and Defect Budget Potential Solutions 20
Figure 58 Defect Detection and Characterization Potential Solutions 22
Figure 59 Yield Learning Potential Solutions 25
Figure 60 Wafer Environmental and Contamination Control Potential Solutions 26

LIST OF TABLES

Table 88 Yield Enhancement Difficult Challenges 2
Table 89 Defect Budget Technology Requirement Assumptions....................3
Table 90 Yield Model and Defect Budget MPU Technology Requirements....................4
Table 91 Yield Model and Defect Budget DRAM Technology Requirements....................5
Table 92 Defect Target Calculator....................6
Table 93a Defect Detection Technology Requirements—Near-term....................8
Table 93b Defect Detection Technology Requirements—Long-term....................9
Table 94a Yield Learning Technology Requirements—Near-term....................12
Table 94b Yield Learning Technology Requirements—Long-term....................13
Table 95a Technology Requirements for Wafer Environmental Contamination Control—Near-term....................17
Table 95b Technology Requirements for Wafer Environmental Contamination Control—Long-term....................18

YIELD ENHANCEMENT

SCOPE

The Yield Enhancement Chapter is partitioned into four focus topics: *Yield Model and Defect Budget, Defect Detection and Characterization, Yield Learning, and Wafer Environment(s) Contamination Control*. Key business metrics rely on the success of rapid yield ramp and the associated competencies found within these four focus topics. These competencies crosscut all process technologies, as well as the facility infrastructure, integrated circuit (IC) design, and process integration. Key messages include continued emphasis on reduction of process- and equipment-generated defects to meet defect targets for mature product yields. Significant efforts will be necessary to baseline, reduce and control yield loss associated with systematic mechanisms. Defect-to-fault and fault-to-defect mapping, kill ratios, and failure isolation techniques are also critical challenges as physical device dimensions and corresponding defect dimensions continue to shrink. There must be renewed and funded development of defect detection, review, and classification technologies where much greater sensitivity and throughput is necessary. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and WIP data, will have to be developed to enable rapid yield learning. Specific recommendations are needed for standard monitor-wafer preparation, detection recipes, edge exclusion, test structures, short/long loops and sampling to ensure line control and yield improvement. Order-of-magnitude improvements in process critical fluid and gas impurity levels are not believed to be necessary well into the sub-90 nm technology nodes. Clarification of potential contamination from point-of-delivery to point-of-use will define control systems necessary for delivered purity. Pre-cursors for new dielectric materials will need to be evaluated.

The shift in definition of this chapter from defect reduction to yield enhancement leads to its expansion into previously non-addressed areas of concern. For example, non-defect related yield loss from parametric test, circuit probe, and package test will now be examined. Other areas such as edge-die recovery will also be included in the scope of the chapter. These issues will be incorporated in the continuing annual revisions.

DIFFICULT CHALLENGES

The difficult challenges for yield enhancement technologies are summarized in Table 88. Defect budgets will require frequent revalidation and updates, as information about future processing technologies becomes available. Yield models need to better consider complex integration issues with respect to random defect-limited yield as well as systematic limited yield (such as parametric yield loss, circuit yield loss, etc.) for future technology nodes. Future defect models must consider electrical characterization information, with reduced emphasis on optical inspections and analysis. Detecting defects associated with high aspect ratio contacts, and combinations of trenches and vias in dual-damascene structures will continue to be difficult defect detection challenges. More specifically, the detection of via defects within the structure of a damascene trench on a process layer containing up to 10 billion similar structures will continue to be the grand challenge. The challenge is complicated by the simultaneous need for high sensitivity and high throughput, two detection characteristics that normally are caught in a tradeoff as the fabrication facility moves from optimization of tool performance for baseline yield learning to production line monitoring. Fault isolation complexity is expected to grow exponentially, combining the difficult tasks of defining fault dimensions in the horizontal plane and vertical layers (stack). Analyzing circuit failures that leave no detectable physical remnant presents an extremely difficult challenge. Statistical means of accurately dealing with near-zero defect adder data that frequently exhibit high coefficients of variation is a fundamental data reduction challenge. Through the use of advanced test structures and modeling techniques, the fundamental challenge in the area of process critical materials is to understand the correlation between impurity concentration and device yield, reliability, and performance. This correlation will determine whether increasingly stringent contamination limits are truly required and will provide early warning of the need for tighter specifications. Process tools must have increased capability to automatically self-monitor production for yield excursions, failures, and faults and to initiate corrective actions.

Table 88 Yield Enhancement Difficult Challenges

DIFFICULT CHALLENGE ≥ 65 nm, THROUGH 2007	SUMMARY OF ISSUES
Develop and Validate Systematic Yield Models—Process-induced defects, equipment generated particles, product/processing measurements, and design/layout sensitivities have to be correlated to yield.	Correlate process-induced defects (PID), particles per wafer pass (PWP), product inspections, and *in situ* measurements. Develop parametric and process-to-design mismatch yield-loss models. Address sampling and statistical issues with ultra-small populations. Increase Yield Model accuracy.
High Aspect Ratio Inspection—High-speed cost-effective tools must be developed that rapidly detect defects associated with high-aspect-ratio contacts/vias/trenches, and particularly defects near/at the bottom of these features.	Poor transmission of energy into bottom of via and back out to detection system. Large number of contacts and vias per wafer
Defect/Fault Sourcing for Rapid Yield Learning—Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test, and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed. Automated data/image mining and reduction algorithms must be developed to source defects from multiple data sources (facility, design, process and test)
Correlation of Impurity Level to Yield—Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product.	Establish an employment methodology for each material type. Define a standard test for yield/parametric effect.
DIFFICULT CHALLENGE < 65 NM, BEYOND 2007	SUMMARY OF ISSUES
Develop Yield Models that Include New Materials and Integration-Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.
Non-visual Defect Sourcing and Design for Manufacture and Test—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected. Also, IC designs must be optimized for a given process capability and must be testable/diagnosable.	Many defects that cause electrical faults are not detectable inline. Tools are needed that enable design to process matching for optimum yields. Also, testability/ability to diagnose must be designed into the IC for rapid electrical failure sourcing.
Precursors for New Materials—Required purity levels for delivered dielectric pre-cursors are not known or well understood.	Establish methodology for establishing purity standards for new dielectric pre-cursors.

NEEDED RESEARCH

The research and paths to potential solutions for the Yield Model, Defect Budget, and for Yield Learning are well mapped in the illustrations below. Continued cooperation from semiconductor manufacturers is required for accurate validation of the Yield Model. Innovative algorithms for defect sourcing will be required for rapid Yield Learning, particularly when the electrical fault has no detectable optical or SEM image.

For High Aspect Ratio Inspection (HARI) applications and at defect sizes below 100nm (diameter), defect detection and characterization will be hampered by detection tools having low throughput and high cost-of-ownership. An economical solution must be found if large risk to production inventory is to be avoided.
Wafer Environment(s) Contamination Control must center attention on the point of use of a pure material since realistic cost of manufacture must be maintained. Innovative ideas need to be studied, such as local filtering of only undesirable contaminants from a re-usable process gas/fluid. Vendors for pre-cursors for new dielectric materials will need to examine their purity requirements using a standardized method.

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

$$Y_{Die} = Y_S * Y_R = Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha}$$

The overall die yield of an IC process can broadly be described as a product of systematic (or gross) limited yield (Y_S) and random-defect limited yield (Y_R). The defect budget technology requirements defined in Tables 90 and 91 are based on a negative binomial yield model where Y_R is the random-defect limited yield, A is the area of the device, D_0 is the electrical fault density, and α is the cluster factor. Assumptions for the defect budget technology requirements in this revision are indicated in Table 89. The defect budget target calculation for the 2001 ITRS is based on results of three studies (1997, 1999, and 2000) of particles per wafer pass (PWP) levels at international SEMATECH member companies. These targets were extrapolated from median PWP value per generic process tool type and then scaled to a MPU and DRAM generic process-flow respectively. Note that the defect budget targets for all process steps include wafer-handling defectivity of the process tool. In addition a 10% wafer per lot sampling rate for inspection and measurement was assumed.

$$PWP_n = PWP_{n-1} \times \frac{F_n}{F_{n-1}\left(\frac{S_{n-1}}{S_n}\right)^2}$$

This PWP extrapolation equation was used to calculate PWP budget values from technology node to technology node. The extrapolation takes into consideration increase in chip size, increase in complexity, and shrinking feature size. In this equation PWP is the particles per wafer pass defect density per square meter, F is the average faults per mask level (determined by the random electrical fault density (D_0) divided by number of masks at a given technology node), S is the minimum critical defect size, and n refers to the technology node. All PWP budget values are defined with respect to a 75 nm critical defect size. Each entry in the PWP section of Tables 90 and 91 refers to a generic tool type used in the MPU and/or in the DRAM process flow. Since future actual tools and processes are not known, this roadmap assumes that no new process, material, or tool will be acceptable with a larger PWP budget than prior methods. This assumption needs periodic validation. This defect budgeting method tends to be a worst-case model since all process steps are assumed to be at minimum device geometry. In actuality, many processes allow process zones with more relaxed geometries. However, the same tools are used for both minimum and relaxed geometries. The costs of underestimating yield (unused capacity costs) are small and may be offset by the opportunity for additional production. The major driver for increased cost due to overestimating yield is the cost of scrapped material. Thus, a worst-case defect budgeting model is prudent.

Table 89 states the yield, and the product maturity assumptions that were used in calculating electrical fault density values and PWP defect budget target values for MPUs and DRAMs respectively. These assumptions for the most part are as defined in the ORTC. Table 90 presents the random PWP defect budget targets necessary to meet the stated assumptions for a cost-performance MPU as defined in the *ORTC Table 1a*. This MPU is assumed to have a small L1 cache, but the device consists primarily of logic transistor functionality. With respect to MPUs, this analysis assumes that the process/design improvement target factor (*ORTC Table 1b*) in each technology node is met. Similarly, Table 91 presents the random PWP budget targets necessary to meet the yield assumptions stated in Table 89 for DRAMs. The electrical fault density that is used to calculate faults per mask level (which is used as input to the PWP extrapolation equation) is based on only the periphery (logic/decoder) area of the DRAM chip. This is projected in the ORTC to be 45% of chip area at the stated product maturity. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM can implement redundancy to attain the overall yield target of 85%. A calculator for scaling the contents of Table 90 and 91 to specific user yield, technology, and chip size requirements is included in this ITRS revision as Table 92.

Table 89 Defect Budget Technology Requirement Assumptions

PRODUCT	*MPU*	*DRAM*
YIELD RAMP PHASE	*VOLUME PRODUCTION*	*VOLUME PRODUCTION*
$Y_{OVERALL}$	**75%**	**85%**
Y_{RANDOM}	**83%**	**89.5%**
$Y_{SYSTEMATIC}$	**90%**	**95%**
Cluster Parameter	**5**	**5**

Table 90 Yield Model and Defect Budget MPU Technology Requirements

Year of Production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	45	32	22
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	50	35	25
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	25	18	13
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	18	13	9
MPU										
MPU ½ metal one Pitch (nm) [A]	**150**	**130**	**107**	**90**	**80**	**70**	**65**	**45**	**32**	**22**
Critical Defect Size (nm)	**75**	**65**	**54**	**45**	**40**	**35**	**33**	**23**	**16**	**11**
Chip Size (mm2) [B]	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**
Random D_0 (faults/m^2) [D]	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**
# Mask Levels [E]	**25**	**25**	**25**	**25**	**25**	**27**	**27**	**27**	**29**	**29**
Random Faults/Mask	**54**	**54**	**54**	**54**	**54**	**50**	**50**	**50**	**47**	**47**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type scaled to 75nm critical defect size or greater										
CMP Clean	**448**	**337**	**228**	**161**	**127**	**90**	**78**	**37**	**18**	**8**
CMP Insulator	**1084**	**814**	**552**	**390**	**308**	**219**	**189**	**90**	**43**	**20**
CMP Metal	**1225**	**920**	**623**	**441**	**348**	**247**	**213**	**102**	**48**	**23**
Coat/Develop/Bake	**196**	**147**	**100**	**70**	**56**	**39**	**34**	**16**	**8**	**4**
CVD Insulator	**963**	**772**	**523**	**370**	**292**	**207**	**179**	**86**	**40**	**19**
CVD Oxide Mask	**1267**	**950**	**644**	**455**	**360**	**255**	**220**	**105**	**50**	**23**
Dielectric Track	**308**	**232**	**157**	**111**	**88**	**62**	**54**	**26**	**12**	**6**
Furnace CVD	**549**	**412**	**279**	**198**	**156**	**111**	**95**	**46**	**22**	**10**
Furnace Fast Ramp	**497**	**373**	**253**	**179**	**141**	**100**	**86**	**41**	**19**	**9**
Furnace Oxide/Anneal	**321**	**241**	**164**	**116**	**91**	**65**	**56**	**27**	**13**	**6**
Implant High Current	**430**	**323**	**219**	**155**	**122**	**87**	**75**	**36**	**17**	**8**
Implant Low/Med Current	**392**	**295**	**200**	**141**	**112**	**79**	**68**	**33**	**15**	**7**
Inspect PLY	**400**	**300**	**203**	**144**	**114**	**81**	**70**	**33**	**16**	**7**
Inspect Visual	**429**	**323**	**219**	**155**	**122**	**87**	**75**	**36**	**17**	**8**
Litho Cell	**332**	**250**	**169**	**120**	**95**	**67**	**58**	**28**	**13**	**6**
Litho Stepper	**315**	**237**	**160**	**113**	**90**	**64**	**55**	**26**	**12**	**6**
Measure CD	**374**	**281**	**190**	**135**	**106**	**75**	**65**	**31**	**15**	**7**
Measure Film	**321**	**241**	**164**	**116**	**91**	**65**	**56**	**27**	**13**	**6**
Measure Overlay	**298**	**224**	**152**	**107**	**85**	**60**	**52**	**25**	**12**	**6**
Metal CVD	**585**	**439**	**298**	**211**	**166**	**118**	**102**	**49**	**23**	**11**
Metal Electroplate	**302**	**227**	**154**	**109**	**86**	**61**	**52**	**25**	**12**	**6**
Metal Etch	**1300**	**976**	**661**	**468**	**370**	**262**	**226**	**108**	**51**	**24**
Metal PVD	**667**	**501**	**339**	**240**	**190**	**135**	**116**	**56**	**26**	**12**
Plasma Etch	**1183**	**889**	**602**	**426**	**336**	**239**	**206**	**99**	**46**	**22**
Plasma Strip	**547**	**411**	**278**	**197**	**156**	**110**	**95**	**46**	**21**	**10**
RTP CVD	**357**	**268**	**181**	**128**	**101**	**72**	**62**	**30**	**14**	**7**
RTP Oxide/Anneal	**234**	**175**	**119**	**84**	**66**	**47**	**41**	**19**	**9**	**4**
Test	**91**	**69**	**47**	**33**	**26**	**18**	**16**	**8**	**4**	**2**
Vapor Phase Clean	**822**	**617**	**418**	**296**	**234**	**166**	**143**	**68**	**32**	**15**
Wafer Handling	**37**	**28**	**19**	**13**	**10**	**7**	**6**	**3**	**1**	**1**
Wet Bench	**535**	**402**	**272**	**192**	**152**	**108**	**93**	**45**	**21**	**10**

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

[A] As defined in the ORTC Table 1a

[B] As defined in the ORTC Table 2a

[C] As defined in the ORTC Table 5a

[D] Based on assumption of 83% Random Defect Limited Yield (RDLY)

[E] As defined in the ORTC Table 5a

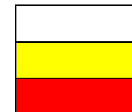
Table 91 Yield Model and Defect Budget DRAM Technology Requirements

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65	45	32	22
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65	50	35	25
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25	18	13	9
DRAM										
DRAM ½ PITCH (nm) [A]	130	115	100	90	80	70	65	45	32	22
CRITICAL DEFECT SIZE (nm)	65	58	50	45	40	35	33	23	16	11
CHIP SIZE (mm^2) [B]	127	100	118	93	147	116	183	181	240	238
CELL ARRAY AREA (%) @ PRODUCTION	55%	55%	56%	56%	56%	57%	57%	58%	58%	58%
NON-CORE AREA (mm^2)	57	45	52	41	64	50	79	77	101	99
OVERALL ELECTRICAL D_0 (FAULTS/m^2) AT CRITICAL DEFECT SIZE OR GREATER [C]	2890	3671	3163	4047	2580	3293	2100	2155	1643	1670
RANDOM D_0 (FAULTS/m^2) [D]	1963	2493	2148	2748	1752	2236	1426	1464	1116	1134
# MASK LEVELS [E]	21	22	24	24	24	24	24	26	26	26
RANDOM FAULTS/MASK	93	113	89	115	73	93	59	56	43	44
DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type scaled to 75nm critical defect size or greater										
CMP Clean	1076	1021	610	632	318	311	171	78	30	14
CMP Insulator	833	790	472	489	246	241	132	60	23	11
CMP Metal	1276	1211	723	750	378	369	203	92	36	17
Coat/Develop/Bake	333	316	188	195	98	96	53	24	9	4
CVD Insulator	923	876	523	542	273	267	147	67	26	12
CVD Oxide Mask	1133	1075	642	665	335	327	180	82	32	15
Dielectric Track	467	443	264	274	138	135	74	34	13	6
Furnace CVD	638	605	361	374	189	184	101	46	18	9
Furnace Fast Ramp	601	571	341	353	178	174	96	43	17	8
Furnace Oxide/Anneal	481	456	272	282	142	139	76	35	13	6
Implant High Current	559	530	316	328	165	161	89	40	16	7
Implant Low/Med Current	533	506	302	313	158	154	85	38	15	7
Inspect PLY	729	691	413	428	216	211	116	53	20	10
Inspect Visual	752	713	426	441	222	217	119	54	21	10
Litho Cell	624	592	354	367	185	180	99	45	17	8
Litho Stepper	415	394	235	244	123	120	66	30	12	6
Measure CD	623	591	353	366	184	180	99	45	17	8
Measure Film	586	556	332	344	173	169	93	42	16	8
Measure Overlay	570	541	323	335	169	165	91	41	16	8
Metal CVD	587	557	333	345	174	170	93	42	16	8
Metal Electroplate	446	423	253	262	132	129	71	32	12	6
Metal Etch	1080	1025	612	634	320	312	172	78	30	14
Metal PVD	644	611	365	378	191	186	102	46	18	9
Plasma Etch	1144	1085	648	672	338	331	182	83	32	15
Plasma Strip	878	833	497	516	260	254	140	63	24	12
RTP CVD	574	545	325	337	170	166	91	41	16	8
RTP Oxide/Anneal	420	398	238	247	124	121	67	30	12	6
Test	82	78	46	48	24	24	13	6	2	1
Vapor Phase Clean	1215	1152	688	713	359	351	193	88	34	16
Wafer Handling	34	33	20	20	10	10	5	2	1	0
Wet Bench	870	825	493	511	257	251	138	63	24	12

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



[A] As defined in the ORTC Table 1a

[B] As defined in the ORTC Table 2a

[C] As defined in the ORTC Table 5a)

[D] Based on assumption of 89.5% Random Defect Limited Yield (RDLY

[E] As defined in the ORTC Table 5a

DEFECT TARGET CALCULATOR

The random defect targets in Tables 90 and 91 are based on predefined technology nodes, using data collected by International SEMATECH member companies on 164 tools, which are divided into 30 generic tool categories. Even with targets for both memory and logic products, rarely do actual user circuit line widths and areas match the ITRS technology node assumptions. Therefore Wright Williams & Kelly developed a defect target calculator[1] to help semiconductor suppliers and manufacturers compare the roadmap targets to their current or planned needs.

Instructions

The defect target calculator, shown as a *static* example as Table 92, allows users to enter key technology parameters and estimate a defect target for a specific chip.

To be able to activate click once here for the live version file of this calculator or right click to download the file to your computer.

The only parameters required are the ***Minimum Critical Defect Size***, ***Random Defect Limited Yield Requirement***, ***Chip Size***, ***Number Of Mask Levels,*** *and for memory only,* ***the Peripheral (Logic) Chip Area***. This calculator uses the same extrapolation method as the roadmap tables.

Definitions

Minimum Critical Defect Size—One half the user's metal 1 pitch for the technology of interest (nanometers)

Random Defect limited Yield—Portion of your yield, which is reduced based on your random defectivity. Has to be multiplied by the systematic limited yield to calculate the overall die yield (%)

Chip Size—The area (critical or hole die size) of the user's device (square millimeters)

Mask Levels—The number of mask levels in the user's technology

Peripheral (Logic) Chip Area—Area of the layout without redundancy, chip area minus cell area (%). Only used in the DRAM calculation

Table 92 Defect Target Calculator

	USER INPUT	
Minimum Critical Defect Size (nm)	75	
Random Defect limited Yield (%)	83.0%	
Chip Size (mm^2)	140	
Number of Mask Levels	25	
Peripheral (Logic) Chip Area (%)	100.0%	
Random D_0 (faults/m^2)	1356	1356
Random Faults/Mask	54	54
	User Targets	
	MPU	*DRAM*
CMP Clean	448	828
CMP Insulator	1084	641
CMP Metal	1225	983
Coat/Develop/Bake	196	256
CVD Insulator	963	711
CVD Oxide Mask	1267	872
Dielectric Track	308	359
Furnace CVD	549	491
Furnace Fast Ramp	497	463
Furnace Oxide/Anneal	321	370
Implant High Current	430	430
Implant Low/Medium Current	392	410
Inspect PLY	400	561
Inspect Visual	429	579
Lithography Cell	332	481
Lithography Stepper	315	319
Measure CD	374	479
Measure Film	321	451
Measure Overlay	298	439
Metal CVD	585	452
Metal Electroplate	302	343
Metal Etch	1300	832
Metal PVD	667	496
Plasma Etch	1183	881
Plasma Strip	547	676
RTP CVD	357	442
RTP Oxide/Anneal	234	323
Test	91	63
Vapor Phase Clean	822	935
Wafer Handling	37	27
Wet Bench	535	669

[1] *Developed by Darren Dance, Wright, Williams, and Kelly. 1999.*

DEFECT DETECTION AND CHARACTERIZATION

The ability to detect inline yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production—process research and development (PRD), yield ramp (YR), and volume production (VP)—broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabs begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the chip manufacturers just-in-time for each phase of the process cycle. Tools that meet the requirements for PRD are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate YR must be available several months before production begins. Finally, the ability to monitor excursions at a technology node is needed when the product hits high yield levels.

Technology requirements are separated into unpatterned wafer inspection, patterned wafer inspection, and high aspect ratio inspection, as shown in Table 93. The effects of the buried patterning in post-chemical mechanical planarization (CMP) wafers makes patterned wafer inspection with grazing angle laser inspection tools approximate unpatterned inspection for the purposes of tool qualification, and appropriate for this roadmap. Also, unpatterned inspection utilized extensively for tool qualification, has implemented defect review from such scans, which has increased in importance in the last few years. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is treated separately from patterned wafer inspection due to special sensitivity requirements described in the *Difficult Challenges* section as well as note C under Table 93. Best HARI defect detection tools will be able to indicate 0.3 × technology node events for contact and via shape (defined at the bottom of the feature: highest resistive point), size, and remaining material, which is the optimum HARI defect definition. Again, current Table 93 revisions have the defect size at full feature, as detected by the current methods of voltage contrast, but manufacturing inputs still desire the .3× feature size due to detrimental resistivity impacts.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside requirements are based on lithography depth-of-focus considerations as stipulated in the *Lithography* chapter Technology Requirements table, and also defined slightly differently in the *Front End Process* Starting Materials table, and Surface Preparation table.

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers (defects that cannot be detected with conventional optical technologies) is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and back end of processing. Macro defects that impact large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved to match the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology node.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The price, fab space occupied, and the throughput of defect detection tools are major contributors to their cost-of-ownership (CoO). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table 93 have been stipulated on the basis of detecting accurately sized Polystyrene Latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pattern flaws, and scratches. There is an urgent need for the development of a

defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

Defects detected on future technology generation wafers will require higher resolution microscopes for review. Rapid developments in Scanning Electron Microscopy (SEM) have already enabled quick review and classification of such defects. Speeding up SEM review could provide the opportunity to gather information on more defects than currently possible, thereby increasing yield learning.

Table 93a Defect Detection Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007	Driver
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
MPU PRINTED GATE LENGTH (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
MPU PHYSICAL GATE LENGTH (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]*								
Process R&D at 300 cm^2/hr (1 wafer/hr)	78	72	66	54	48	42	39	*0.6 x DR*
Yield ramp at 1200 cm^2/hr (4 wafer/hr)	104	96	88	72	65	56	52	*0.8 x DR*
Volume production at 3000 cm^2/hr (10 wafer/hr)	130	120	110	90	80	70	66	*1.0 x DR*
*High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]*								
All stages of manufacturing	130	120	110	90	80	70	65	*1.0 x DR*
Process verification (1 wafer/hr)	130	120	110	90	80	70	65	*1.0 x DR*
Volume manufacturing (4 wafer/hr)	130	120	110	90	80	70	65	*1.0 x DR*
Cost of Ownership :volume manufacturing, non-HARI ($/wafer scanned, 10/hr)	2–5	2–5	2–5	3–7	3–7	3–7	3–7	
CoO HARI	20–50	20–50	20–50	20–50	20–50	20–50	20–50	
*Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]*								
Metal film	91	85	77	32	56	35	33	*0.5 x DR*
Nonmetal films	70	65	59	49	43	35	33	*0.5 x DR*
Bare silicon	70	65	59	49	43	35	33	*0.5 x DR*
Wafer backside 200mm (# events flip method)	2500	2000	2000	2000	2000	2000	1000	
Wafer backside 200mm (defect size nm)	200	200	200	200	100	100	100	
Defect Review (Patterned wafer)								
Resolution (nm) *[F]	7	7	6	5	5	4	3	*0.05 x DR*
Coordinate accuracy (µm) at resolution	2	2	1	1	1	1	1	*(J)*
Coordinate accuracy (µm) at size	15	12	12	10	10	7	7	
*Automatic Defect Classification at Defect Review Platform *[G, H]*								
Redetection: minimum defect size (nm)	52	48	44	36	30	28	26	*0.4 x DR*
Number of defect types	10	10	10	15	15	15	15	*[K]*
Speed (seconds/defect)	7	5	5	5	5	5	5	
Speed w/elemental (seconds/defect)	20	15	13	10	10	10	10	

**polystyrene latex ; spheres utilized to simulate defects of known size during sizing calibration.*

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow–Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

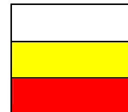


Table 93b Defect Detection Technology Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*	*Driver*
DRAM ½ Pitch (nm)	*45*	*32*	*22*	
MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*	
MPU Printed Gate Length (nm)	*25*	*18*	*13*	
MPU Physical Gate Length (nm)	*18*	*13*	*9*	
Patterned Wafer Inspection, PSL Spheres at 90% Capture				
Process R&D at 300 cm^2/hr (1 wafer/hr)	**27**	**19**	**13**	*0.6 x DR*
Yield ramp at 1200 cm^2/hr (4wafer/hr)	**36**	**26**	**18**	*0.8 x DR*
Volume production at 3000 cm^2/hr (10wafer/hr)	**46**	**32**	**22**	*1.0 x DR*
High Aspect Ratio Feature Inspection: Defects other than Residue				
All stages of manufacturing	**45**	**32**	**22**	*1.0 x DR*
Process verification (1 wafer/hr)	**45**	**32**	**22**	*1.0 x DR*
Volume manufacturing (4 wafer/hr)	**45**	**32**	**22**	*1.0 x DR*
Cost of Ownership volume manufacturing, non-HARI ($/wafer scanned, 10 /hr)	**3 - 7**	**3 - 5**	**3 - 5**	
CoO HARI	**20 - 50**	**20 - 50**	**20 - 50**	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [D, E]				
Metal film	**23**	**16**	**11**	*0.5 x DR*
Nonmetal films	**23**	**16**	**11**	*0.5 x DR*
Bare silicon	**23**	**16**	**11**	*0.5 x DR*
Wafer backside 200mm (# events flip method)	**1000**	**1000**	**500**	
Wafer backside 200mm (defect size nm)	**100**	**60**	**50**	
Defect Review (Patterned wafer)				
Resolution (nm) *[F]	**3**	**2**	**2**	*0.05 x DR*
Coordinate accuracy (µm) at resolution	**0.5**	**0.5**	**0.5**	*[J]*
Coordinate accuracy (µm) at size	**5**	**5**	**5**	
Automatic Defect Classification at Defect Review Platform				
Re-detection minimum defect size (nm)	**18**	**13**	**9**	*0.4 x DR*
Number of defect types	**20**	**20**	**25**	*[K]*
Speed (seconds/defect)	**5**	**5**	**5**	
Speed w/elemental (seconds/defect)	**10**	**10**	**10**	

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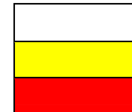

Notes for Table 93a and b:

[A] Patterned wafer scan speed is required to be at least 300 cm^2 /hour for process R&D mode, 1,200 cm^2 /hour for yield ramp mode, and, at least, 3,000 cm^2 /hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435. (Example-- 3000 cm^2 /hr is about 10, 200 mm wafers and 4.3, 300 mm wafers).

[B] Patterned wafer nuisance defect rate shall be lower than 5% in all process phases. False counts in the R&D phase less than 5%, and less than 1% in the yield ramp and volume production phase. Nuisance is defined as an event indicated and a defect is present, just not the type of interest. These maybe significant and could be studied at a later date. The defect classifier must consider the defect type and assign significance. False is defined at an event is indicated, but no defect can be seen using the review optics path of the detection tool, which supports recipe setup validation.

[C] HARI defects are already considered "killers" at any process stage, but defined at the contact/via levels for full feature size capture. Hence, minimum defect sensitivity was stipulated as 1.0× technology node at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more is the model to be detected. If in the future, detection tools can determine size, shape, or remaining material on the order of 0.3× technology node, this will more adequately match known experience for resistance changes. Scan speed for HARi tools have been broken out into process verification and volume production types. Process verification usually refers to SEM-type tools (but not necessarily in the future) and includes voltage contrast capability. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435.

Cost of Ownership is derived from the elements found in the International SEMATECH Metrology Tool Model.

[D] Unpatterned wafer defect detection tools will be required to scan 150 (200 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually.

[E] Metal films inspection tools must detect defects greater than half the minimum contacted pitch (Interconnect chapter technology requirements) × 0.6 (process R&D requirement for patterned wafer defects) for non-grainy films and × 0.6 for rough or grainy films. Nonmetal films and bare Si detection sensitivity must be at least as good as that for patterned wafer inspection to justify monitor wafer usage.

Backside wafer particles are specified as events found at the size indicated. The yellow indication is due to only some inspection tools being capability of meeting this added particle spec.

[F] Resolution corresponds to 10% of patterned wafer detection sensitivity for volume production.

[G] ADC: Detectability, as % of defects redetected, should be greater than 95; Accuracy, as the % of defects correctly classified as per a human expert, should be greater than 95; Repeatability should be greater than 95%; and Reproducibility, as COV%, should be no greater than 5%.

[H] Assumptions: 5,000 wafer starts per month, defects per wafer based on surface preparation at FEOL, leading to defects per hour

that need review, 100% ADC.

[I] Backside defects for 300 mm wafers is approximated by multiplying the 200 mm table values by 2.373. The defect sizes remain the same.

[J] Driver is redetection by SEM ADC instrument at a 5000× field of view.

[K] The trend of increasing numbers of defect types, read across the table, is also to indicate decreasing defect size.

YIELD LEARNING

Rapid identification of defect and fault sources through integrated data management is the essence of rapid yield learning. Table 94 presents the technology requirements for the yield learning focus topic. Learning must proceed at an accelerated rate to maintain the yield ramp from introduction to maturity within the expected timeline despite the growth in circuit complexity and the amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. At future technology nodes, the time necessary to source manufacturing problems must at least remain constant, approximately 50% of the process cycle time on average, during yield ramp. In the face of this increased complexity, strategies and software methods for integrated data management (IDM) have been identified as critical for maintaining productivity. IDM must comprehend integrated circuit design, visible and non-visual defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the IDM system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. IDM will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as automatic defect classification (ADC) and spatial signature analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information. The technology requirements for various types of defects are described below.

VISIBLE DEFECTS

Tools are needed to detect, review, classify, analyze, and source continuously shrinking visible defects.

NON-VISUAL DEFECTS

Defects that cause electrical failure but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-visual defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-visual defects) will become increasing challenging. Techniques need to be developed that rapidly isolate failures and partitions them into those caused by visible defects, non-visual defects, and parametric issues.

PARAMETRIC DEFECTS

As minimum feature size decreases, the systematic defect limited yield (Ys) decreases as well. A major contributor to the Ys component of yield is parametric variation within a wafer and wafer-to-wafer. Parametric defects have traditionally been referred to as "non-visual defects". However, parametric defects require separation from the "non-visual defects" for rapid sourcing.

ELECTRICAL FAULTS

As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the number of transistors per unit area (cm^2) times the number of process steps, forming the defect sourcing complexity factor as shown in Table 94. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity.

DATA MANAGEMENT SYSTEMS

The current practice in data management system (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient IDM is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect and fault sourcing capabilities, methods must be established for integrating workflow information (such as WIP data) with the DMS, particularly in commercial DMS systems. This will be important when addressing issues of advanced process and tool control beyond simple tool shutdown, such as lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time-based data such as that generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time-based data such that it can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

Table 94a Yield Learning Technology Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Wafer size (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Number of mask levels	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Number of processing steps	**490**	**503**	**516**	**530**	**543**	**556**	**570**
Cycle time during ramp (# days)	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Defect/Fault Sourcing Complexity [A], [G]							
Logic transistor density/cm^2 (1E6)	**14**	**19**	**26**	**35**	**47**	**63**	**85**
Defect sourcing complexity factor (1E9) [B]	**7**	**10**	**13**	**18**	**25**	**35**	**49**
Defect sourcing complexity trend [C]	**1**	**1**	**2**	**3**	**4**	**5**	**7**
Data Analysis for Rapid Defect/Fault Sourcing							
Patterned wafer inspection sensitivity (nm) during yield ramp	**104**	**96**	**88**	**72**	**64**	**56**	**52**
Average # of inspections/wafer during full flow	**5**	**5**	**5**	**5.4**	**5.4**	**5.4**	**5.8**
Defect data volume (DV) (# data items/wafer) (1E13) [D]	**5.5**	**7.1**	**9.4**	**12.5**	**15.8**	**20.7**	**25.7**
Defect data volume (DV) trend [E]	**1**	**1**	**2**	**2**	**3**	**4**	**5**
Yield Learning During Ramp from 30% to 80% Sort Yield [F]							
# of yield learning cycles/year based on full flow cycle time	**14.6**	**14.6**	**14.6**	**13.5**	**13.5**	**13.5**	**12.6**
Required yield improvement rate per learning cycle	**3.4**	**3.4**	**3.4**	**3.7**	**3.7**	**3.7**	**4.0**
Time to identify and fix new defect/fault source during ramp	**12.5**	**12.5**	**12.5**	**13.5**	**13.5**	**13.5**	**14.5**
# of learning cycles/year for 1 defect/fault source/month	**8.6**	**8.6**	**8.6**	**7.5**	**7.5**	**7.5**	**6.6**
Required yield improvement rate/learning cycle for 1 defect/fault source/month	**5.8**	**5.8**	**5.8**	**6.7**	**6.7**	**6.7**	**7.6**
Excursion Control							
Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*	*	*	*	*
Time to recognize electrical fault signature	*	*	*	*	*	*	*
Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*	*	*	*	*
Time to fix defect mechanism	*	*	*	*	*	*	*

** = to be updated in 2002*

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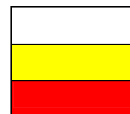

Table 94b Yield Learning Technology Requirements—Long-term

YEAR OF PRODUCTION	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*50*	*35*	*25*
MPU PRINTED GATE LENGTH (nm)	*25*	*18*	*13*
MPU PHYSICAL GATE LENGTH (nm)	*18*	*13*	*9*
Wafer size (mm)	**450**	**450**	**450**
Number of mask levels	**31**	**33**	**35**
Number of processing steps	**610**	**650**	**690**
Cycle time during ramp (# days)	**31**	**33**	**35**
Defect/Fault Sourcing Complexity [A], [G]			
Logic transistor density/cm^2 (1E6)	**210**	**519**	**1279**
Defect sourcing complexity factor (1E9) [B]	**128**	**337**	**883**
Defect sourcing complexity trend [C]	**18**	**48**	**126**
Data Analysis for Rapid Defect/Fault Sourcing			
Patterned wafer inspection sensitivity (nm) during yield ramp	**18**	**13**	**9**
Average # of inspections/wafer during full flow	**6.2**	**6.6**	**7**
(# data items/wafer) (1E13) [D]	**57.4**	**120.8**	**271.2**
Defect data volume (DV) trend [E]	**10**	**22**	**49**
Yield Learning During Ramp from 30% to 80% sort yield [F]			
# of yield learning cycles/year based on full flow cycle time	**11.8**	**11.1**	**10.4**
Required yield improvement rate per learning cycle	**4.2**	**4.5**	**4.8**
Time to identify and fix new defect/fault source during ramp	**15.5**	**16.5**	**17.5**
# of learning cycles/year for 1 defect/fault source/month	**5.8**	**5.1**	**4.4**
Required yield improvement rate/learning cycle for 1 defect/fault source/month	**8.7**	**9.9**	**11.3**
Excursion Control During Manufacturing			
Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*
Time to recognize electrical fault signature	*	*	*
Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*
Time to fix defect mechanism	*	*	*

** = to be updated in 2002*

Notes for Table 94a and b

[A] Defect/Fault sourcing means identifying the point of occurrence (identify process tool, design, test or process integration issue causing a visible or non-visual defect, parametric problem or electrical fault).

[B] Defect sourcing complexity factor = (logic transistor density #/ cm^2)×(# processing steps)

[C] Defect sourcing complexity trend is normalized to 130nm technology node.

[D] Defect data volume (DV) = (# of inspection/wafer in process flow)(wafer area)/patterned wafer sensitivity during ramp Assumes 20% of wafers are inspected on average at each mask step during ramp.

[E] DV trend is normalized to 130nm technology node.

[F] Assumes cycle time of one day per mask level. Also, assumes linear reduction in yield learning time based on time to identify and fix each defect/fault source.

[G] Rapid defect sourcing and yield learning assumptions as follows

- *Keep yield ramp constant (30% intro yield to 80% mature yield) for successive technology nodes.*
- *Keep time to source new yield detractors to 50% of process cycle time.*
- *New material introduction should not increase defect/fault sourcing time.*
- *Focus defect/fault sourcing on ramp portion of yield learning curve.*
- *Data collection, retention and retrieval will go up exponentially and significant improvement will be required in the IDM tools to enable the above assumptions.*

[H] T_{MP}, N, T_C, V, M and R, respectively represent time between measurement points, number of process steps, cycle time, process variability, number of possible defect mechanisms and resources.

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table 95.

Wafer environment control—There is definitive consensus that as device geometries approach 90 nm and beyond, wafer isolation will prove to be an enabling technology. The percentage of process steps affected by non-particulate or molecular contamination is expected to increase. The use of copper and other novel materials in the process introduces other potential contaminants. Because of these trends, wafer isolation technology, integrated tool mini-environments and closed carriers (e.g., Front Opening Unified Pods - FOUPs) are needed. FOUPs will also facilitate factory automation for wafer handling. The wafer environment contamination control (WECC) technology requirements indicate target levels of ambient acids, bases, condensables, dopants, and metals for specific process steps. Other exposure times and sticking coefficients may be scaled linearly.

Airborne Molecular Contamination—Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of Airborne Molecular Contamination (AMC). Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden. Acid vapors in the air have been linked with the release of boron from HEPA filters and the impact of amines on DUV photoresists are well known examples of AMC affecting wafer processing. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation in the cleanroom to measure AMC at the part per trillion level. SAW devices and APIMS have been used to measure low level AMC, but low cost, routine monitoring may be required as devices approach molecular dimensions. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front end processes. Although numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures, the need for nitrogen purging of wafer environment enclosures is being investigated for critical process steps. Not all process steps will be impacted by AMC. For example, future lithography systems will require vacuum processing and are not expected to impose new AMC control requirements in the cleanroom environment. The potential for AMC to impact new processes should be considered in all process integration studies.

Process critical materials—Little understanding exists today regarding impurity specifications in novel materials such as Cu plating solutions, CMP slurries, Chemical Vapor Deposition (CVD) precursors, and high/low κ materials and additional experimental investigation is required. Particle levels per volume have been held constant at critical particle size. Assuming an $1/x^3$ power law relationship, this means a cleanliness increase of approximately 2× per generation. Measurement of particles at the critical size is desirable, but monitoring of larger size particles is likely with critical particle size concentrations inferred from assumed particle size distributions.

Ultrapure Water—Ultrapure water (UPW) is generally considered to be >18.1 megΩ resistivity and below 1 PPB in ionics (cations, anions, metals), total organic carbon , silica (dissolved and colloidal), particles, and bacteria. Table 95 shows technology requirements as an extrapolation from the present. Lower criteria than present "state of the art" are not projected unless a process need is demonstrated according to each manufacturers requirements. Particle counters are capable of measuring only to 50nm for UPW. By assuming a particle size distribution, is should be possible to infer particle concentrations to particle sizes of 10 nm.

One important trend in UPW is the consideration of some parameters as process variables rather than contaminants, looking at stability more than absolute levels. Some semiconductor manufactures now treat dissolved oxygen (DO) in this way, while others still consider it a contaminant. Stability of temperature and pressure also are becoming more important.

Contaminant quality levels in UPW must be viewed in the context of where that quality is required and where it is to be measured. Points of measurement are referred to as the Point of Distribution (POD), Point of Connection (POC), and Point of Use (POU). The POD is just after the last treatment step and the POC and POU are at the back of the tool and in the tool, respectively. UPW quality, more than any other critical fluid, can change between these three locations and requires particular attention to maintain quality through-out. Further, as the focus shifts from the POD to the POU, the measurement methods can become more difficult and costly.

Due to the environmental impact of large demands on water sources and wastewater treatment, conservation activities are typically required. Technologies are needed to ensure water quality is maintained as more waters are recycled to the front end of the UPW system. Appropriate treatment technologies and analytical technique developments are needed. A well-implemented recycle program can actually improve final water quality by using a "cleaner" stream for the feed**.**

General test methodologies for monitoring contaminants in UPW are indicated in Figure 56. A more complete treatment of UPW concerns is covered in the *supplemental material of this chapter.*

Parameter	Measured (POD/POC)	Test Method
Resistivity	Online	Electric cell
Viable bacteria EPI Bacteria Scan RDI	Lab Lab Lab	Incubation Stained samples w/ Fluorescent Microscopy Laser-scanning Cytometry
TOC	Online	Resistivity / CO_2
Reactive Silica	Online or Lab	Colormetric
Colloidal Silica	Calculation	Total minus Reactive
Total Silica	Lab	ICP/MS
Particle Monitoring	Online	Light scatter
Particle Count	Lab	SEM – Capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP/MS
Dissolved O_2	Online	Electric Cell

Figure 56 General Test Methodology for Ultrapure Water

Liquid chemicals—For process chemicals, pre-diffusion cleaning requirements drive the most aggressive impurity levels. The purity levels of liquid chemicals are expected to remain unchanged from 2001 to the next technology node. The trend toward the use of more dilute chemistries helps to offset increased purity levels.

This evolution shows only a 10× improvement required over the next 15 years. Importantly, liquid particle counting technology is a very critical challenge below 90 nm. For HF last or SC-1 last cleans, use of novel chemistry (such as complexants, pH adjustments) may be required to meet the surface preparation requirements. With the increased use of CMP there must be a better understanding of purity requirements for slurries including the development of specifications for parameters such as agglomeration and ease of removal. Particle counters currently are capable of measuring only to 100nm for reactive liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to particle sizes of 20 nm.

Bulk/specialty gases—Although generic guidelines for impurities and chemicals are found in Table 95, specific needs may vary for each individual gas. No major changes are required for bulk ambient gases such as nitrogen, oxygen, argon, and hydrogen. Impurity reduction improvements have been pushed out to later nodes in some cases. However, inline non-intrusive particle measurements at the critical size in these and specialty gases will be a significant challenge. Although current technology can be extended to meet the measurement requirements at point of use (POU) continuous particle monitoring in each specialty gas line would add substantial costs to factory infrastructure. For specialty gases the sensitivity to contamination may vary significantly by process. For example, a given contamination level in certain deposition gases may have far more impact than the same level of contaminants in certain etchant gases. POU filters, and in some cases purifiers and generators, can be utilized to meet the most stringent requirements. Cost-effective rapid

response detection of molecular impurities is required. Purity requirements for gases related to low κ and Cu processes are too speculative to include at this time.

Novel materials—Impurity specifications for novel materials used in processing will be increasingly important. Specifications for critical materials such as novel metal oxides, CMP slurries, low/high dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied. Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements.

Design-to-process interactions—The need for standard test structures is critical in determining defect sources and mechanisms. Once the design process interactions are understood, device design ground rules may be established and communicated that decrease process sensitivity. Cycles of process sensitivity analysis and reduction will be critical to advancing device design and yield. Additionally, sensitivities of designs to various levels of random defects need to be considered in the design process.

Process-to-process interactions—Interactions that result in defect formation (such as thickness of photoresist and contact density can affect the level of residue inside a via/contact) between process steps may drive particular requirements to a tool or process upstream or downstream that are not necessarily germane to that tool or process. Cluster tools and wet sinks are two examples of tools that must be carefully designed to ensure that their modules do not transfer any contaminants that degrade the performance of adjacent modules. To detect, to understand, and to eliminate unwanted process interactions, process monitoring and control will play a key role. The appropriate sensors and data must be available, along with an appropriate information management system to correlate process parameters to upstream/downstream parameters and yield and provide smart, inter-tool and intratool statistical process control (SPC).

Table 95a Technology Requirements for Wafer Environmental Contamination Control—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Wafer Environment Control							
Critical particle size (nm) [A]	65	58	52	45	38	35	33
# Particles > critical size (/m^3) [B]	5	4	3	2	2	1	1
Airborne Molecular Contaminants (ppt)) [C]							
Lithography—bases (as amine, amide, or NH_3)	750	750	750	750	750	<750	<750
Gate—metals (as Cu, E=2 × $^{10-5}$) [C]	0.2	0.2	0.15	0.1	0.1	0.07	<0.07
Gate—organics (as molecular weight greater than or equal to 250, E=1 × $^{10-3}$) [D]	100	90	80	70	60	60	50
Organics (as CH_4)	1800	1620	1440	1260	1100	900	<900
Salicidation contact—acids (as Cl-, E=1 × $^{10-5}$)	10	10	10	10	10	<10	<10
Salicidation contact—bases (as NH_3, E=1 ×$^{10-6}$)	20	16	12	10	8	4	<4
Dopants (P or B) [E]	<10	<10	<10	<10	<10	<10	<10
Process Critical Materials							
Critical particle size (nm) [A]	65	58	52	45	38	35	33
Ultrapure Water							
Total oxidizable carbon (ppb)	1	1	<1	<1	<1	<1	<1
Bacteria (CFU/liter)	<1	<1	<1	<1	<1	<1	<1
Total silica (ppb)	0.1	0.1	0.1	0.1	0.05	0.05	0.05
# Particles>critical size (/ml)	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
Critical cation, anion, metals (ppt, each)	<20	<20	<20	10	10	10	10
Liquid Chemicals [F]							
Particles—critical size (ml)	<10	<10	<10	<10	<1	<1	<1
HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	<150	<135	<110	<100	<90	<50	<50
Critical cation, anion, metals (ppt, each)	<10	<10	<10	<5	<5	<5	<1
HF-only, TOC (ppb)	<30	<30	<25	<20	<15	<10	<10
HCl, H_2SO_4: All impurities (ppt)	<1000	<1000	<1000	<1000	<1000	<1000	<1000
BEOL Solvents, Strippers K, Li, Na, (ppt, each)	<1000	<1000	<1000	<1000	<1000	<1000	<1000
ILD CVD Precursors (e.g., TEOS)							
Metals (ppb)	<1	<1	<1	<0.1	<0.1	<0.1	<0.1
H_2O (ppmV)	<10	<10	<10	<5	<5	<5	<1
Bulk Gases							
N_2, O_2, Ar, H_2: H_2O, O_2, CO_2, CH_4 (ppt, each)	<1000	<1000	<1000	<1000	<1000	<100	<100
# Particles > critical size (/liter)	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
Specialty Gases							
# POU particles > critical size (/liter) [F]	2	2	2	2	2	2	2
Inerts—Oxide/Photoresist Etchants/Strippers							
O_2 (ppbV)	<1000	<1000	<1000	<500	<500	<500	<100
H_2O (ppbV)	<1000	<1000	<1000	<500	<500	<500	<100
Individual specified metals (ppbWT)	<10	<10	<10	<10	<10	<1	<1

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow–Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

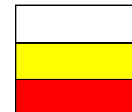

Table 95b Technology Requirements for Wafer Environmental Contamination Control—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
MPU Printed Gate Length (nm)	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*18*	*13*	*9*
Wafer Environment Control			
Critical particle size (nm) [A]	**23**	**16**	**11**
# Particles > critical size (/m^3) [B]	**1**	**<1**	**<1**
Airborne Molecular Contaminants (ppt) [C]			
Lithography—bases (as amine, amide, or NH_3)	**<750**	**<750**	**<750**
Gate—metals (as Cu, $E=2\times10^{-5}$) [C]	**<0.07**	**<0.07**	**<0.07**
Gate—organics (as molecular weight greater than or equal to 250, $E=1\times10^{-3}$) [D]	**40**	**30**	**20**
Organics (as CH_4)	**<900**	**<900**	**<900**
Salicidation contact—acids (as Cl-, $E=1\times10^{-5}$)	**<10**	**<10**	**<10**
Salicidation contact—bases (as NH_3, $E=1\times10^{-6}$)	**<4**	**<4**	**<4**
Dopants (P or B) [E]	**<10**	**<10**	**<10**
Process Critical Materials			
Critical particle size (nm) [A]	**23**	**16**	**11**
Ultrapure Water			
Total oxidizable carbon (ppb)	**<1**	**<1**	**<1**
Bacteria (CFU/liter)	**<1**	**<1**	**<1**
Total silica (ppb)	**0.01**	**<0.01**	**<0.01**
Particles—critical size (ml)	**<0.2**	**<0.2**	**<0.2**
Critical cation, anion, metals (ppt, each)	**<10**	**<10**	**<10**
Liquid Chemicals [F]			
# Particles > critical size (/ml)	**<1**	**<1**	**<1**
HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	**<50**	**<40**	**<40**
Critical cation, anion, metals (ppt, each)	**<1**	**<1**	**<1**
HF-only, TOC (ppb)	**<8**	**<6**	**<4**
HCl, H_2SO_4: All impurities (ppt)	**<1000**	**<1000**	**<1000**
BEOL Solvents, Strippers K, Li, Na, (ppt, each)	**<1000**	**<1000**	**<1000**
ILD CVD Precursors (e.g., TEOS)			
Metals (ppb)	**<0.1**	**<0.1**	**<0.1**
H_2O (ppmV)	**<1**	**<1**	**<1**
Bulk Gases			
N_2, O_2, Ar, H_2: H_2O, O_2, CO_2, CH_4 (ppt, each)	**<100**	**<100**	**<100**
# Particles > critical size (/liter)	**<0.1**	**<0.1**	**<0.1**
Specialty Gases			
# POU particles > critical size (/liter) [F]	**2**	**2**	**2**
Inerts—Oxide/Photoresist Etchants/Strippers			
O_2 (ppbV)	**<100**	**<50**	**<50**
H_2O (ppbV)	**<100**	**<50**	**<50**
Individual specified metals(ppbWT)	**<1**	**<1**	**<1**

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow–Manufacturable Solutions are Known

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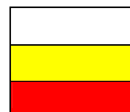


Notes for Table 95a and b

[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles. For UPW water and liquid chemicals (see text), particle measurements at critical particle size is not possible with existing metrology, but is inferred from assumed particle size distributions and measurements of particles at sizes greater than critical particle dimension.

[B] Airborne particle requirements are based on an assumed value for deposition velocity of 0.01 cm/second, resulting in 1 particle/m^2/hr. for a ambient concentration of 3 particles/m^3. (This value represents an approximate value at atmospheric conditions.

[C] Ion indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography is defined by lithography roadmap. Gate metals and organics scale as surface preparation roadmap metallics and organics. All airborne molecular contaminants calculated as S=E(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1, N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second)*

[D] The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general molecular weights < 250 not considered detrimental due to the higher volatility of these compounds.

[E] Includes P, B, As, Sb

[F] Particle targets apply at POU, not incoming chemical. Point-of-tool connection chemical metallic targets are based on Epi starting material, sub-ppb contribution from bulk distribution system, 1:1:5 standard clean 1 (SC-1) and elevated temperature 1:1:5 standard clean 2 (SC-2) final clean step. "HF last" or "APM last" cleans would require ~10× and ~100× improved purity HF (mostly Cu) and APM chemicals, respectively.

[G] Critical metals and ions include: Ca, Co, Cu, Cr, Fe, Mo, Mn, Na, Ni, W

[H] TOC values are based on best available technology and are not necessarily supported by yield data.

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

The defect budget validation effort initiated by International SEMATECH for the 1997 and 1999 editions of the ITRS has continued for the 2001 revision. To ensure on-going relevance of defect target roadmaps, modeling validation must be completed periodically. Research into better yield modeling techniques is required to address future modeling challenges. Modeling of systematic defect limited yield (SDLY) limiters is increasingly becoming a significant focus of yield learning experts. . This is being driven by the fact that SDLY issues tend to dominate in the early yield ramp stages, and these yield ramp rates continue to accelerate. In addition, parametric limited yield issues and design to process mismatch tend to limited yield in the early ramp timeframe. The increasing dominance of non-visual defects will further complicate yield modeling and defect budgeting. Thus, defect models will need to better consider electrical characterization information, and reduce emphasis on visual analysis. This will require research into new characterization devices and methods. Interconnect process layers are a particular challenge and have been so identified in the technology requirements. Some issues include modeling the yield impacts of ultra-thin film integrity, increased process complexity, interconnect speed and transmission characteristics, and the impact of wavelength dependent defects on reticles that may or may not result in defects. This research is complicated by the lack of state-of-the-art semiconductor processing capabilities in universities and other research sources. Figure 57 illustrates the potential solutions.

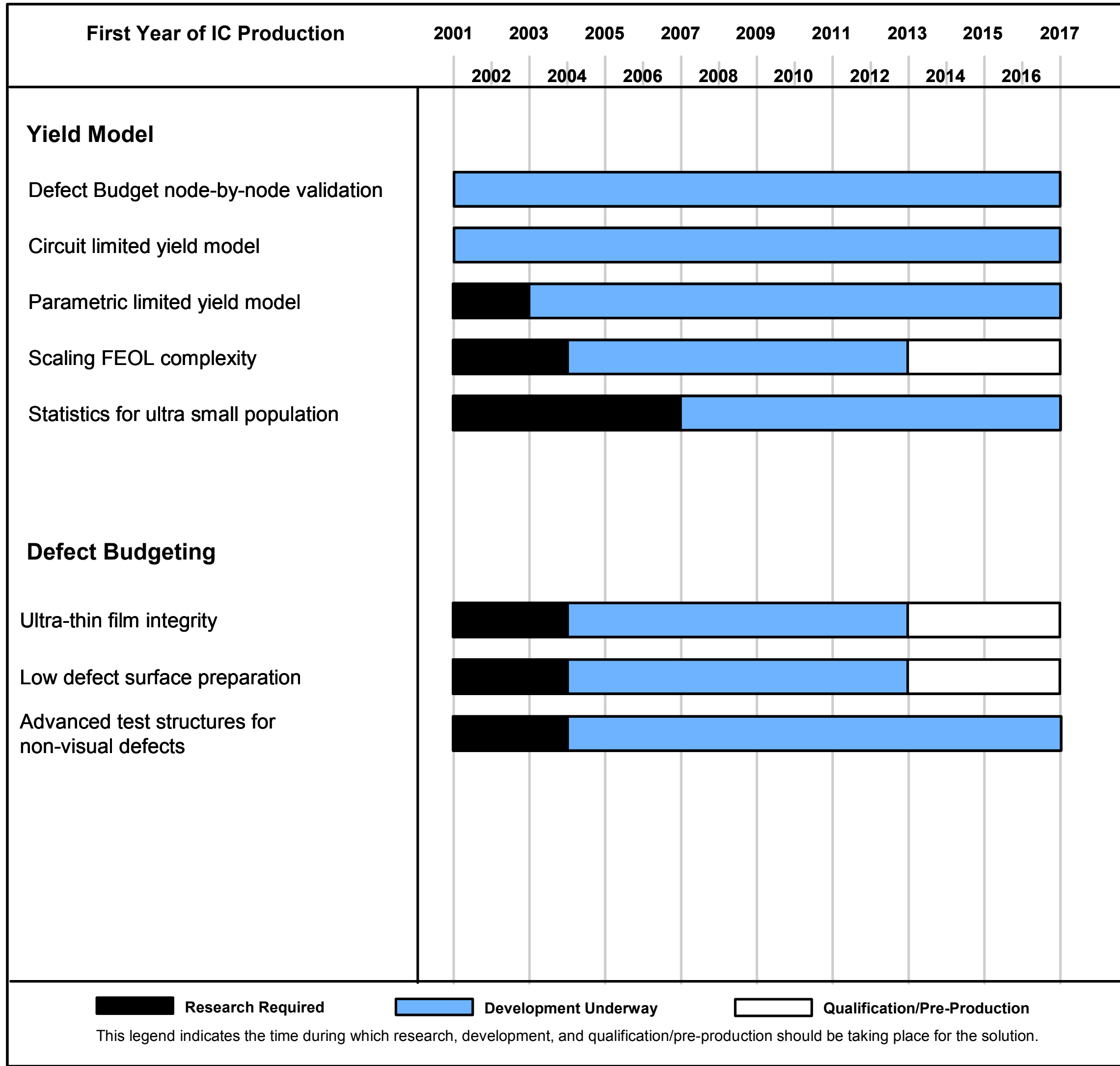


Figure 57 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION AND CHARACTERIZATION

Considerable research and development is now necessary to meet the technology requirements for advanced defect detection tools. Detection in high aspect ratio (HAR) structures created Post-Etch (Figure 58) is currently deficient. Light-scattering and optical-imaging solutions for production will consequently become limited by 2005. The quest for an effective solution to the detection of very thin residue at the bottom of a isolated HAR structures demands faster development of novel methods such as holographic imaging, e-beam (scattering or imaging), acoustic imaging techniques, and X-ray imaging.

There is a lack of suitable component technologies for developing novel detection systems. Significant advancement associated with shorter wavelengths, continuous-wave lasers, detectors with higher quantum efficiency and higher acquisition speed, suitable low-loss and low-aberration lenses, waveplates and polarizers, and robust mechanical and acousto-optic scanners are needed now to continue the economical development of optical techniques.

Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. Arrayed detection schemes for parallel data acquisition from a larger area of the wafer need to be explored. Enhancement of signal-to-noise ratio using software algorithms could possibly extend optical approaches.

Potential solutions must comprehend the need for greater amounts of defect-related data e.g. composition, shape, defect classification, and rapid decision-making. (Refer to the following section on Yield Enhancement for a comprehensive explanation of the needs in this area.) Automated defect classification, spatial signature analysis, adaptive sampling, yield-impact assessment, and other algorithmic techniques are already reducing time to decisions and product at risk. Defect detection and characterization equipment must produce more information for these techniques to analyze. The challenge of improved sensitivity to smaller defect sizes has moved characterization platforms in-line to provide higher resolution. The tradeoff between associated throughput and the provided information is crucial. Thereby, defect detection is evolving closer to the defect source. Development to integrate defect detection into process equipment must progress at faster pace to implement automated process control.

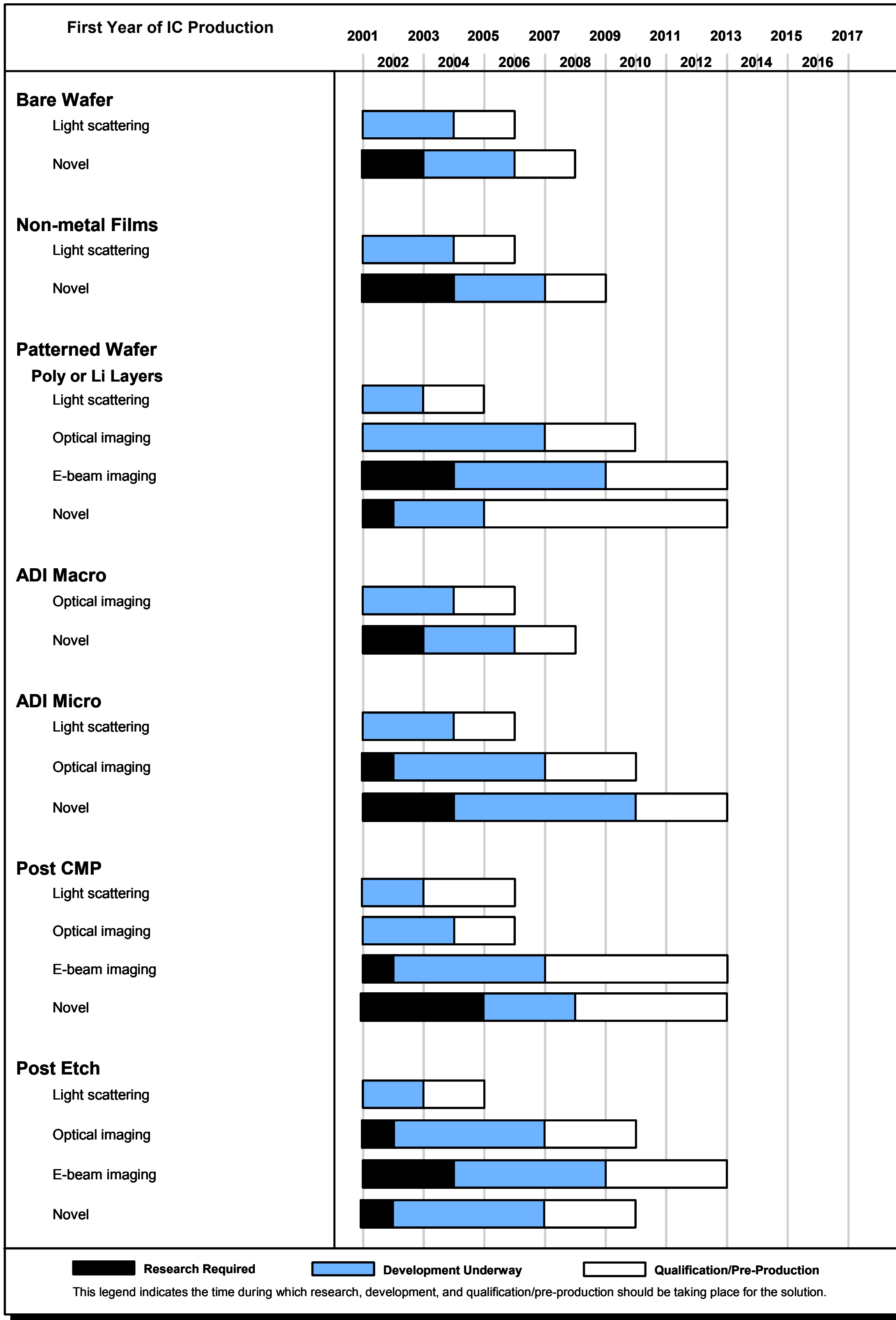


Figure 58 Defect Detection and Characterization Potential Solutions

YIELD LEARNING

As indicated by the yellow and red areas of the yield learning technology requirements table, the two areas that require highest attention are data management and rapid defect/fault sourcing. A collaborative effort between the stakeholders from device makers, metrology & information technology suppliers and academia is required to formulate and execute a strategic plan to manage all data relevant to rapid yield learning. Without such collaboration, much redundancy will continue to exist in data management and analysis. Additional potential solutions are provided in the Data Management System section below.

As noted above, yield learning can proceed at an acceptable rate of <5% yield improvement per month in the absence of defect/fault sources. However, given the technology transfer history of our industry, numerous defect/fault sources may be anticipated after the process technology is handed off to manufacturing by the process R&D group. There are two ways to achieve the required ramp of 30% to 80% yield in a year: 1. Reduce the total number of new defect/fault sources or mechanisms. 2. Reduce the time to source and fix each new defect/fault source or mechanism. Whereas the first approach is mostly company dependent, the second approach requires numerous tools and techniques for rapid defect/fault sourcing as shown below.

Moreover, with the continued increase in complexity of the design and fabrication process, the ability to detect and react to yield impacting trends and excursions in a timely fashion will require a larger dependence on passive data. This will be acutely true during yield ramp where maximum productivity and profit benefits will be achieved. Passive data is defined as defect, parametric, and electrical test data collected inline from the product through appropriate sampling strategies. The additional time required to perform experiments, such as short-loop testing, will not be readily available at future nodes. The time necessary to trend potential problems and/or identify process excursions will require the development of sampling techniques that maximize the signal-to-noise ratio inherent in the measured data. The goal of Integrated Data Management (IDM) is to identify process issues in as few samples as possible. Analysis techniques that place product data in the context of the manufacturing process provide a stronger "signal" and are less likely to be impacted by measurement noise since they comprehend various levels of process history and human experience (lessons learned). Therefore, potential solutions for rapid yield learning include the development of technologies that generate information from product data and tool-health or other *in situ* process measurements. Automation methods are also required that correlate product information with fabrication processes, sometimes referred to as data mining. Fundamental to the successful integration of new methods and technologies is a requirement for standards that facilitate data communications in the virtual and/or physically merged database environment.

VISIBLE DEFECTS

Although tools for sourcing visible defects are fairly well established (optical and SEM detection and review, SSA, ADC, EDX, FIB), new tools and methodologies will have to be developed to achieve adequate signal to noise ratio for differentiating real defects from background nuisance defects and to characterize the elemental composition of continuously shrinking visible defects.

NON-VISUAL DEFECTS

Affordable inspection techniques are needed that go beyond optical microscopy and offer high resolution without sacrificing throughput. To source non-visual defects, the resolution of analytical tools for failure analysis needs to be improved. Technology nodes below 90 nm will require the development of affordable failure analysis techniques that can extend the range of detectable defects down to the atomic level. In addition, the resolution of internal node DC micro probing for characterizing individual circuit/transistor parameters or isolating leakage paths needs to be improved. Design to process interactions that can lead to localized non-visual structural defects have to be researched and modeled. Design for Testability/Diagnose-ability techniques need to utilize these models to enhance the localization of a defect source.

PARAMETRIC DEFECTS

Saving more parametric data as measured on circuit testers will aid in sourcing parametric source defects. This information will allow for correlation to process data, through a variety of techniques, including spatial signature analysis. Modeling the probabilities of factors that can lead to "parametric defects" can also reduce the time it takes to source the cause. Built-In Self Test (BIST) techniques must be developed to identify race conditions and other failure modes that are a function of parametric variation or mismatch.

ELECTRICAL FAULTS

Presently, memory array test chips and memory arrays within microprocessors are used to quickly isolate faults. This technique is likely to be extended to non-arrayed devices. Future products must be designed so that the test process can isolate failures. Design for test (DFT) and BIST are two methods that can aid in defect isolation. Both DFT and BIST failure pattern must map to a physical location on a circuit. Accurate fault to defect mapping models must also be developed to further assist in the defect localization process. Other test programs are needed to save failure pattern information so that it can be analyzed based on pre-determined (modeled) failure mode probabilities. All of these techniques will allow yield engineers to more quickly and precisely determine the locations and causes of circuit failures.

DATA MANAGEMENT SYSTEMS (DMS)

The following key areas of R&D investment have been identified by Oak Ridge National Lab (ORNL), as part of a SEMATECH-sponsored DMS assessment study, as necessary elements for meeting tomorrow's DMS challenges:

- Standards for data/file formats and coordinate systems
- DMS/WIP integration
- DMS methodologies for data collection, storage, archiving and purging
- DMS for advanced tool/process control

Additional findings from this study are available in the *supplemental material* of this roadmap.

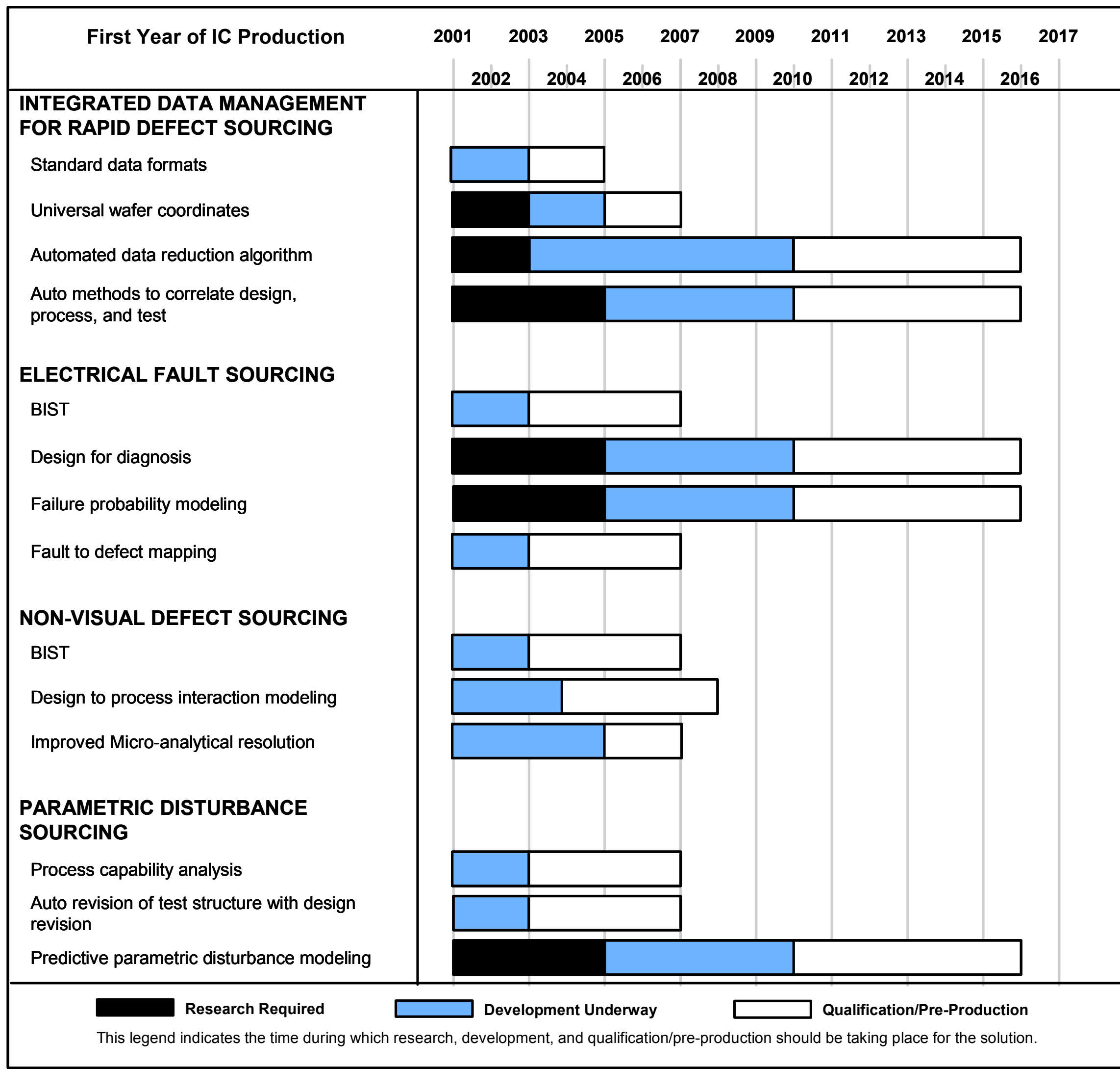
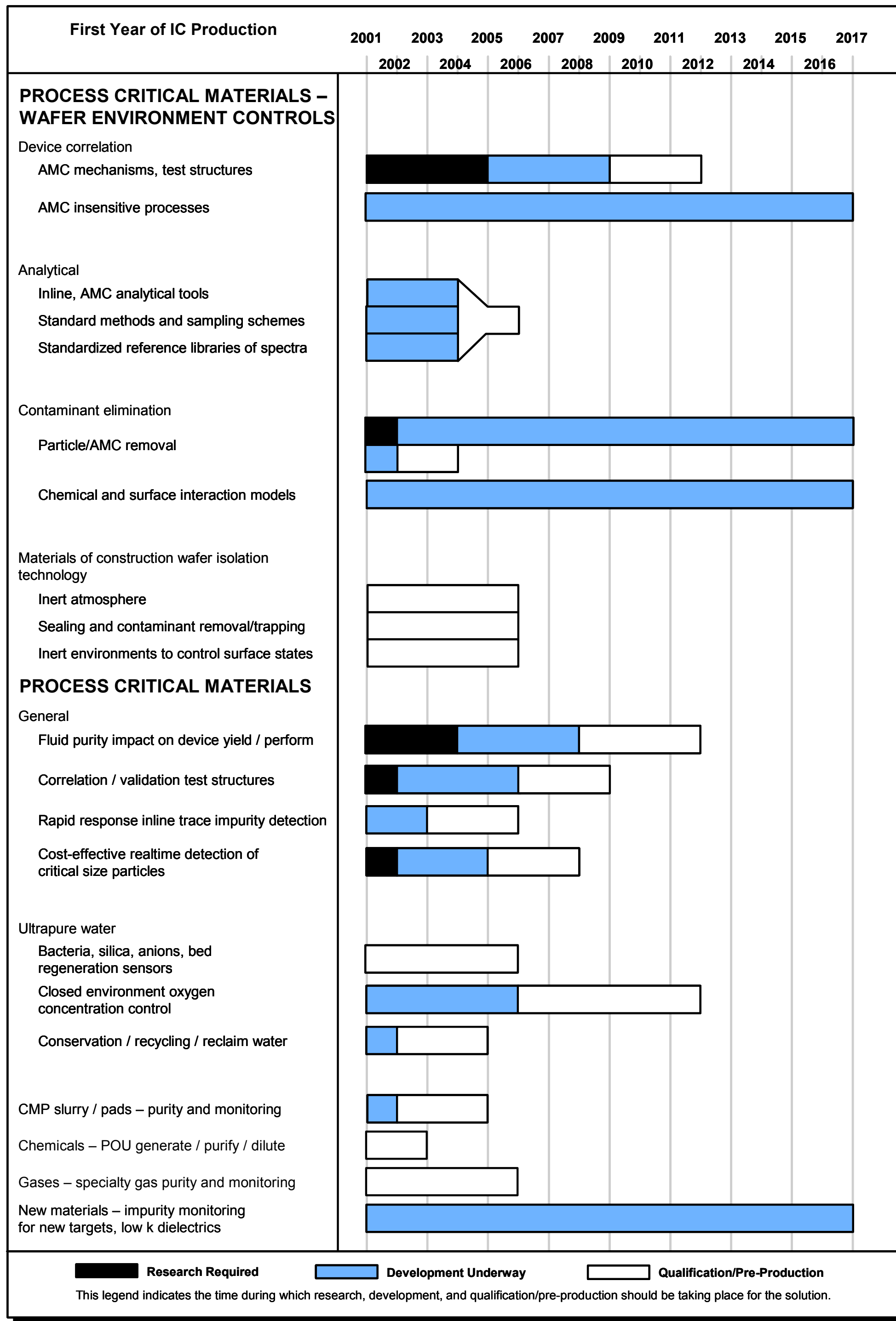


Figure 59 Yield Learning Potential Solutions

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and actually enable cost-effective high volume manufacturing for 130–100 nm devices. Refer to Figure 60. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other nonvisual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for

post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.



AMC—Airborne Molecular Contamination

Figure 60 Wafer Environmental and Contamination Control Potential Solutions

Process critical materials—Figure 60 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities. UPW quality focus needs to move towards the

point of use. Water quality is generally measured at the point of production and not at the POU or at the wafer. An understanding of the impact of the tool upon water quality, specifically particles, silica , and dissolved oxygen, needs to be understood to ensure quality is carried to the wafer. Inline trace impurity analytical technology for process critical materials is needed to better understand purity levels at the POU. Ultrapure water particle levels are easily achieved with existing design and filtration practice and verified with available offline particle metrology. Improved online monitoring is required to detect excursions realtime for particle sizes below 0.1 µm. Improved analytical technology is needed to characterize ultra-trace levels of silica . Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water. Demonstration of the effectiveness and efficiency of particle filters in specialty gases is needed to increase the confidence that the filters are performing adequately without continuous monitoring. The requirements to measure particles at POU for specialty gases below 90 has been met by the development of an inline condensation nucleus counter (CNC) compatible with oxidizers, corrosives, and flammable and toxic gases. Specifications and standard test methods will need to be established for new materials.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Availability of affordable, accurate, repeatable, real time sensors for nonparticulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum loadlock tools, thereby decreasing contamination and loadlock pumpdown times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink endstations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and nonabsorbing materials development are key to effective wafer isolation deployment.