INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

EXECUTIVE SUMMARY

ACKNOWLEDGMENTS

INTERNATIONAL ROADMAP COMMITTEE

◈*Europe*—Wolfgang Arden, Patrick Cogez, Mart Graef, Gerhard Goltz
◈*Japan*—Hidemi Ishiuchi, Toshihiko Osada
◈*Korea*— Joo-Tae Moon, Hyun-Chul Sohn
◈*Taiwan*—Mong-Song Liang, Chen-Hsi Lin, C.Y. Lu
◈*U.S.A.*—Pushkar Apte, Bob Doering, Paolo Gargini

TECHNOLOGY WORKING GROUP KEY CONTRIBUTORS

Chip-Size/Technology Node Study Group—Alan Allan, Chris Case, Chi-Shih Chang, Walter Class, Bob Doering, Donald Edenfeld, Denis Fandel, David Jensen, Andrew Kahng, Fred Lakani, Harry Levinson, Chris Long, Jeff Pettinato, Shizuo Sawada, Luan C. Tran, Peter Zeitzoff

System Drivers and Design—Satoshi Akui, Ken Albin, Martin Anderson, Kanji Aoki, Larry Arledge, Yoshimi Asada, Kenji Asai, Woo-Hyun Baek, Bob Bentley, Kerry Bernstein, Valeria Bertacco, David Blaauw, Shawn Blanton, Ralf Brederlow, Mike Briere, Ben Brown, Ken Butler, Juan-Antonio Carballo, Mi-Chang Chang, C. Chen, Liang-Gee Chen, Young-Jung Choi, John Cohn, Don Cottrell, John Darringer, Hugo de Man, Stephane Donnay, Wolfgang Ecker, Dale Edwards, Yoshiharu Furui, Shinji Furuno, Jim Garrison, Sudhir Gowda, Carlo Guardiani, Hosam Haggag, Tamotsu Hiwatashi, Kelly A. Hopmeier, Mark Hsieh, Koichiro Ishibashi, Shih-Jie Jou, William Joyner, Andrew Kahng, Masaru Kakimoto, Haruhisa Kashiwagi, Stan Kaveckis, Jamil Kawa, Chang Kim, Chang-Hyun Kim, Jae-Suk Kim, Chi-Hau Kong, Victor Kravets, Dennis Lau, Seok-Joong Lee, C.C. Lee, Tsung-Hsien Lin, Gin-Kou Ma, Vinod Malhotra, Martin Margala, Grant Martin, Kazuya Masu, Masami Matsuzaki, Sury Maturi, Don McMillan, Anne Meixner, Y.N. Mo, Sharon Murray, Sani Nassif, Tomoji Nukiyama, Isao Okada, Nobuhiro Okano, Nobuto Ono, Sule Ozev, David Pan, Vijay Pitchumany, Carl Pixley, Daniel Purdy, John Rawlins, Bill Read, Kevin Redmond, John Rockway, Michael Rodgers, Wolfgang Rosenstiel, Toshitada Saito, Karem Sakallah, Joseph Sauerer, Jean-Pierre Schoellkopf, Peter Schwarz, Yahiro Shiotsuki, Gary Smith, Mani Soma, Leon Stok, Mikio Sumitani, Robert Taft, Tah-Kang Ting, Ryoichi Tomishige, Hiroki Tomoshige, Tadao Toyoda, Kunio Uchiyama, Maarten Vertregt, Piet Wambaq, Lawrence K Whitcomb, Jim Wieser, Bruce Wile, Alfred Wong, Ching-San Wu, Akihiro Yamada, Ichiro Yamamoto, David Yeh

Test and Test Equipment—Joong-Bae Ahn, Katsuhiko Aiyoshi, Joel Amtsfield, Frank Anderson, Ken-ichi Anzou, Davide Appello, Dave Armstrong, Bassam Asfoor, Roger Barth, Vishwas Bhide, Mike Bienek, Dan Brija, Carl Buck, Scott Buckner, Yi Cai, Jwu E Chen, Paul Chen, Wei-ming Chi, Jeong-Ho Cho, Pat Cochran, Jack Courtney, Gordon Cowan, Guiseppe Paolo Crisenza, Dennis Eaton, Don Edenfeld, Mike Egloff, Kouichi Eguchi, Stefan Eichenberger, Michiaki Emori, Satoshi Fukumoto, Rudy Garcia, Anne Gattiker, Larry Gilg, Hosham Haggag, Mike Harris, Kazumi Hatayama, Ken Heiman, Klaus Dieter Hilliges, Masaki Hirano, Shigeyoshi Hirose, Hisao Horibe, Bernd Juling, Takayuki Katayama, Kyu-Cheul Kim, Takuya Kobayashi, Tomoaki Kobayashi, Jens Kober, John Lakoski, Matt Lauderdale, Chumg Len Lee, Kuen-Jong Lee, Kwan-Jong Lee, Mike Li, C. S. Lin, Charles Lin, Michio Maekawa, Peter Maxwell, Mike Mayberry, Dan Meyer, Shinji Mori, Peter Muhmenthaler, Luis Muller, Oliver Nagler, Yasushi Nakajima, Udaya Natarajan, Pierpaolo Nicosia, Phil Nigh, Yasumasa Nishimura, Kazuya Noguchi, Akira Ooishi, Bill Ortner, Hideharu Ozaki, David Pfaff, Bill Price, Rochit Rajsuman, James Rhodes, Paul Roddy, Mike Rodgers, Charles Rothschild, Masayuki Sato, Yasuo Sato, Ulrich Schoettmer, Fayez Sedarous, Rene Segers, Meng Lieh Sheu, Lee Song, Chauchin Su, Hiroyoshi Suzuki, Tetsuo Tada, I Shih Tseng, J. S Tseng, Masanori Ushikubo, Jody Van Horn, Don Van Overloop, Robert van Rijsinge, Erik Volkerink, Larry Wagner, Hitoshi Watanabe, Burnie West, Tom Williams, Cheng Wen Wu, Wen Ching Wu, Osamu Yamada, Mitsuo Yamazaki, Daniel Yang, Wen Kun Yang, Raymond Yin, Yervant Zorian

Process Integration, Devices, and Structures—Yasushi Akasaka, Joe E. Brewer, C.P. Chao, Travis Chao, Osbert Cheng, S. C. Chien, James Chung, Simon Deleonibus, Theodore A. (Ted) Dellin, Carlos Diaz, Samuel K.H. Fung, J.C. Guo, Toshiro Hiramoto, Digh Hisamoto, Atsushi Hori, Ken Hsieh, W.Y. Hsieh, Margaret Huang, Jim Hutchby, Sung-Bo Hwang, Jiro Ida, Kiyotaka Imai, Young-Phil Kim, Tzu-Jae King, Dae-Hong Ko, Sang-Don Lee, Chia Wen Liang, Glen Lin, Y.T. Lin, Rich Liu, S.L. Lung, Mike Ma, Y.J. Mii, Naoki Nagashima, Takashi Nakamura, Tak H. Ning, Hidekazu Oda, Dong-Keun Park, Mark Rodder, Shizuo Sawada, Klaus Schruefer, Yee-Chaung See, Tae-Wook Seo, Kentaro Shibahara, Hun-Jong Shin, Riichiro Shirota, Thomas Skotnicki, Toshihiro Sugii, Yoshitaka Tadaki, Shuichi Tahara, Shinichi Takagi, Denny Tang, Luan C. Tran, Cheng taung Tsai, MJ Tsai,

Ting S. Wang, Jason Woo, Chien Wu, Chung-Cheng Wu, Michael Wu, Qi Xiang, Geoffrey Yeap, Makoto Yoshimi, Peter Zeitzoff, Bin Zhao

Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications—Hideo Aoyagi, Herbert S. Bennett, Ralf Brederlow, Doug Coolbaugh, Julio Costa, Peter E. Cottrell, Stefaan Decoutere, Jim Dunn, Mark Fedasiuk, Ronald Grundbacher, Dave Halchin, Yoshihiro Hayashi, Erwin Hijzen, Digh Hisamoto, W. Margaret Huang, Anthony A. Immorlica, Jay John, Alvin Joseph, Takahiro Kamei, Tom Kazior, Yukihiro Kiyota, Dim-Lee Kwong, Minh Le, Victor Liang, David McQuiddy, Jan-Erik Mueller, Marco Racanelli, Bernard Sautreuil, Hisashi (Sam) Shichijo, H.C. Tseng, Chuck Weitzel, Ching-San Wu, Peter Zampardi, Bin Zhao, Herbert Zirath, John Zolper

Emerging Research Devices and Materials—Dimitri Antoniadis, Marc Baldo, Karl Berggren, Charles Black, Dawn Bonnell, George Bourianoff, Alex Bratkovski, Joe Brewer, John Carruthers, Sang Wook Cheong, Philippe Coronel, Supriyo Datta, Kristen De Meyer, Erik DeBenedictis, Simon Deleonibus, Alex Demkov, Steve Erwin, Michael Forshaw, Christian Gamrat, Michael Garner, Bruno Ghyselen, Jeff Grossman, Dan Hammerstrom, Daniel J.C. Herr, Toshiro Hiramoto, Susan Holl, James Hutchby, Berry Jonker, Ted Kamins, Richard Kiehl, Tsu-Jae King, Gerhard Klimeck, Zoran Krivokapic, Phil Kuekes, Louis Lome, Mark Lundstrom, Kathryn Moler, David Muller, Rama Muralidhar, Wei-Xin Ni, Tak Ning, Tobias Noll, Yuri Ponomarev, Muralidhar Ramachandran, Ramamoorthy Ramesh, Mark Reed, L. Rafael Reif, Lothar Risch, David A. Roberts, Vwani Roychowdhury, John Henry Scott, Sadasivan Shankar, Wei-Tsun Shiau, Kentaro Shibahara, Thomas Skotnicki, Morley Stone, Shinichi Takagi, Tom Theis, Jim Tour, Luan Tran, Rudolf M. Tromp, Ming-Jinn Tsai, Peter Varman, Eric Vogel, Kang Wang, Rainer Waser, Stan Williams, H.-S. Philip Wong, In Kyeong Yoo, Makoto Yoshimi, Peter Zeitzoff, Yuegang Zhang, Victor Zhirnov, Igor Zutic

Front End Processes—Khaled Ahmed, Mauro Alessandri, Michael Alles, Olli Anttila, Luis Aparicio, Leo Archer, Souvik Banerjee, Joel Barnett, Tom Bastein, Twan Bearda, Larry Beckwith, Ivan (Skip) Berry, Roberto Bez, Frederic Boeuf, Bill Bowers, George Brown, Murray Bullis, Mayank T. Bulsara, Ahmed Busnaina, Jeff Butterbaugh, George K. Celler, Cetin Cetinkaya, Juanita Chambers, David Chang, Kow-Ming Chang, Mark Chang, Tien-Sheng Chao, S. C. Chen, Victor Chia, Albert Chin, Luigi Columbo, Michael Current, Tim Dalton, Carlos H. Diaz, Anthony (Tony) Dip, Bruce Doris, Roxanne Dulas, Laszlo Fabry, Jeff Farber, Sue Felch, Graham Fisher, Hideaki Fujiwara, Nobuo Fujiwara, Michael Fury, Glenn W. Gale, Ernst Gaulhofer, Hans Gossmann, Dinesh C. Gupta, Martin Gutsche, Greg Higashi, Dick Hockett, Andrew Hoff, Harry Hovel, Daniel Huang, J. M. Huang, Ru Huang, Tiao-Yuan Huang, Howard Huff, Bill Hughes, Makarem Hussein, Huang-Tsung Hwang, Yoshikazu Ibara, Simon Jang, Bob Johnston, Mototaka Kamoshida, Ho-Kyu Kang, Sien Kang, Seiichiro Kawamura, Bruce Kellerman, Yung Kim, Brian Kirkpatrick, Hiroshi Kitajima, Martin Knotter, Mitsuo Kohno, Daniel Koos, Alex Ku, Michitaka Kubota, Paul Langer, Larry Larson, Jeff Lauerhaas, Jeong-Gun Lee, Kun-Tack Lee, Lurng-Sheng Lee, Tan-Fu Lei, Meikei Leong, Didier Levy, Kuan Liao, Tom Lii, Hong Lin, Wen Lin, Jerry Liu, Shih-hsin Lo, Shrikant Lohokare, Don McCormack, Tom McKenna, Doug Meyer, Fred Meyer, Michihiko Mifuji, Ichiro Mizushima, Stephane Monfray, Jim Moreland, Nairn Moumen, Wolfgang Mueller, Anthony Muscat, Dave Myers, Toufic Najia, Toshiro Nakanishi, Sadao Nakashima, Yasuo Nara, Masaaki Niwa, Faran Nouri, Helmut Oefner, Atsushi Ogura, Toshihide Ohgata, Carl Osburn, Jin-Goo Park, Shiesen Peng, Darryl Peters, Gerd Pfeiffer, Francesco Pipia, Noel Poduje, Jagdish Prasad, Krishnaswamy Ramkumar, K. V. Ravi, Rick Reidy, Karen Reinhardt, Jae-Sung Roh, Ed Rutter, Pete Sandow, Tom Seidel, Hwa-il Seo, Giorgio Servalli, Jim Shen, Hyun-Soo Shin, Stephen Silverman, Greg Smith, Jong-Won Sohn, Chris Sparks, Bob Standley, Jack Thomas, Carl Treadwell, Hong-Hsiang Tsai, Bing-Yue Tsui, Hidetsugu Uchida, Jason Underwood, Steven Verhaverbeke, Peter Wagner, Mike Walden, Masaharu Watanabe, Neil Weaver, Susanne Weizbauer, Jeff Wetzel, Ted White, Rick Wise, S. G. Wuu

Lithography—Jin-Ho Ahn, Hiroshi Arimoto, Emanuele Baracchi, R. K. Chen, T. Y. Chen, John Cheng, HanKu Cho, Han-Ku Cho, Jae-Sung Choi, Jin-Young Choi, Ron Chu, Kevin Cummings, Giang Dao, Akihiro Endo, Ted Fedynyshyn, Gene Fuller, Reiner Garreis, Jan Willem Gemmink, Janice Golda, George Gomba, Maureen Hanratty, Isamu Hanyu, Naoya Hayashi, Scott Hector, Dan Herr, Iwao Higashikawa, B. Y. Hsu, Jerry Huang, J.R. Hwang, Koki Inoue, Rainer Kaesmaier, Masaomi Kameyama, S. H. Kau, Yoshio Kawai, Beth Kells, Hyeong-Soo Kim, Kurt Kimmel, Y. C. Ku, H. C. Kuo, Keishiro Kurihara, Benjamin Lin, Burn J. Lin, C. H. Lin, J. T. Lin, John Lin, Susumu Mori, Shigeru Moriya, Shinji Okazaki, Yoshimitsu Okuda, Se-Jin Park, Dave Patterson, S. Y. Po, Sergei Postnikov, Chris Progler, Morde Rothschild, Masaru Sasago, Gil Shelden, Phil Seidel, C. L. Shih, Kazuyuki Suko, Takashi Taguchi, Yoichi Takehana, Hidehito Tanaka, Rebecca Tang, Tsuneo Terasawa, Walt Trybula, H. C. Tsai, Takayuki Uchiyama, Gerd Unger, Mauro Vasconi, Keiji Wada, Ulrich Wagemann, C. M. Wang, Lon A. Wang, M. H. Wang, Phil Ware, John Wiesner, Grant Willson, Masaki Yamabe, Yuichi Yamada, Atsuko Yamaguchi, Tadayuki Yamaguchi, Thomas Zell

Interconnect—Nobuo Aoi, Lucile Arnaud, Hans-Joachim Barth, Ivan Berry, Christopher Case, Kow-Ming Chang, Bau-Tong Dai, Mamoru Endo, Manfred Engelhardt, Alexis Farcy, Paul Feeney, Akira Fukunaga, Bob Geffken, Marilyn Glendenning, Narishi Gonohe, Dirk Gravesteijn, Harold Hosack, Calvin Hsueh, Calvin Hsueh, Fred Huang, Masayoshi Imai, Makiko Kageyama, Si-Bum Kim, Mauro Kobrinsky, Noh-Jung Kwak, Han-Choon Lee, Hyeon-Deok Lee, Hyeon-Dyuck Lee, Gene Li, J.D. Luttmer, Mike Mills, Hiroshi Miyazaki, Ken Monnig, N.S. Nagaraj, Tomoji Nakamura, Gary Ray, Rick Reidy, Guenther Schindler, Hideki Shibata, Winston Shue, Hyunchul Sohn, Michele Stucchi, Tony Tsai, Manabu Tsujimura, Kazuyoshi Ueno, David Wu, Osamu Yamazaki, C. H. Yu, Douglas Yu

Factory Integration—Hiroyuki Akimori, Josef Bichlmeier, Mike Bufono, Hugo S.C. Chang, Jonathan Chang, Wesley W. H. Chang, Al Chasey, Allan Chen, Thomas Chen, Gilbert Chiang, Eric Christensen, Ron Denison, Klaus Eberhardt, Patrick Fernandez, Neil Fisher, Len Foster, Ashwin Ghatalia, Barbara Goldstein, Arieh Greenberg, Sven Hahn, Chung Soo Han, Parris Hawkins, Michio Honma, George Horn, J. J. Hsu, Giichi Inoue, Junji Iwasaki, Mani Janakiram, Melvin Jung, Kazuhiro Kakizaki, Franklin Kalk, Atsuhiko Kato, Shigeru Kobayashi, Shoichi Kodama, Todd Lasater, In-Kyu Lee, Ya-Shian Li, Ricky Lin, Maggie Liu, Span Lu, Les Marshall, Dave Miller, Akira Mitsui, Eckhard Müller, Hideki Nakajima, Seiichi Nakazawa, Richard Oechsner, Mikio Otani, Chel-Soo Park, S. H. Park, Suk-Hee Park, Jeff Pettinato, Dev Pillai, Lisa Pivin, Scott Pugh, Adrian Pyke, JB Ragothaman, Claus Schneider, Mike Schwartz, Steve Seall, Marlin Shopbell, Arnie Steinman, Dan Stevens, Peggy Su, Abol Taghizadeh, Junichi Takeuchi, T.M. Tseng, K.R. Vadivazhagu, Joost van Herk, Philippe Vialletelle, Harvey Wohlwend, Hiromi Yajima, Makoto Yamamoto, William W.L. Yuan

Assembly and Packaging—Joe Adam, Steve Adamson, Mark Bird, Bill Bottoms, Kwang-Yu Byun, Chi-Shih Chang, Bill Chen, Carl Chen, Paul Chen, Wen Yan Chen, David Cheng, P. K. Chiang, Young-Bok Choi, Tsung-Yao Chu, Dan Evans, Nobuo Futawatari, George Harman, Shuya Haruguchi, Ryo Haruta, James Ho, Ted Ho, S. P. Hsu, Chender Huang, Lewis L. Hwan, Mahandevan Iyer, Hisao Kasuga, Michitaka Kimura, Eric Kung, Dong-Ho Lee, R.S. Lee, Simon Li, Mirng-Ji Lii, M.S. Lin, Hermen Liu, Shelton Lu, Hirofumi Nakajima, Kieth Newman, Kazuo Nishiyama, Bob Pfahl, Klaus Pressel, Bernd Roemer, Young-Bin Sun, Coen Tak, Kuniaki Takahashi, Takashi Takata, Ho-Ming Tong, F.J. Tsai, Ruenn-Bo Tsai, Shigeyuki Ueda, Shoji Uegaki, Henry Utsunomiya, Juergan Wolf, David Wu, Enboa Wu, Vincent Yang, Wen Kun Yang, Wilson Yang, Zhiping Yang, Eiji Yoshida

Environment, *Safety*, *and Health*—Junichi Aoyama, Hans-Peter Bipp, Roger Chang, George Chen, Steve Cho, Geun-Min Choi, Terry Francis, Nigel Hsu, Ho-Song Hwang, Francesca Illuzzi, Jim Jewett, CY Kao, Shou-Nan Li, C.N. Lin, Sam Lin, Mary Majors, Ed McCarthy, Mike Mocella, Joseph K.C. Mou, Larry Novak, Takayuki Oogoshi, Chyr-Hwan Suen, Tetsu Tomine, Ming Shih Tsai, Sy-Wen Wong, Ted Wong, Walter Worth, Tim Yeakley, Jung-Pin Yu

Yield Enhancement—Scott Anderson, Hyun-Chul Baek, Tracey Boswell, Mark Camenzind, Jan Cavelaars, Kristen Cavicchi, C. H. Chang, Chung-I Chang, Jeff Chapman, Chan-Yuan Chen, Victor Chia, Do-Hyun Cho, Uri Cho, James S. Clarke, J-M. Collard, Mark Crockett, Dirk de Vries, John Degenova, James Dougan, Diane Dougherty, Francois Finck, Tom Gutowski, Jeffrey Hanson, Rob Henderson, Benoit Hirschberger, Christoph Hocke, Ji Ho-Hong, J.J. Hsu, Jim Huang, Steven Hues, Yoji Ichiyasu, Masahiko Ikeno, Francesca Illuzzi, Rick Jarvis, Jim Jewett, Wang Jiun-Fang, Billy Jones, C. S. Jou, Keith Kerwin, John Kurowski, Sumio Kuwabara, M T Liu, Mingo Liu, Y.T. Liu, Chris Long, Michael Lurie, Steven Ma, James McAndrew, Robert McDonald, Mike McIntyre, Len Mei, Yoko Miyazaki, Fumio Mizuno, Mansour Moinpour, William Moore, Chris Muller, Yoshinori Nagatsuka, Andreas Neuber, Kazuo Nishihagi, Andreas Nutsch, Joseph O'Sullivan, Akira Okamoto, Takanori Ozawa, Shang-Kyun Park, Kevin T. Pate, Dilip Patel, Lothar Pfitzner, Dieter Rathei, Ron Remke, Mike Retersdorf, Ralph Richardson, J. Ritchison, Dave Roberts, Dan Rodier, John Rydzewski, Koichi Sakurai, Tony Schleisman, Sarah Schoen, Hisaharu Seita, C. H. Shen, Yoshimi Shiramizu, Val Stradzs, Ed Terrell, Ines Thurner, Bart Tillotson, Ken Tobin, Stephen Toebes, Jimmy Tseng, Ken Tsugane, Hank Walker, Tings Wang, Jian Wei, Dan Wilcox, Hubert Winzig, Walter Worth, Albert Wu, Yuichiro Yamazaki , C. S. Yang

Metrology—John Allgair, Chas Archie, Mike Bishop, Dick Brundle, Michele Buckley, Ben Bunday, Hugo Celio, Fang-Cheng Chen, Man-Ho Cho, Alain Diebold, Shinji Fujii, Dick Hockett, Jia-Rui Hu, Chin Yi Huang, P.Y. Hung, Masahiko Ikeno, Jung-Yeul Jang, Soo-Bok Jin, David Joy, Eiichi Kawamura, Chul-Hong Kim, Steve Knight, Isao Kojima, King Lee, Pete Lipscomb, Ulrich Mantz, Jack Martinez, Joaquin Martinez, Fumio Mizuno, Kevin Monahan, Kazuo Nishihagi, Baw-Ching Perng, Noel Poduje, Michael Postek, Jimmy Price, Gary Rubloff, Jyu-Horng Shieh, Jyu-Horng Shieh, Chin Soobok, Rien Stoup, Aritoshi Sugimoto, Vladimir Ukraintsev, Brad van Eck, Mauro Vasconi, Dick T.A.P. Verkleij, Andras Vladar, Dan Wack, Atsuko Yamaguchi, Yuichiro Yamazaki, Stefan Zollner

Modeling and Simulation—Doelf Aemmer, Susumu Asada, Vivek Bakshi, Augusto Benvenuti, Lars Bomholt, Ingo Bork, Stephen M. Cea, Y. T. Chia, Yong-Soo Cho, Jae-Hoon Choi, An De Keersgieter, Wolfgang Demmerle, Andreas Erdmann, Masato Fujinaga, Youichi Hayashi, Anco Heringa, Howard Huff, Noriyuki Ishihara, Herve Jaouen,

Christian Kalus, Mitsunori Kimura, Karson Knutson, Jun Komachi, Erasmus Langer, Giles Le Carval, Keun-Ho Lee, Keun-Ho Lee, Jürgen Lorenz, Chris A. Mack, Meyya Meyyappan, Rainer Minixhofer, Wolfgang Molzer, Christoph Müller, Mitsutoshi Nakamura, Seiji Ogata, Marius Orlowski, Shane Palmer, Paul Pfäffli, Peter Pichler, Concetta Riccobene, Shigeo Satoh, F. Schellenberg, Vivek Singh, Walt Trybula, Peter L.G. Ventzek, Tetsunori Wada, Tiger Wang, J. Wiley, Reinout Woltjer, Robert Wright, Jeff Wu, Bernhard Wunderle, Peter Zeitzoff, Song Zhao

REGIONAL SUPPORT TEAMS

We acknowledge and thank the regional teams for their support:
◈*Europe—Infineon*—Carola Siebert, *SEMI Europe*—Johanna Turpeinen, Fred Kolbe, and Walter Roessger
◈*Japan*—Yasuaki Hokari
◈*Korea*—Jae-Min Jun
◈*Taiwan*—Celia Shih
◈*USA*—Yumiko Takamori, Linda Wilson
Intel meeting support team—Sally Yanez, Barbara Pebworth
International SEMATECH—Dave Anderson, Debra Elley, Sue Gnat, Mario Gonzales, Sarah Mangum, Marilyn Redmond, Bob Ruliffson, Donna Towery
National Science Foundation—Mihail Roco
SEMI North America— Pat Gardner, Jody Sullivan
SIA—Judy Ajifu Rodgers

FOREWORD

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus-building process. This document predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A. ensures that the ITRS is a valid source of guidance for the semiconductor industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. These five regions jointly sponsor the ITRS.

The Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally *The National Technology Roadmap for Semiconductors* (*NTRS*). The semiconductor industry became a global industry in the 1990s, as many semiconductor chip manufacturers established manufacturing or assembly facilities in multiple regions of the world. This realization led to the creation of the *International Technology Roadmap for Semiconductors* in the late 90s. The invitation to cooperate on the ITRS was extended by the SIA at the World Semiconductor Council in April 1998 to Europe, Japan, Korea, and Taiwan. Since then, full revisions of the ITRS were produced in 1999, 2001 and 2003; ITRS updates were produced in the even-numbered years (2000, 2002, 2004).

The 2005 ITRS represents a major departure from the previous versions of Roadmaps because it removes the concept of "technology node" as the main pace setter for the IC industry. In the past, DRAM products set the technology pace by quadrupling the number of bits every three years with the introduction of a new major technology generation. The relation among transistor density (4×) and metal half-pitch (×0.7) and year of introduction (three-year) remained constant from the mid-70s to the mid-90s. The reduction from generation to generation of the DRAM half-pitch of metal by 30% (0.7× the previous technology generation) identified a "technology node." However, the increase in the number of bits by four times from one technology node to the next led to a continuous increase in die size that eventually negatively affected the economics of this silicon cycle. In an attempt to minimize the increase in die size many IC companies accelerated the speed at which new technology nodes were introduced from a three-year cycle to a 2–2 ½-year cycle in the second half of the 90s.

As device features become smaller, MPU and Flash technologies have been approaching (and in some cases producing) features even smaller than DRAM. Additionally, MPU and Flash products have been introduced at a comparable or, at times, even faster pace than DRAMs. As a result, the use of a single number (such as a technology node) derived from the half-pitch of DRAM no longer suffices to characterize the whole semiconductor industry. The 2005 ITRS addresses an independent measure of the technology pace of DRAM, of MPU, and of Flash products.

Another change in the 2005 ITRS indicates the growing interest in new nanoscale devices representing alternatives to CMOS. Emerging Research Devices topics are now addressed in a separate chapter from the Process Integration, Devices, and Structures chapter. Indeed, even though CMOS is (and will remain) the industry workhorse up to and beyond the year 2020, it is anticipated that new devices will be introduced in the latter half of the next decade utilizing different and new ways of processing and storing information. Most of the proposed devices rely very heavily on new material properties and therefore, a new sub-chapter on Emerging Research Materials has been added to the ERD chapter.

In conclusion, it is the purpose of the ITRS documents to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university, consortia, and government labs.

The ITRS documents have become and remain a truly common reference for the entire semiconductor industry. Indeed, the cooperative efforts of the ITRS participants have fostered cooperation among international consortia, universities, and research institutions around the world. It is hoped that the 2005 ITRS will further contribute to stimulate cooperative R&D investments so that the financial burden can be more uniformly shared by the whole industry. It is also hoped that the 2005 ITRS will continue to stimulate the fundamental elements that encourage innovation in individual companies.

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INTRODUCTION

OVERVIEW

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements of productivity and quality of life through proliferation of computers, electronic communication, and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. *The International Technology Roadmap for Semiconductors (*ITRS*)* has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further reduce the cost per function (historically, ~25–29%% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?" This challenge has become so formidable that increasingly more of the semiconductor industry's research effort, including consortia and collaboration with suppliers, has been shared in a precompetitive environment.

The 2005 ITRS is the fourth fully revised edition and the result of the continued worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensures that the 2005 ITRS continues to be the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The diverse expertise and dedicated efforts that this international effort mobilized have brought the Roadmap to a new level of worldwide consensus about future semiconductor technology requirements.

The complete 2005 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site *http://public.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the international technology working groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The international technology working groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2005 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices / Emerging Research Materials
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. In 2005, 1288 experts participated in revising the Roadmap (a 27% increase from the 2003 participants). The composition of the total TWG membership is analyzed in Figure 1.

The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

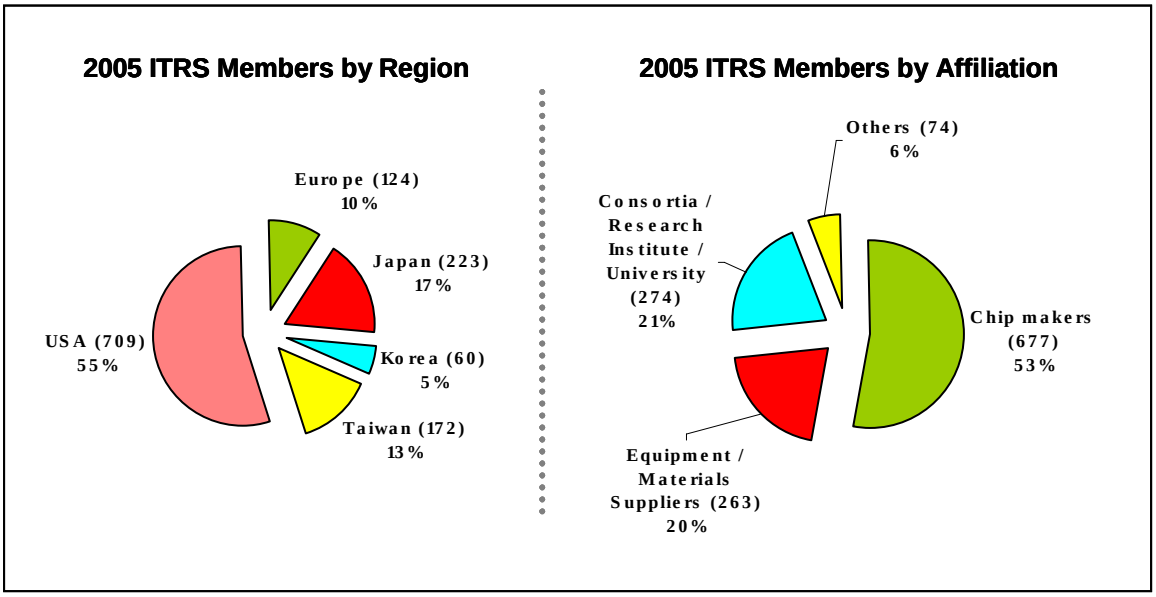


Figure 1 Composition of the ITRS Teams—1288 Global Participants

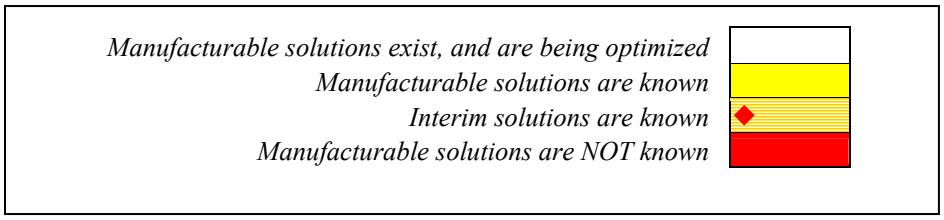
For the 2005 edition, three ITRS meetings were held worldwide as follows: Munich, Germany (sponsored by the ESIA and hosted by Infineon); San Francisco, U.S.A., sponsored by the SIA and organized by SEMATECH; and Seoul, Korea (sponsored and hosted by the KSIA). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004) while complete editions are released each odd-numbered year (2001, 2003, 2005). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS identifies the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity or confidence levels, represented by colors in the tables, for these targets:



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap

technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

A good example of that is the adoption, in this 2005 edition of the Roadmap, of 2012 as the year of introduction of 450 mm wafers in volume production. While this date was based on an economics model, it should not be seen so much as a forecast at this stage, than as a way to induce the working groups to focus on the various technical issues associated with such a transition to 450 mm.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the roadmap, and it proved itself very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS roadmapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2005 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2005, 2006… through 2013) and "Long-term Years" (2014, 2015 … through 2020) This format is illustrated in Table B, which contains a few key rows from lithography-related ORTC Table 1a and 1b, including the new Flash product uncontacted polysilicon half-pitch technology trend line item. Only the DRAM stagger-contacted M1 half pitch line item is used as a standard header for all the 2005 ITRS ITWG tables. At the discretion of the ITWGs, other product technology trend driver line items may be selected from ORTC Table 1a and 1b for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

YEAR OF PRODUCTION	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	80	70	65	57	50	45	40	36	32
MPU/ASIC stagger-contacted Metal 1 (M1)½ Pitch (nm)	90	78	68	59	52	45	40	36	32
Flash Uncontacted Poly Si ½ Pitch (nm)	76	64	57	51	45	40	36	32	28
MPU Printed Gate Length (nm)	54	48	42	38	34	30	27	24	21
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13

Long-term Years

YEAR OF PRODUCTION	2014	2015	2016	2017	2018	2019	2020
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	28	25	22	20	18	16	14
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	28	25	22	20	18	16	14
Flash Uncontacted Poly Si ½ Pitch (nm)	25	23	20	18	16	14	13
MPU Printed Gate Length (nm)	19	17	15	13	12	11	9
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes. However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver.

For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition is already reflected in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. Thus, in the 2005 ITRS, we no longer use the term "technology node." Instead, each distinct scaling feature is specifically referenced as such. Note that, for some degree of continuity, we are still showing DRAM M1 half-pitch at the top of many tables, but it is no longer described as the measure of "technology node." It is just one among several historical indicators of IC scaling. With this change, it is hoped that the ITRS will no longer contribute to industry confusion related to the concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage in each case, for example, the metal-1 pitch of their specific product.

For reference on the 2005 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 2.

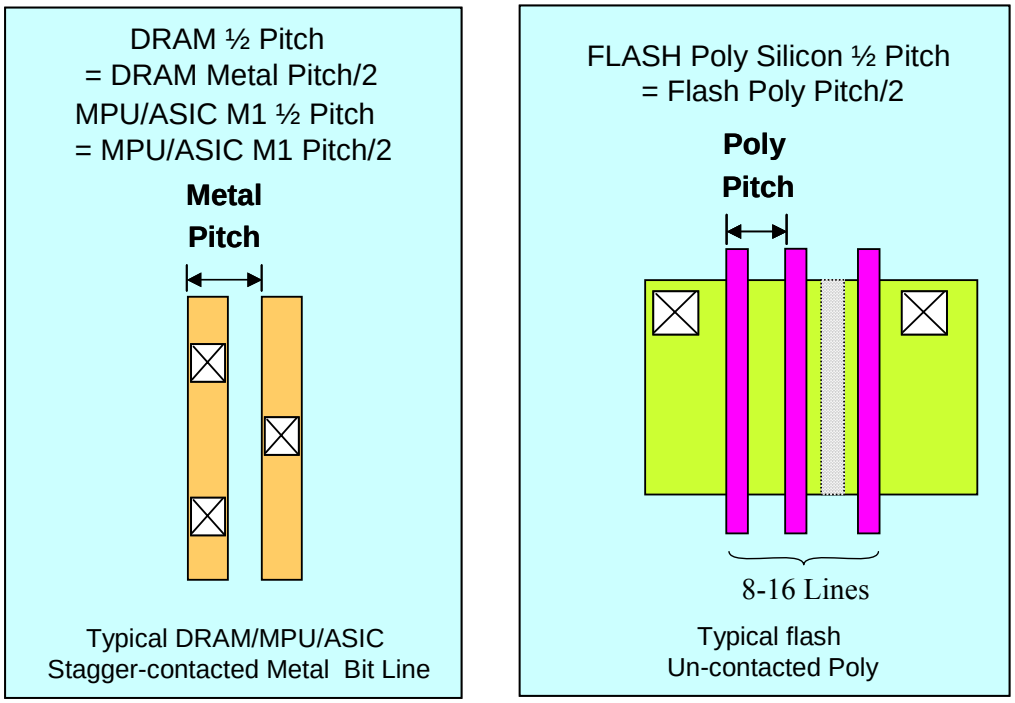


Figure 2 2005 Definition of Pitches

MEANING OF ITRS TIME OF INTRODUCTION

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 3.

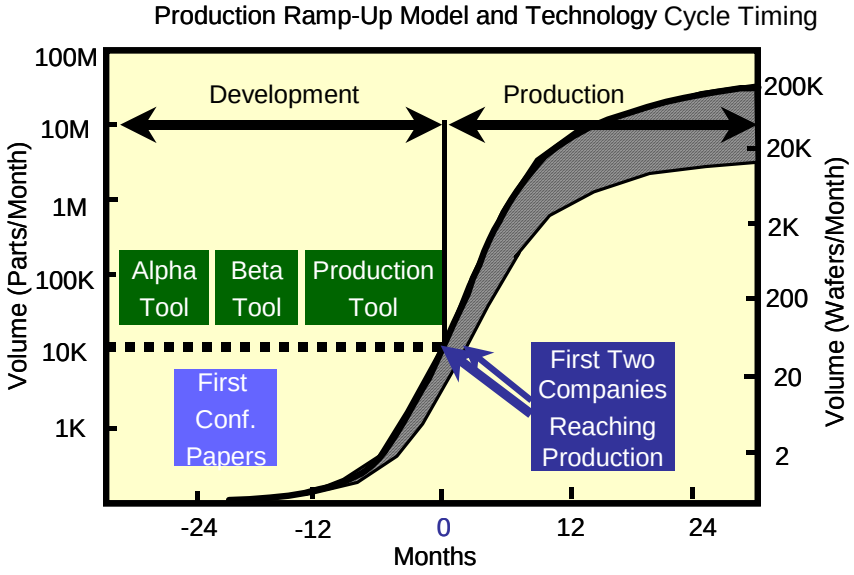


Figure 3 A Typical Production "Ramp" Curve

The "Production" time in the ITRS refers to the time when the first company brings a technology to production and a second company follows within three months. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figure 3 can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month).

2005 SICAS INDUSTRY MANUFACTURING TECHNOLOGY CAPACITY UPDATE

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

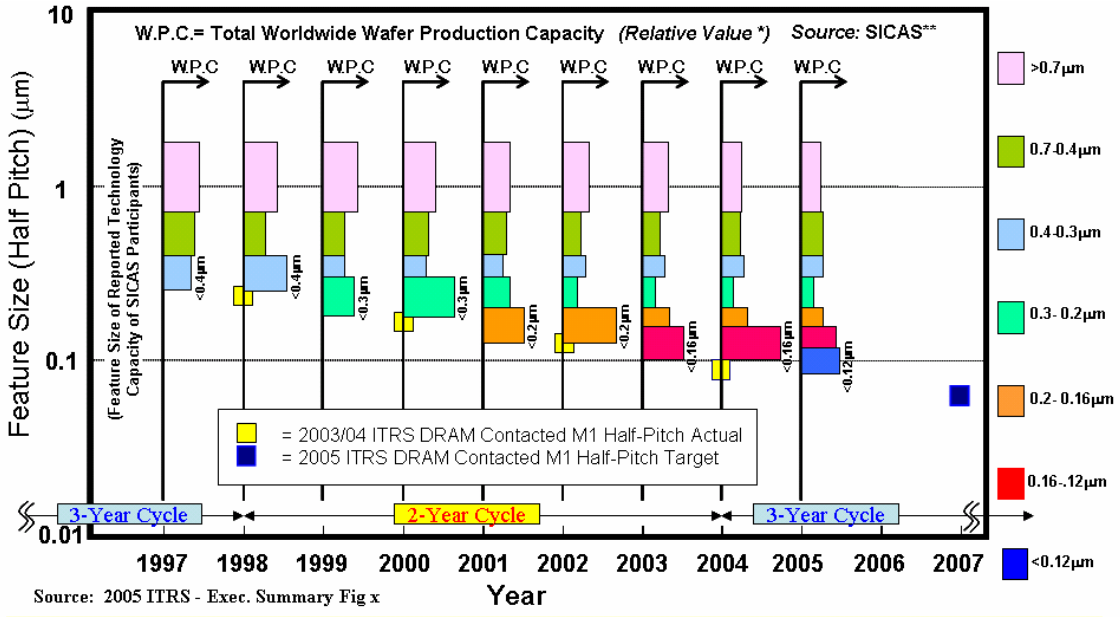
Figure 4 shows, in horizontal bar graph format (normalized by bar area to total MOS IC industry silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits, which are quite widespread.

The ITRS technology cycle, as measured by DRAM metal 1 (M1) half-pitch, is shown as yellow marks (for the historical actual timing), as reported by the industry surveys conducted by ITRS TWGs. The surveys conducted in 2003 and 2005 have indicated that first production of the leading-edge DRAM M1 half-pitch has been on a two-year cycle (for 0.71× reduction), from 250 nm in 1998 through 90 nm in 2004. The blue mark indicates the timing for the next 2005 ITRS target for the 65 nm technology in 2007. Subsequent targets for 0.71× reduction of the DRAM M1 half-pitch are placed on a three-year cycle through the present ITRS roadmap horizon in 2020.

Note that the first production of the leading-edge feature size ramps into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the timing for first production. Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations rapidly grows to nearly half the capacity of the industry within two to three years after their introduction.

However, it is also notable that relative share of trailing edge capacity does not appear to decline rapidly (migrate upward to leading-edge), and the leading-edge capacity split shares get "crowded" as products migrate to the next leading-edge capacity. This phenomenon has significant implications to the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology "grand challenge."

Suppliers must support not only longer-lasting trailing edge factories, but also many diverse technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge.



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2005. The area of each of the production capacity bars corresponds to the relative share of the Total MOS IC production start silicon area for that range of the feature size (y-axis). Data is based upon capacity if fully utilized.*

Figure 4 Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution[1]

ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. Thus new technologies may involve not only new devices, but also new manufacturing paradigms.

Microprocessors, memories and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many functional requirements, such as power consumption, wireless communication (RF), passive components, sensing and actuating, and biological functions do not scale with Moore's Law. In many of these cases, non-CMOS solutions are employed. SoC and SiP are not necessarily competing with each other. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, SiP) will become increasingly important. Furthermore, functions initially fulfilled by non-CMOS dedicated technologies can be in a later step integrated onto a CMOS SoC using mixed technologies derived from core CMOS. So the partitioning of system-level functions between SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, etc. For SiP applications, packaging will be a functional element and a key differentiator. Refer to Figure 5 for an illustrative graphic.

[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Supply statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of July, 2005. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm.*

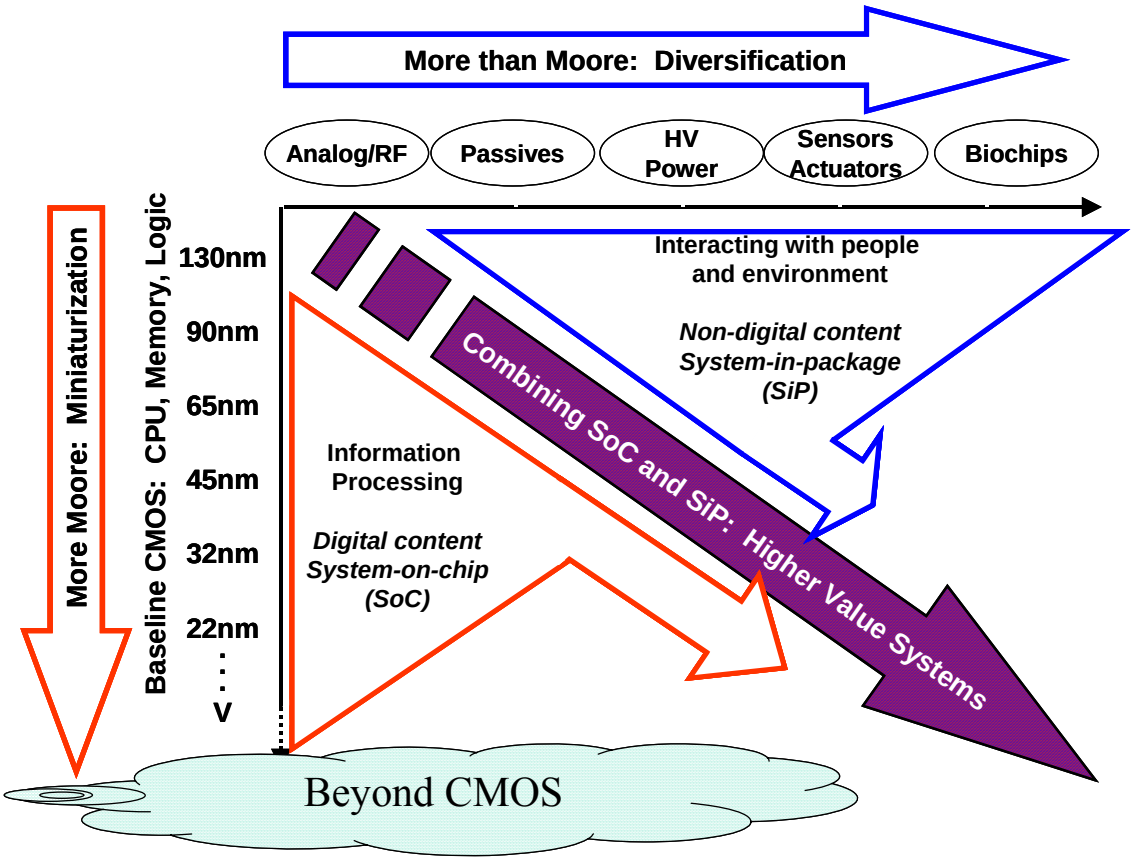


Figure 5 Moore's Law and More

The scope of the 2005 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

POSITION ON POTENTIAL SOLUTIONS

The ITRS strives to avoid prematurely identifying definite solutions to the future technology challenges. This is difficult, since guidance on the research needs is intended. Despite this need to provide guidance, the Roadmap participants are continually pursuing new ways to prevent the Roadmap itself from being interpreted as limiting the range of creative approaches to further advance microelectronics technology. One of the resulting compromises has been to only present *illustrative examples of potential solutions* to selected challenges in the ITRS. These are not to be construed even as complete lists of all solutions suggested to date, much less exhaustive lists of what should be explored. A few of the potential technical solutions are listed, where known, only to inform the readers of current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process.

It *is* the intent of this document to identify the technological barriers and when the industry will likely run into them. It is *not* the intent of this document to identify the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other new concepts. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative solutions. *The semiconductor industry's future success continues to depend on new ideas!*

2005 ITRS SPECIAL TOPICS

WIRELESS TECHNOLOGY

In past years the scope of the ITRS has been widened continuously: In the 2003 version of the ITRS a new sub-chapter on Wireless Technologies was included to take into account that mobile applications have quickly grown to become an

important driver for semiconductor products and technologies. The ITRS had therefore been expanded by extending the scope of the already existing analog and mixed-signal (AMS) working group to include radio frequency (RF) technologies for wireless communication and also III-V compound semiconductors in the 2003 ITRS Roadmap as a section in the Process Integration chapter. In the present 2005 ITRS edition, Wireless Technology becomes a separate chapter taking into account the growing importance of this field and its specific performance requirements at the device and system level (low standby power, low operating power).

EMERGING RESEARCH DEVICES

The 2001 ITRS document marked the additional investigation of the limits of traditional scaling, its extension by improving electrical performance with new or improved materials and of the introduction and feasibility of new device architectures. This new section on Emerging Research Devices (ERD), first presented in 2001 highly coordinated with the Process Integration, Devices, and Structures (PIDS) chapter, has evolved considerably since then. In this 2005 ITRS edition, Emerging Research Materials is now a separate chapter.

Some of the new device and memory concepts that were previously discussed in the ERD section have become more mature in the recent years. Therefore these concepts have been transferred from the ERD chapter into the PIDS and Front End Processes (FEP) chapters. This transfer includes the so-called non-classical CMOS devices, both single-gate and multi-gate architectures, as well as the phase-change-memory and the floating-body DRAM.

EMERGING RESEARCH MATERIALS

Many of the new device and memory concepts that are being discussed in the ERD chapter will employ new materials, for example, for the device itself as well as for interconnect and passivation. The requirements for these new materials are critically dependant on the properties and specifications of the new devices and memories. To support the Technology Working Group of ERD, a sub-group for Emerging Research Materials (ERM) has been formed. The results of this work are published in the Emerging Research Materials (ERM) sub-chapter in the ERD chapter.

GRAND CHALLENGES

IN THE NEAR- (THROUGH 2013) AND LONG-TERM (2014 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling, although the 2003 edition of ITRS reported on the deceleration of scaling envisaged by Moore's Law to a three-year cycle. Flash device's scaling is still a two-year cycle until 2006, MPU is a 2.5-year cycle until 2010, and DRAM is a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planer bulk MOSFET, FD-SOI MOSFET, and Fin-FET. The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges to be overcome to achieve continuing growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges." In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues. It should be noted there are many other important challenges that are not included in this section. ITRS is rather intended to encourage creative and flexible approaches to advanced microelectronics technologies.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2005 through 2013) and the "long term" (2014 through 2020) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~2013)

ENHANCING PERFORMANCE

SCALING OF MOSFETS TO HALF PITCH 32 NM [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

Scaling planar bulk CMOS will face significant challenges. The required high-channel doping to control short-channel effects degrades carrier mobility, lowers the drain current, and increases band-to-band tunneling across the junction and gate-induced drain leakage (GIDL). Moreover, statistical fluctuation of channel dopants causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. Implementation into manufacturing of new structures such as ultra-thin body, fully depleted silicon-on-insulator (SOI), and multiple-gate MOSFETs (e.g., finFETs) is expected. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and architecture improvements, particularly to manage power dissipation.

SIGNAL ISOLATION [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Signal isolation, especially between the digital and analog regions of the chip, is a particular challenge for scaled technologies and for increased integration complexity. Noise coupling may occur through the power supply, ground, and shared substrate. The difficulty of integrating analog and high-performance digital functions on a chip increases with scaling in both device geometry and supply voltage. Signal isolation is critical for success in co-integrating high performance analog circuits and highly complex digital signal processing (DSP) functions on the same die or substrate. Such co-integration is required in many modern communication systems to reduce size, power, and cost.

HIGH-PERFORMANCE AND LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Fundamental changes in materials and structures of the low standby power (LSTP) devices will be required to sustain continued performance and density improvement. The introduction of new materials such as high-permittivity (high-κ) gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes makes predicting trends uncertain for threshold and current mismatch and for 1/f noise. The electrical characteristics of non-classical CMOS, such as dual-gate, fully depleted SOI devices, are fundamentally different than that of conventional CMOS. These differences include benefits for circuit designers as well as obstacles to be overcome. Thus, the fabrication of

conventional precision analog/RF driver devices, resistors, and varactors may require separate process steps with the attendant increase in die cost. Furthermore, the steady reduction in analog supply voltage poses a significant circuit design challenge.

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Equivalent electrical oxide thickness becomes increasingly thinner due to the requirement for CV/I improvement. Reduction of the equivalent gate oxide thickness (EOT) has emerged as the most difficult challenge associated with the future device scaling. Continued optimization of oxynitride gate dielectric and scaling of this material toward EOT of less than 1 nm consistent with device reliability is envisaged for high-performance (HP) MPU. Oxynitride, however, will no longer meet the strict leakage current requirement in low-power applications (low operating power (LOP) and LSTP). Therefore, introduction of higher dielectric constant (high-κ) material in which tunneling current can be suppressed while maintaining the drain current will be necessary. In either case, the gate electrode material and process should be optimized so that the depletion width in the gate electrode may be minimized and the boron-diffusion prevented. The former necessitates the introduction of metal gates having appropriate work function after the conventional poly Si ceases to work. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system and also these new high-κ and metal gate stacks are fundamental structure expected to be used with the future new structure CMOS such as fully-depleted SOI or multi-gate MOSFETs.

CMOS INTEGRATION OF NEW MEMORY MATERIALS AND PROCESSES [FRONT END PROCESSES]

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance of 25–35 fF to ensure reliability of stored data. This has resulted in the introduction of dielectric materials with a high dielectric constant (high-κ), such as aluminum oxide, aluminates (for example, HfAlOx) and tantalum oxide, along with a three-dimensional (3D) memory structure. The capacitor structures are shifting from metal-insulator-silicon (MIS) to metal-insulator-metal (MIM) to avoid problems associated with capacitor dielectric thickness. For further scaling, however, it will be necessary to address process construction by using a thinner dielectric film and/or a higher dielectric constant material.

In Flash memory devices, on the other hand, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. This difficult trade-off problem hinders scaling, suggesting the need to introduce high-κ material and 3D structure devices into Flash memory process. Along with scaling issue of ferroelectric material in FeRAM, process integration of these materials and 3D capacitor will continue to pose major challenges in the development of memory applications.

IMMERSION LITHOGRAPHY [LITHOGRAPHY]

As a successor to ArF lithography, immersion technology has the potential to extend optical lithography down to 32 nm half pitch, with lesser focus on the other candidates for the post-ArF lithography. To realize immersion lithography in volume production in time it is imperative to ensure its maturity. Control of defects, including bubbles, and staining developed within the immersion environment has been a critical issue in immersion lithography, and improvement of immersion resists and top-coats is required urgently. The proposed line widths are smaller than those for existing ArF lithography, so, as a result, the resist performance requirements for immersion, such as line edge roughness (LER), scanning electron microscope (SEM) induced critical dimension (CD) changes and defects size, are difficult. Moreover, to extend immersion lithography down to 32 nm half-pitch requires development of resist with a very high index of refraction, high index immersion fluid, its recycling system, and higher index lens materials.

EUVL: EXTREME ULTRA VIOLET LITHOGRAPHY [LITHOGRAPHY]

Although immersion technology shows the possibility of extending optical lithography down to 32 nm half pitch, lithography beyond this is controversial. Candidates for post-optical lithography are extreme ultraviolet lithography (EUVL), mask-less lithography (ML2), and imprint technology. EUVL has noticeably higher throughput than the other candidates, and has the potential to cover from 45 nm to 16 nm half pitches and beyond. In order to introduce EUVL into volume production in time, there are many remaining issues requiring real solutions that must satisfy both technical and economical considerations. These issues include mask blank defect level, light source, resist, optics performance, contamination of optics, protection of mask without pellicle, and so on.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are both commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. In addition, it is becoming very difficult to suppress LER, which depends on gate material, photoresist type, and etch chemistry, even by the optimum control of resist printing and etching. CD control and LER measurement also pose challenges to metrology in terms of accuracy and efficiency. Since off-current between source and drain may be affected by the LER, target for controlling LER should be set with understanding the impact of LER on device performance. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, development of low dielectric constant (low-κ) material together with low-resistivity metal system is critical. Low-κ material should have sufficient mechanical/chemical/thermal integrity to survive harsh integration processes, such as chemical mechanical planarization (CMP), etching/ashing/wet cleaning, and assembly/packaging. Since resistivity of narrow Cu interconnect wire is predicted to start to increase below 100 nm line width due to electron scattering at the Cu/barrier-metal interface and the grain boundary, and the influence on circuit performance is becoming serious gradually for intermediate wiring since 65 nm half pitch (circa 2007), care should be taken at 32 nm half pitch (circa 2013). "Barrier engineering" including construction of very thin and low-resistive barrier metal, as well as efficient "pore sealing" for low-κ material, is essential to achieve high conductivity in a narrow Cu interconnect.

ENGINEERING MANUFACTURABLE INTERCONNECT STRUCTURES [INTERCONNECT]

Introduction of new materials and technologies for interconnect has raised additional issues due to their combinations and interactions. These include adhesion at the interfaces, contamination, diffusion, and leakage concerns. The revealed issues related to mechanical and chemical damage by CMP and etching/ashing/wet process should be solved. Complexity in interconnect structure also makes the effective dielectric constant deviate from its intrinsic value. Failure mechanisms in the Cu/low-κ systems should be clarified, along with establishment of detection metrology and predictive models. In regard to assembly and packaging technology, lack of optimization tools for interconnect/packaging architecture design makes total optimization of interconnect system difficult.

MANAGEMENT OF OVERALL POWER CONSUMPTION [DESIGN]

Non-ideal scaling of planar CMOS devices, together with the roadmaps for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery. First, extrapolation from the Overall Roadmap Technology Characteristics and the System Drivers chapter shows that high-performance MPU power consumption significantly exceeds the high-performance single-chip package power limits established in the Assembly and Packaging chapter, even with allowed power densities in excess of 250 W/cm^2. The SOC-Power Efficient (PE) driver requires flat or almost flat power, even as logic content (even in the presence of massive multi-processing) and throughput continue to grow exponentially. Design technology (DT) must address the resulting power management gap, which is reiterated in the System Drivers chapter. Additionally, increasing power densities worsen thermal impact on reliability and performance, while decreasing supply voltages worsen switching currents and noise. These trends stress on-chip interconnect resources (such as to control infrared (IR) drop in light of the Assembly and Packaging roadmap for bump count and passivation opening size), automatic test equipment (ATE) limits, and burn-in paradigms. Integration of distinct HP, LOP, and LSTP devices demands power optimizations that simultaneously exploit many degrees of freedom, including multi-V_t, multi-T_{ox}, multi-V_{dd} inside cores and among cores—while guiding additional power optimizations at the architecture, operating system, and application software levels.

HIGH-FREQUENCY DEVICE AND CIRCUIT MODELING FOR 5-100 GHZ APPLICATIONS [MODELING AND SIMULATION]

Accurate and efficient modeling of interconnect parasitics and delays is of prime importance. Two-dimensional (2D) and three-dimensional (3D) effects on interconnects must be considered with their statistical variations. Partitioning is needed for distributed R-L-C extractions. Efficient simulation technique should handle multi-layer dielectrics. Compact models are needed for active devices, such as hetero junction bipolar transistors (HBTs), CMOS, laterally diffused (LD)

MOSFETs, and III/V materials. These include non-quasi-static effects, substrate noise, 1/f noise, and surrounding parasitics. Compact models are needed for passive devices (for example, varactors, inductors, high-density capacitors, transformers, and transmission lines). These parameter extractions for RF compact models preferably try to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Modeling of effects that have a more global influence gains importance. Examples are crosstalk, substrate return path, substrate coupling, electromagnetic (EM) radiation, and heating. For these global effects, accurate and efficient layout extractions are needed. If possible, models should be physics-based to enable efficient modeling of statistics and variations.

FRONT-END PROCESS MODELING FOR NANOMETER STRUCTURES [MODELING AND SIMULATION]

Front-end process modeling for nanometer structures is a key challenge for the prediction of device performance. It overlaps to some extent with the Difficult Challenge of "Ultimate nanoscale CMOS simulation capability," which also includes material and device simulation. Most important and challenging in the area of front-end process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing, diffusion and activation of dopants under implantation damage and stress. Due to the strongly reduced thermal budgets needed for shallow junction, the junction formation process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of dopant atoms and defects. Implantation damage, amorphization, recrystallization, and silicidation must be accurately simulated. To meet these requirements, hierarchy approach from atomistic to continuum of dopants and defects are needed. Model development, calibration and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects and stress, especially regarding two-dimensional and three-dimensional measurements.

COST-EFFECTIVE MANUFACTURING

SCALING OF MAXIMUM QUALITY DESIGN IMPLEMENTATION PRODUCTIVITY [DESIGN]

The number of available transistors double every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and reusing the design are the key considerations for this issue. Namely, overall design productivity of quality- (difficulty-) normalized functions on-chip must improve at the rate of two times per technology cycle. However, analog and mixed-signal design traditionally suffers from difficulty in improving design productivity and reusing the design along with process migration. There is a pressing need to develop a new design methodology to ameliorate those problems by implementing analog and mixed-signal synthesis, verification, and testing. Embedded software productivity also needs to be improved on a similar scale since the on-chip memory size is also growing and some functions are built into such embedded software rather than the hardware.

ENABLING TEST OF INCREASINGLY COMPLEX DEVICES [TEST AND TEST EQUIPMENT]

Several device trends are presenting great challenges to test. Increasing device IO bandwidth requirements are rapidly driving the proliferation of faster and wider high-speed interfaces. Increasing integration of previously disparate semiconductor technologies in System-On-Chip (SOC) or System-In-Package (SIP) designs are driving significant rethinking of test strategies. Emerging technologies such as RF, analog, optical and MEMs present some unique test challenges and will require significant improvements in test methods as they become more pervasive or integrated with digital CMOS technologies. The increasing variety and complexity of device package designs coupled with an increasing divergence of the electrical/thermal/mechanical characteristics between the end-use and test environments is driving ever more complex and optimized test capability. Finally, several device architecture trends such as more sophisticated power management or self repair mechanisms could lead to new test requirements that depart from the longstanding deterministic stored stimulus and response test model.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law do not translate to test. Design For Test (DFT) innovations, widespread use of structural test techniques such as scan testing, and the enabling of higher levels of test parallelism have been very successful in keeping test costs in check to date. However, new test requirements for increasingly complex devices, increasing quality requirements and practical limits on parallel testing will present great challenges in the future. In particular, some contributors to the total cost of test, such as test tooling (e.g., probe cards), are not scaling and threaten to dominate the total test cost if present trends continue.

INCREASING TEST PROCESS COMPLEXITY [TEST AND TEST EQUIPMENT]

Process complexity is both a grand challenge and an opportunity for test. The value proposition of test has been steadily increasing as semiconductor manufacturers attempt to get more and more out of test. Increasingly, test is used to modify, differentiate, or customize specific die. Increasingly sophisticated data feedback is being used to tune manufacturing. Test for yield learning is already critical and this is expected to become more so with the introduction of new semiconductor processes that will be inherently more variable. Increasing device complexities are also leading to a higher order dimensionality of test conditions (for example, adding multi-power, multi-voltage, multi-frequency topologies as opposed to single valued temperature, voltage and frequency).

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Various types of business models such as integrated device manufacturer (IDM), collaboration between fabless and foundry, joint venture, and variety of task sharing and out-sourcing have emerged and become widespread in response to customers' rapidly changing complex business requirements. It is noteworthy that a high-mix and low-volume manufacturing model is in a strong demand in response to diversified customers' requirement on SoC devices.

Semiconductor manufacturing factories now must integrate and implement an even larger number of new and different capabilities in factory integration technology regime in a much shorter time and cost effective manner. The ultimate goal for this is to realize high product reliability and productivity in volume manufacturing or in the high mix and small volume-manufacturing model. Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge.

Modeling of factory capacity detailed with various parameters and metrics is the base requirement for more comprehensive and integrated factory operation decisions to be made for the necessary optimization among product cycle time, product reliability, and the productivity. It is fundamentally required to establish an information platform on which more abstraction of problems and requirements with the finer granularity of information is to be performed. The Factory Integration chapter is to be referred for "Proactive Visualization" and "Strategically Hierarchical Quality Assurance."

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

It is well known that cost and the manufacturing cycle time are in a trade-off relation among other Factory Integration problems. Job flow manufacturing and single-wafer manufacturing methods have been investigated to improve this problem. The grand premise for these manufacturing methods to be applied is the much higher availability, stability and reliability of the process tools and elimination of non-product wafers (NPW) processing and tool set up operations.

This premise is becoming more difficult to be assumed as manufacturing needs go into the more stringent process rules. This fundamental improvement cannot be achieved by the individual productivity improvement effort by each of the device makers, but it calls for the industry's reformation including revised task sharing where the collaborative efforts are required based on an equipment engineering system (EES) scheme. The implementation of enhanced equipment quality assurance (EEQA) is an immediate challenge as the very first step of this improvement where equipment suppliers are to use an EES scheme to examine equipment capabilities with electronic data out of equipment.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

Many new materials will be introduced in IC packages in next few years in order to meet requirements of environmental regulations, to improve package performance, and to be compatible with low-κ dielectrics used in Cu interconnects with 65 nm half pitch and beyond. Nano-materials present significant opportunities that the packaging community needs to take advantage of. The ICs front-end progress is based upon a high level of investment in material and process technology and equipment. There is no corresponding investment in the back-end for materials, process, and equipment. Wafer-level package and SiP have promises of dramatic cost performance and form factor improvement. The industry will require investment and knowledge of infrastructure to perfect technology of high-volume production. The changing marketplace by consumerization of electronic products presents the tremendous opportunity for the packaging industry in implementing the technologies to fill the gap created by physical limit of Moore's law scaling.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation.

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently.

SIGNAL TO NOISE RATIO [YIELD ENHANCEMENT]

Currently inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Increasing the inspection sensitivity at the same time increases the challenge to find small but yield-relevant defects under a vast amount of nuisance and false defects. At the same time a low cost of ownership (CoO) of the tools is demanded for high throughput inspection. This is in conflict with the issue of improving the signal-to-noise ratio. The key of a successful inspection result is, besides achieved sensitivity, the ease to get to the defects of interest (DOI).

HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel can cause yield problems. Currently, the defect inspection of the wafer edge and the bevel, as well as the wafer backside, is not paid too much attention. Therefore, the defect inspection concepts or technologies are under development or have to be realized within the next years. It is a key challenge to find the root cause inspection of wafer edge, bevel, and apex on the wafer front and backside.

FACTORY LEVEL AND COMPANY WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology and combination of metrology for complement should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). On the other hand *in situ* and inline metrology is becoming requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline metrology), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into a database useful for determining process control parameters and correlating metrology information and yield to enhance yield. Therefore, standards for process controller and data management must be agreed upon and the structure of such a database should be optimized. Sensors, their calibration, sensing method, and data processing are being improved and require continued improvement for precise methodology.

MEASUREMENT OF COMPLEX MATERIAL STACKS [METROLOGY]

Even measurement of film thickness of complex material stacks is difficult for processing wafers. The characterization of complex material stacks and interfacial properties, including physical and electrical properties, is challenging. Direct measurement of stress in a nano-sized and buried area is required. At the same time, reference materials and standard measurement methodologies are critically required for new, high-κ gate and capacitor dielectrics with engineered thin films and interface layers; interconnect barrier and low-κ dielectric layers, as well as other process needs. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. Metal gate work function characterization is another pressing need.

IN THE LONG TERM (~2014 THROUGH 2020)

ENHANCING PERFORMANCE

IMPLEMENTATION OF ADVANCED, NON-CLASSICAL CMOS DEVICE WITH ENHANCED DRIVE CURRENT [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

To continue MOSFET scaling to less than L_g = 15 nm, it is quite likely that the device structure will change to advanced non-classical CMOS such as multiple-gate, ultrathin body (UTB) MOSFETs. In these devices, various "technology boosters," such as mobility enhancement by strained Si, elevated source source/drain, high-κ gate dielectric, and metal gate electrode, will likely be simultaneously implemented with the new device structure. In UTB MOSFETs having less

than 10 nm Si thickness, various quantum effects will impact the electric characteristics. Toward the end of the Roadmap timeframe, devices will increasingly be operated in the quasi-ballistic mode, where the current gain will be enhanced by parameters different from those currently known. Eventually, carbon nanotubes, nanowires, and other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed. Choice of the optimum device structures, their physical characterization, and construction of cost-effective processing flows will become very important along with construction of their circuit architecture.

DEALING WITH FLUCTUATIONS AND STATISTICAL PROCESS VARIATION IN SUB-15 NM GATE LENGTH MOSFETS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

Fundamental issues of statistical fluctuations for sub-15 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, LER, and line width roughness (LWR).

GATE CD CONTROL IMPROVEMENTS AND PROCESS CONTROL [LITHOGRAPHY]

With aggressive scaling of devices, the required gate CD control comes down to 1.3 nm in 3σ with a LWR of less than 1.5 nm in 3σ in 2013 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) Furthermore, resolution and precision measurements for CD down to 7 nm, including LWR metrology of 0.8 nm in 3σ is very challenging, along with the required overlay accuracy of 2.8 nm in 3σ or better in 2019. The maximum permissible defect size on patterned wafer is reduced to smaller than 30 nm. Without metrology and inspection tools having sufficient accuracy and resolution, CD control improvements and process control will be difficult to achieve.

IDENTIFY SOLUTIONS THAT ADDRESS GLOBAL WIRING SCALING ISSUES [INTERCONNECT]

Traditional and classical interconnect parameter scaling will no longer satisfy LSI performance requirements, especially in chip-size long global interconnect with extremely large RC delay. Defining and finding potential solutions beyond Cu conductor and low-κ dielectrics will require material innovation, combined with accelerated system architecture/design, packaging, and unconventional interconnect. Novel interconnect schemes include 3D interconnect, RF/microwave, optical interconnects, etc.

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness, and threshold voltage; this presents severe challenges in light of both scaling and variability. Off-currents in low-power devices increase by a factor of 10 per technology cycle. Therefore design technology must be the key contributor to maintain constant static power.

COST-EFFECTIVE MANUFACTURING

DESIGN FOR MANUFACTURABILITY (LITHOGRAPHY, VARIABILITY) [DESIGN]

Due to manufacturability issues, "red bricks," technology requirements for which no known solutions exist, are increasingly common throughout the ITRS. On the other hand, challenges that are impossible to solve within a single technology area of the ITRS may be solvable (more cost-effectively) with appropriate partnership with design technology. Several examples include design for test (fault models, ATPG, built in self test (BIST)), die-package-board and system-in-package co-design, design techniques to manage variability, and intelligent interfaces to mask production and inspection flows. Manufacturability, i.e., the ability to produce a chip in large quantities at acceptable cost and according to an economically feasible schedule, is one such challenge that requires design-for-manufacturing (DFM) techniques. Manufacturability is affecting design primarily due to lithographic hardware limitations. In the long term it will become a major crisis as variability builds on these limitations in its multiple forms and dramatically invades all aspects of a design.

NEXT GENERATION STARTING MATERIALS GREATER THAN 300 MM [FRONT END PROCESSES]

Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material. Historical trends suggest that the next generation is 450 mm in diameter and currently is projected to be in production in year 2012. Though worldwide discussions have already started, it should be emphasized that development efforts on 450 mm wafers would need to be substantially accelerated from the present levels. Enhanced coordination will also be required amongst Starting Materials, Factory Integration, Yield Enhancement TWGs and the IRC to more effectively assess the anticipated onset of 450 mm use.

CHEMICAL AND MATERIAL MANAGEMENT BY ESH DESIGN AND MEASUREMENT METHODS [ESH]

Equipment design engineers and equipment users require timely information regarding ESH characteristics of potential new process chemicals and materials. This information is essential to the proper selection of optimal chemicals and materials for function and ESH impact with respect to reaction product emissions, health and safety properties, compatibility of materials with equipment and other chemical components, flammability, and reactivity. It must be possible to do so while minimizing unnecessary impacts on business after processes are developed and are in production. For integrated ESH design and measurement methods, a methodology for determining the lowest ESH impact of materials and processes needs to be developed.

PROCESS STABILITY VERSUS ABSOLUTE CONTAMINATION LEVEL INCLUDING THE CORRELATION TO YIELD [YIELD ENHANCEMENT]

Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determining required control limits. Energy-dispersive spectroscopy (EDS) of SEM is limited as an inline elemental analysis technique. Methodologies for employment and correlation of fluid/gas types to yield of a standard test structure/product, and the correlation of different contaminants to wafer yield to define a standard test for yield/parametric effect and definition of maximum process variation (control limits) are important.

INLINE DEFECT CHARACTERIZATION AND ANALYSIS [YIELD ENHANCEMENT]

Inline elemental analysis techniques are required as an alternative to energy-dispersive X-ray (EDX) analysis systems. The focus of required development is on light elements, small amount of samples due to shrinking particle size, and increasing importance of microanalysis. SEM/EDS is limited as an inline elemental analysis technique. This is due to several reasons as follows: 1) EDS is not a small volume technique for our desired scale; 2) EDS supplies insufficient chemistry information (for example, the lack of chemical state information), and 3) EDS causes e-beam damage as the insulating substrate can cause severe charging, which results in the destruction of the SEM image resolution and makes it difficult to know if the beam is actually on the particle. This grand challenge is a crosscut of yield enhancement and metrology issues.

NON-DESTRUCTIVE PRODUCTION MEASUREMENTS [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures and defect detection is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. The combination of high-resolution optics, waveform analysis, and non-charging technique enables precise grasp of 3D structures for both CD measurement and defect detection. At the same time, CD-SEM must be calibrated by scanning probe microscopy for reliable and stable measurement.

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Increasingly, new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This is required especially for gate stacks and interconnect structures. Modeling related to reliability and process variations is needed. In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Furthermore, computational material science needs to be developed and applied to contribute to the assessment and selection of new materials in order to reduce experiment effort. This Grand Challenge crosscuts more of the difficult challenges in the Modeling and Simulation chapter.

WHAT IS NEW FOR 2005—THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS

WHAT'S NEW?

The overall strategy for System Drivers is composed on three principles derived from industry trends. First, the Drivers must be gradually aligned in the long term with the major market drivers for the semiconductor industry. Second, when possible these drivers should match the market drivers for related worldwide roadmaps such as iNEMI (e.g., consumer, office, medical, etc.). Third, the alignment should not eliminate "fabric" drivers (components used to build each of the market-driver chips) that drive technology, such as embedded memory or analog/mixed-signal. Based on these principles, the 2005 System Drivers chapter has two important changes and various revisions with respect to the 2004 Update.

The first change is the alignment of the product market segments table with the major industry drivers featured in major roadmaps like iNEMI. As a result, the first table in the chapter has changed and the new version is shown below. The segments considered include portable/consumer, office, medical, networking/communications, defense, and automotive. Over the next years, focus will be put on completely aligning the rest of the chapter to these drivers. As of the 2005 version, more than a third of the chapter is aligned with these drivers.

The second change is the introduction of a new driver called "SoC-PE" (Power Efficient System-on-Chip) to replace the "SoC-PDA" driver to represent the critical portable consumer segment. This driver provides insights in medium and long-term challenges in areas such as power consumption, productivity, and the number of architectural elements (which has implications of software productivity as well), and uses a architectural template that attempts to reflects industry trends accurately.

Various sections of the *System Drivers chapter* (and its tables) have also been revised to provide a more up-to-date picture, including the analog/mixed-signal driver and the embedded memory driver.

Table ITWG 1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 mos 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important. Recent advances in multi-core processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 yrs. 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions
IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 mos 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multi-core processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts High speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog Simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-pos resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems. Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software.	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning). MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D /A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f— intermediate frequency I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplex RTOS—real-time operating system

DESIGN

WHAT'S NEW?

The Design chapter includes three important highlights with respect to the previous roadmap version: the creation of a quantified roadmap version; the introduction of substantial content in the emerging field of design for manufacturability, and the introduction of a new overall challenges table.

By far the most important highlight is the quantified roadmap. The chapter has effectively gone through a major overhaul in its 2005 version. The overall strategy is based on providing a comprehensive, quantitative design technology roadmap including requirements and solutions tables that resemble the ones found in the other roadmap chapters. As a result, the 2005 ITRS *Design chapter* features the first worldwide quantitative design technology roadmap. Challenges, requirement metrics, and solution tables are aligned on a design step basis, including electronic system-level design, logic/circuit/physical design, design verification, design for test, and design for manufacturability. Ten new requirements and solutions tables describe the new roadmap.

A new section on the emerging challenges in Design For Manufacturability section was introduced in the 2004 Update and has been permanently established, including its standard roadmap tables, in the 2005 Roadmap. A multi-level variability framework has been developed as a model to understand and quantify the relationships between design technology roadmap items and manufacturing-related items in the rest of the roadmap chapters, including PIDS and others.

Finally, a new table for overall grand challenges in design technology, shown below, has been established in the 2005 roadmap version. The table describes the five grand design technology challenges—design productivity, power consumption, manufacturability, reliability, and interference—and provides details in the form of a list of requirements for each challenge (rightmost column). The most important of these five challenges (productivity as an overall "meta-challenge," and power consumption and manufacturability as the two critical challenges) appear explicitly in the Overall Technology Roadmap Characteristics. These requirements shown in the rightmost column correspond to the actual roadmap tables found later in the chapter for each design step (electronic system-level design, logic/circuit/physical design, design verification, design for test, and design for manufacturability).

DIFFICULT CHALLENGES

Table ITWG 2 Overall Design Technology Challenges

Challenges ≥32 nm	*Summary of Issues*
Design productivity	System level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent testbench, coverage-based verification Logic/circuit/layout: analog circuit synthesis, multi-objective optimization
Power consumption	Logic/circuit/layout: dynamic and static (leakage), system and circuit, power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/layout: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/layout: signal integrity analysis, EMI analysis, thermal analysis
Challenges <32 nm	*Summary of Issues*
Design productivity	Complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static-logic, and emerging devices Cost-driven design flow Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	SOI power management
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test EMI— electromagnetic interference ESL— Electronic System-level Design HW/SW—hardware/software MTTF—mean time to failure SOI—silicon on insulator

TEST AND TEST EQUIPMENT

WHAT'S NEW?

The 2005 Test roadmap has undergone substantial evolution since the 2003 edition. Most significant is the reorganization of the Test Technology Requirements section to better reflect the reality of increasing integration of previously disparate chip designs. Looking forward over the ITRS horizon, each device under test (DUT) could be considered a system-on-a-chip (SOC) or system-in-package (SIP) containing one or more of the following "cores": logic, IO, memory, analog, RF, etc., each with unique test requirements. The revamped Test Technology Requirements section opens with an overview of these SOC/SIP test challenges including the introduction of a generic SOC model and continues with sections dedicated to the test requirements and challenges for each type of core.

Beginning with this 2005 edition of the ITRS Test chapter, we have also reorganized the Difficult Challenges section of the test chapter. The key change is to split the previous Difficult Challenges section into Key Drivers and Difficult Challenges, as well as add a Future Opportunities section. This split will distinguish the drivers, i.e., primary boundary conditions that define the scope of solutions for upcoming manufacturing test for semiconductor components, from key technical and business challenges. At a high level, these boundary conditions actually represent expectations or even requirements of the test process, while the challenges represent current and upcoming key roadblocks, strategic inflection points, and opportunities for the future

For many years, the mission of semiconductor manufacturing test has been described as "screening defects" and to a lesser extent or within certain business segments "speed binning" or "speed classification." It is interesting to note that some of the most important test challenges are now actually centered on some of the more subtle historical missions of manufacturing test—reliability and yield learning. It is also important to note that the impact of these challenges affect not only on the manufacturing test process itself, but are essential to entire semiconductor business, both in terms of enabling the cadence or timely delivery of future processes and cost-effective products, but also in terms of meeting customer expectations for reliability.

DIFFICULT CHALLENGES

Within the Difficult Challenges section, the challenges are listed in order of perceived importance or priority; for example, test for yield learning followed by screening for reliability followed by increasing systemic defects. In contrast, there is no specific intent in the ordering of the Key Drivers, whereas they are all boundary conditions or requirements that the semiconductor test solutions must meet. Table ITWG3 summarizes all of the key test drivers, challenges and opportunities. Each is expounded upon in greater detail within the *Test and Test Equipment chapter*.

Table ITWG 3 Summary of Key Test Drivers, Challenges and Opportunities

KEY DRIVERS (NOT IN ANY PARTICULAR ORDER)	
Device trends	• Increasing device interface bandwidth (both number of signals and signal data rates) • Increasing device integration (SOC, SIP, MCP, 3D packaging) • Integration of emerging and non-digital CMOS technologies (RF, Analog, Optical, MEMs) • Package form factor and electrical / mechanical characteristics • Device characteristics beyond one sided deterministic stimulus/response model
Increasing test process complexity	• Increased device customization and line item complexity during the test process • Increasing "distributed test" to maintain cost scaling • Increased data feedback for tuning manufacturing • Higher order dimensionality of test conditions (e.g., adding multi-power, multi-voltage, multi-freq topologies to single valued T, V, freq)
Continued economic scaling of test	• Physical limits of further test parallelism • Managing (logic) test data volume • Effective limit for speed difference of HVM ATE versus DUT • Acceptable increases for interface hardware and (test) socket costs • Trade-off between the cost of test and the cost of quality
DIFFICULT CHALLENGES (IN ORDER OF PRIORITY)	
Test for yield learning	• Critically essential for fab process and device learning below optical device dimensions
Screening for reliability	• Increasing implementation challenges and efficacies of burn-in, IDDQ, and Vstress • Erratic, non deterministic, and intermittent device behavior
Increasing systemic defects	• Testing for local non-uniformities, not just hard defects • Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Potential yield losses	• Tester inaccuracies (timing, voltage, current, temperature control, etc) • Overtesting (e.g., delay faults on non-functional paths) • Mechanical damage during the testing process • Defects occurring in test-only circuitry, e.g., BIST • Some IDDQ-only failures • Faulty repairs of normally repairable circuits • Overly aggressive statistical post-processing
FUTURE OPPORTUNITIES (NOT IN ANY ORDER)	
Test program automation (not ATPG)	Automation of generation entire test programs for ATEs
Simulation and modeling	Simulation and modeling of test interface hardware and instrumentation seamlessly integrated to the device design process
Convergence of test and system reliability solutions	Re-use and fungability of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES AND STRUCTURES

WHAT'S NEW?

Compared to the previous versions, improved MOSFET modeling software is used in the 2005 ITRS *Process Integration, Devices, and Structures chapter* to generate the transistor parameters in the Logic Technology Requirements tables. For these tables, in previous editions of the ITRS, planar bulk MOSFETs were utilized initially, but these were eventually replaced by ultra-thin body fully depleted (UTB FD) silicon-on-insulator (SOI) MOSFETs, which in turn were replaced by multiple-gate MOSFETs. In the 2005 ITRS, planar bulk CMOS is extended as long as possible, while UTB FD SOI MOSFETs and multiple-gate MOSFETs are implemented in 2008 or later and run in parallel with the extended planar bulk CMOS. This multiple parallel path scenario was adopted because it reflects a more realistic scenario, in which some companies will choose to extend planar bulk CMOS as long as possible, while others will choose to switch to UTB FD SOI and multiple-gate MOSFETs sooner. Another important change is that both high-κ gate dielectric and metal gate electrodes are projected in 2008 for both high-performance and low-power logic. In the 2003 edition, high-κ gate dielectric was projected in 2006 for low standby power logic and in 2007 for high-performance and low operating power logic, and metal gate electrodes were projected for later years for all types of logic. Finally, for non-volatile memory, phase change random access memory (PC RAM) has been added in the 2005 ITRS because this type of memory is apparently approaching mainstream production in several years.

DIFFICULT CHALLENGES

Table ITWG 4 Process Integration Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 32 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), stochastic doping variations, and difficulty in adequately controlling short channel effects. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs.
2. Implementation of high-κ gate dielectric and metal gate electrode in a timely manner	High κ and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work function, ensuring adequate channel mobility with high-κ, reducing the defects in high-κ to acceptable levels, ensuring reliability, and others.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple changes are projected over the next decade, such as.: Material: high-κ gate dielectric, metal gate electrodes by 2008 or so Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, followed by multiple-gate structures. It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.
4. Scaling of DRAM and SRAM to the 32 nm technology generation	DRAM main issues with scaling—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. Also, reducing the cell area factor in a timely manner is quite challenging. (Cell area factor = a = cell area/F^2, where F=DRAM half pitch). SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities and soft error rate with scaling. Also, difficult lithography and etch issues with scaling.
5. Scaling high-density non-volatile memory to the 32 nm technology generation	Flash—Non-scalability of tunnel dielectric and interpoly dielectric. Dielectric material properties and dimensional control are key issues. FeRAM—Continued scaling of stack capacitor is quite challenging. Eventually, continued scaling in 1T1C configuration. Sensitivity to IC processing temperatures and conditions. SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions

Table ITWG 4 Process Integration Difficult Challenges (continued)

Difficult Challenges<32 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to effectively scale MOSFETs to 11 nm gate length and below. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-11 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc,) are currently unclear. For detail, refer to ITRS Interconnect chapter.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate physically or functionally into a CMOS platform. Such integration may be difficult. See Emerging Research Devices sections for more discussion and detail.

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

WHAT'S NEW?

Radio frequency and analog/mixed-signal (RF and AMS) technologies now represent essential and critical technologies for the success of many semiconductor products. Such technologies serve the rapidly growing wireless communications market. They depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe, and others of which are not compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table. Recognizing wireless applications, which are enabled by RF and AMS technologies, as a new system driver for the ITRS, the International Roadmap Committee (IRC) requested in 2003 that III-V compound semiconductor devices be included in the roadmap.

The purposes of the 2005 ITRS *RF and AMS chapter* are:

1) Present the challenges that RF and AMS technologies have in meeting the demands of wireless applications for cellular phones, wireless local area networks, wireless personal area networks (PAN), phased array RF systems, and other emerging wireless communication, radar, and imaging applications operating between 0.8 GHz and 100 GHz.

2) Address the intersection of CMOS, BiCMOS, and SiGe heterojunction bipolar transistors (HBTs) with III-V compound semiconductor devices.

The RF and AMS Working Group is organized into five sub-groups:
1) RF and AMS CMOS (0.8 GHz–10 GHz),
2) RF and AMS Bipolar Devices (0.8 GHz–10 GHz),
3) Power Amplifiers (0.8 GHz–10 GHz),
4) Passive for RF and Analog (0.8 GHz–10 GHz), and
5) Millimeter Wave (10 GHz–100 GHz).

The RF and AMS chapter presents the challenges, technical requirements, and potential solutions that RF and AMS technologies have in meeting the demands of wireless applications. The technology requirements for meeting the demands of wireless systems are manifold, often conflicting and very different from digital requirements. Thus we often see today in wireless systems a combination of specialized analog and RF technologies such as Si CMOS, SiGe, Si BiCMOS, Si LDMOS, GaAs MESFET, GaAs PEMT, GaAs HBT, InP HEMT, and InP HBT.

Cost and performance drive integration. Depending on requirements either monolithic system on chip (SoC) or system in package (SiP) integration may be preferred. When required, the SiP approach is especially suited to bring the specialized RF and AMS technologies together in a highly integrated, high-performance unit.

In addition to the five sections mentioned above, the RF and AMS chapter discusses the increasing significance of signal isolation. As wireless communications systems migrate to support more multi-mode, multi-in/multi-out radio functions, maintaining signal isolation among radio functions and digital baseband functions becomes a very demanding and critical challenge. However, unlike other technologies discussed in the RF and AMS chapter, there are at present no clear definitions and figures of merit for signal isolation performance. Consequently, for the 2005 ITRS there are no technology requirement tables for signal isolation. The 2005 chapter attempts to highlight the importance and the need for more attention to the challenges of signal isolation.

DIFFICULT CHALLENGES

Table ITWG 5 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
Signal isolation	Obstacle preventing full system-on-chip (SoC) implementation because of the exceedingly high RF voltage created by the power amplifier and the power management circuits and the numerous frequencies generated internally by the intermediate frequency (IF) blocks; must be carefully managed to prevent performance degradation as wireless communication schemes become more complicated; progress is limited because a consensus does not exist on appropriate metrics for assessing the progress of signal isolation in the context of the RF and AMS roadmap.
High-performance and low-cost RF and analog/mixed-signal solutions: CMOS compatible semiconductors	Optimizing RF/analog CMOS devices with scaled technologies: mismatch, 1/f noise, voltage gain and leakage with high-κ gate dielectrics Fundamental changes in CMOS device structure to FDSOI or dual-gate devices may lead to the need for separate process steps to fabricate conventional precision analog/RF drive devices, resistors, and varactors Reduced power supply voltages: degradation in SNR and signal distortion performance Cost and integration complexity of integrating bipolar device in aggressively scaled CMOS generation s (such as conflicting thermal budgets) Cost and performance tradeoffs associated with integrating passive devices in scaled CMOS (additional processing steps, silicon area, and need for new materials) High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications
High-performance and low-cost RF and analog/mixed-signal solutions: III-V Compound semiconductors	Substrates with good thermal dissipation and process equipment for fabrication at low cost Compound semiconductor substrate quality, especially for SiC and GaN Larger size compound semiconductor substrates [GaAs, SiC, GaN, and InP] for lower chip costs and compatibility with silicon processing equipment Engineering to relieve stresses in heteroepitaxy, e.g., epitaxial layers in compound semiconductors
Cost effective CAD and design tools	Non-linear and 3D Electromagnetic models for accurate design and simulation CAD solution for integrated radio SIP design (chip, passive, component, package, tool compatibility, and model accuracies) Accurate, fast, and predictive analog and RF compact models. Computationally efficient physical models for compound semiconductors Efficient 3D modeling and simulation for mixed signal circuits. Thermal modeling and simulations that are integrated with RF and digital design tools.
Fast and low cost verification of RF performance	RF/analog/digital tests for SoC systems Reduced RF circuit final tests

RF and AMS CMOS (0.8 GHz–10 GHz): Two major changes in the taxonomy for the technology requirements tables were made. The categories of High-Speed Analog CMOS and RF CMOS were combined in a new category called Performance Analog/RF and the categories of Precision Analog CMOS and Driver CMOS were combined in a new category called Precision Analog/Driver. The Performance Analog CMOS table now is based on LSTP CMOS with a one-year lag. Higher integration and performance levels for logic with mixed-signal circuitry have continued with the following results: 1) Steadily increasing digital processing capabilities enables more signal processing to be done in the digital domain; 2) The F_t and F_{max} of devices have increased along with reduced RF noise; 3) A second or a third I/O-transistor gate oxide is used to optimize performance at higher voltages, to continue to support interfaces to the outside world, and to maintain the high signal-to-noise requirements for mixed-signal applications; 4) Multiple threshold voltages enable optimization of digital power-delay and offer design options for mixed-signal and RF applications; and 5) Reduced power levels for digital, RF, and analog functions.

RF and AMS Bipolar Devices (0.8 GHz–10 GHz): This sub-group now covers bipolar devices at moderate frequencies less than 10 GHz and power less than 0.5 W. There is some unavoidable overlap with high-speed bipolar devices in the mm-Wave table and with high voltage bipolar devices in the Power Amplifier table. The key driving forces include speed, power consumption, noise, and breakdown. The Bipolar Technology Requirements table was separated into three sub-areas: 1) High speed bipolar devices, 2) RF to include most typical bipolar devices used for wireless, and 3) High voltage bipolar devices that were in the 2004 Power Amplifier (PA) table. Silicon (SiGe) bipolar devices are included, but III-V HBTs are not included in this table. They are included in the Power Amplifier table. Major changes from the

2004 tables are: 1) Added $F_t/F_{max}/BV_{ceo}$ for all device types, 2) Removed power supply requirements because they are more meaningful for CMOS, and 3) Added current density at peak F_t for high-speed devices.

Power Amplifiers (0.8 GHz–10 GHz): For 2005, passive devices were removed from the 2004 PA table and incorporated into a separate Passives table. The PA device evolution is slow due to nearly fixed battery voltages and ruggedness requirements. The 2004 predictions for battery voltage reduction from 3.4 V were not realized. Battery technology will remain at the same voltage through the next two to three years. SiGe multiband cellular PAs are being sampled but they are not yet present in any significant volumes. CMOS PAs are being discussed and sampled but demonstrations of viable and rugged PAs are still not published. Highly integrated modules with multi-layer laminates/LTCC are dramatically reducing total RF front-end area. PA potential solutions show silicon integration enablers for PA integration into system chips with a focus on SOI and high resistance substrates and above-IC RF MEMS technology.

Passive Devices for RF and Analog (0.8 GHz–10 GHz): No major changes are expected for the component parameters. The table for 2005 is separated into three parts: 1) Analog—for low frequency analog/mixed signal applications. This includes MOS capacitors and resistors (thin film BEOL and polysilicon resistor). The MOS capacitor roadmap is based on the CMOS roadmap for precision device gate T_{ox}. As CMOS is scaled, an extra polysilicon resistor mask may be required. 2) RF applications that include metal-insulator-metal (MIM) capacitors, inductors, and MOS varactors. The MIM density is expected to meet all near-term requirements (voltage linearity, leakage, matching and Q). 3) PA applications that remain mainly unchanged.

Millimeter Wave (10 GHz–100 GHz): As in previous years, projections are taken out only to the near term [~2013] because the compound semiconductor industry does not have the decades of history from which to extrapolate as does the silicon industry and because it is smaller, less mature, and has lower investment than the silicon industry. Main trends are: 1) Gate dimensions are not shrinking as fast as predicted in the 2003 and 2004 roadmaps. The 70 nm gate technology is not expected to be in production until the 2007 time frame. Advances in performance are tied more to materials and device technologies (e.g., higher performance MHEMTs at the same lithographic dimensions as PHEMTs). 2) Some technologies may become obsolete during this decade. For example, low noise GaAs MESFETs are expected to have no new designs beyond 2006 because foundries are only likely to produce for legacy products and end of life buys. The same trends also apply to low voltage power MESFETs. PHEMTs and InP HEMTs may lose ground to MHEMTs late in the decade. 3) GaN is advancing much quicker than predicted in 2003 and 2004. Some parameters colored "red" for 2007 in the 2004 Update have already been demonstrated; but materials quality and device reliability are still issues for volume production.

EMERGING RESEARCH DEVICES

WHAT'S NEW?

The new 2005 *Emerging Research Devices (ERD) chapter* has been substantially changed and broadened compared to the ERD section in the 2003 edition. The section on non-classical CMOS, prominent in 2003, has been shifted to the PIDS and FEP chapters and a completely new section on Emerging Research Materials (ERM) has been added. Many emerging research devices will require materials with dramatically improved or new properties. To address this need, the Emerging Research Materials Working Group has identified the critical materials properties required for fabrication and operation of these new devices and potential materials solutions. Fabrication of many of these new materials may require new chemicals, synthesis techniques, and metrologies to characterize and improve their performance. This new emerging research materials section provides a comprehensive new treatment of these research needs and opportunities.

Also added are new sections discussing a taxonomy for nano-information processing and proposing a new set of fundamental guiding principles. The Taxonomy section is focused on an organization of generic information processing layers. The guiding principles are intended to bring the perspective of fundamental requirements to the many new and quite different approaches proposed to scale of information processing by orders of magnitude beyond that attainable with ultimately scaled CMOS. Furthermore, a new critical analysis has been performed evaluating the potential performance o the emerging research memory and logic technologies as they mature. Again in 2005, two emerging memory technologies (Nano Floating Gate Memory and Engineered Tunnel Barrier Memory) are seen to offer attractive performance advantages compared to similar commercially available memory technologies. Conversely, the realm of emerging research logic technologies that offer significant performance advantages compared to CMOS requires continued discovery research to identify promising new approaches. The possible exceptions to this perspective are 1 dimensional structures such as nanowires and nanotubes applied to FET-like structures. Additionally, the tables in the research Memory and Logic sections have been substantially improved, and the Memory section now includes a greatly expanded baseline memory table and a new prototypical memory table. The Baseline Memory table now includes both stand-alone and embedded DRAM, SRAM, and both NAND and NOR FLASH. The new Prototypical Memories table includes SONOS, FeRAM, MRAM, and PCM (Phase Change Memory). The Memory and Logic sections also each contain a new "Transition" table. These Transition tables indicate which new technologies have been included and those included in the 2003 edition that have been transferred to PIDS and FEP or have been dropped.

DIFFICULT CHALLENGES

Table ITWG 6 Emerging Research Device Technologies Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Development and implementation into manufacturing of a non-volatile memory technology, scalable beyond 32 nm, combining the best performance features of both volatile and non-volatile memory technologies for both stand-alone and embedded applications.	Identification of the most promising technical approach (es) to obtain electrically accessible, high-speed, high-density, low-power, non-volatile RAM Development of a manufacturable, cost-effective fabrication technology integrable with the process flow for CMOS logic providing for seamless integration onto a CMOS platform
Difficult Challenges < 32 nm	
Toward the maturation of CMOS scaling or beyond, discovery, reduction to practice, and implementation into manufacturing of novel, non-CMOS devices and architectures integrable (monolithically, mechanically, or functionally) with a CMOS platform technology 1D to extend charge based devices Articulate the fundamental physical principles needed to develop new device technologies. Find a new information processing technology that addresses these fundamental principles (see Section entitled "Fundamental Guiding Principles") Make emerging logic and memory devices compatible. (A new logic technology may require a new compatible memory technology.) Integrate the materials, device and architectural communities to interact and collaborate in discovering a new information processing technology.	No current approaches support the information processing technology required for "Beyond CMOS" satisfying the need for additional decades of functional scaling. Discovery and reduction to practice of new, low-cost methods of manufacturing novel information processing technologies Any new technology for information processing must be compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A knowledge gap exists between materials behaviors and device functions. Current metrologies examine fixed material states, but do not probe the state change dynamics.

FRONT END PROCESSES

WHAT'S NEW?

The *Front End Processes chapter* attempts to identify the challenges and potential solutions to "materials-limited device scaling." During the next several years front-end processes will require the introduction of a variety of high-κ materials and highly-engineered metal films for applications as diverse as MOSFET gate stacks, DRAM storage capacitors, and flash-memory storage devices. In addition to these new materials, new device structures, such as fully depleted silicon-on-insulator (FDSOI) and FinFET (including dual- and multi-gate), will be introduced in order to meet performance requirements. Market growth for alternative memories will also require the development and optimization of a broad class of ferroelectric, magnetic, and phase-change thin film materials. Underlying these device changes are rapidly evolving requirements for substrates, such as SOI, and the need for an even larger, 450 mm diameter substrate, within the next seven years.

The transition from extended bulk CMOS to non-classical device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time—some manufacturers choosing to make the transition to non-classical devices earlier, while others emphasize extensions of bulk technology. To support this probable scenario we have provided metrics for parallel paths showing what is required to extend classical CMOS and what can be gained by making a transition to other device structures such as fully depleted SOI and multi-gate. The FEP tables have been lengthened to accommodate entries for extended bulk, FDSOI, and multi-gate devices during years when those technologies are expected to overlap. The requirements for these parallel paths are intended to illustrate some of the trade-offs associated with each alternative technology. For example, bulk CMOS extensions will require more aggressive scaling of gate dielectric thickness and junction depth, while requiring lower resistance contacts. On the other hand, FDSOI and multi-gate devices need gate electrode materials whose work functions are different than those used in bulk CMOS.

Silicon wafer trends, addressed in the FEP Starting Materials section, include several changes that deal with scaling, yield enhancement, and productivity improvements. Edge exclusion has been reduced from 2 mm to 1.5 mm at the 65 nm technology generation for consistency with the Factory Integration TWG direction. This generally poses broad challenges for all FEP sub-TWGs, including the starting wafer. This is particularly difficult for SOI wafers, where the thin silicon layer does not extend all the way to the edge of the substrate wafer, and subsequently leads to the creation of a separate edge exclusion table entry in the SOI section. In the nearer term, silicon thickness values for fully depleted (FD) SOI structures were scaled downward to be consistent with the latest PIDs device requirements. Long-term, manufacturing and controlling the thickness of FD SOI layers were previously identified as having no known solutions and, as a result of further scaling, face even greater challenges. The need to reduce front-surface particles and their size has accelerated, with 65 nm particles now appearing at the 50 nm technology generation and 45 nm particles occurring at the 32 nm technology generation. The wafer diameter title in the tables was changed to the maximum substrate diameter to match the terminology used in the ORTC Lithographic-Field and Wafer-Size Trends Tables. This also appears to more accurately reflect the existence of multiple wafer diameters that indeed are used for device production at a given technology generation. Finally, an extensive section on Emerging Materials trends and opportunities is presented in the Starting Materials section of the FEP chapter via a hyperlink.

With the advent of new materials and integration schemes, surface preparation at 90 nm and beyond is far more challenging than just cleaning the wafer. The formation of the gate dielectric and electrode demand the tightest control of parameters associated with critical cleaning. The ability to remove particles smaller than half the DRAM M1 ½-pitch without damaging the wafer is a formable challenge. Maintaining high cleaning efficiency while removing less than 0.4Å of material and without damage to 23 nm wide gate structures will present a major challenge as early as 2008. Concurrently, metallic contamination must be reduced to or maintained at levels that do not affect device performance. Other critical areas are the removal of high-dose implanted photoresist, cleaning and drying high aspect ratio features such as contacts and capacitor structures, as well as cleaning fine features, such as polysilicon lines, without damage. To address these challenges new cleaning techniques, equipment, and chemicals are required. In addition, the influence of back-surface particles on yield and the need for back-surface particle removal continue to receive a lot of attention. New back surface defect metrology tools should bring a better understanding of this area in the next few years.

Scaling of the equivalent oxide thickness of the gate dielectric remains a key FEP challenge. However, the need for high-κ dielectrics was moved out one year, to 2008, from the last edition of the ITRS, by a combination of more aggressively scaling of junction depths and the use of strain to enhance channel mobility. The 2005 roadmap also brings an increased realization that in the longer-term; gate dielectric leakage needs to be capped at lower values than previously anticipated. In the near term, approaches to minimize Poly-Si depletion become increasingly important. The

methodology used for defining and displaying the equivalent oxide thickness (EOT) of the gate dielectric changed in 2005 to better reflect the effect of gate depletion. In both the 2003 and 2005 editions of the ITRS, the gate stack (dielectric plus electrode) requirements originated from the electrical equivalent thickness in the PIDS device designs. The capacitance (electrical) equivalent thickness (CET) includes not only the EOT but also gate depletion and the effect of quantization in the channel. These later two effects were more accurately calculated for the 2005 roadmap, and EOT requirements were tabulated for several Poly-Si gate doping levels including: ($1 \times 10^{20}/cm^3$ – light doping, $1.5 \times 10^{20}/cm^3$ – nominal doping and $3 \times 10^{20}/cm^3$ – aggressive doping) and for metal gates, having no depletion.

Series resistance of contacts and junctions takes on increased importance in the 2005 ITRS for several reasons. Shallower junctions are projected in the near term to help delay the need for high-κ gate dielectrics. Intermediate term, bulk CMOS extensions require very aggressive scaling to control short channel effects. Fully depleted SOI devices and FinFETs require selective deposition of elevated junctions to even be able to make contacts. As a consequence, there are no good solutions to the series resistance challenge over large portions of the Roadmap.

Control of the physical gate length continues to be a difficult challenge for FEP and for Lithography. A survey revealed that manufacturers were almost universally unable to control the CD to within 10% (3σ), as prescribed in the 2003 ITRS. Pathways around this potential barrier were found by continuous discussions between the FEP, PIDS, Lithography, and Design groups. As a result of this collaboration, changes were made across several chapters of the ITRS, based on the recognition that devices can be economically manufactured with slightly higher variation than previously prescribed. Accordingly, the CD tolerance increased to 12% (3σ) in 2005; and analysis is ongoing to see if the tolerance can be further relaxed, e.g., to 15% in the future. Although the final MPU physical gate lengths remain unchanged from the values in the 2003 ITRS, the printed dimensions were made larger while the amount of resist trimmed away was increased. Along with this change, the partitioning of the total CD tolerance components was changed to 75% to lithography and 25% to etch, from the 80%/20% split in the 2003 ITRS. At the same time, evidence is growing that perhaps the industry is actually using slightly larger physical gate lengths than those in the ITRS. The evidence is not strong enough to warrant a change in the numbers in 2005, but if a trend is discerned, the physical gate lengths values may be revised upwards at the next revision.

For the DRAM stacked capacitor, MIM structures with high-κ dielectric are now required to meet capacitance requirements. Beyond 50 nm (2009) a new dielectric material with dielectric constant greater than 60 will be required. Embedded DRAM in SOC applications will drive several integration challenges. One of those challenges is matching the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic device. The need for advanced capacitor materials in the DRAM trench capacitor are delayed relative to the stacked capacitor by only a few years. Some high-κ materials are currently being used in an SIS structure for trench capacitors, but a metal top electrode will be needed by 2007 and a full MIM structure with high-κ dielectric may be needed by 2009. The cell size factor for the DRAM stacked capacitor is 6, while that for the DRAM trench capacitor remains at 8. Novel cell concepts for the trench capacitor, relying on the replacement of the conventional planar transfer device by 3-dimensional array transistor structures, are envisaged for 65 nm in order to alleviate device-scaling issues.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash-memory is becoming a new technology driver for both critical dimension scaling and material technology. The effective dimension, F, of Flash NAND devices now appears to lead the DRAM half pitch. As the space between adjacent Poly-Si gates shrinks, however, it will no longer be feasible for the control gate poly-Si to overlap the sides of the floating gate. Thus, by 2010 high-κ interlayer dielectrics will be required in order to maintain an acceptable capacitance-coupling ratio. In that same year ferroelectric RAMs (FeRAMs) are projected to need 3D capacitors to provide a charge storage that is competitive with DRAM (~ 30 $\mu C/cm^2$).

The introduction of 450 mm wafers in the FEP Starting Material's tables has been pulled in from 2015 and now appears in 2012, consistent with the direction from the ORTC. Motivation for the newly indicated timing is driven chiefly by productivity enhancements suitable for keeping pace with Moore's Law. Migration to the next diameter wafer has historically been occurring roughly on a 9–11 year cycle. Accordingly, this means that to meet the newly stated timing, the industry is already several years behind schedule. Furthermore, a number of highly-coordinated actions, such as setting standards, need to occur before any actual product/equipment development can be initiated. In contradistinction to even the 300 mm transition, which mainly focused on economic issues, the transition to 450 mm faces both enormous technical challenges and economic risk.

Initially, the industry must adopt numerous inter-related standards, involving wafers, metrology, and processing equipment. One key starting issue is whether 450 mm wafers will be SOI or bulk, since the proposed timing of 450 mm is likely to correspond with a broader adoption of SOI within mainstream IC production, particularly for high performance

logic/MPU applications. Certainly the wafer type (polished, epi, annealed, or SOI) drives standards, metrology, and processing. While unparalleled progress was made in the standardization of 300 mm wafers, the 450 mm effort will call for an even more efficient approach, particularly to reduce the length of time required from initiation to completion of standards, to avoid costly and time-consuming iterations. Specific attention must be paid to materials strength considerations of the silicon wafer, both during production and device processing and, therefore, calls for a more careful determination of the wafer thickness during global standards considerations. Indeed, there already are indications that some IDMs are using thinner 300 mm starting wafers so as to reduce the amount of backside grinding needed to ensure IC chips fit into advanced packages. Wafer characteristics consistent with the lithography used in the respective technology generation must be determined, clearly a non-trivial task. Concurrent with the development of global standards, suppliers across the entire spectrum of materials and equipment must also address the technical challenges associated with wafer, metrology, and processing equipment development. With sufficient resources and collaborative planning between the IDMs and the supplier community, the technical challenges may be sufficiently overcome (in time), but at a cost not necessarily on par with past cost models.

The economic challenges of 450 mm are arguably more daunting than the myriad technical ones. The cost of migration from 300 mm to 450 mm is estimated to be several tens of billions dollars, at a minimum. Indeed, one recently published cost of developing 450 mm processing equipment was in excess of $100 billon, although that frankly does seem somewhat excessive.[2] Device, materials, and processing companies will all need to allocate significant resources to this end, especially those related to material properties, equipment interfaces, and equipment software. Given the magnitude of these costs, many IDMs likely will not be financially capable of affording 450 mm alone. This may lead to an increased number of consortia, joint manufacturing ventures, and contract manufacturing. Due to the enormous overall costs anticipated, perhaps the foremost pre-requisite of embarking on a 450 mm development program is a broad industrial coalition and commitment that includes an agreement on how to fund such costs and the timing of the transition. Given the scope of this undertaking, it will essentially mandate that IDMs provide significant financial backing to material and equipment suppliers in order to partially defray those costs and obtain a reasonable ROI for such suppliers and may even necessitate government funding. On the other hand, productivity alternatives related to design, such as multi-valued logic or innovative architecture, may be pursued by many others. In any case, one might consider that the extensive support required for the 450 mm conversion may take away required support for the continued improvement of 300 mm wafers, of especial concern for those IDMs not desiring to participate in the initial, or ever, 450 mm conversion.

Please refer to the FEP chapter, the Starting Materials section for a more detailed discussion of the issues associated with the migration to 450 mm.

[2] M. LaPedus,"Soaring Tool Costs to Delay 450mm Fabs," EE Times, August 19, 2005.

DIFFICULT CHALLENGES

Table ITWG 7 Front End Processes Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm EOT for high-performance MOSFETs, consistent with device reliability requirements
	Control of boron penetration from doped polysilicon gate electrodes while minimizing depletion of dual-doped polysilicon electrodes
	Introduction and process integration of high-κ gate stack materials and processes for high-performance, low operating and low standby power MOSFETs
	CMOS integration of enhanced channel mobility in both NMOS and PMOS devices, using local and global strained layers
	Introduction of dual metal gate electrodes with appropriate work function
	Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20–50 nm
	Removal of high-κ dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices
	Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is considerably smaller than the feature size printed in the resist, while maintaining <12% overall 3-sigma control of the combined lithography and etch processes
	Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns
	Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control
	Maintenance of CD and profile control throughout the transition to new gate stack materials and processes
	CD and etch metrology
	Site flatness to ensure effective lithographic printing
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers
	Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal
	Integration and scaling of FeRAM ferroelectric materials
	Scaling of Flash interpoly and tunnel dielectric layers may require high-κ
	Limited temperature stability of high-κ and ferroelectric materials challenges
	CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface
	Interface control for DRAM capacitor structures
	Maintenance of surface and interface integrity through full-flow CMOS processing
	Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
	Measurement of back surface particles at/near edge wafer edge (including bevel) has no solution
	Measurement and understanding of clustering of particles needs significant data to define future specification
	Little information associating back surface particles and the effect on yield
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance ($=V_{dd}/I_{on}$)
	Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect
	Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes
	Formation of continuous self-aligned silicide contacts over shallow source and drain regions. Formation of elevated junctions and silicides on FDSOI wafers
	Metrology issues associated with 2D dopant profiling

Table ITWG 7 Front End Processes Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Continued scaling of planar CMOS devices	Higher κ gate dielectric materials including temperature constraints Metal gate electrodes with appropriate work function Sheet resistance of clad junctions CD and L_{eff} control Chemical, electrical, and structural characterization
Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-κ materials and metal gates on standard CMOS) Selection and characterization of optimum device types CMOS integration with other devices, including planar MOSFETs Introduction, characterization, and production hardening of new FEP unit processes Device and FEP process metrology Increased funding of long term research Introduction of strained silicon in the structural configuration for advanced non-classical CMOS
Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2005	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon If 450 mm wafers are to become available for production in 2012 as currently forecasted, wafer manufacturing is already behind schedule and must be implemented in 2005–2006 Enhanced coordination is required amongst Starting Materials, Factory Integration, Yield Enhancement and the IRC to more effectively assess the anticipated onset of 450 mm use
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$ Further scaling of Flash memory interpoly and tunnel oxide thickness FeRAM storage cell scaling Introduction of new memory types and storage concepts (Candidates—MRAM, phase-change memory for 2010, and single electron, molecular, nano-floating products beyond 2010)
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

LITHOGRAPHY

WHAT'S NEW?

In 2005 and beyond, maintaining the rapid pace of half pitch reduction for each technology generation requires overcoming the challenge of improving and extending the incumbent optical projection lithography technology at 193 nm wavelength while simultaneously developing alternative, next generation lithography technologies to be used when optical projection lithography is no longer more economical than the alternatives. The 2005 *Lithography chapter* discusses significant technical challenges that exist in extending optical projection lithography at 193 nm wavelength using immersion lenses and also in developing novel next generation alternative approaches. Not only is it necessary to invent technical solutions to very challenging problems, it is critical that die costs remain economical with rising design costs, process development costs, mask costs, and cost of ownership of the tool and process.

Since the 2003 roadmap was published, working group members defined new criteria for evaluating near-term potential solutions for lithography. Solutions shown in the table for the present and next technology generations must address leading-edge requirements in at least two geographic regions, and all infrastructure including resist and mask must be ready for the timing of the technology. Solutions for three technology generations or more in the future are somewhat more inclusive to encourage continued innovation.

With these criteria, 193 nm wavelength exposure systems, including 193 nm immersion systems, became dominant solutions for the next two technology generations. Neither the use of 157 nm wavelength nor the use of electron beams in combination with masks [for example, electron projection lithography (EPL) or proximity electron lithography (PEL)] continue to be anticipated as potential solutions. Furthermore, immersion lithography appears as a potential solution at the 32 nm and 22 nm generations if high index fluids and lens materials are developed to extend the use of immersion beyond the limits of water-based immersion. The use of two masks per exposure field with each mask having patterns with half pitch two times larger than the primary half pitch may also help extend immersion lithography.

Extreme ultraviolet (EUV) lithography is the most probable potential solution for 32 nm and 22 nm half pitch with imprint and maskless lithography as other options along with innovative immersion. In the Difficult Challenges table, stronger emphasis was placed on challenges related to immersion lithography. More detail appears in the chapter describing resolution enhancement techniques and design for manufacturing with lithography friendly design rules. Continued emphasis was placed on challenges for implementing cost-effective post-optical lithography solutions, and more detail was added on the requirements for extreme ultraviolet (EUV), imprint, and maskless lithographies. A table describing the requirements for imprint templates was added.

Significant changes were made to overlay and CD control tolerances in this 2005 edition. Overlay tolerances have become more demanding to fabricate memory circuits with higher yield. To reduce the effect of lens distortion on overlay error, a single exposure tool may be used to print multiple critical layers for the same wafers. The Lithography working group has participated in discussions with working groups developing other chapters to define CD control requirements. The U.S.A. and Japan working groups separately conducted simulation studies that concluded that < 4 nm 3σ CD control has no known solutions with any technology presently being developed. Controlling critical dimensions to historically required ± 10% tolerances is becoming increasingly difficult.

Circuit design will need to take into account the collective capabilities of all processes that affect transistor performance. The Design TWG simulated circuit delay and power variability as a function of the most significant process and device variables. The simulations indicated that increasing the CD control requirement to ±12% would result in a tolerable variation of circuit delay and power variation given the significant variations of all of the significant parameters affecting these circuit attributes. Hence, the CD control requirement for MPU gates in the Roadmap has been increased from ± 10% to ± 12%.

The difference between the printed pattern width in resist from contacts and MPU gates has also been increased. Post development line width reduction techniques are becoming more prevalent and more capable, but a larger fraction of the root sum square CD error tolerance has been allocated to etch to account for the increasing effect of the etching process on physical gate length control. Printing larger features in resist improves CD control by providing for a larger process window for the lithography process. Because of the particular challenges associated with imaging contact holes, the size of contact holes after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gate length. The size of the bias achieved between the developed and etched contact holes have increased since 2003.

The effects of line edge and line width roughness (LWR) are also becoming increasingly apparent in device performance; therefore, metrology tools need to be modified to accurately measure these variations as well. High frequency line width roughness affects dopant concentration profiles and affects interconnect wire resistance. Line width roughness at larger

spatial frequency results in variations of transistor gate length over the active region of the device. This variation increases leakage of transistors and causes a variation of the speed of individual transistors, which in turn leads to IC timing issues. The definition of line width roughness has been refined and values of low frequency roughness have been established with the intent to establish high frequency values in the future.

DIFFICULT CHALLENGES

Table ITWG 8 Lithography Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD, and defect control for masks
	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Understanding polarization effects at the mask and effects of mask topography on imaging and optimizing mask structures to compensate for these effects
	Eliminating formation of progressive defects and haze during exposure
	Determining optimal mask magnification ratio for <45 nm half pitch patterning with 193 nm radiation and developing methods, such as stitching, to compensate for the potential use of smaller exposure fields
	Development of defect free 1× templates
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	Sufficient lifetime for exposure tool technologies
	Resources for developing multiple technologies at the same time
	ROI for small volume products
	Stages, overlay systems and resist coating equipment development for wafers with 450 mm diameter
Process control	Processes to control gate CDs to < 4 nm 3σ
	New and improved alignment and overlay control methods independent of technology option to <11 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 50 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Control of and correction for flare in exposure tool, especially for EUV lithography
	Lithography friendly design and design for manufacturing (DFM)
Immersion lithography	Control of defects caused in immersion environment, including bubbles and staining
	Resist chemistry compatibility with fluid or topcoat and development of topcoats
	Resists with index of refraction > 1.8
	Fluid with refractive index > 1.65 meeting viscosity, absorption, and fluid recycling requirements
	Lens materials with refractive index >1.65 meeting absorption and birefringence requirements for lens designs
EUV lithography	Low defect mask blanks, including defect inspection with < 30 nm sensitivity and blank repair
	Source power > 115 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Resist with < 3 nm 3σ LWR, < 10 mJ/cm^2 sensitivity and < 40 nm ½ pitch resolution
	Fabrication of optics with < 0.10 nm rms figure error and < 10% intrinsic flare
	Controlling optics contamination to achieve > five-year lifetime
	Protection of masks from defects without pellicles
	Mix and match with optical lithography

Table ITWG8 Lithography Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Mask fabrication	Defect-free masks, especially for 1× masks for imprint and EUVL mask blanks free of printable defects
	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair), especially for 1× masks
	Mask process control methods and yield enhancement
	Protection of EUV masks and imprint templates from defects without pellicles
	Phase shifting masks for EUV
Metrology and defect inspection	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3σ
	Metrology for achieving < 2.8 nm 3σ overlay error
	Defect inspection on patterned wafers for defects < 30 nm, especially for maskless lithography
	Die-to-database inspection of wafer patterns written with maskless lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective optical and post-optical masks
	Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products
Gate CD control improvements and process control	Development of processes to control gate CD < 1.3 nm 3σ with < 1.5 nm 3σ line width roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3σ overlay error, especially for imprint lithography
	Process control and design for low k_1 optical lithography
Resist materials	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Limits of chemically amplified resist sensitivity for < 32 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control

INTERCONNECT

WHAT'S NEW?

The 2005 ITRS *Interconnect chapter* has some significant changes from the 2004 Update.

- The definition of the MPU "Minimum Metal 1 contacted pitch" has been clarified as representing use of a staggered contact layout rather than the side-by-side contacts shown previously. Staggered contacts have long been the predominant industry design practice for MPUs.
- The 2005 Roadmap recognizes an acceleration of MPU product introduction to a two and a half-year cycle for the next two technology generations (2007 and 2009) and then reversion to a three-year cycle after 2009. In addition, the difference in pitch between the MPU metal 1 and intermediate wires also disappears by 2009.
- For quite some time the most aggressive Metal 1 pitch has been the utilized by DRAM; however, the latest roadmap projects that the Metal 1 pitch for MPU is projected to be equivalent to that of DRAM in 2010.
- For Logic, an updated model for the Cu resistivity increase from grain boundary and interface scattering is incorporated in the 2005 ITRS. The new model reflects data for Metal 1, intermediate and minimum global wires at a 1.7 A/R, which is more representative of MPU Cu wiring. The updated Cu resistivity numbers and the new more aggressive Metal 1, intermediate, and global wire pitches were used to calculate the RC delay for a 1 mm line length. For reference, the RC delay assuming no scattering in the Cu wire is also shown. By the year 2013, the RC delay for a minimum pitch global wire is more than 50% longer because of electron scattering.
- Three-dimensional control of critical dimension (3D CD) interconnect features has been listed as one of the critical challenges in several editions of the ITRS. The total variability of M1 wire resistance due to CD variation and scattering has been calculated and is also included in the MPU Technology Requirements table.
- As supply voltage is scaled or reduced, crosstalk has become an issue for all clock and signal wiring levels. A new crosstalk metric has been introduced in the 2005 ITRS for Metal 1, intermediate and global wires. The metric calculates the line length where 25% of the switching voltage is induced on a minimum pitch victim wire by two adjacent aggressor wires. This critical line length for a minimum global wire in 2020 is less than 30% of the line length in 2005. Therefore joint efforts with the design community are needed to address crosstalk issues.
- The low-κ portion of the Roadmap was changed very little with respect to the prior edition. Materials that deliver an effective κ in the range of 3.1–3.4 are in production today, and those material systems that will deliver an effective κ in the range of 2.7–3.0 are expected to be implanted in manufacturing by 2007. Simulations with a variety of assumptions for bulk dielectric, hard mask, etch stops, etc., have been used to calculate the range of effective κ values in the Roadmap and are shown in the Dielectric Potential Solutions Appendix of the Interconnect chapter.
- The proposed changes for DRAM are relatively minor. There are some changes to effective κ values especially in the long-term years. Cu wiring is expected to be introduced in 2007.
- In the Interconnect Surface Prep section, new requirements include improving interfacial adhesion, improving dielectric and barrier reliability, repairing etch damage, and sealing pores in dielectric sidewalls. The main focus in these tables is dual-damascene processing involving copper metal and low dielectric constant insulators.

In assessing the Interconnect roadmap as a whole, however, it still becomes almost entirely "red bricks" (red = "no known solution") by the end of this decade. No new discoveries or major breakthroughs have occurred in the year since closing the 2004 roadmap to change the outlook.

DIFFICULT CHALLENGES

Table ITWG 9 Interconnect Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 32 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*
CMP—chemical mechanical planarization DRAM—dynamic random access memory

FACTORY INTEGRATION

WHAT'S NEW?

The *Factory Integration chapter* of the ITRS focuses on integrating all the factory components needed to efficiently produce the right products in the right volumes on schedule while meeting cost targets. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, and other manufacturing productivity improvements. This in turn requires a factory that can fully integrate all other factory components. Preserving the decades-long trend of 30% per year reduction in cost per function also requires capturing all possible cost-reduction opportunities. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs.

The success and market growth of semiconductors has been driven largely by continuous improvement to cost per function. Many factors have led to these productivity gains including process technology shrinks, wafer size changes, yield improvements, and manufacturing productivity gains. The era of non-incremental technology introductions (high-κ gate dielectric, metal gates, Cu/low-κ interconnect, etc.), complex product designs and large-scale transistor integration, and process complexity (such as system on a chip with 30 or more mask layers) is making the pace of productivity improvements harder to sustain when compared with historical norms.

One positive example where fab productivity gains have continued in a cost-effective manner is the transition to 300 mm wafers where collective wisdom of industry has abated the ballooning increase in the cost of a new fab. Nevertheless, fab investment costs continue to increase driven both by the cost of technology as well as the desire to build larger factories to get economies of scale.

The overall Factory Integration scope addresses several challenges that threaten to slow the industry's growth, including:

3. *Integrating complex business models with complex factories*—Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high-mix and volatile market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. The factory now must integrate an even larger number of new and different equipment types and software applications to meet complex market objectives and customer requirements. High-mix and low-volume product runs are making mask cost, fabrication, and factory integration extremely difficult in a market where average selling prices (ASPs) are declining. Lack of robust and fully featured software systems to manage the complexity of factory and equipment control is also adding to our challenges.
4. *Production equipment reliability, utilization, and extendibility*—Production equipment is not keeping up with availability and utilization targets, which has an enormous impact on capital and operating costs. The industry is unable to effectively reuse equipment or skills due to the rapid introduction of new equipment (157 nm and EUV lithography) and materials (SOI, high-κ gate stack, low-κ dielectrics, etc.).
5. *Maturing 300 mm factory challenges—We are now moving form ramping to maturity on the 300 mm factories and hence it is necessary to focus on improving and sustaining 300 mm efficiency targets such as*: 1) >2.25 more die per wafer than 200 mm, 2) >30% cost per die reduction, 3) 100% automated materials handling system (AMHS) interbay and intrabay systems for operational flexibility and cost improvements, 4) the ability to track and run different recipes for each wafer within a carrier for operational flexibility, and 5) reduction in utilities, power consumption and emission.
6. *Post bulk CMOS and next wafer size manufacturing paradigm*—the conversion to novel devices and the next wafer size beyond 300 mm (i.e., 450 mm wafers) represent key inflection points for semiconductor manufacturing. Novel devices beyond bulk CMOS and their potential impacts to equipment and manufacturing are not well defined, but are expected to be significant. Conversion to wafers larger than 300 mm represents another change opportunity to improve manufacturing cost effectiveness and will be an important factor in the semiconductor industry's ability to continue realizing Moore's law.

In order to address these challenges the following fundamental semiconductor manufacturing attributes must be improved:

- Cost per unit area of silicon—manufacturing cost per unit area of silicon is a measure of productivity. The capital cost of a factory has grown significantly each year, from $50M US in the 1980s to over $3B US in 2005.[3]

[3] *Strategies for determining or dealing with the upper limit of factory cost are beyond the scope of this chapter.*

- Time to ramp a factory to high-volume production with high yields—decreasing time to ramp a factory to high-volume production and high yield has more economic impact than reducing operating costs. New factories must be built and ramped to mature production at a much faster rate, as reflected in the Technology Requirements tables. Existing factories must be upgraded faster without impacting ongoing production.
- Increasing flexibility to accommodate technology and business changes—Technology advances and the globalization of manufacturing enterprises have led to a decrease in cost for electronic components. This enables new markets to open and creates the need to increase the pace of new product introduction. The flexibility to accommodate these changes in business expectations must improve without significant cost impacts.

SCOPE

A semiconductor factory extends across several manufacturing domains (Figure ITWG 1), which include wafer manufacturing or fabrication, chip manufacturing that involves probe/e-test, backgrind, and singulation, and finally product manufacturing where the final package is assembled and tested. Silicon substrate manufacturing and product distribution are outside the scope of factory integration.

In order to clearly understand the integrated factory requirements and at the same time define measurable and actionable metrics, the factory integration is divided into five thrusts, or functional areas, that are required to perform semiconductor manufacturing. The five functional thrusts are Factory Operations, Production Equipment, Material Handling, Factory Information & Control Systems, and Facilities. Factory Operations, and its associated factory business model, is a key driver of requirements and actions for the other five thrusts. Overall, these five thrusts are used to clarify how difficult challenges translate into technology requirements and potential solutions. In addition to these five thrust areas, the factory integration section also addresses the cross-cut issues and also key focus areas that cut across all these five thrusts.

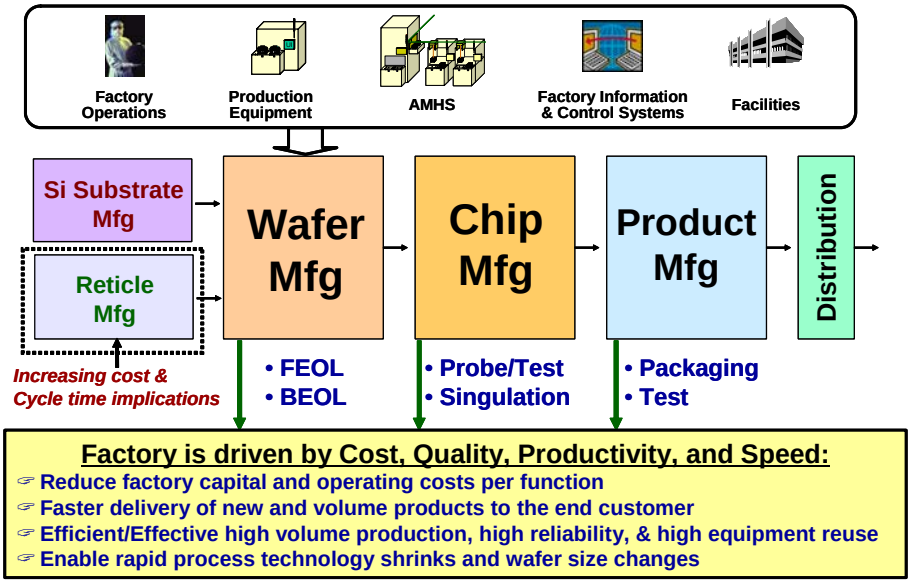


Figure ITWG 1 Factory Integration Scope

DIFFICULT CHALLENGES

Difficult challenges associated with factory integration span multiple technology generation s and cut across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry convenience to minimize disruptions to operating factories. Near-term difficult challenges for the factory include business, technical, and economic issues that must be addressed.

Table ITWG 10 Factory Integration Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Responding to rapidly changing, complex business requirements	Many new and co-existing business models including IDM, Foundry, Fabless, Joint Ventures, Collaborations, other Outsourcing, etc need to be considered in the Factory Integration Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design -> prototype and pilot -> volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with high mix manufacturing as the model in response to diversified customers' requirement Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance to optimize output and improve cycle time for high mix factories Ability to constantly adjust equipment loading to keep the factory profitable Manufacturing knowledge and control information need to be shared as required among disparate factories
Achieving growth targets while margins are declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes
Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Small process windows and tight process targets at >45 nm in many modules make process control increasingly difficult Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

Table ITWG 10 Factory Integration Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability) Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting process requirements at 65nm and 45nm generations running production volumes	Small process windows and tight process targets at 45 nm generations in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging factory paradigm and next wafer size change	Uncertainty about the next wafer size [450mm] and the conversion timing [See Backup material as a link in the electronic chapter at http://public.itrs.net.] Traditional strategies to scale wafers and carriers for the next wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable the next wafer size conversion [to 450 mm] at an affordable cost

ASSEMBLY AND PACKAGING

DIFFICULT CHALLENGES

Table ITWG 11 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Impact of new materials	*BEOL materials including Cu/low κ* Direct wirebond and bump to Cu or improved barrier systems bondable pads Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system Improved fracture toughness of dielectric materials Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed Probing over copper/low κ Singulation technology for circuits incorporating ultra low κ dielectrics
Wafer Level Packaging	I/O pitch between 150 µm and 250 µm greater than 100 I/O Solder joint reliability Wafer thinning and handling technologies Compact ESD structures (this applies to other package types as well) TCE mismatch compensation for large die
Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Rapid turn around modeling and simulation Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) In package decoupling System level co-design EDA for "native" area array is required to meet the Roadmap projections Models for reliability prediction
Embedded Components	Low cost embedded passives: R, L, C Embedded active devices at both wafer and substrate level Wafer level embedded components
Thinned die packaging	Wafer/die handling for thin die Compatibilty of different carrier materials (organics, silicon, ceramics, glass, laminate core) Reliability Testability Thin die for embedded active devices Electrical and optical interface integration
Close gap between chip and substrate – Improved Organic Substrates	Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Increased via density in substrate core Alternative plating finish to improve reliability Tg compatible with Pb free solder processing (including rework @260C)
High Current Density Packages	Electromigration I Thermal/mechanical reliability modeling. Whisker growth Thermal dissipation
Flexible System Packaging	Conformal low cost organic substrates Small and thin die assembly Handling in low cost operation

Difficult Challenges ≥ 32 nm	*Summary of Issues*
3D Packaging	Thermal management Co-Design and simulation tools Wafer to wafer bonding Through wafer Via structure and via fill process Bumpless interconnect architecture
Fine Pitch Packages	Tighter tolerances for fine pitch BGA Minimizing kerf loss in singulation for small outline packages High temperature warpage for fine pitch BGA Reliability to meet drop test requirements for mobile electronics
Difficult Challenges <32 nm	*Summary of Issues*
Package Cost does not follow the Die Cost Reduction Curve	Margin in packaging is inadequate to support investment required to reduce cost Increased device complexity requires higher cost packaging solutions
Small Die with High Pad Count and/or High Power Density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: Improved current density capabilities Higher operating temperature
High Frequency Die	Substrate wiring density to support >20 lines/mm Lower loss dielectrics—skin effect above 10 GHz "Hot spot" thermal management
System-level Design Capability for Integrated Chips, Passives, and Substrates	Partitioning of system designs and manufacturing across numerous companies will make optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Embedded passives may be integrated into the "bumps" as well as substrates.
Emerging Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	Organic device packaging requirements not yet define (will chips grow their own packages) Biological packaging will require new interface types

ENVIRONMENT, SAFETY, AND HEALTH

WHAT'S NEW?

For 2005 the *ESH chapter* has been fully reorganized following a major revision of the ESH Difficult Challenges that now address the four categories: Process Chemical Management, Equipment Management, Product Stewardship, and Facilities Energy and Water Consumption. The revised Difficult Challenges are now more reflective of their multiple functions to be able to incorporate external influences (e.g., regulatory) on semiconductor technology development, serve as a more effective "filter" to evaluate the technology thrust needs, and identify intrinsic needs for ESH R&D. There has been further elimination of repetitive technical requirements that are considered ESH maintenance of business such as tool safety audits, which do not themselves require development, but are a method used to evaluate tools entering the marketplace. Increasing emphasis has been placed on the need to understand and manage materials and material alternatives, given the growth in public policy concern over use of chemicals for which little ESH characterization is available. In addition, Product Stewardship has been formerly identified as an ESH challenge with appropriate technical requirements, as there grows increasing emphasis in the market over reducing hazardous content of products.

DIFFICULT CHALLENGES

Table ITWG 12 ESH Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Lack of quality rapid assessment methodologies to ensure that chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation *Chemical Data Availability* Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals *Chemical Exposure Management* Lack of information on how the chemicals and materials are used and what process by-products are formed
Process and equipment management	*Chemical Reduction* Need to develop processes that meet technology demands while reducing impact on human health, safety and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management *Environment Management* Need to develop effective management systems to address issues related to re-use and disposal of equipment, and hazardous and non-hazardous residues from the manufacturing processes *Water and Energy Conservation* Need to reduce water and energy consumption Need for innovative energy and water-efficient processes and equipment *Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling *Byproducts Management* Need to understand ESH characteristics of process by-products to identify the appropriate mitigation *Chemical Exposure Management* Need to design-out potential for chemical exposures and need for personal protective equipment (PPE) *Equipment Ergonomics* Need to design ergonomically correct and safe equipment *Design for Maintenance* Need to design equipment so that maintenance and service may be safely performed by a single person Need to design equipment so that commonly serviced components and consumable items are easily accessed Need to minimize health and safety risks during maintenance activities.
Facilities energy and water optimization	*Conservation* Need to reduce energy and water use *Tool Heat Removal* Need for more efficient thermal management of cleanrooms and facilities systems *Global Warming Emissions Reduction* Need to design energy efficient processing equipment and manufacturing facilities Need to reduce emissions from processes using GWP chemicals
Sustainability and product stewardship	*End-of-Life Disposal/Reclaim* Need to design tools, equipment and products to facilitate disposal at end of life *Design for ESH* Need method to holisticly evaluate and quantify the ESH impacts of processes, chemicals, and process equipment for the total manufacturing process Need to make ESH a design parameter in development of new equipment, processes and products *Sustainability Metric* Need to identify the elements for defining and measuring the sustainability of a technology generation

Table ITWG 12 ESH Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Lack of quality rapid assessment methodologies to ensure that chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation *Chemical Data Availability* Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals *Chemical Exposure Management* Lack of information on how the chemicals and materials are used and what process by-products are formed
Process and equipment management	*Chemical Reduction* Need to develop processes that meet technology demands while reducing impact on human health, safety, and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management *Environment Management* Need to develop effective management systems to address issues related to re-use and disposal of equipment, and hazardous and non-hazardous residues from the manufacturing processes *Water and Energy Conservation* Need to reduce water and energy consumption Need for innovative energy and water-efficient processes and equipment *Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling *Byproducts Management* Need to understand ESH characteristics of process by-products to identify the appropriate mitigation *Chemical Exposure Management* Need to design-out potential for chemical exposures and need for personal protective equipment (PPE) *Equipment Ergonomics* Need to design ergonomically correct and safe equipment *Design for Maintenance* Need to design equipment so that maintenance and service may be safely performed by a single person Need to design equipment so that commonly serviced components and consumable items are easily accessed Need to minimize health and safety risks during maintenance activities
Facilities energy and water optimization	*Conservation* Need to reduce energy and water use *Tool Heat Removal* Need for more efficient thermal management of cleanrooms and facilities systems *Global Warming Emissions Reduction* Need to design energy efficient processing equipment and manufacturing facilities. Need to reduce emissions from processes using GWP chemicals
Sustainability and product stewardship	*End-of-Life Disposal/Reclaim* Need to design tools, equipment, and products to facilitate disposal at end of life *Design for ESH* Need method to holisticly evaluate and quantify the ESH impacts of processes, chemicals, and process equipment for the total manufacturing process Need to make ESH a design parameter in development of new equipment, processes and products *Sustainability Metric* Need to identify the elements for defining and measuring the sustainability of a technology generation

YIELD ENHANCEMENT

WHAT'S NEW?

The Yield Enhancement ITWG changed and redefined the key challenges for the 2005 ITRS. The most important challenge will be the signal-to-noise ratio for defect inspection tools. Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes requested by technology generations. Increasing the inspection sensitivity at the same time increases the challenge to find small but yield-relevant defects under a vast amount of nuisance, false defects. At the same time a low cost of ownership of the tools demands for high throughput inspection. This is in conflict with the issue of improving the signal-to-noise ratio.

Other topics challenging the Yield Enhancement community are prioritized as follows:

- *High Throughput Logic Diagnosis Capability*—Identification and tackling of systematic yield loss mechanisms
- *Detection of Multiple Killer Defect Types*—and simultaneous differentiation at high capture rates, low cost of ownership and throughput
- *High-Aspect-Ratio Inspection*—Need for high-speed and cost-effective high aspect ratio inspection tools remains, as the work-around approach using e-beam inspection does not meet requirement for throughput and low cost
- *Process Stability versus Absolute Contamination Level Including the Correlation to Yield*—Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits
- *In-line Defect Characterization and Analysis*—as alternative to EDX analysis systems [1]. The Focus is on light elements, small amount of samples due to particle size, and microanalysis
- *Wafer Edge and Bevel Control and Inspection*—In order to find the root cause, inspection of wafer edge, bevel, and apex on front and backside is needed
- *Rapid Yield Learning Requires Efficient Data Management and Test Structures for*—enabling the rapid root-cause analysis of yield-limiting conditions
- *Development of Parametric Sensitive Yield Models*—including new materials, optical proximity correction (OPC), and considering the high complexity of integration

The 2005 *Yield Enhancement chapter* consists of four subchapters as Yield Learning, Defect Budget and Yield Model, Defect Detection and Characterization, and Wafer Environment and Contamination Control. The key changes to previous ITRS editions were within the following subchapters:

- Defect Budget and Yield Model

  The current Defect Budgets tables are based on the survey that was carried out five year ago, so that the color tiling is not done intentionally in this 2005 revision. It is believed that the defect budgets should be re-calculated by using the latest data that will be corrected through a new survey and procedure by next revision. The Yield Enhancement ITWG will survey semiconductor-manufacturing companies for defect control limits of semiconductor manufacturing equipments. Regarding the Yield Model, the Negative Binomial Model has been used. However, another technical area such as Starting Materials and Surface Preparation technologies in Front End Process is using a different model. Therefore, a discussion has been started between YE-ITWG, Starting Material sub-TWG (FEP ITWG) and Surface Preparation sub-TWG (FEP ITWG). Through this discussion, defect models used in ITRS would be unified and the YMDB table will be changed in the next revision.
- Defect Detection and Characterization

  The bevel and edge inspection was identified as increasing yield impact and importance. The existing tables on defect inspection tool table were extended by specifications and requirements of semiconductor manufacturing companies for a new type of defect inspection tools.
- Wafer Environment and Contamination Control

  In the Wafer Environment and Contamination Control section, further consolidation of the values in the Requirements tables has been achieved, moving from the point of connection to the point of entry to the tool as far as possible. This has included an effort to standardize and further define the interface nomenclature. Further requirements and inputs have been received both with regard to emerging processes, such as immersion lithography and new atomic layer deposition (ALD) and chemical vapor deposition (CVD) precursors, as well as clarifications with regard to established processes such as metallization and chemical mechanical planarization (CMP). These

requirements have been compared with actual data from fabs and incorporated into the table. The table has been restructured in a more process-specific way.

The effort to define the importance of process stability versus absolute contamination on yield has been continued and will be for the next revision.

DIFFICULT CHALLENGES

Table ITWG 13 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Signal-to-noise ratio—Increasing the inspection sensitivity at the same time increases the challenge to find small but yield relevant defects under a vast amount of nuisance, false defects. The key of a successful inspection result is, besides achieved sensitivity, the ease to get to the defects of interest (DOI).	Filtering and use of ADC is a potential solution Reduction of background noise from detection units and samples to improve the sensitivity of systems Need to improve signal to noise ratio to delineate defect from process variation Where does process variation stop and defect start?
High throughput logic diagnosis capability—The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window.	Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow Potential issues can arise due to different ATPG flows to accommodate; ATE architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die
Detection of multiple killer defects—Differentiation of multiple killer defect types is necessary at high capture rates, low cost of ownership and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity Reduction of inspection costs is crucial in view of CoO Ability to detect particles at critical size may not exist Detection of line edge roughness due to subtle process variation Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision
High aspect ratio inspection—Need for high-speed and cost-effective high aspect ratio inspection tools remains. The interim approach using e-beam inspection does not meet the requirements for throughput and low cost.	Poor transmission of energy into bottom of via and back out to detection system. To detect rapidly defects at ½× ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches, and especially defects near or at the bottoms of these features Large number of contacts and vias per wafer
Difficult Challenges < 32 nm	*Summary of Issues*
Process stability versus absolute contamination level including the correlation to yield—Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield Define a standard test for yield/parametric effect Definition of maximum process variation (control limits)
Inline defect characterization and analysis—As alternative to EDX analysis systems [1]. The focus is on light elements, small amount of samples due to particle size, and microanalysis.	The sampling probe should show minimum impact as surface damage or destruction of SEM image resolution Supply of information of chemical state and bonding especially of organics is recommended Small volume technique adapted to the scales of technology generations Capability to distinguish between the particle and the substrate signal
Wafer edge and bevel control and inspection—Defects and process problems around wafer edge and wafer bevel can cause yield problems.	Find the root cause inspection of wafer edge, bevel and apex on the wafer front and backside
Rapid yield learning requires efficient data management and suitable test structures—Enabling rapid root-cause analysis of yield-limiting conditions. With increasing process complexity and fewer yield learning cycles with each subsequent technology generation it would be impossible to achieve historic yield ramps and mature yield levels.	Development of automated, intelligent structures, analysis, and reduction algorithms that correlate facility, design, process, test, and WIP data Need of tools and methods for short yield learning cycles
Development of parametric sensitive yield models including new materials—OPC and considering the high complexity of integration. The models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology generations Address complex integration issues Model ultra-thin film integrity issues Improve scaling methods for front-end processes including increased transistor packing density

ADC—automatic defect classification
[1] Cross-link to Metrology chapter

METROLOGY

WHAT'S NEW?

Metrology continues to be greatly challenged by the rapid introduction of new materials, processes, and structures. For the first time, CD-SEM and scatterometry-based measurement of critical dimensions are believed to be extendable to 32 nm. Although carrier mobility is already being improved by processed-based stress, the inadequacy of stress metrology has become a greater issue. The lack of sidewall measurement capability for dielectric layers on FINFET and similar structures is becoming more significant. Inline metrology for control of interface layers also remains a largely unmet challenge. The potential use of 3D interconnect will drive new metrology requirements. In the area of materials characterization, aberration-corrected transmission electron microscopy is pushing toward near atomic level imaging in 3D. Refer to the *Metrology chapter* for greater detail.

DIFFICULT CHALLENGES

Table ITWG 14 Metrology Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low-κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new low-κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. Metal gate work function characteization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 32 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

MODELING AND SIMULATION

WHAT'S NEW?

In 2005, the *Modeling and Simulation chapter* of the ITRS saw a continuation and reinforcement of several trends which have developed during the last years: First, as a cross-cut ITWG it started from a thorough analysis of the requirements of the other ITWGs, both via written material and via several meetings. In the current ITRS this has again resulted in elaborated crosscut texts dealing with the interaction between Modeling and Simulation and each of the other ITWGs. This information has, in turn, again been used as key input for the preparation of the 2005 Modeling and Simulation chapter including its challenges and requirements tables. As part of this, several trends for research requirements have again be enforced, as follows: the need for more predictive physical models; the ever prevailing need for more efficient algorithms and simulation programs that allow to tackle larger problems; more emphasis on material modeling and simulation; broadening of the scope for equipment simulation; and especially the need for a breakthrough in the integration between different levels of simulation, from process through devices and circuits up to design, and between different physical aspects, which were so far largely treated in isolation. Two examples are layout-generated stress, which influence both silicon-processing steps and via stress dependent mobility also directly the electrical device performance, and the coupled electrical-thermal-mechanical simulation of the performance and reliability of interconnects. In many chapters of the ITRS the impact of process variations and statistical fluctuations of dopants has now been highlighted. The consequence drawn by Modeling and Simulation has been the introduction of a new subchapter on "TCAD for Design, Manufacturing and Yield" that summarizes the prospects and requirements on Modeling and Simulation to assess and minimize the impact of such variations on devices and ICs, and finally on design, manufacturing processes, and yield. This new application of TCAD requests substantial developments of physical models and simulation tools.

Since 2003 the scope of the Modeling and Simulation Difficult Challenges have stayed the same, however with considerable evolution in their details. Especially, in 2005 power consumption has been included in the challenge on high-frequency device and circuit modeling. Referring to front-end process modeling, new annealing methods, stress, and doping via epilayers have been explicitly included. In the challenge on integrated modeling of equipment, and materials, feature scale processes and influences on devices plasma reactions are now explicitly mentioned, and electrochemical polishing has been newly added. The challenge on lithography simulation has now put some more emphasis on equipment and mask effects. In the challenge on ultimate nanoscale CMOS simulation capabilities models for stress-induced device performance have been highlighted. For thermal-mechanical-electrical modeling for interconnections and packaging, efficient in-chip package layout and power management have been stressed. Most changes of the four long-term Difficult Challenges emphasize materials and first-principle modeling. Furthermore, the long-term challenge on compact modeling including more physical models and statistics has been broadened by complementing the improvement and enhancement of classical compact modeling by the efficient extraction of circuit-level variations from process and device simulation.

The development of the technological capabilities and the requirements of the focus technologies, especially PIDS, FEP, Lithography and Interconnect have resulted in many changes of the details of the Modeling and Simulation requirement tables. Additionally, the near- and the long-term requirements are now combined into one table, which removes the artificial problem that seven years—the original separation between near- and long-term—is by no way a better time for a requirement to start or to stop.

The likely most difficult challenge for Modeling and Simulation is not a technical one, and is therefore also not mentioned in the tables—Insufficient R&D resources limit the speed of development in Modeling and Simulation, and in turn hinder the community to deliver the required results in time. It has to be stressed that it is not sufficient to make a correct assessment of the industrial requirements in the area and to have in principle concepts and capabilities available to meet those—if research funding is not made available in sufficient amount and in time Modeling and Simulation will not be able to exploit its prospects and will not be able to make its full contribution to the industrial development in nanoelectronics. The ITRS process can here only partly help by promoting cooperation and the most efficient use of resources.

DIFFICULT CHALLENGES

Table ITWG 15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
High-frequency device and circuit modeling for 5–100 GHz applications	Efficient extraction and simulation of full-chip interconnect delay and power consumption
	Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters
	Extension of physical device models to III/V materials
	High-frequency circuit models including non-quasi-static effects, substrate noise, 1/f noise and parasitic coupling
	Parameter extraction assisted by numerical electrical simulation instead of RF measurement
	Scalable active and passive component models for compact circuit simulation
	Co-design between interconnects and packaging
Front-end process modeling for nanometer structures	Diffusion/activation/damage/stress models and parameters including SPER and low thermal budget processes in Si-based substrate, that is, Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices
	Modeling of epitaxially grown layers: Shape, morphology, stress
	Characterization tools/methodologies for ultra shallow geometries/junctions and low dopant level
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Front-end processing impact on reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms, and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Multi-generation equipment/wafer models
Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM)
	Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, and mechanical stability
	Methods to easily calibrate resist model kinetic and transport parameters
	Models that bridge requirements of OPC (speed) and process development (predictive)
	Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system
	Models and experimental verification of non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Multi-generation lithography system models
	Simulation of defect influences/defect printing
	Modeling lifetime effects of equipment and masks
Ultimate nanoscale CMOS simulation capability	Methods, models and algorithms that contribute to prediction of CMOS limits
	General, accurate and computationally efficient quantum based simulators
	Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Gate stack models for ultra-thin dielectrics
	Models for device impact of statistical fluctuations in structures and dopant distribution
	Material models for stress engineering.
	Physical models for stress induced device performance
Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, thermodynamic and electronic properties of low κ, high κ, and conductors for efficient in-chip package layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Model reliability of packages and interconnects (e.g., stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion)
	Models for electron transport in ultra fine patterned conductors.

Table ITWG 15 Modeling and Simulation Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Modeling of chemical, thermomechanical, and electrical properties of new materials	Computational materials science tools to describe materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: Gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties. Linkage with first principle computation and reduced model (classical MD or thermodynamic computation). Accumulation of databases for semiempirical computation. Models for new ULK materials that are also able to predict process impact on their inherent properties.
Prediction of dispersion of circuit parameters	Computer-efficient inclusion of influences of statistics (including correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling Efficient extraction of circuit-level variations from process and device simulation
Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
Optoelectronics modeling	Materials and process models for optoelectronic elements (transmitters and receivers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2004. Additionally, an *ORTC Glossary* is provided as an appendix.

OVERVIEW OF 2005 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using "production tooling." Furthermore, a second company must begin production within three months (see Figure 3). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology "node" manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of "node" advancement. This approach of measuring technology progress complicates the "node" relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology "node" references in Flash memory product announcements, and Flash technology is receiving increased emphasis in the 2005 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage.

The International Roadmap Committee (IRC) has decided in the latest 2005 ITRS that the best way to minimize confusion between the ITRS and individual company public announcements is to separate the tracking of the various technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM product is referenced to un-contacted poly dense parallel lines (refer to Figure 2). To simplify the table header options,

the MPU un-contacted poly half-pitch line item is not included in the 2005 ITRS. Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the new emphasis on separate product trend tracking, the "hpXX" "node" references (i.e., hp90, hp65, hp45, etc, associated only with the DRAM product M1 half-pitch) were removed from the 2005 ITRS common table header.. In the 2005 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) will be emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item.

That being said, the DRAM stagger-contacted M1 half pitch values currently continue to represent the most aggressive interconnect half-pitch driving leading-edge lithographic line/space resolution, and the DRAM M1 half-pitch is used as the common table header reference in the 2005 ITRS. Other individual product technology trends are continuously monitored against DRAM M1 half-pitch, and in the future, overall lithography resolution may be driven by a feature size trend from a different product.

For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is projected to be ahead of DRAM stagger-contacted M1 half-pitch by one year in the near future. A one-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to the DRAM stagger-contacted M1 half-pitch, but additional timing lead increase may require Flash memory technology to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2005 ITRS table technology trend targets have now been completely annualized from 2005 through the 15-year Roadmap horizon in 2020. However, per previously established IRC guidelines, the 2005 ITRS retains the definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures 6 and 7.

Please note from the 2005 ITRS ORTC Table 1a and 1b, that the timing of a technology cycle may be different for a particular product. For example, the DRAM stagger-contact half-pitch M1 is forecast to be on a 0.71×/3-years (0.50×/6-years) timing cycle from the historical 2004/90 nm actual (after being on a two-year timing cycle pace from the 2000/180 nm actual) through the 2019/16 nm target. The annual multiplier for the three-year cycle timing is 0.8909×/year, which is used to calculate the interim annual trend targets (examples: 2005/80 nm, 2020/14 nm).

After taking into account the available industry data and ITWG and IRC inputs, consensus was reached on the new Flash product technology timing model, based on the uncontacted polysilicon half-pitch definition. The Flash uncontacted polysilicon half-pitch is set on a two-year cycle timing pace from 2000/180 nm through 2006/64 nm. At this point, it was determined by the Lithography ITWG that the Flash uncontacted polysilicon half-pitch could numerically be one year "ahead" of the DRAM stagger-contacted M1 half-pitch, even though the same technology process equipment was being used to achieve that target. However, after 2005/64 nm, the Flash uncontacted polysilicon half-pitch would turn to a three-year timing cycle, exactly one-year ahead of the DRAM trend, and would extend to 2020/13 nm on an annual basis.

As noted above, the MPU (and high-performance ASIC) Product Trend cycle timing was changed in the 2005 ITRS to be based on the same stagger-contact M1 half-pitch definition as DRAM. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch was set on a 2.5-years (0.50×/5-years) cycle timing pace from the historical 2000/180 nm actual point through 2010/45 nm. At the 2010/45 nm point, it was decided that the MPU M1 targets would "catch up" and become equal to the DRAM M1 cycle timing targets (3-year timing cycle) through the end of the roadmap in 2020.

The MPU (and high-performance ASIC) final physical gate-length (phGL) targets remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2005/32 nm point, and then the trend targets revert to a three-year timing (0.5×/6 years; 0.8909/year) cycle through the end of the Roadmap to 2020/6 nm. The Lithography and FEP ITWGs reached agreement on a new ratio (1.6818× multiplier above the physical gate length) between the final physical gate length, which includes etch, and the printed gate length targets.

The low-operating-power ASIC gate length targets were established by the PIDs ITWG, and were placed two years behind the MPU (and high-performance ASIC) printed gate length and physical gate length targets.

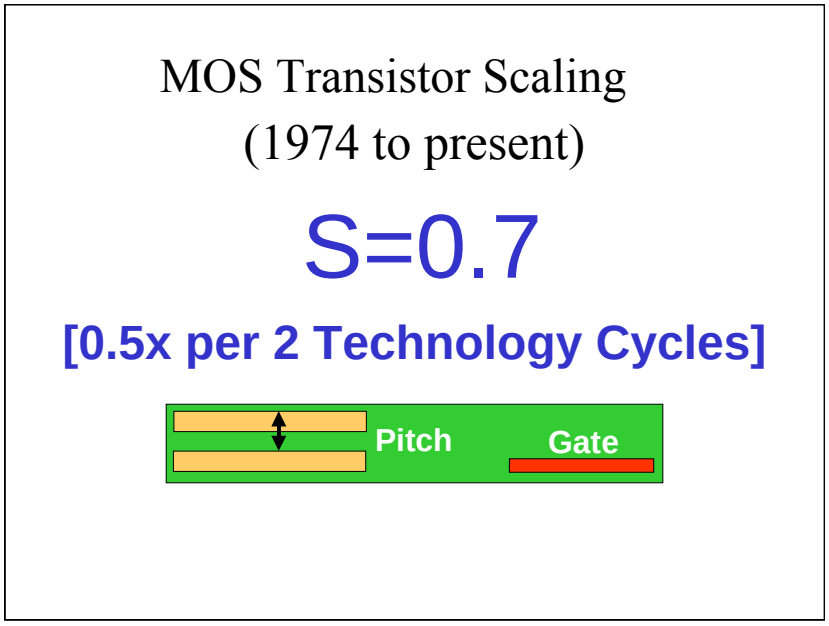


Figure 6 MOS Transistor Scaling—1974 to present

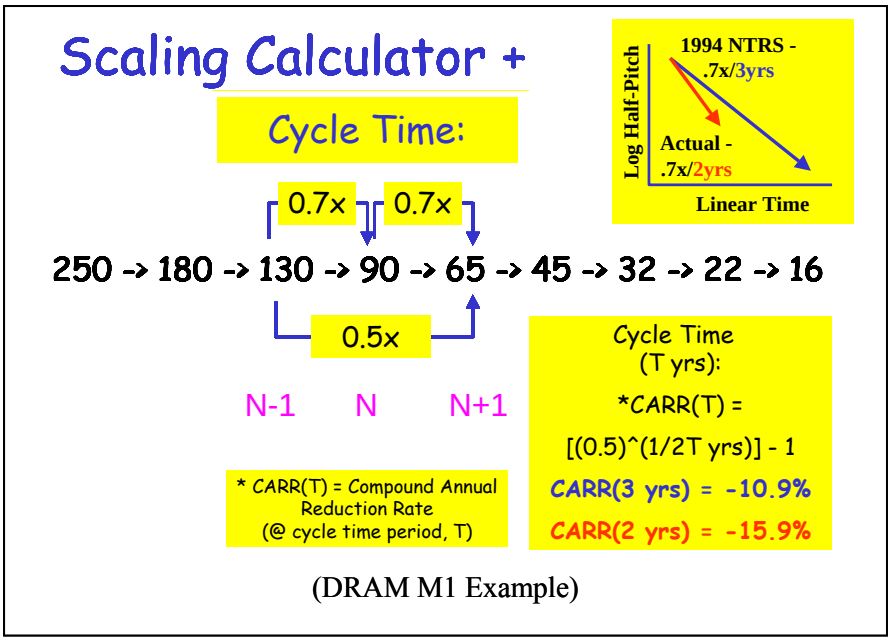


Figure 7 Scaling Calculator

ROADMAP TIMELINE

The 2005 edition of the Roadmap maintains a 15-year projection, from 2005 as a reference year and through 2020. The timing trends of the future technology pace of the DRAM product still represents the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size) after 90nm/2004, unchanged from the 2003 edition. From surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2004, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

In the 2001 ITRS, the 130 nm DRAM product M1 half-pitch was pulled in an additional year (from 2002 in the 1999 ITRS to 2001), anticipating a continuation of an observed historical two-year technology cycle calculated from 350 nm/1995, 250 nm in 1997, 180 nm in 1999). Data provided by DRAM manufacturers in 2003, which was based upon the more rigorous customer-product-qualified production ramp, indicated that the actual production ramp timing was as follows: 350 nm/1995, 250 nm/1998, 180 nm/2000 and 130 nm/2002. This new data indicates a two-year cycle timing, but delayed one year from the original 2001 ITRS timing. Data gathered on actual DRAM product ramped in the 2004 PIDS member surveys confirms the two-year cycle step between 130 nm/2002 and 90 nm/2004. Although there was the possibility of a continuation of this new delayed two-year cycle trend, the present DRAM product manufacturer consensus, confirmed by the PIDS survey update, projects a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch throughout the 2005–2020 Roadmap period, as illustrated in Figure 8.

As mentioned above, the DRAM interconnect half-pitch will continue to be used as the most representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). However, the Flash uncontacted polysilicon half-pitch feature has crossed over DRAM M1, and now is now also a driver of leading-edge technology manufacturing. Similarly, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2.5-year cycle pace and are presently expected to catch up and remain equal to the DRAM half-pitch in 2010/45 nm. With the new product-oriented focus of the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figure 8.

ROUNDED TREND NUMBERS

As a result of the new DRAM half-pitch data inputs, and using 180 nm as the calculation standard for trends, the 2005 ITRS now includes a correction of the past "rounding" convention for the technology cycle trend target. The actual mathematical trend reduces by 50% every other technology cycle, resulting in actual versus rounded number targets, starting from 350 nm in 1995, as follows in Table C.

Table C Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	1995	1998	2000	2002	2003	2004	2006	2007	2009	2010	2012	2013	2015	2016	2018	2019
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**101**	**90**	**71.4**	**63.6**	**50.5**	**45**	**35.7**	**31.8**	**25.3**	**22.5**	**17.9**	**15.9**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**	**50**	**45**	**36**	**32**	**25**	**22**	**18**	**16**

Note the new rounding corrections become more critical as the industry moves into the double-digit cycles of the new nanotechnology (sub-100 nm) era. Please note also that some regions, for their own past publication consistency, will retain their right to continue to track the previous technology generations beginning with 100 nm/2003. Starting from 100 nm in 2003 will result in milestones that are targeted one year earlier than the present 2003 roadmap convention (70 nm/2006; 50 nm/2009; 36 nm/2012; 25 nm/2015). By consensus of the IRC both number sets are available for long-term calculations, since the original 2001 ITRS long-term columns were retained (2010/45 nm; 2013/32 nm; 2016/22 nm), and new columns (2012/36 nm; 2015/25 nm; 2018/18 nm) were added.

UPDATES TO THE ORTC

In addition to the redefinition of the MPU/ASIC M1 half-pitch as a stagger-contacted half-pitch the same as DRAM, a new addition to the 2005 ITRS ORTC technology target line items is the Flash product uncontacted polysilicon half-pitch. This was added to the ORTC Table 1a and 1b, and the previous MPU uncontacted polysilicon half-pitch item was deleted

The *printed* MPU gate length received a major correction to more an aggressive starting point in the 2001 ITRS. In addition, a new *physical* gate length is being tracked that further reduces the bottom gate length dimension of a fully processed transistor. The physical gate length trends remain unchanged for both the *2003* and the 2005 ITRS, and are now forecast to continue scaling by about 70% per three-year cycle through the Roadmap horizon in 2020, consistent with the present DRAM half-pitch trend forecast. Refer to Figure 8.

The ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2006 ITRS Update process, and the possibility of a continued two-year node cycle in some of the individual product technology trends. In particular, Logic and Flash product half-pitch acceleration will be monitored as future technology leadership candidates.

As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap shifts, it was agreed to continue the practice of publishing annual technology requirements from 2005 through 2013, called the "Near-term Years," and also annual requirements from 2014 through 2020, called the "Long-term years".

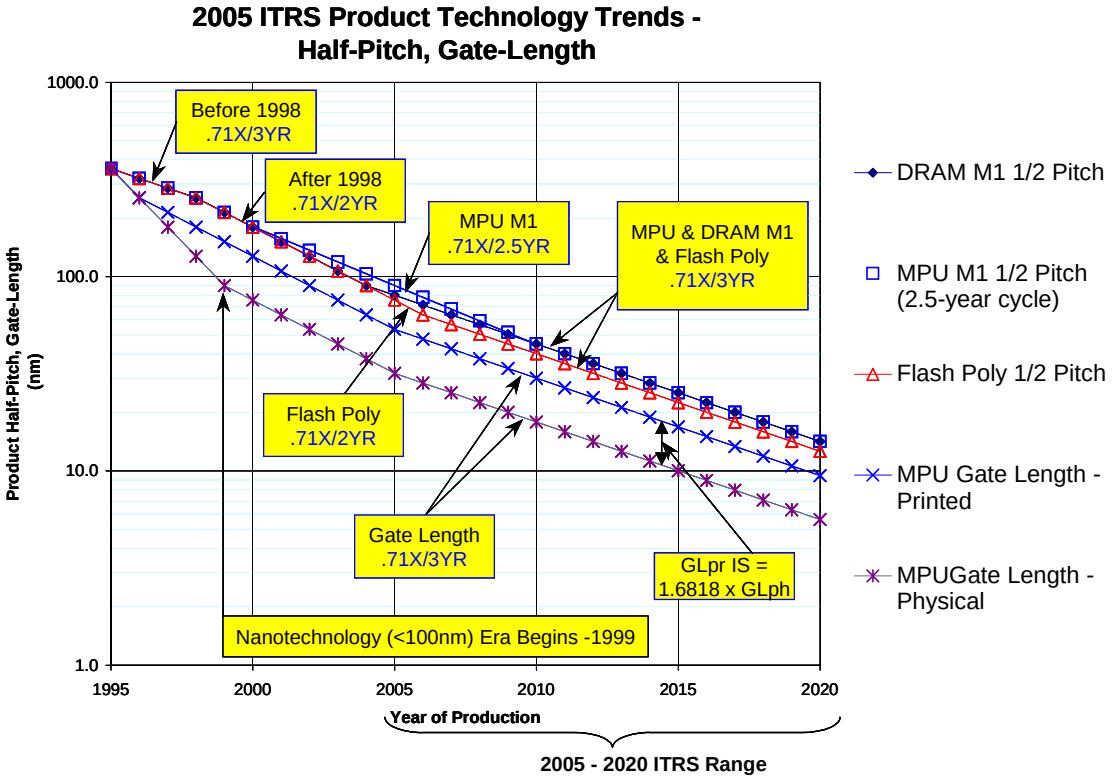


Figure 8 2005 ITRS—Half Pitch and Gate Length Trends

PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. For the 2005 ITRS edition, the singular "technology node" "hpXX" reference has been removed in favor of individual product technology trends which may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolution/shrink paths becomes more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic (as exemplified by MPU) technology moved at the same pace as DRAM technology, but after 2000/180 nm began moving at a slower 2.5-year technology cycle pace while DRAM technology continued on the accelerated two-year pace. During the last few years, the development rate of new technologies used to manufacture microprocessors has continued on the 2.5-year pace, while DRAMs are now forecast to slow to a three-year cycle pace through the 2020 Roadmap horizon. As a result of continuing on the faster 2.5-year cycle pace, microprocessor products are closing the half-pitch technology gap with DRAM, and are now also driving the most leading-edge lithography tools and processes—especially for the capability to process the isolated-line feature of the printed and physical gate length. In addition Flash technology, as defined by uncontacted polysilicon, has also accelerated to the point where it too is driving at the leading edge. With this 2005 Roadmap it is recognized that DRAM is still in the lead as a driver, but the Flash and microprocessor products now also share the technology leadership role.

However, several fundamental differences exist between the two families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch.

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2005 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the ORTC tables. The MPU product chip size tables now appear more similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items were added to communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations. Table 1a and 1b summarize the near and long-term technology trend metrics. As agreed, the ITRS technology "node" identifier associated with the DRAM M1 half pitch, hpXX has been removed, even though DRAM would continue to be the DRAM half-pitch, but also included are the aggressive MPU gate-length performance-driven feature sizes. For completeness, the MPU/ASIC product metal half-pitch is also tracked and will trail slightly behind the DRAM half-pitch, but will become equal in 2010 and beyond. The ASIC/low power gate lengths are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of the half-pitch and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2004/90 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (1998/250 nm–2004/90 nm) accelerated two-year cycle rate is approximately 16%/year reduction on an annual basis (~30% reduction/two years). As noted above the new Flash memory uncontacted polysilicon turns to the three-year pace in 2006 after crossing over the DRAM M1, and the MPU/ASIC M1 (generically referred to as MPU in graphs) catches up to DRAM M1 in 2010/45 nm, and returns to a three-year node pace (refer to Figure 8).

Table 1a Product Generations and Chip Size Model Technology Trend Targets—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Printed Gate Length (nm) ††	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
MPU Physical Gate Length (nm)	**32**	**28**	**25**	**23**	**20**	**18**	**16**	**14**	**13**
ASIC/Low Operating Power Printed Gate Length (nm) ††	**76**	**64**	**54**	**48**	**42**	**38**	**34**	**30**	**27**
ASIC/Low Operating Power Physical Gate Length (nm)	**45**	**38**	**32**	**28**	**25**	**23**	**20**	**18**	**16**
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**76**	**64**	**57**	**51**	**45**	**40**	**36**	**32**	**28**

Table 1b Product Generations and Chip Size Model Technology Trend Targets—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Printed Gate Length (nm) ††	**19**	**17**	**15**	**13**	**12**	**11**	**9**
MPU Physical Gate Length (nm)	**11**	**10**	**9**	**8**	**7**	**6**	**6**
ASIC/Low Operating Power Printed Gate Length (nm) ††	**24**	**21**	**19**	**17**	**15**	**13**	**12**
ASIC/Low Operating Power Physical Gate Length (nm)	**14**	**13**	**11**	**10**	**9**	**8**	**7**
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**25**	**23**	**20**	**18**	**16**	**14**	**13**

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These physical gate-length targets are driven by the need for maximum speed performance in logic microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design chapter tables as needs that drive device design and process technology requirements.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

MPU Physical Gate Length targets are unchanged from the 2003 ITRS and 2004 ITRS Update, but also included are the complete set of annualized Long-term targets through 2020. The printed gate length has been adjusted to reflect the agreement between the FEP and Lithography TWGs to use a standard factor, 1.6818, to model the relationship between the final physical gate length and the printed gate length, after additional processing is applied to that isolated feature.

MPU/ASIC M1 stagger-contact targets have been accelerated to 90 nm in 2005 to reflect actual industry performance per the Interconnect ITWG recommendation, and a new consensus model technology cycle timing of 2.5 years (to 0.71× reduction) has been applied through 2010, when the trend targets become equal to the DRAM stagger-contact M1 through 2020.

Numbers in the header are rounded from the actual trend numbers used for calculation of models in ITRS ORTC and ITWG tables (see discussion in the Executive Summary on rounding practices).

Table 1c DRAM and Flash Production Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
DRAM Product Table									
Cell area factor [a]	**8**	**8**	**8**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af2] (mm^2)	**0.051**	**0.041**	**0.032**	**0.019**	**0.015**	**0.012**	**0.0096**	**0.0077**	**0.0061**
Cell array area at production (% of chip size) §	**63.00%**	**63.00%**	**63.00%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Generation at production §	**1G**	**2G**	**2G**	**2G**	**4G**	**4G**	**4G**	**8G**	**8G**
Functions per chip (Gbits)	**1.07**	**2.15**	**2.15**	**2.15**	**4.29**	**4.29**	**4.29**	**8.59**	**8.59**
Chip size at production (mm^2)§	**88**	**139**	**110**	**74**	**117**	**93**	**74**	**117**	**93**
Gbits/cm2 at production §	**1.22**	**1.54**	**1.94**	**2.91**	**3.66**	**4.62**	**5.82**	**7.33**	**9.23**
Flash Product Table									
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**75.7**	**63.6**	**56.7**	**50.5**	**45.0**	**40.1**	**35.7**	**31.8**	**28.3**
Cell area factor [a]	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**
Cell area [Ca = af^2] (mm^2)	**0.023**	**0.016**	**0.013**	**0.010**	**0.008**	**0.006**	**0.005**	**0.004**	**0.003**
Cell array area at production (% of chip size) §	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**
Generation at production § SLC	**4G**	**4G**	**4G**	**8G**	**8G**	**8G**	**16G**	**16G**	**16G**
Generation at production § MLC	**8G**	**8G**	**8G**	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**
Functions per chip (Gbits) SLC	**4.29**	**4.29**	**4.29**	**8.59**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**
Functions per chip (Gbits) MLC	**8.59**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**
Chip size at production (mm^2)§ SLC	**144**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**
Chip size at production (mm^2)§ MLC	**144**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**
Gbits/cm^2 at production § SLC	**3E+09**	**4.2E+09**	**5.3E+09**	**6.7E+09**	**8.4E+09**	**1.1E+10**	**1.3E+10**	**1.7E+10**	**2.1E+10**
Gbits/cm^2 at production § MLC	**6E+09**	**8.4E+09**	**1.1E+10**	**1.3E+10**	**1.7E+10**	**2.1E+10**	**2.7E+10**	**3.4E+10**	**4.3E+10**

Table 1d DRAM and Flash Production Product Generations and Chip Size Model—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
DRAM Product Table							
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (mm^2)	**0.0048**	**0.0038**	**0.0030**	**0.0024**	**0.0019**	**0.0015**	**0.0012**
Cell array area at production (% of chip size) §	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Generation at production §	**8G**	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**
Functions per chip (Gbits)	**8.59**	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**
Chip size at production (mm^2)§	**74**	**117**	**93**	**74**	**117**	**93**	**74**
Gbits/cm2 at production §	**11.63**	**14.65**	**18.46**	**23.26**	**29.31**	**36.93**	**46.52**
Flash Product Table							
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**25.3**	**22.5**	**20.0**	**17.9**	**15.9**	**14.2**	**12.6**
Cell area factor [a]	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**	**4.0**
Cell area [Ca = af^2] (mm^2)	**0.003**	**0.002**	**0.002**	**0.001**	**0.001**	**0.001**	**0.001**
Cell array area at production (% of chip size) §	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**	**67.5%**
Generation at production § SLC	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**	**128G**
Generation at production § MLC	**64G**	**64G**	**64G**	**128G**	**128G**	**128G**	**256G**
Functions per chip (Gbits) SLC	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**	**137.44**
Functions per chip (Gbits) MLC	**68.72**	**68.72**	**68.72**	**137.44**	**137.44**	**137.44**	**274.88**
Chip size at production (mm^2)§ SLC	**128.3**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**	**128.3**
Chip size at production (mm^2)§ MLC	**128.3**	**101.8**	**80.8**	**128.3**	**101.8**	**80.8**	**128.3**
Gbits/cm^2 at production § SLC	**2.7E+10**	**3.4E+10**	**4.3E+10**	**5.4E+10**	**6.7E+10**	**8.5E+10**	**1.1E+11**
Gbits/cm^2 at production § MLC	**5.4E+10**	**6.7E+10**	**8.5E+10**	**1.1E+11**	**1.3E+11**	**1.7E+11**	**2.1E+11**

Notes for Tables 1c and 1d:

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe refer to Figures 9 and 10 for bit size and bits/chip trends:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Similarly to DRAM, the new Flash product model also targets an affordable (<145 mm^2) chip size and includes a doubling of functions (bits) per chip every technology cycle (three years after 2006) on an Inter-generation. Flash cells have reached a limit of the 4-design factor, so the reduction of the Flash single-level cell (SLC) size is paced by the uncontacted polysilicon (three-year cycle). However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size (refer to Figures 9 and 10).

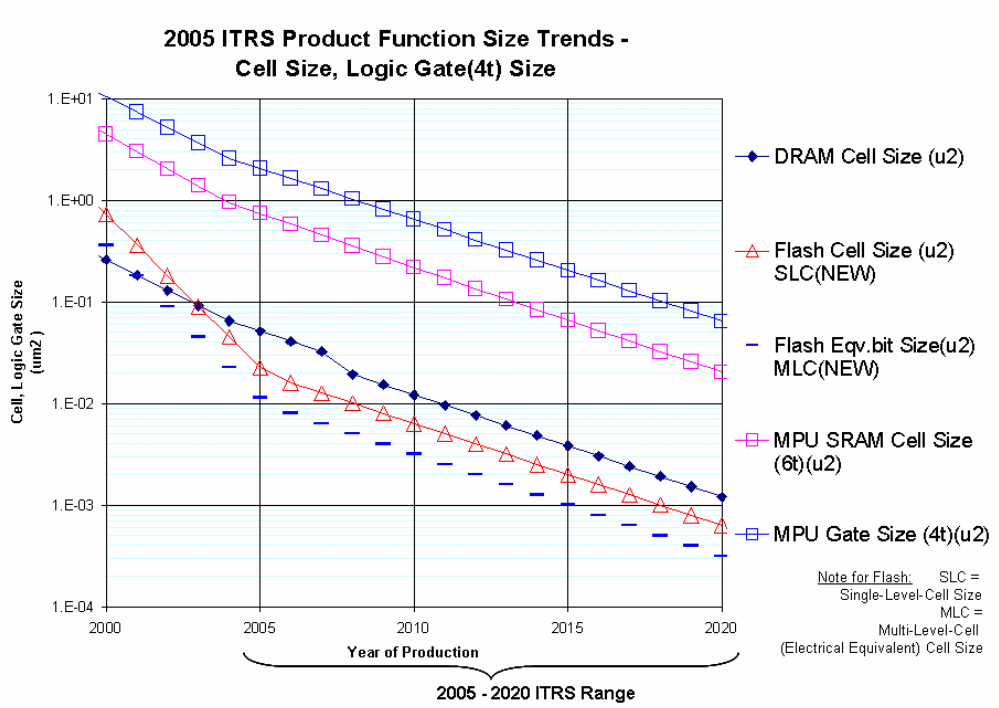


Figure 9 2005 ITRS Product Function Size Trends:
MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

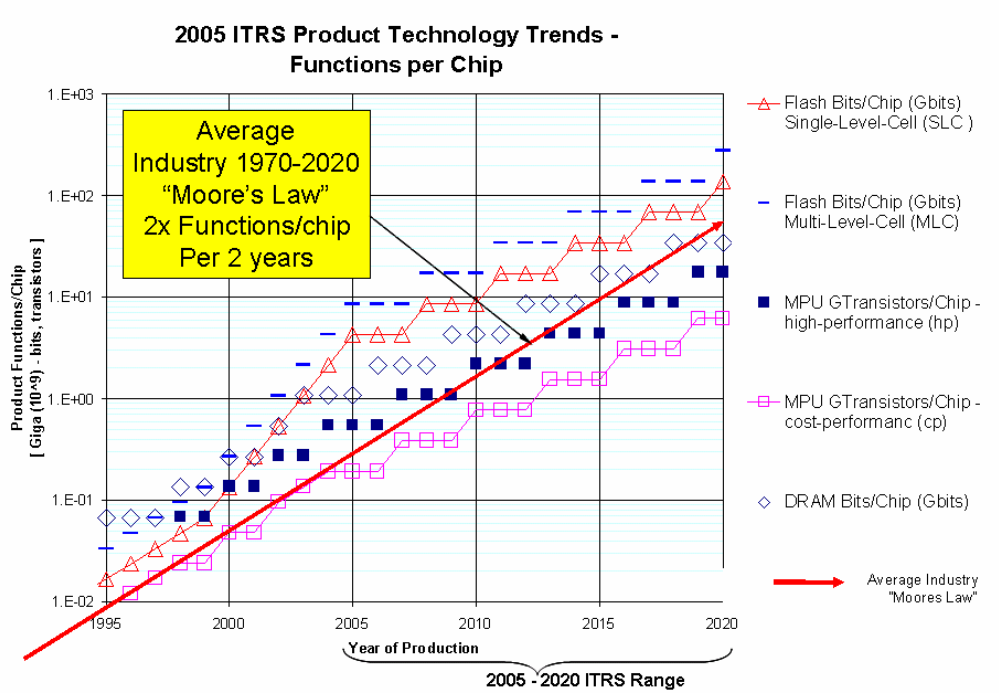


Figure 10 2005 ITRS Product Technology Trends:
Product Functions/Chip and Industry Average "Moore's Law" Trends

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Cell area factor [a]	**8**	**8**	**8**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (mm^2)	**0.051**	**0.041**	**0.032**	**0.019**	**0.015**	**0.012**	**0.010**	**0.008**	**0.006**
Cell array area at introduction (% of chip size) §	**72.95%**	**73.25%**	**73.52%**	**73.76%**	**73.97%**	**74.16%**	**74.30%**	**74.47%**	**74.61%**
Generation at introduction §	**8G**	**8G**	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**
Functions per chip (Gbits)	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**
Chip size at introduction (mm^2) §	**606**	**479**	**757**	**449**	**356**	**563**	**446**	**353**	**560**
Gbits/cm^2 at introduction §	**1.42**	**1.79**	**2.27**	**3.82**	**4.83**	**6.10**	**7.70**	**9.73**	**12.28**

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (mm^2)	**0.005**	**0.004**	**0.003**	**0.002**	**0.002**	**0.002**	**0.001**
Cell array area at introduction (% of chip size) §	**74.70%**	**74.83%**	**74.93%**	**75.00%**	**75.09%**	**75.18%**	**75.27%**
Generation at introduction §	**64G**	**64G**	**128G**	**128G**	**128G**	**256G**	**256G**
Functions per chip (Gbits)	**68.72**	**68.72**	**137.44**	**137.44**	**137.44**	**274.88**	**274.88**
Chip size at introduction (mm^2) §	**444**	**351**	**557**	**442**	**350**	**555**	**440**
Gbits/cm^2 at introduction §	**15.49**	**19.55**	**24.67**	**31.11**	**39.24**	**49.50**	**62.44**

Notes for Tables 1e and 1f:

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per three years (see ORTC Table 1c, d).

Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the Production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*51*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
SRAM Cell (6-transistor) Area factor ++	**115.6**	**113.7**	**111.9**	**110.4**	**109.0**	**107.8**	**106.7**	**105.7**	**104.8**
SRAM Cell (6-transistor) Area factor ++	**91.8**	**94.5**	**97.5**	**100.7**	**104.1**	**107.8**	**106.7**	**105.7**	**104.8**
Logic Gate (4-transistor) Area factor ++	**320**	**320**	**320**	**320**	**320**	**320**	**320**	**320**	**320**
Logic Gate (4-transistor) Area factor ++	**254**	**266**	**279**	**292**	**306**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**
SRAM Cell (6-transistor) Area ++	**0.74**	**0.58**	**0.45**	**0.35**	**0.28**	**0.22**	**0.17**	**0.13**	**0.11**
SRAM Cell (6-transistor) Area w/overhead ++	**1.2**	**0.93**	**0.73**	**0.57**	**0.45**	**0.35**	**0.27**	**0.22**	**0.17**
Logic Gate (4-transistor) Area ++	**2.06**	**1.63**	**1.30**	**1.03**	**0.82**	**0.65**	**0.51**	**0.41**	**0.32**
Logic Gate (4-transistor) Area w/overhead ++	**4.1**	**3.3**	**2.6**	**2.1**	**1.6**	**1.3**	**1.03**	**0.82**	**0.65**
Transistor density SRAM (Mtransistors/cm^2)	**504**	**646**	**827**	**1,057**	**1,348**	**1,718**	**2,187**	**2,781**	**3,532**
Transistor density logic (Mtransistors/cm^2)	**97**	**122**	**154**	**194**	**245**	**309**	**389**	**490**	**617**
*Generation at introduction **	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**	**p16c**	**p16c**
Functions per chip at introduction (million transistors [Mtransistors])	**386**	**386**	**386**	**773**	**773**	**773**	**1546**	**1546**	**1546**
Chip size at introduction (mm^2) ‡	**222**	**353**	**280**	**222**	**353**	**280**	**222**	**353**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**174**	**219**	**276**	**348**	**438**	**552**	**696**	**876**	**1,104**
*Generation at production **	**p04c**	**p04c**	**p07c**	**p07c**	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**
Functions per chip at production (million transistors [Mtransistors])	**193**	**193**	**386**	**386**	**386**	**773**	**773**	**773**	**1546**
Chip size at production (mm^2) §§	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**174**	**219**	**276**	**348**	**438**	**552**	**696**	**876**	**1,104**

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
SRAM Cell (6-transistor) Area factor ++	**104.1**	**103.4**	**102.8**	**102.2**	**101.7**	**101.3**	**100.9**
SRAM Cell (6-transistor) Area factor ++	**104.1**	**103.4**	**102.8**	**102.2**	**101.7**	**101.3**	**100.9**
Logic Gate (4-transistor) Area factor ++	**320**	**320**	**320**	**320**	**320**	**320**	**320**
Logic Gate (4-transistor) Area factor ++	**320**	**320**	**320**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**
SRAM Cell (6-transistor) Area ++	**0.084**	**0.066**	**0.052**	**0.041**	**0.032**	**0.026**	**0.020**
SRAM Cell (6-transistor) Area w/overhead ++	**0.13**	**0.106**	**0.083**	**0.066**	**0.052**	**0.041**	**0.032**
Logic Gate (4-transistor) Area ++	**0.26**	**0.20**	**0.16**	**0.13**	**0.10**	**0.08**	**0.06**
Logic Gate (4-transistor) Area w/overhead ++	**0.51**	**0.41**	**0.32**	**0.26**	**0.20**	**0.16**	**0.13**
Transistor density SRAM (Mtransistors/cm^2)	**4,484**	**5,687**	**7,208**	**9,130**	**11,558**	**14,625**	**18,497**
Transistor density logic (Mtransistors/cm^2)	**778**	**980**	**1,235**	**1,555**	**1,960**	**2,469**	**3,111**
*Generation at introduction **	**p16c**	**p19c**	**p19c**	**p19c**	**p22c**	**p22c**	**p22c**
Functions per chip at introduction (million transistors [Mtransistors])	**3092**	**3092**	**3092**	**6184**	**6184**	**6184**	**12368**
Chip size at introduction (mm^2) ‡	**222**	**353**	**280**	**222**	**353**	**280**	**222**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**1,391**	**1,753**	**2,209**	**2,783**	**3,506**	**4,417**	**5,565**
*Generation at production **	**p13c**	**p13c**	**p16c**	**p16c**	**p16c**	**p19c**	**p19c**
Functions per chip at production (million transistors [Mtransistors])	**1546**	**1546**	**3092**	**3092**	**3092**	**6184**	**6184**
Chip size at production (mm^2) §§	**111**	**88**	**140**	**111**	**88**	**140**	**111**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**1,391**	**1,753**	**2,209**	**2,783**	**3,506**	**4,417**	**5,565**

Notes for Tables 1g and 1h:
++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.
** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*
‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.
§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.
Refer to the Glossary for definitions.

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Logic (Low-volume Microprocessor) High-performance ‡									
Generation at Introduction	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**	**p16h**	**p16h**
Functions per chip at introduction (million transistors)	**1106**	**2212**	**2212**	**2212**	**4424**	**4424**	**4424**	**8848**	**8848**
Chip size at introduction (mm^2)	**492**	**781**	**620**	**492**	**781**	**620**	**492**	**781**	**620**
*Generation at production ***	**p04h**	**p04h**	**p07h**	**p07h**	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**
Functions per chip at production (million transistors)	**553**	**553**	**1106**	**1106**	**1106**	**2212**	**2212**	**2212**	**4424**
Chip size at production (mm^2) §§	**246**	**195**	**310**	**246**	**195**	**310**	**246**	**195**	**310**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**225**	**283**	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**
ASIC									
ASIC usable Mtransistors/cm^2 (auto layout)	**225**	**283**	**357**	**449**	**566**	**714**	**899**	**1,133**	**1,427**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**1,928**	**2,430**	**3,061**	**3,857**	**4,859**	**6,122**	**7,713**	**9,718**	**12,244**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at Introduction	**p16h**	**p19h**	**p19h**	**p19h**	**p22h**	**p22h**	**p22h**
Functions per chip at introduction (million transistors)	**8848**	**17696**	**17696**	**17696**	**35391**	**35391**	**35391**
Chip size at introduction (mm^2)	**492**	**781**	**620**	**492**	**781**	**620**	**492**
*Generation at production ***	**p13h**	**p13h**	**p16h**	**p16h**	**p16h**	**p19h**	**p19h**
Functions per chip at production (million transistors)	**4424**	**4424**	**8848**	**8848**	**8848**	**17696**	**17696**
Chip size at production (mm^2) §§	**246**	**195**	**310**	**246**	**195**	**310**	**246**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**1798**	**2265**	**2854**	**3596**	**4531**	**5708**	**7192**
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	**1,798**	**2,265**	**2,854**	**3,596**	**4,531**	**5,708**	**7,192**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**15,427**	**19,436**	**24,488**	**30,853**	**38,873**	**48,977**	**61,707**

Notes for Tables 1i and 1j:
** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*
‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000), and the combination of both SRAM and logic transistor functionality doubles every technology cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.
Refer to the Glossary for definitions.

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in ORTC Tables 1c, d, e, and f. (also refer to the Glossary for additional details).

Notably, the most recent survey data and publicly available announcements indicate that reduction rate of DRAM cell area factors for the 2005 ITRS models have again been slowed significantly. For example, the DRAM 7 and 7.5 design factors were eliminated in the near term, and the 5 factor was removed completely from the long term, leaving only the 6 factor beginning 2008 through the 2020 ITRS horizon. Furthermore the more aggressive 68% DRAM array efficiency targets from the 2003 ITRS have been slowed to 56% beginning 2008. This reduced DRAM product function density productivity requires that the DRAM "Moore's Law" bits per chip targets have been slowed to 2× every three years in both the near term and long term, pushing the 64 Gbit DRAM product beyond the ITRS year 2020 horizon (refer to Function Size and Functions per Chip in Figures 9 and 10).

In the new 2005 ORTC Flash product model, the function bit size historically accelerated the reduction of its design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. Due to rapid scaling cycles and design factor reductions (to 4), the Flash model chip size accelerated historically in function (bit size) area reduction. As a result, the Flash uncontacted polysilicon half-pitch crossed over DRAM stagger-contacted M1 half-pitch. However, it is believed by the Lithography TWG that leading-edge Flash manufacturing technology is still using comparable processing equipment as leading-edge DRAM, but Flash is not as limited to reduce the cell area, utilizing the same lithography capability as that used for DRAM products.

Flash single-level-cell (SLC) bit technology was thus able to drive quickly to a 76 nm uncontacted polysilicon half-pitch and a "4" design factor in 2005, resulting in a Flash bit cell area that is one-half the size of DRAM (see Figure 9, 2005 ITRS Product Function Size Trends), and allowing the production of a 144 mm^2 4 Gbit SLC product in 2005, when DRAM product was still at 1 Gbit (though the 1 Gbit DRAM has a smaller shrink chip size). Furthermore, Flash

technology is able to create an electrical doubling of bits in the same area, resulting in a virtual doubling of bits per chip to 8 Gbits in the 140 mm^2 affordable first production chip size range.

In the 2001 ITRS the Design ITWG improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including transistor design improvement factors. The original Design ITWG model notes that design improvements occur at a slow rate in SRAM transistors and very little in logic gate transistors. Almost all the "shrink" and density improvement comes from lithography-enabled interconnect half-pitch scaling alone.

The present 2005 ITRS MPU model "starts" in 2000/180 nm (versus original 1999/180 nm) chip size model is unchanged from the 2001 ITRS, and continues to reflect the additional competitive requirements for affordability and power management by targeting flat chip size trends for both high-performance MPUs (310 mm^2) and cost-performance MPUs (140 mm^2). Due to the MPU two-year-cycle half-pitch "catch-up phase" through the year 2004, the MPU products may be able to maintain flat chip sizes due to lithography improvements alone. However, after 2004, the inter-generation MPU chip size model, which is indexed to the ITRS technology cycles, can remain flat only by slowing the rate of on-chip transistors to double every technology generation. Refer to Function Size and Functions per Chip in Figures 9 and 10.

Due to the forecasted return to a three-year technology cycle, the present MPU chip-size model slows the Moore's Law rate of on-chip transistors to 2× every three years. In order to maintain a flat chip size target and also return to the historical doubling every two years of on-chip functionality (transistors), MPU chip and process designers must add additional design/process improvements to the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables 1g, h, i, and j.

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields ($26 \times 33 = 858$ mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG is dependent upon the individual memory and logic product chip size models to drive the requirements for both the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the most appropriate driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2005 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 704 mm^2 lithography field size, fitting at least one introduction-level chip size within that field size. The latest 2005 ITRS production-level DRAM chip size model (less than 140 mm^2 flat target) fits four die within a 572 mm^2 field.

The combination of technology generation scaling and cell design improvements (A-factor reduction) accomplishes that goal, while also maintaining a goal of doubling on-chip bits every two years. However, as mentioned in the product chip size model discussions above, the slowing of DRAM design improvements causes a requirement to add fewer on-chip bits to stay under the affordable chip size and lithography field size. This is accomplished in the present DRAM model by slowing the Moore's Law bits/chip rate to 2×/ three years, as required. The data targets for the DRAM model are included in Tables 1c, d, e, and f. The new Flash production chip size model is also included in those tables, and also targets the maximum affordable chip size to the 140 mm^2 range.

The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG ($26 \times 33 = 858$ mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 mm^2, reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue will be developed by the Lithography TWG in their chapter. The maximum Lithography field size is shown in Tables 2a and b.

The 2005 ITRS DRAM and MPU models, and the new Flash model depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for the 300 mm productivity boost will also increase in urgency, especially for leading-edge manufacturers, but the poor economy has created financial challenges and limited capital investment. The maximum substrate diameter in Tables 2a and b (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity beginning 2001. Also, the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter is not anticipated to be required until 2012 in the present Roadmap. However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter, or an equivalent processing platform, as a productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion requires the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work is being sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH. Most certainly, pre-competitive cooperation between the semiconductor supplier and manufacturer companies will be required to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development.

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Lithography Field Size									
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Lithography Field Size							
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**450**	**450**	**450**	**450**	**450**	**450**	**450**

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Tables 3a and b).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon chip pad-count numbers supplied by the Test ITWG, logic products (MPUs and high-performance ASICs) both approach 4–6K pads over the ITRS period. The MPU products are forecast to increase the total

number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
Total pads—MPU	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (1/3 of total pads)	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**
Power and ground pads—MPU (2/3 of total pads)	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**
Total pads—ASIC high-performance	**4,000**	**4,200**	**4,400**	**4,400**	**4,600**	**4,800**	**4,800**	**5,000**	**5,400**
Signal I/O pads—ASIC high-performance	**2,000**	**2,100**	**2,200**	**2,200**	**2,300**	**2,400**	**2,400**	**2,500**	**2,700**
Power and ground pads—ASIC high-performance (½ of total pads)	**2,000**	**2,100**	**2,200**	**2,200**	**2,300**	**2,400**	**2,400**	**2,500**	**2,700**
Number of Total Package Pins—Maximum [1]									
Microprocessor/controller, cost-performance	**550–900**	**550–990**	**600–1088**	**600–1198**	**660–1318**	**660–1450**	**720-1596**	**720–1754**	**800–1930**
Microprocessor/controller, high-performance	**900**	**990**	**1088**	**1198**	**1318**	**1450**	**1596**	**1754**	**1930**
ASIC (high-performance)	**3000**	**3180**	**3371**	**3573**	**3787**	**4015**	**4256**	**4511**	**4736**

Notes for Tables 3a and 3b:
[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by printed wiring board (PWB) technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
Total pads—MPU	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (1/3 of total pads)	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**	**1,024**
Power and ground pads—MPU (2/3 of total pads)	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**	**2,048**
Total pads—ASIC high-performance	**5,400**	**5,600**	**6,000**	**6,000**	**6,200**	**6,200**	**6,200**
Signal I/O pads—ASIC high-performance	**2,700**	**2,800**	**3,000**	**3,000**	**3,100**	**3,100**	**3,100**
Power and ground pads—ASIC high-performance (½ of total pads)	**2,700**	**2,800**	**3,000**	**3,000**	**3,100**	**3,100**	**3,100**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**800-2124**	**880–2336**	**880–2568**	**960-2824**	**960–3108**	**1050-3418**	**1050-3760**
Microprocessor/controller, high-performance	**2124**	**2336**	**2568**	**2824**	**3108**	**3418**	**3760**
ASIC (high-performance)	**4973**	**5222**	**5483**	**5757**	**6045**	**6347**	**6665**

Package pin count (Tables 3a and 3b) and cost-per-pin (Tables 4a and 4b), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow at an annual rate of approximately 10%, while the cost/pin decreases at 5%/year. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually at 5%/year (.95 cost/pin × 1.10 pins/year = 1.05 cost/year).

In the very competitive consumer electronics product environment, prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases at 10% while the average cost per pin decreases at only 5%, then the following will occur:

7. the average packaging share of total product cost will double over the 15-year roadmap period, and
8. the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip and through the use of multi-chip modules, bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational frequency will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Tables 4c and 4d, which include line items contributed by the Design and the Assembly and Packaging ITWGs to forecast the maximum on-chip and chip-to-board frequency trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant ($\kappa \sim 2–3$) will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip).

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Chip Pad Pitch (micron)									
Pad pitch—ball bond	35	35	30	30	25	25	25	20	20
Pad pitch—wedge bond	30	25	25	25	20	20	20	20	20
Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	130	120	110	100	90	90	90	90
Pad Pitch—2-row staggered-pitch (micron)	45	40	35	35	35	35	35	35	35
Pad Pitch—Three-tier-pitch pitch (micron)	45	40	35	35	35	35	35	35	35
Cost-Per-Pin									
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	.58–1.17	.57–1.11	.64–1.05	.63–1.00	.62–.96	0.61–.94	.60–.92	0.58–.90	0.57–.89
Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	.27–.50	.26–.49	.25–.48	.24–.47	.23–.46	.22–.45	.21–.43	.20–.42	.20–.41

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Chip Pad Pitch (micron)							
Pad pitch—ball bond	20	20	20	20	20	20	20
Pad pitch—wedge bond	20	20	20	20	20	20	20
Pad Pitch—area array flip-chip (cost-performance, high-performance)	80	80	80	80	70	70	70
Pad Pitch—2-row staggered-pitch (micron)	35	35	35	35	35	35	35
Pad Pitch—Three-tier-pitch pitch (micron)	35	35	35	35	35	35	35
Cost-Per-Pin							
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	0.56–.87	0.55–.85	0.54–.83	0.53–.81	0.52–.80	0.51–.79	0.50–.79
Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	.20–.39	.19–.38	.19–.37	.18–.36	.18–.35	.18–.34	.17–.34

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Chip Frequency (MHz)									
On-chip local clock [1]	**5,204**	**6,783**	**9,285**	**10,972**	**12,369**	**15,079**	**17,658**	**20,065**	**22,980**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[2]	**3,125**	**3,906**	**4,883**	**6,103**	**7,629**	**9,536**	**11,920**	**14,900**	**18,625**
Maximum number wiring levels—maximum [3]	**15**	**15**	**15**	**16**	**16**	**16**	**16**	**16**	**17**
Maximum number wiring levels—minimum [3]	**11**	**11**	**11**	**12**	**12**	**12**	**12**	**12**	**13**

Table 4d Performance and Package Chips: Frequency On-chip Wiring Levels—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Chip Frequency (MHz)							
On-chip local clock [1]	**28,356**	**33,403**	**39,683**	**45,535**	**53,207**	**62,443**	**73,122**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) [2]	**23,282**	**29,102**	**36,378**	**45,472**	**56,840**	**71,051**	**88,813**
Maximum number wiring levels—maximum [3]	**17**	**17**	**17**	**18**	**18**	**18**	**18**
Maximum number wiring levels—minimum [3]	**13**	**13**	**13**	**14**	**14**	**14**	**14**

Note for Tables 4c and 4d:

[1] The on-chip frequency is based on the fundamental transistor delay (defined by the PIDS TWG), and an assumed maximum number of 12 inverter delays beginning 2007; after 2007, the PIDS model fundamental reduction rate of ~ -14.7% for the transistor delay results in a ~17.2% growth trend of the on-chip frequency through 2020;

[2] The off-chip frequency, as defined by the Assembly and Packaging model, increases at a growth trend of 25% through 2017, then crosses over the on-chip frequency. The off-chip frequency is expected to increase only for a small number of high-speed pins that will be used in combination with a large number of lower speed pins.

[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Tables 5a and b. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 1 for DRAM and microprocessors. In addition, the data in the table are now reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield Enhancement chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity.

Table 5a Electrical Defects—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**3,517**	**2,216**	**2,791**	**3,516**	**2,215**	**2,791**	**3,516**	**2,215**	**2,791**
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	**1,757**	**2,214**	**1,395**	**1,757**	**2,214**	**1,395**	**1,757**	**2,214**	**1,395**
# Mask Levels—MPU	**33**	**33**	**33**	**35**	**35**	**35**	**35**	**35**	**37**
# Mask Levels—DRAM	**24**	**24**	**24**	**24**	**24**	**26**	**26**	**26**	**26**

Table 5b Electrical Defects—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**3,516**	**2,215**	**2,791**	**3,516**	**2,215**	**2,791**	**3,516**
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	**1,757**	**2,214**	**1,395**	**1,757**	**2,214**	**1,395**	**1,757**
# Mask Levels—MPU	**37**	**37**	**37**	**39**	**39**	**39**	**39**
# Mask Levels—DRAM	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Notes for Tables 5a and 5b:

D_0 — defect density

§ DRAM Model—Cell Area Factor (design/process improvement) targets are as follows:

1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Tables 6a and b, the value of the power supply voltage is now given as a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.5 volts are not expected to be achieved by high-performance processors until beyond 2018 (versus 2013 in the 2001 ITRS). The lowest V_{dd} target is now 0.5V in 2016 for the low operating power applications, a lower target than the 0.6V goal in the 2001 ITRS).

Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable battery operations (now designated as the "Harsh" application category by the Assembly and Packaging TWG). In all cases, total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

Table 6a Power Supply and Power Dissipation—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Power Supply Voltage (V)									
Vdd (high-performance)	**1.1**	**1.1**	**1.1**	**1.0**	**1.0**	**1.0**	**1.0**	**0.9**	**0.9**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.9**	**0.9**	**0.8**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.6**
Allowable Maximum Power [1]									
High-performance with heatsink (W)	**167**	**180**	**189**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.54**	**0.58**	**0.61**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**91**	**98**	**104**	**111**	**116**	**119**	**119**	**125**	**137**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.65**	**0.70**	**0.74**	**0.79**	**0.83**	**0.85**	**0.85**	**0.89**	**0.98**
Battery (W)—(low-cost/hand-held)	**2.8**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Power Supply Voltage (V)							
Vdd (high-performance)	**0.9**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.6**	**0.6**	**0.5**	**1.0**	**0.5**	**0.5**	**0.5**
Allowable Maximum Power [1]							
High-performance with heatsink (W)	**198**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**137**	**137**	**151**	**151**	**151**	**157**	**157**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.98**	**0.98**	**1.08**	**1.08**	**1.08**	**1.12**	**1.12**
Battery (W)—(low-cost/hand-held)	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**

[1] Power will be limited more by system level cooling and test constraints than packaging

COST

Tables 7a and 7b are dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm^2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, and now the 2005 ITRS models *all continue to use that model*, which results in 29% cost reduction of a function (bit, transistor, etc.). That rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2005 ITRS DRAM and MPU cost models continue to use the need for that 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that core cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 5.3 microcents for 8 Gbit DRAMs in 2003. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[4] A corresponding analysis conducted from published data for microprocessors yields similar results.[5] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2005 ITRS retains the original 2001 MPU chip size model. The Design ITWG updated the MPU model in the 2001 ITRS, based upon available data. At that time, the data indicated that logic transistor size is improving only at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to return to a three-year cycle after 2004. Therefore the transistors per MPU chip can double only every three years after 2004, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements are also continuing to slow, as reflected in the 2005 ITRS DRAM Chip Size Model targets. The "6" design factor, a 25% improvement over the "8" factor, is still expected to be implemented in 2008. However, the "5" design factor target, originally placed in 2016 in the 2003 ITRS, has been eliminated, slowing the long-range cost-reduction productivity. Furthermore, the TWG survey of DRAM manufacturers has indicated that the target for the cell array efficiency percentage will decrease to 56% after 2008. The combination of these model changes has further slowed the bit density increase rate of DRAM, so that the rate of bits per chip was slowed in the future to 2×/3 years, moving the 128 Gbit from the present ITRS horizon. These adjustments to the 2005 ITRS DRAM chip size model were required in order to preserve the constant first-production chip size target of less than 140 mm^2, which remains unchanged.

To compensate for slowing DRAM and MPU functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the "equivalent" productivity scaling benefits of chip, package, board, and system-level architecture and designs.

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[4] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

[5] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, December 9, 1996, 148–152.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially, though at a slower rate. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (Tables 4 a and 4b) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2005 ITRS. Further discussion is detailed in the Test chapter.

Table 7a Cost—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Affordable Cost per Function ++									
DRAM cost/bit at (packaged microcents) at samples/introduction	**5.3**	**3.7**	**2.6**	**1.9**	**1.3**	**0.93**	**0.66**	**0.46**	**0.33**
DRAM cost/bit at (packaged microcents) at production §	**1.9**	**1.4**	**0.96**	**0.68**	**0.48**	**0.34**	**0.24**	**0.17**	**0.12**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**44.0**	**31.1**	**22.0**	**15.6**	**11.0**	**7.8**	**5.5**	**3.9**	**2.8**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**26.6**	**18.8**	**13.3**	**9.4**	**6.7**	**4.7**	**3.3**	**2.4**	**1.7**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**24.4**	**17.2**	**12.2**	**8.6**	**6.1**	**4.3**	**3.0**	**2.2**	**1.5**

Table 7b Cost—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**0.23**	**0.16**	**0.12**	**0.08**	**0.06**	**0.04**	**0.03**
DRAM cost/bit at (packaged microcents) at production §	**0.08**	**0.06**	**0.04**	**0.03**	**0.02**	**0.01**	**0.01**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**1.9**	**1.4**	**0.97**	**0.69**	**0.49**	**0.34**	**0.24**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**1.2**	**0.83**	**0.59**	**0.42**	**0.29**	**0.21**	**0.15**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**1.1**	**0.76**	**0.54**	**0.38**	**0.27**	**0.19**	**0.13**

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon average selling prices (ASPs) available from various analyst reports less gross profit margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2007/8×; 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM cell design improvement factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c and d).

Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the Production-phase product chip size to meet the target flat-chip-size model. It can be observed in the latest table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology node cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2005 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1 Mbytes/2001). Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71x/cycle period) generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25 Mt cores in 2002) with a large (example 4 Mbyte/2002) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The present 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip has increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is required due to the new consensus 2005 ITRS forecast of cell-area-factor improvement to 6 by 2008, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2005 ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 3 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in

production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1 Gb/production, 4 G/introduction, plus 512 Mb/256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 ITRS, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size and will also have a "virtual area factor" that is half of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.