INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

FRONT END PROCESSES

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FRONT END PROCESSES

SCOPE

The Front End Processes (FEP) Roadmap focuses on future process requirements and potential solutions related to scaled field effect transistors (MOSFETs), DRAM storage capacitors, as well as Flash and ferroelectric RAM (FeRAM) devices. The purpose of this chapter is to define comprehensive future requirements and potential solutions for the key front end wafer fabrication process technologies and materials associated with these devices. Hence, this Roadmap encompasses the tools, and materials, as well as the unit and integrated processes starting with the silicon wafer substrate and extending through the contact silicidation processes. The following specific technology areas are covered: *starting materials, surface preparation, thermal/thin films, doping*, and *front end plasma etch* for MOSFETs, as well as processes and materials for *DRAM stack* and *trench capacitors, Flash memory gate structures*, *Phase-change memory,* and *FeRAM storage devices*.

A forecast of scaling-driven technology requirements and potential solutions is provided for each technology area. The forecasted requirements tables are model-based unless otherwise noted. The potential solutions identified serve to benchmark known examples of possible solutions, and are intended for other researchers and interested parties. They are not to be considered the only approaches. Indeed, innovative, *novel solutions* are sought, and are identified by red colored regions of the requirements tables.

Some FEP-related topics are presented in other sections of this Roadmap. The scaled device performance and structures' forecasts that drive FEP requirements are covered in the *Process Integration, Devices, and Structures (PIDS)* chapter. Issues for copper/low-κ dielectrics cleaning and surface preparation, plasma etch, and chemical mechanical polish (CMP) for trench isolation are found in the *Interconnect* chapter because of overlap with interconnect tool issues. The crosscut needs of FEP are covered in the following chapters: *Yield Enhancement*, *Metrology*, *Environment, Safety, & Health*, and *Modeling & Simulation*. FEP factory requirements are covered in the *Factory Integration* chapter.

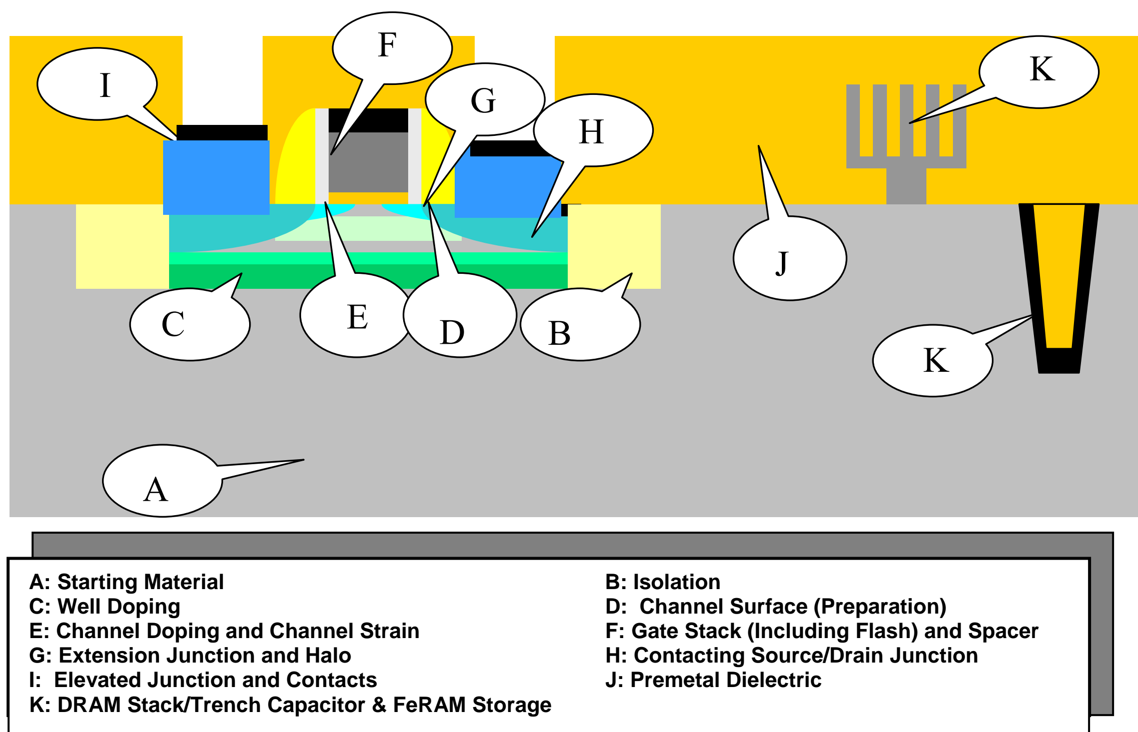


Figure 55 Front End Process Chapter Scope

DIFFICULT CHALLENGES

THE FRONT END PROCESSES GRAND CHALLENGE—

THE FEP RESPONSE TO THE ERA OF MATERIAL-LIMITED DEVICE SCALING

MOSFET scaling has been the primary means by which the semiconductor industry has achieved the historically unprecedented gains in productivity and performance quantified by Moore's Law. These gains have traditionally been paced by the development of new lithography tools, masks, photoresist materials, and critical dimension etch processes. In the past several years it has become clear that despite advances in these crucial process technologies and the resultant ability to produce ever-smaller feature sizes, front end process technologies have not kept pace, and scaled device performance has been compromised. The crux of this problem comes from the fact that the traditional transistor and capacitor formation materials, silicon, silicon dioxide, and polysilicon have been pushed to fundamental material limits and continued scaling has required the introduction of new materials. The current situation can be defined as "material-limited device scaling."

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures. In addition, the end of planar bulk CMOS is becoming visible within the next several years. As a consequence we must be prepared for the emergence of CMOS technology that uses non-conventional MOSFETs or alternatives such as planar fully depleted SOI devices and dual- or multi-gate devices either in a planar of vertical geometry. An overview of the device alternatives is presented in the *Emerging Research Devices chapter*. Many believe these may be needed as early as the year 2008. The challenges associated with these diverse new materials and the control of the physical interfaces associated with these materials constitutes the central theme of the FEP difficult challenges summarized in Table 66.

In no area is this issue more clear or urgent than in the MOSFET gate stack. Here, a new gate dielectric material having a higher dielectric constant is needed. This need was identified in the 1999 ITRS where it was linked to MOSFETs having gate lengths smaller than 65 nm, which were at that time expected to emerge in the year 2005. In the interim, the patterning technology for producing 65 nm gates has accelerated and these have been achieved in 2001. Combined with the extension of silicon oxynitride gate dielectric materials and the introduction of strain-enhanced-mobility channels, the need for high-κ has been delayed. Although promising high-κ candidate materials have been identified, fundamental performance and reliability issues, as well as issues with CMOS integration are still under investigation. It is doubtful that these materials will enter production before the year 2007. In the interim, oxynitride gate dielectric materials have nearly reached their leakage limits as dictated by power consumption; accordingly, only mobility enhancement and channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, are providing enhanced device performance. A re-optimization of the basic device design, done by the PIDS Technology Working Group (TWG), has capitalized on enhanced mobility channels to delay the need for high-κ dielectrics until the year 2008, at which time they will be needed by both low power and by high performance applications if off-state power consumption expectations are to be met. Looking beyond the gate dielectric, the depletion layers that exist in the doped polysilicon gate material become increasingly onerous as planar devices are scaled into the deep submicron region with the result that dual metal gates, having appropriate work functions, are also needed in 2008 to replace the dual doped polysilicon gates, currently the mainstay of CMOS technology.

Table 66a Front End Processes Difficult Challenges—Near-term Years

Difficult Challenges ≥ 32 nm	*Summary of Issues*
New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm EOT for high-performance MOSFETs, consistent with device reliability requirements Control of boron penetration from doped polysilicon gate electrodes while minimizing depletion of dual-doped polysilicon electrodes Introduction and process integration of high-κ gate stack materials and processes for high-performance, low operating and low standby power MOSFETs CMOS integration of enhanced channel mobility in both NMOS and PMOS devices, using local and global strained layers Introduction of dual metal gate electrodes with appropriate work function Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20–50 nm Removal of high-κ dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is considerably smaller than the feature size printed in the resist, while maintaining <12% overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control Maintenance of CD and profile control throughout the transition to new gate stack materials and processes CD and etch metrology Site flatness to ensure effective lithographic printing
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal Integration and scaling of FeRAM ferroelectric materials Scaling of Flash interpoly and tunnel dielectric layers may require high-κ Limited temperature stability of high-κ and ferroelectric materials challenges CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface Interface control for DRAM capacitor structures Maintenance of surface and interface integrity through full-flow CMOS processing Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces Measurement of back surface particles at/near edge wafer edge (including bevel) has no solution Measurement and understanding of clustering of particles needs significant data to define future specification Little information associating back surface particles and the effect on yield
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance ($=V_{dd}/I_{on}$) Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes Formation of continuous self-aligned silicide contacts over shallow source and drain regions. Formation of elevated junctions and silicides on FDSOI wafers Metrology issues associated with 2D dopant profiling

Table 66b Front End Processes Difficult Challenges—Long-term Years

Difficult Challenges < 32 nm	*Summary of Issues*
Continued scaling of planar CMOS devices	Higher κ gate dielectric materials including temperature constraints Metal gate electrodes with appropriate work function Sheet resistance of clad junctions CD and L_{eff} control Chemical, electrical, and structural characterization
Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-κ materials and metal gates on standard CMOS) Selection and characterization of optimum device types CMOS integration with other devices, including planar MOSFETs Introduction, characterization, and production hardening of new FEP unit processes Device and FEP process metrology Increased funding of long term research Introduction of strained silicon in the structural configuration for advanced non-classical CMOS
Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2005	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon If 450 mm wafers are to become available for production in 2012 as currently forecasted, wafer manufacturing is already behind schedule and must be implemented in 2005–2006 Enhanced coordination is required amongst Starting Materials, Factory Integration, Yield Enhancement and the IRC to more effectively assess the anticipated onset of 450 mm use
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$ Further scaling of Flash memory interpoly and tunnel oxide thickness FeRAM storage cell scaling Introduction of new memory types and storage concepts (Candidates—MRAM, phase-change memory for 2010, and single electron, molecular, nano-floating products beyond 2010)
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

Near-term measures such as the use of strained silicon channels are expected to provide needed boosts to device speed, but ultimately, scaling is expected to require the replacement of planar CMOS devices with non-standard dual gate devices including fully depleted planar devices. The introduction of these devices will require the replacement of bulk silicon substrates with ultra-thin, silicon-on-insulator (SOI) substrates and double- or multi-gate devices. The transition from extended bulk CMOS to non-classical device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time—some manufacturers choosing to make the transition to non-classical devices earlier, while others emphasize extensions of bulk technology.

High-κ materials are now in use for both stacked and trench DRAM capacitors. DRAM stacked capacitors will soon require new metal-insulator-metal structures with trench capacitors following by a few years. It is expected that high-κ materials will be required for the Flash memory interpoly and tunnel dielectric layers. In the memory area it is also expected that FeRAM and MRAM will make a significant commercial appearance where ferroelectric and ferromagnetic storage materials would be used. The introduction of these diverse materials into the manufacturing mainstream is viewed as important, difficult challenges. In addition, phase-change memory (PCM) devices are also making a commercial appearance.

In the starting wafer area, it is expected that alternatives to bulk silicon such as various strained silicon alternatives on bulk, as well as silicon-on-insulator substrates will proliferate. These all imply FEP process architecture changes. An important difficult challenge expected to emerge within the Roadmap horizon is the need for the next generation 450 mm silicon substrate. Here, it is questionable whether the incumbent techniques for wafer preparation can be cost-effectively scaled to the next generation. It is also questionable whether this substrate will be bulk silicon or SOI and whether strained silicon will be the required active layer material. The search for potential substrate alternatives presents an important research need that must commence immediately, if this new substrate material is to be ready for device manufacture in the year 2012.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials. In addition, scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Also, the scaled and new device structures that will be introduced will become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed. DRAM stacked and trench storage capacitor structures will show increasing aspect ratios making sidewall contamination removal increasingly difficult.

The etching processes used to form the critical dimension features such as MOSFET gates, and DRAM word and bit lines continue to pose difficult challenges in terms of CD and line profile shape control. These problems are expected to become more difficult as etch techniques are increasingly employed to produce feature sizes that are smaller than those printed in the photoresist. As noted in the section on etching, close collaboration between the FEP, Lithography, PIDS, and Design TWGs have resulted in a larger printed gate and increased etch bias to achieve the same physical gate length. In addition, physical gate length variation was increased to 12% and reallocated between etch and lithography to push out this “red brick wall” for a few years. The introduction of new materials in the gate stack is expected to change the nature of these challenges.

The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. In addition to the scaling imposed need for producing very shallow highly activated junctions, the limited thermal stability of most high-κ materials is expected to place new boundaries on thermal budgets associated with dopant activation. In a worst-case scenario, the introduction of these materials could have a significant impact on the overall CMOS process architecture.

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

STARTING MATERIALS

Technology Requirements—Tables 67a and b forecast trends for starting wafers produced by silicon wafer manufacturers that are intended for use in the manufacture of both high density memories such as DRAMs and high-performance MPUs and ASICs. These requirements include parameters common to all wafers plus parameters specific to polished, epitaxial, and SOI wafers. Fundamental barriers presently limit the rate of cost-effective improvement in wafer characteristics such as localized light scatterers (LLS) defect densities, site flatness values, and edge exclusion dimensions. These barriers include the capability and throughput limitations of metrology tools, as well as wafer manufacturing cost and yield issues fundamental to the crystal-pulling process and subsequent wafer finishing operations. Accordingly, a methodology has been introduced to display not only the ability of the wafer supplier to meet the parameter trends in Tables 67a and 67b, but to also display the metrology tool readiness. For this reason, the wafer parameter trend table cells have been annotated with the silicon supplier criticality color code on the left-hand side of each cell and the metrology tool readiness color code depicted on the right-hand side. The marking system and meanings are shown in the Tables for both DRAM and high-performance MPUs.

Wafer Types—For the device types included in the scope of the ITRS, starting materials selection historically involved the choice of either polished Czochralski (CZ) or epitaxial silicon wafers. Recently, silicon-on-insulator (SOI) wafers have become more than a niche technology, although the total number of SOI wafers shipped is still small compared to polished and epi wafers. The opportunity for SOI wafers to be used in mainstream high-volume applications is being driven by improved high-frequency logic performance and reduced power consumption, as well as enhanced device performance via unique device configurations such as multiple-gate structures. In some cases process flow simplification is also achieved. The selection of wafer type is based strongly on performance versus cost.

Commodity devices such as DRAM are commonly manufactured on lower cost CZ polished wafers. The elimination of “crystal originated pits” (COP) in CZ polished wafers is increasingly required to avoid interference with inline inspections used for defect reduction. High-performance logic ICs are generally manufactured on more costly epitaxial

wafers (compared to polished CZ wafers) because their use has facilitated the achievement of greater-robustness (e.g., soft error immunity and latch-up suppression capability). This latter capability may no longer be as critical due to the implementation of shallow trench isolation (STI) and the development of alternate doping means for achieving latch-up suppression. Historically, most wafers used for MPU and ASIC production were p/p+ wafers (lightly doped epi on a heavily doped substrate). Recently, p/p- epi wafers have been used for many applications. Annealed wafers were introduced in the early 1990s as an alternative means to provide a silicon wafer with a COP free surface and are now used for many leading edge device applications. Annealing occurs in either hydrogen or argon ambients at high temperatures. COPs can also be controlled by appropriately engineered CZ growth methodologies. For the purpose of the Starting Materials tables presented here, annealed wafers and "defect engineered CZ" are both considered forms of polished CZ wafers. This wide variety of starting materials will likely continue into the foreseeable future and is the reason for inclusion of polished, epitaxial, and SOI wafers in Tables 67a and b. Emerging materials that may further augment the variety of starting materials are discussed later in this document.

Parameter Values—The wafer requirements have been selected to ensure that in any given year each parameter value contributes no more than 1% to leading-edge chip yield loss. The values in the tables are generally, but not exclusively, derived from probabilistic yield-defect models. These models take into account leading-edge technology parameters such as critical dimension (CD)—taken as the DRAM half-pitch (that is, the technology generation)—bit density, transistor density, and chip size. The validity of these derived values is limited by the sometimes questionable accuracy and predictability of the underlying models. With the onset of nanometer device dimensions for both the gate dielectric equivalent oxide thickness (EOT) and the device physical channel length, compliance with these model-based values can be very costly and, in some cases, requires re-examination. For this reason, detailed re-assessment of the costs incurred versus the value derived from achieving compliance often suggests limiting the scope of these models via appropriate truncation.

Table 67a Starting Materials Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
DRAM Total Chip Area (mm^2)	**88**	**139**	**110**	**74**	**117**	**93**	**74**	**117**	**93**
DRAM Active Transistor Area (mm^2)	**23.1**	**36.2**	**29.5**	**23.1**	**36.4**	**29.1**	**23.1**	**36.0**	**29.1**
MPU High-Performance Total Chip Area (mm^2)	**246**	**195**	**310**	**246**	**195**	**310**	**246**	**195**	**310**
MPU High-Performance Active Transistor Area (mm2)	**25.1**	**20.0**	**31.7**	**25.1**	**20.0**	**31.7**	**25.1**	**20.0**	**31.7**
*General Characteristics * (99% Chip Yield) [A, B, C]*									
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**
Edge exclusion (mm)	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**
Front surface particle size (nm), latex sphere equivalent [D] [E]	≥90	≥90	≥90	≥90	≥65	≥65	≥65	≥45	≥45
Particles (cm^{-2})	**≤0.35**	**≤0.17**	**≤0.18**	**≤0.17**	**≤0.16**	**≤0.17**	**≤0.17**	**≤0.17**	**≤0.17**
Particles (#/wafer)	**≤238**	**≤116**	**≤123**	**≤120**	**≤113**	**≤115**	**≤115**	**≤265**	**≤271**
Site flatness (nm), SFQR 26 mm × 8 mm site size [F, R]	**≤80**	**≤70**	**≤65**	**≤57**	**≤50**	**≤45**	**≤40**	**≤35**	**≤32**
Nanotopography, p-v, 2 mm diameter analysis area [Q]	**≤20**	**≤18**	**≤16**	**≤14**	**≤13**	**≤11**	**≤10**	**≤9**	**≤8**
*Polished Wafer * (99% Chip Yield)*									
The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D, E]									
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [G]	**≤1.39**	**≤1.15**	**≤1.03**	**≤0.85**	**≤0.71**	**≤0.81**	**≤0.52**	**≤0.43**	**≤0.37**
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [G]	**≤0.37**	**≤0.32**	**≤0.27**	**≤0.23**	**≤0.19**	**≤0.16**	**≤0.14**	**≤0.12**	**≤0.10**
*Epitaxial Wafer * (99% Chip Yield)*									
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Structural Defects, Small Structural Defects and Particles (see General Characteristics) [H, I]									
Large structural epi defects (DRAM) (cm^{-2}) [J]	**≤0.011**	**≤0.007**	**≤0.009**	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	**≤0.009**	**≤0.011**
Large structural epi defects (MPU) (cm^{-2}) [J]	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.005**	**≤0.003**
Small structural epi defects (DRAM) (cm^{-2}) [K]	**≤0.023**	**≤0.014**	**≤0.018**	**≤0.027**	**≤0.017**	**≤0.022**	**≤0.027**	**≤0.017**	**≤0.022**
Small structural epi defects (MPU) (cm^{-2}) [K]	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	**≤0.010**	**≤0.006**
Silicon-On-Insulator Wafer (99% Chip Yield)[R]*									
Edge exclusion (mm) ***	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) [L]	**58–100**	**53–91**	**48–83**	**44–76**	**40–70**	**37–65**	**34–60**	**31–45**	**29–42**
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [M]	**20–36**	**19–34**	**18–33**	**16–30**	**15–29**	**15–28**	**14–27**	**13–15**	**13–15**
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [N]	**48–80**	**42–70**	**38–64**	**34–56**	**30–50**	**26–44**	**24–40**	**22–36**	**18–32**
D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [O]	**≤0.011**	**≤0.007**	**≤0.009**	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	**≤0.014**	**≤0.012**
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [O]	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.004**	**≤0.003**
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [P]	**≤0.218**	**≤0.139**	**≤0.170**	**≤0.218**	**≤0.138**	**≤0.173**	**≤0.218**	**≤0.139**	**≤0.173**
D_{SASOI}, Small area SOI wafer defects (MPU) (cm^{-2}) [P]	**≤0.200**	**≤0.252**	**≤0.159**	**≤0.200**	**≤0.252**	**≤0.159**	**≤0.200**	**≤0.252**	**≤0.159**

** Parameters define limit values, independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time"; other parameter values are most likely near median value, thereby insuring total yield for all parameters is at least 99%.*
*** Values expressed in a per wafer format are calculated assuming the maximum stated wafer diameter, although that diameter likely may not be the predominant one for the corresponding technology generation. Although 450 mm is colored yellow indicating manufacturable solutions are know, it could have easily been colored red, because there has been no acceptable economic solution for funding identified by the industry.*
**** Edge exclusion is repeated in the Silicon on Insulator Wafer section because of inherent limitations associated with certain SOI wafer production techniques that differ from polished and epitaxial wafer edge exclusion capabilities.*

Meaning and Color Coding of Left Box	***Meaning and Color Coding of Right Box***
Technology Requirements Value and Supplier Manufacturing Capability by Color	**Metrology Readiness Capability by Color**
Manufacturable solutions exist, and are being optimized	*Manufacturable solutions exist, and are being optimized*
Manufacturable solutions are known	*Manufacturable solutions are known*
Manufacturable solutions are NOT known	***Manufacturable solutions are NOT known***

Notes for Table 67a and b

[A] Surface metals are empirically grouped into three classes[1, 2]: (a) Mobile metals that may be easily cleaned such as Na and K and may be modeled by taking the flat-band shift of a capacitance-voltage (CV) test approximately 50 mV for a representative 1 nm EOT; (b) metals that dissolve in silicon or form silicides such as Fe, Ni, Cu, Cr, Co, Al, Zn; and (c) major gate-oxide-integrity (GOI) killers such as Ca. Each of these metals is taken at a maximum value of $1 \times 10^{10}/cm^2$ for all subsequent technology generations. The surface concentration of carbon atoms after cleaning is based on the assumption that a 10% (7.3×10^{13} atoms/cm^2) carbon atom coverage on a bare silicon (100) surface can be tolerated during device fabrication. Organics/polymers are therefore modeled approximately 0.1 of a monolayer, $\leq 1 \times 10^{14}$C atoms/cm^2. Surface organic levels are highly dependent on wafer packaging, on hydrophobic or hydrophilic wafer surface conditions, and on wafer storage conditions such as temperature, time and ambient.

Total bulk Fe consistent with recombination lifetime, τ_r, as measured by the SPV technique (for lightly doped p-type material) at low injection level is held at $1 \times 10^{10}/cm^3$ for all subsequent technology generations.[3] Note that the bulk Fe concentration (at/cm_3) cannot be converted to surface concentration (at/cm^2) via wafer thickness. Recombination lifetime $\tau_r = (L^2)/D_n$, where L = minority-carrier diffusion length and D_n = minority-carrier diffusion coefficient at 27°C.[4] The diffusion length is taken equal to the wafer thickness, resulting in a τ_r value of 350 µsec. The allowable lifetime is doubled to ensure a sufficient safety factor, resulting in a final value of 700 µsec. Appropriate technique(s) to control, stabilize and passivate surface effects is required, depending on the technique (SPV, PCD, etc.), especially for a bulk lifetime greater than 20 µsec. For any technique other than SPV, the injection level must be noted. No oxygen precipitation in sample, no back-side mechanical damage, and resistivity of 5–20 Ohm-cm recommended.
[B] Instrumentation choice, target values, and spatial frequency range (scan size) for front-surface microroughness are selected based on application. Power spectral density analysis is recommended to utilize full accessible range of instruments. A typical value for polished wafers is ≤ 0.1 nm (RMS) for all CD generations. Epitaxial, annealed and SOI wafers have values that are typically higher than polished wafers while still meeting the user's requirement.
[C] The oxygen concentration may be specified depending on the particulars of the IC user based on IC process requirements and is generally in the range of 18–31 ppma (SEMI M44-0702, refer to ASTM F121-79).[5] With advanced crystal growth technologies, bulk micro defects (BMDs) can be achieved independent of the interstitial oxygen concentration. The importance of BMDs for gettering has recently again been emphasized and may be especially important in those IC fabrication cases with low thermal budgets.[6] Co-doping techniques (such as nitrogen and carbon) can be used to enhance oxygen precipitation so may be particularly well suited for low thermal budget device processes. Additionally, certain growth methods coupled with heat treatments can also enhance the precipitation of oxygen. Not all device processes, however, require the presence of BMDs. BMDs for internally gettered polished wafers may be generically taken as greater than approximately $1 \times 10^8/cm^3$ after IC processing. BMD density is measured using ASTM F-1239.
[D] Critical front surface particle size = K_1F, [K_1=1] where F is the DRAM half-pitch and is used to calculate required particle densities at the given technology generation. Particle sizes reported in Tables 67a and b are held constant for several generations before being reduced, due to metrology capability. Particle densities are extracted from the conventional Maly Yield Equation [7] {$Y = \exp[-(D_P R_P) A_{eff}]$, where A_{eff}, is the effective chip area $A_{eff}=2.5*F^2T+(1-aF^2T/A_{chip})A_{chip}*0.18$, "a" is the DRAM cell fill factor (see Table 70a) and T = number of transistors or bits/chip per technology generation}(K_1F/PS) [2], where PS is the particle size reported in the table for the respective technology generation. This method therefore applies the square law to calculate the predicted densities for the respective reported particle sizes, using the density for the critical front surface particle size obtained from the Maly Yield Equation as the reference density at each respective technology generation. The kill factor R_P is assumed to be 0.2, although the kill factor may be very dependent upon the specifics of the DRAM fab. The relationship between actual defect size and associated LSE (latex sphere equivalent) size depends on defect type and scanner geometry. The current particle size threshold capability for SOI wafers is approximately 100 nm, due to the altered response in the optical metrology tools, compared to polished or epitaxial wafers.*

[E] Detailed back-surface particle information is not included in Table 67, since, in practice, lithography concerns are being met by identifying these defects visually. This perhaps suggests that only large defects are of impact. If desired, the calculations may be made using the following model for back-surface particle size and density. The front-surface height elevation, H, due to a back-surface particle of size, D, under a back-surface film of thickness, T, and a wafer thickness, W, may be expressed as [(xD +xT +W) – (T + W)], which may be reduced to [(xD) – (1-x)T], where x = 0.6 is the compression of the particle and back-surface film due to the pressure of the chuck on the wafer. Assuming a front-surface elevation of 2(CD) results in a 100% lithographic printing failure, the back-surface particle size is expressed as: D = [(2/0.6) (F) + (0.4/0.6) (T)], where F and T are expressed in nm. In this model, T may be set equal to 100 nm, for example. Back-surface particles modeled for 99% yield: $Y = exp(-D_P R_P A_{eff})$ [7]. $R_P = 1.0$, $A_{eff} = A_{chip} \times 0.03 \times 0.8$, where 0.03 corresponds to 3% of the chip area touching the chuck and 0.8 corresponds to 80% of the effective chip area that is degraded by effects of the back-surface particle on the front-surface de-focus effect. D_p, then, represents the density of defects allowable in visible inspection for backside particles. The equation for the "killer" backside particle diameter strongly depends on two assumptions that are process dependent. The first is that a focal plane excursion of 2 CD is required for a 100% assured printing failure. Although a process window this wide may exist in many cases, some tightly specified exposures maybe less tolerant to focal plane deviations. This would lead to a smaller particle becoming a backside killer. The second assumption is that the particles and film are both compressed to 60% of their original dimension. This assumption might not be true if the particle were made of a material much harder than the film or the particle was similar in hardness to silicon and there was no backside film (T=0). Either of these circumstances allows a smaller particle to become a possible backside killer. The backside yield equation assumes that the entire chip is killed by a back-surface particle generating a front-surface focal plane deviation during lithography (the critical particle diameter is that value accordingly used in the equation, or larger). This occurs because a particle with diameter much smaller than the thickness of the wafer may create a bulge on the front surface up to 10 mm in diameter, so a significant portion of the field is out of focus, and the chip does not yield. A mitigating circumstance occurs if the particle is near the die edge, however, since the bulge at the die edge will tend to create only an apparent local tilt in the field that can be accommodated by a scanning stepper leveling system. This gives rise to the 80% effective degraded area.

[F] The metric for site flatness should be matched to the type of exposure equipment used in leading edge applications, which implies scanning steppers for critical levels. While SFSR may be the most appropriate metric, it has failed to gain appreciable support in the industry. Historical reference to SFQR remains strong and it appears inevitable that this metric will continue to be used in the future. To more closely emulate practical experience of the scanning stepper, the effective site size for local site flatness is being modified to 26 mm $\times$ 8 mm accordingly. Full-field steppers with square fields (nominally 22 $\times$ 22 mm) may still be utilized for non-critical levels although these are increasingly being phased out. In either case, the metric value is approximately equal to F for dense lines (DRAM half pitch). Partial sites should be included. Also note that flatness metrology requires sufficient spatial resolution to capture topographical features relevant for each technology generation.

[G] OSF density empirically modeled by $K_3 (F)^{1.42}$; F in nm; $K_3 = 2.75 \times 10^{-3}$.[8] The utilization of the OSF density relation by extension into technology generation regimes, not envisioned in the original experimental analysis, will require re-assessment. Test at 1100°C, 1 hour wet oxidation, strip oxide/etch;OSF is more difficult to control in n-type material.

[H] Other epitaxial defects such as hillocks and mounds should also be accounted for, but an appropriate yield model is not available. Accurate segregation based upon defect morphology is also not generally available with today's metrology.

[I] Desired epitaxial layer thickness tolerance is ± 4% for a 2 to 10 mm center-point epitaxial layer thickness target value but may be affected on p/p^+ structures due to lack of autodoping suppression via backside film deposition, resulting from incompatibility with 300 mm wafers. In the case of p/p^- epi, the minimum epi layer thickness is designed to avoid the possible influence of bulk grown-in defects such as COPs; this consideration is less critical for p/p^+ where the COPs are significantly reduced in the p^+ substrate compared to p^-.

[J] Large structural epi defects (large area defects >1 μm LSE signal) modeled at 99% yield where $Y = exp(-D_{LAD} R_{LAD} A_{chip})$,[6] where $R_{LAD} = 1$ and A_{chip} applies to DRAM and high-performance MPU as appropriate. METROLOGY NOTE: Many current generation scanning surface inspection systems (SSIS) cannot reliably size surface features with LSE signals greater than about 0.5μm due to the light scattering characteristics of these large structural epi defects and the optical design of the tool. Further, a metrology gap clearly exists since production worthy tools are not available that can separate large structural epi defects from other features like large particles as well as identify and count epitaxial stacking faults.

[K] Small structural epi defects (≤ 1μm LSE signal) modeled at 99% yield where $Y = exp(-D_{SF} R_{SF} A_{chip})$[6] where $R_{SF} = 0.5$ and A_{chip} applies to DRAM and high-performance MPU as appropriate. Starting Materials uses the DRAM at production and the MPU high-performance MPU areas. METROLOGY NOTE: A metrology gap clearly exists since production worthy tools are not available that can identify and count small structural epi defects.

[L] The silicon final device layer thickness (partially depleted) is obtained by 2 $\times$ MPU physical gate length (with a range in nominal values of ± 25%). Range of target value refers to the center point measurement with uniformity to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to Si consumption during device fabrication. In the table, the starting material layer thickness is shown. For years 2003 to 2009 it is obtained by adding 10 nm to the lower value in the range and 20 nm to the higher value in the range. After 2009, 10 nm is added to both values in the range in order to translate the device thickness into the starting material thickness. Si loss depends on processing conditions used—it is assumed here that processing parameters are controlled more tightly after 2009. It should be noted that partially depleted silicon on insulator solutions are shown for all years but may generally not be compatible with more aggressively scaled technology generations.

[M] The silicon final device thickness (fully depleted) is obtained by 0.4 $\times$ MPU physical gate length prior to 2008, 0.35 x MPU physical gate length 2008 to 2011, 0.3 x MPU physical gate length at 2012 and thereafter (with a range in nominal values of ± 25%). Range of target value refers to the center point measurement with uniformity to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to consumption during device fabrication. In the table the starting material layer thickness is shown. For years 2003 to 2009 it is obtained by adding 10 nm to the lower value in the range and 20 nm to the higher value in the range. After 2009, 10 nm is added to both values in the range in order to translate the device thickness into the starting material thickness. Si loss depends on processing conditions used—it is assumed here that processing parameters are controlled more tightly after 2009.

[N] The BOX thickness for fully depleted devices is taken as the 2 $\times$ MPU physical gate length. BOX scales with gate length to help to control short channel effects and heat dissipation. Range in nominal target value of ± 25% allows for trade-off between the BOX and silicon thickness to control short channel effects in the fully depleted SOI devices. NOTE: For partially depleted SOI devices, the BOX thickness has less of a direct impact on device parameters. Considerations of BOX capacitance, circuit heat dissipation, gettering, BOX electrical integrity, SOI wafer manufacturing capabilities, wafer quality and wafer cost have driven the choice of the BOX thickness values. The BOX thickness is expected to remain between 100–200 nm for the timeframe of partially depleted SOI devices.

[O] Large area SOI (LASOI) wafer defects with yield of 99%; $Y = exp(-D_{LASOI} R_{LASOI} A_{chip})$,[6] D_{LASOI} = LASOI defect density, R_{LASOI} =1.0 (best present estimate).

[P] Small area SOI (SASOI) wafer defects with yield of 99%; $Y = exp(-D_{SASOI} R_{SASOI} A_{eff})$,[6] D_{SASOI} = SASOI defect density, R_{SASOI} = 0.2 (best present estimate). Sources of SASOI can include COPs, metal silicides, or local SiO_2 islands in the top silicon layer. These SASOI defects may also be detected by localized light scattering (LLS) measurements.[9, 10, 11]
[Q] Peak-to-valley threshold, 2 mm diameter analysis area. Maximum p-v reading taken as CD/4, based on extrapolation of wafer supplier process capability for 180–90 nm technology generations, plus published data on linewidth distortion for sub-100 nm critical dimensions.
[R] The magnitude of within-wafer variation of various wafer parameters changes over different length scales, depending on the nature of the mechanisms that produce them. The impact on subsequent device manufacturing caused by these variations, which occur at different spatial wavelengths, also depends on the nature of the fab processes and resulting devices. For instance, parameters governed by gas flow and temperature gradient variations, such as CVD layer thickness, typically vary appreciably only over fairly long distances, of the order of millimeters to centimeters. It is often adequate to measure such slowly varying parameters at only a modest number of locations on the wafer, using a metrology tool with a fairly low spatial resolution, in order to control such processes. Other parameters, such as wafer surface topography, vary on multiple length scales with different impacts in the fab. At very large length scale (tens of centimeters), wafer surface height variations are many microns in magnitude (e.g. bow and warp), and can affect various mechanical properties of the wafer. At length scales on the order of one centimeter, the surface variations are fractions of a micron in height. These variations (i.e. site flatness) generally are not critical to mechanical shape of the wafer, but are vital to depth of focus in lithography. At still smaller length scales of a few millimeters or less, the surface height variations are on the order of tens of nanometers high. They do not cause focus failures in lithography, but can produce line width variations in gate lengths and polishing removal uniformity problems in CMP. On the length scale of microns, surface roughness variations are of the order of Angstroms, but can cause gate oxide integrity problems. As another example, in fully depleted SOI wafers, thickness variations of the top silicon layer can cause transistor threshold voltage variation die-to-die (at centimeter length scale), within-die (at millimeter length scale), and conceivably, even transistor-to-transistor (on a sub-micron scale). To control parameter variations across a large range of spatial wavelengths requires a tool capable of measuring the whole wafer to capture long wavelength components, but with a very high density of data points (with correspondingly small sampled area) to capture small wavelength components. The spatial wavelength requirements thus have a profound effect on metrology capability. Methods that work well at long spatial wavelengths may become unsuitable at small spatial wavelengths due to measurement throughput limitations and/or inadequate spatial resolution. Metrology grades in this table reflect current spatial wavelength requirements. Future process and device developments that demand measurement at shorter spatial wavelengths may alter these capability grades in unforeseen ways.

Table 67b Starting Materials Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*D ½*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	M
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*M*
DRAM Total Chip Area (mm^2)	**74**	**117**	**93**	**74**	**117**	**93**	**74**	D ½
DRAM Active Transistor Area (mm^2)	**23.1**	**36.7**	**28.6**	**23.1**	**36.7**	**29.1**	**19.6**	D ½
MPU High-Performance Total Chip Area (mm^2)	**246**	**195**	**310**	**246**	**195**	**310**	**246**	M
MPU High-Performance Active Transistor Area (mm2)	**25.1**	**20.0**	**31.7**	**25.1**	**20.0**	**31.7**	**25.1**	M
*General Characteristics * (99% Chip Yield) [A, B, C]*								
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)**	**450**	**450**	**450**	**450**	**450**	**450**	**450**	*D ½, M*
Edge exclusion (mm)	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*D ½, M*
Front surface particle size (nm), latex sphere equivalent [D][E]	**≥45**	**≥32**	**≥32**	**≥32**	**≥22**	**≥22**	**≥22**	*D ½, M*
Particles (cm^{-2})	**≤0.17**	**≤0.17**	**≤0.17**	**≤0.17**	**≤0.18**	**≤0.18**	**≤0.21**	*D ½*
Particles (#/wafer)	**≤271**	**≤268**	**≤261**	**≤268**	**≤283**	**≤283**	**≤233**	*D ½*
Site flatness (nm), SFQR 26 mm × 8 mm site size [F, R]	**≤28**	**≤25**	**≤22**	**≤20**	**≤18**	**≤16**	**≤14**	*D ½, M*
Nanotopography, p-v, 2 mm diameter analysis area [Q]	**≤7**	**≤6**	**≤6**	**≤5**	**≤4**	**≤4**	**≤4**	*M*
*Polished Wafer * (99% Chip Yield)*								
The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D, E]								
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [G]	**≤0.32**	**≤0.27**	**≤0.22**	**≤0.19**	**≤0.16**	**≤0.14**	**≤0.12**	*D ½*
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [G]	**≤0.09**	**≤0.07**	**≤0.06**	**≤0.05**	**≤0.04**	**≤0.04**	**≤0.03**	*M*
*Epitaxial Wafer * (99% Chip Yield)*								
Total allowable front surface defect density is the sum of epitaxial large structural defects, small structural defects and particles (see General Characteristics) [H, I]								
Large structural epi defects (DRAM) (cm^{-2}) [J]	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	*D ½*
Large structural epi defects (MPU) (cm^{-2}) [J]	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	*M*
Small structural epi defects (DRAM) (cm^{-2}) [K]	**≤0.027**	**≤0.017**	**≤0.022**	**≤0.027**	**≤0.017**	**≤0.022**	**≤0.027**	*D ½*
Small structural epi defects (MPU) (cm^{-2}) [K]	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	*M*
Silicon-On-Insulator Wafer (99% Chip Yield)[R]*								
Edge exclusion (mm) ***	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*M*
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) [L]	**27–38**	**25–35**	**23–32**	**22–30**	**21–28**	**19–26**	**18–24**	*M*
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [M]	**13–14**	**12–14**	**12–13**	**12–13**	**12–13**	**11–12**	**11–12**	*M*
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [N]	**16–28**	**16–26**	**14–22**	**12–20**	**10–18**	**10–16**	**8–14**	*M*
D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [O]	**≤0.014**	**≤0.012**	**≤0.011**	**≤0.007**	**≤0.009**	**≤0.009**	**≤0.009**	*D ½*
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [O]	**≤0.004**	**≤0.003**	**≤0.003**	**≤0.003**	**≤0.005**	**≤0.005**	**≤0.005**	*M*
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [P]	**≤0.218**	**≤0.137**	**≤0.176**	**≤0.218**	**≤0.137**	**≤0.173**	**≤0.256**	*D ½*
D_{SASOI}, Small area SOI wafer defects (MPU) (cm^{-2}) [P]	**≤0.200**	**≤0.252**	**≤0.159**	**≤0.200**	**≤2.252**	**≤0,159**	**≤0.200**	*M*

**Parameters define limit values, independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time"; other parameter values are most likely near median value, thereby insuring total yield for all parameters is at least 99%.*

*** Values expressed in a per wafer format are calculated assuming the maximum stated wafer diameter, although that diameter likely may not be the predominant one for the corresponding technology generation. Although 450 mm is colored yellow indicating manufacturable solutions are know, it could have easily been colored red, because there has been no acceptable economic solution for funding identified by the industry.*
**** Edge exclusion is repeated in the Silicon on Insulator Wafer section because of inherent limitations associated with certain SOI wafer production techniques that differ from polished and epitaxial wafer edge exclusion capabilities.*

Meaning and Color Coding of Left Box	***Meaning and Color Coding of Right Box***
Technology Requirements Value and Supplier Manufacturing Capability by Color	**Metrology Readiness Capability by Color**
Manufacturable solutions exist, and are being optimized	*Manufacturable solutions exist, and are being optimized*
Manufacturable solutions are known	*Manufacturable solutions are known*
Manufacturable solutions are NOT known	*Manufacturable solutions are NOT known*

Model Limitations—These model-based parameter requirements do not include effects of distribution of parameter values intrinsic to the wafer manufacturing process where either of two statistical distributions commonly apply. Parameter values distributed symmetrically around a central or mean value, such as thickness, can often be described by the familiar normal distribution. The values of zero-bounded parameters (such as site flatness, particle density, and surface metal concentration) can usually be approximated by a lognormal distribution, in which the logarithms of the parameter values are normally distributed. The latter distribution is skewed with a long tail at the upper end of the distribution. Validation of the yield models remains elusive despite the experience of more than forty years of IC manufacturing.

The ideal methodology for management of material-contributed yield loss would be to allocate loss by defect type such that these defects do not contribute more than 1% to the overall IC fabrication yield loss. Yield loss for a particular defect is equal to the integral of the product of (1) the probability of failure due to a given value of the parameter (as established by the appropriate yield model) and (2) the fraction of wafers having that value (as established by the normal or lognormal distribution function). By applying this methodology, one could determine acceptable product distributions. Successful implementation of a distributional specification requires that the silicon supplier's process is sufficiently well understood, under control, and capable of meeting the IC user requirements. Until these ideals can be achieved, however, Poisson Distribution yield models based on the best available information are used and parameter limits assigned based on a 99% yield requirement for that parameter. It is further assumed that the yield loss from any individual wafer parameter does not significantly contribute to the yield loss from any other parameters, i.e., that the defect yield impacts are statistically independent. Where validation data are available, this empirical approximation has been shown to result in requirement values nearly equal to the limit values obtained from the aforementioned methodology using parameter distributions.

Cost of Ownership (CoO)—As the acceptance values for many parameters approach metrology limits, enhanced cooperation between wafer suppliers and IC manufacturers is essential for establishing and maintaining acceptable product distributions and costs. Further development and validation of IC yield/defect models is required. However, it is essential to balance the "best wafer possible" against the CoO opportunity of not driving wafer requirements to the detection limit defined by acceptable metrology practice, but instead to some less stringent value consistent with achieving high IC yield. For example, the surface metal and particle contamination requirements for starting wafers are less stringent than the pre-gate values given in Surface Preparation (see Tables 68a and b) because it is assumed that a minimum cleaning efficiency of 50% (actually 95% has been reported for surface iron removal) results during IC processing steps such as the pre-gate clean. It is also noted that the chemical nature of the surface requested by the IC manufacturer (hydrophilic versus hydrophobic) and the wafer-carrier interaction during shipment as well as the humidity in the storage room are important in affecting the subsequent adsorption of impurities and particles on the wafer surface. Further emphasis on the CoO has been ascertained by developing a model examining the viability of a 100% wafer inspection to a particular parameter (i.e., site flatness). This model considers the wafer supplier's additional cost of ensuring 100% compliance to the IC manufacturer's specification relative to the potential loss associated with processing a die with a high probability of failing if a 100% inspection is not done. The relevant worksheets employing this methodology are available on the Web so that each IC manufacturer can analyze the trade-off appropriate for their wafer specifications and product family of interest. *The SFQR description of the model is linked here* and *the actual SFQR_model is additionally included as an Excel file link.*).

Wafer Parameter Selection—Both the chemical nature and the physical structure of the wafer front surface are of critical concern, and wafer parameters related to both are included in Tables 67a and b. Chemical defects include metal and organic particles and surface chemical residues. These defects are equally significant for all wafer types, although there is some concern that the detrimental effects of surface metals may be magnified in ultra-thin SOI films when the metals

diffuse into a small silicon volume. Organic contamination strongly depends on environmental conditions during wafer storage and transportation, and accordingly is not included in Tables 67a and b, although a footnote lists a suggested value.

With the adoption of double-side polished wafers, attention is also being given to particles on the back surface of the wafer to improve both the chemical and physical characteristics. The polished back surface more readily exhibits microscopic contamination and wafer handling damage. As a result, back-surface cleanliness requirements may emerge and drive the need for more stringent robotic handler standards. However, based on a 2003 Starting Materials IC Users Survey, site flatness degradation due to the presence of back-side particles does not currently appear to be of significance and, again, has not been included in this edition of the ITRS. In addition, any back-surface treatments (e.g., extrinsic gettering and oxide back seal) may degrade the quality of both the polished back- and front-surfaces.

Important physical characteristics of the wafer front surface include wafer topography, structural defects and surface defects. Wafer topography encompasses various wafer shape categories that are classified according to their spatial frequency as site flatness, surface waviness, nanotopography or surface micro-roughness. Front surface site flatness and nanotopography are believed to be the most critical of the topographic parameters and are addressed in this ITRS revision. Back surface topography also has begun to receive attention recently, particularly in view of possible wafer interactions with stepper chucks, but the technology for quantifying this interaction is still in its infancy and this parameter is not included in the Tables. Near-edge wafer geometry is also emerging as a potential yield-limiting attribute for silicon wafers. Often referred to as ERO (Edge Roll-Off), it encompasses a variety of angularly and radially varying features in the region of the wafer surface between the substantially flat major central region of the wafer and the edge profile (the intentionally rounded outer periphery of the wafer). No consensus on metrics has yet been reached and therefore no trend values for future technology generations are established.

Structural defects include grown-in microdefects, such as COPs and bulk microdefects (BMDs). Methods of COP control have been discussed above. With advanced silicon manufacturing techniques, BMDs can be controlled independently of the interstitial oxygen concentration. In addition, current fab thermal cycles use lower temperatures and shorter times, and are not suitable to produce high levels of BMD for intrinsic gettering. As a result, in applications for which the customer is depending on BMD for gettering, a careful discussion of options with the silicon supplier is required

Other starting material requirements are expressed in terms of specific types of surface defects for different wafer types. Recent data suggest that certain devices (such as DRAM) produced on polished wafers may be sensitive to very shallow small scratches and pits. Epitaxial and SOI materials appear to exhibit fewer surface defects of this type. On the other hand, Epitaxial and SOI wafer defects include large structural defects (arbitrarily defined as > 1µm) and small structural defects (< 1µm). Epitaxial wafers are subject to grown-in crystallographic defects such as stacking faults, and large defects created by particles on the substrate. Such defects must be controlled to maximize yields when using epitaxial wafers. Several defects are unique to SOI wafers. Large area defects are of the greatest concern to yield, and include voids in the SOI layer and large defects at the SOI/BOX bond interface. These large defects are judged to have a serious effect on chip yield and are assigned a kill rate of 100%. Smaller defects, such as COPs, metal silicides or local SiO_2 islands in the top silicon layer (measured in tens of nanometers to tenths of microns) are believed to have a less severe impact on device performance and thus the allowable density is calculated based on a lower kill rate. The development of laser scanning and other instrumentation to count, size, and determine the composition and morphology of these defects is a critical metrology challenge. The removal and prevention of surface defects continues to be a state-of-the-art challenge for silicon wafer technology.

The dependence of gate dielectric integrity and other yield detractors on crystal growth parameters as well as the related role of point defects and agglomerates have been extensively documented. The resulting defect density (D_o) parameter has served effectively as a measure of material quality for several device generations. However, for devices with EOT < 2 nm, this parameter is no longer an indicator of device yield and performance and has accordingly been deleted from Tables 67a and b as a requirement. It should be noted, however, that starting material cleanliness requirements might change if pre- and post-gate surface preparation methods are modified when high-κ gate dielectric materials are introduced (see *Surface Preparation* section).

Metrology for SOI wafers is a significant challenge. Optical metrology tools operating at visible wavelengths do not have the same capabilities when operating on SOI wafers that they have with polished or epi wafers. Interference effects arising from multiple reflections from the Si and BOX layers fundamentally alter the response of these tools compared to polished and epitaxial wafers, generally degrading the measurement capability. Recently developed UV wavelength optical tools may alleviate these difficulties at least for top silicon layers thicker than 10 nm, because of the much shorter optical absorption depth at short wavelengths. Metrology methods for many of the SOI defect categories call for

destructive chemical etching that decorates but does not uniquely distinguish various types of crystal defects. These various defects may not all have the same origin, size, or impact on the device yield and, therefore, may exhibit different kill rates. Additionally, decorative defect etching on SOI wafers with very thin top silicon layers is very difficult because of the extremely small etch removals that must be used to avoid completely etching away the entire top silicon layer. Non-destructive and fast-turn around methods are also needed for the measurement of electrical properties and structural defects in SOI materials. Finally, the metrology issues for the various strained silicon configurations (spatially varying strain levels and Si:Ge composition, threading dislocations and associated defects as well as unique surface roughness issues) will require significant efforts (see *Emerging Materials* section below).

Layer thickness and uniformity are included in Tables 67a and 67b for both epitaxial and SOI wafers. For SOI wafers, the broad variety of today's IC applications requires a considerable range of Si-device layer and buried oxide (BOX) layer thicknesses. A number of SOI wafer fabrication approaches are now entering production to serve this range of SOI applications. In some cases this includes strained SOI (sSOI), which has the same layer structure as conventional SOI, except for the fact that the Si film is under biaxial tensile strain that increases the electron mobility, and to much lesser extent also the hole mobility. Strained Si is discussed in more detail in "*Emerging Materials*." The tables give incoming silicon thickness for both partially depleted (PD) and fully depleted (FD) devices. While the PD thickness values are extended through 2020, it is expected that about 2012 the actual application will be multi-gate devices. In the first order, these PD values are consistent with expected silicon thickness values for such multi-gate devices.

Potential Solutions—Figure 56 lists the most significant starting materials challenges and shows potential solutions that have been identified, along with the necessary timing for development of these solutions and their transfer into high-volume production. In alignment with Tables 67a and b, Figure 56 reflects the requirements of leading edge DRAMs and high-performance MPUs, built on 300 mm or larger diameter wafers. It should be noted however that application of 200 mm wafers beyond the 90 nm technology generation is occurring and requires double-side polishing to achieve the necessary flatness and nanotopography levels. Implementation of this wafer type will require additional investments from both the wafer suppliers and users.

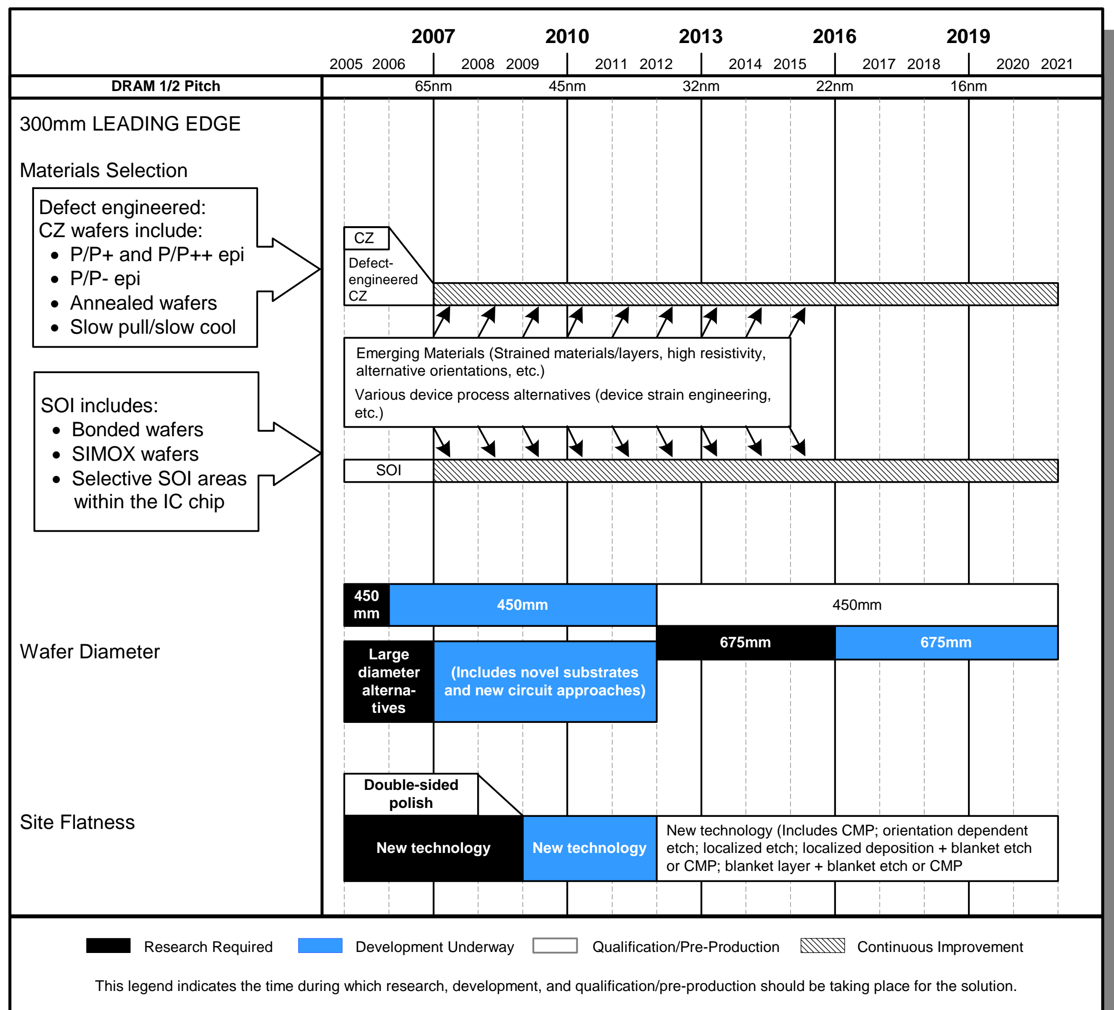


Figure 56 Starting Materials Potential Solutions

Material Selection—The materials selection category is divided into two sections: defect engineered CZ wafer and SOI wafers. The type of material chosen depends strongly on the IC application and cost performance optimization. The former is typically utilized for cost-sensitive applications while the latter is used for performance-sensitive applications. As noted in Figure 56, potential solutions are diverging, which will result in a greater challenge to available resources.

Emerging Materials—The utilization of emerging materials that augment other methods to meet ITRS targets have become critically important to the future of the silicon industry. For the 2005 ITRS, three distinct categories of emerging materials have been identified: 1) thermal management solutions, 2) mobility enhancement solutions, and 3) system-on-chip solutions. Examples of emerging materials that could potentially provide thermal managements solutions (i.e., improve heat dissipation properties) for future microelectronics applications include: Si-on-diamond, isotopically pure Si, and Si-on-insulator with the insulator being a material of higher thermal conductivity than SiO_2, for example Al_2O_3 (alumina) or silicon nitride. In addition to concerns regarding heat dissipation, future microelectronic systems will feature transistor channels that have greater mobility than that of Si. Among those emerging materials potential solutions targeted at enhancing channel mobility are: strained Si, germanium (relaxed and strained), and carbon nanotubes. Lastly, the ability to integrate new functionality into traditional CMOS logic architecture can be enabled by emerging materials innovations as well. High resistivity Si substrates and monolithic optical interconnection on Si are potential system-on-chip solutions. These emerging material topics, although potentially providing technical solutions to critical challenges facing future microelectronics, lack the maturity to include detailed specifications in Tables 67a and b for this year's

ITRS revision. However, these topics will continue to be tracked and the emerging materials committee of the ITRS has assembled a *detailed set of notes and references for the reader that are provided as a link.*

Wafer diameter—Productivity enhancement has historically been achieved partially by wafer diameter migration. The transition from 200 mm to 300 mm occurred at a time when the industry was facing serious economic challenges. This substantially delayed the onset of high-volume manufacturing for that diameter versus the expected timing based on the historical cycle. This has already influenced the timing of the move from 300 mm to 450 mm. *Issues related to 450 mm silicon wafer introduction have been compiled separately and provided as supplemental document link.*

Site Flatness—The industry made a substantial gain in site flatness process capability by going to double-sided polish for 300 mm wafers. Incremental improvements on this basic gain are expected to satisfy IC manufacturers' requirements to approximately the 65 nm technology generation. Continued improvement beyond that point may require the implementation of new flatness-improvement technologies, including those discussed in Figure 56 and its accompanying text. However, next generation lithography may strongly impact the actual flatness requirements.

FRONT END SURFACE PREPARATION

Wafer cleaning and surface preparation continue to evolve in parallel to the implementation of new materials and processes while retaining certain long-held characteristics. In front-end surface preparation, research and development have historically focused on maximizing the quality of the gate dielectric. This focus continues as the industry moves toward high-κ gate dielectrics and metal gate electrodes. The new high-κ, metal gate materials, new integration schemes as well as new transistor structures will eventually drive new requirements for front-end surface preparation. Additionally, the use of ceria-based slurries for CMP, the ability to remove high-dose implanted resist, the use of epitaxial SiGe for raised source/drains, the use of new materials for capacitors, and the increasing aspect ratio for contacts will all drive the investigation of new techniques and chemistries for cleaning.

Technology requirements for surface preparation are shown in Tables 68a and b; more details for the data are available in the *supplemental material*. Front-end predictions continue to be problematic due to the lack of data associated with future dielectric and gate electrode materials and their properties, however there seems to be a convergence on the type of high-κ material to be used, as Hf-based material are becoming more ubiquitous in device publications. Metal gate materials and the integration schemes are still under investigation; however, the metals that are used in a dual metal CMOS device must still be cleaned to a level that does not effect device performance.

Particulate contamination, both on the front and back surfaces of the wafer will continue to be a concern at increasingly demanding levels. Control of particle levels without damage to structures or etching of material is seen as a formidable challenge. The Poisson model continues to be used to predict the allowable defect density of front surface particles based on yield. The "killer defect" size, the critical particle diameter, continues to decrease, based on the technology generation. More emphasis is being based on the yield requirement, available in the *Yield Enhancement* section. It is anticipated that future models will be driven by the Yield Enhancement TWG, to ensure compatibility with the rest of the Yield Enhancement Roadmap. Back surface and bevel edge defects and particles with respect to the effect on yield are being more thoroughly investigated. Now that there is commercially available equipment to detect back surface and edge defects, more data on yield should be forthcoming. However, with an understanding that a low level of back surface particles is desirable, there is little data or models available that can link the size or density of back surface particles to yield on the front surface of the wafer. Please see the table footnotes for further explanation.

Table 68a Surface Preparation Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*D ½*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*M*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*D ½, M*
Front surface particles										
Killer defect density, D_pR_p (#/cm^2) [A]	**0.027**	**0.017**	**0.022**	**0.027**	**0.017**	**0.022**	**0.027**	**0.017**	**0.022**	*D ½*
Critical particle diameter, d_c (nm) [B]	**40.1**	**35.7**	**31.8**	**28.4**	**25.3**	**22.5**	**20.1**	**17.9**	**15.9**	*D ½*
Critical particle count, D_{pw} (#/wafer) [C]	**94.2**	**59.3**	**75.2**	**94.8**	**59.7**	**75.2**	**94.8**	**135.3**	**170.4**	*D ½*
Back surface particle diameter: lithography and measurement tools (µm) [D][E]	**0.16**	**0.12**	**0.12**	**0.12**	**0.1**	**0.1**	**0.1**	**0.1**	**NA**	*D ½*
Back surface particles: lithography and measurement tools (#/wafer) [D][E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	*D ½*
Back surface particle diameter: all other tools (µm) [D][E]	**0.2**	**0.16**	**0.16**	**0.16**	**0.14**	**0.14**	**0.14**	**0.14**	**NA**	*D ½*
Back surface particles: all other tools (#/wafer) [D][E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	*D ½*
Critical GOI surface metals (10^{10} atoms/cm^2) [F]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	*MPU*
Critical other surface metals (10^{10} atoms/cm^2) [F]	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	*MPU*
Mobile ions (10^{10} atoms/cm^2) [G]	**1.9**	**1.9**	**2**	**2.2**	**2.4**	**2.5**	**2.3**	**2.5**	**2.4**	*MPU*
Surface carbon (10^{13} atoms/cm^2) [H]	**1.4**	**1.3**	**1.2**	**1**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	
Surface oxygen (10^{13} atoms/cm^2) [I]	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	*D ½, M*
Surface roughness LVGX, RMS (Å) [J]	**4**	**4**	**4**	**4**	**4**	**2**	**2**	**2**	**2**	
Silicon loss (Å) per cleaning step [K]	**0.8**	**0.7**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	*M*
Oxide loss (Å) per cleaning step [L]	**0.8**	**0.7**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	*M*
Allowable watermarks # [M]	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*M*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

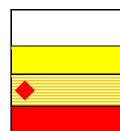
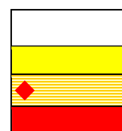


Table 68b Surface Preparation Technology Requirements—Long-term Years)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*D ½*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*M*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*M*
Wafer diameter (mm)	**450**	**450**	**450**	**450**	**450**	**450**	**450**	*D ½, M*
Wafer edge exclusion (mm)	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*D ½, M*
Front surface particles								
Killer defect density, D_pR_p (#/cm^2) [A]	**0.027**	**0.017**	**0.022**	**0.027**	**0.017**	**0.022**	**0.027**	*D ½*
Critical particle diameter, d_c (nm) [B]	**14.2**	**12.7**	**11.3**	**10.0**	**9.0**	**8.0**	**7.1**	*D ½*
Critical particle count, D_{pw} (#/wafer) [C]	**214.6**	**135.4**	**170.5**	**214.6**	**135.4**	**170.4**	**214.9**	*D ½*
Back surface particle diameter: lithography and measurement tools (µm) [D][E]	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	*D ½*
Back surface particles: lithography and measurement tools (#/wafer) [D][E]	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	*D ½*
Back surface particle diameter: all other tools (µm) [D][E]	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	*D ½*
Back surface particles: all other tools (#/wafer) [D][E]	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**	*D ½*
Critical GOI surface metals (10^{10} atoms/cm^2) [F]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	*MPU*
Critical other surface metals (10^{10} atoms/cm^2) [F]	**1**	**1**	**1**	**1**	**1**	**1**	**1**	*MPU*
Mobile ions (10^{10} atoms/cm^2) [G]	**2.4**	**2.3**	**2.3**	**2.3**	**2.3**	**2.3**	**2.3**	*MPU*
Surface carbon (10^{13} atoms/cm^2) [H]	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	
Surface oxygen (10^{13} atoms/cm^2) [I]	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	*D ½, M*
Surface roughness LVGX, RMS (Å) [J]	**2**	**2**	**2**	**2**	**2**	**2**	**2**	
Silicon loss (Å) per cleaning step [K]	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	*M*
Oxide loss (Å) per cleaning step [L]	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	*M*
Allowable watermarks # [M]	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*M*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 68a and b:

[A] Killer defect density is calculated from the formula for 99% yield, $Y=0.99=\exp[-D_pR_pA_{eff}]$. A_{eff} is the effective chip area, D_p is the defect density, and R_p is a defect kill factor indicating the probability that a given defect will kill the device. The product D_pR_p is the density of device-killing defects on the wafer. R_p is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, R_p was assumed to be 0.2 for any particle > the critical particle size, d_c. For DRAM, $A_{eff}= 2.5F^2T+(1-aF^2T/A_{chip})*0.6A_{chip}$ where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and A_{chip} is the DRAM chip size. For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length. Because A_{eff} can increase or decrease with each successive technology generation, D_pR_p does not always decrease over time.

[B] Critical particle diameter, d_c, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.

[C] An example is provided which assumes that the kill factor, R_p, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using $[R_p*3.14159*(\text{wafer radius-edge exclusion})^2]$. To convert from particles/wafer at the critical particle size to particles/wafer at an alternative size, a suggested conversion formula is: $D_{alternate}=D_{critical}*(d_{critical}/d_{alternate})^2$.

[D] and [E] These tables reflect particles added through touching the back surface of the wafer during processing and handling. For incoming wafers, the general consensus is that the specification of back surface particles should be the same as the front side (Table 68a). While there are some experimental models and empirical data available for particles added during process and handling (and future tables may use these models) there is, as yet, no industry agreement regarding the number or sizes of back surface particles that could be deleterious to semiconductor processing. Consequently, the back surface contact specs are based on present day realistic expectations (reflecting the TOTAL number of touches in any given front end of line process tool) and future aggressive lithographic improvements. Arguments have been made that back surface particles affect device yield mainly at the lithographic steps by causing the front surface of the wafer to move out of the focal plane leading to critical dimension variations. While it is not clear how the limited back surface contact achievable with pin chucks interacts with back surface particle density to cause front surface flatness variations, there is emerging evidence that "clustering" of small (<200 nm) particles are more likely to result in front side lithographic depth of focus problems than that of individual small particles. Because not all surface measurement tools are able to measure clustering, definitive data is not yet available, and future tables will reflect this data. In addition, it is also not clear how lithographic depth-of-focus (DOF) will change from year to year as this is not specified in the lithography roadmap. Aggressive specs for litho/measurement tool in outlying years (2007–2010) may necessitate edge-grip or edge-contact handling only. It is not possible to measure absolute levels of back surface particles on in-process wafers due to large variation in back surface finish and films especially for 200 mm wafers. A generally accepted practice is to process wafers with the polished front surface down in order to assess back surface particle adders for a particular process or operation. This metric reflects the TOTAL number of touches in any given front end of line process tool. Back surface particle metrics are for wafers with 3 mm edge exclusions as technology for measuring at/near the bevel edge is not available at this time. This limitation may be problematic for measuring particles generated by edge grip end-effectors.

[F] In roadmaps prior to 2003, metal contamination targets have been based on an empirically derived model predicting failure due to metal contamination as a function of gate oxide thickness. However, the oxides used in the experiments from which this model was derived were far thicker than gate oxide thicknesses used today. More recent data suggest an updated approach is appropriate. The metals are empirically grouped into three classes.[12, 13] (a) Mobile metals which may be easily removed such as Na and K and may be modeled by taking the flat-band shift of a capacitance-voltage (CV) test less than or equal to 50 mV. (b) Metals which dissolve in silicon or form silicides such as Ni, Cu, Cr, Co, Hf, and Pt. (c) Major gate-oxide-integrity (GOI) killers such as Ca, Ba, and Sr. Metals such as Fe may fall into both classes (b) and (c). Targets for mobile ions are based on allowable threshold voltage shift from a CV test. Current targets for GOI killers and other metals are based on empirical data.[14]. For extrapolation to future years, there may be reason to predict less stringent targets because effects should scale with respect to physical dielectric thickness (not EOT) that will increase upon introduction of high-κ gate dielectrics. However, in the absence of data to corroborate such a prediction, as well as predictions of physical dielectric thickness, the targets are left constant for future years. In addition, the introduction of SOI may also affect the allowable levels of metal contamination, as there is evidence metals may build up at the buried oxide layer interface. It is not yet clear how this will affect allowable metals level and has not been accounted for in these tables. Another factor to be considered in future years is the spatial distribution of localized contamination as opposed to the average contamination per wafer.

[G] The model for mobile ions, D_i, calculates the number of ions that will create a threshold voltage shift that is within a portion of the Allowable Threshold Voltage Variability (ATVV). For the mobile ion model in 2005, it is assumed that the ATVV is 3% of the Nominal Power Supply Voltage for Low Operating Power or Low Standby Power Technology (see PIDS chapter). The portion of ATVV allocated to mobile ions is assumed to be 5%. Therefore, $D_i=1/q(C_{gate}*ATVV*0.05)$, where C_{gate} is computed for an electrically equivalent SiO_2 gate dielectric thickness and q is the charge of an electron. This model reduces to $D_i = ((3.9*8.85)/1.6)*(0.05*ATVV/EOT)*10^9$, where ATVV is in mV and EOT is in nm (also from Low Operating Power or Low Standby Power Technology Requirements Table in the PIDS chapter), and the oxide dielectric constant is 3.9. Note that the year-to-year value for D_i does not always decrease because D_i is not only proportional to ATVV, but is also inversely proportional to EOT.

[H] Residual carbon resulting from organic contamination after surface preparation. The original surface Carbon model was initiated at the 180 nm technology generation and corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm^2). Surface carbon for subsequent technology generations is scaled linearly with the ratio of CD (DRAM ½ pitch) to 180 nm. $D_c=(CD/180)(7.3E+13)$.

[I] Surface oxygen requirements at <1E+12 atoms/cm^2 are driven by the needs of pre-epitaxial cleaning. Epitaxial deposition of Si and SiGe is used for some devices, now, and will find more widespread use with the implementation of strained silicon channel technology. While some level of oxide can be removed in-situ, prior to epitaxial deposition, the trend towards lower deposition temperature will preclude the use of higher temperature hydrogen pre-bake processes. Surface oxygen concentrations up to <1E+13 atoms/cm^2 are acceptable for processes such as pre-silicide cleaning. Current pre-gate cleaning does not require an oxide-free surface, but the pre-gate surface should be either fully passivated by a continuous oxide layer or have <1E+13/cm^2. An intermediate level of oxygen will be unstable. Currently high-κ gate dielectrics require and oxide-passivated surfaces prior to deposition, however, much works is ongoing to be able to deposit high-κ. dielectrics directly on silicon.

[J] In the 2001 ITRS, it was assumed channel mobility cannot be degraded by >10% due to surface preparation induced surface roughness. It was further claimed that current technologies were successfully manufactured with AFM based determination of 2Å RMS of surface micro-roughness. Where this is still approximately true for surface preparation induced, i.e. additive roughness, it is more direct to simply measure roughness on product immediately after the low voltage gate oxidation (LVGX) pre-clean. In this case, the total surface micro-roughness takes into account starting substrate roughness, plus the additional micro roughness induced by pre-cleans and strips of initial oxidation, any implant screen oxidations, or sacrificial oxidations, the first portions of the high voltage gate oxidation (dual gate flows), and any additional roughness brought about by plasma nitridations. With this taken into account, product has recently been successfully built with 4Å RMS surface micro-roughness. This may in part be explained by TCAD predictions that show carrier mobility being mainly affected by spatial frequencies smaller than those that are typically sampled by AFM micro-roughness metrology tools.

[K] The values for silicon loss are driven by requirements of high-performance Logic in the portion of the flow where source/drain extensions are fabricated. Specific values are relative to silicon loss measured optically on blanket polysilicon test wafers. Actual consumption on product will vary driven by damage from plasma etch/ash, ion implantation, and dopant concentrations. Decreasing values are in response to the requirement to control negative impact on drive currents (Ids). If the silicon under the source/drain extensions is recessed, this changes the junction profile increasing the source/drain extension resistance and decreasing drive currents. It is not yet possible to express a rigorous model connecting this metric with table parameters such as implant mask levels, junction depth, and critical dimension. IC manufacturers are currently targeting silicon loss to be 1.0Å per cleaning step for the 90 nm technology generation and 0.5Å per cleaning step for the 65 nm technology generation. It is not clear what will be required or possible in the longer term years, so the value is set at 0.4Å in 2008 and held constant until the 45 nm generation, then 0.3 Å until the 32 nm generation, then 0.2Å.

[L] The values for oxide consumption are driven by requirements of high-performance Logic in the portion of the flow where source/drain extensions are fabricated and tied to the silicon loss values. Specific values are relative to thermal oxide consumption on blanket test wafers. Actual consumption on product will vary driven by damage from plasma etch/ash, ion implantation, and dopant concentrations. Decreasing values are in response to the requirement to control negative impact on drive currents (Ids). If the silicon under the source/drain extensions is recessed, this changes the junction profile increasing the source/drain extension resistance and decreasing drive currents. By not consuming the oxide, assuming similar processing, this reduces the ability of subsequent processes to further oxidize and consume silicon. Less oxidized silicon equates to less silicon recess under the source/drain extensions. Also, consumption of deposited oxide in the isolation areas is a concern. It is not yet possible to express a rigorous model connecting this metric with table parameters such as implant mask levels, junction depth, and critical dimension. IC manufacturers are currently targeting oxide consumption to be 1.0Å per cleaning step for the 90 nm generation and 0.5Å per cleaning step for the 65 nm generation. It is not clear what will be required or possible in the longer term years, so the value is set at 0.4Å in 2008 and held constant until the 45 nm generation, then 0.3 Å until the 32 nm generation, then 0.2Å.

[M] Water marks cannot be tolerated on the wafer due to the catastrophic failure they cause on each die touched, as watermark can range from sub-micron to millimeters in diameter. Therefore a single wafer mark will exceed the maximum allowable die loss of 1%, hence the specification is zero water marks per wafer.

Control of particulate contamination will become more challenging as the need to minimize oxide and silicon loss becomes more critical. However, devices in 2008 will probably be fully depleted, fabricated on SOI substrates with raised source/drains, therefore the number of implant mask steps may decrease and this may mitigate the amount of allowable oxide and Si loss per post-implant mask cleaning step. In addition, the introduction of SOI and raised source/drains may also affect the allowable levels of metal contamination, as there is evidence metals may build up at the buried oxide layer interface. It is not yet clear how this will affect allowable metals level and it has not been accounted for in these tables.

Interface control is expected to become increasingly critical as devices begin to utilize deposited gate dielectric materials and epitaxial Si and SiGe for strained channel formation. Deposited high-κ gate dielectrics may require an oxidized or nitrided surface prior to deposition, whereas epitaxial Si will require an oxide-free surface. The surface preparation implemented prior to high-κ deposition might be accomplished through chemical oxidation—ozonated cleans have already been proven to be effective, and others are under investigation. High-κ gate dielectrics may also lead to a loosening of requirements for metal contaminant control as gates become physically thicker. After gate formation, post-etch cleans must be introduced which are compatible with high-κ dielectrics and metal gate electrodes. New MPU and DRAM materials coupled with tightening material budgets will increase the need for highly selective etching chemistries and processes, and these must be introduced without deleterious ESH effects.

There is universal understanding that watermarks cannot be tolerated on a cleaned surface, the line item for watermarks is reinstated in the 2005 roadmap.

Surface preparation challenges along with potential solutions are shown in Figure 57. Wet chemical critical cleaning is still favored because many inherent properties of liquid solutions facilitate the removal of metals (high solubility in liquid chemistries) and particles (zeta-potential control, shear stress and efficient energy transfer by megasonics). The need for other techniques will arise, however, to provide interfacial control for advanced gates as well as non-etching, damage-free particle removal. At this time, broadly effective and non-damaging particle and residue removal using liquid and non-liquid techniques are under development. Single wafer cleaning, both wet and dry, is expected to see increased implementation due to process integration and cycle time concerns, but it remains unclear when its use will become widespread in Front End of Line Processes. Single wafer critical cleaning will not likely be widely adopted until single wafer thermal and deposition processes are used for the gate stacks.

New cleaning techniques, such as water aerosol and cryogenic aerosol, have been implemented in manufacturing as single wafer systems. Other techniques for cleaning, such as laser and supercritical CO_2 processes are experiencing a high level of research and development and if implemented most likely will be on a single wafer system. However, the barriers for acceptance of these techniques are high, because solutions for cleaning already exist. Chemistries used for cleaning will continue to evolve. Dilute chemistries, especially RCA cleans, have shown feasibility and are used in production. Because they can lead to less attack of the oxide and silicon surfaces, dilute chemistries have gained greater acceptance in most advanced fabs. Ozonated water processes are being implemented as replacements for some sulfuric acid based resist strips and post-cleans. The use of ozonated water does reduce the use of chemicals and water; however, the implementation is not widespread due to the slow processing times and potential for corrosion. In addition, new resist formulations for 193 nm lithography may pose challenges for ozonated water resist stripping as well as for sulfuric acid based resist stripping.

Potential solutions are only indicated for the near-term years (through 2009) as it is unclear what challenges will exist for surface preparation at the 22 nm technology generation. As in the past, it is expected that current and future surface preparation processes will be the subject of continuous improvement efforts.

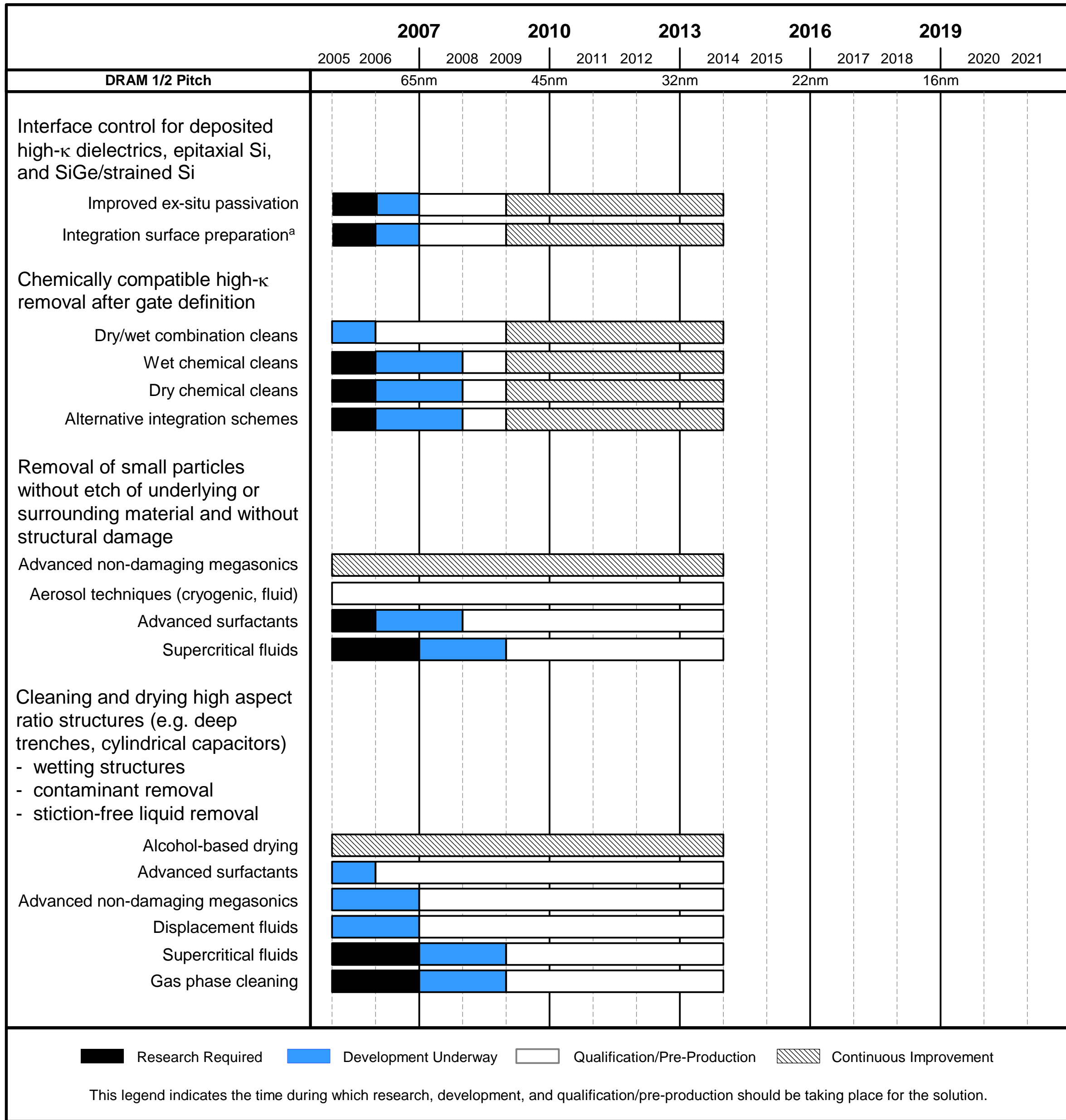


Figure 57 Surface Preparation Potential Solutions

Other thrusts, such as Environmental, Safety, and Health and *Yield Enhancement*, overlap surface preparation. Reduced chemical usage, chemical and water recycling, and alternative processes using less harmful chemistries can offer ESH and CoO benefits. Efforts in chemical and water usage reduction should continue. Automated process monitoring and control can also reduce CoO, and their increased use is expected particularly for 300 mm and larger wafer sizes where the cost of monitor wafers and process excursions become excessive. New cleaning requirements will arise related to immersion lithography, but will be tied to the implementation of that lithographic method and should be itemized by the *Lithography* technology working group in the future. Surface preparation overlaps with defect reduction technology in the need for defining appropriate purity levels in chemicals and DI water. To minimize CoO, aggressive purity targets should be adopted only where a technological justification exists. In all areas of surface preparation, a balance must be achieved between process and defect performance, cost, and environmental, health, and safety issues. Refer to the *Environment, Safety, and Health* chapter for a comprehensive overview.

THERMAL/THIN FILMS, DOPING, AND ETCHING

Front end processing requires the growth, deposition, etching and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors (for example, silicon). The difficult challenges in front end processing include: (1) the growth or deposition of reliable very thin (with electrical equivalent thickness ≤ 1.0 nm) gate dielectric layers; (2) the development of alternate high dielectric constant layers, including suitable interface layers, for both logic and DRAM capacitor applications; (3) the development of depletion-free, low-resistivity gate electrode materials, (4) the development of reliable processes to enhance the channel mobility in both NMOS and PMOS devices through channel strain, (5) the formation of low resistivity contacts to ultra-shallow junction devices, and (6) the development of resist trim and gate etch processes that provide excellent CD control. Other important challenges include the achievement of abrupt channel doping profiles, defect management for minimum post-implant leakage under reduced thermal budget environments, and formation of precise sidewall spacer structures.

An array of "Technology Innovations" are expected to be required to sustain the trend for increased transistor performance for deeply scaled devices, as detailed in the *PIDS chapter.* Strained-Si channels have just recently been introduced (to boost carrier mobility and drive currents), and work is underway to compare and assess the limits of alternative methods to introduce strain. Other technology innovations are expected to be introduced within the next five years—in particular high-κ gate dielectrics (to reduce gate leakage and control short channel effects) and metallic gates (to eliminate doped polysilicon depletion effects which limit practical scaling of gate stack layers). Even with the successful introduction of these new materials and structures, the limitations of planar bulk CMOS transistors, particularly the increased sub-threshold leakage currents exhibited at reduced threshold and drive voltages, will drive the introduction of new device structures such as fully depleted silicon (or Ge) on insulator and multi-gate transistors. This rapid introduction of new materials and device structures in the next five to seven years constitutes an unprecedented multiplicity of challenges to develop, and also to integrate these developments into effective, cost-efficient production technologies. During this period of transition, the plethora of choices for the device structure seems likely to lead to some divergence within the industry, some companies choosing to aggressive scale bulk CMOS parameters, while others make the transition to FDSOI and multi-gate structures where the requirements may be less stringent. The thermal and thin film, doping, and etching requirements are given in Tables 69a and b.

THERMAL/THIN-FILMS

The gate dielectric has emerged as one of the most difficult challenges for future device scaling. Requirements summarized in Tables 69a and b indicate an equivalent oxide thickness (EOT) progressing to substantially less than 1 nm. Direct tunneling currents and boron penetration (from the polysilicon layer) preclude the use of silicon oxynitride dielectric layers below about 1 nm thickness. Even in high-performance applications that have high allowable leakage, progress in scaling oxynitrides to 1 nm and below seems to have stalled since the 2003 ITRS, largely because of high leakage currents. Fortunately, the implementation of enhanced-mobility channels has delayed the need for high-κ dielectrics by a couple of years. In the table, empty grey cells indicate which requirements are indicated only in the near-term, intermediate, or long-term years. For example, higher dielectric constant materials may be needed as early as the 57 nm technology generation (2008). At the same time depletion-free, metal-gate electrodes will be needed. For low-power applications where the allowable gate leakage is very low, higher dielectric constant materials may also be needed as early as 2008, albeit while still using poly-Si gate electrodes. Despite promising results and even some early announcements, to date, no fully suitable alternative high-κ material and interface layer has been identified with the stability, reliability, and interface characteristics to serve as a gate dielectric for these applications. A significant, global research and development effort has been implemented to identify and qualify a suitable alternative gate dielectric material. The near-term gate dielectric solution requires the fabrication and use of ultra-thin silicon oxynitride films. The Hf-based family of high-κ gate dielectrics has been significantly studied during the past several years. Nevertheless, near-term solutions will impose severe restraints on surface preparation, pre-and post-process ambient control, silicon compatible materials development (e.g., gate electrodes and contacts), and post-processing thermal budgets. Similar problems are anticipated with the DRAM storage capacitor dielectric, anticipated to occur at an earlier technology generation.

Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1E20-doped poly-Si [A, A1, A2]	1.1	1.0	1.0						
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.2	1.1	1.1	0.5					
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.3	1.2	1.2	0.71	0.54	0.41			
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				0.9	0.75	0.65	0.5	0.5	
Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance [B, B1, B2]	1.8E+02	5.4E+02	8.0E+02	9.1E+02	1.1E+03	1.6E+03	2.0E+03	2.4E+03	
Metal gate work function for bulk MPU/ASIC $\|E_{c,v} - \phi_m\|$ (eV) [C]				<0.2	<0.2	<0.2	<0.2	<0.2	
Channel doping concentration (cm^{-3}), for bulk design [D]	3.7E+18	4.6E+18	5.4E+18	7.3E+18	8.6E+18	8.9E+18	8.6E+18	8.8E+18	
Bulk/FDSOI/DG – Long channel electron mobility enhancement factor for MPU/ASIC [E]	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Drain extension X_j (nm) for bulk MPU/ASIC [F]	11	9	7.5	7.5	7	6.5	5.8	4.5	
Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width ((Ω–μm) [G]	180	170	140	140	120	105	80	70	
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	653	674	640	740	677	650	548	593	
Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	3.5	3.1	2.8	2.5	2.2	2.0	1.8	1.5	
Contact X_j (nm) for bulk MPU/ASIC [I]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	
Allowable junction leakage for bulk MPU/ASIC (μA/μm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
Sidewall spacer thickness (nm) for bulk MPU/ASIC [J]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	
Maximum silicon consumption for bulk MPU/ASIC (nm) [K]	17.6	15.4	13.8	12.7	11.0	9.9	8.8	7.7	
Silicide thickness for bulk MPU/ASIC (nm) [L]	21	19	17	15	13	12	11	9	
Contact silicide sheet R_s for bulk MPU/ASIC (Ω/sq) [M]	7.5	8.6	9.6	10.5	12.1	13.5	15.1	17.3	
Contact maximum resistivity for bulk MPU/ASIC (Ω-cm^2) [N]	1.6E-07	1.3E-07	9.5E-08	8.3E-08	6.2E-08	4.7E-08	3.2E-08	2.5E-08	
STI depth bulk (nm) [O]	367	359	353	339	335	331	323	316	
Trench width at top (nm) [P]	80	70	65	57	50	45	40	35	
Trench sidewall angle (degrees) [Q}	>86.9	>87.2	>87.4	>87.6	>87.9	>88.1	>88.2	>88.4	

Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years (continued)

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Trench fill aspect ratio – bulk [R]	5.1	5.6	5.9	6.4	7.2	7.9	8.6	9.5	
Equivalent physical oxide thickness for FDSOI MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				0.9	0.8	0.7	0.6	0.5	0.5
Gate dielectric leakage at 100°C (A/cm^2) FDSOI high-performance [B, B1, B2]				7.7E+02	9.5E+02	1.2E+03	1.4E+03	2.1E+03	2.2E+03
Metal gate work function for FDSOI MPU/ASIC $\|\phi_m – E_i\|$ (eV)| NMOS/PMOS [S]				± 0.15	± 0.15	± 0.15	± 0.15	± 0.15	± 0.15
Saturation velocity enhancement factor MPU/ASIC [T]	1	1	1	1.1	1.1	1.1	1*	1*	1*
Si thickness FDSOI (nm) [U]				7.6	6.8	6.2	5.4	5.1	4.4
Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC × width ((Ω–μm) [G]				155	140	125	110	90	75
Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]				688	691	679	682	649	628
Spacer thickness, FDSOI elevated contact [J]				12.1	11.0	9.9	8.8	7.7	7.2
Thickness of FDSOI elevated junction (nm) [V}				22	20	18	16	14	13
Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]				22	20	18	16	14	13
Silicide thickness for FDSOI MPU/ASIC (nm) [L]				28	24	22	19	17	16
Contact silicide sheet R_s for FDSOI MPU/ASIC (Ω/sq) [M]				5.8	6.7	7.4	8.3	9.5	10.2
Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm^2) [N]				9E-08	7E0-8	6E-08	4E-08	3E-08	2E-08
Trench fill aspect ratio – FDSOI [W]				0.6	0.6	0.6	0.6	0.6	0.6
Equivalent physical oxide thickness for multi-gate MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]							0.8	0.7	0.6
Gate dielectric leakage at 100°C (nA/μm) muti-gate high-performance [B, B1, B2]							6.3E+02	7.9E+02	8.5E+02
Metal gate work function for multi-gate MPU/ASIC [S]							midgap	midgap	midgap
Si thickness for multi-gate (nm) [U]							10.3	9.0	8.4
Maximum allowable parasitic series resistance for multi-gate NMOS MPU/ASIC × width ((Ω–μm) [G]							105	95	90
Maximum drain extension sheet resistance for multi-gate MPU/ASIC (NMOS) (Ω/sq) [G]							543	557	565
Spacer thickness, multi-gate elevated contact [J]							8.8	7.7	7.2
Thickness of multi-gate elevated junction (nm) [V]							16	14	13
Maximum silicon consumption for multi-gate MPU/ASIC (nm) [K]							16	14	13
Silicide thickness for multi-gate MPU/ASIC (nm) [L]							19	17	16
Contact silicide sheet R_s for multi-gate MPU/ASIC (Ω/sq) [M]							8.3	9.5	10.2
Contact maximum resistivity for multi-gate MPU/ASIC (Ω-cm^2) [N]							4.2E-08	3.4E-08	2.9E-08

Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years (continued)

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Physical gate length low operating power (LOP) (nm)	**45**	**37**	**32**	**28**	**25**	**23**	**20**	**18**	**16**
Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	**1.4**	**1.3**	**1.2**	**0.8**	**0.7**	**0.6**	**0.6**	**0.6**	
Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for metal gate [A, A1, A2]				**1.1**	**1**	**0.9**	**0.9**	**0.9**	
Gate dielectric leakage at 100°C for bulk (A/cm^2) LOP [B, B1, B2]	**3.3E+01**	**4.1E+01**	**7.8E+01**	**8.9E+01**	**1.0E+02**	**1.1E+02**	**4.5E+02**	**6.9E+02**	
Metal gate work function for bulk low operating power $\lvert E_{c,v} - \phi_m \rvert$ (eV) [S]				**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	
Allowable junction leakage for bulk LSTP (pA/µm)	**10**	**10**	**10**	**10**	**10**	**10**	**16**	**21**	
Equivalent physical oxide thickness for FDSOI low operating power T_{ox} (nm) for metal gate [A, A1, A2]							**0.9**	**0.9**	**0.8**
Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LOP [B, B1, B2]							**2.0E+02**	**2.8E+02**	**3.1E+02**
Metal gate work function for FDSOI and multi-gate LOP [S]							**midgap**	**midgap**	**midgap**
Equivalent physical oxide thickness for multi-gate low operating power T_{ox} (nm) for metal gate [A, A1, A2]							**0.9**	**0.9**	**0.8**
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LOP [B, B1, B2]							**1.3E+02**	**1.9E+02**	**2.2E+02**
Physical gate length low standby power (LSTP) (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**	**23**	**20**
Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	**2.1**	**2.0**	**1.9**	**1.2**	**1.1**	**1**	**1**	**0.9**	**0.8**
Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for metal gate [A, A1, A2]				**1.6**	**1.5**	**1.4**	**1.4**	**1.3**	**1.2**
Gate dielectric leakage at 100°C for bulk (A/cm^2) LSTP [B, B1, B2]	**1.5E-02**	**1.9E-02**	**2.2E-02**	**2.7E-02**	**3.1E-02**	**3.6E-02**	**4.8E-02**	**7.3E-02**	**1.1E-01**
Metal gate work function for bulk LSTP $\lvert E_{c,v} - \phi_m \rvert$ (eV) [S]				**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Equivalent physical oxide thickness for FDSOI low standby power T_{ox} (nm) for metal gate [A, A1, A2]								**1.3**	**1.2**
Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LSTP [B, B1, B2]								**4.5E-02**	**5.0E-02**
Metal gate work function for FDSOI and multi-gate LSTP $\lvert \phi_m - E_i \rvert$ (eV) NMOS/PMOS [S]								**-/+ 0.1**	**-/+ 0.1**
Equivalent physical oxide thickness for multi-gate low standby power T_{ox} (nm) for metal gate [A, A1, A2]								**1.2**	**1.1**
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LSTP [B, B1, B2]								**4.5E-02**	**5.0E-02**

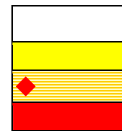
Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years (continued)

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Thickness control EOT (% 3σ) [X]	<±4	<±4	<±4	<±4	<±4	<±4	<±4	<±4	<±4
Poly-Si or metal gate electrode thickness (approximate) (nm) [Y]	64	56	50	46	40	36	32	28	26
Gate etch bias (nm) [Z]	22	20	17	15	14	12	11	10	8
L_{gate} 3σ variation (nm) [AA]	3.84	3.36	3.00	2.76	2.40	2.16	1.92	1.68	1.56
Total maximum allowable lithography 3σ (nm) [AB]	3.33	2.91	2.60	2.39	2.08	1.87	1.66	1.45	1.35
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [AB]	1.92	1.68	1.50	1.38	1.20	1.08	0.96	0.84	0.78
Resist trim maximum allowable 3σ (nm) [AC]	1.11	0.97	0.87	0.80	0.69	0.62	0.55	0.48	0.45
Gate etch maximum allowable 3σ (nm) [AC]	1.57	1.37	1.22	1.13	0.98	0.88	0.78	0.69	0.64
CD bias between dense and isolated lines [AD]	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%
Minimum measurable gate dielectric remaining (post gate etch clean) [AE]	>0	>0	>0	>0	>0	>0	>0	>0	>0
Profile control (side wall angle) [AF]	90	90	90	90	90	90	90	90	90
Allowable V_t shift from charge in dielectric (mV) [AG]	10	10	10	10	10	10	10	10	10
Allowable interfacial charge in high-κ gate stack (cm^{-2})[AH]	1.0E+11	1.1E+11	1.1E+11	1.8E+11	2.0E+11	2.2E+11	2.2E+11	2.4E+11	2.7E+11
Allowable bulk charge in high-κ gate stack (cm^{-3}) [AI]	2.4E+17	2.7E+17	3.0E+17	7.5E+17	8.9E+17	1.1E+18	1.1E+18	1.3E+18	1.7E+18
Allowable bulk charge in high-κ gate stack (ppm) [AI]	11.1	12.3	13.6	34.0	40.5	49.0	49.0	60.5	76.6
Allowable critical metal impurity level in high-κ dielectric (ppm) [AJ]	1.1	1.2	1.4	3.4	4.1	4.9	4.9	6.1	7.7

** Refer to supplemental material worksheets, 2003 Contact R_S and 2003 $R_S X_j$ online for a more complete description of the modeled devices.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 69a and b

[A] This number represents the effective thickness of the dielectric alone, at the maximum operating frequency of the technology, without substrate or electrode effects. This parameter is obtained through an electrical measurement of capacitance corrected for substrate (quantum) and electrode (depletion) effects. The electrical, or capacitance equivalent, thickness (CET), in contrast to EOT, includes a contribution due to gate (Poly-Si) depletion. A more detailed discussion of the measurement of EOT is on a separate workbook page of the linked file . Values for EOT were derived from the electrical device requirements (CET) as given in the PIDS chapter. MASTAR and other simulations were used to subtract the substrate dark space and gate depletion for the prescribed channel configuration, doping and voltage at each technology generation.

[A1] EOT values are reported for alternate gate electrode options: Poly-Si whose doping at the dielectric interface is $1 \times 10^{20}/cm^3$ (light doping), $1.5 \times 10^{20}/cm^3$ (the nominal case) and $3 \times 10^{20}/cm^3$ (representing aggressive doping) and Metal gate. In approximate terms, Poly depletion for 1.5E20 doping was about 0.4 nm, and it was about 0.3 nm for 3e20. Thus, increasing Poly-Si doping from 1E20 to 3E20 increases the allowable EOT by 0.2 nm. Similarly, metal gates can use EOTs that are about 0.4 nm thicker than 1.5E20-doped Poly-Si. Due to numerous practical difficulties at the high-κ/Poly-Si interface, it is envisioned that many companies may want to introduce metal gate at the same time, or maybe even before, high-κ dielectrics are introduced.

[A2] The color-coding of each technology generation considers the ability of known dielectrics to meet gate leakage, uniformity, and reliability requirements. For all three applications (HP, LOP, and LSTP), the gate leakage requirements, in this scenario, can no longer be met by optimized oxynitride (which is taken to have a leakage of 1/30 that of SiO_2); hence high-κ dielectric is needed. Based on early announcements and encouraging results with high-κ dielectrics and poly-Si gates, particularly at 1 nm EOT and above, (many of which employed a layered SiON-HfSiON system), were colored yellow. All other high-κ dielectrics, i.e., those thinner than 1 nm and those requiring metal gates, are colored red because a manufacturing solution to all known problems is not at hand.

[B] The gate leakage, specified at 100°C, is derived from the transistor sub-threshold leakage at room temperature. This device leakage is specified in the PIDS chapter section on Logic—High Performance and Low Power Technology Requirements as the off-state leakage (excluding the junction and the gate leakage components) at room temperature. The gate leakage specification (at 100°C) is taken to be multiple of the (room temperature) device sub-threshold leakage spec. The multiplier includes two factors: The first, or Initial Factor, accounts for the fact that not all transistors on real chips are not the low V_t (high leakage but high current drive; hence, fast) transistors specified in the PIDS table. Most transistors on HP chips are higher V_t, lower leakage and current drive. The factor of 0.1 is our estimate of a reasonable number to use to take account of these multiple transistor in HP. Conversely in LOP and LSTP chips, most of the devices are the lower V_t; hence the initial factor is 1. The second factor, High T Factor, is used to account for the fact that the device sub-threshold leakage, which is specified at room temperature, rapidly increases with operating temperature. For high-performance devices, which operate at high temperatures, this factor was taken as 10; for low operating and low standby power applications, where the temperature is lower, the factors were taken as 5 and 1, respectively. Models are provided online as linked supplemental files, in the electronic version of this chapter at http://public.itrs.net. Tying the gate leakage to the device sub-threshold leakage in this way was assumed to be satisfactory from a circuit's operation standpoint, but it should be noted that not all design approaches (companies) will allow such a high gate leakage. The gate leakage is measured on the minimum nominal device, and the specification is taken to apply to all transistor bias configurations, that is, both when $V_g = V_s = 0$ and $V_d = V_{dd}$ as well as when $V_s = V_d \approx 0$ and $V_g = V_{dd}$.

[B1] The areal gate leakage is modeled as the allowable gate leakage divided by the physical gate length. However, it should be noted that the total gate leakage is the sum of three leakage components: 1) leakage between the source and the gate in the gate-source overlap area, 2) leakage between the channel and the gate over the channel region, and 3) leakage between the gate and the drain in the gate-drain overlap area. The magnitude of each of these three components will depend on the gate, source, and drain biasing conditions. The color coding of leakage values is based on UTQUANT simulations of tunneling current from an inversion channel to the gate for the mid-point EOT. (These simulation results are given in a separate worksheet file online at http://public.itrs.net.) It should be emphasized that the tunneling current density will generally be much higher between the junction and gate than between an inversion channel and gate. Thus these simulations represent a best case (lowest leakage) condition, where the gate-to-junction overlap area is minimal. When oxide will meet the leakage specification, the value is coded white. Based on recent experience, optimized oxynitride dielectrics have about 30 times less leakage current than oxide; value are coded white when optimized oxynitride is needed to meet the leakage specs. Requirement values requiring alternate, high-κ dielectrics are coded yellow or red as discussed in Footnote A2.

[B2] The unmanaged gate leakage power is the total static chip power that would occur if all the devices on a chip had gate leakage equal to the maximum allowable value. Power management will require the extensive use of power reduction techniques, such as power-down or multiple V_t devices to achieve an acceptable static power level.

[C] The gate electrode work functions come from the PIDS device design. In bulk devices, the electrode work function and the channel doping jointly control device threshold, which is selected to maximize I_{on}, while meeting the I_{off} specification. In addition, the doping affects both short channel effects and channel mobility and, thus, requires an optimization. The PIDS design shows that work functions 0.1 eV below E_c and 0.1 eV above E_v are best for NMOS and PMOS respectively. The requirement stated in the table is for the work function to be within 0.2 eV of the Silicon band edge. Even though there is some leeway in the choice of the gate work functions, the work function itself needs to be controlled to within about 10 mV 3σ, since that it becomes a component of the device threshold voltage tolerance.

[D] The channel doping for bulk CMOS devices comes from the PIDS device design. The doping, along with the gate dielectric thickness and the junction depth control short channel effects and thus must be co-optimized. The reduced short channel effects associated with higher channel doping must also be traded off for reduced channel mobility and increased tunnel leakage. The values presented in the table reflect a representative co-optimization. Channel doping above $5 \times 10^{18}/cm^3$ was colored yellow because of concerns about excessive band-to-band tunneling leakage in junctions.

[E] Bulk/FDSOI/DG – Long channel Electron Mobility Enhancement Factor, representing the enhancement in peak electron mobility in NMOS devices.

*[F] X_j at Channel (Extension Junction) as given by the PIDS Bulk device designs (with a range of ± 25%). In earlier roadmaps X_j was taken as 0.55*Physical Gate Length; however since CET is no longer scaling with gate length, extension junction scaling has become more aggressive. Junction depths for NMOS and PMOS are the same.*

[G] The maximum allowable parasitic series resistance for NMOS devices comes from the PIDS device design. The allowable resistance for PMOS is taken to be 2.2 times the NMOS values. The maximum drain extension sheet resistance is modeled by allocating 15% of the allowable source and drain parasitic resistances to the drain extensions. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net). The drain extension sheet resistance value must be optimized together with the contact resistance and junction lateral abruptness (which effects spreading resistance), in order to meet the overall parasitic resistance requirements. This is a relatively crude model and the resultant sheet resistance values should only be used as a guide.

*[H] Channel abruptness in nm per decade drop-off in doping concentration) = 0.11 * Physical Gate Length (nm – based on Short Channel effect.[15] This lateral abruptness is consistent with a 3 decade fall off of doping over the lateral extent of the junction, which is taken to be 60% of the vertical junction depth. Note discussion of the integration choices in the supplemental material online at http://public.itrs.net.*

*[I] Contact Junction Depth = 1.1*Physical Gate Length (with a range of ±33%) for Bulk devices. Junction depths for NMOS and PMOS are the same.*

[J] Spacer thickness (width) is taken as the same as the Contact Junction Depth, namely $1.1 \times L_{gate}$,, for bulk devices.. Validity established using response surface methodology in "Response Surface Based Optimization of 0.1 µm PMOSFETs with Ultra-Thin Oxide Dielectrics"[16]. For FDSOI and Multi-gate devices, the spacer width was taken to be half that value, i.e., $0.55 \times L_{gate}$. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net).

[K] Silicon consumption is based on half the contact junction depth, for bulk devices. For advanced fully depleted and multi-gate devices, having elevated contacts, the silicide thickness is such that the silicide/silicon interface is coplanar with the channel/gate dielectric interface. The silicon consumption is equal to the added silicon thickness.

[L] Silicide thickness is based on the silicon consumption, which is taken to be 1/2 of the Contact X_j midpoint to avoid consumption-induced increase in contact leakage for bulk devices. Less than half of the junction can be consumed.[17] For fully-depleted and multi-gate devices, having elevated contact structures, the silicide thickness is that thickness yielded by consumption of the contact silicon added above the plane of the gate dielectric/channel interface. For cobalt and titanium di-silicide layers this silicide thickness is nominally equal to the silicon consumed. For nickel mono-silicide the silicide thickness is equal to 2.22/1.84× of the silicon consumed. In the table we have assumed NiSi implementation. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net).

[M] Contact silicide sheet resistance: assumes 16 $\mu\Omega$-cm silicide resistivity for NiSi.

[N] The Si/Silicide maximum interfacial contact resistivity values were calculated assuming that 100% of the PIDS total allowed MOSFET Source/Drain resistance is allocated to the contact resistivity. It further assumes that the transistor contact length is taken to be twice the MPU half pitch, where length is in the direction of current flow. Since the PIDS allocation is in terms of $R_s \times W$, the equation for the contact resistivity rhoc is: rhoc = $R_s \times W \times M$. These values should be appropriately modified if different transistor contact lengths are assumed. (See the worksheet on Contact Rs in the linked file of the electronic version of the chapter online at http://public.itrs.net). Note that this contact resistivity is the maximum allowable and cannot be used for real devices. The contact resistivity was colored red below 9×10^{-8} Ohm-cm^2 and white above 1×10^{-7} Ohm-cm^2. The values of contact resistivity, drain extension sheet resistance, and drain extension lateral abruptness must be co-optimized in order to meet the overall parasitic resistance requirements.

[O] Assumes that the trench depth for bulk is proportional to the contact junction depth plus depletion width into the well. The constant of proportionality was determined by setting the 2003 value equal to 400 nm.

[P] Assumes a minimum trench width equal to the MPU half-pitch.

[Q] Assumes that the trench width is reduced by no more than half of the top dimension.

[R] Assumes a mask thickness equal to half of the DRAM half-pitch adds to the trench depth in the substrate

[S] In fully-depleted and multi-gate devices, the gate work function is the prime determinant of device threshold; accordingly values near midgap are more appropriate. The scenario depicted in the table is one which seeks to maintain the same work function over time for a given device type and to minimize the number of different work functions needed for different applications. Dual work function gates are best served with work functions that are ± 0.15 eV from midgap for NMOS and PMOS respectively (± 0.1 eV for LSTP applications). Several applications, including some low cost ones, can be satisfied with a single midgap work function for both NMOS and PMOS. As with gate electrodes for bulk devices, work function control of 10 mV, 3σ is required.

*[T] Saturation Velocity enhancement factor. *After 2013, a velocity enhancement factor is included into the Ballistic enhancement factor, k_{bal} (see PIDS chapter)*

[U] Si thicknesses for FDSOI and multi-gate devices was based on PIDS device optimization to control short channel effects. Although some company-to-company differences in the final optimized nominal thickness is expected, the tolerance on the final thickness is ±10%. The colorization of the FDSOI thickness is based on thinning the material specified in the Starting Materials tables (in Tables 68a and b), which are controlled to ±5%, to the final thicknesses required by PIDS devices, which require a ±10% tolerance, assuming that the thinning process introduces no additional variation in thickness. Silicon thickness for all multi-gate requirements was colored red, where control of the thickness, sidewall angle, and channel mobility have not been demonstrated.

[V] The thickness of the elevated junctions in FDSOI and in Multi-gate was taken as equal to the Physical Gate Length. In this model, the entire thickness of the elevated junction is consumed to form silicide. By adjusting this thickness tradeoffs can be made between silicide sheet resistance and lateral parasitic junction-to-gate capacitance.

[W] Based on a trench depth equal to the FDSOI thickness

[X] From Modeling of Manufacturing Sensitivity and of Statistically Based Process Control [18] Requirements for 0.18 micron NMOS device.

[Y] Gate thickness is taken as two times the physical gate length. Thicker gates reduce gate series resistance, but at the expense of increased topography and aspect ratio.

[Z] Bias is defined as the difference between the printed gate length and the final post-etch gate length.

[AA] The total gate length 3σ variation encompasses all random process variation including point-to-point on a wafer, wafer-to-wafer, and lot-to-lot variations. It excludes systematic variations such as lithography proximity effects, and etch variations such as CD bias between densely spaced and isolated lines. This total variability is taken to be less than or equal to 12% of the final feature size. A conventional MOS structure is the basis for these calculations. MOS transistor structures that vary in any way from the conventional structure (e.g. Vertical MOS transistors) will have different technical challenges and will not fall within these calculations. The data is computed taking into account lithographic errors during resist patterning and combined etch errors due to both resist trim and gate etch.

[AB] The allowable lithography variance σ^2_L is limited to 3/4 of the total variance, σ^2_T of the combined lithography and etch processes. It is further assumed that the lithographic and etch processes are statistically independent and therefore that the total variance is the sum of the etch and lithography variances. This implies among other things that the printed features in the resist have vertical wall profiles and be sufficiently thick to with-stand the etch process without loss of dimensional fidelity. Refer to the Etch supplemental file in the electronic version of this chapter online at http://public.itrs.net.

[AC] It is assumed that the resist trim and gate etch processes are statistically independent and therefore that the respective variances, σ^2, of the two processes are additive. 1/3 of the combined trim-etch variance is allocated to the trim process, with the remaining 2/3 allocated to the etch process.

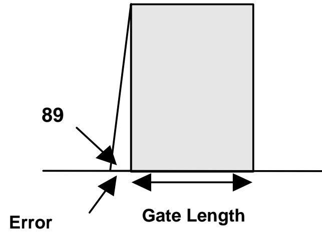
[AD] 15% dense-iso CD budget is a combination of measurements from Etch, Lithography and Metrology.

[AE] It is important that some dielectric remains after the gate etch clean step. Between technology generations the dielectric thickness decreases and there is an onset of using high-κ materials (2008) to replace the gate dielectric. Both advances represent challenges to ensure there is an amount of remaining dielectric and the ability to measure the remaining material.

[AF] Profile can be a major contributor to etch errors (see inset). Accurate measurement of vertical profiles remains difficult. Long term, the effect of edge roughness on device performance needs to be addressed and methodology of the measurement determined.

Gate error produced @ 89 degrees = 3.5 nm

Gate Length:	65nm	53nm	45nm	37nm	32nm	30nm	25nm
% error =	5.4	6.6	7.8	9.4	10.9	11.7	14



[AG] Values taken from SEMATECH working documents. Charge includes centers that are initially charges or centers which trap/detrap charge during long term stressing.

[AH] Assumes that all of the charge is at the Si-gate dielectric interface, i.e., there is no bulk charge and no charge at an SiO_2/high-κ interface

[AI] Assumes: i) a single (high-κ) dielectric with uniformly-distributed charge, and ii) a relative dielectric constant of 4 times that of SiO_2. Conversion of the bulk concentrations to units of ppm in the dielectric assume the metal atom density in the high-κ dielectric is the same as that of Si in SiO_2, namely $2.2 \times 10^{22}/cm^3$.

[AJ] Assumes that 90% of the charge (and traps) in the high-κ are due to intrinsic bonding defects and that 10% can be due to metallic impurities. The critical metals are expected to be: a) transition metals with low or mid-gap d-states, including Ti, Sc, Nd, V, Ta, Nb, b) transition metals having more d electrons than the high-κ metal, c) Cu, Ag, Ag, and d) radioactive isotopes of high-κ metals.

Table 69b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term Years

Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*DRAM*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*MPU*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*MPU*
Bulk/FDSOI/DG – Long channel electron mobility enhancement factor for MPU/ASIC [E]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	*MPU/ASIC*
Equivalent physical oxide thickness for FDSOI MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]	0.5	0.5						*MPU/ASIC FDSOI*
Gate dielectric leakage at 100°C (A/cm^2) FDSOI high-performance [B, B1, B2]	3.3E+03	3.7E+03						*MPU/ASIC FDSOI*
Metal gate work function for FDSOI MPU/ASIC $\|\phi_m - E_i\|$ (eV) NMOS/PMOS [S]	+/- 0.15	+/- 0.15						*MPU/ASIC FDSOI*
Saturation velocity enhancement factor MPU/ASIC [T]	1*	1*	1*	1*	1*	1*	1*	*MPU/ASIC*
Si thickness FDSOI (nm) [U]	3.3	3.0						*MPU/ASIC FDSOI*
Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC × width ((Ω–μm) [G]	75	75						*MPU/ASIC FDSOI*
Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]	700	771						*MPU/ASIC FDSOI*
Spacer thickness, FDSOI elevated contact [J]	6.1	5.5						*MPU/ASIC FDSOI*
Thickness of FDSOI elevated junction (nm) [V}	11	10						*MPU/ASIC FDSOI*

Table 69b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term Years (continued)

Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	2014	2015	2016	2017	2018	2019	2020	Driver
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14	DRAM
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14	MPU
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6	MPU
Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]	11	10						MPU/ASIC FDSOI
Silicide thickness for FDSOI MPU/ASIC (nm) [L]	13	12						MPU/ASIC FDSOI
Contact silicide sheet R_s for FDSOI MPU/ASIC (Ω/sq) [M]	12.1	13.3						MPU/ASIC FDSOI
Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm^2) [N]	2E-08	2E-08						MPU/ASIC FDSOI
Trench fill aspect ratio – FDSOI [W]	0.6	0.6						FDSOI
Equivalent physical oxide thickness for multi-gate MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]	0.6	0.6	0.5	0.5	0.5	0.5	0.5	MPU/ASIC Multigate
Gate dielectric leakage at 100°C (nA/µm) muti-gate High-performance [B, B1, B2]	1.0E+03	1.1E+03	1.2E+03	1.4E+03	1.6E+03	1.8E+03	2.2E+03	MPU/ASIC Multigate
Metal gate work function for multi-gate MPU/ASIC [S]	midgap	midgap	midgap	midgap	midgap	midgap	midgap	MPU/ASIC Multigate
Si thickness for multi-gate (nm) [U]	6.8	6.1	5.5	4.8	4.1	3.3	2.6	Multigate
Maximum allowable parasitic series resistance for multi-gate NMOS MPU/ASIC × width ((Ω–µm) [G]	85	70	65	65	60	55	50	MPU/ASIC Multigate
Maximum drain extension sheet resistance for multi-gate MPU/ASIC (NMOS) (Ω/sq) [G]	641	577	591	687	720	809	781	MPU/ASIC Multigate
Spacer thickness, multi-gate elevated contact [J]	6.1	5.5	5.0	4.4	3.9	3.3	3.3	MPU/ASIC Multigate
Thickness of multi-gate elevated junction (nm) [V]	11	10	9	8	7	6	6	MPU/ASIC Multigate
Maximum silicon consumption for multi-gate mpu/asic (nm) [K]	11	10	9	8	7	6	6	MPU/ASIC Multigate
Silicide thickness for multi-gate MPU/ASIC (nm) [L]	13	12	11	10	8	7	7	MPU/ASIC Multigate
Contact silicide sheet R_s for multi-gate MPU/ASIC (Ω/sq) [M]	12.1	13.3	14.8	16.7	19.0	22.2	22.2	MPU/ASIC Multigate
Contact maximum resistivity for multi-gate MPU/ASIC (Ω-cm^2) [N]	2.4E-08	1.8E-08	1.5E-08	1.eE-08	1.1E-08	8.8E-09	7E-09	MPU/ASIC Multigate
Physical gate length low operating power (LOP) (nm)	14	13	11	10	9	8	7	LOP
Equivalent physical oxide thickness for FDSOI low operating power T_{ox} (nm) for metal gate [A, A1, A2]	0.8	0.8	0.7					LOP FDSOI
Gate dielectric leakage at 100 °C for FDSOI (A/cm^2) LOP [B, B1, B2]	3.6E+02	3.8E+02	1.1E+03					LOP FDSOI

Table 69b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term Years (continued)

Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*DRAM*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*MPU*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*MPU*
Metal gate work function for FDSOI and multi-gate LOP [S]	midgap	midgap	midgap	midgap	midgap	midgap	midgap	*LOP*
Equivalent physical oxide thickness for multi-gate low operating power T_{ox} (nm) for metal gate [A, A1, A2]	0.8	0.8	0.7	0.7	0.7	0.7	0.7	*LOP Multigate*
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LOP [B, B1, B2]	3.6E+02	3.8E+02	9.1E+02	1.0E+03	1.1E+03	1.3E+03	1.4E+03	*LOP Multigate*
Physical gate length low standby power (LSTP) (nm)	18	16	14	13	11	10	9	*LSTP*
Equivalent physical oxide thickness for FDSOI low standby power T_{ox} (nm) for metal gate [A, A1, A2]	1.1	1.1	1.1	1.0	1.0	0.9	0.9	*LSTP FDSOI*
Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LSTP [B, B1, B2]	5.6E-02	6.3E-02	7.1E-02	7.7E-02	8.3E-02	9.1E-02	1.0E-01	*LSTP FDSOI*
Metal gate work function for FDSOI and multi-gate LSTP $\| \phi_m - E_i \|$ (eV)| NMOS/PMOS [S]	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	*LSTP*
Equivalent physical oxide thickness for multi-gate low standby power T_{ox} (nm) for metal gate [A, A1, A2]	1	0.9	0.8	0.8	0.8	0.8	0.8	*LSTP Multi-gate*
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LSTP [B, B1, B2]	6.0E-02	6.5E-02	7.5E-02	8.0E-02	8.6E-02	1.0E-01	1.3E-01	*LSTP Multi-gate*
Thickness control EOT (% 3σ) [X]	<±4	<±4	<±4	<±4	<±4	<±4	<±4	*MPU/ASIC*
Poly-Si or Metal Gate electrode thickness (approximate) (nm) [Y]	22	20	18	16	14	12	12	*MPU/ASIC*
Gate etch bias (nm) [Z]	8	7	6	5	5	5	3	*MPU/ASIC*
L_{gate} 3σ variation (nm) [AA]	1.32	1.20	1.08	0.96	0.84	0.72	0.72	
Total maximum allowable lithography 3σ (nm) [AB]	1.14	1.04	0.94	0.83	0.73	0.62	0.62	*MPU/ASIC*
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [AB]	0.66	0.60	0.54	0.48	0.42	0.36	0.36	*MPU/ASIC*
Resist trim maximum allowable 3σ (nm) [AC]	0.38	0.35	0.31	0.28	0.24	0.21	0.21	*MPU/ASIC*
Gate etch maximum allowable 3σ (nm) [AC]	0.54	0.49	0.44	0.39	0.34	0.29	0.29	*MPU/ASIC*
CD bias between dense and isolated lines [AD]	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	*MPU/ASIC*
Minimum measurable gate dielectric remaining (post gate etch clean) [AE]	>0	>0	>0	>0	>0	>0	>0	*MPU/ASIC*
Profile control (side wall angle) [AF]	90	90	90	90	90	90	90	*MPU/ASIC*

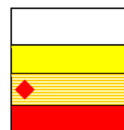
Table 69b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term Years (continued)

Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*DRAM*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*MPU*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*MPU*
Allowable V_t shift from charge in dielectric (mV) [AG]	**10**	**10**	**10**	**10**	**10**	**10**	**10**	*MPU/ASIC*
Allowable interfacial charge in high-κ gate stack (cm^{-2})[AH]	**2.0E+11**	**2.0E+11**	**2.0E+11**	**2.2E+11**	**2.2E+11**	**2.4E+11**	**2.4E+11**	*MPU/ASIC*
Allowable bulk charge in high-κ gate stack (cm^{-3}) [AI]	**8.9E+17**	**8.9E+17**	**8.9E+17**	**1.1E+18**	**1.1E+18**	**1.3E+18**	**1.3E+18**	*MPU/ASIC*
Allowable bulk charge in high-κ gate stack (ppm) [AI]	**40.5**	**40.5**	**40.5**	**49.0**	**49.0**	**60.5**	**60.5**	*MPU/ASIC*
Allowable critical metal impurity level in high-κ dielectric (ppm) [AJ]	**4.1**	**4.1**	**4.1**	**4.9**	**4.9**	**6.1**	**6.1**	*MPU/ASIC*

** Refer to supplemental material worksheets, 2003 Contact Rs and 2003 RsXj online for a more complete description of the modeled devices.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Intermediate and long-term solutions require the identification of materials with a higher dielectric constant (>10 suggested for intermediate term and >20 for long term) with other electrical characteristics (such as stability and interface-state densities) and reliability approaching that of high quality gate SiO_2. A progression from Hf-based dielectrics to Group III and rare earth (RE) oxides to ternary oxides might be required. A major problem with a material other than SiO_2 is the anticipation that a very thin SiO_2 or SiON layer may still be required at the channel interface to preserve interface-state characteristics and channel mobility. This interface layer would increase the equivalent oxide thickness and severely degrade any benefits that accrue from the use of the high-κ dielectric; epitaxial dielectrics may eliminate the interfacial layer, but there is considerable, unresolved concern about high interfacial charge levels and degraded channel mobility in those systems

The presence of an intermediate layer of O-Si-O bonding to bridge between the silicon substrate and high κ metal ions is expected to limit the scaling of equivalent oxide thickness to nominally 0.4 nm. It is also anticipated that an appropriate material may be required between the high-κ material and the gate electrode to minimize mutual interaction, to inhibit the growth of additional dielectric layers during subsequent processing, and to control/tune the effective gate electrode work function. Improved thickness control and uniformity will also be essential to achieve V_t control for 300 mm and larger wafers. Sensitivity to post-gate, process-induced damage associated with ion implant and plasma etching is expected to increase, especially as it relates to leakage current associated with the gate dielectric perimeter.

Another challenge is the realization of dielectric properties that meet both the gate leakage specification and the reliability requirements. To achieve these needs, the high κ dielectric must have a band gap of 4–5 eV with a barrier height of >1 eV to limit thermionic emission and direct tunneling. In addition, the candidate dielectric material must have negligible trap densities to be stable and to suppress Frenkle-Poole tunneling. Finally, the material must have excellent diffusion barrier properties to prevent contamination of the transistor channel by gate electrode material or gate electrode dopant.

The gate electrode also represents a major challenge for future scaling, where work function, resistivity, and compatibility with CMOS technology are key parameters for the new candidate gate electrode materials. Near-term potential solutions to the gate electrode problem include improvements in the doped polycide gate stack or the use of boron-doped Si-Ge gate electrodes. The development of enhanced means of activating the doped polysilicon for achieving tighter control of the work function as well as boron penetration resistance of the gate dielectric (e.g., the use of silicon nitride) is of great importance. Channel autodoping associated with boron out-diffusion and polysilicon depletion will eventually require the phase-out of dual-doped polysilicon gate material.

Intermediate and longer-term solutions involving metal gates are much more complex and are actively being researched. For one thing, the optimal gate electrode work function differs between different device type and between applications. In bulk NMOS and PMOS devices, band-edge work functions provide the best tradeoff between drive current and short-channel-effect control. Yet, fully-depleted SOI and multi-gate devices are better optimized with dual work function gates whose Fermi levels are a couple hundred meV above and below mid gap. Low-cost, low power applications, may be able to advantageously employ a single (mid-gap) gate work function. Hence, tunable work function systems are of high importance. Fully- or totally-silicided (FUSI, TOSI) gate electrodes are receiving much current attention, in an attempt to define the range of work function tuning that is possible in these systems. Sheet resistance considerations may ultimately require the use of cladded gate electrodes, where an interface layer is used to achieve the desired gate work function and the second layer is used to lower the overall gate sheet resistance.

Another very difficult challenge in device scaling is channel mobility enhancement, making mechanical stress a first-order consideration in the choice of front end materials and processes. Potential solutions are complex, in part because electron and hole mobilities are enhanced in different ways by stress, so that NMOS and PMOS devices need to be stressed differently. Conventional processes (trench isolation, gate electrodes, silicides) introduce local stress, which must be accounted for. In addition, global stress can be introduced using alternating layers of Si and SiGe; furthermore, strained Si (or Ge) layers can be used on SOI. Finally stressed layers can be deposited on top of devices or into the substrate (SiGe recessed junctions). Orienting PMOS devices along <100> directions, rather than the traditional <110> direction, can also be employed to enhance hole mobility. The challenges is to integrate multiple sources of local and global stress in such a way that the mobility enhancement from each source is additive, that both NMOS and PMOS devices are enhanced, and that the critical shear stress limit of the substrate is not exceeded (locally).

In order to maintain high device drive currents, technology improvements are required to increase channel mobility of traditional bulk CMOS devices, as well as partially depleted-, and fully depleted SOI devices. The use of strained channel layers, such as strained Si on relaxed Si-Ge for NMOS and strained Si on strained Si-Ge for PMOS will help in achieving this objective but will require considerable process optimization. These enhanced mobility, e.g., strained, channel devices may be needed in conjunction with oxynitride gate dielectrics, before the introduction of high-κ materials. Alternate devices such as non-standard, double gate devices anticipated in the longer-term would also benefit from strained silicon channels.

The incorporation of mobility-enhanced channels, alternate interfacial layers, high κ dielectrics, and new gate electrode materials into CMOS configurations pose significant integration challenges. The limited thermal stability of many of the candidate material systems is incompatible with junction annealing cycles typically used after gate formation The use of these new materials may require that either junction annealing temperatures be dramatically lowered, or alternate processes be used that reverse the sequence of gate stack and junction formation. Examples of these include the "replacement gate" or gate-last processes. These schemes increase manufacturing complexity, CoO, and may impact device performance and reliability. Consequently strenuous efforts are in place to retain the conventional CMOS process architecture.

Sidewall spacers are currently used to achieve isolation between the gate and source/drain regions, as well as to facilitate the fabrication of self-aligned, source/drain-engineered dopant structures. The robustness of the sidewall spacer limits the gate and source/drain contacting structure and processes that can be used to form these contacts. Sidewall spacers have traditionally been formed from deposited oxides, thermal oxidation of polysilicon, deposited nitrides, and various combinations thereof. Traditional sidewall processes will continue to be used at least until the time (2008 est.) when elevated or raised source/drain structures are required, at which time process compatibility with the side-wall spacer will become critical. Fully-depleted SOI devices will require thin, robust sidewalls having gate dielectric-like reliability and stability. In addition, they must be optimized to minimize parasitic capacitance and series resistance. Below a physical gate length of about 20 nm, even the best state-of the-art thermal oxides are susceptible to defect formation when subjected to selective epitaxial silicon or silicide processes anticipated for elevated contact structures. Nitrides or oxynitrides may offer a better alternative than oxide; however, additional research is needed to find and qualify an acceptable sidewall spacer, compatible with the high-κ gate dielectric.

Thermal and deposited thin films are also very important for filling shallow isolation trenches as well as for pre-metal dielectrics. Trends for decreasing trench width, and higher aspect ratio gaps, suggest that top and bottom corner profile control, and controlled uniform filling of dense/isolated structures, are the key requirements for this application. In the fabrication of shallow trench isolation structures, the top corner of the active region is generally exposed by HF etching of pad and sacrificial oxides prior to the growth or deposition of the gate dielectric. The gate conforms to this corner, forming a region of higher electric field and potentially high defectivity. This region can be thought of as a transistor in parallel with the bulk transistor, with both a lower threshold voltage and saturation current. This leads to a 'hump' in the

I_d/V_g characteristics and higher subthreshold leakage. Accordingly, the top corner of the STI trench is rounded, usually by oxidation prior to the deposition of the isolation oxide. Increasing the radius of curvature of this corner increases the V_t of the parasitic transistor and decreases the magnitude of this 'hump'. However, unless new processes are used, device scaling will lead to a decreased radius of curvature.

The magnitude of the parasitic drain current also depends on the degree of recession of the field oxide adjacent to the active edge, since that will in part determine the cross section of the edge 'transistor'. Therefore, as the radius of curvature is scaled down with the isolation width, hopefully so is the recession of the field oxide, resulting in at least partial mitigation of the degradation associated with the decrease of the radius of curvature. The recession of this oxide depends on the 'hardness' of the deposited isolation oxide to CMP processing and to HF dipping, as well as to the thickness of the pad and sacrificial oxides, all of which are process design choices that are optimized at each technology generation.

The key thermal/doping integration issues are maintaining shallow junction profiles, junction abruptness, obtaining high dopant activation, ensuring thermal compatibility of materials, and controlling the impact of these issues on device electrical performance. A potential solutions roadmap for Thermal/Thin Films is given in Figure 58. The technology changes associated with incorporation of strained substrates, high-κ dielectrics, metal electrodes, strain layers, and non-bulk CMOS are sufficiently major that two years of process qualification and pre-production will likely be needed before they are ready for full production. For example, extraordinary amounts of reliability data will be needed before totally new gate stack materials would be released for sale to customers. This is in contrast to previous, less radical changes, which only required a year for qualification.

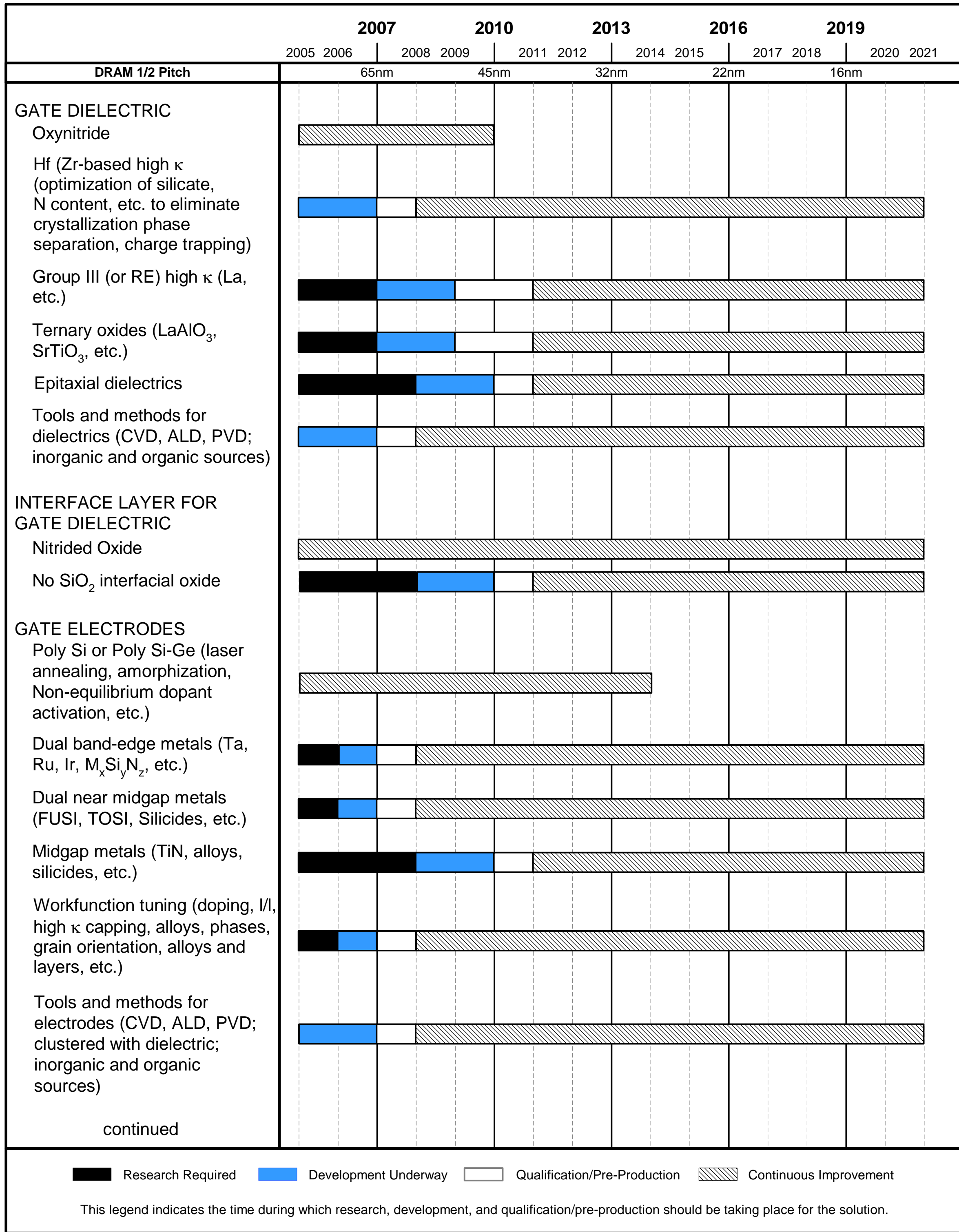


Figure 58 Thermal/Thin Films Potential Solutions

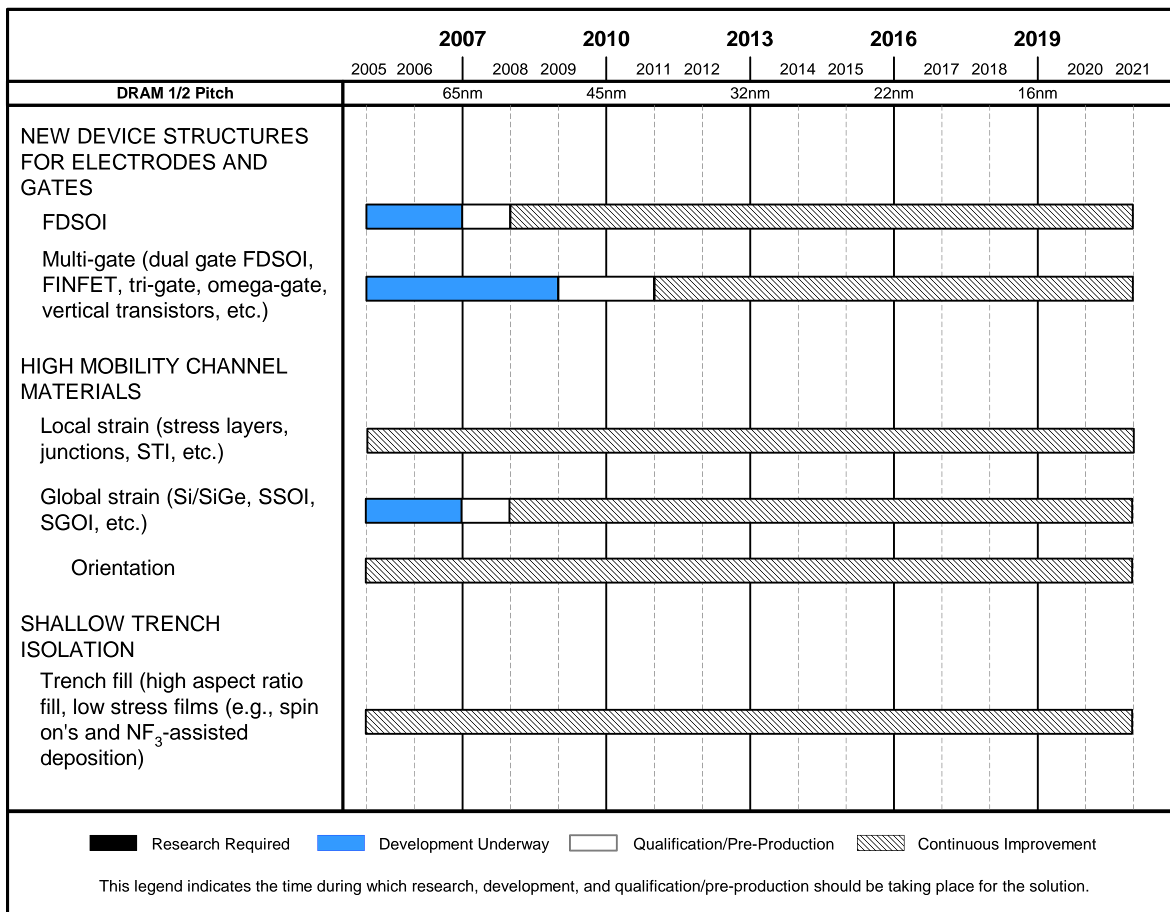


Figure 58 Thermal/Thin Films Potential Solutions (continued)

DOPING TECHNOLOGY

The traditional scaling of bulk CMOS devices is becoming increasingly difficult with the consequence that the introduction of numerous new materials and device structures is anticipated within the next few years. The transition to non-classical CMOS devices is expected to be staggered among different companies so that different device architectures may be present at any given technology generation. This is discussed in detail in the PIDS chapter where the following device scenario may be inferred for the High-Performance Transistor:

Years 2005 through 2012—bulk silicon MOSFETS with the following enhancements:

- Optimized oxynitride gate dielectric
- High-κ gate dielectric and metal gate electrode stacks starting in 2008
- Elevated contacts

Years 2008 through 2015—Fully depleted SOI single gate planar devices with elevated contacts

Years 2011 through 2020—Fully-depleted, dual—or multi-gate devices, e.g. FINFET.

Difficult Challenges—In the very short term, through 2007, the difficult challenges for doping of CMOS transistors are 1) extending the concentration of active p-type and n-type polysilicon gate doping beyond presently known limits in order to limit depletion layer thickness in poly-Si gates; 2) achieving doping profiles in the source/drain extension regions to attain progressively shallower junction depths needed for control of short-channel effects (~10 nm), while concomitantly optimizing the sheet resistance (~500 Ohms/sq)-junction depth product, doping abruptness at the extension-channel junction, and extension-gate overlap; 3) achieving controlled doping profiles in the channel region to set the threshold voltage while concomitantly minimizing short channel effect and maximizing carrier mobility, and 4) the formation of, and making low-resistance contact to shallow, highly doped source/drain regions. Already selectively-deposited, in-situ-doped junctions have started to be used to provide uniaxial stress to enhance channel mobility and at the same time to

replace ion implantation and thermal annealing. The co-optimization of channel stress, junction doping, and contact materials adds to the challenge.

Also in the near term, but beyond 2007, the grand challenge is more directly stated as “Transistor Structure”, where extensions of planar bulk devices will become increasingly difficult to control short channel effects—even with very aggressively scaled junctions and high-κ/metal gate stacks. To alleviate the need for such aggressive scaling, planar, bulk CMOS will likely start to be replaced with non-classical CMOS, i.e., FDSOI and double- and multi-gate devices, which are likely to be implemented on vertical pillars. These non-classical devices present a new set of challenges, including the need for ultra-thin SOI starting material and need for elevated contacting junctions.

Longer term, series resistance, particularly of contacts, seriously threatens the further scaling of devices. Since W/L of devices remains relatively constant with channel length scaling, the device resistance remains relatively constant. Yet contact hole sizes scale as the square of the lithographic dimension, causing contact resistances to rapidly increase for smaller feature sizes.

Source and Drain Extensions—For planar bulk CMOS, the management of short channel effects is expected to have a significant impact on processes used for doping drain extensions, channels, halos, and channel edges. Drain extension doping levels are expected to increase, driven by the need to reduce junction depth while concomitantly minimizing parasitic resistance. The implant energy and dose requirements as well as the resulting peak active dopant concentration in the supplemental material are derived from the need to achieve an extension series resistance equal to 15% of the PIDS total series resistance, assuming dopant activation with negligible diffusion (i.e. flash or non-melt laser annealing or solid phase epitaxial regrowth).

In a bulk planar MOSFET the as-implanted (vertical) junction depth with its proportional lateral straggle strongly influences subsequent lateral diffusion and encroachment of the channel. Short channel behavior is therefore strongly linked to the vertical junction depth, and the drain extension resistance is strongly linked to doping concentration and lateral abruptness. The conventional assumption has always been that a more abrupt (box like) lateral junction is better for short channel behavior, essentially since there is less encroachment of the extension doping into the channel, and hence less counter-doping for a more abrupt junction. However, it has recently been shown that due to charge sharing very abrupt junctions also degrade threshold voltage roll-off, and DIBL increases monotonically as junctions become increasingly abrupt (i.e., have steeper doping gradients). Consequently there exists a minimum abruptness of finite value for optimum device performance.

Theoretically an accumulation resistance of the source extension can be defined which strongly depends on lateral abruptness with the smallest accumulation resistance achieved for the most abrupt lateral junction. However, the accumulation resistance cannot be simply viewed as a resistive component in the current path of the device, since any change in its value will change the whole behavior of the device, most notably its short channel behavior. Any change of abruptness has to be followed by a new optimization of the device. Authors who have done so have found no relevant improvement in device performance from abrupt profiles.

The effort to model the requirements for sheet resistance, junction depth, junction abruptness, and series resistance has led to an appreciation of the complexity of the interdependence between these parameters with each other and their combined influence on the overall transistor design. Therefore, the process that collectively optimizes junction depth, doping concentration and lateral abruptness essentially requires the design of the complete transistor characteristics for each technology generation. This is a task beyond the scope of this roadmap. To that end therefore, all three requirements in the technical requirements tables have been indicated as “guidance” rather than well-defined requirements. In general terms however, for P-channel devices, sensitivity simulations indicate that above a critical abruptness value there is only a marginal reduction in parasitic resistance. Improving the abruptness beyond some critical value therefore gives only minor improvements. On the other hand, for n-channel devices, a more abrupt source extension junction leads to a higher source injection velocity and higher resulting drive current. Therefore, for NMOS devices, higher abruptness values continue to be desirable.

The realization of ultra-shallow source and drain extension junction depths, that are vertically and laterally abrupt, requires not only the development of new and enhanced methods for implanting the doping species, but requires as well the development of thermal activation processes that have an extremely small thermal budget. This is required to truncate the enhanced diffusion that accompanies the activation of the implanted dopant species. The current methods under investigation are identified in the potential solutions Figure 59. These methods may introduce significant cost adders to the CMOS process flow. Therefore, one should carefully evaluate the incremental benefits in lateral and vertical abruptness that these processes deliver versus the costs incurred. Sub-nanometer spatially resolved 2D metrology is needed to monitor the location and shape of both vertical and lateral dopant profiles in the extension region.

For non-bulk, fully-depleted ultra-thin-body (FD-UTB) MOSFETs, envisioned in year 2008 and beyond, doping processes will require modification for optimized device drive current and threshold voltage stability. The critical extension junction depth is determined by the thickness of the active silicon layer; thus it becomes somewhat less challenging to make from an implant and anneal perspective. The vertical junction depth in particular looses its meaning since it is now constrained by geometry, the thickness of the Si layer. However, this does not imply that any implant energy is suitable for the extension of an UTB device, since the lateral junction is still linked to the (virtual) vertical one. To derive reasonable values for junction depth, doping concentration and lateral abruptness essentially requires the design of the complete transistor characteristics for each technology generation—a task beyond the scope of this roadmap. Contacts to these ultra-thin extension junctions becomes much more difficult than in bulk devices, and elevated junctions are required, at least as sacrificial layers for contact silicidation. It remains to be seen how effective such elevated junctions will be in imparting sufficient strain to adequately enhance channel mobility.

FD-UTB devices do not require channel doping to manage the short channel effect, and therefore may be implemented using intrinsic, undoped silicon channels. However, the precise control of doping around the gate edge to optimize gate/drain overlap (or underlap) and the management of parasitic resistance remain important technology challenges.

Vertical channel transistors, such as the FINFET, provide the additional challenge of doping closely spaced arrays of potentially high-aspect-ratio pillars. Such structures seem likely to require isotropic doping processes to form extension junctions.

Contacts and Series Resistance—Scaling of contact area, source/drain junction depth, and contact silicide thickness will lead to increases in parasitic resistance effects unless new materials and processes are developed for producing the self-aligned silicide contact and shunt. The fundamental contact-scaling problem arises from the lateral scaling of the contact area in two dimensions. As a consequence, the contact resistivity associated with the interface between the silicide and the doped contact silicon ultimately becomes the dominant component of the overall source/drain parasitic resistance. The control of this issue requires that: a) dopant concentration at the interface is maximized, b) a lower-barrier-height junction material such as silicon/germanium is used as the contact junction and/or c) low-barrier-height, dual metal (silicides) be used to contact n+ and p+ junctions. An alternative, yet to be practically demonstrated, is to form Schottky barriers that serve as junctions and contacts. The use of selectively deposited silicon-germanium materials in the contact and the controlled profiling of the contact dopant provide potential solutions to these problems. However, the CMOS integration of these processes that mandate different dopant species for the p-channel and n-channel devices makes this a significant challenge. These integration challenges are made more difficult by the fact that the transistor gates are also doped and silicided together with the contact regions.

In bulk devices, several interdependent scaling issues arise that require mutual optimization between contact junction depth, silicide thickness, and silicon/silicide contact resistivity. The contact junction depth, despite the strategic placement of halo implants must still scale with gate length, as shown in Table 69. Because of this, progressively less of the contact depth remains available for silicide formation. To avoid high contact resistance and high contact leakage, no more than half the contact depth can be consumed in the formation of the silicide. Therefore with scaled contacts, the silicide must become progressively thinner to accommodate the progressively more shallow contact junction. This practice cannot be continued beyond a certain point because the silicide will tend to become discontinuous and therefore not adequately shunt the contact. Self-aligned NiSi contacts alleviate this problem since they form slightly thicker (more stable) films for a given amount of junction consumption and they are formed at lower temperatures where agglomeration is not as severe compared to the predecessor, $CoSi_2$. Even in bulk devices, ultimately selective deposition of silicon or germanium epitaxial layers in the contact region is required thereby making more silicon available for the silicide formation process. However, as previously discussed, selective epitaxial deposition places increased demands for perfection and robustness on the sidewall spacer.

Another challenge is posed by the introduction of high-κ dielectric/metal gate electrode stacks, also anticipated in the near term. The limited thermal budget of the candidate high-κ materials, will significantly impact the contact formation and shunting strategies.

Planar single-gate and vertical multi-gate, fully depleted CMOS transistor structures present a new array of challenges for formation of contacts, e.g., to thin, vertical multi-channel arrays linked to heavily-doped contact bus structures. Mastering the intricacies of formation of reliable contacts to these 3D structures will require an additional set of rapid innovations in contact technology. Here, the management of the series resistance of the contact structure remains a major challenge. For the planar single gate devices, the introduction of elevated contacts cannot be avoided without incurring major resistance penalties. Similarly, the research literature contains many references to the strategic use of selective epitaxial shunting of the contact regions of double gate devices in order to realize the required reduction in parasitic resistance. On the other

hand, elevated junctions increase the junction-to-diffusion parasitic capacitance, so that both the resistance and the capacitance must be considered. The whole issue of CMOS integration, and its associated dual-doping requirements and how doping is accomplished on these epitaxially enhanced contacts remain a major development issue.

Channel—The maintenance of acceptable off-state leakage with continually decreasing channel lengths will require channel-doping levels for planar CMOS transistors to increase in order to control short channel effects for extremely small devices. Increasingly precise control of both vertical and lateral channel doping profiles is required to deal with short channel effects, introducing new challenges for doping tools, process and metrology. The circuit speed advantages of increased drive current for high-performance logic applications has and will continue to drive the use of strained-Si channels materials to increase carrier mobility and to counter the trend towards lower carrier mobility driven by increased channel doping for control of short channel effects. Junction leakage, whether due to band-to-band tunneling, carrier recombination, or contact tunneling and thermionic emission, continues to be an issue, particularly for bulk devices. Part of the leakage concern arises because of direct tunneling as channel levels increase, and part because low-thermal budget annealing processes may not remove all crystal damage and dopant diffusion is insufficient to move the junction depletion region beyond regions of un-annealed damage. Leakage is sensitive to junction and channel doping, junction abruptness and damage removal.

Channel designs for fully depleted CMOS, either in planar SOI or vertical, multi-gate devices, favor the use of intrinsic, undoped silicon. This approach avoids the carrier mobility degradation associated with channel doping but requires that threshold voltage be exclusively controlled by the work function of the gate electrode. These devices usually require dual work function gates that might be achieved by a single metal whose work functions are “tuned” by changes in composition, e.g. through doping.

Optimization of the doping transition from highly-doped contact regions to intrinsic channels, reduction of subthreshold leakage at high-field channel edges in multi-gate designs and solution to a large number of process integration issues arising from a fully 3-D transistor design must be dealt with before the successful introduction of multigate, fully-depleted CMOS production. These challenges, added to the anticipated shifts to high-κ gate dielectrics and dual-work function, metal-gate materials, constitute a revolutionary change in transistor technology in the coming 4 to 7 years.

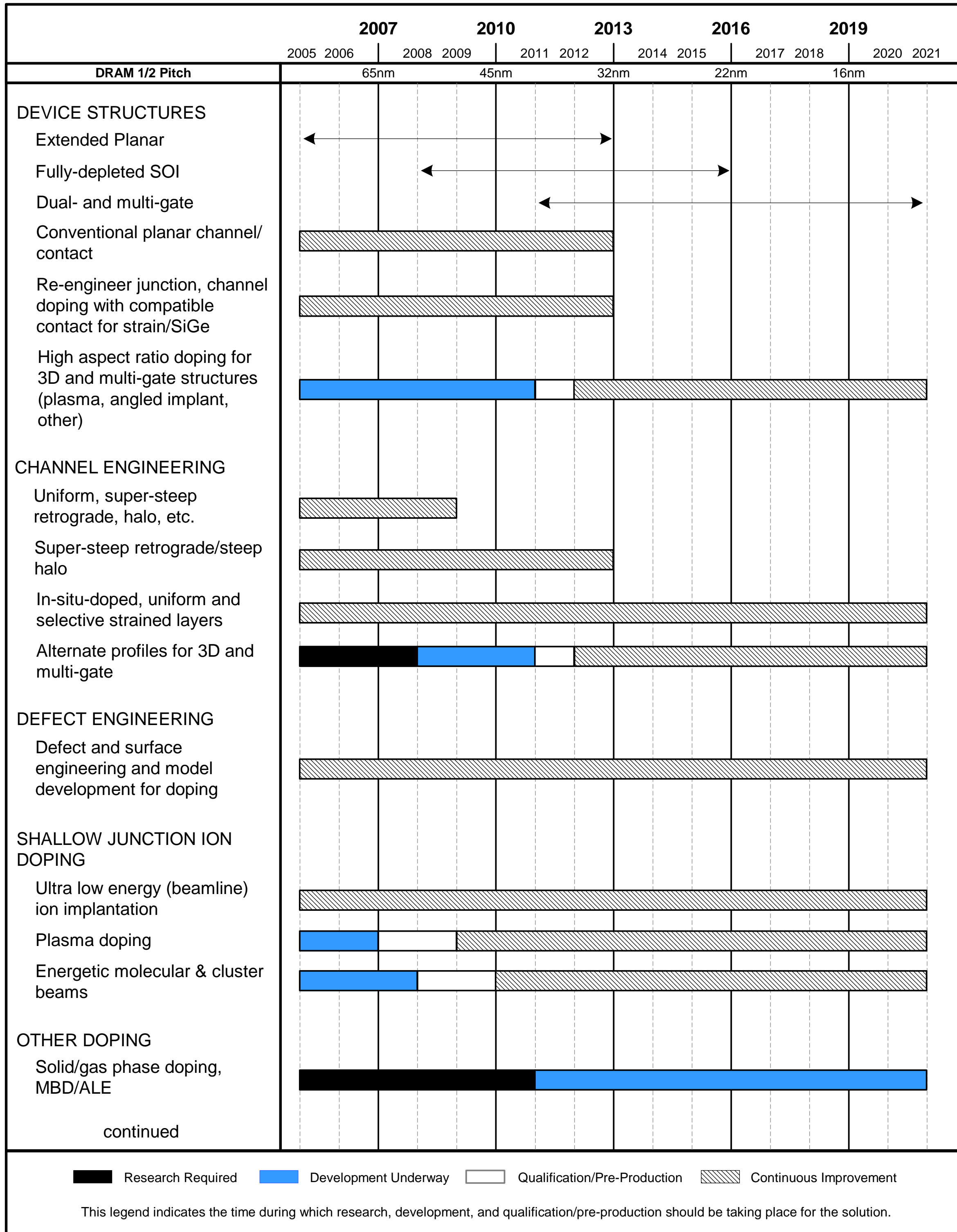


Figure 59 Doping Potential Solutions

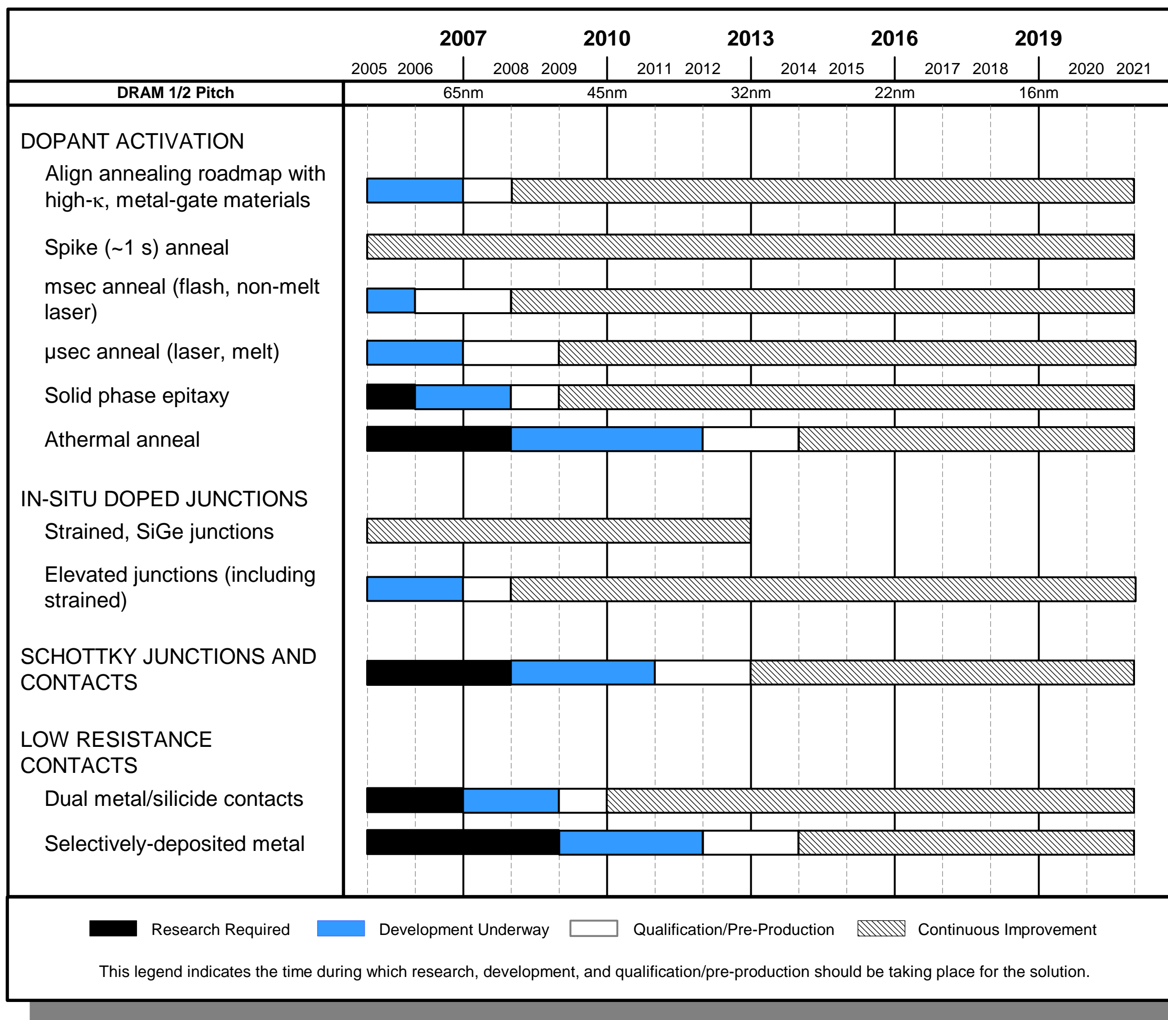


Figure 59 Doping Potential Solutions (continued)

FRONT END ETCH PROCESSING

Reduction in critical dimension (CD) and process control remain key challenges for FEP etch technology. These, coupled with new materials such as high-κ gate dielectrics, metal gates, new generations of photoresist, and potentially, non-planar transistor structures, make the challenges truly formidable. In addition, other CD reduction technologies, such as resist trim, are also now being used in production as an alternative to, or in combination with enhanced lithography approaches such as optical proximity correction (OPC), and phase shift masks (PSM).

To achieve the level of control required, etch modules must have a number of fundamental design attributes (refer to FEP Table 69a). CD etch uniformity is a strong function of chamber design which fundamentally must address both uniform gas distribution and particularly uniform plasma distribution consistent with low bias voltage. Although compensation effects can be used to improve uniformity, these introduce unacceptable repeatability risks because they create an inherently narrow process window. Wafer edge profile consistently remains an issue. Edge profile control is independent of wafer size and can possibly be considered one of the major challenges to equipment design generally. Even though very uniform plasmas may be formed across the chamber diameter, the uniformity at the wafer edge must be modified by edge compensation to account for edge anomalies. Theoretically, CD control at the sub-2 nm level can be achieved in a variety of ways, but the end result must be a vertical, smooth edge profile, achieved with a damage-free process that exhibits good selectivity control and minimum micro-loading. Of particular importance is the need for damage free processing, especially as it relates to controlled completion of the gate etch process without damage to the underlying silicon. Meeting this requirement becomes increasingly difficult as critical dimensions shrink and new gate dielectric layers are introduced (See Figure 60). In situ etch monitoring to achieve etch stop on very thin gate dielectric layers and

feed-forward/feed-back integrated metrology for profile control may well become standard techniques used to achieve sub-1 nm CD control.

The required CD control and etch characteristics mentioned above must also be achieved with new materials, such as high-κ dielectric films and metal gate structures (See Figure 60). Many plasma sources have been developed with the intent to offer improved etch performance through high ion density and separate ion energy and density control. Generally speaking however, the plasma density for optimum results is in the $\sim 10^{11}/cm^3$ regime, achievable with standard techniques. Equipment and process development may well take multiple paths. Evolution of ECR and ICP processing is expected to continue and may well develop the necessary features to deal with new gate materials. It is also possible that new etch approaches may be required to deal with the particular non-volatile by-products produced by etching metal gate electrodes. Such developments will also have collateral impacts on overall equipment robustness and particularly on MTBC and MTTC. For high-κ gate dielectric layers with metal gates these developments must be completed by 2008. To deal with sensitivity to damage, chemical downstream etching, neutral stream or other innovative etching techniques should be investigated as a possible finish- or over-etch step. Work using pulsed plasmas is already underway with this in mind. Ideally, for cost reasons, if not from a technical viewpoint, development should lead to an etch tool which can deal with both new gate materials and possible stringent damage requirements that may be brought about by advanced chip architecture (See Figure 60).

As linewidth shrinks, the presence of line edge roughness (LER is becoming increasingly important to CD control along with the slope angle of the etched gate. The LER is at best staying constant as the linewidth shrinks, which makes it a major scaling concern. There is also some evidence that LER contributes to gate leakage. Both lithography and etch can contribute to LER. The choice of gate material, photoresist type and etch chemistry all contribute to the degree of LER. It is not clear whether trim and etch can serve to reduce LER, but in any case it will become a more pervasive problem which we will need to know how to unambiguously measure and control. The current methods of quantification of LER need to be standardized so as to allow meaningful industry wide discussion of how to deal with this problem. To set a control target for this quantity, the impact of LER to device performance has to be better understood and the associated measurement methodology and equipment will also have to be developed.

Resist trim of printed features is being used in production environments to reduce gate physical dimensions as an alternative to, or in addition to lithographic techniques such as OPC and PSM. Trimming also allows compensation for within-wafer and dense/isolated line width variation in subsequent steps to enable the meeting of overall profile and CD requirements. A flexible FEP etch reactor and process is essential here. It is important to note that in addition to reducing the width of the resist uniformly across the wafer, the height of the resist must not be excessively reduced or selectivity issues will arise when transferring the pattern into the underlying hard mask. Another consideration is corner faceting. While the overall resist height may well remain intact, faceting reduces the effective height and the selectivity requirement becomes more difficult to achieve. The 193 nm resists will be used for the foreseeable future with the advent of immersion lithography. 193 nm resist is very susceptible to LER, and has poor etch resistance, so selectivity is a concern as resist thickness is scaled to improve resolution. If 157 nm lithography is needed, the resists will be of course thinner and less dense, less robust against currently used etch processes. This will lead to selectivity and resist reticulation issues. Multi-level resist techniques are also being developed to enable smaller feature transfer into underlying materials.

Changes to gate stack materials will probably occur in two phases. First, the introduction of metal or metal nitride gate materials and second, the introduction high-κ gate dielectric materials. High-κ gate dielectrics other than silicon oxides and nitrides are expected in 2008 on the low standby power devices, as EOT is reduced to less than 1 nm. It is well known that the interaction between gate materials and lithography is a vital aspect to achieving good CDs and electrical performance. These new high-κ gate dielectric materials themselves may be more difficult to etch after the electrode is formed, due to ion damage and densification. On the other hand, stopping on this more robust dielectric layer materials will be easier. Wet etching of the high-κ material may be difficult because increased thickness (compared to SiO or SiN materials) may result in unacceptable undercut profiles. Clearly, as gate dielectrics with increased κ values are introduced, new etch challenges will be uncovered. Metal gate electrode materials will also pose a CMOS integration challenge. Because of work function requirements, the candidate metal gate materials for p+ polysilicon replacement (Pt, Ir, Ni, Mn, Co) will be different from those that replace the N+ polysilicon (Ta, Zr, Hf, Ti) These materials generally have less volatile by-products than doped polysilicon, and in addition each is expected to have its own distinct etch process requirements. Therefore CMOS integration of the etching processes becomes more difficult. This brings into question whether a simultaneous etch of both gates is possible. One solution might be the use of protective resist overcoat/masks similar to the ion implant masks used in selective CMOS doping. The combined damage-free etching of dual metal gates together with damage-free stopping on a high-κ dielectric remains the ultimate goal.

The introduction of new gate materials will also impact defectivity. Strict FEP etch requirements related to defect density and plasma damage must also be met. With existing device designs, plasma damage introduced by various tunneling phenomena, hot carriers, and charging is fairly well understood, and characterized with existing device designs and materials. With the onset of new materials, new issues will arise relative to new damage mechanisms. To meet future defect density requirements the plasma processes and etch tools must generate considerably fewer and smaller particles. Improvements will be required in the etch chemistries, the control of deposition in the etch chamber, and the cleaning procedures used for the etch chamber maintenance. These requirements will have to be met, consistent with acceptable wafer processing cost and tool uptime. Plasma etch tool design and plasma-processing conditions must be developed that do not cause charging damage. Alternative high-κ and/or stacked gate dielectric materials will require development of multi-step etch processes. This requirement may translate into the need to change gas chemistries in the same etch module in order to etch a variety of stacked materials, or the need to etch the bulk material in a main etch step, followed by completion in a finishing etch, followed by an over-etch step. It is highly desirable to ascertain the amount of material remaining prior to completion of the main etch through the use of interferometry or a similar sensing technique so that a pre-emptive endpoint can be determined. Again, a highly selective non-damaging process is required.

As non-planar transistors become necessary, etch becomes much more challenging. FinFET configurations bring new constraints to selectivity, anisotropy, and damage control. The formation of the fins themselves involves sub-lithographic process control of a spacer-defined feature about 0.6 times the gate length, which was previously the most tightly controlled CD on the wafer. Profile control must be very tight in order to make very parallel fin surfaces without defects. The gate etch provides many new challenges such as cleaning stringers from the bottom of fins, etching thick potentially planarized poly and stopping on very thin oxynitrides or high-κ material, and preserving photoresist. Spacer etch will present unique problems. The spacer must be removed from the face of the fin, which can be many hundreds of angstroms high, without removing it from the corners, and without etching through the buried oxide support for the fins, or damaging the top. This may require more selective processes, and improved anisotropy without photoresist present.

Shallow Trench Isolation (STI) also has some challenging integration issues as we move towards the 45 nm regime and beyond. Here, many device manufacturers are using etch processes, rather than classic thermal processing, to round the top corner of the STI trench as a means for alleviating the classic transistor double-hump effect. Etching also has the advantage of not encroaching into the active area. For this application, integration challenges are top- and bottom-corner rounding radius control, STI wall slope control and the void-free filling of the trench with high quality oxide. These characteristics must be controlled for both variable STI gap widths and variable density of STI features while maintaining CD control.

The scaling of sidewall spacer width and its dimensional control presents another challenge to plasma etch. The spacer width and its sensitivity to over-etch is governed by the gate electrode profile, the thickness control and conformality of the spacer dielectric deposition process, as well as the anisotropy of spacer etch process (refer to FEP Tables 69a and b). An accurate assessment of the scalability of the sidewall spacer from an etch perspective is hindered by the limited availability of process control data. Here the use of feed-forward/feed-back integrated metrology may well provide a breakthrough.

For future DRAM device generations using stacked capacitor structures, the development and introduction of high aspect ratio cont via etches (HARC) of ~15:1 together with efficient post-etch residue removal processes remains crucial. The ability to maintain CD and selectivity consistent with appropriate etch stopping and low damage to the shallow contact junctions will be key technical challenges. For ultra shallow junctions a small and controlled degree of silicon contact etching is desirable for optimum device contact resistivity and leakage.

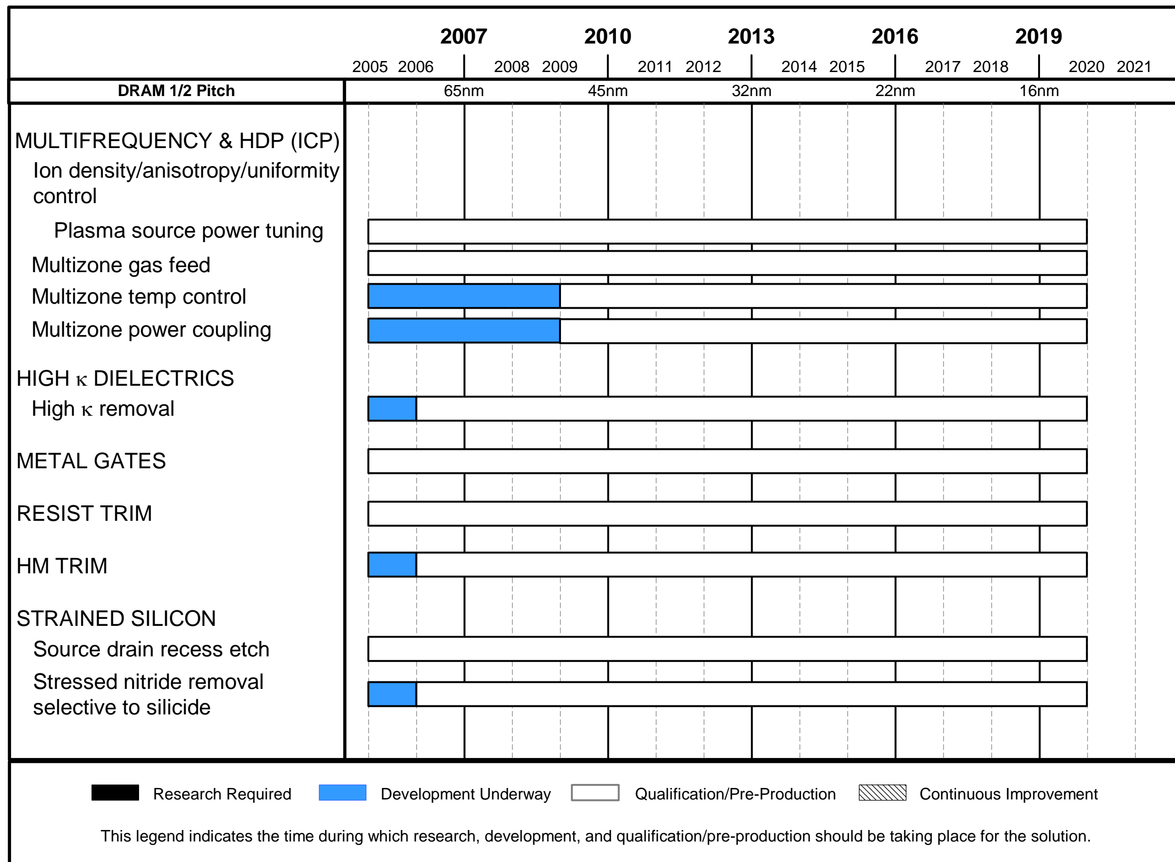


Figure 60 Front End Processes Etching Potential Solutions

DRAM STACKED CAPACITOR

Historically, the quadrupling capacity of DRAM products every three years has been based on the following:

1. Reduction of the minimum feature size (2×)
2. Expansion of the chip size (about 1.4×)
3. Improvement of cell area factor and cell efficiency (about 1.4×)

However, continued chip size growth is inhibited due to economic reasons and cell factor improvement is impaired due to the physical limit of the cell layout. Instead of quadrupling, DRAM products of intermediate capacity such as 128 Mb and 512 Mb, have appeared respectively after the 64 Mb and 256 Mb DRAM generations. DRAM capacitor technology faces new challenges of introducing new storage capacitor dielectric and electrode materials. Table 70 summarizes the technology requirements for the DRAM stacked capacitor. The DRAM cell size is being scaled down and an area of at least $8F^2$ (F is feature size) was realized at the 180 nm technology generation, which was the smallest cell size with a folded bit line architecture. Each of the target values in Table 70 is based on the assumption that a cell capacitance retains at least 25fF/cell to assure stable circuit function and sufficient soft-error immunity.

With the onset of the mega-bit era, nitride/oxide dielectric films, together with 3-dimensional polysilicon capacitor structures, have been used to keep the cell capacitance sufficiently high for sensing and noise immunity. However, it was difficult to keep a sufficiently high cell capacitance value using these materials and structure at the 130 nm technology generation and beyond. Thus, alternative high-κ dielectrics such as Ta_2O_5 and Al_2O_3 were introduced at this technology generation. Ta_2O_5, with a range of dielectric constants, is one of the most promising dielectrics mentioned above. For the 130 nm generation, a poly-silicon bottom electrode and a 3D capacitor cell with high- κ dielectric and metal counter-electrode have been used (this is an example of a metal-insulator-silicon (MIS) structure). This MIS stack, using Ta_2O_5 as a dielectric, has an effective dielectric constant of 22. However, due to the growth of an oxide layer at the interface during thermal annealing of the capacitor dielectric, this structure is not viable beyond the 90 nm technology generation. On the

other hand, if metals such as Ru and Pt are used as the bottom electrode of the storage node (MIM), a Ta_2O_5 stack exhibits an effective dielectric constant of more than 50 because the metal electrode is free from oxidation and can provide a highly oriented crystal microstructure.[19] Therefore, a MIM structure is required beyond the 90 nm generation.

At and beyond the 90 nm generation, metals or conductive metallic nitrides/oxides such as Pt, Ru, TiN, RuO_2 and IrO_2 have to be used as the storage node bottom electrode primarily to improve the immunity to oxidation and provide a template for preferred microstructure. From the thermal budget viewpoint, these electrode materials should be deposited at low temperature by using CVD based methods. However, relatively higher temperature annealing in oxygen ambient will most likely be required. Lowering the process temperature is needed if metals are used for bit lines to minimize device performance degradation.

The cell size factor, a, is projected to remain at 8 through the 65 nm generation—not scaling as rapidly as projected in 2003–4. Beyond the 65 nm generation, the factor a is projected to remain at 6. These estimations reflect the present R&D conditions.

Reducing leakage current at lower processing temperatures is another difficult challenge for DRAM capacitor technology for the 90 nm generation and beyond. Careful process integration is required to prevent capacitor film degradation caused by plasma damage and the oxide reducing processes used in the BEOL (Back End Of Line).

Beyond the 65 nm generation, the EOT (Equivalent Oxide Thickness) will need to decrease to less than 1 nm. Beyond the 45 nm generation, new ultra high-κ materials with a dielectric constant over 60 will be required. Potential solutions for the capacitor dielectric materials having the appropriate dielectric constant, based on survey of DRAM manufacturers, are given in Figure 61. However, investigations and discussions are still on-going regarding which capacitor high-κ materials will satisfy reliability conditions during the next 10 years. Even if such new materials are successfully developed, an upper electrode deposition process for a very high aspect ratio storage node may limit capacitor integration. Therefore, in addition to material and process development, new memory cell concepts such as a gain cell architecture will be required at the 45 nm generation and beyond.

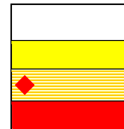
The process technology requirements for system-on-a-chip (SOC) with embedded DRAM exhibit many variations depending on the ratio of logic area and memory area. Cell capacitance requirements for embedded DRAM may be smaller than those for stand-alone DRAM. One of the serious problems for SOC is contact via formation. In general, the stacked capacitor DRAM processes require relatively deep contact vias as compared with those in logic processes. Therefore, the contact via size of DRAM has to be enlarged to minimize aspect ratio. For this reason it will be difficult to achieve the same metal line pitch for the logic section using the same DRAM design rule. In the logic-based SOC, cell size expansion is needed to reduce the capacitor height and to decrease the contact via aspect ratio. On the other hand, in the memory-based SOC, the metal line pitch has to be adjusted so that the DRAM contact via size may be kept large enough. Therefore, some additional break-through in SOC is required to solve this contact via density issue.

Table 70a DRAM Stacked Capacitor Films Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) [A]	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Cell size factor a [B]	8	8	8	6	6	6	6	6	6
Cell size (μm^2) [C]	0.051 =0.16x0.32	0.041 =0.14x0.29	0.032 =0.13x0.25	0.019 =0.11x0.17	0.015 =0.10x0.15	0.012 =0.090x0.14	0.00096 =0.080x0.12	0.0077 =0.071x0.11	0.0061 =0.064x0.96
Storage node size (μm^2) [D]	0.019 =0.08x0.24	0.015 =0.071x0.21	0.012 =0.064x0.19	0.0064 =0.057x0.11	0.0051 =0.051x0.10	0.0041 =0.045x0.090	0.0032 =0.040x0.080	0.0026 =0.036x0.071	0.0020 =0.032x0.064
Capacitor structure	Cylinder /Pedestal MIM	Cylinder /Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
t_{eq} at 25fF (nm) [G]	1.8	1.4	1.1	0.90	0.80	0.60	0.60	0.50	0.50
Dielectric constant	40	50	50	50	50	50	60	60	60
SN height (μm)	1.4	1.4	1.2	1.6	1.8	1.9	2	2	2
Cylinder factor [E]	1.5	1.5	1	1	1	1	1	1	1
Roughness factor	1	1	1	1	1	1	1	1	1
Total capacitor area (μm^2)	1.38	1.22	0.62	0.55	0.55	0.52	0.48	0.43	0.38
Structural coefficient [F]	26.8	30.0	19.2	28.6	36.0	42.6	50.2	56.3	63.2
t_{phy}. at 25fF (nm) [H]	18.2	17.9	14.1	11.5	10.3	7.7	9.2	7.7	7.7
A/R of SN (OUT) for cell plate deposition [I]	32.0	39.4	33.9	47.6	60.0	64.2	92.5	98.4	121.7
HAC diameter (μm) [J]	0.10	0.09	0.08	0.07	0.06	0.05	0.05	0.04	0.04
Total interlevel insulator and metal thickness except SN (μm) [K]	0.84	0.81	0.78	0.75	0.73	0.7	0.68	0.66	0.63
HAC depth (μm) [L]	2.24	2.16	1.98	2.35	2.53	2.6	2.68	2.66	2.63
HAC A/R	23.3	25.2	25.9	34.5	41.7	48.1	55.7	62.1	68.9
$V_{capacitor}$ (Volts)	1.6	1.5	1.4	1.3	1.2	1.1	1	1	0.9
Retention time (ms) [M]	64	64	64	64	64	64	64	64	64
Leak current (fA/cell) [N]	0.94	0.88	0.82	0.76	0.70	0.64	0.59	0.59	0.53
Leak current density (nA/cm^2)	68.1	71.9	131.7	138.3	127.7	124.7	121.0	135.9	137.4
Deposition temperature (degree C)	~500	~500	~500	~500	~500	~500	~500	~500	~500
Film anneal temperature (degree C)	~750	~750	~750	~750	<750	<750	~650	~650	~650
Word line R_s (Ohm/sq.)	2	2	2	2	2	2	2	2	2

HAC—high aspect contact

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 70a and b:

[A] 2005 Overall Roadmap Technology Characteristics, Table 1a and b

[B] $a = (\text{cell size})/F^2$ (F : minimum feature size)

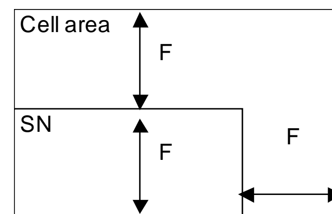
[C] Cell size = $a*F^2$ (cell shorter side = 2F)

[D] SN size = $(a/2 - 1)*F^2$ (SN shorter side = F)

[E] Cylinder structure increase the capacitor area by a factor of 1.5

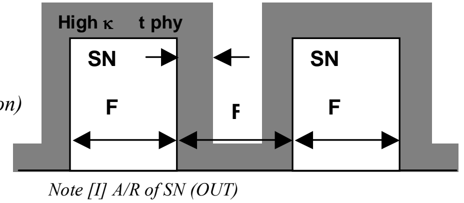
[F] SC = (total capacitor area) / (cell size)

[G] $t_{eq} = 3.9*E0*(\text{total capacitor area})/25fF$



Notes[C] & [D] Cell area and Projected SN area

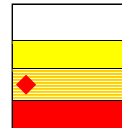
[H] t_{phy}. = t_{eq}*E_r/3.9 If polysilicon is used as a bottom electrode. t_{phy}. =(t_{eq}-1)*E_r/3.9
[I] A/R of SN (OUT) = (SN height) / (F - 2* t_{phy}.)
[J] HAC diameter = 1.2*F
[K] The thickness is assumed to be 1.05 µm@180 nm. (10% reduction by each technology generation)
[L] HAC depth = SN height + total interlevel insulator and metal thickness
[M] DRAM retention time (PIDS)
[N] (Sense Limit*C*V_{dd}/2)/(Retention Time * MARGIN) (Sense limit=30% leak, MARGIN=100)



Note [I] A/R of SN (OUT)

Table 70b DRAM Stacked Capacitor Films Technology Requirements—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) [A]	28	25	22	20	18	16	14
Cell size factor a [B]	6	6	6	6	6	6	6
Cell size (μm^2) [C]	0.0048 =0.057x0.085	0.0038 =0.051x0.076	0.0030 =0.045x0.068	0.0024 =0.040x0.060	0.0019 =0.036x0.054	0.0015 =0.032x0.048	0.012 =0.028x0.043
Storage node size (μm^2) [D]	0.0016 =0.032x0.064	0.0013 =0.025x0.051	0.0010 =0.023x0.045	0.00080 =0.020x0.040	0.00064 =0.018x0.036	0.00051 =0.016x0.032	0.00040 =0.014x0.028
Capacitor structure	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
t_{eq} at 25fF (nm) [G]	0.45	0.40	0.40	0.30	0.25	0.20	0.15
Dielectric constant	80	80	80	100	100	100	100
SN height (µm)	2	2	2	2	2	2	2
Cylinder factor [E]	1	1	1	1	1	1	1
Roughness factor	1	1	1	1	1	1	1
Total capacitor area (μm^2)	0.34	0.30	0.27	0.24	0.21	0.19	0.17
Structural coefficient [F]	70.9	79.5	89.2	100	112	126	141
t_{phy} .at 25fF (nm) [H]	9.2	8.2	8.2	7.7	6.4	5.1	3.8
A/R of SN (OUT) for cell plate deposition [I]	202.3	226.1	328.4	429.1	397.0	353.8	308.6
HAC diameter (µm) [J]	0.03	0.03	0.03	0.02	0.02	0.02	0.02
Total interlevel insulator and metal thickness except SN (µm) [K]	0.61	0.59	0.57	0.55	0.53	0.51	0.49
HAC depth (µm) [L]	2.61	2.59	2.57	2.55	2.53	2.51	2.49
HAC A/R	76.7	85.5	95.2	106.0	118.1	131.4	146.3
$V_{capacitor}$ (Volts)	0.8	0.8	0.7	0.6	0.6	0.6	0.6
Retention time (ms) [M]	64	64	64	64	64	64	64
Leak current (fA/cell) [N]	0.47	0.47	0.41	0.35	0.35	0.35	0.35
Leak current density (nA/cm^2)	137.1	154.0	151.3	145.7	163.6	183.7	206.2
Deposition temperature (degree C)	~500	~500	~500	~500	~500	~500	~500
Film anneal temperature (degree C)	<650	<650	<650	<650	<650	<650	<650
Word line R_s (Ohm/sq.)	2	2	2	2	2	2	2



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM M1 ½ -pitch (nm)			65			45			32			22			16	
Top Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, …															
Capacitor Dielectric Material	Al_2O_3, HfO_2, Ta_2O_5			Ta_2O_5, TiO_2			Ultra high κ; new materials, strontium -based, perovskites									
Bottom Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, others															

Figure 61 DRAM Stacked Capacitor Potential Solutions[20]

DRAM TRENCH CAPACITOR

Tables 71a and b summarize the technological requirements for trench DRAM capacitors. The target values are based on the assumption that a cell capacitance retains at least 28 fF per memory cell to ensure sufficient signal and retention margin. It is further assumed that the cell size will remain 8 F^2.

For technology generations down to and including the 90 nm design rule, a conventional nitride/oxide dielectric has been used as capacitor dielectric in trench cells. Additional surface enhancement techniques have been implemented starting with the 90 nm generation. The trench profile is widened below a certain depth (bottle-shaped trenches) and the trench side walls are roughened (trench surface roughening) to increase the capacitor surface area.

At and below the 80 nm generation high-κ materials such as Al_2O_3 or HfSiON will be used as storage capacitor dielectric. Atomic Layer Deposition (ALD) will be utilized to deposit new materials into high aspect ratio trenches. Metal top electrodes are anticipated at the 65 nm generation and will allow the replacement of SIS by MIS capacitors. Conductive metal nitrides are the most attractive material candidates for the top metal plate. Ultimately, MIM capacitors are required for the 50 nm generation.

Trench technology allows the fabrication of rigid and mechanically extremely stable high aspect ratio capacitor structures. As a result of ground-rule shrinking, the trench aspect ratio (trench depth divided by trench top width after etch) will increase up to values of ~ 80:1 for the 65 nm design rule. Even higher aspect ratios are anticipated at smaller ground rules.

Novel cell concepts relying on the replacement of the conventional planar transfer device by 3-dimensional array transistor structures are envisaged for the 65 nm technology generation in order to alleviate device-scaling issues. The cell size factor, a, is projected to remain at 8. Reducing the cell size factor to 6 will degrade the cell efficiency and increase the process complexity, resulting in nearly no gain in overall productivity.

For embedded applications, the trench technology with its capacitor buried in the substrate enables a planar transition between the DRAM cell array and the logic circuit. The trench DRAM concept also avoids deep, high aspect ratio contact holes. In addition, since the capacitor is processed prior to the transfer device, degradation of device performance from the capacitor-forming thermal budget is not encountered.

Table 71a DRAM Trench Capacitor Technology Requirements—Near-term Years

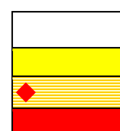
Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Cell size factor	**8**	**8**	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Cell size (μm^2)	**0.051**	**0.039**	**0.034**	**0.026**	**0.020**	**0.016**	**0.013**	**0.010**	**0.008**
Trench structure	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**
Trench circumference (nm)	**665**	**582**	**540**	**474**	**416**	**374**	**333**	**291**	**266**
Trench area enhancement factor (bottle) [A]	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**
Trench surface roughening factor	**1.25**	**1.25**	**1.2**	**1**	**1**	**1**	**1**	**1**	**1**
Effective oxide thickness (CET)(nm)	**4.4**	**4.3**	**3.9**	**2.8**	**2.3**	**2.0**	**1.8**	**1.6**	**1.4**
Trench depth [μm], (at 35fF)	**6.2**	**6.8**	**6.8**	**6.7**	**6.2**	**6.1**	**6.2**	**6.1**	**6.0**
Aspect ratio (trench depth/trench width)	**60**	**75**	**80**	**90**	**95**	**105**	**120**	**135**	**145**
Upper electrode	**Poly-Silicon**	**Poly-Silicon**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**
Dielectric material	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**
Bottom electrode	**Silicon**	**Silicon**	**Silicon**	**Silicon**	**Silicon**	**1: Silicon**	**1: Silicon**	**Metal**	**Metal**
					2: Metal	**2: Metal**	**2: Metal**		
Capacitor structure/dielectric	**Silicon-Insulator-Silicon/High-κ**		**Meal-Insulator-Silicon/High-κ**		**1: MIS/High-κ 2: MIM/High-κ**			**Metal-Insulator-Metal / High-κ**	

[A] Bottle factor = checkerboard square perimeter / conventional elliptical perimeter
Perimeter of trench ellipse = pi(3/2(a+b)-sqrt(ab))= 7,933 * short half axis*

Table 71b DRAM Trench Capacitor Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Cell size factor	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Cell size (μm^2)	**0.006**	**0.005**	**0.004**	**0.003**	**0.003**	**0.002**	**0.002**
Trench structure	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**
Trench circumference (nm)	**233**	**208**	**183**	**166**	**150**	**133**	**116**
Trench area enhancement factor (bottle) [A]	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**	**1.6**
Trench surface roughening factor	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Effective oxide thickness (CET)(nm)	**1.2**	**1.0**	**0.8**	**0.7**	**0.6**	**0.5**	**0.4**
Trench depth [μm], (at 35fF)	**5.8**	**5.5**	**5.0**	**4.8**	**4.5**	**4.2**	**3.8**
Aspect ratio (trench depth/trench width)	**160**	**170**	**175**	**185**	**190**	**200**	**210**
Upper electrode	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**
Dielectric material	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**	**High-κ**
Bottom electrode	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**	**Metal**
Capacitor structure/dielectric	**Metal-Insulator-Metal/High-κ**						

[A] Bottle factor = checkerboard square perimeter / conventional elliptical perimeter
Perimeter of trench ellipse = pi(3/2(a+b)-sqrt(ab)) = 7,933 * short half axis*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known

Manufacturable solutions are NOT known

NON-VOLATILE MEMORY (FLASH)

Tables 72a and b summarize the main technology requirements for NOR and NAND flash memories. The most important issues are related to the cell area reduction (see the non-volatile memory technology requirements, in the *PIDS chapter*) and to the consequent scaling down of the thickness of the two key active dielectrics of the memory cell, namely the tunnel oxide and the interpoly dielectric, in a way that guarantees the charge retention and endurance requirements for the memory cell. For NAND Flash the best definition of the minimum feature size is the half-pitch of the memory cell when viewing a cross section parallel to the bit line, that is also the half pitch of the poly 2-word line. Refer to Figure 62.

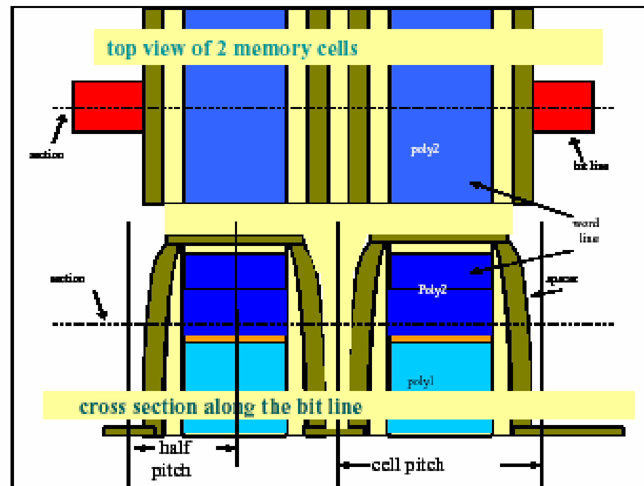


Figure 62 Minimum Feature Size of NAND Flash Memory

For NOR Flash memories the definition of the minimum feature size is not very easy and can vary among the different Flash manufacturers. Referring to Figure 63, the following are definitions of the minimum feature size specific for NOR Flash memories, as follows:

- the half pitch when viewing a cross section parallel to the poly 2 word line
- the poly 1 to poly 1 distance along the word line
- the minimum contact size

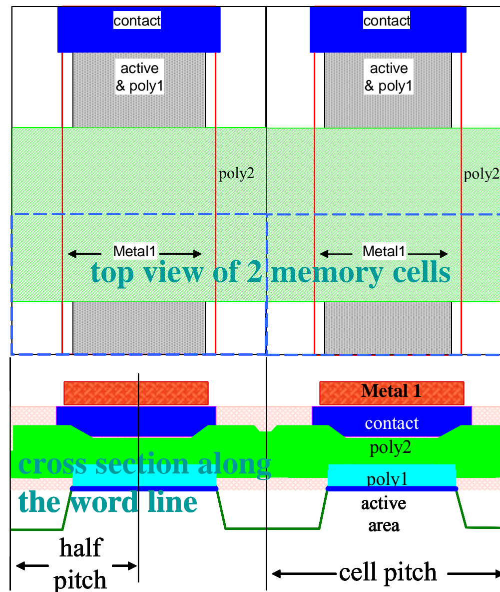


Figure 63 Minimum Feature Size of NOR Flash Memory

The tunnel oxide thickness must be reduced for the programming/erasing performances while scaling the interpoly dielectric thickness reduction is necessary to keep the capacitance coupling ratio, α_g, at an almost constant value in order to achieve acceptable ratios between the control and floating gate voltages. The coupling ratio is typically improved by reducing the interpoly dielectric thickness and increasing the tunnel oxide thickness and the floating/control gate coupling area. Scaling the tunnel oxide thickness is one of the key challenges for Flash memories, since this dielectric must simultaneously guarantee good charge retention properties, that are better with a higher thickness, and high write/erasing performances, that are better with a lower thickness.

The impact of the floating/control gate coupling area on the α_g factor becomes a critical issue starting from the 45-40 nm technology generation for both NOR and NAND flash devices, when the spacing between two adjacent floating gates (poly 1) becomes too small to allow the control gate (poly 2) to overlap the vertical poly 1 sidewalls, as is done in the present architecture. The lack of electrical coupling between poly 1 and poly 2 along the vertical sidewalls of the poly 1 results in a strong degradation of the α_g value and requires a strong reduction of the interpoly dielectric thickness as a compensation. This situation is illustrated in Fig. xx.

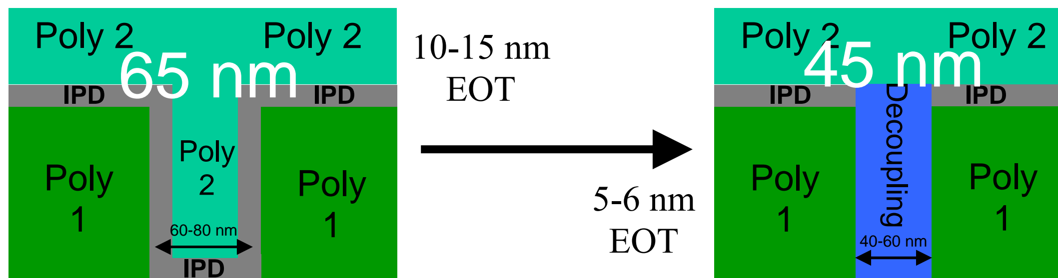


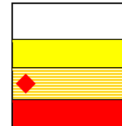
Figure 64 Flash Memory Interpoly Dielectric Thickness Scaling at 45 nm

The present interpoly dielectric technology is based on oxy-nitride stacked layers and will probably not be feasible for an aggressive EOT reduction, due to unacceptable charge retention properties. Thus, the introduction of high-κ materials at this step will be necessary. Alternatively, new floating gate designs to maintain a high coupling area with the control gate or storage materials different from poly-silicon are potential solutions. From this point of view, the 45-40 nm technology generation will be a transition one with both classical and new solutions depending on the architecture schemes chosen for the memory cells.

Table 72a FLASH Non-volatile Memory Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
Flash technology generation NOR/NAND - F (nm) [A]	**80/70**	**70/65**	**65/55**	**57/50**	**50/45**	**45/40**	**40/35**	**35/32**	**32/28**
Flash NOR tunnel oxide thickness (EOT-nm) [B]	**8–9**	**8–9**	**8–9**	**8–9**	**8–9**	**8**	**8**	**8**	**8**
Flash NAND tunnel oxide thickness (EOT-nm) [B]	**7–8**	**7–8**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**
Flash program/erase window min DVT SLC/MLC (V) [D]	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**
Flash erase/program time degradation t_{max}/t_0 at constant V [E]	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**
Flash NOR interpoly dielectric thickness (EOT-nm) [F]	**13–15**	**13–15**	**13–15**	**13–15**	**13–15**	**◆ 6–13**	**◆ 6–13**	**◆ 6–13**	**4–6**
Flash NAND interpoly dielectric thickness (EOT-nm) [F]	**13–15**	**13–15**	**10–13**	**10–13**	**10–13**	**◆ 5–12**	**◆ 5–12**	**◆ 5–12**	**4–6**
Flash interpoly dielectric thickness control EOT (% 3s) [G]	**<±6**	**<±6**	**<±6**	**<±6**	**<±6**	**<±5**	**<±5**	**<±5**	**<±5**
Flash interpoly dielectric T_{max} of formation t >5′/<5′ (ºC) [H]	**750/900**	**750/900**	**750/900**	**750/900**	**750/900**	**650/800**	**650/800**	**650/800**	**600/700**
Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [I]	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**
Tunnel / Interpoly max leakage current (A) at 2 V for 10 years data retention [J]	**1 E-24**	**1 E-24**	**5 E-25**	**5 E-25**	**5 E-25**	**2.5E-25**	**2.5E-25**	**2.5E-25**	**1.3E-25**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

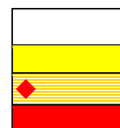


Notes for Tables 72a and b:
[A] In the past Flash devices tended to lag behind the current CMOS technology generation, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.
[B] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling. Tunnel oxides less than 7 nm seem to pose fundamental problems for retention reliability.
[C] Tunnel oxide thickness control must guarantee correct program/erase window
[D] Between minimum and maximum values of the program/erase distributions for Single/Multilevel cells (SLC/MLC)
[E] Time degradation after maximum specification number of write/erase cycles considering no erasing/program voltage correction
F] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue. High-κ interpoly will help reducing the interpoly EOT and maintain constant coupling ratio without loosing retention.
[G] Thickness control to assure correct coupling ratio and minimum thickness for charge retention
[H] For long (>5 min) and short (<5 min) thermal processes to avoid tunnel oxide and device degradation
[I] Uniform step coverage is important to assure charge retention, especially when the floating gate sidewall is electrically coupled with the control gate to enhance the coupling ratio
[J] Maximum leakage current through the tunnel and interpoly dielectrics to assure 10 years data retention. It is calculated considering a floating gate voltage of -2 V when the cell is programmed and a total capacitance that is a half every technology generation. In case of 20 years data retention the leakage current target value is 50% than the reported value.

Table 72b FLASH Non-volatile Memory Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash technology generation NOR/NAND - F (nm) [A]	**28/25**	**25/22**	**22/20**	**20/18**	**18/16**	**16/14**	**14/12**
Flash NOR tunnel oxide thickness (EOT-nm) [B]	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**
Flash NAND tunnel oxide thickness (EOT-nm) [B]	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**
Flash program/erase window min DVT SLC/MLC (V) [D]	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**
Flash erase/program time degradation t_{max}/t_0 at constant V [E]	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**
Flash NOR interpoly dielectric thickness (EOT-nm) [F]	**4–6**	**4–6**	**3–5**	**3–5**	**3–5**	**3–5**	**3–5**
Flash NAND interpoly dielectric thickness (EOT-nm) [F]	**4–6**	**4–6**	**3–5**	**3–5**	**3–5**	**3–5**	**3–5**
Flash interpoly dielectric thickness control EOT (% 3s) [G]	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**
Flash interpoly dielectric T_{max} of formation t >5'/<5' (ºC) [H]	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**
Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [I]	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**
Tunnel / Interpoly max leakage current (A) at 2 V for 10 years data retention [J]	**1.3E-25**	**1.3E-25**	**6E-26**	**6E-26**	**6E-26**	**3E-26**	**3E-26**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



PHASE CHANGE MEMORY

Since the Phase Change Memory (PCM) technology is based on the basic properties of the chalcogenide alloy[1], the integration of the material into a standard CMOS process provides a serious challenge: not just for the single cell concept, already proven to be viable, but also for the manufacturability of very high density NVMs, where the technology can be considered robust only if demonstrated only over many billions of cells.

In a compact, functional array, a PCM data-storage cell is formed with a variable resistor (heater) and chalcogenide material (either in the crystalline or in the amorphous state) with in series a selector device (transistor). Hence, the basic PCM cell has a 1T/1R structure. The type of transistor and of data-storage varies depending on the application and the process architecture strategy. For high-density memory, a more compact cell layout is achieved via the vertical integration of a pnp bipolar transistor[21, 22] while for embedded memory the transistor is a n-channel MOS, where a larger cell size is balanced by a minimum process cost overhead with respect to the reference CMOS.

The integration of the data-storage occurs between the front-end and the back-end of the CMOS process. The "simple" variable resistor, i.e. the heater and chalcogenide system, may be obtained in different ways and the choice is a function of the understanding of the process complexity, current performances, thermal properties and scaling perspective.[23] One possible reported approach uses a sub-litho contact heater with a planar chalcogenide or a modified version with a recession in the contact and chalcogenide confinement, to improve the thermal properties and hence reduce the reset current.[24, 25] A completely different approach relies on the definition of the contact area between the heater and the chalcogenide by the intersection of a thin vertical semi-metallic heater and a trench, called "µtrench", in which the

[1] *Chalcogenides are alloys based on the VI group elements that have the interesting characteristic to be stable at room temperature both in the amorphous and in the crystalline phase. In particular, the most promising are the GeSbTe alloys which follow a pseudobinary composition (between GeTe and Sb2Te3), often referred as GST.*

chalcogenide is deposited.[22] Since the µtrench can be defined by sub-litho techniques and the heater thickness by film deposition, the cell performance can be optimized by tuning the resulting contact area still maintaining a good dimensional control.

The most important integration issue is represented by the chalcogenide alloy itself. The material properties are sensitive to the deposition system and conditions, the etch processes, the sealing dielectrics. The general issues are related to the chalcogenide material contamination due to the integration with other materials in an already established process environment and the thermal stability, with possible degradation due to post-deposition thermal treatments.

FERROELECTRIC RANDOM ACCESS MEMORY (FERAM)

FeRAM was a new addition to the 2001 ITRS, and was the result of collaboration between the FEP and PIDS technology working groups. The critical requirements tables, Tables 73a and b and potential solutions roadmap, Figure 65, were revised based on the result of the questionnaire of PIDS to the FeRAM manufacturers.

Historically speaking, FeRAM devices had been proposed much earlier than semiconductor memory devices.[26] At present however, memory capacity is limited to ~1/1000 that of commodity DRAM, due to limited ferroelectric film reliability and to difficulties associated with capacitor fabrication. These difficulties together with the lack of a "killer application" have constrained commercial production. FeRAMs depend substantially on the continued development of materials such as ferroelectric films making the forecasts presented here somewhat speculative. Nevertheless, the roadmap covers the years 2005 to 2020 in order to provide a strategic overview of the technology directions and the challenges that must be overcome. This section deals with 1) *Feature size*, 2) *Cell size*, 3) *Ferroelectric materials*, and 4) *Minimum switching charge estimation*.

Feature Size—Table 73a shows a feature size of 0.13 µm for commercial products in 2005 using the same criteria as DRAM. In the longer term, beyond 2010, feature size growth is forecasted to be 0.7× every three years. Currently, FeRAM process technology considerably lags leading edge memory such as DRAM and FLASH. In the near term therefore (2005–2008), it is forecasted that FeRAM scaling will occur at an accelerated rate. This forecasted scaling rate yields a 90 nm technology in 2008.

Cell Size—Currently, the mainstream cell structure is the One Transistor-One Capacitor (1T-1C) cell and has replaced the 2T-2C cell that was formerly needed to ensure stable data read out. The 1T-1C configuration is mandatory for the realization of large capacity FeRAM. As far as the capacitor structure is concerned, the change from the planar capacitor type to a stack configuration has resulted in a cell size reduction. A 3D capacitor is assumed to appear in 2010 when the normal Stack structure cannot provide the minimum needed switching charge. The different capacitor configurations are shown in the drawing accompanying Tables 73a and b. The above-mentioned cell structure and capacitor configuration changes are forecasted to reduce the cell area factor to 24 in years 2010–2012 after which the cell area factor will be gradually scaling down. Smaller cell size factors such as ten may appear following the results of learning experiences with leading DRAM technology.

Ferroelectric Materials Alternatives—There are several ferroelectric materials under evaluation at the present time[27], but at present there is no clear, decisive material choice. Two current materials contenders are PZT, or $Pb(Zr,Ti)O_3$ and SBT, or $SrBi_2Ta_2O_9$. SBT has superior fatigue-free characteristics with a Pt bottom electrode and is more suitable for low voltage operation because of its smaller coercive field (E_c). (Fatigue is defined as a resistance to polarization reversal that develops after repeated cycling of the memory capacitor.) SBT is therefore favored to replace PZT, which was first used in production. However, compared to PZT, SBT has a smaller switching charge per unit area, Q_{SW}, which is important since it is more difficult to maintain minimum switching charge when scaling. Also, degradation of film characteristics due to processes after the film fabrication may hamper such replacement. It is also reported that PZT has superior imprint characteristics. (Imprint is defined as the capability to read a signal after a long-time holding during multiple same data write operations. The phenomenon appears as hysteresis shifts along the voltage axis.

The most important issues with PZT and SBT films are suppression of film deterioration that is attributed to oxygen loss, the achievement of stable data read/write characteristics, and data retention. Process improvements are also required for embedding FeRAM. It is important to avoid high temperature annealing or hydrogen incorporation into ferroelectric films after the oxygen anneal used to crystallize the films. For example, low temperature MOCVD ferroelectric film deposition after metal wiring processes, which avoids high temperature anneals, or hydrogen barrier layers may be used. Also, conductive oxides such as IrO_2 or $SrRuO_3$ (SRO) are often used as capacitor electrodes since their use improves ferroelectric film quality.

Physical Vapor Deposition (PVD) and Chemical Solution Deposition (CSD) including Sol-Gel methods are currently the most commonly used methods for ferroelectric film deposition. However, continued scaling dictates the need to shift to methods with better step coverage such as MOCVD. A reported MOCVD study has shown that a (111) oriented PZT film

is very effective at yielding an improved switching charge.[28] Etching of capacitor electrodes is very difficult to do with RIE since the most suitable capacitor electrodes do not have volatile etch products. Therefore sputter etching is widely used. This limits CD control and makes scaling more difficult. High temperature etching for improving sidewall slope of the capacitor is thus being developed to overcome this difficulty.[27]

PZT and SBT are often doped. For instance PZT may be doped with lanthanum, and SBT with niobium. Doping is used to achieve the following film enhancements: leakage current suppression, improved endurance or imprint characteristics, suppression of post process film degradation, and others. Besides PZT and SBT, one of the promising new materials is BLT or $(Bi,La)_4Ti_3O_{12}$,[29] of which characteristics are between the foregoing two.[27] In addition, $BiFeO_3$ (BFO) has gained attention as a new candidate material. BFO has. giant ferroelectric polarization of 150μC/cm^2 or more.[30] Since the characteristic of each film has been improved by efforts in recent years, it seems to be more important to master the material rather than selection.

Estimated Minimum Switching Charge—The estimated minimum switching charge has been derived as follows. The sense amplifier for FeRAM is assumed to be basically the same as that of DRAM. Therefore, the bitline signal voltage was calculated using DRAM data from the 1999 ITRS. These data provide that the capacitance C_S remain constant at 25fF/cell independent of technology generation, and the bitline capacitance is 320fF at the 1 Gb or 0.18 µm generation. Based on this data with the further assumption that bitline capacitance is proportional to $F^{2/3}$, where F is the feature size[31] allows for the calculation of $\Delta V_{bitline}$. The $\Delta V_{bitline}$ is about 140 mV, and we assume that this is needed for the sense amplifier circuit independent of the technology generation. Multiplying $\Delta V_{bitline}$ (140 mV) with $C_{bitline}$ then gives the minimum switching charge.

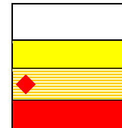
Dividing the minimum switching charge value derived above by the ferroelectric film switching charge per unit area, Q_{SW}, (assumed to be 30 µC/cm^2) then yields the desired capacitor area. If this area is larger than the projected capacitor size, then a 3D capacitor should be adopted. Based on this, a 3D capacitor will be needed by year 2010.

The FeRAM forecast of Tables 73a and b is based on these assumptions and calculations. "Red brick walls" begin to appear in 2008 at the earliest, and become more widespread in 2009. The first priority to break through these walls is the development of highly reliable ferroelectric materials that exhibit negligible post-process degradation.

Table 73a FeRAM Technology Requirements—Near-term Years

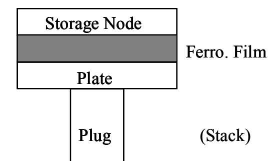
Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Feature size (μm) [A]	0.13	0.11	0.10	0.09	0.08	0.065	0.057	0.05	0.045
Access time (ns) [B]	30	30	20	20	20	15	15	15	10
Cycle time (ns) [C]	50	50	30	30	30	25	25	25	16
Cell area factor: a [D]	34	34	30	30	30	24	24	24	20
Cell size (μm^2) [E]	0.575	0.411	0.300	0.243	0.192	0.101	0.078	0.060	0.041
Capacitor footprint (μm^2) [F]	0.32	0.23	0.158	0.128	0.101	0.049	0.038	0.029	0.018
Capacitor active area (μm^2) [G]	0.32	0.23	0.158	0.128	0.101	0.076	0.069	0.064	0.059
Cap active area/footprint ratio [H]	1.00	1.00	1.00	1.00	1.00	1.55	1.85	2.20	3.31
Height of bottom electrode/F (for 3D capacitor) [I]	n/a	n/a	n/a	n/a	n/a	0.80	1.23	1.73	2.55
Capacitor structure [J]	stack	stack	stack	stack	stack	3D	3D	3D	3D
Cell structure [K]	1T1C	1T1C	1T1C	1T1C		1T1C	1T1C	1T1C	1T1C
V_{op} (Volt) [L]	1.5	1.5	1.2	1.2	1.2	1.0	1.0	1.0	0.7
Minimum switching charge density ($\mu C/cm^2$) at V_{op} [M]	11.4	14.2	19	22	26	30	30	30	30
Minimum switching charge per cell (fC/cell) at V_{op} [N]	36.1	32.3	30.3	28.2	26.1	22.7	20.8	19.1	17.8
Retention at 85°C (Years) [O]	10	10	10	10	10	10	10	10	10
Endurance [P]	1.0E+13	1.0E+14	1.0E+15	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 73a and b:
[A] Feature size "F" is defined as the critical dimension in the cell from the first two companies in mass production, regardless of whether the FeRAM is stand-alone or embedded.
[B] Not referenced.
[C] Not referenced.

[D] a = Cell size/$F1^2$.
[E] Cell size = a $F1^2$.*
[F] $\{(\text{cell size})^{1/2} - (\text{capacitor space})\}^2$ is assumed, where capacitor space = 1.5 F.*
[G] 3D is assumed to be a pedestal structure.
[H] More than 1 for 3D capacitors, otherwise: 1.
*[I] For instance, 0.24 means that the height is 0.24*F.*
[J] See figures (right).
[K] Besides cell structures, configurations are being investigated; ex. Chain-FeRAM.
[L] V_{op}=operational voltage. Low voltage operation is a key issue. Matsushita's 0.18 μm sample with SBT at 2003: 1.1V.
[M] This value can be calculated by [S] divided by [L]. This value is assumed to be 40 for 3D.
[N] Calculated by $\Delta V_{bitline} * C_{bitline}$ with the assumptions that $\Delta V_{bitline}$=140 mV is needed and $C_{bitline}$ is as same as DRAM.
[O] Depends on applications. 85°C comes from the specifications for IC cards.
*[P] 100 MHz*10 years=3E+16. Some 1E+15 is required to compete with SRAM and DRAM.*



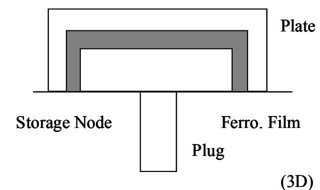
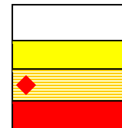


Table 73b FeRAM Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	**11**	**10**	**9**	**8**	**7**	**6**	**6**
Feature Size (µm) [A]	**0.04**	**0.035**	**0.032**	**0.028**	**0.025**	**0.022**	**0.02**
Access time (ns) [B]	**10**	**10**	**8**	**8**	**8**	**6**	**6**
Cycle time (ns) [C]	**16**	**16**	**12**	**12**	**12**	**10**	**10**
Cell area factor: a [D]	**20**	**20**	**16**	**16**	**16**	**14**	**14**
Cell size (μm^2) [E]	**0.032**	**0.025**	**0.016**	**0.013**	**0.010**	**0.007**	**0.006**
Capacitor footprint (μm^2) [F]	**0.014**	**0.011**	**0.0064**	**0.0049**	**0.0039**	**0.0024**	**0.0020**
Capacitor active area (μm^2) [G]	**0.055**	**0.050**	**0.047**	**0.043**	**0.040**	**0.037**	**0.035**
Cap active area/footprint ratio [H]	**3.88**	**4.63**	**7.38**	**8.81**	**10.25**	**15.12**	**17.17**
Height of bottom electrode/F (for 3D capacitor) [I]	**3.18**	**4.01**	**4.98**	**6.11**	**7.23**	**8.87**	**10.16**
Capacitor structure [J]	**3D**	**3D**	**3D**	**3D**	**3D**	**3D**	**3D**
Cell structure [K]	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**
V_{op} (Volt) [L]	**0.7**	**0.7**	**0.7**	**0.7**	**0.7**		
Minimum switching charge density (uC/cm^2) at V_{op} [M]	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Minimum switching charge per cell (fC/cell) at V_{op} [N]	**16.4**	**15.0**	**14.2**	**13.0**	**12.0**	**11.0**	**10.4**
Retention at 85°C (Years) [O]	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Endurance [P]	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Year of First Product Shipment	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Ferroelectric Materials	PZT, SBT							PZT, SBT, New Materials								
Deposition Methods	PVD, CSD, MOCVD			MOCVD, New Methods												

CSD – Chemical Solution Deposition

PZT – P (Zr, Ti)O_3

SBT – $SrBi_2Ta_2O_9$

Figure 65 FeRAM Potential Solutions

An endurance of 10^{15} read/write cycles, which is comparable to other RAMs such as SRAM and DRAM, is required. In order to confirm such endurance values, testing within a practical time period is very critical, since the FeRAM temperature acceleration factor is rather small. Some new ideas such as Non-destructive Read-out scheme, which is free from the limitation of read/write cycles, are being investigated to overcome endurance issues.

Recently FeRAMs are gradually being used for IC cards and for personal authentication, etc. utilizing the feature of fast program speed and high endurance instead of EEPROM or FLASH memory. Security application has a possibility to grow into a large market for FeRAM.

An encouraging fact is that the storage capacity of commodity Flash memory has dramatically increased and is currently almost equal to or even greater than that of DRAM. This increase has occurred because of market demand for large

capacity, nonvolatile memory. FeRAM could also satisfy this market demand and therefore could be another Flash. Global efforts by researchers for FeRAM development are highly encouraged.

CROSS-CUT ISSUES

FEP METROLOGY CROSS-CUT ISSUES

Advanced gate stack, wafer cleaning, and doping process technologies as well as starting materials measurement requirements continue to challenge existing metrology capability. This is highlighted by the near term and long term Metrology Challenges table in the Metrology Roadmap and by the discussion of FEP Metrology in the Metrology Roadmap. The FEP Metrology Technology Requirements Table lists measurement precision for gate dielectric thickness and other FEP films and processes, and the FEP Metrology section indicates that meeting the stated precision is a difficult goal. It is important to note that interfacial measurements for control of gate dielectric processes will be very difficult. The Key Metrology Challenges that are based on FEP needs are:

- Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. Control of gettering.
- Measurement of complex material stacks and interfacial properties including physical and electrical properties.
- The specific FEP requirement is for measurement of high-κ gate stacks including metal gates and interface process control. The addition of SOI and strained silicon requires development of metrology capability.
- 3D dopant profiling

FEP MODELING AND SIMULATION CROSS-CUT ISSUES

In this year's ITRS the FEP challenges surround the introduction of new materials and of non-classical CMOS. This raises various requirements on Modeling and Simulation. Especially, in the coming era of material-limited device scaling, material issues need to be addressed in most modeling areas. This includes among others strained materials – so the importance of modeling of stress and strain is further growing. New device architectures request especially large progress in numerical device simulation, together with improvements of the simulation of the process steps used to fabricate these devices, e.g. the formation of shallow junctions. Both shrinking device dimensions and the non-planar architectures, especially also SOI devices, increase the impact of interfaces because the volumes in between are decreasing. These effects must be appropriately included in the physical process and device models. Process variants are getting increasingly important as devices further scale—a premier example is the redistribution of variance allowance between lithography and etching in this roadmap—and simulation can and must contribute to assessing the impact of such variants on the final device and chip. High-κ dielectrics are required to be introduced by 2008, so modeling must be able to appropriately describe them as soon as possible. The formation of ultra-shallow, abrupt, highly activated drain extensions continues to be a major challenge, and support from modeling is required both to improve the physical understanding for the processes used (e.g. kinetics of dopants and point defects during annealing) and to subsequently optimize them by numerical simulation. This knowledge is also needed for defect engineering that aims at achieving shallower junctions by the exploitation of the interaction between dopant atoms and defects. Furthermore, the reduction of critical dimensions (CD) and their variations including LWR and LER are generally a key issue, and it is highly desirable to use simulation to identify among the many parameters influencing CD the most important ones, in order to minimize experimental effort.

FEP ENVIRONMENT, SAFETY, AND HEALTH CROSS-CUT ISSUES

Refer to the *Environment, Safety, and Health* chapter for comprehensive information and link to a new chemical screening tool (*Chemical Restrictions Table*).

INTER-FOCUS ITWG DISCUSSION

It should be evident that FEP shares numerous issues and dependencies with other Focus ITWGs. Chief among those are issues surrounding gate EOT and leakage requirements with the PIDS and to some extent the Design ITWGs. Other issues with these ITWGs revolve around junction depth and sheet resistance requirements as well as requirements driven by alternate device structures. Resolution of these issues is generally attained through compromise and trade-offs. Despite the relaxation in overall CD tolerance from 10% to 12%, control still remains an issue that was not resolved in this edition of the ITRS and will require ongoing resolution among the FEP, Lithography, PIDS and Design ITWGs. It is further expected that there will be more extensive discussions with PIDS regarding the optimal tradeoff of device parameters in non-traditional MOSFETS such as FinFET and other multi-gate transistors. Other interactions include those with the

Yield Enhancement ITWG to validate different statistical defect models. A very important interaction was with the Interconnect ITWG where members of the FEP surface preparation team provided technical support in the development of interconnect surface preparation and cleaning technical requirements and potential solutions.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

Significant challenges must be overcome to continue shrinking integrated circuit technologies and, in the long term, more radical devices may need to be integrated with CMOS to continue increasing performance. Emerging research devices include both memory and logic devices and while these are still in research, challenging issues must be overcome to integrate these with CMOS. Many of the ERD memory and some of the logic devices are based on conventional charge state technology and could use processing modules that are currently on the FEP roadmap. These will be briefly highlighted. Many of the longer term ERD would use new device materials and introduce new process modules and integration complexity, and these devices are very speculative and intercept timing has not been defined.

Emerging Research Memory Devices

- Nano-floating gate
- Ferroelectric FET
- Insulator resistance change
- Polymer
- Molecular

Emerging Research Logic Devices

- Ferromagnetic (Including magnetic QCA)
- 1D Structures
- Resonant tunneling
- Molecular (Including electric QCA)
- Single electron transistor (SET)
- Spin

Of these devices, the nanofloating gate, SET, and RTDs could use many existing processes, but would probably need an engineered dielectric. The 1D structures (nanotubes, nanowires, etc) will need new processes to control diameter, location, orientation, and new doping processes. The polymer and molecular devices would require low temperature processing and reliable contacts that are compatible with CMOS integration. The other devices will introduce more radical materials that will require significant work to make them compatible with CMOS processing.

The 1D structures require catalyst and CVD processes optimized to control diameter, structure, location, and orientation. They will also need new processes to selectively dope these 1D structures and new contact materials and processes to form the low resistance contacts. Nanowires would require extremely tight control of dopant ion implant dose and energy, and new high-κ gate dielectric processes may be needed to passivate the multi orientation surfaces of Si, SiGe or Ge. Carbon nanotubes will require new doping processes that don't currently exist, and new gate dielectrics and gate electrodes may be needed to control threshold voltages.

Insulator resistance phase change memory and Ferroelectric FET memory would introduce a radical new material that would require a new deposition capability and new etches and cleans. These materials are often complex metal oxides that must be deposited at high temperature, and contact formation and integration may be challenging.

Traditionally some RTDs are fabricated with III-V semiconductors, and this would introduce complex new processes and materials into the FEP for integration with CMOS. Recent work has demonstrated devices made of SiGe that would require integration, but many challenges must be overcome with these materials, particularly to achieve peak/valley I/V ratios > 5. Further, the best use of Si and SiGe based RTD's is their integration into a CMOS gate, which brings another set of complex materials and integration issues.

Spin transistors will require integration of radical new materials with CMOS and this will require new deposition capabilities and introduce much process complexity. These devices are very speculative at this time, but some include GaMnAs, GeMn, as well as spin injection from ferromagnetic materials into the semiconductor that has dramatic contamination challenges.

The level of process complexity for Emerging Research Devices will continue to increase as new materials are used and then integrated on the CMOS platform. This will require development of new deposition, etch, and clean processes and new barrier layer and contact technologies.

CONCLUSION

This chapter of the 2005 ITRS has attempted to clearly identify the challenges and potential solutions to “materials-limited device scaling.” During the next several years front-end processes will require the introduction of a variety of high-κ materials and highly-engineered metal films for applications as diverse as MOSFET gate stacks, DRAM storage capacitors, and flash-memory storage devices. In addition to these new materials, new device structures, such as FinFET, will be introduced in order to meet performance requirements. Market growth for alternative memories will also require the development and optimization of a broad class of ferroelectric, magnetic, and phase-change thin film materials. Underlying these device changes are rapidly evolving requirements for substrates, such as SOI, and the need for an even larger, 450 mm diameter substrate, within the next 7 years.

The transition from extended bulk CMOS to non-classical device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time—some manufacturers choosing to make the transition to non-classical devices earlier, while others emphasize extensions of bulk technology. To support this probable scenario we have provided metrics for parallel paths showing what is required to extend classical CMOS and what can be gained by making a transition to other device structures such as fully-depleted SOI and multi-gate.

We also note the acceleration of flash-memory applications as a new driver of material technologies, such as high-κ dielectrics, and of process technologies, such as critical dimension etching. The rapid expansion of the market for flash memories will bring more focus on the material and process challenges for these devices.

Pathways around potential barriers are found by close cooperation between different ITRS Technology Working Groups. This was demonstrated over the past two years by continuous discussion of the physical gate length variation challenge between the FEP, PIDS, Lithography, and Design groups. This collaboration resulted in changes across several chapters of the ITRS including a shift between printed dimensions and etch bias, a redistribution of allowable variation, and a recognition that devices can be economically manufactured with slightly higher variation than previously prescribed. Continued cross-TWG collaborations, such as this, will be crucial to finding pathways around future barriers.

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STARTING MATERIALS

SURFACE PREPARATION

THERMAL, THIN FILM, DOPING AND ETCHING

DRAM STACKED CAPACITOR

PHASE CHANGE MEMORY

FERROELECTRIC RANDOM ACCESS MEMORY (FERAM)

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