INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

FACTORY INTEGRATION

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FACTORY INTEGRATION[1]

Factory Integration section of the ITRS focuses on integrating all the factory components needed to efficiently produce the required products in the right volumes on schedule while meeting cost targets. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, and other manufacturing productivity improvements. This in turn requires a factory that can fully integrate all other factory components. Preserving the decades-long trend of 30% per year reduction in cost per function also requires capturing all possible cost reduction opportunities. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs. (*Contributors to this chapter are included online.*)

The success and market growth of semiconductors have been driven largely by continuous improvement to cost per function. Many factors have led to these productivity gains including process technology shrinks, wafer size changes, yield improvements, and manufacturing productivity. The era of non-incremental technology introductions (high-κ gate dielectric, metal gates, Cu/low-κ interconnect, etc.), complex product designs and large-scale transistor integration, and process complexity (such as System On a Chip with 30 or more mask layers) is making the pace of productivity improvements harder to sustain when compared with historical norms.

One positive example where Fab productivity gains have continued in a cost-effective manner is the transition to 300 mm wafers where collective wisdom of industry has abated the ballooning increase in the cost of a new Fab. Nevertheless, Fab investment costs continue to increase driven both by the cost of technology as well as the desire to build larger factories to get economies of scale.

Overall Factory Integration scope addresses several challenges that threaten to slow the industry's growth, including:

1. *Integrating complex business models with complex factories*—Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high mix and volatile market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. The factory now must integrate an even larger number of new and different equipment types and software applications to meet complex market objectives and customer requirements. High mix and low-volume product runs are making mask cost, fabrication, and factory integration extremely difficult in a market where average selling prices (ASPs) are declining. Lack of robust and fully featured software systems to manage the complexity of factory and equipment control is also adding to our challenges.
2. *Production equipment reliability, utilization, and extendibility*—Production equipment is not keeping up with availability and utilization targets, which has an enormous impact on capital and operating costs. The industry is unable to effectively reuse equipment or skills due to the rapid introduction of new equipment (157 nm and EUV lithography) and materials (SOI, high-κ gate stack, low-κ dielectrics, etc.).
3. *Maturing 300 mm factory challenges—We are now moving from ramping to maturity on the 300 mm factories and hence it is necessary to focus on improving and sustaining 300 mm efficiency targets such as*: 1) >2.25 more die per wafer than 200 mm, 2) >30% cost per die reduction, 3) 100% automated materials handling system (AMHS) interbay and intrabay systems for operational flexibility and cost improvements, 4) the ability to track and run different recipes for each wafer within a carrier for operational flexibility and 5) reduction in utilities, power consumption and emission.
4. *Post Bulk CMOS and next wafer size manufacturing paradigm*—the conversion to novel devices and the next wafer size beyond 300 mm (i.e., 450 mm wafers) represent key inflection points for semiconductor manufacturing. Novel devices beyond bulk CMOS and their potential impacts to equipment and manufacturing are not well defined, but are expected to be significant. Conversion to wafers larger than 300mm represents another change opportunity to improve manufacturing cost effectiveness and will be an important factor in the semiconductor industry's ability to continue realizing Moore's law.

[1] *Factory integration is the combination of factory operations, production equipment, facilities, material handling, factory information and control systems, and probe/test manufacturing working in a synchronized way to profitably produce complex products for a time-sensitive market.*

In order to address these challenges the following fundamental semiconductor manufacturing attributes must be improved:

- Cost per unit area of silicon—manufacturing cost per unit area of silicon is a measure of productivity. The capital cost of a factory has grown significantly each year, from $50M US in the 1980s to over $3B US in 2005.[2]
- Time to ramp a factory to high-volume production with high yields—decreasing time to ramp a factory to high-volume production and high yield has more economic impact than reducing operating costs. New factories must be built and ramped to mature production at a much faster rate as reflected in Technology Requirements tables. Existing factories must be upgraded faster without impacting ongoing production.
- Increasing flexibility to accommodate technology and business changes—Technology advances and the globalization of manufacturing enterprises have led to a decrease in cost for electronic components. This enables new markets to open and creates the need to increase the pace of new product introduction. The flexibility to accommodate these changes in business expectations must improve without significant cost impacts.

SCOPE

A semiconductor factory extends across several manufacturing domains (Figure 80), which include wafer manufacturing or fabrication, chip manufacturing that involves probe/e-test, backgrind, and singulation, and finally product manufacturing where the final package is assembled and tested. Silicon substrate manufacturing and product distribution are outside the scope of factory integration.

In order to clearly understand the integrated factory requirements and at the same time define measurable and actionable metrics, the factory integration is divided into five thrusts, or functional areas, that are required to perform semiconductor manufacturing. The five functional thrusts are Factory Operations, Production Equipment, Material Handling, Factory Information & Control Systems, and Facilities. Factory Operations, and its associated factory business model, is a key driver of requirements and actions for the other four thrusts. Overall, these five thrusts are used to clarify how difficult challenges translate into technology requirements and potential solutions. In addition to these five thrust areas, the factory integration section also addresses the cross-cut issues and also key focus areas that cut across all these five thrusts.

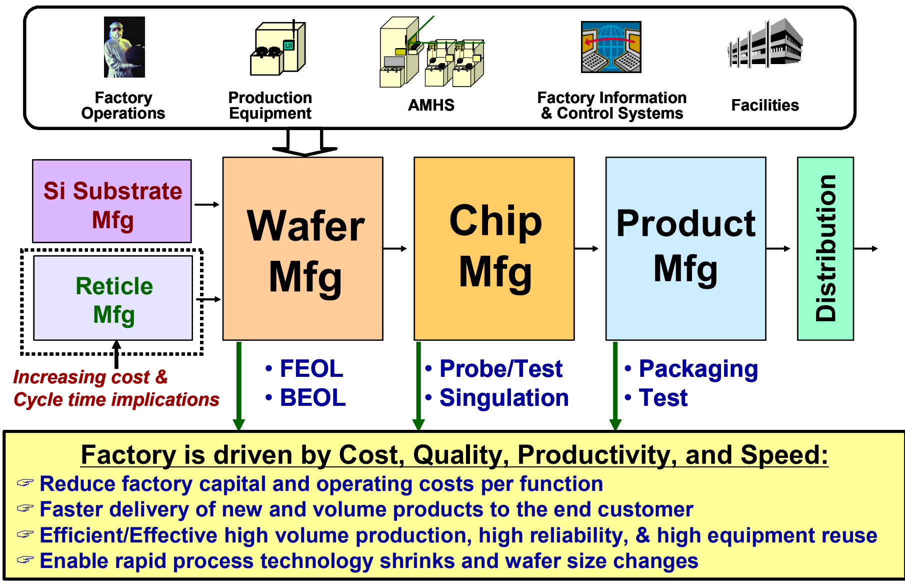


Figure 80 Factory Integration Scope

DIFFICULT CHALLENGES

Difficult challenges associated with factory integration span multiple technology generations and cut across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry

[2] *Strategies for determining or dealing with the upper limit of factory cost are beyond the scope of this chapter.*

convenience to minimize disruptions to operating factories. Near-term difficult challenges for the factory include business, technical, and economic issues that must be addressed.

Table 84a Factory Integration Difficult Challenges—Near-term

Difficult Challenges ≥32 nm	*Summary Of Issues*
Responding to rapidly changing, complex business requirements	Many new and co-existing business models including IDM, Foundry, Fabless, Joint Ventures, Collaborations, other Outsourcing, etc need to be considered in the Factory Integration Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design -> prototype and pilot -> volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with high mix manufacturing as the model in response to diversified customers' requirement Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance to optimize output and improve cycle time for high mix factories Ability to constantly adjust equipment loading to keep the factory profitable Manufacturing knowledge and control information need to be shared as required among disparate factories
Achieving growth targets while margins are declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes
Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Small process windows and tight process targets at >45nm in many modules make process control increasingly difficult Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

Table 84b Factory Integration Difficult Challenges—Long-term

Difficult Challenges <32 nm	*Summary of Issues*
Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability) Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting process requirements at 65nm and 45nm generations running production volumes	Small process windows and tight process targets at 45nm generations in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging factory paradigm and next wafer size change	Uncertainty about the next wafer size [450mm] and the conversion timing [See Backup material as a link in the electronic chapter at http://public.itrs.net.] Traditional strategies to scale wafers and carriers for the next wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable the next wafer size conversion [to 450 mm] at an affordable cost

TECHNOLOGY REQUIREMENTS

To achieve the primary goals listed above, we need to evaluate the technology requirements and identify potential solutions to the difficult challenges. This is accomplished in the Factory Integration by breaking up the section into the following five integrated and complementary functional areas:

- Factory Operations (FO) cover the set of policies and procedures that are used to plan, monitor and control production within a factory.
- Production Equipment (PE) covers process and metrology equipment (including embedded controllers) and their interfaces to other factory elements.
- Automated Material Handling Systems (AMHS) covers transport, storage, identification, tracking, and control of direct and indirect materials.

- Factory Information and Control Systems (FICS) includes computer hardware and software, manufacturing execution and decision support systems, factory scheduling, control of equipment and material handling systems, and process control.
- Facilities include the infrastructure of buildings, utilities, and monitoring systems.

Table 85 provides a summary of key focus areas and issues for each of the factory integration functional areas beyond 2005. The challenges stemming from Next wafer size (NWS) will be addressed in a separate table.

Table 85 Key Focus Areas and Issues for FI Functional Areas Beyond 2005

Functional Area	*Key focus and issues*
Factory Operations (FO)	1) Reduce mfg cycle times, 2) Improve Equipment Utilization, 3) Reduce Losses from High Mix.
Production Equipment (PE)	1) NPW reduction, 2) Reliability Improvement, 3) Run rate (throughput) improvement, 4) 1.5 mm wafer edge exclusion challenge.
Automated Material Handling Systems (AMHS)	1) Increase throughput for Traditional and Unified Transport, 2) Reduce Average Delivery times, 3) Improve Reliability
Factory Information and Control Systems (FICS)	1) Increase Reliability, 2) Increase Factory Throughput, 3) Reduce or Maintain Mask Shop Cycle Time, 4) Reduce Costs
Facilities	1) Factory Extendibility, 2) AMC, 3) Rapid Install/Qualification, 4) Reduce Costs

FACTORY OPERATIONS

Factory operations refers to the efficient and effective application of resources and integration of other facets of manufacturing such as information and control system, material handling, equipment, and facilities in order to maximize throughput, minimize cycle time, work-in-progress (WIP) and maintain lower operating cost. Equipment metrics, particularly, run rate improvement, availability, and utilization are also included in the technology requirements table.

The Factory Operations Technology Requirements table lists the high-level production metrics and their required improvement targets through time in order for a semiconductor factory to achieve competitive performance characteristics. The factory operational metrics are cycle time per mask level, X-factor for hot lots and non-hot lots, lots per carrier, and wafer layers per day per headcount. These metrics are further segmented to differentiate between two kinds of factories: high volume, high mix and high volume, low mix. These metrics are primarily focused around 40K WSPM high-mix factories with short life cycle products. In addition, there are a set of factory ramp-up metrics—first tool move-in to first full-loop wafer out, technology-generation-to-technology-generation change over, and floor space effectiveness.

The performance characteristics of a factory that best defines its competitive posture will depend on a number of factors. For example, there is a well-established trade-off between cycle time and asset utilization, with higher asset utilization leading to higher cycle times. Thus, each factory must balance the value of lowering cycle time for the business segment(s) in which it participates versus the cost of the lower asset utilization. Similarly, a high-mix factory will have operational characteristics and will need decision support tools that will be different than those for a factory that is low mix and high volume. Asset utilization is captured in the form of equipment utilization, availability, and capacity degradation. Another metric, overall equipment effectiveness (OEE) is not explicitly mentioned in the operations table since the key elements of OEE namely, utilization and availability are captured in the technology tables.

Once the fundamental performance characteristics have been established for a factory, there is a continuing need for increased productivity. This increased productivity is reflected either in lower cycle times or in increased throughput for the same capacity investment. It is also essential to address average number of wafers processed before a reticle change since the high-mix factory coupled with next wafer size (such as 450 mm) wafer would demand lesser number of wafers processed between reticle changes.

These requirements are meant to provide guidance so that research can be better focused toward the innovations required to achieve these objectives. These innovations are envisioned to be in the form of new concepts, policies, models, algorithms, etc. These will be expressed in the form of software applications that would be developed and released to manufacturing. These software applications will be integrated into the overall factory information and control systems, either as decision support tools or as execution tools. These tools will help to drive factory productivity improvements to achieve Factory Operations objectives.

The Factory Operations potential solutions are classified into planning decision support (DS) tools at the strategic level and tools for running the factory at the tactical or execution level. The solution components for these two levels are quite different but are essential in order to effectively manage high-mix factories. The tactical tools need quick access to transactional data whereas the DS tools need large sets of data with several analysis/reporting options. The stringent engineering requirement is driving need for more data that is resulting in data explosion. It is critical to not only collect necessary data but also to develop intelligent analytics and algorithms to identify and use the right signals to make data driven decisions.

Demand information propagated over the factory network (Fab/sort/assembly/test) is neither accurate nor responsive, which results in poor factory and supply chain planning. Successful determination of where, when, and in what quantities the products are needed is essential for improving manufacturing productivity. The cost of capital equipment is significantly increasing and now constitutes more than 75% of wafer Fab capital cost and via depreciation a significant fraction of the fixed operating costs as well. Reducing the impact of these increasing costs on overall wafer costs requires improvements in equipment utilization, availability, and capacity loss due to set up (for high mix), tool dedication, etc. Effective factory scheduling also plays a key role in improving equipment reliability and utilization and it also leads to improved cycle time and On-Time-Delivery (OTD). In order to effectively utilize the expensive production equipment, it is imperative that effective scheduling and dispatching tools be utilized. Several factors complicate Fab scheduling. These include AMHS that is not fully integrated with lot scheduling tools as well as scheduling policies that are not effectively integrated into lot scheduling tools. A real-time scheduling and dispatching tool integrated with AMHS and incorporating preventive maintenance (PM) scheduling, and resource scheduling policies is required to reduce WIP, improve OTD and improve capacity utilization. (Refer to the *Factory Operations Potential Solutions table*.) (Additional details on *Factory Operations technology requirements and potential solutions* are provided as links)

Factory Operations Technology Requirements

Table 86a Factory Operations Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
Non-hot lot (average of 94% lots)									
Cycle time per mask layer (days).	1.6	1.5	1.5	1.5	1.4	1.4	1.2	1.2	1.2
X-Factor [1]	3.2	3.1	3.1	3.1	3.05	3.05	3.05	3.05	3.05
Hot lot (average top 5% of lots)									
Cycle time per mask layer (days)	0.62	0.55	0.55	0.55	0.51	0.51	0.0.47	0.47	0.47
X-Factor [1]	1.4	1.3	1.3	1.3	1.3	1.3	1.2	1.2	1.2
Super hot lot (average top 1% of lots)									
Cycle time per mask layer (days)	0.33	0.32	0.32	0.32	0.31	0.31	0.3	0.3	0.3
High-mix capacity degradation	11.67%	10%	8.33%	6.67%	5%	5%	5%	5%	5%
Bottleneck equipment [2] [3]									
Utilization	90%	92%	92%	92%	94%	94%	94%	94%	94%
Availability	92%	94%	94%	94%	96%	96%	96%	96%	96%
Wafer layers/day/head count	55	61	61	61	67	67	73	73	73
Number of lots per carrier (high mix) [4]	Multiple	Multiple	Multiple	Multiple	Multiple	Multiple	Multiple	Multiple	Multiple
Facilities cycle time (months)									
1st tool to 1st full loop wafer out (months)	3.5	3	3	2.5	2.5	2.5	2	2	2
Generation-to-generation change-over (weeks)	13	12	12	12	11	11	10	10	10
Floor space effectiveness	1×	1×	1×	1×	1×	1×	1×	1×	1×
Average number of wafers between reticle changes	40	35	30	25	20	20	20	20	20

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known

Manufacturable solutions are NOT known

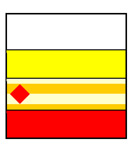
Notes for Tables 86a and b:
[1] X-factor is shown for continuous improvement. Actual X-Factor values will depend heavily on raw process time for a given process technology or generation.
[2] A bottleneck tool usually refers to a lithography tool
[3] Utilization and Availability are shown for continuous improvement
[4] High mix is defined as the followings:

- *Running > three technology generation concurrently in the same Fab*
- *Running > ten process flows within the same technology generation*
- *Running > 50 products concurrently through the Fab*
- *Many of small lots of 1–10 wafers in size*
- *Running an average of < 50 wafers between Reticle changes for each lithography expose equipment*
- *Lot starts are based on customer orders. There is a daily variation in the number of lots you start with different products and process flows*
- *At least five large volume products (product flows) with no one product having >50% of production volume*

Table 86b Factory Operations Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Non-hot lot (average of 94% lots)							
Cycle time per mask layer (days).	1.13	1.13	1.13	1.05	1.05	1.05	1.05
X-Factor [1]	**3.05**	**3.05**	**3.05**	**3**	**3**	**3**	**3**
Hot lot (average top 5% of lots)							
Cycle time per mask layer (days)	**0.44**	**0.44**	**0.44**	**0.39**	**0.39**	**0.39**	**0.39**
X-Factor [1]	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1.1**
Super hot lot (average top 1% of lots)							
Cycle time per mask layer (days)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
High-mix capacity degradation	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
Bottleneck equipment [2] [3]							
Utilization	**94%**	**94%**	**94%**	**94%**	**94%**	**94%**	**94%**
Availability	**96%**	**96%**	**96%**	**96%**	**96%**	**96%**	**96%**
Wafer layers/day/head count	**81**	**81**	**81**	**89**	**89**	**89**	**89**
Number of lots per carrier (high mix) [4]	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**	**Multiple**
Facilities cycle time (months)							
1st tool to 1st full loop wafer out (months)	**1.5**	**1.5**	**1.5**	**1**	**1**	**1**	**1**
Generation -to-generation change-over (weeks)	**9.5**	**9.5**	**9.5**	**9**	**9**	**9**	**9**
Floor space effectiveness	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**	**1×**
Average number of wafers between reticle changes	**15**	**15**	**15**	**13**	**13**	**13**	**13**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Explanation of Items for Factory Operations Requirements

Item	*Explanation*
Factory cycle time per mask layer (non-hot lot)	*Measure of total time to process a wafer lot per mask layer. Assume 25 wafers per lot. For example, if a process has 20 masking layers, and cycle time per mask layer is 1.5, then total factory (fabrication) cycle time is 20 × 1.5 = 30 days. A key metric of time to money.*
Factory cycle time per mask layer (hot lot)	*Same definition as of above. Factories typically prioritize these lots over non-hot lots. As a result, the cycle time for hot lots is < 50% of non-hot lots. Assume 25 wafers per lot. New product lots can be processed as hot lots*
Factory cycle time per mask layer (super-hot lot)	*Assume ~ five wafers per lot. Factories typically prioritize these lots over conventional lots, hold tools downstream to rapidly move them through the process flow and reduce sampling rates. As a result, the*

Item	Explanation
	cycle time for super hot lots are shorter than hot lots.
X-factor [1]	*X-factor is the total cycle time (queue time + hold time + raw process time + travel time) divided by the raw process time (RPT). Raw process time for a lot at a tool is the time it takes to process a lot on the tool. Generally this time will be from when the tool starts to process the lot (and thus cannot be moved to another tool for processing) until the lot is finished and can be moved to the next operation. Raw process time for a technology is the sum of the raw process times for each of the tools in the processes in the technology plus the total travel time. Raw process time is not shown in the technology table since X factor and cycle time per mask layers are shown.* *The relationship is: cycle time = raw process time × X-factor* *Assume current cycle time is 1.6 days/mask level and the X-factor for normal lots is 3.2 at 80% utilization. Thus RPT for normal lots = 1.6/3.2 = 0.5* *Assume same RPT for normal and hot lots. X-factor for hot lots is determined by "last-in-first-out" priority*
High-mix capacity degradation	*The penalty paid by factory operations in terms of lost capacity due to high mix (measured in %). This capacity loss is caused by reduced batch sizes, increased set ups, etc. This is the average for all tool sets in the line. Degradation increases from 5% (low mix, 25 wafers/FOUP, change recipe/setup every ten lots, single product on a wafer) to maximum. Of 15% (high-mix, <25 wafers/FOUP, change recipe/setup for every FOUP, multiple product in a lot). This metric impact the utilization of effective capacity, which is best, defined as being (1–(Idle No WIP)).* *Idle No WIP is the fraction of a tool's capacity that is idle when the tool is up and there is no WIP either waiting to be run on the tool or in transit to the tool. In some cases, No operator can also contribute to utilization of effective capacity.*
Bottleneck equipment utilization and availability [2] [3]	*Availability is defined in SEMI E10[3] as "the probability that the equipment will be in a condition to perform its intended function when required."* *Utilization is defined in SEMI E10 as "the percentage of time the equipment is performing its intended function during a specified time period." All based on 25-wafer lot. Availability includes setup, idle and processing time, utilization is considered as time directly adding value of constraint equipment (usually lithography tools) measured in % without sacrificing cycle time. Constraint equipment utilization (normally lithography) is the pulse of the Fab and usually determines the output capacity.*
Wafer layers/day/head count	*Measure of productivity that includes equipment output and direct labor staffing.* *Equation = total wafer processed per day in the factory × number of lithography mask layers/total number of direct labor employees per day.*
Number of lots per carrier (high mix) [4]	*The number of lots in each carrier that need to be tracked, monitored, and processed. For high-mix factories, the number of wafers can be <25 per lot and the production equipment must be able to run a different recipe and/or parameters for each wafer within the carrier. It also requires the factory information and control system to be able to track, monitor, and control the wafer at each point the factory and within the equipment. The factory information and control system must have the ability to drive the production equipment to run different recipes and/or parameters for each wafer. Multiple lots per carrier mean more than one product lot. High mix is at least five large volume products (product flows) with no one product has >50% of production volume.*
Time to 1st wafer out time (months) –1st tool move-in to 1st full loop wafer out	*A key metric of new factory ramp-up time. This is the time elapsed in months from first tool move-in to first full loop wafer out.*
Generation-to-generation change-over (weeks)	*The time in weeks for a new product or process to be implemented in a working factory (production equipment move-in to first lot out). About 80% of the current equipment is reused and 20% is new. Equipment already in place or available and may need to be qualified. Furnace and wet process equipment are not replaced. Not serial number 1 equipment*
Floor space effectiveness	*This is a measure of equipment installation density in the clean room, and drives the requirement for the smallest footprint and the fastest run rate for production equipment.* *Equation = (Number of processing steps in the Fab × WSPM/(floor space area × 30 days).* *For every major generation, one additional metal layer is added, and assuming a 4% increased run-rate improvement each year (by reduced processing time per wafer), the best that can be mathematically achieved is getting the same output per square meters of clean room for each new generation.*
Average number of wafers between reticle changes	*This is a measure of how efficiently high-product mix can be handled in the factory.* *As the metric indicates, it is the average number of wafers processed before a reticle is changed.*

FOUP—front opening unified pod

[3] *SEMI E10-0699E: Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM).*

PRODUCTION EQUIPMENT

The scope of production equipment section includes all process and metrology equipment in the factory. Also included are tool embedded controllers, front-end module (EFEM) and load ports for carrier and wafer handling, software, and firmware interfaces to host systems, and all facilities interfaces of the equipment. Equipment metrics, particularly run rate improvement, availability, and utilization, are also included in the technology requirements table.

Effective design and control of production equipment is central to controlling the cost of processing each unit area of silicon. The industry's growth rate will not be sustainable in the future if increasing capitalization cost trends continue without significant improvement in productivity. There are several factors that impact productivity of the equipment. They include the following:

5. Finding breakthrough solutions for increasing equipment reliability, availability and utilization.
6. Reducing variation within and between equipment and attaining chamber and tool matching.
7. Improving inter-operability and exchangeability by improving compliance to physical and data interface standards.
8. Extending equipment lifetime to support multiple technology generations.
9. Achieving more effective use of utilities and consumables, including reduction of non-product wafers, while simultaneously reducing environmental impacts.
10. Reducing "relative or normalized equipment capital cost" (rate at which equipment cost increases vis-à-vis requirements for process capability) by speeding up the processing rate. This will drive reduced cost of ownership.
11. Reducing intrinsic setup time that comes with high-mix factories through quick turn around setup options.
12. Improving equipment design to reduce losses from high product mixes (i.e., set-up time reduction or elimination).

The Production Equipment potential solutions are prioritized towards attaining the improvements listed above. Equipment standards and interoperability solutions directly enable cost reduction of tools. Reliability and utilization improvements can be achieved by innovative solutions in the area of *in situ* monitoring, advance process control capability, design for manufacturing, smarter embedded controllers, self-diagnostics, remote diagnostic capability, and single-wafer level tracking and control. More efficient equipment designs are achieved through the use of higher efficiency power distributions systems within the tool, more efficient tool-heat-load removal methods, and optimized recycling and reuse of water. Another high priority area is finding ways to extend the life of the equipment to support multiple technology generations. Potential solutions to improve flexibility of the equipment and to reduce intrinsic setup time will reduce cycle time and increase tool utilization, and will deliver much needed capabilities in carrier-level and wafer level integrated flow and controls. Other important areas are finding innovative solutions for ramp-up cycle time reduction and spares cost reduction. An additional emerging focus area requiring innovate solutions is the prevention control of Airborne Molecular Contamination (AMC). Lastly, efficient and cost-effective equipment development will be a critical milestone in the industry transition to the next wafer processing size. (See the *Production Equipment Potential Solutions table*.) (Links are provided for details on *Production Equipment technology requirements, potential solutions,* and for Agile Manufacturing and e-Manufacturing potential solutions.)

PRODUCTION EQUIPMENT TECHNOLOGY REQUIREMENTS

Table 87a Production Equipment Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
Throughput improvement (run-rate) per year	4%	4%	New base	4%	4%	New base	4%	4%	>0%
New non-product wafers (NPW) as a % of wafer starts per week	<14%	<13%	<12%	<11%	<11%	<11%	<10%	<10%	<10%
Overall NPW activities versus production wafers activities	10%	7%	7%	7%	5%	5%	5%	5%	5%
% capital equipment reused from previous generation	>90%	>90%	>90%	>90%	>90%	>90%	>90%	>90%	Limited
Wafer edge exclusion	2 mm	2 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5mm
Equipment lead time from setup to full throughput capable	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks
Process availability (A80)	92%	>92%	>94%	>95%	>95%	>95%	>95%	>95%	>95%
Metrology availability (A80)	96%	96%	96%	>96%	>97%	>98%	>98%	>98%	>98%
Intrinsic setup time reduction, vs. base	6%	10%	12%	12%	15%	15%	17%	17%	> 17%
Ability to run different recipes and parameters for each wafer	Partial	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
248 nm lithography scanner productivity (wafers outs per week per tool)	7400	7400	7700	7700	8000	8000	8000	8000	8000
193 nm lithography scanner productivity (wafers outs per week per tool)	5300	5300	5600	5600	6000	6000	6000	6000	6300
Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	90	80	70	60	50	50	35	35	35

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

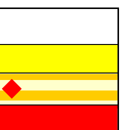


Table 87b Production Equipment Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Throughput improvement (run-rate) per year	4%	4%	4%	4%	4%	4%	4%
New non-product wafers (NPW) as a % of wafer starts per week	<9%	<9%	<9%	<9%	<9%	<9%	<9%
Overall NPW activities versus production wafers activities	5%	5%	5%	5%	5%	5%	5%
% capital equipment reused from previous generation	Limited	Limited	Limited	Limited	>70%	>70%	>70%
Wafer edge exclusion	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm	1.5 mm
Equipment lead time from setup to full throughput capable	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks	4 wks
Process availability (A80)	>95%	>95%	>95%	>95%	>95%	>95%	>95%
Metrology availability (A80)	>98%	>98%	>98%	>98%	>98%	>98%	>98%
Intrinsic setup time reduction, vs. base	> 17%	> 17%	> 17%	> 17%	>20%	>20%	>20%
Ability to run different recipes and parameters for each wafer	Yes	Yes	Yes	Yes	Yes	Yes	Yes
248 nm lithography scanner productivity (wafers outs per week per tool)	8000	8000	8000	8000	8000	8000	8000
193 nm lithography scanner productivity (wafers outs per week per tool)	6300	6300	6300	6300	6500	6500	6500
Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	25	25	25	25	18	18	18

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Explanation of Items for Production Equipment Requirements

Item	*Explanation*
Throughput improvement (run-rate) per year (high mix)	Throughput improvements are achieved by reducing the processing time per wafer, and optimizing non-value added wafer handling and wafer-staging steps inside the equipment and by increasing the efficiency of the equipment embedded controller. Also eliminate any dead time between sequential wafer processing steps. If current run-rate is 100 wafers/hour, the required run-rate next year is (100 × 1.04) = 104 wafers/hour and (104 × 1.04) = 108 wafers/hour the following year.
New non-product wafers (NPW) as a % of wafer starts per week	Ratio of new non-production wafer consumption divided by total production wafer started for the same period. Typical non-product wafers include test wafers, monitor wafers, calibration wafers, dummy wafers.
Overall NPW activities versus production wafers activities	Ratio of total non-production wafer activities (process moves, including recycling wafers) divided by total production wafer activities for the same period. Typical non-product wafers include test wafers, monitor wafers, calibration wafers, dummy wafers. Consumption quantity includes both new and reused (reclaimed) non-product wafers.
% capital equipment reused from previous generation	% of capital (production) equipment quantity that is reused from generation N to N+1. Example: if X number of production equipment of generation N can be reused for generation N+1 and the total number of production equipment for generation N+1 is Y, then equipment reuse % is defined as X/Y.
Wafer edge exclusion	Dimension in millimeters measured from wafer edge that is not used for printing saleable chips. Includes front and rear sides of wafer.
Equipment lead time from setup to full throughput capable	Time elapsed between when tool has been installed and production ready till the time the equipment has been qualified to run wafers at the quoted throughput (wafers per hour). This is specifically applicable for lithography tools (worst case).
Process availability (A_{80})	Availability is 100% minus (scheduled downtime % – setup% + unscheduled downtime %) of the process (non-metrology) equipment (80% percentile). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.
Metrology availability (A_{80})	Availability is 100% minus (scheduled downtime % – setup% + unscheduled downtime %) of the process (non-metrology) equipment (80% percentile). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.
Intrinsic setup time reduction year to year	Intrinsic setup time reduction is mainly dependent on improvements to process equipment with quick setup capability (software, hardware improvements) and faster qualification capability. This metric will impact capacity.
Ability to run different recipes and parameters for each wafer	Ability for production equipment to run a different recipe and/or parameters for each wafer within a carrier. This facilitates the ability to have multiple lots per carrier. Base requirements also include the ability to track, monitor, and control the wafer at each point the factory or within the equipment. For production equipment, it impacts the extent of "recipe cascading" that enables equipment to run in a continuous (non-stop) mode between lots in the same carrier and between sequential carriers.
248 nm lithography scanner productivity (wafers outs per week)	The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 248 nm scanners in the Fab.
193 nm lithography scanner productivity (wafers outs per week)	The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 193 nm scanners in the Fab.
Maximum allowed electrostatic field on wafer and mask surfaces (V/cm)	Wafer and mask surface electric fields measured when they are removed from their carriers. Refer SEMI standards E78[4] and E43[5] for measurement methods.

MATERIAL HANDLING SYSTEMS

Ergonomic and safety issues coupled with the need for efficient and rapid material transport are the major drivers in defining material handling systems for the 300 mm wafer generation and beyond. The automated material handling systems must have acceptable Return on Investment (ROI) and must interface directly with all inline (i.e., used in normal process flow) production equipment. With the increase in 300 mm production equipment size, the utilization of floor space in the factory must improve. Solutions to provide short lead and install times, and better utilization of floor space through integration of process and metrology equipment must be developed.

Figure 83 is based on the premise that as demands on the material handling system continues to increase, the drive toward combining interbay and intrabay transport function into one integrated capability, known as a direct or tool-to-tool direct transport system, will be a reality. This does not imply one system or even one system from one supplier. The system may

[4] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*

[5] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

be composed of interoperable sub-systems from multiple (best of breed) suppliers and will have the ability to avoid sending lots through stockers.

For efficient production in such an environment, there will be a need to integrate WIP scheduling and dispatching systems with storage and transport systems with the goal to reduce product processing cycle time, increase productivity of process tools, reduce storage requirements, and reduce total movement requirements. The priority for direct delivery will be as follows:

1. Super hot lots (< 1% of WIP) and regular hot lots (~5% of WIP).
2. Ensure bottleneck production equipment is always busy.
3. Utilize direct tool-to-tool moves for gating metrology process steps, send-ahead wafers and other lots opportunistically. Development is currently underway and qualification/pre-production should occur as early as 2004–2006.

Concurrent with the drive towards direct tool-to-tool transportation systems in 300mm factories to transport WIP, IC makers, running high-volume/high-mix production will require automated transport for reticles in reticle standard mechanical interface (SMIF) pods. It is expected that automated material handling systems for WIP and reticles will need to demonstrate similar performance characteristics. IC makers may choose different storage schemes in a reticle stocker. One case calls for bare reticle storage in the stocker and the other being stored in reticle SMIF pods. Potential solutions for reticle transport systems must not negatively impact the lithography equipment's footprint, run rate, and ease of installation or de-installation. The adoption of automated reticle transport systems by IC makers will depend on the business model employed at the factory.

Over the next four years, material handling equipment/component failures must be reduced by ~50%, while the time to repair each failure is similarly reduced. Throughput must be increased substantially and achieved with reduced delivery time. Furthermore, the material handling system needs to be designed so that it can accommodate the extendibility, flexibility, and scalability demands on the factory.

Initial discussions for the next wafer size transition (450mm) have begun and initial concepts for carrier capacity have implications on AMHS that will need to be researched over the next few years and potentially developed/qualified by 2012. Some challenges will be to have an AMHS that can potentially handle ~5x increase in Moves per Hour (MPH), ~5x increase in reliability requirements, etc. The trade off between lot size and MPH increase will need to be evaluated. The AMHS design will need to be revisited along with investigation into whether the wafer transport/storage (near tool) will be within the scope of the AMHS (EFEM). Other items that will impact the AMHS design will be the 450mm factory size, factory layout and factory throughput requirements.

(Link to *the Material Handling potential solutions table.*) (Refer to supplemental files *for additional details on Material Handling technology requirements and potential solutions.*)

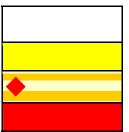
Table 88a Material Handling Systems Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm)(contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*	*450*
Transport E-MTTR (minutes) per SEMI E10	**10**	**9**	**9**	**8**	**8**	**8**	**8**	**8**	**8**
Storage E-MTTR (minutes) per SEMI E10	**25**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Transport MMBF	**8,000**	**11,000**	**15,000**	**25,000**	**35,000**	**35,000**	**35,000**	**45,000**	**45,000**
Storage MCBF	**25,000**	**35,000**	**45,000**	**55,000**	**60,000**	**60,000**	**60,000**	**70,000**	**70,000**
Peak system throughput (40K WSPM)									
Interbay transport (moves/hour)	**2250**	**2500**	**2575**	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**
Intrabay transport (moves/hour) — high throughput bay	**250**	**260**	**270**	**280**	**290**	**300**	**300**	**300**	**300**
Transport (moves/hour)—unified system	**4240**	**4740**	**4900**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
Stocker cycle time (seconds) (100 bin capacity)	**12**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Average delivery time (minutes)	**6**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Peak delivery time (minutes)	**12**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Hot lot average delivery time (minutes)	**3**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
AMHS lead time (weeks)	**12**	**<9**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**
AMHS install time (weeks)	**24**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Downtime to extend system capacity when previously planned (minutes)	**120**	**<30**	**<15**	**<15**	**<0**	**<0**	**<0**	**<0**	**<0**
Time required to integrate process tools to AMHS (minutes per LP)	**15**	**12**	**12**	**10**	**10**	**5**	**5**	**5**	**5**

Table 88b Material Handling Systems Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Transport E-MTTR (minutes) per SEMI E10	**8**	**7**	**7**	**7**	**6**	**6**	**6**
Storage E-MTTR (minutes) per SEMI E10	**20**	**15**	**15**	**15**	**10**	**10**	**10**
Transport MMBF	**45,000**	**55,000**	**55,000**	**55,000**	**65,000**	**65,000**	**65,000**
Storage MCBF	**70,000**	**80,000**	**80,000**	**80,000**	**100,000**	**100,000**	**100,000**
Peak system throughput (40K WSPM)							
Interbay transport (moves/hour)	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**	**2660**
Intrabay transport (moves/hour) — high throughput bay	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Transport (moves/hour)—unified system	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
Stocker cycle time (seconds) (100 bin capacity)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Average delivery time (minutes)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Peak delivery time (minutes)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Hot lot average delivery time (minutes)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
AMHS lead time (weeks)	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**	**<8**
AMHS install time (weeks)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Downtime to extend system capacity when previously planned (minutes)	**<0**	**<0**	**<0**	**<0**	**<0**	**<0**	**<0**
Time required to integrate process tools to AMHS (minutes per LP)	**5**	**5**	**5**	**5**	**5**	**5**	**5**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Explanation of Items for Material Handling Systems Requirements

Item	*Explanation*
Transport E-MTTR (min per SEMI E10)	*Mean time to repair equipment-related failures (AMHS Transport); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.* *Notes: Refers to unscheduled, supplier dependent failures. Includes interbay and intrabay transport systems. Offline repair of components is not included in this time. Includes embedded software control systems (transport controllers). Does not include storage AMHS equipment or errors induced by the storage equipment. Does not include load port, FOUP carrier, or MES level software issues. Does not include reticle system.*
Storage E-MTTR (min per SEMI E10)	*Mean time to repair equipment-related failures (AMHS Storage); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.* *Notes: Refers to unscheduled, supplier dependent failures. Includes storage equipment load ports and embedded software. Does not include interbay or intrabay transport or incidents induced by these errors. Does not include FOUP carrier or MES level software issues. Does not include reticle system.*
Transport MMBF (mean move between failure)	*Average number cycles (delivery from pt A-pt.B) made by AMHS interbay or intrabay transport equipment before a person has to intervene to fix a failure. Number of transport moves / Number of supplier dependent unscheduled failures. Reference transport MPH definition for details on move.*
Storage MCBF (mean cycle between failure)	*Average number cycles (delivery from point A to point B) made by AMHS storage equipment before a person has to intervene to fix a failure. Number of storage cycles / Number of supplier dependent unscheduled failures per quarter. Reference cycle time definition for details on stocker cycle.*
Interbay transport (moves/hour)	*Number of material handling moves per hour performed by the interbay transport system. An interbay transport move is defined as a carrier move from the loading of an interbay system at a stocker interbay port to the unloading of the same Load at the destination stocker. Moves are counted by the Host (MCS).*
Intrabay transport (moves/hour)	*Number of material handling moves per hour performed by an intrabay transport loop. An intrabay transport move is defined as a carrier move between loadports (between stocker ports and production equipment load port, between two production equipment load ports). Moves are counted by the Host (MCS).*
Tool-to-Tool Direct transport (moves/hour) – Unified system	*A transport move is defined as a transfer of a carrier between any two loadports (stocker, process tool or transfer point between transport systems). Note that stocker robot moves from/to load ports are not assumed concurrent with nor included in system throughput moves. Moves are counted by the Host (MCS).*
Stocker cycle time (seconds) (100 bin capacity)	*Stocker cycle time is defined as the time (in seconds) from when the Host(MCS) issues the move command to the time the stocker signals completion with the move complete command to the host. The physical motion is the stocker internal robot moving to a carrier at a port or storage bin, picking up the carrier, and delivering it to another port or storage bin within the same stocker. Stocker cycle time shall be determined as the average of several different types of moves over a period of time. The moves should include all ports and all shelf locations. Each move needs to alternate between different carriers. The maximum MCS communication time is assumed to be 1 second.*
Average delivery time (minutes)	*The time begins at the request for carrier movement from the MES and ends when the carrier arrives at the load port of the receiving equipment.*
Peak delivery time (minutes)	*Peak delivery time is considered the peak performance capability defined as the average delivery time plus two standard deviations.*
Hot lot average delivery time (min)	*Reference definition for Average Delivery Time. Reference Factory Operations section for further details on hot lots.*
AMHS lead time (weeks)	*Time elapsed, in weeks, between when a purchase order has been placed for a material handling system until the time the first shipment is FOB at supplier's dock. This assumes that at the time of PO placement the equipment configuration is fixed. This lead time should not be affected by market demand on supplier.*
AMHS install time (weeks)	*Time elapsed, in weeks, between when the first component of the system is moved in from the dock until the final component is fully installed, started up, and tested to meet full designed throughput capability. Assume new factory and uninterrupted installation of the material handling system (assume no facility, MCS or tool delays). Based on 20K WSPM fab of approximately 200 meters by 80 meters, with 15–20 short bays. Does not include reticle systems.*
Downtime to extend system capacity when previously planned (minutes)	*Impact to material handling system in terms of downtime, in minutes, of the material handling system, required for making connections to system track extensions or a new storage when previsions for this expansion were incorporated in the original design.*
Time required to integrate process tools to AMHS (minutes per LP)	*The Downtime to the transport system when a process tool is integrated to the AMHS. Addition of tool occurs on a track with existing vehicle traffic (no bypass units around tools). Assume tool is placed correctly and physical tool move in does not impact the AMHS. System not stopped for PIO install (tool side). Time includes: Hardware install on track, teaching LP, Software updates, Delivery Testing. Scope ends when all vehicles have capability to deliver to new LP.*

FACTORY INFORMATION AND CONTROL SYSTEMS

The scope of Factory Information and Control Systems (FICS) includes computer hardware and software, manufacturing execution and decision support systems, factory scheduling, control of equipment and material handling systems, and process control. FICS applications are essential to enabling potential solutions that meet Technology Requirements in several functional areas, including Factory Operations, Production Equipment, and Material Handling System solutions.

Production Equipment and Factory Operations place a strong reliance on FICS applications to drive equipment performance improvements. FICS applications must accurately track equipment availability, utilization, and run rate. Drill-down reporting capabilities will enable the factory to quickly identify performance losses and improvement opportunities. Active monitoring of equipment health is required to improve Mean Time Between Failure (MTBF) and Mean Time To Repair (MTTR) on bottleneck equipment. The application of Equipment Engineering Systems E-diagnostic and E-manufacturing capabilities will allow increased data collection and analysis, monitoring of equipment health, remote diagnostic capabilities, prediction of future failures and equipment reliability improvement by equipment suppliers to minimize unscheduled repairs and equipment downtime, improving MTTR and MTBF.

Factories must eliminate Production Equipment idle time when material is available for processing. FICS applications must support integration of the Manufacturing Execution System (MES), with the Equipment Tracking, with the factory scheduler/dispatcher and the Automated Material Handling System (AMHS). Integration of these different systems is required to determine what material should be processed next at a piece of equipment in order to ensure timely material delivery that will minimize equipment idle time. Information from equipment, such as processing status, load port availability, PM scheduling, and expected completion time, will need to be collected and compared to dynamic dispatch lists that indicate what material is to be processed next. This must be evaluated against estimated transit times based on current material location, as well as AMHS work queues so that decisions on when to dispatch the next set of material to equipment can be accurately determined. Further integration with yield management systems will enable optimized routing of material to tools that produce maximum yield. Integration with e-diagnostics and PM systems will enable predictive maintenance based on equipment usage trends. Intelligent analysis by factory systems will allow automated decision-making on whether a PM can be completed sooner than scheduled, or pushed to a future time, by predicting the downstream impact to both the equipment health and the factory output.

Cycle time reduction requirements from Factory Operations, specifically for priority lots, drive additional AMHS potential solutions, including integrated delivery, and direct transport of material to tools without return to a stocker. This shift in manufacturing methodology will require detailed knowledge of lot priority and chamber-level equipment status to be integrated with the scheduler, dispatcher, and material handling system to ensure that priority lots spend minimum time awaiting AMHS or Production tool availability. Future factory systems must support zero-footprint AMHS conveyer-based storage systems, including the ability to dynamically know current material location, and ensure the material is optimally routed to the correct production equipment.

Yield improvements also rely heavily on FICS solutions. FICS Potential solutions will provide data acquisition and interact with advanced process control systems to prevent process excursions, improve yield, reduce non-product runs, reduce cycle time due to rework, and reduce equipment calibration and maintenance. FICS solutions include an Equipment Engineering System (EES), which includes fault detection and classification (FDC), run-to-run control at both a lot and wafer level, and integrated metrology capabilities. Process Control solutions must be able to support the ability to run different process parameters for each wafer, both between and within process runs. They must support a robust method for exchanging data with other process control and factory system software. Increased reliance on process control systems requires these applications be reliable and scalable to support performance requirements. The concept of Engineering Chain strives for accurate, flexible, and rapid data exchange from design to final product to realize cost and cycle time reductions. A common data model for integrating the Engineering Chain partners including design, mask manufacturing, wafer manufacturing, and final manufacturing would facilitate accessibility to critical information needed for optimal manufacturing effectiveness. Driven by escalating mask costs and cycle times, Engineering Chain potential solutions will initially focus on mask operations. Aggressive Optical Proximity Correction (OPC), necessitated by shrinking wafer lithography process margins, has caused a data explosion and a concomitant increase in mask production cycle times, which has been aggravated by over constrained mask tolerances by reducing mask production yield. Time to send and load tape-out data, as well as time for OPC and data preparation, will increase significantly with each generation. FICS solutions are required to maintain a steady cycle time for these operations, starting in 2004, despite increased complexity in future generation designs. Optimizing OPC and mask tolerances while preserving wafer manufacturing yield requires timely exchange of accurate information about mask and wafer lithography process capabilities to the design engineers and for designers to effectively communicate context-sensitive mask tolerances to the mask manufacturer. The existing multitude of proprietary data formats, coupled with a linear data flow, obscure design

intent and downstream manufacturing capabilities. Data and feedback mechanisms essential to accurately characterize equipment and processes for refining production goals must be identified. The existing fractured data flow flattens the hierarchy in the original design data, contributing to the data explosion and decreasing mask writing tool speed, one of the two main mask cost drivers. Implementing mask data formats that support future design and lithography practices would streamline the data flow. Research is required on FICS potential solutions such as information models for effectively communicating requirements along the Engineering Chain in order to support design for manufacturability and more equitable sharing of error budgets. FICS solutions must also address security concerns as data become more accessible throughout the Engineering Chain.

Achieving these goals will require conformance to industry interface standards. Specific tool- and/or manufacturing-defined proprietary interfaces will not be acceptable. Open, standardized interfaces are required to avoid custom solutions, which increase implementation time with an added cost to both the IC manufacturer and the FICS supplier. New standards will be required to support agile manufacturing and process control initiatives. Time to develop these new standards must be decreased, through collaboration between IC makers and FICS suppliers. Lead time for FICS conformance to standards will need to decrease through parallel development of standardized FICS with development of new standards, to ensure that standards-based FICS applications are available to meet factory requirements. ITRS factory and university groups will need to conduct research to determine time to develop and integrate factory-wide applications and control systems applications, and identify additional opportunities for improvement. Ultimately, the improved time-to-market for standards-compliant applications will reduce time and cost of integration, allowing IC makers and suppliers to focus on improved capabilities rather than customized integration, and decreasing the risk introduced with integrating new applications into an existing factory.

Software flexibility and extendibility is required to permit very high levels of reuse when processes and technologies are upgraded in the factory. When semiconductor manufacturers develop new technologies, processes, or products, or bring up new tools or factories, it is desirable to reuse factory information and control systems. Note that the reusability targets are not intended to inhibit new suppliers, nor the adoption of new ideas, systems, or technologies. Rather, the targets are intended to insure modularity and extendibility of software systems from one technology generation to the next, in order to reduce the risk and additional cost resulting from the introduction of new applications.

The difficult challenge of increased complexity leads to an increase in the amount of data produced by production equipment and AMHS systems. Production equipment will be providing increased volumes of data: sensor data required for fault detection, advanced process control data, tool performance data, and wafer level information required for 300mm processing. Factory Information and Control Systems must be scalable to manage the collection and storage/retrieval of this increase in data collection. Additionally, FICS must support the ability to filter through the magnitude of data, to identify the specific set of information required to make decisions for factory operation and business-level decisions. Integration of FICS applications with business-level software systems provides accurate factory floor data for supply management, and improved product tracking. Potential solutions will require the standardization of technologies (e.g. XML) that enable this level of integration.

Cyber infections such as viruses, worms and denial of services have made security a key focus area with the potential of disrupting factory operations due to downtime and reduced manufacturing productivity. Cyber security guidelines for IC Makers and OEMs have been published by ISMI in March 2005. These guidelines should be followed to prevent threat of factory downtime. While the cyber security provides a tactical relief to the operations environment, semiconductor equipment continue to pose significant security challenges in the integration with the IC Maker environment. The top issues include intellectual property (IP) preservation, system integrity and integration with IC Maker directory services. Potential solutions such as re-organization of the equipment software sub-systems to include role-based security, increased robustness in design and integration into industry standards such as LDAP (Lightweight Directory Access Protocol) and possibly new SEMI standards and guidelines. Please see the references attached:

- *Equipment Security Guidelines www.sematech.org/docubase/abstracts/4567beng.htm*
- *Equipment Security Additional Capabilities Proposal Documents*

As shown in Table 89, increased reliance on factory information and control systems places greater emphasis on system availability. Increased factory complexity leads to increased integration of factory information and control systems. Because of this, there will be added attention to decreasing the occurrence of full fab downtime incidents caused by a failure of a single application. Furthermore, scheduled downtime to install or upgrade mission critical systems and databases must have minimal impact on the factory operations. Potential solutions include software applications and databases that are capable of dynamic upgrades, software applications that can monitor health of factory systems and that can induce load-balancing, and fault tolerant computer systems with transparent hardware switching for failovers.

Table 89a Factory Information and Control Systems Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*
Availability of mission critical applications (% per year)	**99.98**	**99.986**	**99.987**	**99.99**	**99.991**	**99.991**	**99.994**	**99.994**	**99.994**
Downtime of mission critical applications (minutes per year)	**105 min**	**75 min**	**75 min**	**68 min**	**53 min**	**45 min**	**30 min**	**30 min**	**30 min**
Full factory down due to unscheduled FICS downtime (minutes per year)	**120 min**	**60 min**	**60 min**	**60 min**	**<15 min**	**< 15 min**	**<15 min**	**<15 min**	**<15 min**
Full factory down due to scheduled FICS downtime (minutes per year)	**180 min**	**180 min**	**180 min**	**120 min**	**120 min**	**120 min**	**60 min**	**60 min**	**60 min**
Mean time to recover for mission critical applications (minutes down per year)	**30**	**15**	**<15**	**<15**	**<15**	**<15**	**<15**	**<15**	**<15**
MCS design to support peak number of AMHS transport moves (moves/hr)	**12.7**	**14.2**	**14.7**	**15K**	**15K**	**15K**	**12.3K**	**12.3K**	**12.7**
FICS design to support peak number of AMHS direct transport moves (moves/hr)	**1270**	**1420**	**1470**	**1500**	**1500**	**1500**	**N/A**	**N/A**	**1270**
Time to send and load tape-out data into mask shop data system (hours)	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**
Time for OPC calculations and data preparation for mask writer (days)	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**
Time for OPC calculations only (days)	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
% Factory information and control systems reusable for next generation	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**
Wafer-level recipe/parameter adjustment	**Partial**	**Partial**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Within-wafer recipe/parameter adjustment	**Partial**	**Partial**	**Partial**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

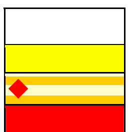
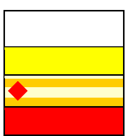


Table 89b Factory Information and Control Systems Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Availability of mission critical applications (% per year)	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**	**99.999**
Downtime of mission critical applications (minutes per year)	**8 min**	**8 min**	**8 min**	**4 min**	**4 min**	**4 min**	**4 min**
Full factory down due to unscheduled FICS downtime (minutes per year)	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**	**<15 min**
Full factory down due to scheduled FICS downtime (minutes per year)	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**	**0 min**
Mean time to recover for mission critical applications (minutes down per year)	**5**	**5**	**5**	**2**	**2**	**2**	**2**
MCS design to support peak number of AMHS transport moves (moves/hr)	**14.2**	**14.2**	**14.7**	**15K**	**15K**	**15K**	**15K**
FICS design to support peak number of AMHS direct transport moves (moves/hr)	**1420**	**1420**	**1470**	**1500**	**1500**	**1500**	**1500**
Time to send and load tape-out data into mask shop data system (hours)	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**	**6–12**
Time for OPC calculations and data preparation for mask writer (days)	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**	**4–8**
Time for OPC calculations only (days)	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
% Factory information and control systems reusable for next generation	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**	**>93%**
Wafer-level recipe/parameter adjustment	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Within-wafer recipe/parameter adjustment	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Explanation of Items for Factory Information and Control Systems Requirements

Item	*Explanation*
Availability of mission critical application (% per year) *Downtime of mission critical application (minutes per year)*	*Availability (A) is 100% minus (scheduled downtime % + unscheduled downtime %). Scheduled downtime and unscheduled downtimes are defined in SEMI E10.*
Full Factory Down Incidents (per year)	*Number of full factory downtime incident per year for mission critical system due to downtime of mission critical applications. Mission critical applications are those that are required to keep the entire wafer factory operational. Depending on factory configuration, these include: MES, Scheduler / Dispatcher, MCS, Cell Controller, SPC, Reticle system, Facilities Control Systems.*
Mean Time to Recover for mission critical applications (minutes)	*Mean time to recover a mission critical application following an unscheduled downtime. Mission critical applications within the factory information and control systems are those that are required to keep the entire wafer factory operational. Mean time to recover is measured in minutes per incident.*
Availability of the total factory system (% per year) *Factory down due to unscheduled FICS (minutes per year)* *Factory down due to scheduled FICS downtime (minutes per year)*	*Availability (Ai) is 100% minus (scheduled downtime % + unscheduled downtime %) for each mission critical factory information and control system applications. Scheduled downtime and unscheduled downtimes are defined in SEMI E10. The total availability of the factory = [A1 * A2 * A3 * A4]. The metric values assume that there are up to 4 mission critical applications within a factory.*
Peak number of AMHS transport moves supported by material control system (moves/hr)	*Maximum number of transport moves per hour supported by Material Control System (MCS). Able to support: peak # of moves for unified transport system * 1.5 (to translate to separate interbay/intrabay system) * 2 (safety factor for FICS)*
Peak number of Direct Transport moves (moves/hr)	*Target number of Direct Transport moves per hour supported by FICS. Direct Transport moves are defined as carrier moves directly from one production equipment tool load port to another production equipment tool load port. Assume 10% of peak number of transport moves will require Direct Transport*
Time to send and load tape-out data into Mask Shop data system	*Time in hours to send data from mask designer to mask shop's OPC application.*
Time for OPC calculations and data preparation for mask writer (days) *OPC Time only (days)*	*Time in hours to perform OPC calculations + Time in hours to convert the output of the OPC engine to the format the mask writer understands + Time in hours to transmit the data into the mask writing system* *Time for OPC calculations only is the time in hours to perform the OPC calculations once the OPC application has received the tape-out data from the mask designer*
% Factory information and control systems reusable for next generation	*Percentage of factory information and control systems (both computer hardware and software) that is reused from process technology generation to process technology generation, measured in cost.*
Ability to adjust recipes/parameters within a run	*Ability for Factory Information and Control systems to run a different recipe and/or parameters for each wafer within a carrier. This facilitates the ability to have multiple lots per carrier. Base requirements also include the ability to track, monitor, and control the wafer at each point the factory or within the equipment.*

FACILITIES

Facilities include the overall physical buildings, cleanroom, and facility infrastructure systems, up to and surrounding the production equipment, directly associated with semiconductor manufacturing operations (does not include adjacent general office spaces and corporate functional areas are not included). Production equipment requirements, manufacturing goals, management philosophies, environmental, safety, and health (ESH) requirements, building codes and standards, defect-reduction targets and wafer cost reduction targets will affect the facility and supporting facility infrastructure systems requirements, complexity, and costs.

The industry continues to demand facilities that are increasingly flexible, extendable, and reliable, come on-line more quickly, and more cost effective; however, production equipment requirements, ESH compliance and factory operational flexibility are continuing to drive increased facility capital and operating costs. Factory size is continuing to increase with more complex, larger, and heavier production and support equipment. New and different process steps are increasing the cleanroom size faster than factory production output increases. Consequently, the increasing size and complexity of the factory, the production equipment and material handling systems, as well as the pressure to reduce time to market and facility costs will make maintaining many of the current technical requirements a challenge (as described in Table 90a and b). Better coordination between production equipment operation, maintenance, and environmental requirements and facility infrastructure system design and installed capabilities is necessary to achieve these goals, improve system utilization, and control facility capital and operating costs.

Facility complexity and costs are also rising due to impacts from many other areas including the greater variety in gases/chemicals, more stringent ESH regulations, and more stringent electrostatic discharge (ESD) and electromagnetic interference (EMI) controls. Accommodating all these complexity drivers will require early collaboration with production

equipment manufacturers to provide innovative and cost effective solutions for maintenance, abatement, and reclaim/recycle. Meeting production equipment requirements (vibration, purity) at point-of-use may be a more cost-effective approach to meeting future requirements without increasing facility costs or sacrificing flexibility. For example, reducing facility vibration requirements and then working with production equipment manufacturers to ensure proper vibration control at the tool will control facility vibration at the tool and reduce facility costs without decreasing the facility's flexibility. Reduction of gas and chemical purity and piping installation specifications on central supply systems and concentrating ultra purity requirements to the specific equipment or areas required can also help control costs, improve flexibility and enhance operating reliability. The rise of airborne molecular contamination (AMC) and electromagnetic interference (EMI) will require revisiting contamination control procedures with new methods and materials, which could also affect facility components used during construction. Facility operations will also require coordination with production equipment vendors to ensure proper AMC and EMI control.

Production equipment installation costs and time continue to be driven higher by more gas, chemical and utility connections and ESH compliance requirements and the lack of installation consistency, constantly changing design requirements, and inaccurate documentation. Earlier awareness of new production equipment designs and standardizing production equipment connections and materials of construction would allow for a basebuild construction "design for facilities" emphasis.

The demand to reduce time from groundbreaking to first full loop wafer out while increasing production equipment complexity and operational flexibility and the variation in global codes, standards, and regulations will require a paradigm shift. This shift entails complete integration of the IC manufacturer, the factory designers/builders and the production equipment vendors into the entire project team. As a minimum, the project team must be assembled early and include process engineers, manufacturing engineers, facility engineers, design consultants, construction contractors, vendor/suppliers and process equipment manufacturers. Development of techniques such as standardized design concepts, generic fab models, and off-site fabrication will be required to relieve construction congestion and reduce construction time and to control facility costs to meet desired goals. Challenging the wafer cycle life requirements to coordinate with the facility infrastructure capability will also help control capital cost and reduce facility time to market.

Factory operating costs are continuing to be driven by higher facility depreciation, higher utility consumption, and higher labor costs. Reduced exhaust/makeup air requirements and higher voltage power for production equipment will result in lower operating costs as well as construction costs. Relaxed cleanroom cleanliness requirements through the use of mini-environments and isolation technology (SMIF, FOUPs) will also reduce operating costs as well as initial capital costs; however, cleanroom airborne particle cleanliness requirements has led to a reduction in airflow causing temperature, humidity, cleanliness, and backside maintenance concerns. As the cleanroom cleanliness is relaxed, these concerns must be address through the production equipment. For example, as the general fab cleanliness reaches ISO Class 6, the production equipment maintenance needs must be built into the equipment or through the use of a portable VFH hood to provide localized clean air.

Although reliability of facility infrastructure systems is currently sufficient to support manufacturing, much of this reliability has been achieved through costly redundancy. Improvement is still needed in the design and operation of individual electrical, mechanical and control components and systems to reduce manufacturing interruptions. Collaboration with facility equipment manufacturers may modify the N+1 philosophy for redundancy and positively affect costs without sacrifice to reliability.

Finally, any significant change in the production equipment set (such as new chemistries or wafer environment requirements), either for post CMOS or beyond 300 mm, will have an impact on the factory requirements, schedules, and costs which cannot be reliably predicted from current 300 mm technology. (Refer to the Facilities Potential Solutions figure.)

For more information and details on *Facilities Technology Requirements and Potential Solutions*, access the electronic chapter links for Factory Integration online..

Table 90a Facilities Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*	*450*	*450*
Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM) (low mix only)	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**	**0.34**
SubFab to Fab ratio	**1**	**1**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**	**0.75**
Facility service life (in three-year generations)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Facility cleanliness level (ISO 14644) [1]	**Class 6 at rest**	**Class 6 at rest**	**Class 6 at rest**	**Class 6 at rest**	**Class 6 at rest**	**Class 6 at rest**	**Class 6 at rest**	**Class 7 at rest**	**Class 7 at rest**
Facility cleanliness level (Airborne molecular contamination AMC) – ppt M	*Discussed in Yield Enhancement Tables*								
Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [2]	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**	**6.25 (VC D)**
Facility non-critical vibration areas (micrometers per second) [2]	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**	**50 (VC A)**
Maximum allowable electrostatic field on facility surfaces (V/cm)	**90**	**80**	**70**	**63**	**55**	**50**	**44**	**38**	**35**
Gas, water, chemical purity	*Discussed in Yield Enhancement Chapter*								
Factory construction time from groundbreaking to first tool move-in (months)	**10**	**9**	**9**	**9**	**8**	**8**	**9**	**9**	**9**
Production equipment install and qualification cost as a % of capital cost	**8%**	**8%**	**7%**	**7%**	**6%**	**6%**	**5%**	**8%**	**8%**
Facility operating cost (including utilities) as a % of total operating cost	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**	**13%**
Utility cost per total factory operating cost (%)	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Power, water, and chemical consumption	*Discussed in ESH Chapter*								

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

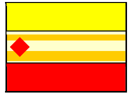


Table 90b Facilities Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Wafer Diameter (mm)	*450*	*450*	*450*	*450*	*450*	*450*	*450*
Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM) (low mix only)	0.34	0.34	0.34	0.34	0.34	0.34	0.34
SubFab to Fab ratio	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Facility service life (in three-year generations)	3	3	3	3	3	3	3
Facility cleanliness level (ISO 14644) [1]	Class 7 at rest	Class 7 at rest	Class 7 at rest	Class 7 at rest	Class 7 at rest	Class 8 at rest	Class 8 at rest
Facility cleanliness level (Airborne molecular contamination AMC) – ppt M	*Discussed in Yield Enhancement Tables*						
Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [2]	6.25 (VC D)	6.25 (VC D)	6.25 (VC D)	6.25 (VC D)	6.25 (VC D)	6.25 (VC D)	6.25 (VC D)
Facility non-critical vibration areas (micrometers per second) [2]	50 (VC A)	50 (VC A)	50 (VC A)	50 (VC A)	50 (VC A)	50 (VC A)	50 (VC A)
Maximum allowable electrostatic field on facility surfaces (V/cm)	31	28	25	22	20	18	15
Gas, water, chemical purity	*Discussed in Yield Enhancement Chapter*						
Factory construction time from groundbreaking to first tool move-in (months)	9	9	8	8	8	8	8
Production equipment install and qualification cost as a % of capital cost	8%	7%	7%	6%	6%	5%	5%
Facility operating cost (including utilities) as a % of total operating cost	13%	13%	13%	13%	13%	13%	13%
Utility cost per total factory operating cost (%)	3%	3%	3%	3%	3%	3%	3%
Power, water, and chemical consumption	*Discussed in ESH Chapter*						

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Explanation of Items for Facilities requirements:

Item	*Explanation*
Manufacturing (cleanroom) area/wafer starts per month (m^2/WSPM)	*"Manufacturing (cleanroom) area" is defined as the space in square meters containing the process and metrology equipment used for direct manufacturing processes such as photolithograph, diffusion, etch, thin films, CMP, excluding subFab spaces containing support equipment and facility infrastructure systems.*
Wafer starts per month (WSPM)	*Wafer starts per month is defined as the number of new 300mm wafers introduced into production for processing during a given 30 day period*
Sub-Fab to Fab ratio	*"Sub-Fab to Fab ratio" is defined as the footprint of the production equipment support plan area to the manufacturing area above. Relates to and extends factory operations "floor space effectiveness."*
Facility service life (in three-year generations)	*Facility service (system) life is the number of generations (process changes) that the system is available before major renovation is required to meet process requirements.*
Facility cleanliness class (ISO 14644)	*Cleanliness classification of wafer factory manufacturing (cleanroom) area as defined by ISO 14644-1.*
Facility critical vibration areas (litho, metro, other) (micrometers per second)	*"Vibration critical" is defined as area of the primary manufacturing floor in which a significant portion of the equipment is highly sensitive to floor vibration, the mitigation was not provided at the tool itself, and excessive vibrations can have serious deleterious effects on product. Extensive measures may be required in the facility's structural and mechanical equipment design based upon the needs of this space category. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-DTE012.1[6] for definition of amplitudes, measurement methods, and signal processing requirements*
Facility non-critical vibration areas (micrometers per second)	*"Vibration non-critical" is defined as area of the primary manufacturing floor in which all or some of the equipment is only moderately vibration sensitive, and the structural system performance can be reduced. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-DTE012.1 for definition of amplitudes, measurement methods, and signal processing requirements.*
Maximum allowable electrostatic field on facility surfaces (V/cm)	*Facility surface electric field limits apply to all factory materials-construction materials, furniture, people, equipment and carriers Refer to SEMI standards E129[7], E78[8] and E43[9] for measurement methods.*
Factory construction time from groundbreaking to first tool move-in (months)	*Factory construction time is defined as the period of time in months from first concrete placement to the time that the first tool is moved into the manufacturing area and is ready for hookup, i.e., building systems have passed inspection sufficient to begin the tool installation process.*
Production equipment install and qualification cost as a % of total capital cost	*"Production equipment installation cost" is defined as the cost of all labor and materials necessary to accept, move-in, and connects production equipment to the facility infrastructure systems to make the production equipment operational. This includes qualification, but excludes facility infrastructure systems and upgrades, and the cost of the production equipment.*
Total Capital Cost	*Total Capital Cost is defined as all labor and material costs necessary to complete a new semiconductor factory including production equipment and facility capital cost. This excludes costs for land.*
Facility operating cost (inc. utilities) as a % of total factory operating cost	*"Facility operating cost" is defined as all facility expenses directly related to supporting manufacturing including depreciation, utility, labor and maintenance costs.*
Utility cost per total factory operating cost (%)	*"Utility cost" is defined as the cost of power, water, gases, and chemicals required to support manufacturing, including the factory material and consumables.*
Total Factory Operating Cost	*Total Factory Operating cost is defined as the total annual operating expenses necessary for operating the factory including depreciation, materials, maintenance, and labor.*

POTENTIAL SOLUTIONS

The principal goals of factory integration are maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs. The difficult challenges of 1) Responding to Complex Business Requirements, 2) Achieving Growth Targets, 3) Managing Factory Complexity, 4) Meeting Factory and Equipment Reliability, Capability or Productivity Requirements, 5) Meeting the Flexibility, Extendibility, and Scalability Needs, 6) Meeting Process Requirements at 65nm and 45nm at Production Volumes, 7) Increasing Global Restrictions on Environmental Issues, 8) Post-conventional CMOS Manufacturing Uncertainty, and 9) Emerging Factory Paradigm and Next Wafer Size must be addressed to achieve these goals. Potential solutions are identified for Factory

[6] *IEST-RP-DTE012.1: Handbook for Dynamic Data Acquisition and Analysis.*
[7] *SEMI E129: Guide to Assess and Control Electrostatic Charge in A Semiconductor Manufacturing Facility.*
[8] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*
[9] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

Operations, Production Equipment, Material Handling Systems, Factory Information and Control Systems, and Facilities. Note that the bars containing wafer diameter data represent potential solutions that are wafer-size specific.

Potential solutions are shown as *Research required*, *Development underway*, and *Qualification/pre-production*. The purpose is to provide guidance to researchers, suppliers and IC makers on the timing required to successfully implementing solutions into factories. Several research efforts are being planned (Ex: FORCe) in order to address the technology requirements and to develop these potential solutions. For simplicity, these activities are serial in each table; however, they overlap each other in practice.

Factory Operations

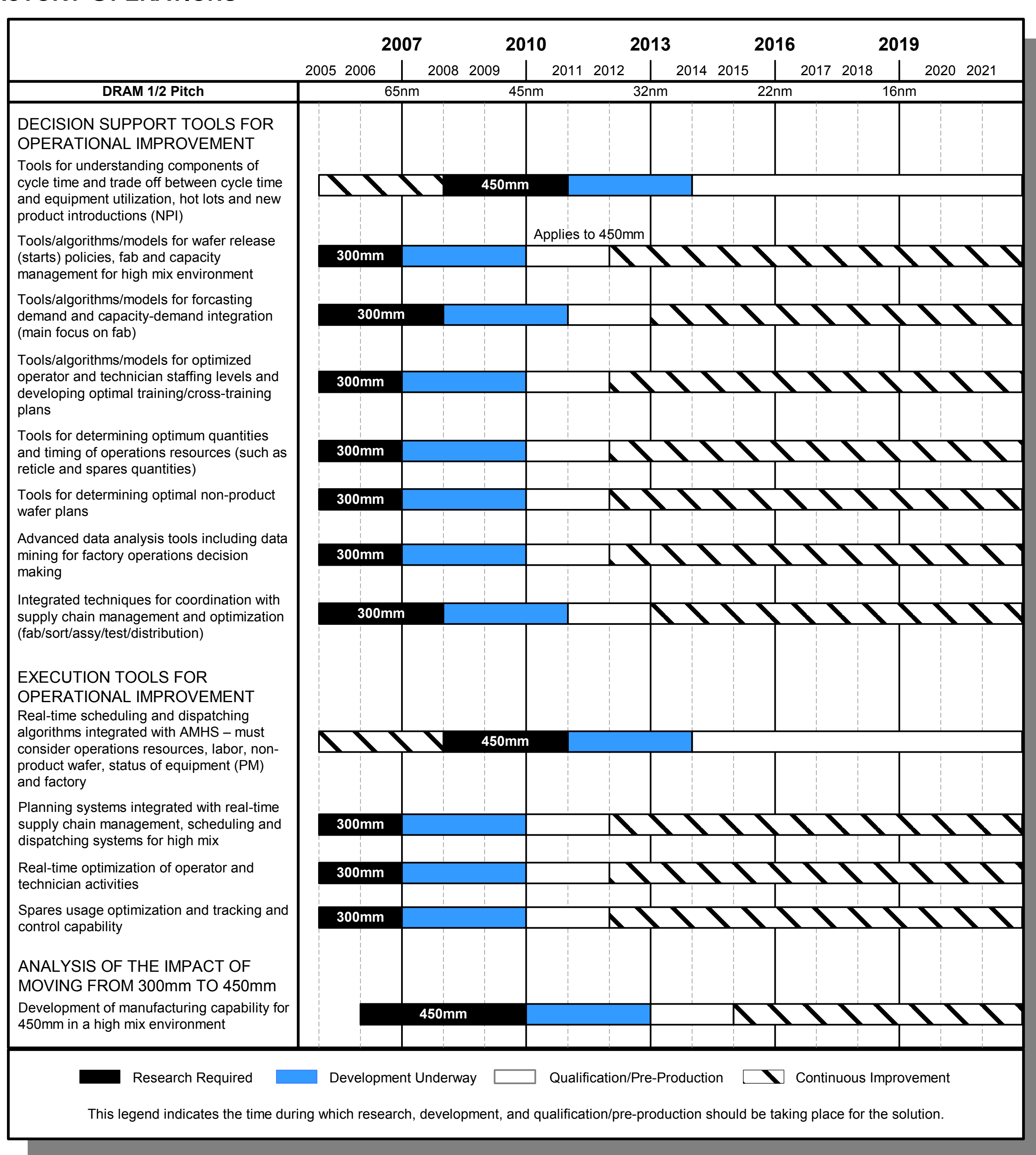


Figure 81 Factory Operations Potential Solutions

PRODUCTION EQUIPMENT

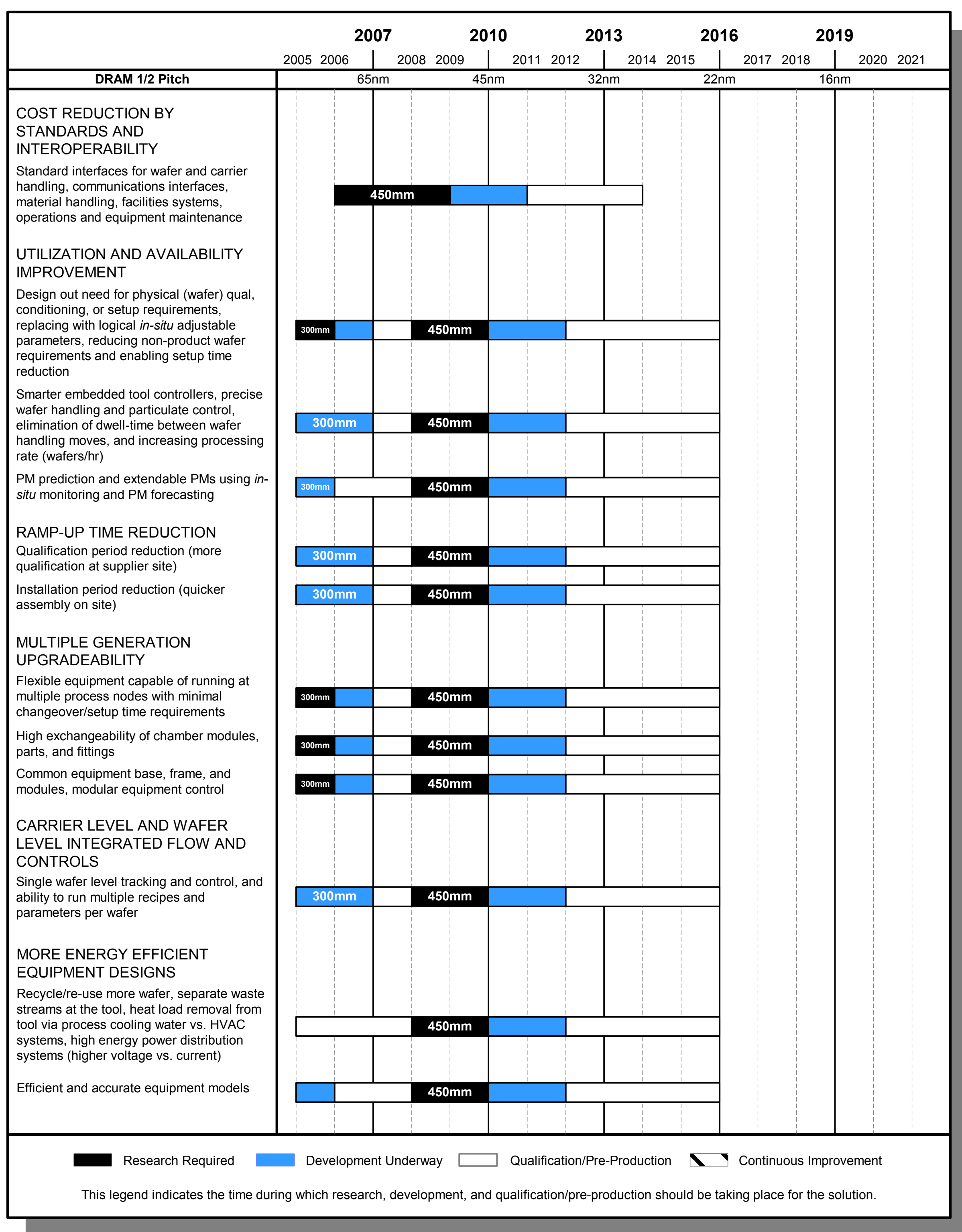


Figure 82 Production Equipment Potential Solutions

MATERIAL HANDLING SYSTEMS

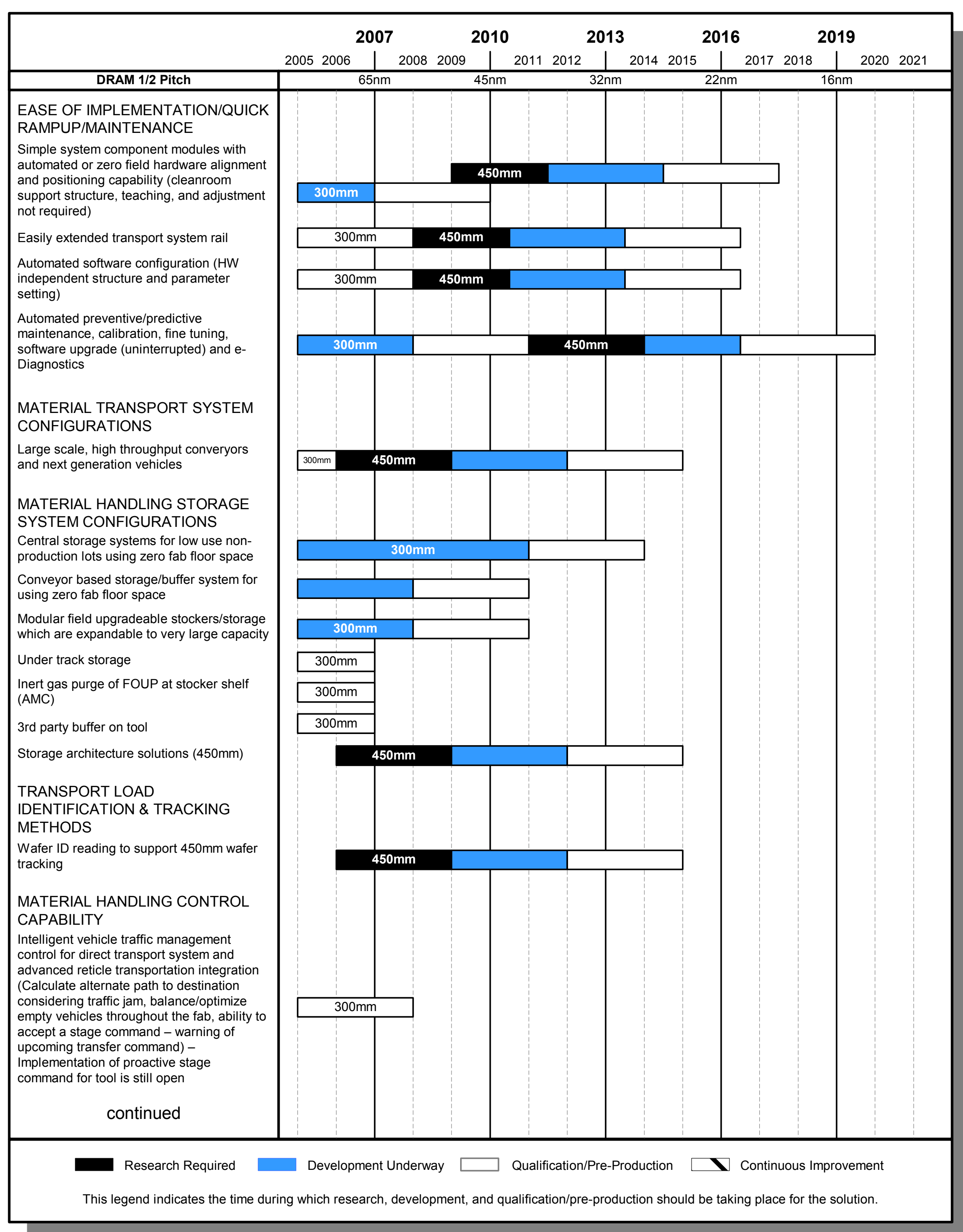


Figure 83 Material Handling Systems Potential Solutions

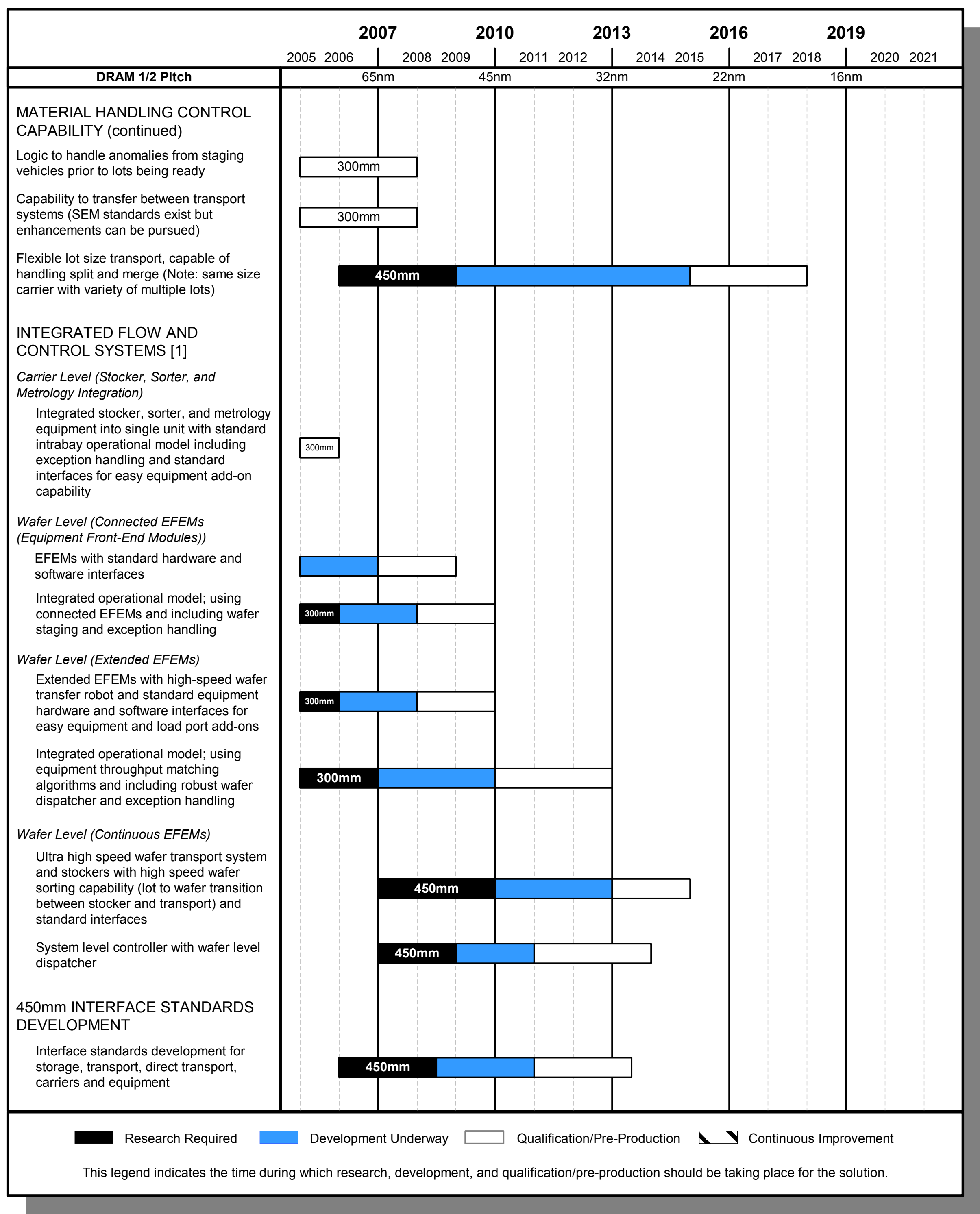


Figure 83 Material Handling Systems Potential Solutions (continued)

FACTORY INFORMATION AND CONTROL SYSTEMS

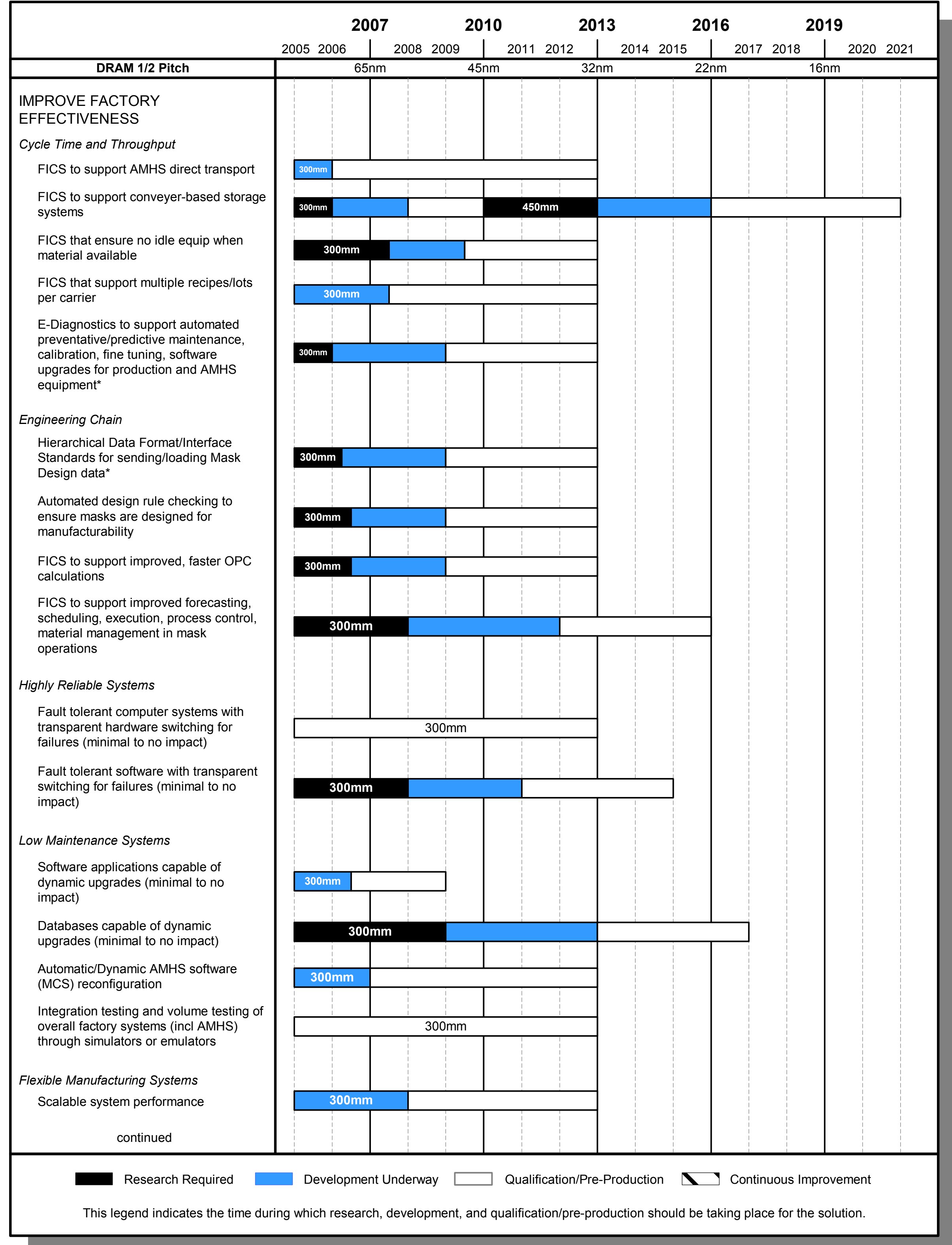


Figure 84 Factory Information and Control Systems Potential Solutions

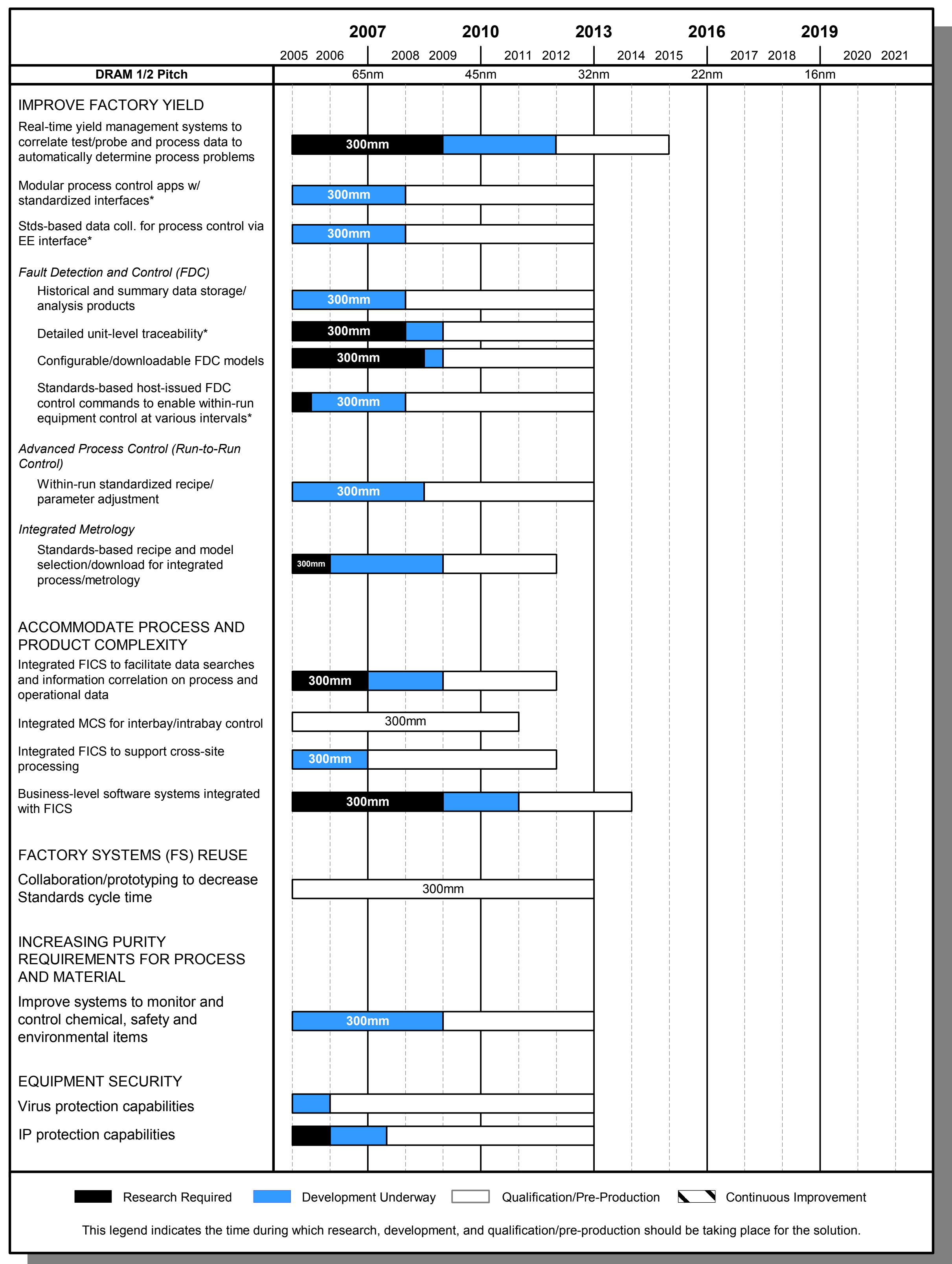


Figure 84 Factory Information and Control Systems Potential Solutions (continued)

FACILITIES

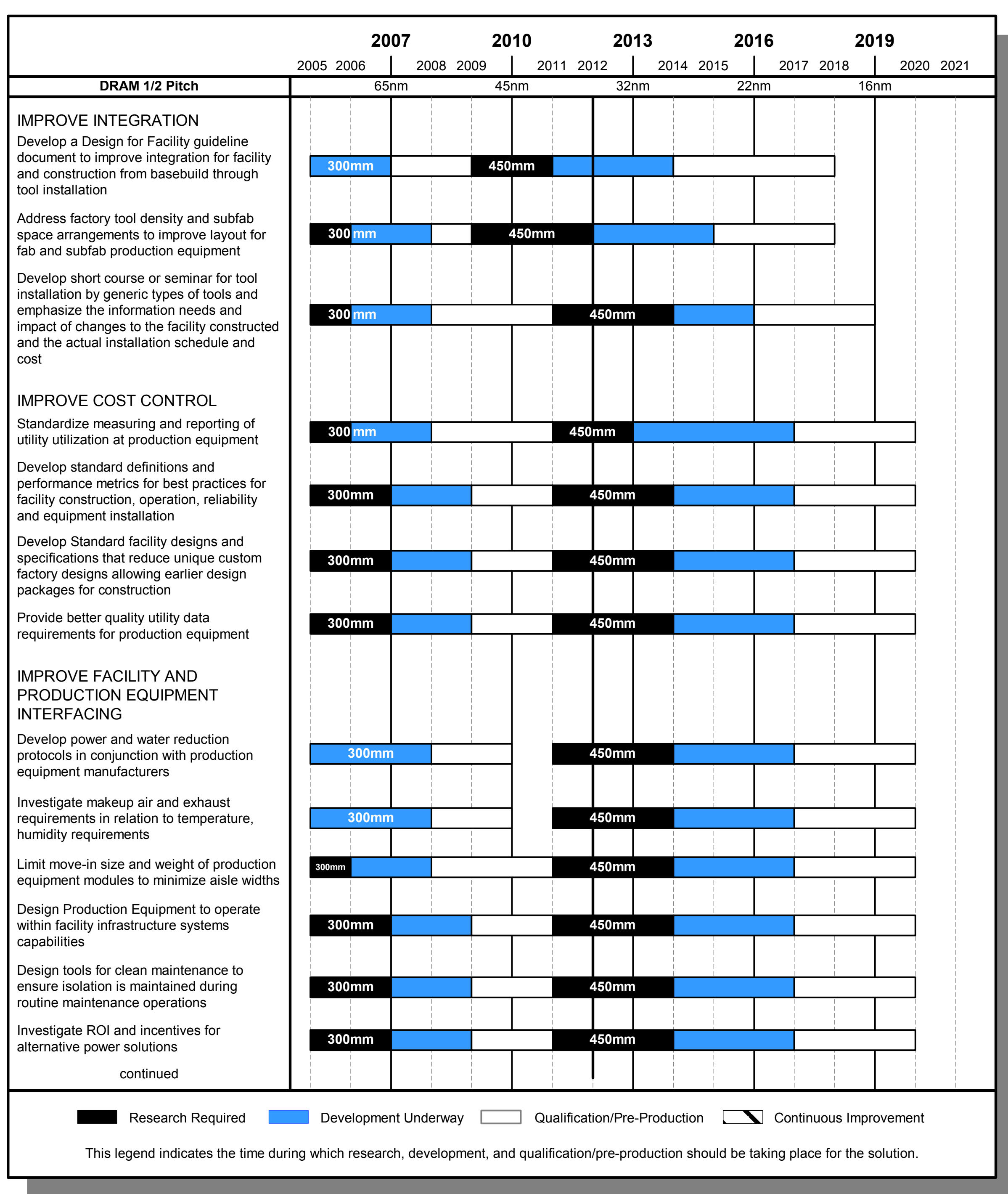


Figure 85 Facilities Potential Solutions

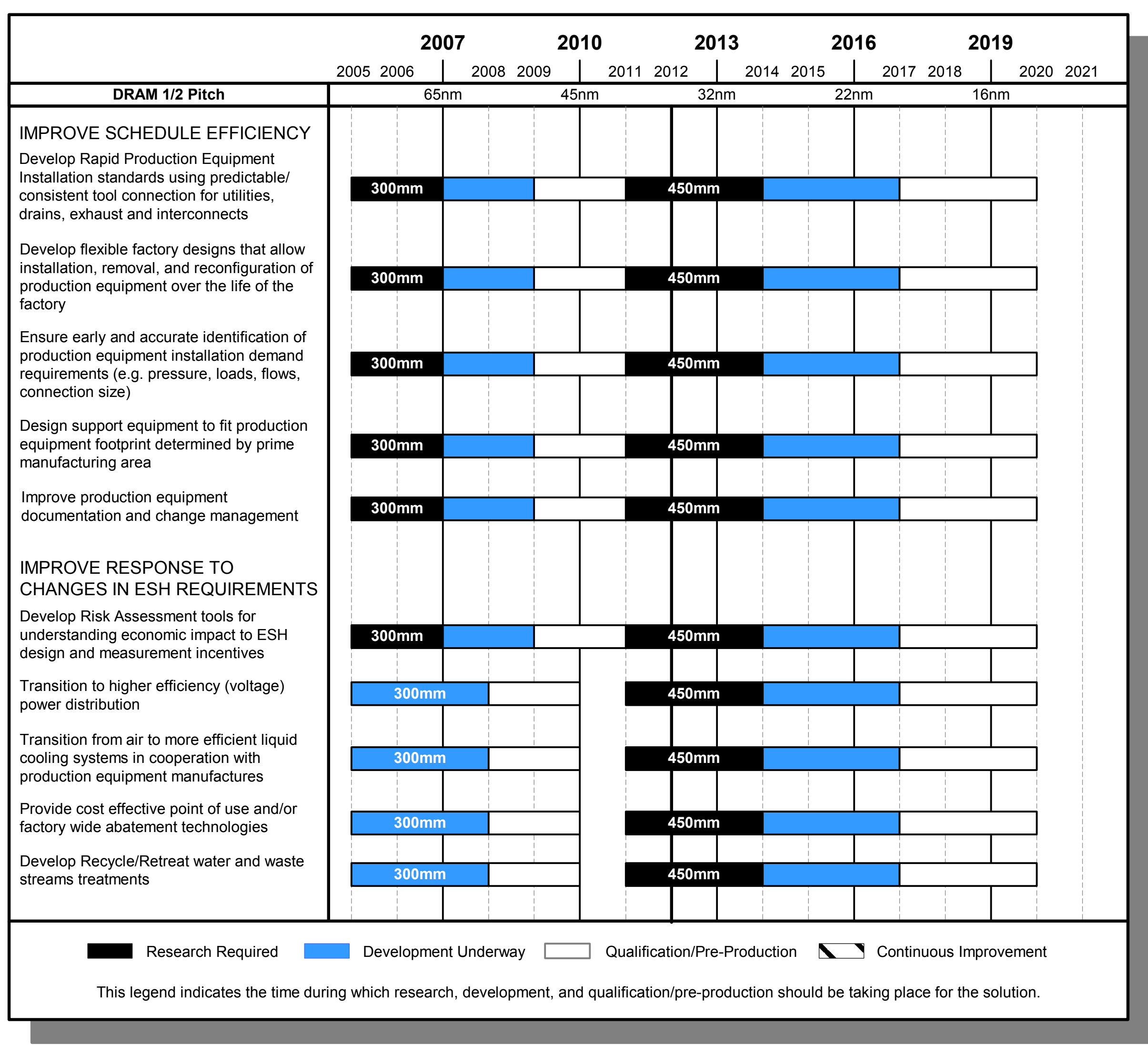


Figure 85 Facilities Potential Solutions (continued)

CROSSCUT ISSUES

Factory Integration technology requirements is often driven by the device, processing, yield, metrology, ESH, litho and other technology working group requirements. In order to fully understand the crosscut issues, Factory Integration interfaces with the other technology working groups and pulls together a list of key crosscut challenges and requirements. Table 91 below is the summary of key crosscut challenges and requirements generated in the year 2005 (Next Wafer Size challenges are listed separately).

Table 91 Crosscut Issues Relating to Factory Integration

Crosscut Area	*Factory integration related key challenges*
Interconnect	1.5 mm wafer edge exclusion may post challenges (need to justify additional die per wafer from 1.5mm); Overall increasing cost of abatement needs to be addressed. New materials impact.
Front end Process (FEP)	1.5 mm wafer edge exclusion is a challenge to starting material and SOI. FEP to communicate special facility AMC requirements.
Litho	Current focus on Immersion and EUVL (power, consumables); Fast reticle change; vibration specs; reticle storage issues; Need to coordinate YE inputs on water quality (temp and pH); AMC relative to the Reticle (reticle storage and in the litho equipment).
ESH	Ergonomics, Tool design, Chemical consumption concerns; AMC and particulate levels to be maintained; Regulations; ESH chemical abatement analysis needed. As per ESH, the trend is point of use versus central. Global warming ◊ Factories and Power suppliers will be asked to limit CO_2 emissions soon.
Metrology	Need for Integrated Metrology continues? Data standards; AMC relative to the Reticle (reticle storage and in the litho equipment).
Yield Enhancement	YE to maintain AMC technical requirements; traceability issues? No wafer coordinate standards exist today. Not having a data standard is inconvenience only. Need Design to Test coordinate system
Assembly & Packaging	Wafer level packaging issues (will be addressed by A&P and they will let FI know if there is any specific FI needs); Chip level (Dice) traceability.

INTERCONNECT

The *Interconnect chapter* described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. For the year 2005, Interconnect is working with Factory Integration (FI) on wafer edge exclusion, airborne molecular contamination (AMC) and next wafer size (450 mm). Another challenge faced by Interconnect that impacts Factory Integration is the introduction of new materials.

FRONT END PROCESSING (FEP)

The *Front End Processes* (FEP) Roadmap focuses on future process requirements and potential solutions related to scaled field effect transistors (MOSFETs), DRAM storage capacitors, as well as Flash and ferroelectric RAM (FeRAM) devices. The key issues FEP is working with FI are wafer edge exclusion, next wafer size (450 mm). Other crosscut issues are: 1.5 mm wafer edge exclusion is a challenge to starting material and SOI. FEP to communicate special facility AMC requirements.

LITHOGRAPHY

The *Lithography chapter* deals with the difficulties inherent in extending optical methods of patterning to physical limits, and also evaluates the need to develop entirely new, post-optical lithographic technologies capable of being implemented into manufacturing. Key challenges that need to be addressed by FI are to ensure the infrastructure (power, water) readiness for EUVL and to improve Advanced Process Control (APC) for Litho equipment. Other issues to be addressed are vibration needs and AMC impact on reticle.

ENVIRONMENTAL, SAFETY AND HEALTH (ESH)

ESH continues to play a very important role in factory design and operation. Decisions made at the earliest stages of factory planning will have a dramatic impact on the ability of that factory to economically meet rigorous safety and environmental requirements. Early consideration of safe and environmentally responsible design is essential to develop factories that comply with ESH requirements while achieving rapid start-up schedules and avoiding costly redesigns and retrofits.

Equipment suppliers have made good progress integrating point of use abatement devices and the tool. However, tool footprint in the sub-Fab has increased significantly as a result. An immediate challenge therefore is to find an efficient tool design that incorporates point of use devices without an overall increase in footprint both in the Fab as well as in the sub-Fab.

A plan for continuous improvement of safety in future factories must be established. A thorough understanding of safety risks associated with automated equipment will lead to standards that assure safe working conditions for both people and product. These standards must be directed at the integrity of automated systems, the tools with which they interface, and the interfaces as well.

Our industry faces increasing environmental limitations. The availability of adequate water supply already places restrictions on the size and location of factories. The goal is to build factories that minimize resource consumption and maximize resource reclamation. Effluents of environmentally toxic materials need to be reduced to near zero—perhaps to zero levels.

Conservation of energy is very critical, more than ever before. The constraint to this is the size of the factory, which then puts a very large potential pollution burden on the energy provider and the wafer fabrication plant.

While much of the responsibility for ESH programs rests with the equipment suppliers, application of advanced resource management programs will have a significant impact. International ESH standardization and design programs can be greatly enhanced through training programs established for and by the industry. Consideration of ESH standards in equipment design, maintenance, de-commissioning, and final disposition will reap substantial rewards in ESH performance as well as cost. Refer to the *Environment, Safety, and Health chapter* for comprehensive information and to the new chemical screening tool (*Chemical Restrictions Table*).

YIELD MANAGEMENT

Development of good yield management strategies reduces costs and investment risks. A factory yield model defines typical operational performance and permits a Pareto of performance and yield detractors. A factory model based on experimental mapping of process parameters and process control strategies reduces the need for increased metrology tools and monitor wafers. It is also critical to determine tolerance variations for process parameters and interactions between processes to reduce reliance on end-of-line inspections. Factory models should also be capable of handling defect reduction inputs to assure efficient factory designs for rapid construction, rapid yield ramp, high equipment utilization, and extendibility to future technology generations.

Yield management systems (YMS) must be developed that can access and correlate information from multiple data sources. YMS should also work with measurement/metrology equipment from multiple suppliers using pre-competitive standards based data formats. Refer to the *Yield Enhancement* chapter for a more comprehensive discussion on YMS.

METROLOGY

Metrology systems must be fully integrated into the factory information and control systems to facilitate run-to-run process control, yield analysis, material tracking through manufacturing, and other off-line analyses. The scope of measurement data sources will extend from key suppliers (masks and silicon wafers) through Fab, probe, assembly, final test and be linked to business enterprise level information. This data-to-information capability should exist as early as possible in a factory's history to minimize the time spent qualifying equipment and ramping the factory to production. Data volumes and data rates will continue increase dramatically due to wafer size increases and process technology shrinks. Analysis of this data will require connectivity and correlation to multiple data sources across the factory (Fab, probe, etc.). In 300 mm factories, review and classification tools may eventually appear in clusters or integrated clusters to create a more efficient factory interface. Some 30 0mm process equipment will include integrated measurement (IM) capabilities to reduce cycle time and wafer-to-wafer process variance. Integrated metrology must be fully integrated to the process equipment embedded control system and not add to the process equipment footprint, and be selected carefully by IC makers to balance. Integrated management costs must be carefully balanced against benefits to make specific implementation decisions that improve the overall factory productivity. Refer to the *Metrology* chapter for overall metrology topics.

ASSEMBLY AND PACKAGING

Packaging has become the limiting element in system cost and performance. The Assembly and packaging role is expanding to include system level integration functions. Process flow complexity and the proliferation of form factors in recent years have resulted in increased use of materials handling and software automation in the assembly and packaging phase of semiconductor manufacturing, leading to higher costs and flexibility challenges.

Material handling costs are driven by indirect materials such as carts, magazines, carriers, and trays, which are used to transport product between tools and transfer product within tools. Other material handling costs result from capital equipment used to load and/or transfer product.

Equipment automation software costs are driven by the lack of relevant standards, and/or the lack of adherence to existing standards. This requires the development of custom software interface. Demand in this software automation in the assembly and packaging areas has increased dramatically as the desire to trace units throughout their production cycle are coupled with the desire to have the data and control that increases capital equipment productivity.

To meet industry trends of declining average selling prices and increased market segmentation, significant cost reductions and flexibility improvements are needed in the areas of material handling and equipment communications. Applying the roadmap process to identify requirements and implement standards for carriers, media, and hardware/software equipment interfaces in assembly and packaging manufacturing are potential solutions to these cost issues. The *Assembly and Packaging chapter* details specific requirements for packaging technology.

STATIC CHARGE AND ELECTROMAGNETIC INTERFERENCE CONTROL

Electrostatic charge adversely impacts every phase of semiconductor manufacturing, causing three basic problems, as follows:

1. Electrostatic attracted (ESA) contamination increases as particle size decreases, making defect density targets more difficult to attain. Electrostatic attraction of particles to masks will become a more serious problem if future lithography methods eliminate the pellicle used to keep particles away from the mask focal plane.
2. Electrostatic discharge (ESD) causes damage to both devices and photomasks. Shrinking device feature size means less energy is required in an ESD event to cause device or mask damage. Increased device operating speed has limited the effectiveness of on-chip ESD protection structures and increased device sensitivity to ESD damage.
3. Equipment malfunctions due to ESD-related electromagnetic interference (EMI) reduce OEE, and have become more frequent as equipment microprocessor operating speeds increase.

These three problems occur where bare wafers and photomasks are produced, where devices are produced in wafer fabs, and where individual devices are produced in backend packaging, assembly, and test. (Link to supplemental material for additional details on ESD and background on static control.)

In addition to Static Charge Control, Electromagnetic interference (EMI) (see the standard SEMI E33 for definition)[10] causes variety of problems for semiconductor manufacturing, including, but not limited to, equipment lockup and malfunction, sensor misreading, metrology errors and others. There are many sources of EMI in semiconductor environment that include electromagnetic emission from ESD, operation of equipment, especially high-energy tools, wireless communication and alike. Co-location of sensitive equipment with high-energy tools, cabling, ground problems, improper maintenance of equipment and others further aggravate EMI problems.

As feature sizes decrease, the impacts described above are likely to become more pronounced, particularly for metrology equipment that utilizes beam-based processes to perform its intended functions. Therefore, understanding EMI phenomena, its impacts, and how to mitigate it in a cost effective fashion become more important as process technology progresses into the future.

Currently EMI is not well understood by the end user and thus leads to misdiagnosed problems and misapplied EMI mitigation/controls. This needs to be addressed at a global level to prepare for what is expected to be more electromagnetic-related impacts in the future. To address the above mentioned concern we propose the following:

- Formation of a working group to document electromagnetic trends in the form of a technology roadmap
- Research in this area to help better gauge EMI sensitivity

[10] *SEMI E33-94 - Specification for Semiconductor Manufacturing Facility Electromagnetic Compatibility.*

- Publication of a User Guide that documents:
  - EMI theory in usable terms
  - EMI case histories that clearly articulate the types of problems and typical solution paths
  - EMI measurement methodologies for real-world applications including the monitoring of EMI intensity and number of events in relevant areas.
  - EMI mitigation methods and industry common practices for assessment and audit of these methods.

To control and reduce the negative impact of EMI on wafers, materials and equipment, more comprehensive studies, advanced methods and measurement tools are needed.

FACTORY INTERFACE STANDARDS REQUIREMENTS

Standards work best when applied to pre-competitive areas and when there is a benefit to all participants. Successful development, implementation, and testing of non-proprietary standards have major ramifications on the factory ability to rapidly come online and ramp to full volume in a cost-effective manner. Standardization of inter-operating elements, especially interfaces between different systems in a factory, improves the industry's ability to manage rising factory complexity.

Global cooperation among IC manufacturers and equipment suppliers for 300 mm factories has resulted in the definition and implementation of many non-proprietary factory integration standards. This activity has provided enormous industry benefits by minimizing equipment development time, reducing the cost and risk of development, and has helped reduce factory complexity.

Figure 87 shows industry progress toward the development and implementation of 300 mm standards. It also identifies areas of future work where standards do not exist, but are needed. This is shown with respect to four critical areas of the factory, which have maximum benefits from global cooperation—production equipment, facility systems, material handling systems, and factory information and control systems. Refer to the supplemental file link for additional details on industry standards.

FOCUS AREA

In the year 2005 the Factory Integration evaluated several key technology areas that impact the Factory Integration near term and longer term needs and also cuts across all the Factory Integration sub-sections. This section provides details on the 3 key focus areas i.e. 1) Airborne Molecular Contamination (AMC), 2) Proactive Visualization and 3) Next Wafer Size (450 mm) challenges

AIRBORNE MOLECULAR CONTAMINATION (AMC)

Airborne Molecular Contamination (AMC) (see SEMI Std F21 for definition)[11] needs to be controlled in front-end and back-end of line operations in semiconductor fabs.

This control may be achieved fab-wide or at certain critical processes, potentially also at different levels for different processes. The "wafer environement contamination control" tables of the Yield Enhancement Chapter provide recommended contamination levels as follows:

a. AMC as measured/monitored in the cleanroom air and /or purge gas environment
b. Surface Molecular Contamination (SMC) on monitoring wafers

Cost effective integration of AMC controls into factory design and operation should incorporate a variety of measures all the way from detection of AMC sources through control methods up to the active protection of the wafer environment.

The sources of AMC originate both from outside and inside of the fab. The outside AMC sources origins are: industrial (e.g. organics, acids), traffic, agricultural (e.g. ammonia, hydrogen sulfide) and other pollution types. Unfortunately, when not controlled, the semiconductor factories exhausts themselves turn to a major external source for AMC (reversed back to the FAB). The inside AMC sources origins are: outgassing from construction materials (e.g. polymers, coatings,

[11] *SEMI F21-1102 - Classification of Airborne Molecular Contaminant Levels in Clean Environments.*

concrete), accidental releases of exhausts and chemicals used in the cleanroom for maintenance/cleaning/hook-up activities. All these may also lead to corrosion of wafer and facility materials, to damages in Boron silicate glass fiber filters and subsequent Boron release into the cleanroom. In addition, the personnel in the cleanroom are a source for AMC.

The AMC levels which are caused by outgassing from fab materials will typically reduce with time, when no additional sources are being added. The timely identification of the AMC sources determines which measures are appropriate in order to prevent from damage on the wafer.

Known active AMC control measures inside the facility are:

- Air washer/adsorber in the make-up air handling units
- Chemical filters in the re-circulating air flow
- Chemical filters for the Mini-environment/Stocker
- Purging of wafers and reticles carriers

Modeling and simulation tools are required to determine and validate the most appropriate integrated AMC control solutions. Furthermore, these tools should deliver a fair basis to estimate the cost effectiveness of the proposed solutions.

To keep the AMC under control multi-facetted programs are recommended. They include: Surface Molecular Contamination measurements and analyses, off-line sampling with impingers, on-line instrumentation, cooling traps, adsorbtion tubes. The great challenge and the essential goal is to elaborate a data management system, which links these measurements to metrology and provide feedback for APC and run-to-run control via a compatible data interfaces

PROACTIVE VISUALIZATION

Device makers are required to adapt their manufacturing resource and operation models to more complex and diversified business environment with flexibility and agility. SoC (System on Chip) manufacturing is a good example of the typical challenging manufacturing business models that expose distinct production deficiencies. Proactive visualization is an effort to grasp the manufacturing problems and requirements by breaking down and recapturing with a high degree of abstraction and the finer information granularity. Figure 86 shows a comprehensive and integrated visualization matrices and relationship. The table structure is a typical matrix with *manipulation* axes and *value* axes with layered structure.

Another aspect of proactive visualization is the delivery time structure. The possible trade-offs between delivery time and cost or between cycle time and device quality assurance need to be investigated. Delivery time can be broken down along with three viewpoints of; the fab resource, the fab operation, and, the product lot. Resource and fab operation viewpoints are usually used for maximization of throughput and minimization of manufacturing cost in LM/HV production model, whereas the product lot and fab operation viewpoints are usually used for cycle time reduction or delivery time conformance purposes. HM/LV production model requires all of these viewpoints for the higher level optimization. Some of the delivery time elements are lot size dependent. It is necessary to describe fab ability to handle the smaller lots.

The mean SoC order sizes are believed to shrink continuously as the larger diameter wafer transition proceeds and the short delivery time is persistently required. The cycle time trend needs to be captured along with the order size trend and the available maximum wafer diameters for volume production in ITRS Roadmap. Averaged cycle time for one mask layer can be a good metrics, and is expected to decrease together with the decreasing trend in the hypothetical default lot size.

STRATEGICALLY HIERARCHICAL QUALITY ASSURANCE

The current semiconductor fabrication equipment is very complex in terms of the discrete capabilities and a composite functionality. The reliability assurance is becoming a big challenge both for the equipment suppliers and users. The equipment activity may be divided into the following three hierarchical consecutive abstract activity domains;

1. Parametric process conditions,
2. Control activity in internal devices,
3. Subsystems or functional devices activity.

Currently the top domain activity is monitored and examined with limited parametric data for the process conditions. Since the underlying domains have not been well visualized, these 3 domains are not consecutively related in terms of process execution reliability.

Equipment Engineering Capability Guidelines by Selete/JEITA and ISMI (2002)[12] call for necessary collaborations between equipment suppliers and device makers with using high quality EE (equipment engineering) data collected through "the second port" on the equipment.

The gap in the process execution reliability chain may be fulfilled if effective collaborations between these consecutive domains and across the business boundary are established with the help of fine information granularity. Equipment reliability assurance contents (such as evidence data, data model, and verification specification) are to be exchanged between the equipment suppliers and the device makers for this to happen. EE data required in EEC guidelines will help provoke *Proactive Visualization* across the intra-company and the business boundaries in the industry to enable more strategic task sharing. The requirement of equipment supplier's involvement in *Proactive Visualization* has been well discussed and organized as a strategic proposal as *EEQA* (Equipment Engineering Quality Assurance).

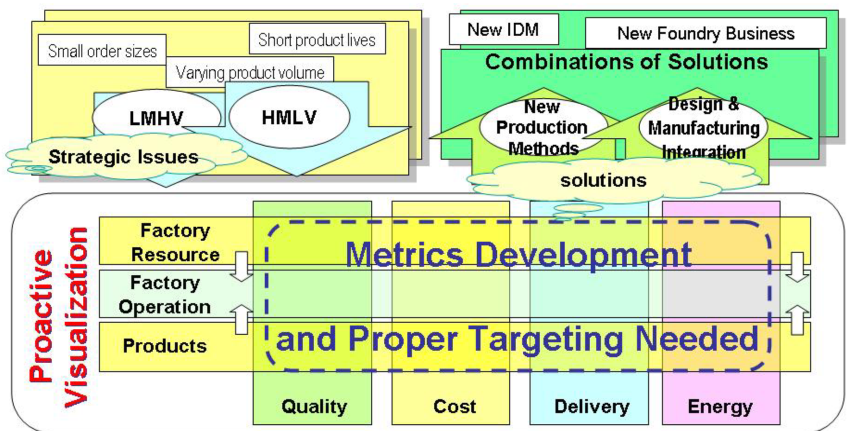


Figure 86 Comprehensive Analysis and Decision Makings Need Matrix Table with Manipulation and Value Axes

NEXT WAFER SIZE (450 MM) TRANSITION CHALLENGES

In keeping up with the Moore's law the Semiconductor Industry looks at increasing the wafer size as one viable option in addition to device innovations such as transistor design improvements, new materials, and lithography feature size reductions to reduce cost per function by ~30% each year over the past 30 years, while enabling factories to be highly productive. The last wafer size transition from 200mm to 300mm occurred 10 years ago and it is showing clear indication of ~30% cost improvement. As 300mm wafer production enters its 3rd major technology generation (130nm, 90nm, and 65nm), the industry must now start planning and making decisions to transition to the next wafer size, presumably 450mm, in a manner that manages risks and meets the operational needs of the future, including the economics. In the year 2005, the Factory Integration is evaluating the next wafer size transition with the interception date of 2012. Given that the 300mm transition required about 7 years of preparation time for IC makers and suppliers; it is expected that 450mm will also need similar preparation timeline as shown in Figure 87.

[12] *Equipment Engineering Capability Guidelines by Selete/JEITA and ISMI (2002).*

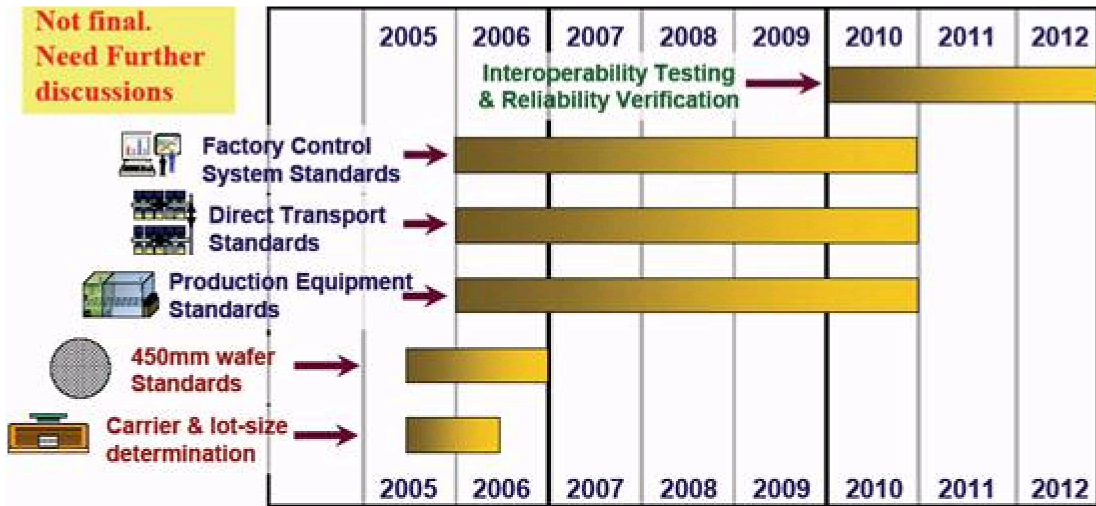


Figure 87 450 mm Timeline

This timeline starting in 2005 would enable critical technology decisions to be made before factory equipment and systems are designed. Based on several discussions among the ITRS members, the earliest technology decisions are to be made around wafer specifications, production lot-sizes, and wafer carrier characteristics, such as flexibility in the capacity, purging, etc., since these drive process and metrology equipment configurations, material handling systems, and overall facility/factory designs. Figure 88 shows the six key attributes that need to be evaluated for effective 450 mm factory design.

#1 Priority for 2005 Industry Analysis is Wafer Characterization

Attribute	Technology Decisions
Wafer	Material, Size, Thickness, ID, Registration, Edge Exclusion
Wafer Carrier	Number of Wafers, Size, Door Type, AMHS Strategy, ID
Production Equipment	Single wafer vs. mini-batch, cleanliness, interface standards, productivity targets relative to 300mm (NPW usage, etc.)
Factory	Factory Size, Egress, Cleanliness, Sub-Fab attributes, Clean-room height
Automated Material Handling Systems	Direct transport concepts, carrier delivery time, overall throughput, efficient storage concepts
Manufacturing Systems	Process Control & Yield Data Standards, Carrier delivery time, Decision Making Time, Data Flow

Figure 88 450 mm Key Attributes

Initial discussions on the 450 mm wafer transition within the Factory Integration team and also with the other TWG uncovered several technical as well as business challenges. Table 92 lists the challenges captured from these discussions.

Table 92 List of Next Wafer Size Challenges

Technology WG	*Next wafer size (450mm) challenges*
FI – Factory Operations	Business model: Need to define operations axes: High volume vs. Low volume; High mix vs. Low mix; front end vs. backend (Metal layers), Cu/Al; Logic vs. DRAM, WSPW (small versus large). Transportation lot size versus carrier lot size; More single wafer processes; 2–10 wafer lots; High mix issues; cycle time issues.
FI – Production Equipment	Mix use a certain small capacity mini-environment carrier (Ex: Bottom opening 5–10 wafer carrier); Conveyor transport; Small footprint tool buffering; 300 mm to 450 mm conversion? Equipment platform concept; Wafer gripping and edge exclusion; Alpha tool development?
FI – Factory Information & Control Systems	Factory automation (load lock, transportation method, etc.); Stringent process control needs for high mix small lot production
FI – AMHS	Conveyor transport may be required for 20k to 30k WSPM Fabs running small (5–10 wafer) Lot carriers; Impact on MPH; Transport batch size?
FI – Facilities	Extendibility of current fabs, watch out for increased sub-fab area; abatement point-of-use and new material issues; Height, vibration, floor density
Interconnect	Need a common team working on 450 mm issues (similar to 300i). Wafer edge exclusion (1.5 mm?); Cost of abatement due to NWS and new materials.
Front end Process (FEP)	450mm presents unprecedented challenges: Technical: meeting specs over larger areas); Economic: for wafer, equipment, and metrology suppliers; Critical path definition.: already late to meet development cycle; Standardization: Wafer spec (type, thickness, diameter tolerance); FEP will investigate at what generation we may have to switch to single wafer processing; 450mm issues will be highlighted in sub chapter, position paper
Lithography	Current focus on Immersion and EUVL (power, consumables); Fast reticle change; vibration specs; reticle storage issues
ESH	Ergonomics, Tool design, Chemical consumption concerns; AMC and particulate levels to be maintained; Regulations
Metrology	Need for Integrated Metrology continues? Data standards
Yield Enhancement	Wafer size configuration; traceability?
Assembly & Packaging	Wafer package (FOSB, FOUP, door configuration, etc.); traceability?
Other	Need a common team working on 450 mm issues (similar to 300i). Apply lessons learned from 200mm to 300 mm transition. We need to learn from LCD manufacturers.

It is imperative to start with defining key wafer attributes since in most cases, it drives the rest of the factory design decisions. To meet high-mix and fast cycle time requirements, it is likely that the industry may adopt a single-wafer processing strategy for all production equipment which would pose several challenges to equipment manufactures and operations that needs to be addressed in the coming years. In addition to single wafer processing versus mini-batch, it is necessary to evaluate: vehicle-based versus conveyor transport system, need for on-tool buffering, mini environment carriers that allow mix use of different capacities (Ex: bottom opening carriers) and flexible lot size to name a few. These critical decisions should be followed up by development of open industry standards in order to reduce the number of design permutations and to achieve cost-efficiency within the factory. Figure 89 is the recommended approach to address the Next Wafer Size initiate in order to be ready for the 2012 timeline.

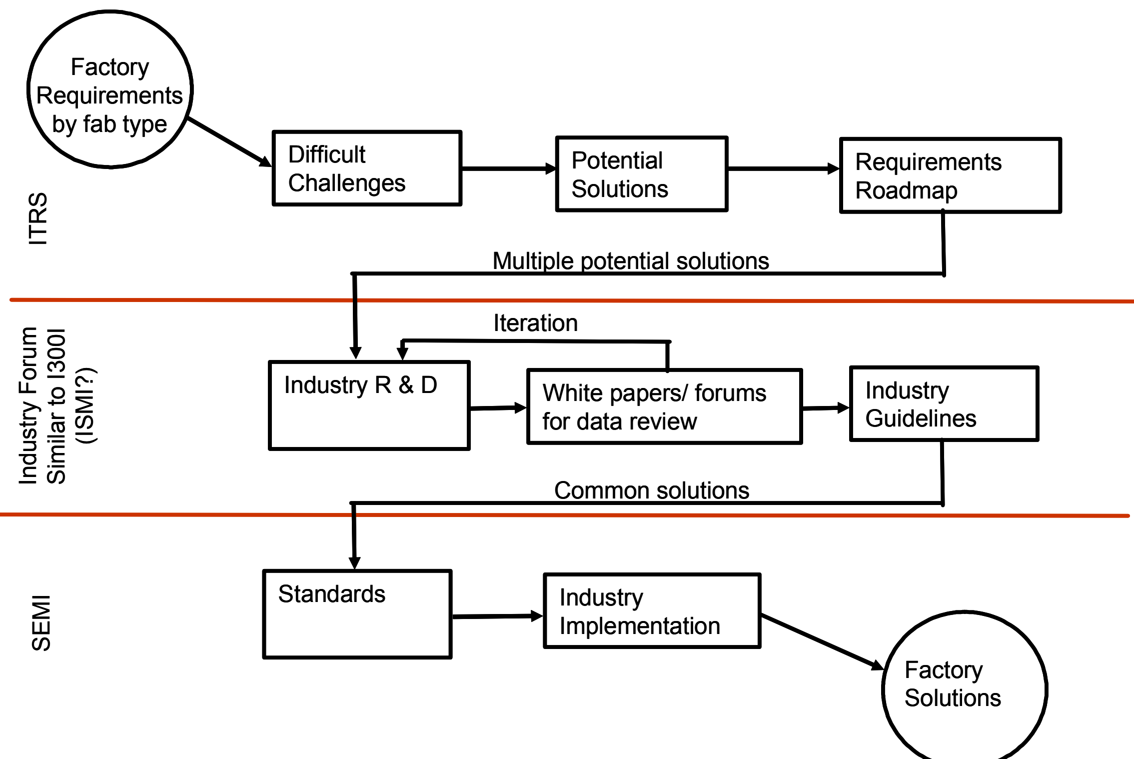


Figure 89 Approach to Address 450 mm Initiative

SUMMARY

Factory Integration section of the ITRS focuses on integrating all the factory components needed to efficiently produce the required products in the right volumes on schedule while meeting cost targets. In 2005, the Factory Integration chapter provides the technical requirements by the five sub-groups and also the proposed potential solutions. This section also provides Factory Integration related challenges from the crosscut issues and key focus areas (AMC, proactive visualization and next wafer size) that need to be addressed in order to keep up with the technology generation changes and at the same time maintaining decades-long trend of 30% per year reduction in cost per function. The challenges addressed in the Factory Integration chapter is a combination of manufacturing, process and business related issues that needs to be addressed collectively by the ITRS Factory Integration global team.