INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

INTERCONNECT

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

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INTERCONNECT

SCOPE

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap for Semiconductors (ITRS) emphasized an ongoing change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low-κ dielectric introduction for microprocessers (MPUs) and application-specific ICs (ASICs) was one of the central issues for the 2003 ITRS Interconnect area. The 2005 ITRS shows the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A new crosstalk metric is also introduced. The technical product driver for the smallest feature size remains the dynamic random access memory chip (DRAM), however, the Metal 1 pitch for MPU's is expected to equal that of DRAM by 2010.

Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, radio frequency (RF), or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant predicted by the ITRS has been problematic. Fluorine doped silicon dioxide ($\kappa = 3.7$) was introduced at 180 nm, however insulating materials with $\kappa = 2.7–3.0$ were not widely used until 90 nm. The reliability and yield issues associated with integration of these materials with dual damascene copper processing proved to be more challenging than predicted. The integration of porous low-κ materials is expected to be even more challenging. Since the development and integration of these new low-κ materials is rather time invariant, the predicted acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable κ to later technology generations. The κ values of the bulk dielectric materials are defined in the Dielectric Potential Solutions figure and the range of effective κ values for the integrated dielectric stack is listed in the Technology Requirements tables. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge. (For a more thorough explanation, access the link to the calculation of the effective κ for various integration schemes.)

The conductor, barrier, and nucleation potential solutions have been grouped into sections for local, Metal 1, intermediate, and global wiring levels, as well as passive devices. Atomic layer deposition (ALD), characterized by excellent conformality and thickness control, is still receiving attention for applications in the deposition of conductors, barriers, nucleation layers and high-κ dielectric materials. The Cu resistivity rise due to electron scattering effects poses a critical challenge even in the near term, and is also an area of focus. Characterization shows significant contributions to resistivity by scattering from both grain boundaries and interfaces. Research to date has not identified any solutions that would have a large impact on this phenomenon.

Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. The resulting difficult challenge for etch is to form precise trench and via structures in low-κ dielectric material to reduce variability in RC. Etch-induced sidewall damage will increase κ and must be minimized. Post-etch resist strip has also been shown to cause damage to low-κ materials with a resultant increase in the effective κ of the structure. Attention to the ionic species in both etch and strip that cause the damage has been an area of focus. Novel approaches to repair the damage, such as supercritical CO_2, are also being investigated.

The Planarization Potential Solutions section has been divided into sections for planarization of conductors and insulators. One of the primary integration challenges with low-κ materials is adhesion failure between barrier or capping materials and the dielectric during the planarization process. Porous low-κ materials are even more problematic and are therefore one of the key focus areas for planarization development efforts.

DIFFICULT CHALLENGES

Table 79 highlights and differentiates the five key challenges in the near term (≥ 32 nm) and long term (< 32 nm). In the near term, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce the dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be mitigated.

Dimensional control is a key challenge for present and future interconnect technology generations. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratio (A/R) of intermediate and global levels. At 45 nm, feature size effects, such as electron surface scattering, will increase the effective resistivity and may require new conductor technologies. Cu and low κ will continue to find applications in future chip generations, but for global wiring, new interconnect solutions such as RF, optical and three-dimensional integrated circuit (3D IC) may be required to improve delay and power, which will bring even more material and process integration challenges.

Feature size reduction, new materials, and damascene structures areall a challenge to on-chip metrology capability for interconnect development and manufacture. Critical dimension (CD) measurements are needed for very high aspect ratio features and ultra-thin barriers. Methods must be developed to accommodate the increased complexity of the wiring levels of future chips. Other metrology challenges include measuring resistivity and dielectric constant at high frequency, adhesion and mechanical properties.

Table 79 Interconnect Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.

Table 79 Interconnect Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*
CMP—chemical mechanical planarization DRAM—dynamic random access memory

TECHNOLOGY REQUIREMENTS

To adequately describe the wiring needs of interconnect, near term (2005–2011) and long term (2012–2020) technology requirements and potential solutions are addressed for two specific classes of products: MPUs and DRAM. For MPUs, Metal 1, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a hierarchical scaling methodology that has been broadly adopted. The 2005 roadmap recognizes an acceleration of MPU product introduction to a two-year cycle for the next two technology generations (2007 and 2009) and reversion to a three-year cycle after 2009. It also projects that the Metal 1 pitch for MPU will become equivalent to that of DRAM in 2010. In addition, the difference in pitch between the MPU Metal 1 and intermediate wires disappears by 2009. The latest roadmap also clarifies the issue of MPU Metal 1 "contacted pitch" as referring to lines with staggered rather than side-by-side contacts. The use of staggered contacts has been the standard MPU design methodology for quite some time.

The accelerated scaling of MPU pitch has aggravated the copper electromigration problem. J_{max} limits for current dielectric cap technology for copper will be exceeded by 2008. A substantial effort is being directed toward development of selective metal cap technology for copper, such as CoWP, which will bring near-term relief for this problem. However, there is still concern about yield loss due to metal shorts caused by these selective processes. Improved dielectric caps are also being explored.

Electron scattering models have been improved and can now predict the Cu resistivity rise as a function of line width and aspect ratio. There is a significant contribution to the increase in resistivity from both grain boundary and interface electron scattering as shown in Figure 68. To date, research has not identified any potential solutions to this problem.

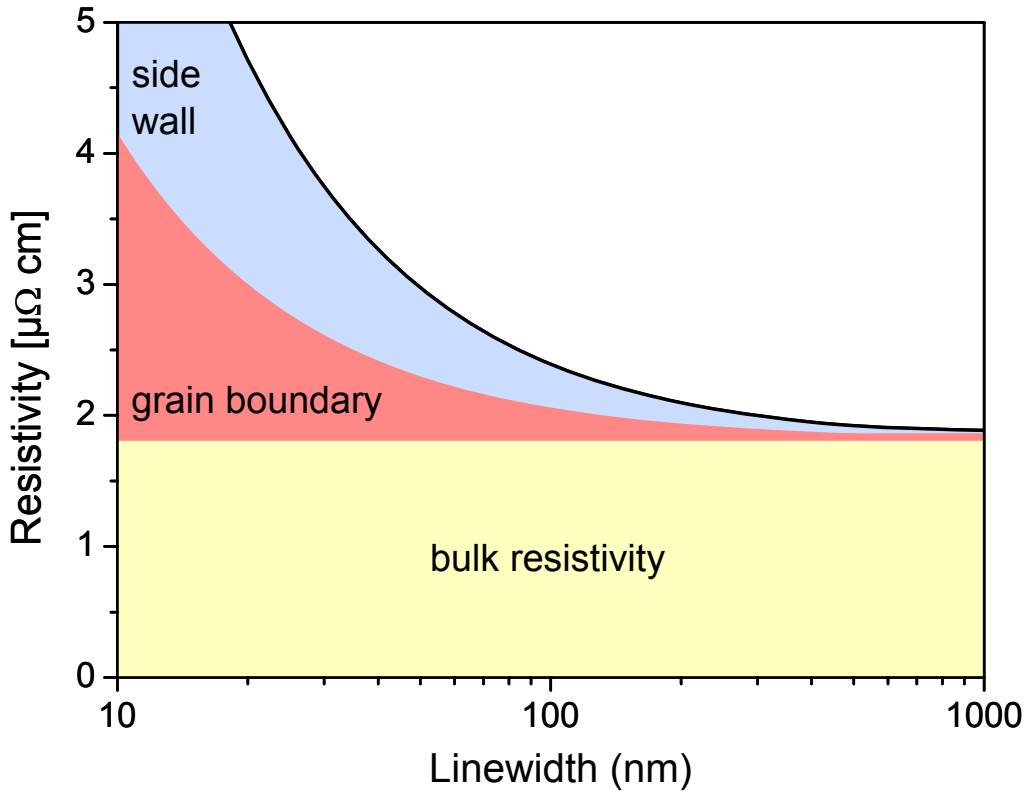


Figure 68 Cu Resistivity

Accordingly, Cu resistivity numbers for minimum Metal 1, intermediate and global wires are now listed for all the years of the roadmap. The effect of this resistivity increase on the RC performance metrics is also calculated and included in the technology requirements table. Three-dimensional control of critical dimension (3DCD) interconnect features has been listed as one of the critical challenges in several editions of the ITRS. The total variability of M1 wire resistance due to CD variation and scattering has been calculated and is also included in the MPU technology requirements table. Since the length of Metal 1 and intermediate wires usually shrinks with traditional scaling, their impact of their delay on performance is minor. Global interconnects, which have the greatest wire lengths, will be impacted most by the degraded delay. The benefit of materials changes or some amelioration of the Cu resistivity rise will be insufficient to meet overall performance requirements. Figure 69 shows the delay of Metal 1 and global wiring in future generations. Repeaters can be incorporated to mitigate the delay in global wiring but consume power and chip area.

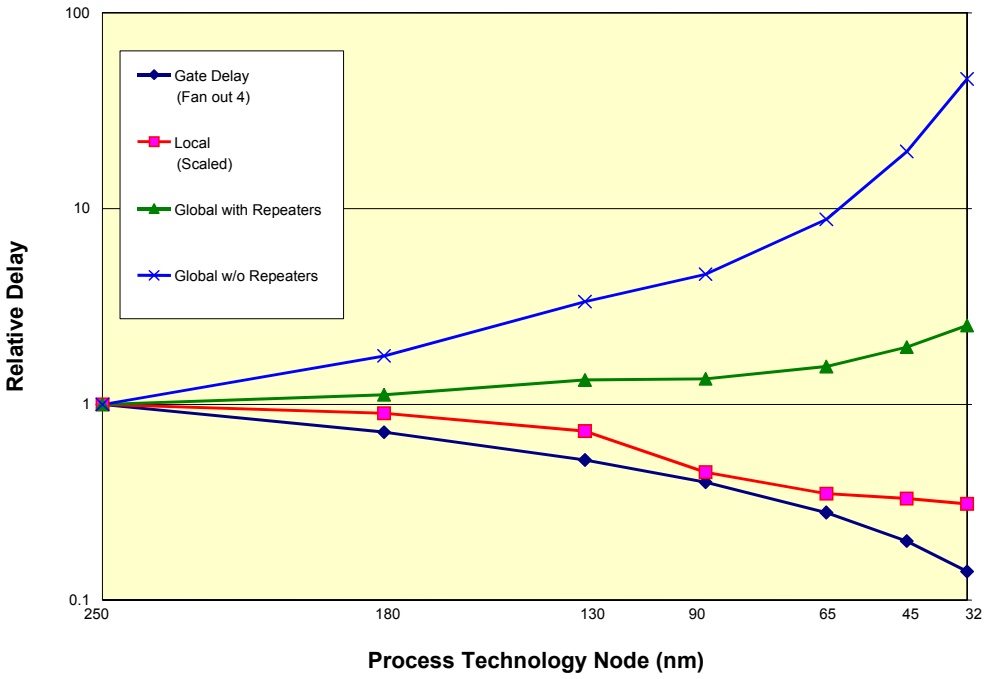


Figure 69 Delay for Metal 1 and Global Wiring versus Feature Size

In the long term, new design or technology solutions (such as 3D IC, free space RF, optical interconnect) will be needed to overcome the delay, power, and bandwidth limitations of traditional interconnect. Inductive effects will also become increasingly important as the operating frequency increases, and additional metal patterns or ground planes may be required for inductive shielding. As supply voltage is scaled or reduced, crosstalk has become an issue for all clock and signal wiring levels. A new crosstalk metric has been introduced in the 2005 ITRS for Metal 1, intermediate and global wires. The metric calculates the line length where 25% of the switching voltage is induced on a minimum pitch victim wire. This critical line length for a minimum global wire in 2020 is less than 30% of the line length in 2005. Therefore joint efforts with the design community are needed to address crosstalk issues. The 2005 Roadmap continues to reflect the ongoing reduction of dielectric constant for future technology generations as new porous low-κ dielectric materials and eventually air gap technology are introduced.

MPU CROSS SECTION

MPUs utilize a high number of metal layers with a hierarchical wiring approach of steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. Refer to Figure 70.

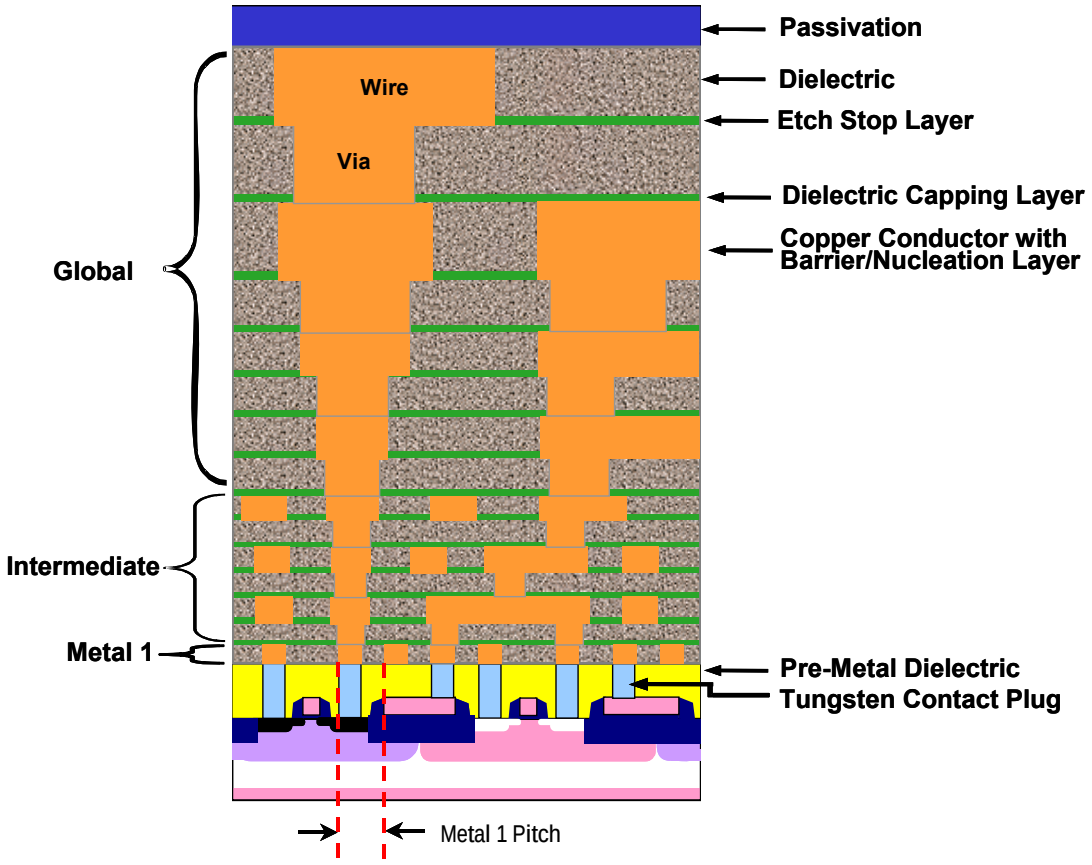


Figure 70 Cross-section of Hierarchical Scaling—MPU Device

To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified solely to meet performance requirements.

ASIC CROSS SECTION

ASICs share many of the technology attributes of MPUs, for example, Cu wiring and low-κ dielectrics. ASIC design methodology is generally more regular, consisting of Metal 1, intermediate, semi-global (2× intermediate) and global (4× intermediate) wire pitches. An ASIC only, semi-global wiring pitch has been added to the MPU technology requirements table in 2005. A typical ASIC cross section is shown in the Figure 71 below.

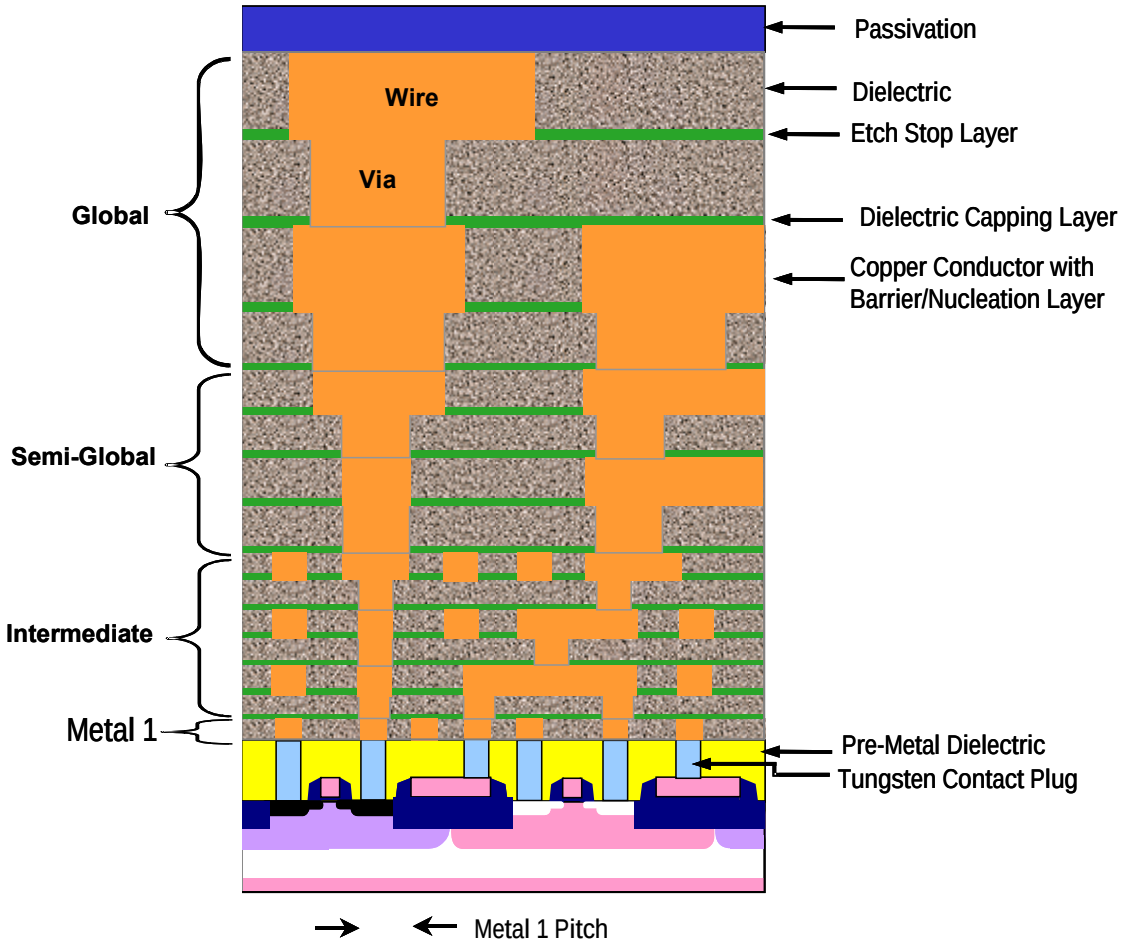


Figure 71 Cross-section of Hierarchical Scaling—ASIC Device

DRAM interconnect technology reflects the most aggressive metal pitch and highest aspect ratio contacts and will continue to provide the most significant challenges in dimensional control and defect management. However, the MPU Metal 1 pitch is projected to equal that of DRAM in 2010. The introduction of low-κ dielectric materials (fluorinated silica glass (FSG)) is underway and copper at 65 nm half pitch is required to meet the performance of high-speed memory products. However, the pricing sensitivity of the marketplace may delay introduction if cost savings associated with copper are not realized. This suggests that capability for aluminum processing must be continuously improved and extended.

Damascene processing flows dominate MPU/ASIC fabrication methodologies and usage in DRAM is expected to broaden. Figure 72 illustrates several typical interlevel dielectric (ILD) architectures available to create the interconnect wiring levels. While current copper damascene processes utilize physical vapor deposited (PVD) Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to end of the year of the forecasted roadmap (2020) but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of damascene features. Surface segregated, chemical vapor deposition (CVD), ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required.

Near-term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for decoupling and metal-insulator-metal (MIM) capacitors and materials with high remanent polarization for ferroelectric memories. The thermal, mechanical, and electrical properties of these new materials present a formidable

challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials will be required that have sufficient optical contrast to serve as low-loss waveguides.

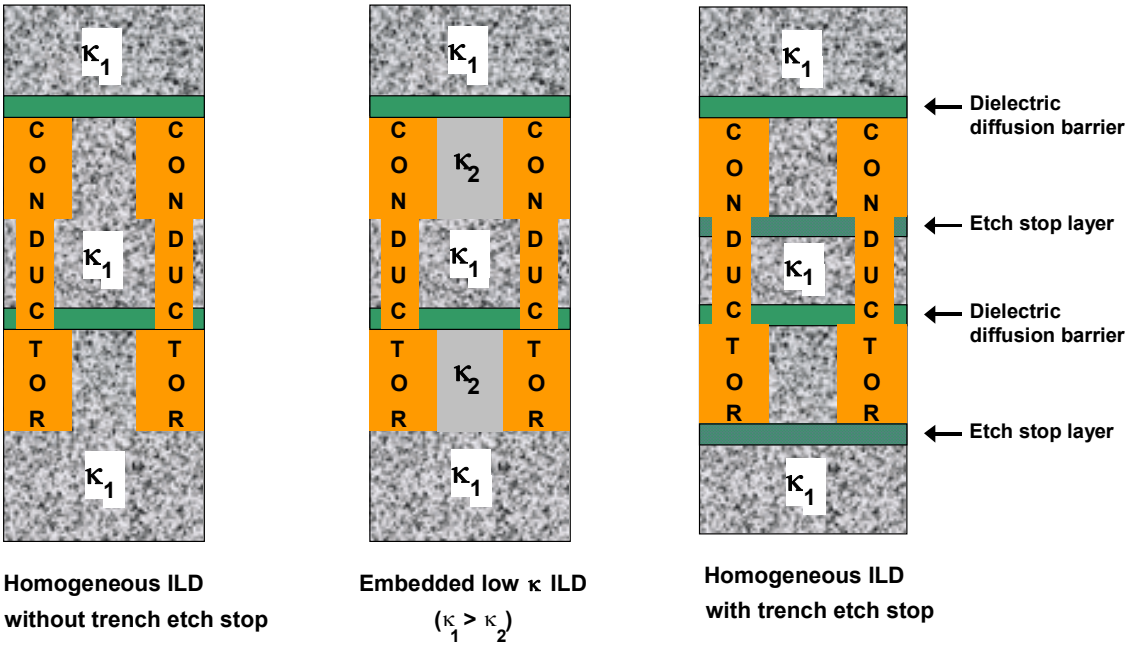


Figure 72 Typical ILD Architectures

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long-term solution. For copper CMP, minimization of erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Further research is needed to improve planarization processes (with associated end-point) that are compatible with low-κ dielectrics characterized by low density and poor mechanical strength. Improvements in post-CMP clean will be critical in achieving the low defect densities required for future devices. Etch, resist strip, and post-etch cleans must be developed that maintain the desired selectivity to etch stop layers and diffusion barriers, but that do not degrade low-κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

Table 80a MPU Interconnect Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Number of metal levels	**11**	**11**	**11**	**12**	**12**	**12**	**12**	**12**	**13**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	**1019**	**1212**	**1439**	**1712**	**2000**	**2222**	**2500**	**2857**	**3125**
FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	**4.9**	**4.1**	**3.5**	**2.9**	**2.5**	**2.3**	**2**	**1.8**	**1.6**
J_{max} (A/cm^2) – intermediate wire (at 105ºC)	**8.91E+05**	**1.37E+06**	**2.08E+06**	**3.08E+06**	**3.88E+06**	**5.15E+06**	**6.18E+06**	**6.46E+06**	**8.08E+06**
Metal 1 wiring pitch (nm)	**180**	**156**	**136**	**118**	**104**	**90**	**80**	**72**	**64**
Metal 1 A/R (for Cu)	**1.7**	**1.7**	**1.7**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.9**
Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	**307**	**409**	**486**	**626**	**783**	**966**	**1224**	**1357**	**1572**
Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	**440**	**612**	**767**	**1044**	**1388**	**1792**	**2392**	**2857**	**3451**
Conductor effective resistivity (μΩ–cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	**3.15**	**3.29**	**3.47**	**3.67**	**3.9**	**4.08**	**4.3**	**4.63**	**4.83**
Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]	**6.5**	**5.6**	**4.8**	**4.3**	**3.7**	**3.3**	**2.9**	**2.6**	**2.4**
Line length (μm) where τ = RC delay (Metal 1 wire) no scattering	**53**	**43**	**36**	**29**	**24**	**20**	**17**	**15**	**13**
Line length (μm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4]	**136**	**118**	**107**	**96**	**90**	**84**	**79**	**73**	**61**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**15**	**13**	**12**	**11**	**9**	**8**	**7**	**6**	**6**
Total Metal 1 resistance variability due to CD erosion and scattering (%) [4]	**28**	**29**	**28**	**29**	**30**	**30**	**31**	**32**	**32**
Intermediate wiring pitch (nm)	**200**	**167**	**140**	**118**	**104**	**90**	**80**	**72**	**64**
Intermediate wiring dual damascene A/R (Cu wire/via)	**1.7/1.5**	**1.7/1.6**	**1.8/1.6**	**1.8/1.6**	**1.8/1.6**	**1.8/1.6**	**1.8/1.6**	**1.9/1.7**	**1.9/1.7**
Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	**254**	**360**	**437**	**626**	**797**	**984**	**1246**	**1334**	**1596**
Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	**355**	**527**	**682**	**1039**	**1413**	**1825**	**2436**	**2784**	**3504**

Table 80a MPU Interconnect Technology Requirements—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Conductor effective resistivity (μΩ–cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	**3.07**	**3.22**	**3.43**	**3.65**	**3.9**	**4.08**	**4.3**	**4.59**	**4.83**
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**7.3**	**6**	**5.2**	**4.3**	**3.7**	**3.3**	**2.9**	**2.6**	**2.4**
Line length (μm) where τ = RC delay (intermediate wire) no scattering	**59**	**45**	**38**	**29**	**24**	**20**	**17**	**15**	**13**
Line length (μm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4]	**235**	**185**	**165**	**136**	**126**	**116**	**106**	**95**	**80**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**17**	**14**	**13**	**11**	**9**	**8**	**7**	**7**	**6**
Semi-global wire pitch (nm) (ASIC only)	**400**	**334**	**280**	**236**	**208**	**180**	**160**	**144**	**128**
Minimum global wiring pitch (nm)	**300**	**250**	**210**	**177**	**156**	**135**	**120**	**108**	**96**
Ratio range (global wiring pitches/intermediate wiring pitch)	**1.5–10**	**1.5–12**	**1.5–14**	**1.5–17**	**1.5–20**	**1.5–22**	**1.5–25**	**1.5–29**	**1.5–31**
Global wiring dual damascene A/R (Cu wire/via)	**2.2/2.0**	**2.2/2.0**	**2.3/2.1**	**2.3/2.1**	**2.4/2.2**	**2.4/2.2**	**2.4/2.2**	**2.5/2.3**	**2.5/2.3**
Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	**96**	**139**	**168**	**242**	**301**	**371**	**470**	**511**	**611**
Interconnect RC delay (ps) for 1 mm Cu min pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	**111**	**165**	**209**	**316**	**410**	**523**	**687**	**787**	**977**
Conductor effective resistivity (μΩ–cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	**2.53**	**2.62**	**2.73**	**2.87**	**3.00**	**3.10**	**3.22**	**3.39**	**3.52**
Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3]	**7.3**	**6**	**5.2**	**4.3**	**3.7**	**3.3**	**2.9**	**2.6**	**2.4**
Line length (μm) where τ = RC delay (global wire at minimum pitch – no scattering)	**95**	**73**	**62**	**47**	**39**	**33**	**27**	**24**	**20**

Table 80a MPU Interconnect Technology Requirements—Near-term Years (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Line length (µm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4]	**170**	**147**	**137**	**130**	**128**	**124**	**120**	**115**	**97**
Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	**220**	**220**	**230**	**230**	**240**	**240**	**240**	**250**	**250**
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**24**	**21**	**19**	**17**	**15**	**14**	**13**	**13**	**10**
Conductor effective resistivity (µΩ–cm) Cu wiring, assumes no scattering	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Interlevel metal insulator – effective dielectric constant (κ)	**3.1–3.4**	**3.1–3.4**	**2.7–3.0**	**2.7–3.0**	**2.5–2.8**	**2.5–2.8**	**2.5–2.8**	**2.1–2.4**	**2.1–2.4**
Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	**≤ 2.7**	**≤ 2.7**	**≤ 2.4**	**≤ 2.4**	**≤ 2.2**	**≤ 2.2**	**≤ 2.2**	**≤ 2.0**	**≤ 2.0**

**Refer to Executive Summary Figure 4 for definition of metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

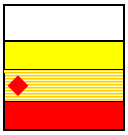


Table 80b MPU Interconnect Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal levels	**13**	**13**	**13**	**14**	**14**	**14**	**14**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	**3571**	**4000**	**4545**	**5000**	**5555**	**6250**	**7143**
FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	**1.4**	**1.3**	**1.1**	**1**	**0.9**	**0.8**	**0.7**
J_{max} (A/cm^2) – intermediate wire (at 105ºC)	**1.06E+07**	**1.14E+07**	**1.47E+07**	**1.54E+07**	**1.80E+07**	**2.23E+07**	**2.74E+07**
Metal 1 wiring pitch (nm)	**56**	**50**	**44**	**40**	**36**	**32**	**28**
Metal 1 A/R (for Cu)	**1.9**	**1.9**	**2**	**2**	**2**	**2**	**2**

Table 80b MPU Interconnect Technology Requirements—Long-term Years (continued)

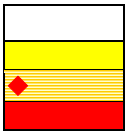
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	**2053**	**2346**	**2943**	**3563**	**3754**	**4752**	**6207**
Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	**4853**	**5951**	**8040**	**10252**	**11432**	**15853**	**23105**
Conductor effective resistivity (μΩ-cm) Cu Metal 1 wiring including effect of width dependent scattering and a conformal barrier of thickness specified below	**5.2**	**5.58**	**6.01**	**6.33**	**6.7**	**7.34**	**8.19**
Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3]	**2.1**	**1.9**	**1.7**	**1.5**	**1.3**	**1.2**	**1.1**
Line length (μm) where τ = RC delay (Metal 1 wire) no scattering	**10**	**9**	**7**	**6**	**5**	**5**	**4**
Line length (μm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4]	**52**	**47**	**41**	**36**	**33**	**29**	**24**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array	**5**	**5**	**4**	**4**	**4**	**3**	**3**
Total Metal 1 resistance variability due to CD erosion and scattering (%) [4]	**31**	**33**	**32**	**33**	**35**	**33**	**33**
Intermediate wiring pitch (nm)	**56**	**50**	**44**	**40**	**36**	**32**	**28**
Intermediate wiring dual damascene A/R (Cu wire/via)	**1.9/1.7**	**1.9/1.7**	**2.0/1.8**	**2.0/1.8**	**2.0/1.8**	**2.0/1.8**	**2.0/1.8**
Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	**2085**	**2382**	**2982**	**3610**	**3803**	**4813**	**6287**
Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	**4927**	**6042**	**8147**	**10386**	**11581**	**16059**	**23405**
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	**5.2**	**5.58**	**6.01**	**6.33**	**6.7**	**7.34**	**8.19**
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**2.1**	**1.9**	**1.7**	**1.5**	**1.3**	**1.2**	**1.1**
Line length (μm) where τ = RC delay (intermediate wire) no scattering	**10**	**9**	**7**	**6**	**5**	**5**	**4**
Line length (μm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4]	**68**	**60.5**	**53**	**46**	**43**	**40**	**37**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% x height, 50% areal density, 500 μm square array	**6**	**5**	**4**	**4**	**4**	**3**	**3**
Semi-global wire pitch (nm) (ASIC only)	**112**	**100**	**88**	**80**	**72**	**64**	**56**
Minimum global wiring pitch (nm)	**84**	**75**	**66**	**60**	**54**	**48**	**42**
Ratio range (global wiring pitches/intermediate wiring pitch)	**1.5–36**	**1.5–40**	**1.5–45**	**1.5–50**	**1.5–56**	**1.5–63**	**1.5–71**
Global wiring dual damascene A/R (Cu wire/via)	**2.5/2.3**	**2.6/2.4**	**2.6/2.4**	**2.6/2.4**	**2.8/2.5**	**2.8/2.5**	**2.8/2.5**

Table 80b MPU Interconnect Technology Requirements—Long-term Years (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm	798	896	1157	1400	1433	1814	2370
Interconnect RC delay (ps) for 1 mm Cu minimum pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	1353	1601	2210	2794	2983	4064	5795
Conductor effective resistivity (μΩ-cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	3.73	3.93	4.20	4.39	4.58	4.93	5.38
Barrier/cladding thickness (for minimum pitch Cu global wiring) (nm) [3]	2.1	1.9	1.7	1.5	1.3	1.2	1.1
Line length (μm) where τ = RC delay (global wire at minimum pitch - no scattering)	16	14	11	10	9	7	6
Line length (μm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4]	85	79	71	64	61	55	49
Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	250	260	260	260	280	280	280
Cu thinning global wiring due to dishing (nm), 100 μm wide feature	10	9	8	7	7	6	6
Conductor effective resistivity (μΩ-cm) Cu wiring, assumes no scattering	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ)	2.1–2.4	1.9–2.2	1.9–2.2	1.9–2.2	1.6–1.9	1.6–1.9	1.6–1.9
Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	≤ 2.0	≤ 1.8	≤ 1.8	≤ 1.8	≤ 1.6	≤ 1.6	≤ 1.6

**Refer to Executive Summary Figure 4 for definition of metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 80a and b:
[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for Metal 1 and five intermediate wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.
[2] This metric is calculated by assuming that a 5 FIT (failure in ten thousand) reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.
[3] Calculated for a conformal layer to meet minimum effective conductor resistivity with no scattering.
[4] Crosstalk is a calculated value. This metric will be managed by IC design.

Table 81a DRAM Interconnect Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Number of metal layers	4	4	4	4	4	4	4	4	4
Contact A/R – stacked capacitor	15	16	16	17	17	>20	>20	>20	>20
Metal 1 wiring pitch (nm) *	160	140	130	114	100	90	80	72	64
Specific contact resistance (Ω-cm^2) for n^+ Si	2.50E-08	2.30E-08	2.00E-08	1.70E-08	1.40E-08	1.20E-08	9.80E-09	8.20E-09	6.90E-09
Specific contact resistance (Ω-cm^2) for p^+ Si	4.50E-08	3.80E-08	3.20E-08	2.70E-08	2.20E-08	1.80E-08	1.50E-08	1.30E-08	1.10E-08
Specific via resistance (Ω-cm^2)	7.00E-10	6.00E-10	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10
Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu	3.3	3.3	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ)	3.6–4.1	3.6–4.1	3.6–4.1	3.1–3.4	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

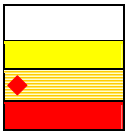
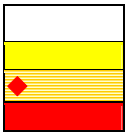


Table 81b DRAM Interconnect Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 Half Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal layers	4	4	4	4	4	4	4
Contact A/R – stacked capacitor	>20	>20	>20	>20	>20	>20	>20
Metal 1 wiring pitch (nm) *	56	50	44	40	36	32	28
Specific contact resistance (Ω-cm^2) for n^+ Si	5.80E-09	4.80E-09	4.00E-09	3.40E-09	2.80E-09	2.34E-09	1.96E-09
Specific contact resistance (Ω-cm^2) for p^+ Si	9.20E-09	7.40E-09	6.20E-09	5.10E-09	4.30E-09	3.60E-09	3.01E-09
Specific via resistance (Ω-cm^2)	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.88E-10	4.90E-10
Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ)	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



POTENTIAL SOLUTIONS

DIELECTRIC POTENTIAL SOLUTIONS

The industry is still in the early stages of a very difficult transition from silicon dioxide, silicon nitride and the relatively simple dual damascene integration process of full via first (FVF). These dielectric materials exhibit some of the best combinations of mechanical, electrical, and chemical stability properties that integration engineers have had the luxury of working with. The FVF integration process requires the fewest number of deposition layers to integrate, and yields the lowest effective dielectric constant value relative to the bulk dielectric constant of the ILD layer. In the future, a continual growth in the number of individual dielectric layers constituting the ILD stack (cap, via, trench, etch stop, CMP stop) is most likely. This growth will present adhesive and cohesive challenges associated with the increasing number of interfaces of dissimilar materials. The ability to cluster the deposition processing of sequential layers to minimize contamination and reduce cost of ownership (CoO) has become increasingly more difficult. Alternate curing technologies are being introduced to address a combination of deficiencies in adhesion and cohesion strength limitations, porogen removal and remediation of materials damaged in subsequent processing steps. The industry has chosen an overall evolutionary path for the adoption and introduction of low-κ ILD materials instead of the revolutionary path contemplated in the ITRS 2001 document. This evolutionary path may be associated either with the current family of low-κ ILD materials (PECVD, with incremental reductions of κ value) and/or the original low-κ ILD integration scheme (hybrid, with independent roadmaps for each dielectric layer).

New dielectric material requirements must encompass the needs of both conventional and novel device architectures as well as almost every existing end use. Some dielectric materials are finding additional uses in alternate locations of the BEOL structure with new emphasis on the required combination of electrical, mechanical and processing properties. Even with new and ever more stringent requirements for future technology generations, the lifetime of the existing class of silica based dielectric materials has been successfully extended because of challenges with the material properties or integration schemes required of these new ILD materials. The following four overall BEOL dielectric challenges still remain valid throughout the fifteen-year scope of this roadmap:

- Development of true low-κ materials and manufacturing processes capable of achieving the minimum effective permittivity (κ_{eff}) possible, for maximum device performance at a viable performance/price ratio, for Cu dual damascene technology
- Rapid understanding of the current reliability and failure modes associated with emerging low-κ ILD materials, dielectric barrier materials, environmental effects and packaging structures
- Development of moderate (κ >20) to high (κ >100) permittivity materials and manufacturing processes capable of achieving continually higher bit density at a viable bit/price ratio for stand-alone memory applications, decoupling and MIM capacitors for MPU/ASICs and system-on-a-chip (SOC).
- Sufficient development activity focused on invention and integration of new materials for emerging technologies to replace conventional wiring-based electronics, with alternatives such as RF, optical, and bio-based interconnect.

To address the range of dielectric material requirements and add focus to each specific application within the BEOL, the Dielectric Potential Solutions Figure 73 has been divided by application and a section was added to illustrate the importance of deposition and cure technology within the platform development for dielectric materials.

The values reported in Table 80a and b for the "Interlevel metal insulator (minimum expected)—bulk dielectric constant" and "Interlevel metal insulator—effective dielectric constant" have been derived from a generic electrical simulation model for three mainstream integration schemes with parameters specific to years defined in this current roadmap. The methodology used by this working team consisted of employing a standard simulation model and incorporating the most "realistic" parameters for Cu cap, hardmask, trench ILD, via ILD, and geometries specific to each year detailed in this roadmap. A second simulation was performed which incorporated the most "aggressive" parameters for Cu cap, hardmask, trench ILD, and via ILD with consistent geometries specific to the year incorporated in this roadmap. The range reported for the "Interlevel metal insulator—effective dielectric constant" represents the highest value calculated using the realistic parameters within the three integration schemes simulated and the lowest value calculated using the aggressive parameters within the same three integration schemes. The "Interlevel metal insulator (minimum expected)—bulk dielectric constant" reported for each year represents the most aggressive ILD material parameter used in the realistic case. The value is reported as ≤ to acknowledge that some IC companies may choose a more aggressive low-κ ILD material, below this value, but choose a more conservative integration scheme that delivers a higher effective dielectric constant than the minimum value reported in the "Interlevel metal insulator—effective dielectric constant" range.

Many electrical simulation models exist to extrapolate the effective κ values from well-controlled test structures within a die. Figures A1-A3 in the Dielectric Appendix show simulated effective κ results for representative low-κ integration schemes for the current and next two technology generations (90, 65, 45 nm). The model inputs are specific to the ITRS 2005 targets for layer thickness, aspect ratios and dielectric materials projected to be commercially available concurrent with proposed manufacturing ramp timings. Three values of effective κ are indicated corresponding to their integration schemes for each technology generation. The logical basis of κ-value derivation is clarified in this roadmap and appropriate interconnect parameters are presented based on a logical model as shown in Figure A4. The critical path is assumed to consist of typical circuits such as 2NAND+Inverter connected with average long intermediate wires having multiple-stages and long intermediate/global wires. Both long intermediate and global wires are divided by optimized repeaters in order to reduce RC delays, and long global wires have reverse-scaled width and thickness. The model assumption is summarized in Table A1. Under the assumption, scaling of both wiring resistance and capacitance should be completely implemented so as to reduce the delay time of high-end SOC by 30% per technology generation. The effective κ scaling curve calculated by this theoretical approach is shown compared with the above effective κ simulation extraction results in Figure A5. These figures are in good agreement with each other.

PRE-METAL DIELECTRIC (PMD)

Improvements or changes in the technology used to deposit pre-metal dielectric (PMD) layers have advanced since the last roadmap. These changes are driven by the move to NiSi, increases in the aspect ratios of spaces between adjacent gates in DRAMs, and the simultaneous requirement for high phosphorous doping concentrations and low thermal budgets in NOR-type flash memories. The increasing use of NiSi doped junctions and gate conductors in logic circuits will challenge those deposition technologies, which require anneals in the 450ºC to 490ºC range. Thermal budget restrictions will also accompany the introduction of metal gates; however, these continue to fall within the same range dictated by NiSi. This problem is intensified when high phosphorous doping concentrations are also required. Some NOR-type flash memories already incorporate NiSi while requiring PMD phosphorous concentrations as high as 10% to meet charge retention requirements. The aspect ratios of the spaces between adjacent gates in DRAMs are expected to reach 16:1 by 2005 and will increase thereafter. As a result, DRAM PMD deposition by plasma-based processes could become increasingly problematic. Plasma induced damage (PID) of thin gate dielectrics by plasma based PMD deposition processes continue to be insignificant. However, it could become an area of concern as gate dielectrics become thinner and/or are replaced by new high κ materials. Finally, low-κ dielectrics will be required for DRAMs for the layer incorporating bit lines to reduce capacitance. For example, κ_{eff} values ranging from 2.7 to 3.1 will be required by 2010, decreasing to 2.3 to 2.6 by 2020. It is conceivable that future PMD deposition processes will incorporate multiple steps, and possibly multiple process types, to satisfy the requirements of gap fill, thermal budget and doping concentration. Combinations of spin-on and plasma deposition, are already being reported at the technical conferences with manufacturing introductions planned in a few years.

INTRA-METAL DIELECTRIC

Concurrent with low-κ materials introduction is a planned migration of metal barrier deposition technologies (PVD→CVD→ALD) as well as the continued reduction in barrier thickness to maintain the targeted Cu resistivity. The combination of these integration challenges, coupled with design improvements to alternately address projected crosstalk and RC delay problems, has postponed the industry-wide implementation of low-κ ILD material past that proposed in the last three ITRS documents.

The preferred integration scheme for silicon-based dielectric materials continues to be the original “full via first” process already implemented with silicon dioxide. Organic based dielectric materials have usually adopted a dual inorganic hardmask scheme. Both of these integration schemes provide a cost-effective manufacturing process and also yield the lowest κ_{eff}. The κ_{eff}, paramount to the design community, is the parameter indicative of the composite dielectric permittivity experienced by an electrical signal traveling along the Cu interconnects within a chip. Recently, there has been significant discussion about combining the inorganic and organic dielectric materials in a “hybrid” dielectric stack in an effort to optimize performance and minimize process integration complexity and challenges. Many electrical simulation models exist to extrapolate these values from well-controlled test structures within a die. In the figures in the Dielectric Appendix simulation extraction results for representative low-κ integration schemes are presented for several technology generations. The model inputs are specific to the ITRS targets for layer thickness, aspect ratios, and dielectric materials projected to be commercially available concurrent with future proposed manufacturing ramp timings. Extreme low-κ dielectrics ($\kappa < 2.0$) will be required after 2012. Novel integration schemes may be required, such as air gap architecture (hybrid dielectric stack utilizing air ($\kappa = 1.0$)).

Integration challenges associated with etch selectivity/damage, 193 nm photoresist, Cu CMP, and packaging process compatibility are still areas of significant effort across almost all low-κ dielectric materials. Physical, mechanical, and electrical properties and the relationships between them are not sufficient to predict integration success.. Therefore, a steep learning (reinventing) curve is in progress throughout the industry. The technical community still entertains a healthy debate about microstructure requirements for porous dielectric materials with respect to pore size, pore shape, aspect ratio, and degree of interconnectivity (open versus closed).

HARDMASK

Hardmask is a generic term used to describe the dielectric film deposited on top of the trench level intra-metal dielectric. It has two main functions: to assist in patterning of the dual damascene structure for subsequent metal fill and as a highly selective CMP stop layer. In addition, this layer is called upon to prevent fast diffusion of acid or base moieties that could interact detrimentally with the traditional acid-catalyzed photoresist systems employed at 248 nm and 193 nm. Depending on the efficiency of CMP and acid/base moiety inhibition, this layer could be either inconsequential to the overall κ_{eff} or a significant contributor. For most integration schemes, the composition of this layer can be chosen independently of most other dielectric layer choices. However, in the case of the hybrid integration scheme, the etch sequence is simplified if the hardmask dielectric material and the via layer dielectric material are similar. There are both spin-on and CVD deposited solutions available with dielectric constant values down to at least 3.0. Some spin-on offerings are available with a dielectric constant as low as 2.2.

ETCH STOP –VIA

The via etch stop layer also has two main functions. It must have adequate etch selectivity with respect to the via dielectric layer so that etching of the underlying IMD adjacent to non-landed vias is avoided. It also serves as the cap for the underlying Cu wiring layer. It must be a Cu diffusion barrier and have acceptable adhesion and interface properties so that Cu electromigration requirements are met. The via etch stop layer can also be a significant contributor to overall κ_{eff} so its thickness and κ value should both be minimized.

ETCH STOP –TRENCH

The primary function of the trench etch stop is to provide adequate etch selectivity, as compared to the trench level dielectric, to form a smooth well-defined trench bottom. Significant trench bottom roughness can be a reliability issue if it affects metal barrier coverage. Variability in trench depth can be a significant contributor to variation in metal line resistance. In alternate integration schemes, such as hybrid ILD structures, the need for discrete trench etch stop layers is eliminated because dielectrics with different etch characteristics are employed.

DRAM

DRAM technology has just begun the arduous process of implementing an assortment of medium dielectric constant materials ($5<\kappa<40$) in stacked capacitor structures. Trench-defined DRAM technology could possibly delay the implantation of these medium dielectric materials for an additional generation because of the enhanced active area available. Both DRAM technologies will develop an understanding of these medium dielectric constant materials as a stepping-stone to the higher κ (>40) alternatives. These high dielectric constant materials are most likely to be tried in stacked capacitor structures initially, followed by trench capacitor structures, before they are considered as replacements for silicon dioxide at the gate level.

DEPOSITION AND CURE TECHNOLOGIES

Deposition technology for the dielectric materials employed in the ILD stack have been historically based on plasma etch CVD (PECVD) with a small niche dedicated to spin-on. PECVD remains the dominant deposition technology, based on incumbency. There are some efforts to develop equipment that utilize supercritical CO_2 ($scCO_2$) as a solvent. The approximately zero surface tension associated with CO_2 at the triple point (solid-vapor-liquid coexist) offers solutions to gapfill of very high aspect ratio structures and compatibility with an apparent infinite number of dielectric surface energies.

There is renewed interest in cure technologies because of the potential promise to reduce the thermal budget of BEOL processing, both absolute temperature and time. Cure technologies are also being investigated as a means of improving mechanical properties of low and ultra-low-κ ILD materials in an effort to reduce processing concerns associated with CMP and packaging as well as thermal/mechanical cycle degradation. In addition, for ultra-low-κ ILD materials, removal

of the porogen after templating (of closed pores) has been enhanced by techniques other than just thermal energy. Investigations into the use of both broadband and wavelength-specific ultraviolet (UV) energy have been reported and continue to be developed. Electron-beam sources have been previously developed and are now being applied to dielectric materials to enhance mechanical properties, remove porogen materials, and improve adhesion between the many dielectric layers that now compose the ILD stack.

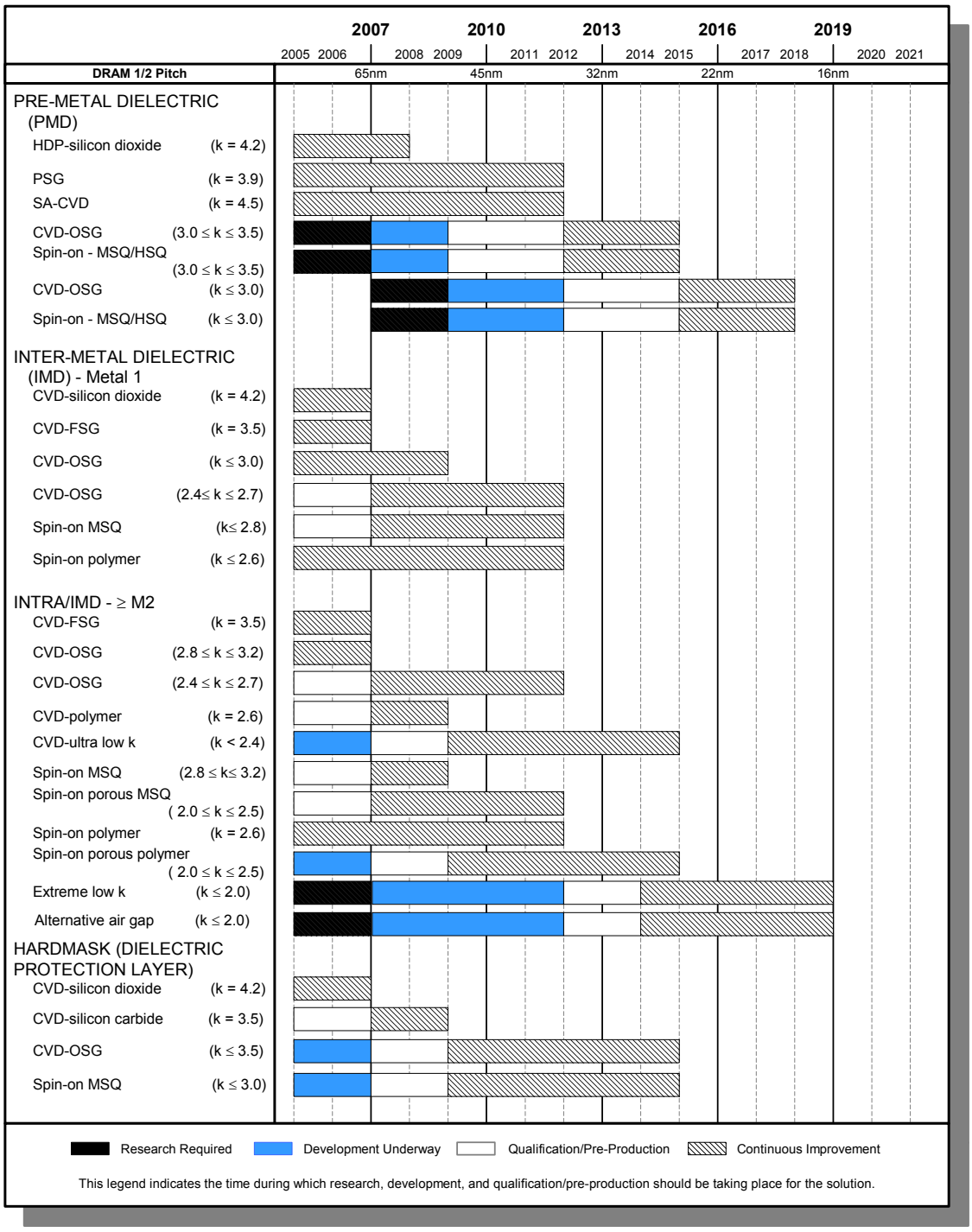


Figure 73 Dielectric Potential Solutions

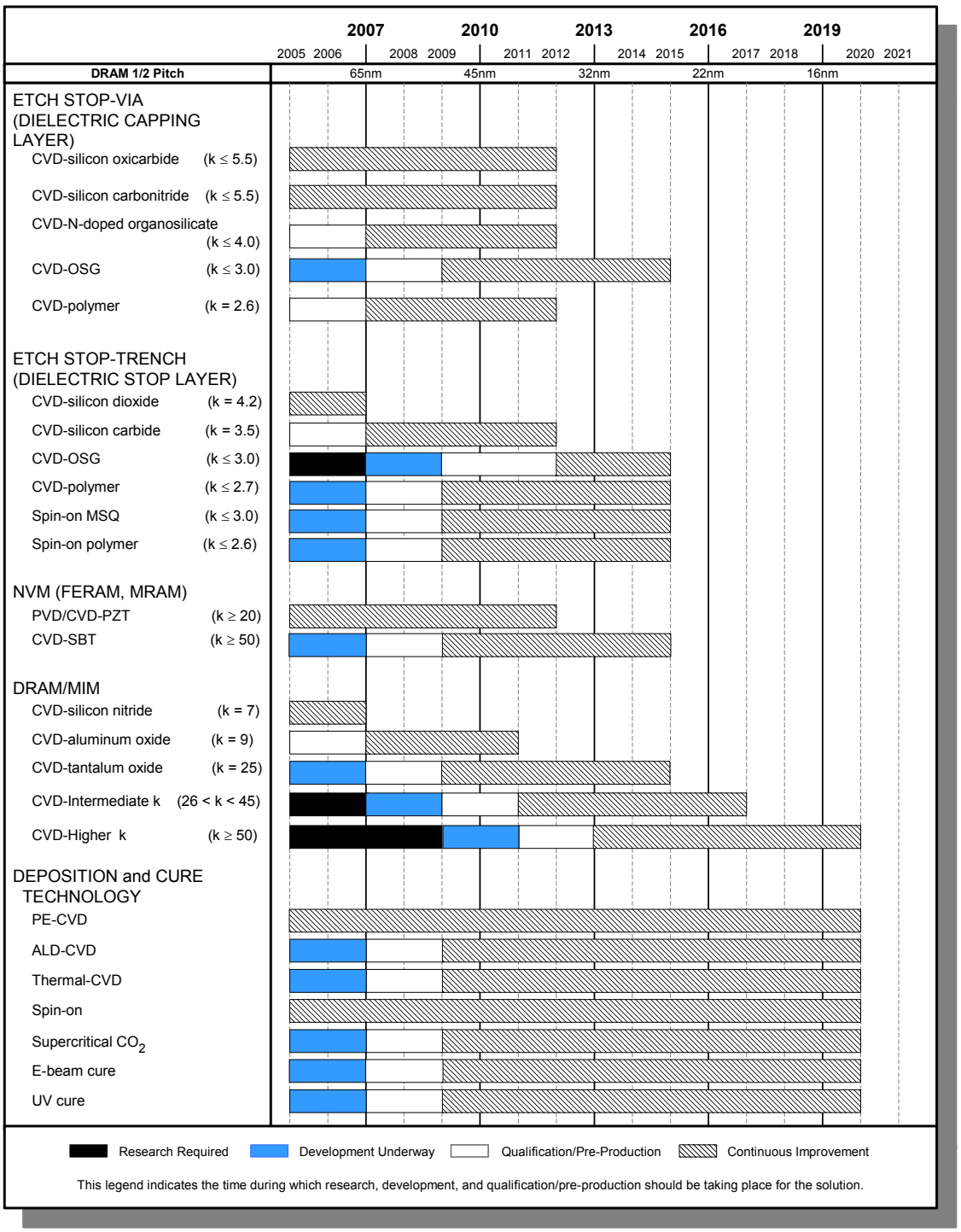


Figure 73 Dielectric Potential Solutions (continued)

BARRIER POTENTIAL SOLUTIONS

Barriers for tungsten local wiring and contact fill will continue to utilize Ti/TiN films in the near term (See Figure 74). There will be continuous improvement of established deposition techniques such as long throw and ionized PVD and CVD to improve compatibility with the new seamless W technology. Development of ALD Ti/TiN is underway and is likely to improve the overall seamless W fill process by eliminating the "pinch off" of the contact hole characteristic of other deposition techniques. CVD Ti/TiN barriers will continue to be improved for high aspect ratio contacts (for example, DRAM stacked capacitors) filled with W conductor. Migration to the ALD versions of these films will occur since W plug conductivity needs will dictate use of the thinnest possible barrier films. Conventional PVD and CVD barrier technologies will be continuously improved to allow Al fill to be extended to higher aspect ratio structures, however it is likely that ALD barriers will also replace these techniques in the future. Research is also underway to explore alternate materials and fill techniques for high aspect ratio contact structures that would allow simplification of the current contact/barrier/conductor film stack. Since one of the primary functions of the TiN barrier is prevention of the interaction of Ti with F from the WF_6 precursor, a change to non-fluorine containing tungsten precursors could allow for elimination of the barrier film entirely. Other materials such as Ru are being considered as replacements for W in contact plug applications.

Barrier materials used for Cu wiring must prevent its diffusion into the adjacent dielectric but in addition must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta has become the predominant industry solution but other nitrides and silicon nitrides and carbides of Ta, Ti, and W have also shown promise. Long throw, ionized PVD, and CVD depositions will continue to be improved to meet the very challenging sidewall coverage requirements of future dual damascene structures. However, even the most advanced of these deposition techniques tend to narrow the upper part of the dual damascene trench and limit the fill capability of the ECD Cu process. A great deal of effort is underway to develop ALD barriers that are expected to become the predominant future solution for copper. ALD TaN and WNC are furthest along in development but questions remain concerning their interface properties with Cu and whether adequate electromigration performance can be ensured. One potential solution to this issue is the use of a PVD Ta flash layer followed by PVD Cu to provide the required interface to ECD Cu. At this juncture, it appears that improvement in PVD barrier deposition techniques will allow their continued use for MPUs with 45 nm half pitch. ALD Ru appears to be compatible with direct plating of ECD Cu and also provides a good Cu interface, however its barrier properties are suspect. Two advanced potential solutions are ALD TaN/ALD Ru and ALD WNC/ALD Ru bi-layer barriers. One major obstacle to the adoption of ALD for barriers is penetration of the precursor materials into the porous low-κ dielectrics targeted for future technology generations. *In situ* modification of the etched low-κ sidewalls may be used either with ALD or as a standalone barrier solution to resolve this issue. Development is also underway to explore deposition of barriers by electroless techniques and from supercritical CO_2. Another focus area for metal barriers is the top surface of the Cu dual damascene structure. Plasma enhanced chemical vapor deposition (PECVD) dielectric Cu barriers such as Si_3N_4, SiCN, and SiC are predominately used for this application. Their disadvantages are degraded Cu electromigration properties and a rise in overall κ_{eff} of the structure because of their higher κ values. Their advantage is the minimal shorting risk between the ever-narrower wire spacing of future generations. Selective metal capping barriers such as W, CuSiN, or CoWP are being explored for this application and have demonstrated a large increase in Cu electromigration properties by improvement of the top Cu interface. The industry has been slow to adopt selective metal capping processes because of the risk of yield loss from metal shorts.

A great deal of research and development in the area of advanced barrier materials and deposition techniques will be needed, since engineering the smoothness and other properties of the Cu barrier interface will be key to ameliorating the expected Cu resistivity increase from electron scattering effects. Research and development is still in the early stages for the various proposed solutions to the global wiring problem. Appropriate barriers will need to be developed for all of these technologies.

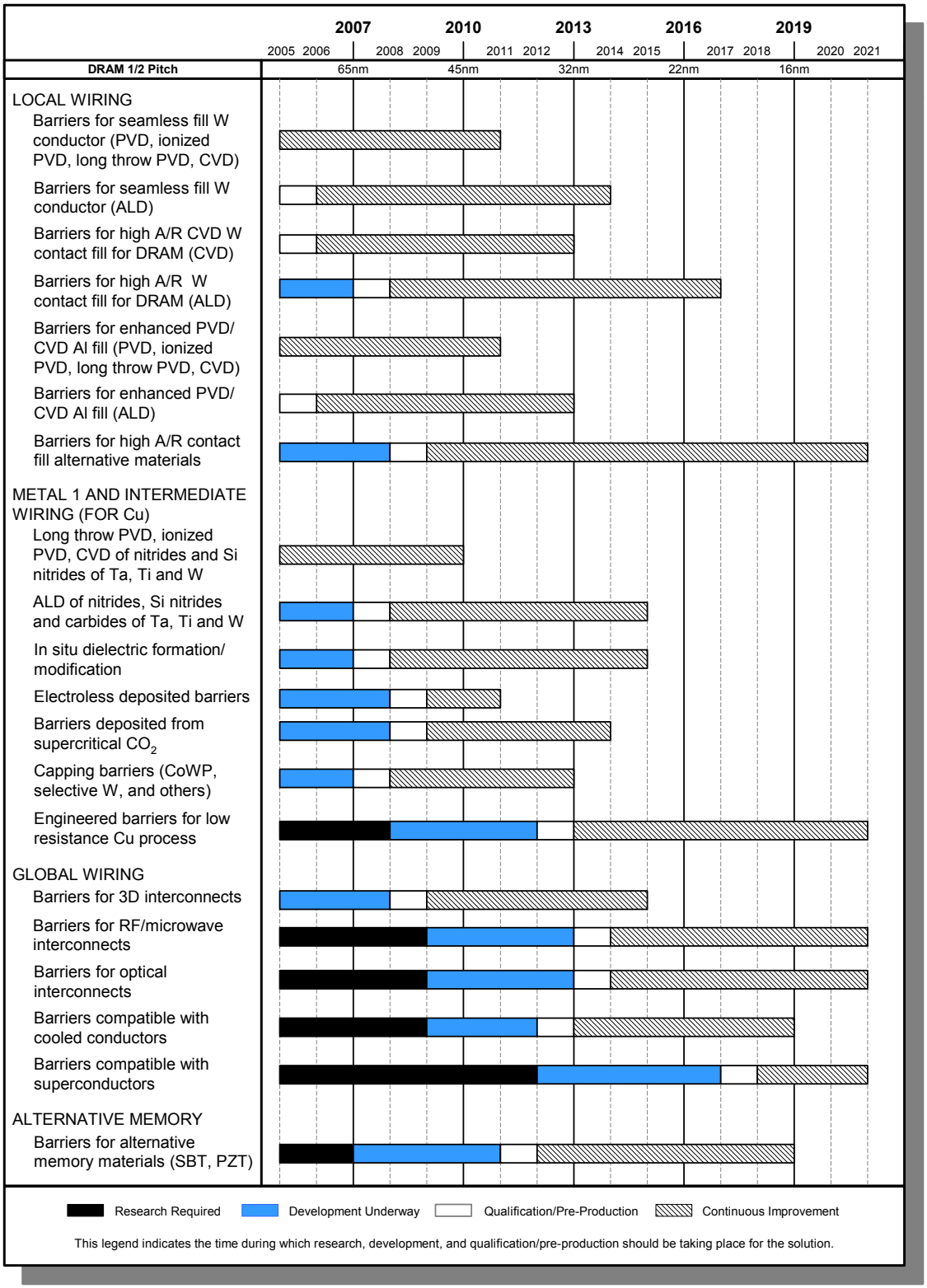


Figure 74 Barrier Potential Solutions

CONDUCTOR POTENTIAL SOLUTIONS

Local wiring, which is sometimes called metal zero, is limited to very short lengths and usually contacts adjacent transistors. Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, ASICs and DRAMs. ALD, in conjunction with CVD techniques, is being utilized first in the W deposition area to accomplish a seamless W fill. The absence of seams at the local wiring or contact level is especially important when the subsequent wiring level is ECD copper in order to avoid defect issues associated with retained plating solution. There is a problem associated with the standard silane nucleation step in the CVD W process in that this Si-rich film takes up an ever-larger portion of the plug and will result in unacceptably high resistance for future technology generations. Refer to Figure 75. Modification of the process to minimize or eliminate this layer is an area of focus. Alternative materials such as Ru, deposited by ALD, are also being investigated. Continued development of ALD tungsten deposition will be needed to accomplish W fill of high aspect ratio (17:1 in 2009) contacts for stacked capacitor DRAM designs. Alternate materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts, which are projected to have aspect ratios greater than 20:1 by 2010. Aluminum may continue to be used for local wiring and enhanced CVD/PVD flow techniques will continue to be improved for damascene architectures.

Cu will be the preferred solution for the Metal 1 and intermediate wiring levels in MPUs and ASICs and electrochemical deposition will continue to dominate the market in the near term. There will be continuous improvement in the plating chemistry and ECD tool design to allow seamless fill of smaller geometry higher A/R structures. Development is also underway to accomplish both deposition and planarization in a single tool by combining ECD with CMP, a form of chemically enhanced planarization (CEP). CVD Cu may become competitive as a fill technology if the same "superfilling" behavior and microstructure characteristic of ECD can be achieved. Alternatively combinations of CVD and PVD Cu may be employed to accomplish seamless fill at smaller geometries. Deposition of Cu and other conductors from supercritical CO_2 solutions is still in the research phase but is also a promising technology. Minimum feature size Metal 1 and intermediate Cu wiring in MPUs and ASICs is already experiencing a resistivity increase due to electron scattering. The line lengths of these wiring levels tend to scale with technology generation so the impact to performance is minimal.

Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. The resistivity of the smallest pitch global wiring level is expected to increase about 40% by the end of this decade. This is more problematic, since global wiring traverses longer lengths and is more likely to impact performance than Metal 1 and intermediate wiring. Cu interfaces, microstructures and impurity levels will need to be engineered to alleviate the impact of this resistivity rise. MPUs use a hierarchical wiring approach in which the pitch and thickness of the global wires are increased at each level. Indeed the final global wiring level is little changed from one generation to the next and so will not be affected by electron scattering effects.

Other design alternatives are the use of repeaters or oversized drivers, both of which impact chip size and power. The most likely near-term solutions are judicious use of design and signaling options, packaging, or 3D ICs to minimize the effect of the narrower more resistive global wires. A great deal of research is also underway on the use of either RF or optical techniques to resolve this issue. More radical solutions include cooled conductors, superconductors, nanotubes etc. All of the above global wiring alternatives are discussed in greater detail in the new concepts section of the Interconnect roadmap.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of MIM capacitors to improve yield and reliability. Both Al and Cu are currently in use for standard spiral inductors, but in the future various magnetic materials may emerge with different inductor designs to reduce the area of these devices.

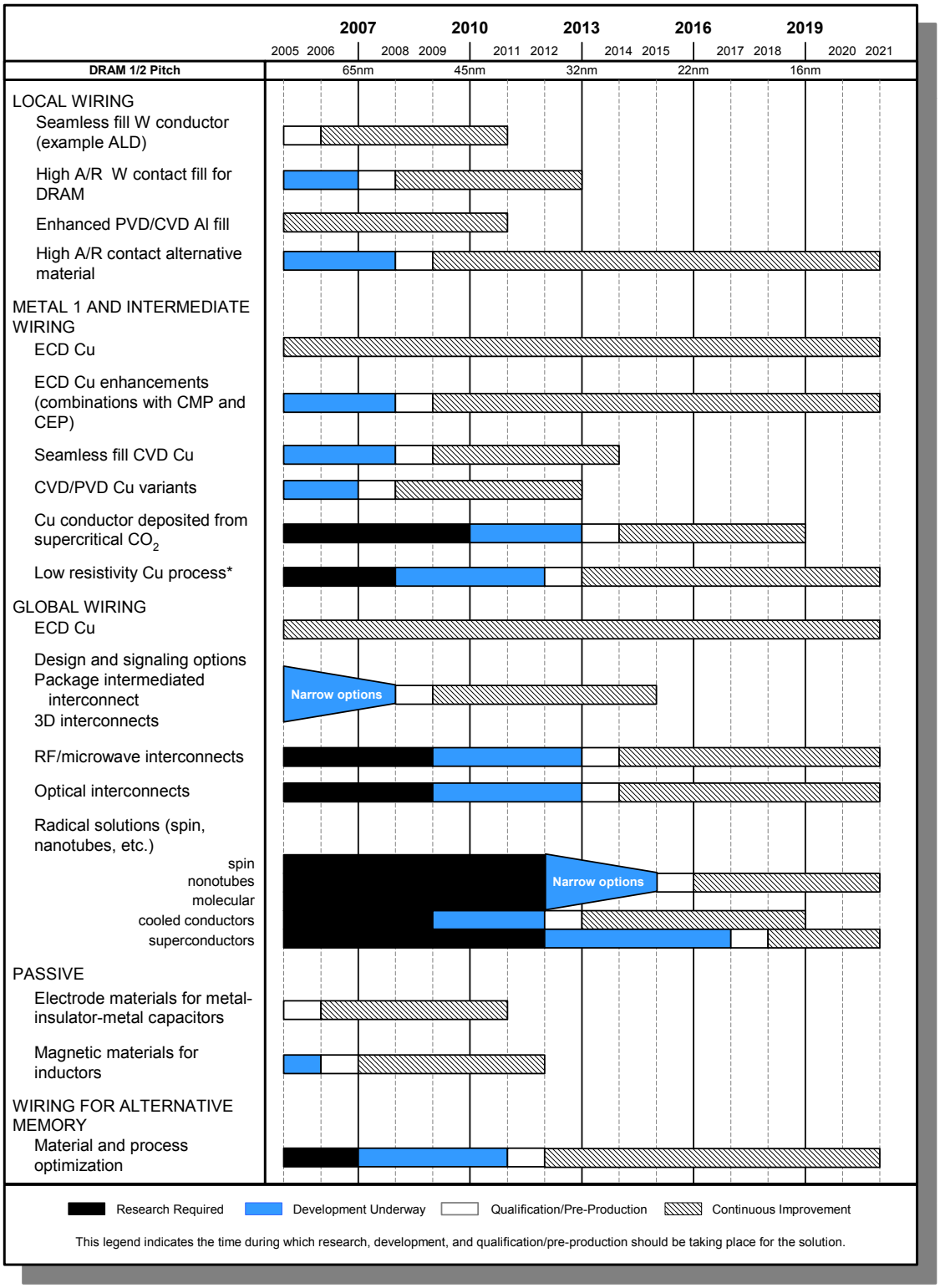


Figure 75 Conductor Potential Solutions

NUCLEATION POTENTIAL SOLUTIONS

The conformality and coverage of the nucleation layer is often the critical factor in determining whether the subsequent conductor deposition will be seamless or free of voids. For local wiring and contact fill, there will be continued improvement in ALD W nucleation layers that have been used to enable seamless or high aspect ratio W fill. In addition,

these ALD nucleation layers must be either extremely thin or have very low resistivity, so that the overall conductivity of the plug is not affected. In the area of Al fill, the CVD Al nucleation layer may be extended to ALD to allow continuous improvement in the fill characteristics of this technology. Refer to Figure 76. Development is still underway for alternative materials and processes for high aspect ratio DRAM contacts but ALD nucleation layers will likely be needed for this technology. For Metal 1, intermediate and global wiring, enhanced PVD Cu deposited through either long throw or various ionized techniques continues to be the dominant nucleation layer for ECD Cu. There has been improvement in the sidewall coverage and uniformity of these layers that will allow their use at the tightest dimensions of the 65 nm and potentially 45 nm technology. In addition, PVD Cu nucleation layers will continue to be used on the global wiring levels with larger critical dimensions. Eventually, these enhanced PVD techniques will not be able to provide reliable nucleation layers at the M1 and intermediate wiring levels and they will be replaced by ALD technology. There continues to be research on several nucleation layer options including electroless, ALD, and supercritical CO_2 technology. Although ALD Ru seems to be only a marginal barrier to Cu diffusion, it does appear to be a very good nucleation layer for ECD Cu. Therefore it may be used in conjunction with other barriers, such as either ALD TaN or ALD WNC. Another potential solution to the problem of marginal PVD Cu sidewall coverage is repair of the nucleation layer through ECD techniques. A more elegant solution to the problem involves modification of the ECD process and/or barrier to be self-nucleating, thereby eliminating the need for a Cu nucleation layer.

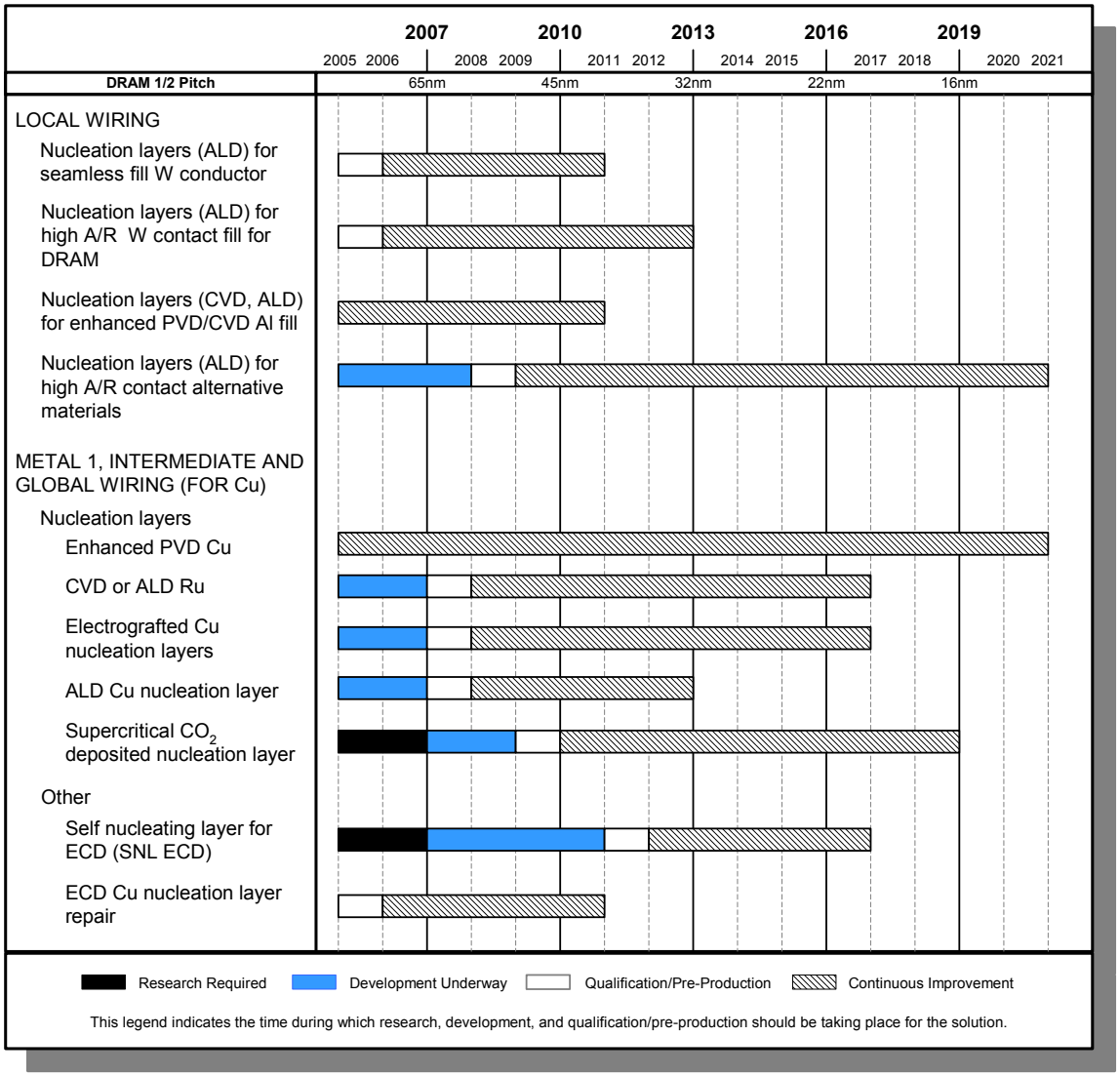


Figure 76 Nucleation Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Planarization is an integral part of the process flows for advanced interconnect systems. Chemical mechanical polishing and near alternatives remain the leading planarization technologies of interest. New materials, structures, and reduced CDs will be required for future generations and with them the potential need for unique planarization process solutions. Each application shares a common theme of deposition and then removal of sacrificial material to produce the desired surface.

The initial section of the planarization potential solutions chart, Figure 77, details a timeline for the major planarization applications. This timeline serves as a preface to the potential solutions described in the Equipment and Consumables sections that follow. The applications are categorized as dielectrics or conductors.

Although shallow trench isolation (STI) is not part of the interconnect structure, it is included for completeness. Direct planarization (without additional steps to reduce bulk film to be removed) is the standard for today's processes. The need for STI may be reduced in future technology generations as new raised transistor structures are implemented that can be isolated using the pre-metal dielectric (PMD) film. The current PMD planarization step is being used with both a target method (stopping in the bulk film at a target thickness) and a selective method (stopping on an underlying film). The use of more selective PMD steps will be driven in logic technologies by new front end of the line (FEOL) structures. The evolution of new planarization applications is a certainty; however, planning for them is difficult. These new conductor and dielectric applications are expected to be needed at 45 nm and may include FEOL processes, planarization of nitride films, removal of new materials for non-volatile memory (NVM) cells, polishing photoresist, and other processes.

Polysilicon (poly) films are conductors, but they planarize similarly to dielectric films. Traditional poly planarization stops with high selectivity on a range of underlying dielectric films; however, lower selectivity options are now needed as well. Planarity of poly features has also become more important, especially for the production of Flash memory. The use of tungsten at the contact level and as a niche for local interconnects should continue well into the future.

Achieving the performance required for copper and its barrier is regarded as the largest challenge ahead for planarization processes. Polishing of copper with tantalum-based barriers on standard dielectrics is a mainstream activity today. Copper and barrier planarization is faced with many challenges over time. The impact of excess removal of metal during planarization on the variation of wire resistivity is well documented. The effect of planarization on electron scattering in narrow Cu wires is not well understood. In addition, the dielectrics between metal lines are increasingly fragile and prone to liquid absorption as well as delamination. Factories are also faced with a variety of dielectric films across the process levels within a technology generation. The adoption of ALD technology for barriers will result in more conformal depositions that will dramatically reduce the amount of barrier material that can be used as a CMP stop during copper planarization. The choice of materials used for the barrier will also change over time. New conductor planarization applications will also be required. Planarization of noble metals for memory capacitors has been delayed, but is still likely. The need for planarization for metal gates is possible as materials and integration schemes are decided. Interest in aluminum damascene wiring has also resurfaced. A variety of metals and alloys are being utilized in NVM chips.

Development will continue in equipment. Integrated wafer buffing and cleaning are standard on polishing equipment and will need to be able to handle tailored solutions. Post-CMP wafer cleaning will likely become more closely integrated with the planarization process. In the future, cleaning solutions will be increasingly tailored to the planarization application that they follow. This customized cleaning approach results from the presence of unique combinations of chemistries, particles, and films present. The mechanical energy for cleaning will continue to be applied by buff pads, brushes, and contact-less methods. Various polish endpoint detection techniques are used today, with inline film thickness metrology as an available option. Next generation tools may include a range of inline metrology to measure forces, temperatures, planarity, and defectivity and also allow for automatic process control (APC). Equipment, especially for copper and barrier, will need to operate at low downforce levels in order to minimize the stress applied to fragile films. The stress will have to be radially tunable in order to achieve excellent non-uniformities in removal rate and recess.

Development of alternative planarization techniques is gaining in importance. These include options such as chemically enhanced planarization, (chemical or non-electrochemical mechanical polishing, and press planarization. These alternatives may offer advantages for productivity or film loss, but are especially needed for reaching the very low sheer stresses that will be required.

Consumables are the largest contributor to many planarization performance metrics, so significant advances will be required. High solids slurries utilized today are being driven to increased consistency, especially in defectivity. Development of slurries with low or no solids is critical to the simultaneous achievement of improved productivity with

better planarity and defectivity. Novel chemistries will help defray the productivity loss associated with decreasing pressures. The abrasives used will have to be engineered to fit their applications. Significant advances will also be needed from both hard and soft pads, usually made with urethanes, and used across the applications. Pads that contain abrasives are a niche market today. There is a strong need for development of a wide range of pad types that can be paired with slurries by application. Technologies need to be developed that can simultaneously offer consistent performance in planarity, defectivity and productivity. To respond to large numbers of planarization applications and different integration schemes for each, formulations will be increasingly optimized from tunable platforms to offer unique performance. Many of the alternative planarization techniques will need robust manufacturing-ready fluids in order to enable the technique.

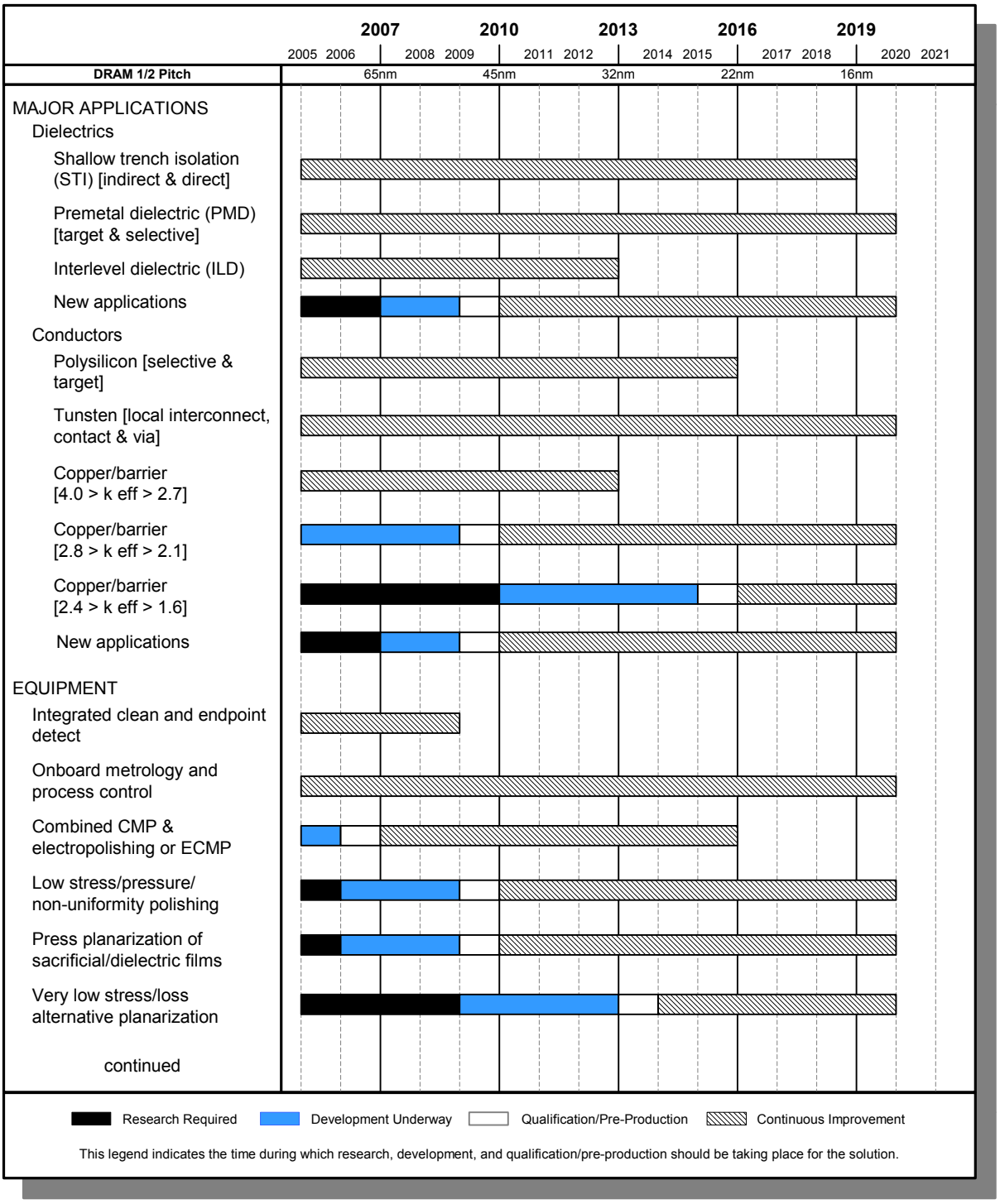


Figure 77 Planarization Potential Solutions

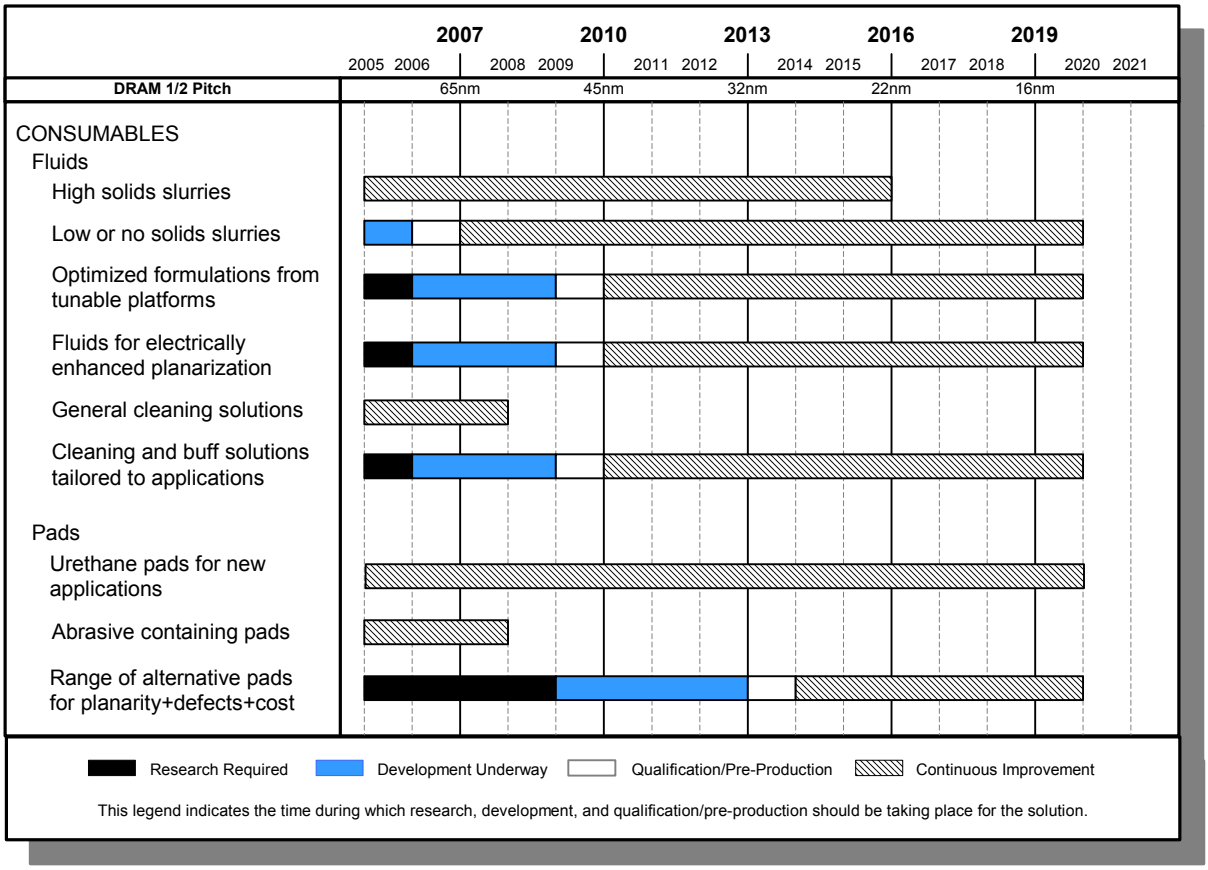


Figure 77 Planarization Potential Solutions (continued)

ETCH POTENTIAL SOLUTIONS

Future BEOL etch technology development will continue to address an array of conductor and dielectric materials. Dielectric etch challenges will be dominant in logic technology where a variety of inorganic, organic, or hybrid materials will be used to meet κ_{eff} requirements. Refer to Figure 78. Combinations of these materials will also be employed to take advantage of material dependant etch selectivities. Continual refinement of current capacitively coupled source technology is expected to be able to adequately address the materials challenges as well as shrinking trench and via dimensions at nearly constant aspect ratios. Future logic technology will require the introduction of progressively higher dielectric constant materials to offset cell area reductions. Refractory metal barriers will also be required in the case of FeRAM. Source technology development must deal with the low volatility of the etch products from these materials. The already high aspect ratios of contacts in memory technology will continue to increase. However, it is anticipated that current source technology will address future needs with continued refinement.

It now appears that Al alloys will continue to be used as conductors down to 25 nm half pitch in some memory technologies. Continued refinement of current inductively coupled source technology should continue to be adequate. The processes currently used for refractory metal electrodes such as Pt and Ir as well as those used for ferroelectric materials have high sputter components. Unacceptable leakage can result from the re-deposition of etch products on capacitor sidewalls. New etch chemistries that produce higher volatility products are desirable. Nonetheless, source cathode/chuck designs capable of operating at 500ºC might be required. Current Si deep trench etch technology is expected to meet future challenges with continuous refinement.

Capacitively coupled source technology will continue to be used to etch Cu dual damascene dielectric stacks. However, technical challenges will continue to mount. First, reductions in photoresist thickness needed to achieve smaller feature sizes will require higher etch selectivity to photoresist. Though the trench first dual damascene scheme is currently dominant, it might require augmentation with hardmask schemes to deal with this issue. Alternatively, where etch

selectivity is even inadequate for hardmasks, tri-layer resist approaches might be necessary. Etch chemistries and processes that reduce sidewall roughness are also required.

Shrinking dimensions and the introduction of porous ULK dielectric materials will further challenge both etch and strip processes. Trench sidewall damage caused by current processes will be unacceptable at future technology nodes. A constant depth of damaged sidewall material will comprise a larger fraction of the dielectric materials between adjacent Cu lines, raising the κ_{eff}. Porous ULK dielectric materials are more easily damaged to a greater depth. Etch processes that cause less carbon depletion from hybrid organic-inorganic dielectric materials will be required.

Damage free photoresist and residue removal would be facilitated by the development of etch processes that produce less deposited residue and/or re-deposited sputtered material, such as Cu sputtered during etch stop open. Low damage photoresist and residue removal is facilitated by source technology that provides more directionality than is available from conventional high-pressure strip systems. Additional damage repair and/or pore sealing steps might be required for porous ULK dielectric etching. These requirements might force the expansion of etch or strip tools into multi-station systems. Problems such as moisture absorption or the reaction of moisture with damaged dielectrics could require *in situ* process flows that include etch, dry strip, wet strip, damage repair, degas and pore sealing steps. Ultimately, etch or strip tools could come to resemble PVD cluster platforms. Such platforms might also facilitate other processes where a mixed variety of materials are present or where exposure of a form of residue to the atmosphere would make it more difficult to remove. The extendibility of plasma-based dry strip technology is a concern. It might be necessary to replace it with alternative technologies at very advanced technology nodes.

3D IC stacking technologies require etching vias through the entire depth of a wafer. Such etch processes have been demonstrated using current capacitively coupled source technology. This technology, with continuous improvement, is expected to be able to meet future requirements. Through wafer via etching removes relatively large amounts of material per wafer. Consequently, high atomic weight inert gases are being investigated as a means to accelerate etch rates. Reactor availability is also affected by the large amounts of etched materials. More effective means of reducing reactor down time will have to be investigated for high volume manufacturing.

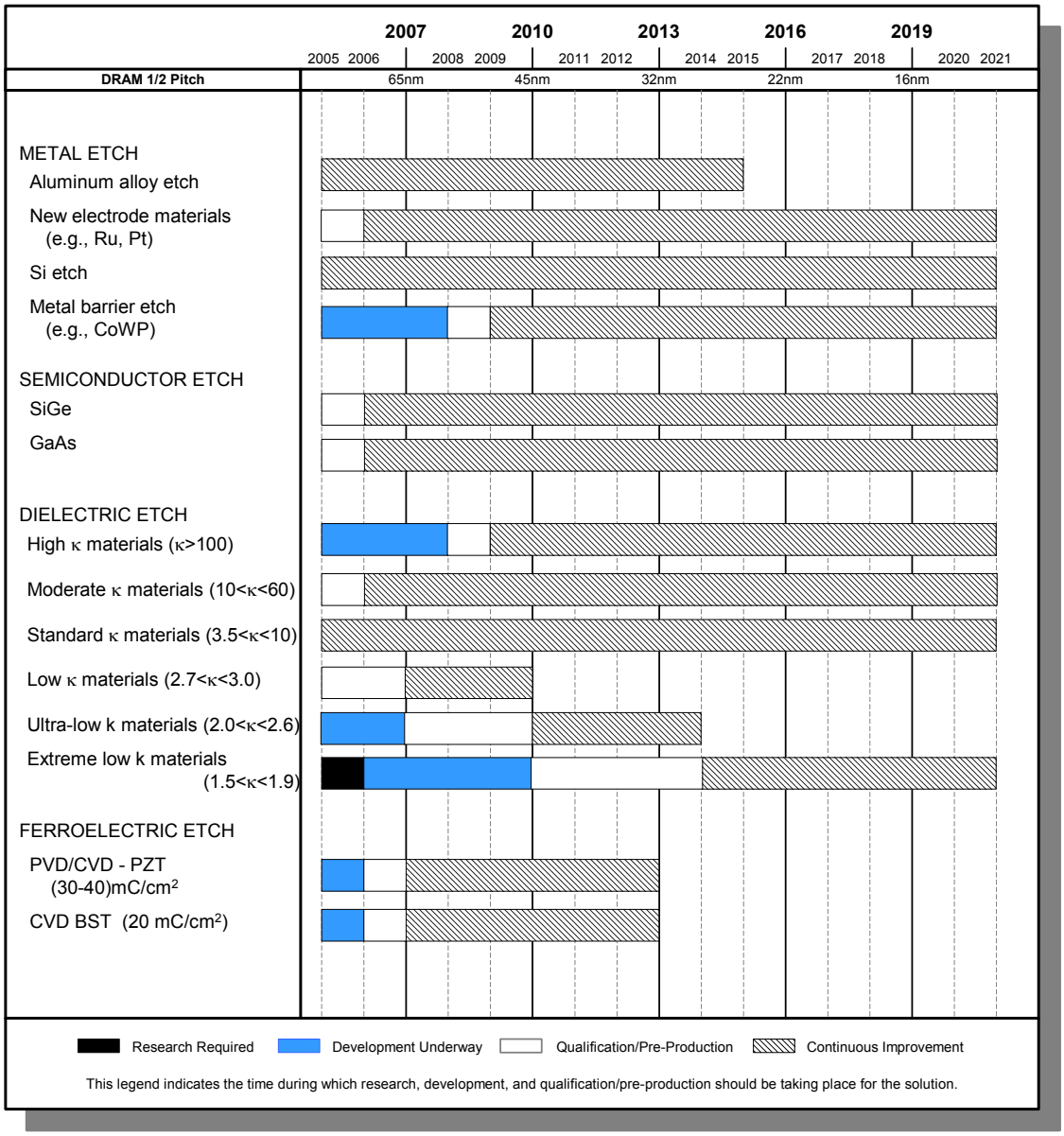


Figure 78 Etch Potential Solutions

INTERCONNECT SURFACE PREPARATION

Interconnect structures based on copper and ultra low-κ materials continue to present difficult surface conditioning challenges. Additionally, high aspect ratio structures for contacts and capacitors increase the cleaning and surface conditioning challenges. Interconnect surface preparation includes post-etch photoresist stripping, post-strip residue removal, post-CMP cleaning for dielectrics and metals, pre-deposition cleaning for dielectrics and metals and post-deposition cleaning for dielectrics and metals. New requirements for surface preparation include improving interfacial adhesion, improving dielectric and barrier reliability, repairing etch damage and sealing pores in dielectric sidewalls. The main focus in Tables 82a and b is dual damascene processing involving copper metal and low dielectric constant insulators. Interconnect necessarily involves several other metallic films as barriers and seed layers as well as silicon oxide and silicon nitride dielectric films as etch stops and hardmasks.

Wet cleaning, plasma cleaning, UV/laser cleaning, and other dry cleaning methods, such as supercritical fluids and cryogenic aerosols are all being considered as potential solutions. No one technique or technology has solved all the

technical challenges for surface conditioning. For example, plasma stripping is cost-effective for removing photoresist and residue, but is unable to remove metallic contamination. Wet cleaning is effective for removing metallic contamination, but drying of high aspect ratio features has proven challenging.

Although surface conditioning is generally considered as a separate, stand-alone process, it has been incorporated into other process tools where a technical advantage is achieved, such as CMP. The combination of various surface-conditioning methods has proven successful for cleaning the wafer surface. For example, a typical post-etch cleaning sequence for the trench step of dual damascene and then the subsequent dielectric barrier removal includes the trench etch, an *in situ* post-etch photoresist strip and dielectric barrier removal all in one etch/clean cluster. For porous low-κ materials, an additional damage repair and pore sealing processes may be included *in situ*, to limit increases in κ_{eff} and to prevent penetration of the barrier metal into the porous low-κ dielectric.

Both logic and DRAM devices have cleaning challenges. As DRAM manufacturing migrates to copper interconnect, the same surface conditioning issues that logic faces need to be addressed. Additionally, high aspect ratio features such as contacts and cylindrical capacitors are difficult to clean and to dry. The front surface, back surface, and edge of the wafer must be effectively cleaned of particles, metallic and organic contamination. The surface must not be roughened and the materials must not be affected.

Challenges and potential solutions for interconnect surface preparation are primarily based on copper and low- κ integration schemes. Refer to Figure 79. For the near term, the low-κ dielectrics will be dense or nano-porous materials. For these materials, sidewall damage that may occur during etch, resist strip and clean can have a major impact on the effective κ-value of the dielectric, as well as the reliability and yield. Cleaning (residue and particle removal) on extremely hydrophobic, high aspect ratio structures, presents unique challenges. Copper films must be cleaned without corrosion, especially around the barrier-copper interface, and the final surface must assure electrical contact by being free of thick oxide layers. Copper from the edges and backside of the wafer must be cleaned to prevent undesirable migration of the copper to the transistor.

Meso-porous low-κ dielectrics—which are expected to be integrated by 2012—present extreme surface preparation challenges. The large pore density of these materials allow etch and surface preparation chemistries/plasmas to penetrate deeply into the dielectric. This can result in deep, sub-surface damage with subsequent increases in the dielectric constant, decreased dielectric breakdown, dielectric voiding, and reduced reliability. Porous, carbon-containing ultra-low-κ dielectrics integration may prove especially difficult. Surface preparation and cleaning techniques being investigated for this generation may extend beyond wet and plasma cleaning to supercritical fluids, cryogenic aerosols, and laser cleaning. Advanced wet, plasma, and thermally activated techniques are believed to be extendable into the future, as improvements to these technologies are expected. Sealing of surface pores may be needed to enable use of thin ALD barriers and prevent barrier penetration into the dielectric. Several wet and dry techniques are being investigated.

Wet cleaning will continue to be the method of choice for post-CMP, post-strip, and pre-deposition cleaning for at least the foreseeable future. Cleaning of copper and low-κ dielectric materials can be accomplished by wet methods or wet plus dry combinations. Dilute acid-based formulations with additions of fluorine-based chemicals, surfactants, chelating agents, and/or corrosion inhibiting agents will be used. Other advanced wet cleaning techniques, such as the use of dilute solutions of ozone, supercritical fluids or other unique approaches are still in the research stage and may be used should the conventional techniques fail to deliver adequate performance.

Carbon-containing low-κ dielectric films present the problem of a hydrophobic surface, which is difficult to rinse and dry without creating watermarks or leaving undesirable surfactant residue. This challenge might be addressed with front end surface preparation techniques such as surface tension drying or may drive the introduction of new processes such as supercritical CO_2 or the introduction of new chemicals that can replace 2-propanol. In addition, shrinking critical dimensions are creating more fragile structures and will require cleaning processes that are damage-free.

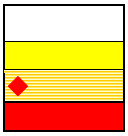
Particle removal is becoming more important as geometries continue to shrink. Backside, edge, and front side particle removal must be accomplished to successfully clean a wafer. New methods being investigated include the extension of megasonics, brush, and other physical methods that minimize wafer damage. Edge and backside particles are known to cause yield degradation, however, quantification is difficult. New tools are being developed that can measure the particles on the edge and backside, and will allow correlation to the yield impact.

Cleaning processes and chemical formulations will address environmental, health, and safety issues by using less concentrated, less hazardous, and more environmentally friendly chemicals. Fluorine-based chemicals and chelating agents in particular have disposal issues. Reducing the use of water is also a goal.

Table 82a Interconnect Surface Preparation Technology Requirements—Near-term Years*

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*D ½*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*M*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particles										
Killer defect density, D_pR_p (#/cm^2) [A]	**0.028**	**0.019**	**0.023**	**0.016**	**0.02**	**0.025**	**0.016**	**0.02**	**0.025**	
Critical particle diameter, d_c (nm) [B]	**40**	**35**	**32.5**	**28.5**	**25**	**22.5**	**20**	**17.5**	**16**	
Critical particle density, D_{pw} (#/wafer) [C]	**97**	**64**	**80**	**54**	**68**	**86**	**123.3**	**155**	**195**	
Back surface particles										
Back surface critical particle diameter (nm) [D]	**0.2**	**0.16**	**0.16**	**0.16**	**0.14**	**0.14**	**0.14**	**0.14**	**NA**	
Back surface critical particle density (#/wafer) [E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	
Edge bevel particles										
Edge bevel critical particle diameter (nm) [F]	**160**	**140**	**130**	**114**	**100**	**90**	**80**	**70**	**64**	
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Metallic Contamination										
Critical front surface metals (10^9 atoms/cm^2) (H)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**1000**	**1000**	**500**	**500**	**500**	**250**	**250**	**250**	**100**	
Mobile ions (10^{10} atoms/cm^2) [J]	**5**	**5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	**2.4**	
Organic contamination (10^{13} C atoms/cm^2) [K]	**1.4**	**1.3**	**1.2**	**1**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	
Cleaning Effects on Dielectric Material										
Maximum dielectric constant increase due to Etch, Strip + Clean [L]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	
Maximum dielectric constant increase due to rework [L]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**	
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



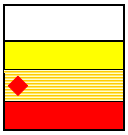
Notes for Tables 82a and b:
*[A] Killer defect density is calculated from the formula for 99% yield, Y=0.99=exp[-DpRpAeff]. Aeff is the effective chip area, Dp is the defect density, and Rp is a defect kill factor indicating the probability that a given defect will kill the device. The product DpRp is the density of device-killing defects on the wafer. Rp is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, Rp was assumed to be 0.2 for any particle > the critical particle size, dc. Aeff is assumed to be the same as for Front End Surface Preparation. For DRAM, Aeff=2.5F2T+(1-aF2T/Achip)*0.6Achip. where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and Achip is the DRAM chip size. For MPUs, Aeff=aT(GL)2, where GL is the gate length. Because Aeff can increase or decrease with each successive technology generation, DpRp does not always decrease over time.*
[B] Critical particle diameter, dc, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.
*[C] An example is provided which assumes that the kill factor, Rp, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using [Rp*3.14159*(wafer radius-edge exclusion)2]. To convert from particles/wafer at the critical particle size to particles/wafer at an alternative size, a suggested conversion formula is: Dalternate=Dcritical*(dcritical/ dalternate)2.*
[D] & [E] Metrics for Backside particle critical diameter and count have been taken from the requirements from table from the FEOL surface preparation document.
[F] & [G] Edge bevel critical particle size is taken as 2 DRAM ½ Pitch. The size was determined to be particles that could be shed and then distributed onto the wafer surface causing detrimental yield reduction. Few references exist correlating edge defects with yield, however, minimization of the particle size and density is important. The levels are still under evaluation, however, and no values are presented here, although current practices indicate edge bevel particle adders for any interconnect process step, in particular CMP, should be less than 4 defects per quadrant of the wafer. Again, this value should be treated as guidance, not a specification.*
[H] Front surface metallic contamination levels are based on degradation of yield from metallic diffusion into the transistor or leakage of the device from metal migration. Data shows that Cu levels <1E13 can cause interconnect leakage and <1E10 can cause transistor degradation. The ability of the Cu to diffuse into the dielectric and then through the silicon to the transistors is questionable as many references site the fact that Cu cannot diffuse though thick silicon, nevertheless, the lower the Cu contamination the better. The levels are still under evaluation, however, and the values presented here should be treated as guidance, not a specification.
[I] Back surface Cu contamination levels are based on degradation of electrical parameters of the transistor caused by Cu diffusion through the silicon. Many studies have been undertaken that evaluate the effects of backside Cu contamination on the transistors. The most profound affect is TDDB due to electric field drift. Oxygen on the back surface prevents the diffusion into the silicon. However, once in the silicon the Cu will diffuse and precipitate, dependent on thermal treatments. Various references quote a concentration as high as 1E15 and others quote as low as 1E11 as degrading device performance, dependent on test device structures and film thicknesses. Again, the levels are still under evaluation and the values presented here should be treated as guidance, not a specification. Reference: A. A. Isrtatov and E. R. Weber, J. Electrochem. Soc. 149(1) G21(2002).
[J] Mobile ions for interconnect are less stringent than the front end line metrics. Although the mobile ions can lead to the same electrical degradation and do the same damage from migration through the dielectric, the oxide does getter some of the sodium. For backside contamination levels, use the front end values. For interconnect, the causes shown here are guidance as to allowable levels, approximately twice the value of the front end metrics.
[K] Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean and after post-CMP clean. Leaving this film may result in undesirable delamination of subsequently deposited layers or "carbon spots" caused by a monolayer or more of BTA (benzotriazole)-copper complex. A monolayer, about 1 nm of BTA on copper yields a carbon atom density of about 4E14 atoms/cm2. Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, Dc at the 180 nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm^2). Dc for subsequent generations was scaled linearly with the ratio of CD to 180 nm. Dc = (CD/180)(7.3E+13).
[L] Etching, stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant. Changes to the dielectric constant need to be measured (at a minimum) by interdigitated trench test structures, as measurements on planar films through MIS capacitor measurements are generally not representative of integrated structures. One common approach is to compare measured RC products with those from computer simulations assuming bulk dielectric constant values. The difference between the measurement from the simulation can be representative of the etch/strip/clean damage. The color change from Yellow to Red in 2012 reflects the dielectric change to a κ-value of < 2.1.
[M] Current etch and strip methods can damage porous low-κ films through the removal of carbon species; however, the extent of this damage may not be fully determined until after subsequent wet cleans. The CD loss after etch and strip may be negligible, but, following wet clean, the CD loss may become significant. Because the clean can remove film thicknesses rendered vulnerable by the etch, the extent of CD loss after wet cleans can be the result of both the etch and cleans processes. While not explicit in measurable CD loss, bowing of the trench and via structures should be minimized to allow conformal liners and plating base deposition and to reduce copper voiding effects. The color change from Yellow to Red in 2012 reflects the dielectric change to a k-value of < 2.1.

Table 82b Interconnect Surface Preparation Technology Requirements—Long-term Years*

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*D ½*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*M*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*M*
Wafer diameter (mm)	**450**	**450**	**450**	**450**	**450**			*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**			*D ½, M*
Front surface particles								
Killer defect density, D_pR_p (#/cm^2) [A]	**0.016**	**0.02**	**0.014**	**0.017**	**0.022**			
Critical particle diameter, d_c (nm) [B]	**14**	**12.5**	**11**	**10**	**9**			
Critical particle density, D_{pw} (#/wafer) [C]	**123.1**	**155**	**106**	**133.4**	**168**			
Back surface particles								
Back surface critical particle diameter (nm) [D]	**NA**	**NA**	**NA**	**NA**	**NA**			
Back surface critical particle density (#/wafer) [E]	**NA**	**NA**	**NA**	**NA**				
Edge bevel particles								
Edge bevel critical particle diameter (nm) [F]	**56**	**50**	**44**	**40**	**36**			
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**			*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**			*M*
Metallic Contamination								
Critical front surface metals (10^9 atoms/cm^2) (H)	**10**	**10**	**10**	**10**	**10**			
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**100**	**100**	**100**	**100**	**100**			
Mobile ions (10^{10} atoms/cm^2) [J]	**2.4**	**2.4**	**2.3**	**2.3**	**2.3**			
Organic contamination (10^{13} C atoms/cm^2) [K]	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**			
Cleaning Effects on Dielectric Material								
Maximum dielectric constant increase due to Etch, Strip + Clean [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**			
Maximum dielectric constant increase due to rework [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**2.00%**			
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**			

** Columns for years 2019 and 2020 will be updated in 2006.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



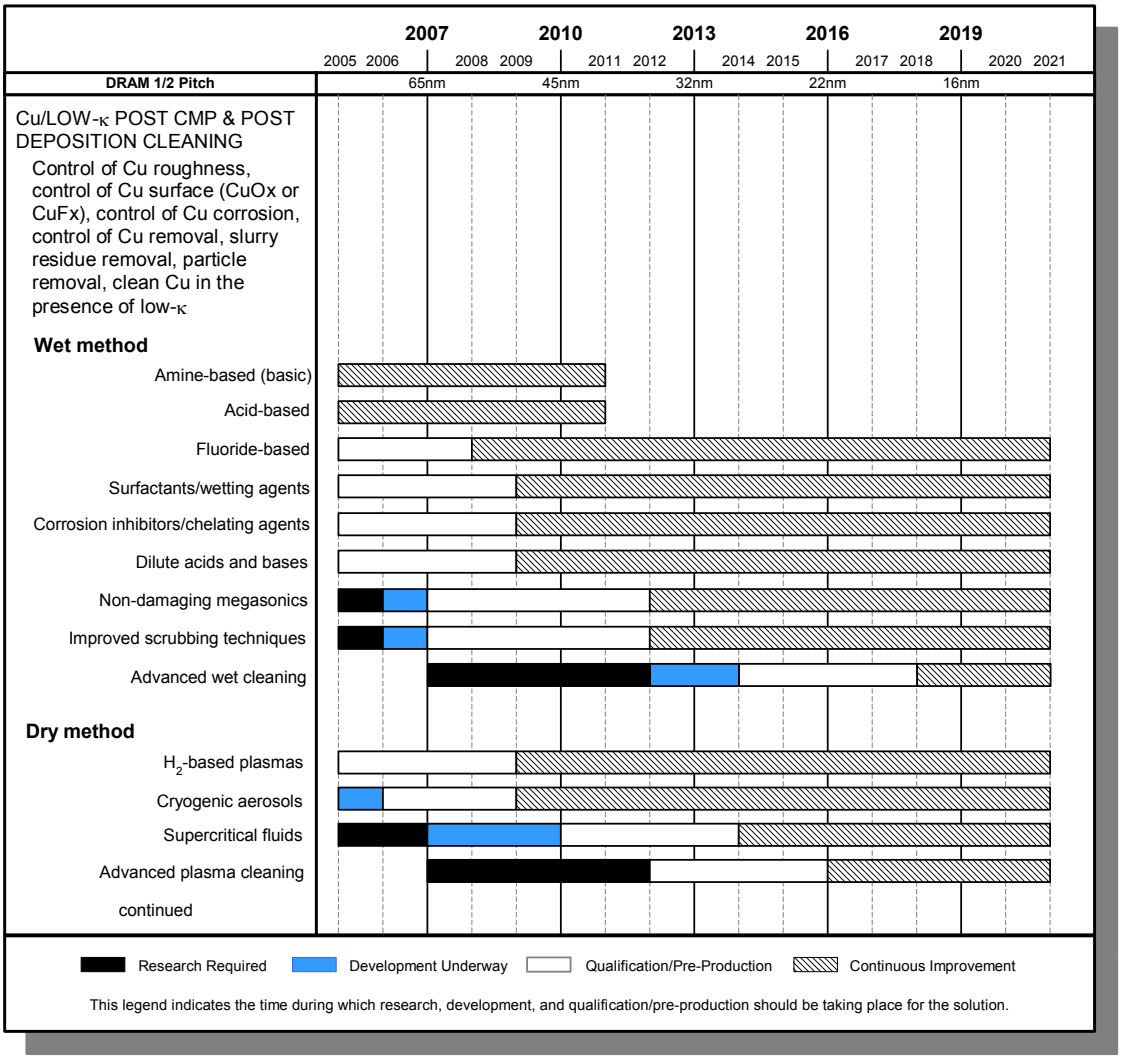


Figure 79 Interconnect Surface Preparation Potential Solutions

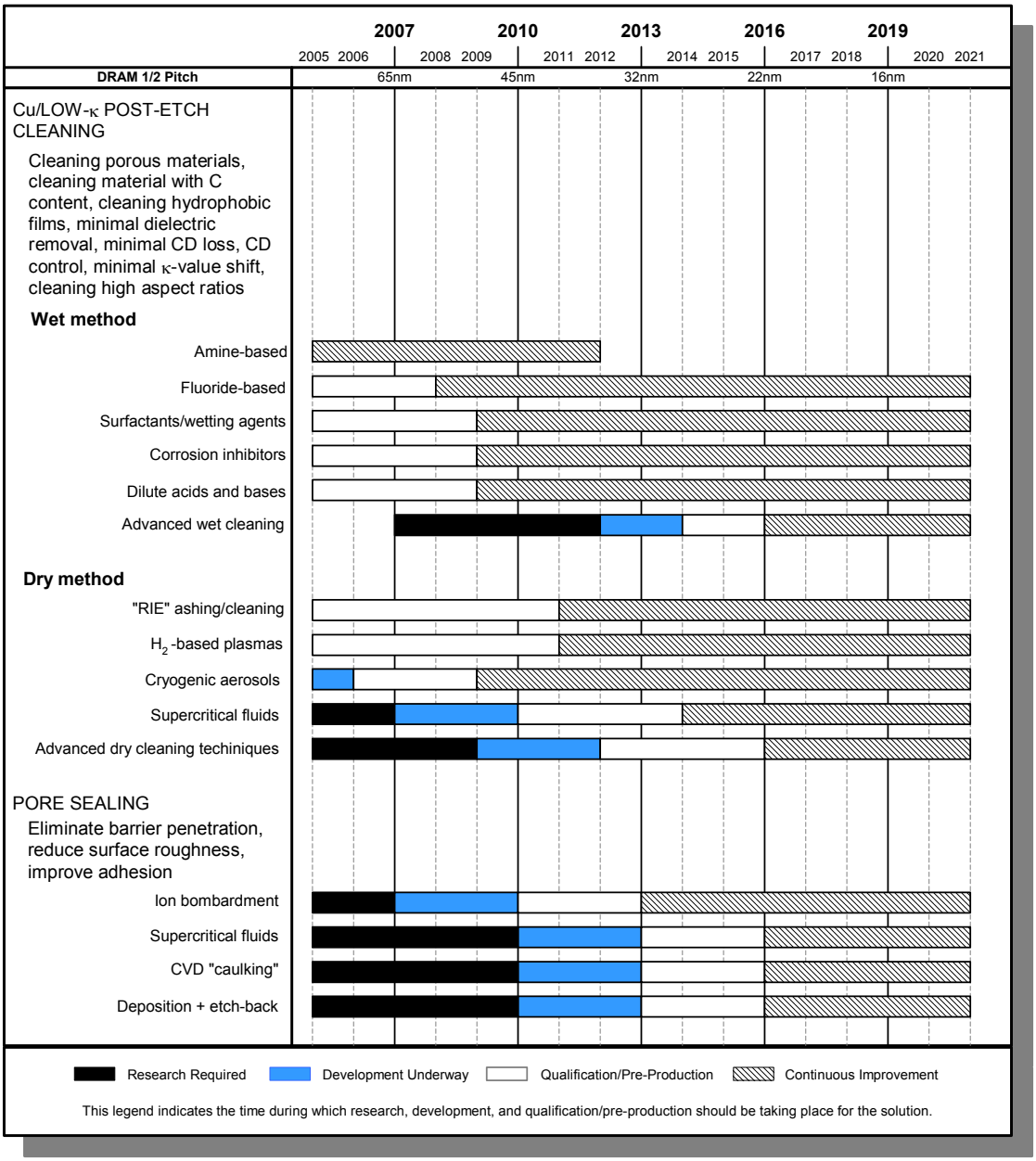


Figure 79 Interconnect Surface Preparation Potential Solutions (continued)

PASSIVE DEVICES

INTRODUCTION

Precision passive devices are a new demanding challenge for current and future on-chip interconnect architectures. The request for high quality capacitors, inductors and resistors is mainly driven by advanced mixed-signal, high frequency (RF) and system-on-a-chip (SOC) applications. Reduction and control of substrate coupling noise and other parasitics for mixed-signal and RF CMOS applications is one of the major tasks. From an application point of view the most important requirements for passives are listed in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter. In the past, the traditional method of realizing passive circuit elements (for example, capacitors, resistors) on ICs was integration during front end processing. In this case doped monocrystalline Si substrate, polycrystalline Si and Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during

front end processing suffer increased performance degradation especially when used at high frequencies. Therefore, there is an increasing demand for low loss, low parasitics, but high quality passive devices in the interconnect levels.

For interconnect integration the key challenge is to achieve this goal in a modular and cost-effective way, without sacrificing the overall interconnect performance and reliability. Currently two fundamentally different approaches are pursued. One is the introduction of optional or additional interconnect levels in combination with new materials to accomplish the necessary functions and attributes with the highest Q-factors and a minimum usage of additional chip area. In general, this approach has the disadvantage of higher process complexity and potentially higher manufacturing cost. The alternative is simply to use native or "parasitic" properties, e.g., capacitance, inductance and resistance, of existing interconnect levels. This second approach is the least demanding for wafer manufacturing, but suffers typically by reduced Q-factors of the passive devices and a larger chip area consumption.

MIM CAPACITORS

High quality MIM capacitors are seeing increased use in CMOS, BICMOS and bipolar chips. Typical applications are filter and analog capacitors (for example, in A/D or D/A converters), RF coupling and RF bypass capacitors in RF oscillators, resonator circuits and matching networks. Key attributes of MIM capacitors are high linearity over broad voltage ranges (low voltage coefficients), low series resistance, good matching properties, small temperature coefficients of capacitance, low leakage currents, high breakdown voltage and sufficient dielectric reliability.

The economic demand for small chip area consumption leads directly to the request for higher MIM charge storage densities. Above a capacitance density of 1.5–2 $fF/\mu m^2$ a further thinning of the traditionally used Si-oxide or Si-nitride dielectrics is no longer useful because of increased leakage currents and reduced dielectric reliability. Therefore new high-κ dielectric materials, such as Al_2O_3, Ta_2O_5, HfO_2, etc., or combinations of different materials are being evaluated as MIM dielectrics and will be used in future applications.

As always, the introduction of new materials leads to new challenges in material processing (such as ALD deposition), process integration and reliability. High quality films with excellent thickness uniformity, low defect densities and high dielectric constants need to be deposited below 450 °C to be compatible with the overall interconnect architecture. To reduce parasitic substrate coupling and allow for high quality factors of the MIM capacitors, integration into upper metallization levels is preferred.

Low resistive capacitor electrodes and perfectly engineered electrode-dielectric interfaces are necessary to achieve high MIM quality factors and the required reliability. Some promising integrations of high κ materials in MIM capacitors have been demonstrated in the literature (see the *Appendix: Passive Devices*). However, improvements are still necessary in order to come to cost-effective and manufacturable solutions with a minimum of additional process steps.

INDUCTORS

High quality on-chip inductors are critical components in analog/mixed signal and high frequency (RF) applications. Currently they are widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers and low noise amplifiers. Key attributes are high quality factors, Q, at high inductance, high self-resonance frequency, low Ohmic losses, low eddy currents and low capacitive substrate losses.

Today, spiral inductors in the upper thick Al- or Cu-metallization levels are most widely used in order to fabricate low resistive coils with sufficient spacing from the Si-substrate to achieve optimized quality factors. These simple spiral inductors can be fabricated relatively easily using standard interconnect processes. But they may not in every case be good enough to fulfill all future RF requirements. Therefore, some more advanced constructions and approaches are being pursued.

Examples like shunted coils, realized in several metallization levels, the use of metallic or even magnetic ground planes, suspended spiral inductors in air-gaps, post passivation add-on modules with coils in fat redistribution metal layers (several μm metal thickness) or solenoidal inductors with and without ferro-magnetic core fillings have been successfully demonstrated. Other possibilities for reducing substrate losses is the use of high Ohmic Si substrates, SOI substrates or localized semi-insulating Si-substrate areas after ion- or proton- bombardement (see appendix: Passive devices).

However, not all of these alternative fabrication schemes are suitable for manufacturing, because of integration and process complexity issues or incompatibilities with device or product requirements. These approaches are an expression

of the constant struggle for improved performance with higher inductance at higher frequencies or improvements in quality factor by reducing the Ohmic losses in the coil and/or the parasitic substrate.

RESISTORS

Precision thin film resistors are widely used in analog and mixed signal circuits and specific SOC applications. Key attributes are precise resistance control, excellent matching properties, high voltage linearity, low temperature coefficients, low 1/f noise and low parasitics resulting in high Q values. Today the most widely used Si-substrate-, poly-Si-, or silicide- resistors fabricated during front end processing suffer mainly from poor 1/f noise performance and substrate losses.

Thin film resistors in the metallization levels can significantly improve the 1/f noise performance and other substrate losses. Key challenges for resistors in the interconnect are finding materials with moderate and tunable sheet resistance compatible with the standard interconnect materials and integration schemes, excellent thickness control and good etch selectivity to dielectrics with a modular integration scheme. Especially for Cu-metallization schemes, TaN has been found to be a promising candidate; however, other materials may see use in the near future.

More details on the applications, typical requirements, the processing and integration challenges of the different passive devices (MIM capacitors, inductors and resistors), including a list of recent references, can be found in the interconnect appendix section on 'Passive Devices'.

RELIABILITY

INTRODUCTION

Rapid changes are occurring in interconnect materials and structures resulting in significant new reliability challenges. Understanding failure mechanisms in Al and SiO_2 technology grew incrementally over some 35 years. In the last ten years the industry has moved to copper, and is now also attempting to install a series of new and/or significantly modified low-κ interlayer dielectric materials. All of these changes are expected to occur with no reduction in the reliability afforded from the previous mature materials sets. Failures are further exacerbated by continued increases in interconnect density, number of layers, and power consumption. This section presents a short description of the reliability concerns that have been identified with Cu/low κ metalization.

Copper was adopted partially due to the expectation that it would have higher reliability than aluminum. Under equivalent circumstances that could be true. However, the industry has continued to reduce feature sizes and increase line current densities, as well as the overall number of metal lines on the die to the point that maintaining reliability of copper is just as challenging as it was for aluminum. Metal reliability of copper is strongly dependent on the properties of the surrounding barrier and seed layers as well as the surrounding dielectric. Reliability of Cu/low-κ interconnects must be viewed as reliability of a system, which is now known to have three high level differences from its predecessors:

1. The physics of metal migration are somewhat different than that of aluminum
2. In low-κ dielectrics the metal is more likely to be in tension rather than compression
3. As the 'κ' of the dielectric is reduced, so is mechanical strength

CU METALIZATION

High performance logic began transitioning to copper ten years ago and today the majority of leading-edge circuits make use of it. Copper readily diffuses into silicon and most dielectrics, and must be encapsulated with metallic (such as Ta, TaN) or dielectric (such as SiN, SiC) diffusion barriers to prevent electrical leakage between metal wires and degradation of transistor performance. Cu diffusion is greatly enhanced by electric fields imposed between adjacent wires during device operation, and absolute barrier integrity is crucial to long-term device reliability. Copper, unlike aluminum, has no self-passivation layer and it has been shown that surface diffusion dominates electromigration behavior, thus, the interfaces with diffusion barriers play a key role in overall reliability.

Study is now focused on understanding what appears to be two principal failure types, currently referred to as "weak" and "strong" mode. Strong mode failures are usually the result of voids forming on the interface at the top of the line between the Cu and the dielectric barrier. These are typical electromigration failures, following Black's equation, but with the principal diffusion pathway being along the surface of the Cu line and not the internal grain boundaries. Weak mode

failures are not well understood, but generally result from voids forming in the vicinity of the via (not necessarily in the via). As weak mode failures result in much shorter lifetimes their cause and mitigation are areas where much research is needed.

ULTRA LOW-K MATERIALS

The industry transition to low-κ (defined roughly as those having bulk $\kappa \leq 3.0$) materials has taken longer than any prior roadmap has predicted. This transition has been paced first by the ability to assemble structures using materials that are inherently less mechanically and chemically robust, and then by the reliability of those structures in their end product use.

Silicas, with backbone modifications that include carbon (SiOC), are the material family of choice. There are however, still some manufacturers using organic polymers in certain applications. The dense forms of these materials will afford bulk-κ values reaching as low as ~2.5. To go lower in κ, porosity is added to reduce the volume fraction. FSG materials, with permittivity lowered by the incorporation of fluorine, have not proven to be viable as they were found to be generally chemically unstable.

In comparison to SiO_2, all of the low-κ candidates present common reliability challenges:

- All have thermal expansion coefficients that in general place the metallization in tension resulting in "via popping" failures that may not appear until after packaging and test. The more carbon in the material backbone the higher the expansion coefficient and more stress applied to the metals.
- All have lower mechanical and yield strength offering less capability to maintain the structure under the strains induced in processing, packaging and field use. Cracking and delamination failures in bonding is the current challenge for the industry. New micro-cracking phenomena have recently been observed that may not appear at a given layer until several more have been placed on top. Finally the lower κ materials are less resistant to metal extrusion forces that arise from either stress or electromigration.
- All of the candidate materials have lower chemical integrity; the principal impact of this is damage to the low-κ material during processing, which can increase its κ to values greater than that of the SiO_2 it was to replace. In many cases the damage is correlated with an increase in the moisture absorption and moisture content of the film. While the industry is striving to eliminate or repair the damage (for lower κ value) the reliability impact of the residual damage or of the repaired layers is largely unknown.

ULTRA LOW-K (POROUS LOW-K)

The inclusion of porosity into dielectric films exacerbates most of the above effects. Films become mechanically weaker to the point that it is postulated the bulk dielectric presents no constraint against thermal stresses, external mechanical forces, or metal extrusion mechanisms. Finally to achieve any benefit from the ultra low-κ bulk materials, dielectric assist layers such as hardmasks, CMP and etch stops, and diffusion barriers must either be eliminated and/or lowered in κ value which reduces their integrity as well.

The question of how to form a continuous metal barrier on the porous trench sidewalls and bottom that acts as a copper diffusion barrier has not been answered by the industry, much less the failure physics and reliability of the barriers and the interfacing copper lines.

Process gases and chemicals are absorbed into the bulk of the porous films. Here again, as in the case of damage the industry is striving to eliminate them for fabrication reasons or to achieve lower κ, but the reliability impact of any residuals in the layers is largely unknown

The physical mechanisms responsible for dielectric breakdown in porous low-κ dielectrics are not well understood. Failure is generally attributed more to the integration scheme than to the intrinsic material properties of the dielectrics. Contributing factors include the thickness and composition of the diffusion barrier and assist layers (hardmasks, CMP/etch stops) and the quality of the interfaces. Reliability also depends on the integrity of edge seals and passivation during and after assembly and packaging operations in order to prevent oxygen from moving through the porous material. Moreover, there is no consensus on the trustworthiness of extrapolations from stress conditions to use conditions: for example, the applicability of either the "E" or "1/E" models, whether the failure mechanisms are even the same at high versus low fields, or whether the test structures are representative of the failure sites in actual designs.

CU/LOW-κ MATERIALS AND PROCESSES

The work devoted to low- κ materials research indicates that the challenges outlined above cannot be met by developing a revolutionary new low-κ material that is orders of magnitude more robust than its predecessors. Modifications to all of the unit processes and their integration must prevent or ameliorate low-κ damage. Damascene structures in low-κ changed the approach to photoresist stripping and subsequent cleaning for interconnect layers. Initially, hardmask materials and oxygen-based chemistries for etching organic low-κ dielectrics enabled *in situ* stripping of the photoresist during the trench, contact or via etch steps. However, damage and its corresponding rise in κ value forced the use of reducing chemistries as well as new ash chamber designs. Paradoxically, some material systems work best with downstream ashing where others require a more directional reactive ion etch (RIE) like ash chamber. Dry stripping alone usually is insufficient to remove residues and particles from structures with high aspect ratios without attacking the low-κ dielectrics or copper and its barriers, so an additional wet process is usually required. No single set of strip tools, chemistries, and combinations will work for all low-κ 's and all low-κ and assist layer combinations.

Lower levels of damage have been observed resulting from CMP and pre-metalization sputter etch. The industry will work to ameliorate this damage to reduce κ, but the detailed reliability implications of any combination of processes and materials will need to be understood. All of these unit processes bring their own specific yield loss mechanisms as well as susceptibility to longer-term reliability problems.

MODELING AND SIMULATION

Cost-effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- Wire length
- Current densities expected for the currents required by the circuit
- Calculated local operating temperature, which includes the effects of Joule heating in the circuit and elsewhere

These tools must become an integral part of the circuit designer's tool set to help predict product reliability before processing begins and to develop solutions that anticipate technology and thereby accelerate their introduction.

FUTURE RELIABILITY DIRECTIONS

The sections above discuss only reliability concerns that have been identified thus far for the Cu/low-κ system. Continuing research is needed to fully understand the multi-variable nature of copper and low-κ interconnect reliability and provide accurate models for designed-in reliability. Many of the problems that result in Cu reliability issues will be more severe as feature sizes scale, as surface area to volume ratio of the metallization increases; as geometries scale to feature sizes where electron surface scattering effects become a significant contributor to resistivity, and as current densities rise. The fundamental reliability limits of copper/low-κ metallization must be identified to assess technology extendibility in these ranges, and to identify any unique failure modes that may arise.

It is expected that one or more alternate interconnect approaches, such as optical, package intermediated, 3D, or microwave, will begin to be used within the next five years. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

SYSTEMS AND PERFORMANCE ISSUES

INTERCONNECT PERFORMANCE

The adequacy of near-term interconnect technology (copper wires and low-κ dielectrics) to continue meeting the performance requirements for ICs fabricated for succeeding technology generations varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. As requirements become more stringent, it is

increasingly necessary that interconnect be considered as part of a "system" that includes the package and the silicon chip to satisfy the total technology need for the IC. Calculations show that using the existing roadmap values for technology generations from 180 nm down to 15 nm, the delay of scaled wires increases by approximately 10 ps while the delay of fixed length wires increases by approximately 2000 ps. If these wires are modified with repeating inverters, these delays reduce to approximately 3 ps for scaled wires and 40 ps for fixed length wires. In some designs these increases can be handled by modifications such as modular architectures to reduce the need for fixed length lines. However, such significant modifications to circuit architecture suffer from the disadvantages of needing new design tools and not being generally applicable to all designs.

While delay is a major factor for many digital applications, crosstalk and noise associated with decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits. These trends are a strong function of design strategy, and should be considered in that context.

In addition to the problems with scaled wires for clock and signaling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to decreasing V_{dd}, causes an increased voltage drop between the power supply and the bias point for fixed length wires. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires.

SYSTEM LEVEL INTEGRATION NEEDS

The interconnect problems identified in the prior section, along with other increasing demands due to new applications, require a system-level integration viewpoint for interconnect technology that encompasses electrical performance as well as the physical and functional assembly of macro functions to achieve desired operating characteristics. Assembly of individual components (such as bare chip or block functions on a single chip) must encompass all the performance and reliability requirements imposed on the system. For interconnect, the requirements are currently met through the distinctly separate functions of on-chip interconnect, package, silicon chip, and board-level technologies. In the future, this viewpoint will not be adequate because it is now widely conceded that interconnect technology alone cannot solve the on-chip global interconnect problem with current design methodologies. Rather, the current view is that design, process technology, packaging, and board construction will need to come together to provide an optimized integrated system level solution for interconnect requirements.

The current projection for evolution of interconnects is that in the short term, interconnect delay problems in new ICs will be met by circuit design within the constraints of planar technology with special attention to minimizing the lengths of critical paths. This approach will be done in concert with a substantial push in Cu/low-κ technology, as well as more innovative packaging and board approaches, to minimize the changes needed in design architectures while still meeting the continued advances in performance projected by the ITRS.

In the intermediate term, Cu/low-κ will be pushed to its limits, and new design architectures as well as chip-package co-design will be achieved with new CAD tools to significantly facilitate needed performance advances. Beyond these extrapolations of current practices, radically new design, packaging, and interconnect technology options will be needed. These new options will demand the total systems view of the IC, and will combine the package, the interconnect, and the silicon chip in the solution. A view of various options for combining the package, the interconnect, and the silicon chip into a complete solution is presented in the next section.

NEW INTERCONNECT CONCEPTS AND RADICAL SOLUTIONS

The need for interconnect concepts beyond the conventional metal/dielectric system that has served the industry for the first four decades of its existence has been brought on by the continued increase of frequency and power of ICs, and the continued push to smaller geometries to satisfy the needs of Moore's law. The difficulties for interconnect technology resulting from technology scaling and material changes can be easily validated by observing that in the older 1.0 μm Al/SiO_2 technology generation the transistor delay was ~20 ps and the RC delay of a 1 mm line was ~ 1.0 ps, while in a projected .035 μm Cu/low κ technology generation the transistor delay will be ~1.0 ps, and the RC delay of a 1 mm line will be ~250 ps.[1] This dramatic reversal from performance limited by transistor delay to performance limited by interconnect delay shows clearly the inadequacy of continuing to scale the conventional metal/dielectric system to meet future interconnect requirements.

Multiple options have been devised to provide alternatives to the metal/dielectric system and solve the delay/power problem. A list of the predominant possibilities is shown in Table 83. Although some of these approaches, most notably the first two, are relatively mature from a technology standpoint, it appears that unlike Al/SiO_2 or Cu/low κ, no single one of these solutions will be used universally over all IC product types (Note that this does not mean that they are demonstrated as commercially viable. Issues such as cost, testability, Si area required, etc. remain to be studied). The list in Table 83 is the Interconnect ITRS working group view of increasing complexity of implementation, based on the current status of these technologies. Since none of these radical approaches are either in prototype development or volume production by major integrated device manufacturers (IDMs), there is not a formal roadmap for associated technology parameters. Not all of these alternatives are expected to be viable for production. Even if they are shown to be technically feasible, they may not be used for a number of reasons, both operational and economic. ~~Figure A5 is provided to illustrate the expected timing of the path for the most promising of these alternatives to proceed from research to development to being available (but not necessarily chosen) for implementation.~~ The appearance of a formal roadmap of specific parameters as a function of time will be evidence for a particular approach being selected for product implementation. Such roadmaps should appear at a time near the transition from "Narrowing Options" to "Implementation." The following sections describe some of these options in more detail, as well as describing issues that need to be addressed to increase the viability of the approach.

Table 83 Options for Global Interconnects Beyond the Metal/Dielectric System

Use Different Signaling Methods – Signal design – Signal coding techniques
Use innovative design and package options – Interconnect-centric design – Package intermediated interconnect – Chip-package co-design
Use Geometry – 3D
Use Different Physics – Optics (emitters, detectors, free space, waveguides) – RF/microwaves (transmitters, receivers, free space, waveguides) – Terahertz photonics
Radical Solutions – Nanowires/nanotubes – Molecules – Spin – Quantum wave functions

DIFFERENT SIGNALING METHODS

This approach utilizes available technology with innovative approaches to signal format and circuit operation to produce current and voltage waveforms that are more compatible with high-speed global interconnects than the usual square wave approaches. Several options for this approach have been proposed. Two of those options are described below.

Raised Cosine Signaling[2]—Raised cosine signaling advocates assert that the noise crosstalk due to inductive and capacitive coupling effects will become increasingly important, and will eventually become the dominant problem over local and global propagation delays. This potential increase of crosstalk by various sources is due to 1) higher near-field coupling via capacitive, inductive and resistive links, a result of device scaling and close proximity of wires and metal layers; 2) increased coupling between distant parts via substrate and power rails; 3) increased noise coupling from intrinsic device noise such as flicker, thermal, and shot noise, and 4) high frequency radiation effects due to interconnect discontinuities. Aggressive clock distribution designs require the amount of skew and jitter for a clock signal to be less than 3–4% of the clock period. As an example, in the ITRS roadmap, the on-chip local clock is targeted for 10 GHz and global clock rates are approaching 3 GHz. This implies that the jitter/skew must be controlled to within 4 ps and 13 ps, respectively. The raised cosine technique addresses the noise crosstalk problem by using raised cosine pulses instead of square pulses as the basis functions of high-speed buses, as well as high efficiency current-mode drivers to minimize both power consumption and noise crosstalk. This approach has been shown to reduce the crosstalk noise in specific technology applications by as much as 40%.

Resonant Clocking[3]—In the resonant clock approach, traditional tree-driven grids are combined with on-chip inductors to "resonate" the clock capacitance at the fundamental frequency of the clock node. The energy of the fundamental will "slosh" back and forth between electric and magnetic forms and not be dissipated as heat. The clock drivers only need to provide the energy at the fundamental necessary to overcome losses and inject the higher frequencies required to provide sharper (not sinusoidal) clock edges. Power and clock latency are also improved because the effective capacitance of the grid is lower and fewer pre-driver stages are necessary to drive the grid. Power reduction of almost 40% is projected to be possible, depending on the Q of the resonant system. Potential skew and jitter reductions come about because of the reduced buffer latency and the bandpass characteristics of the resonant network.

CRITICAL CHALLENGES

- Manufacturing issues such as testing, cost, Si area consumed, etc.
- Extending the limited scalability of these approaches
- Providing high Q on-chip components for resonant circuits

INNOVATIVE DESIGN AND PACKAGE OPTIONS

Among the most effective short term solutions to the difficulties in IC manufacturing posed by increasing frequency and increasing power have been approaches that leverage areas of technology other than materials and processing. These other areas are predominantly design and packaging. The promise of this approach, already fulfilled in recent technology generations, is to forestall the requirement for very low-κ dielectrics or more radical approaches to global interconnect. The liability of this approach is that few design tools are available to do the multi-scale, multi-phenomenon, modeling and simulation necessary for design optimization when radical circuit architectures and packaging structures are combined. A few of the options in this approach are described below.

Interconnect-centric Design[4]—A procedure that has already been used for critical path design for several technology generations is interconnect-centric design. In this approach, interconnect design—including interconnect planning, interconnect synthesis, and interconnect layout—are optimized (often at the expense of other circuit features) at every level of the design process. This approach has the distinct advantage of using current technology to optimize performance in the design areas where interconnect is a bottleneck. It suffers from two specific disadvantages. First, appropriate interconnect design tools and design models are not available to implement this approach over all designs, so much of this work becomes custom. Second, to carry this approach to its fullest benefit often requires a major revision of standard design and layout practices, which are inconsistent with the advantages offered by scaling and technology changes that have been used in the past to follow Moore's law.

Package Intermediated Interconnect[5]—A compelling option for reducing the global interconnect problem is to move some of the interconnects from the primary chip to thicker metallization and higher performance levels on the package, or on a supplementary chip designed to carry only interconnects. This approach is labeled "Package Intermediated Interconnect." The signals would then be transferred back to the primary chip at an appropriate point. In some cases, a "Sea of Leads" approach might be used to provide major density increases in I/O to benefit not only global interconnect, but at the same time, power and ground connections. The basic components of most of the package intermediated approaches have been demonstrated at the laboratory level. Additional research in areas such as power requirements, manufacturing issues, and cost is needed. Creative development is also needed to provide implementations of this approach that will circumvent the inherent cost and reliability limitations introduced by added elements and connections.

Chip Package Co-Design[6]—Chip package co-design is the unification of models and design tools that allows global optimization and characterization of the IC/package system under development. In the optimum case this design approach would allow combined electrical, thermal, and mechanical simulation and optimization. In this approach the design trade-off complexities between various parts of the design would be captured, distributed, and managed using a co-design model. This approach needs to encompass the chip, the package, and the board (if it provides a significant interaction).

CRITICAL CHALLENGES

- Availability of design tools to do the multi-scale, multi-phenomenon, modeling and simulation necessary for design optimization for radical circuit architectures, or for combined circuits and packaging structures
- Cost and reliability of additional interconnects between chip and package
- Cost of supplemental chip (if used)

- Design issues associated with division of interconnects between chip and package
- Probing and testing of total structure

GEOMETRY

3D ICs[7]—A simple yet elegant way to reduce the burden of high frequency signal propagation across monolithic ICs is to reduce the line length needed by employing stacking of active devices using 3D interconnects. Such 3D interconnects allow communications among the active devices with minimum distance required for signal propagation. The stacked active device layers may be separate chips that are individually bonded and communicate through the package through conventional bond pads; separated chips bonded together via face-to-face pads; separate chips using innovative "through wafer" interconnects, or multiple stacks of active devices in the interconnect layers on a single chip. The separate chip approach contacted through the package is used in large volume applications today, but does not provide the minimum signal propagation lengths that could be available by through-wafer interconnects or 3D integration on a single chip. In addition, it does not provide the advantage that active devices within the 3D layers would achieve to facilitate high-speed signal transmission. Roadmap items for the separately pinned-out stacked die approach can be found in the *Assembly and Packaging* chapter of the ITRS.

The main driver for 3D integration in current systems seems to be the density perspective and not so much the possible improvement of interconnect performance. The packaging approach using stacked die has been generally adequate for this application. In future systems needing increased performance and increased functionality, it is expected that other forms of 3D integration will become more advantageous. In the SOC (System-on-a-Chip) versus SIP (System-in-a-Package) versus 3D integration debate, decreasing yield of larger die required for SOC, the high process complexity and cost associated with SOC, the limited performance increases available with SIP, the advantages of performance and density of 3D integration, and the need for systems requiring heterogeneous technologies, will favor the 3D approach. However, there may not be one universal approach to 3D integration. Depending on product and system requirements different 3D process options, such as wafer-to-wafer, chip-to-wafer, or chip-to-chip, may coexist with only limited potential for standardization.

CRITICAL CHALLENGES

- Thermal management capability compatible with high heat load of 3D interconnect
- Capabilities for thinning and bonding wafers
- Capabilities for patterning, etching, aligning and filling dense, narrow inter-chip vias
- Means to build transistor grade electronic materials for active devices at low temperature and within the interconnect structure
- Models of manufacturing cost and yields for 3D integration that allow intelligent selection among the 3D process options for specific product applications
- Probing and test of the 3D structure
- Reliability of 3D IC stacks
- Limited standardization of 3D stacking processes

DIFFERENT PHYSICS FOR SIGNAL PROPAGATION

Options for continued progress of interconnect performance significantly beyond that provided by the options described above will require employing approaches that introduce materials and structures beyond the conventional metal/dielectric system, and may require information carriers other than charge. Three examples of approaches being considered are included below.

Optical Interconnects[8]—Optical interconnects are considered a possible option for replacing the conductor/dielectric system for global interconnects. The optical approach has many variants, the simplest perhaps having emitters off-chip and only free space waveguides and detectors in top layers on-chip. Progressively more complex options culminate in monolithic emitters, waveguides, and detectors.[9] The optical interconnect option has many advantages, but also has several clear areas requiring significant research. The decisions on which signals to include in optical communications and which should remain in conventional metal dielectric, and the choice of on-chip optical emitters, are significant. In the case of optical interconnects, it is easy to assume that this solution will meet speed requirements because the signal travels at "the speed of light." However, to define the total interconnect system for this approach it is necessary to consider the delays associated with rise and fall times of optical emitters and detectors, the speed of light in the

transmitting medium, losses in the optical waveguides (if used), the signal noise due to coupling between waveguides, and a myriad of other details.

CRITICAL CHALLENGES

- For implementations requiring on-die emitters, a high efficiency, high switching rate laser source, monolithically integrated into Si CMOS, (at low cost) needs to be developed
- A low power modulator, monolithically integrated into Si CMOS, (at low cost) to be used in conjunction with an off-chip continuous laser
- Low power, high efficiency, small size optical detectors monolithically integrated into Si CMOS (at low cost)
- Low cost couplings between off-die lasers and on-die waveguides and detectors
- Reliability investigations

RF/microwave interconnects[10] [11]—A relatively radical alternative to the usual metal/dielectric interconnects is to use transmission of signals from one part of a chip to another via RF or microwaves. This option essentially takes the form of a LAN on a chip, with transmitters, and receivers combining antennas and appropriate signal generation and signal detection circuitry. Transmission in this case has been proposed to be a "free-space transmission" through the package and IC structures. Another possibility is that the RF signal is capacitively coupled through a waveguide in the package lid. The transmission has been proposed as a sinusoidal signal or as a coded digital signal, depending on the specific system concept employed. Each option has its own particular advantages and disadvantages, as well as its own unique requirements. The basic concepts of this approach to global interconnects have been demonstrated.

CRITICAL CHALLENGES

- Complete characterization of total system concept for cost and performance comparison with alternative solutions
- Full design rules for the electrical and electromagnetic portions of RF and microwave interconnect
- Identification of appropriate IC substrate and packaging materials for optimized transmission of RF and microwaves

Guided terahertz waves[12] *and plasmons*[13]—Terahertz waves and plasmons are hybrids of RF and optical signaling, using transmission frequencies from around 10^{12} Hz to optical. These are propagated through micro-stripline waveguides possibly built with Cu/low κ or SiO_2. This approach is attractive because it provides the opportunity to significantly extend the bandwidth of interconnect systems without changing the material set. This technology may lend itself to smaller feature sizes than optical or RF and may be usable in intermediate interconnect layers.

CRITICAL CHALLENGES

- High efficiency sources capable of monolithic integration into Si CMOS (at low cost)
- Low power terahertz or optical modulators that can be monolithically integrated into Si CMOS (at low cost)
- Low power, monolithically integrated into Si, CMOS (at low cost) detectors of small feature size need to be developed. (The small terahertz detectors that are currently available are largely bolometric, and do not afford the bandwidth promised by the terahertz carrier.)
- A study of micro-stripline scalability to determine such parameters as: impedance, losses, dispersion, mode stability, power handling capability, electrical reliability, "microstrip-to-microstrip crosstalk," and others needs to be performed with a resulting set of design rules

RADICAL SOLUTIONS

In addition to the aforementioned options for global interconnect solutions, there are several more radical options that may offer unique advantages. These radical alternatives include such areas as nanotube interconnects[14], molecular interconnects[15], spin coupling, and quantum waves.[16] These options are in their early stages of development, and have a common critical need for a total system concept that demonstrates their utility in the interconnect function as well as a manufacturing methodology for their fabrication. In addition, continuing research has uncovered new and unexpected features of some of these radical alternatives.[17] Although many important features of radical solutions to the interconnect problem have been realized, there is still a critical need for additional creative approaches that will provide the defined roadmap capabilities while meeting the difficult challenges of cost and manufacturability.

The discussions above have described several *new concepts and radical alternatives* for providing interconnect solutions compatible with the increasing requirements needed to continue the progression of IC technology. Although several independent approaches are described, it is expected that the solutions used will be different for different applications, and that the ultimate solutions may require a combination of several of the approaches described above. This realization makes it imperative that cross-functional research is emphasized to ensure that the best approaches using all of the possible techniques are fully evaluated.

Interconnect technology has been following an evolutionary path ever since it's inception by Robert Noyce in his 1959 patent. Even the difficult transitions to Cu/low κ are relatively minor technology transitions in comparison to some of the disruptive technologies proposed above. There are many technology issues to be dealt with but before the industry will embrace a large investment to arrive at solutions, some strategic questions need to be addressed:

1. How does the approach fit in the solution of the overall interconnect problem?
2. How much of the problem does it solve? (for which products?)
3. When will the technology be ready for implementation?
4. How does the capability of this technology match needs at the projected time of implementation?
5. How extendable or for how many generations will it provide benefit?
6. What other technologies will need to be developed to effectively implement the solution?
7. What changes in software, hardware, manufacturing, applications, or business will need to be in place to effectively implement the solution?
8. What technical problems need to be solved before implementation and what is their current state?
9. What needs to be done/added to provide the implementation on time?
10. How will the technology be transferred into the mainstream?

CROSS-CUT CHALLENGES

INTERCONNECT AND DESIGN & MODELING AND SIMULATION

The interconnect performance of future technology nodes can no longer be provided by material and technology improvements alone. Therefore the interaction between material science, wafer technology, design, modeling and simulation is becoming of even greater importance in supporting the continuing interconnect scaling. Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Further, the models are largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and chose the correct interconnect routing, (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to effectively utilize both the near term and far term proposed interconnect systems. The upcoming new interconnect challenges specifically;

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1cm). This capability will also be needed for systems using RF or terahertz wave interconnections.
2. The impact of the Cu resistivity increase on delay time must be considered in realistic models. These models need to take into account line width, line aspect ratio, sidewall roughness, metal grain size and the respective coefficients for grain boundary-, surface- and impurity-scattering.
3. Signal delay uncertainties because of crosstalk effects between neighboring interconnects and the impact of dummy metal features need to be considered in appropriate models. Because of increasing line aspect ratios these effects may become major issues.
4. Process variations (e.g., CD tolerances, line height variations, sidewall roughness, etc.) will become of ever increasing importance with further shrinking of interconnect line and via sizes. Therefore variation tolerant designs and variation sensitive models and simulations are needed to support the upcoming technology nodes.

5. A means to optimally place function blocks will be needed for the 3D integrated circuits not only on an individual die but also now on a stack of die.
6. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
7. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurances of reliability critical 'hot spots' within the die. Predictive thermal models, that can accommodate thermal impacts of low-k dielectrics with reduced heat conductivity, RF standing waves, the multiple heat generating layers embedded in the 3D IC stack, and heat generated by, as well as thermal performance of optical devices and quantum well devices will be needed

Modeling and simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to prediction of resistivity increase of further shrinking copper interconnects (due to grain structures, Cu/barrier interfaces and impurities) and the physical structure and properties of new low-k dielectrics and other more exotic interconnect materials.

In all of these cases, modeling and simulation should provide predictions accurate enough to reduce as much as possible the need and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for modeling and simulation is increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical and electrical modeling (which in this issue of the roadmap has newly become one of the short-term challenges for modeling and simulation).

Specific interconnect needs for modeling and simulation include: performance prediction (including high frequency effects and reliability) for complex (e.g., 3D) structures fabricated with real non-idealized processes (etching, PVD, CMP), with hierarchical capability to choose the appropriate tradeoff between speed and accuracy for the application in question; tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; and materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier, and dielectric). Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, and copper thinning and dishing in CMP. See the *Modeling and Simulation* chapter.

ENVIRONMENT, SAFETY, AND HEALTH

Interconnect technologies carry unique environmental, safety, and health (ESH) challenges. The drive for performance at the advanced technology nodes requires the introduction of many new materials (low-κ dielectrics; copper conductors; seed, barrier and pore sealing materials, etc.) and new processes (electrochemical deposition, CVD metal/dielectric deposition, Cu/barrier CMP, low κ etch/clean, and others) This results in numerous ESH concerns, especially considering the rapid pace of insertion of these unique materials and processes into manufacturing. Both wet and dry processes will continue and require appropriate abatement; the introduction of new metal and dielectric materials adds to these ESH challenges. The new materials, precursors, and processes that will be required for the low-κ dielectrics and CVD conductor/seed/barrier depositions must be carefully screened for ESH issues during the early phase of development. Health and safety properties of reaction products/emissions; materials compatibility with equipment and other chemical components; flammability and reactivity must be predetermined to ameliorate any potential ESH impact. The industry must continue to reduce chemical usage, and chemical emissions and waste (copper plating solutions, CMP slurries, acids/solvents, PFCs, water) through process optimization, use of alternative chemistries, recycling, and/or abatement. Refer to the Environment, Safety, and Health chapter for comprehensive information and for a link to a new chemical screening tool (Chemical Restrictions Table).

At this point it appears that the insertion of low–κ materials has only a minor impact on ESH. The materials themselves are relatively benign. The CVD precursors are in many respects much less dangerous than the SiH_4 predecessors. Solvent systems for spin-on low κ are generally environmentally acceptable when handled using normal manufacturing procedures. The etch chemistries for forming the damascene relief structures use gases that the industry has experience in handling and abating.

The transition to copper metallization has eliminated the need for the halogenated etch chemistries used in aluminum etch, but has created aqueous waste streams containing copper metal and ions, and suspended particles. These waste

streams are the result of the electroplating chemicals used for the deposition and residues that result from the subsequent copper CMP process. The copper in these waste streams can be highly dilute; either at the source (e.g., CMP rinse water), or as a result of combining them with other acid waste at the facility level. In the case of CMP, the slurry of abrasive particles are a large proportion of the waste stream, which also includes relatively small amounts of Cu metal and Cu ions. Solutions such as electrophoresis, electrowinning and ion exchange exist to remove the copper from the more concentrated copper plating waste stream. However, copper removal from the CMP slurries is more difficult due to the dilution. A more recent ESH concern is the potential impact of the nano-particles (particles < 100 nm in size) most likely contained in the spent CMP slurries. There is evidence that the properties of nano-particles can be quite different form the bulk properties of the material with, as of now, poorly understood health and environmental implications.

2005 ITRS INTERCONNECT APPENDIX

DIELECTRIC

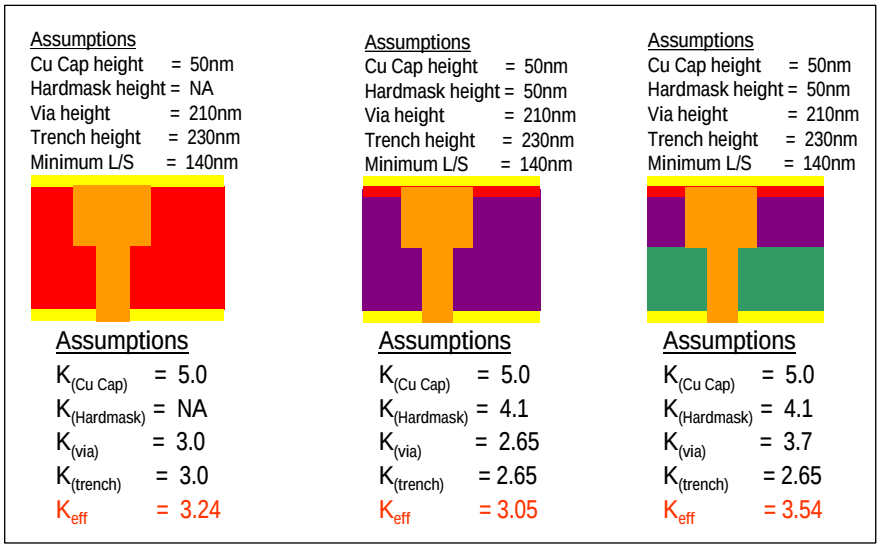


Figure A1 90 nm Potential Solutions (2004)

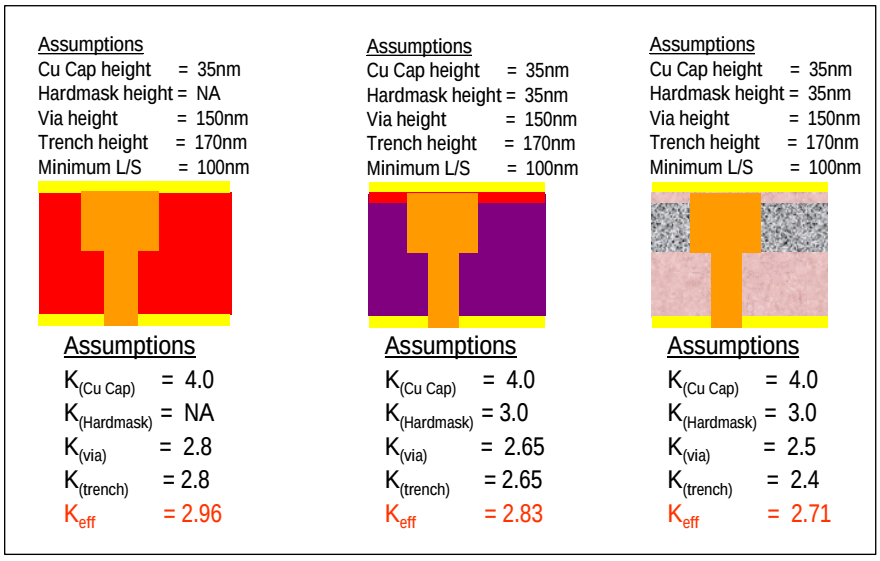


Figure A2 65 nm Potential Solutions (2007)

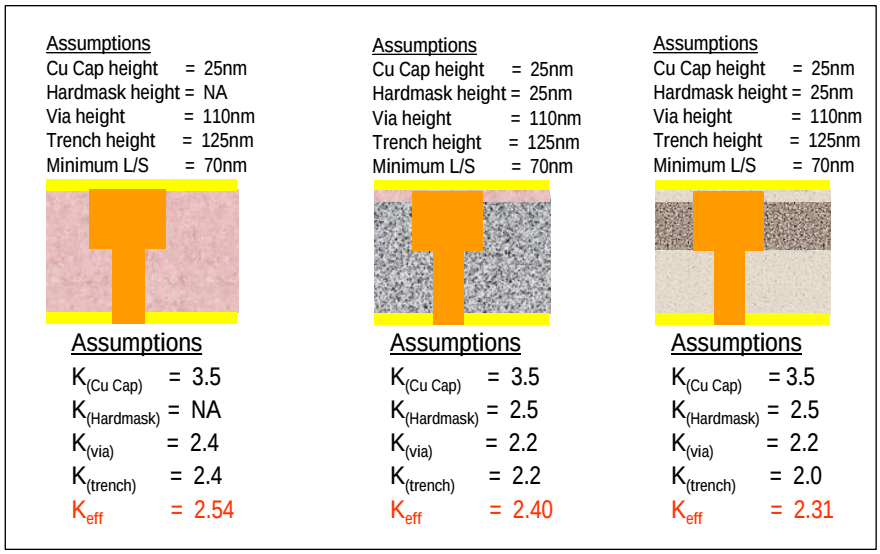


Figure A3 45 nm Potential Solutions (2010)

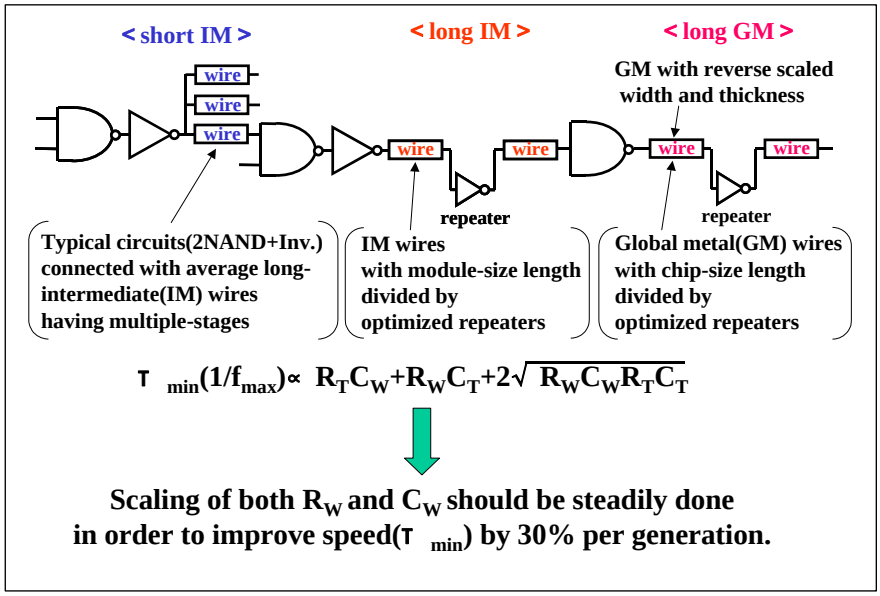


Figure A4 Critical Path in High-end SOC and RC Scaling Scenario

Table A1 Assumption on Interconnect Parameter Estimation Model

	Assumption on Interconnect Parameter Estimation
Design Rule	× 0.70/scaling, reverse scaling for GM
Chip Size	=7 mm^2 as 1-clock cycle limit
Module Size	× 0.70/scaling
Repeater	Inserted for long IM and GM wires
Gate Density	× 2.0/generation (based on ITRS 2002 MPU roadmap)
Active Power Density	× 0.6/generation with average-long IM wire
Logic Depth	× 0.75/scaling
T min.	× 0.70/scaling

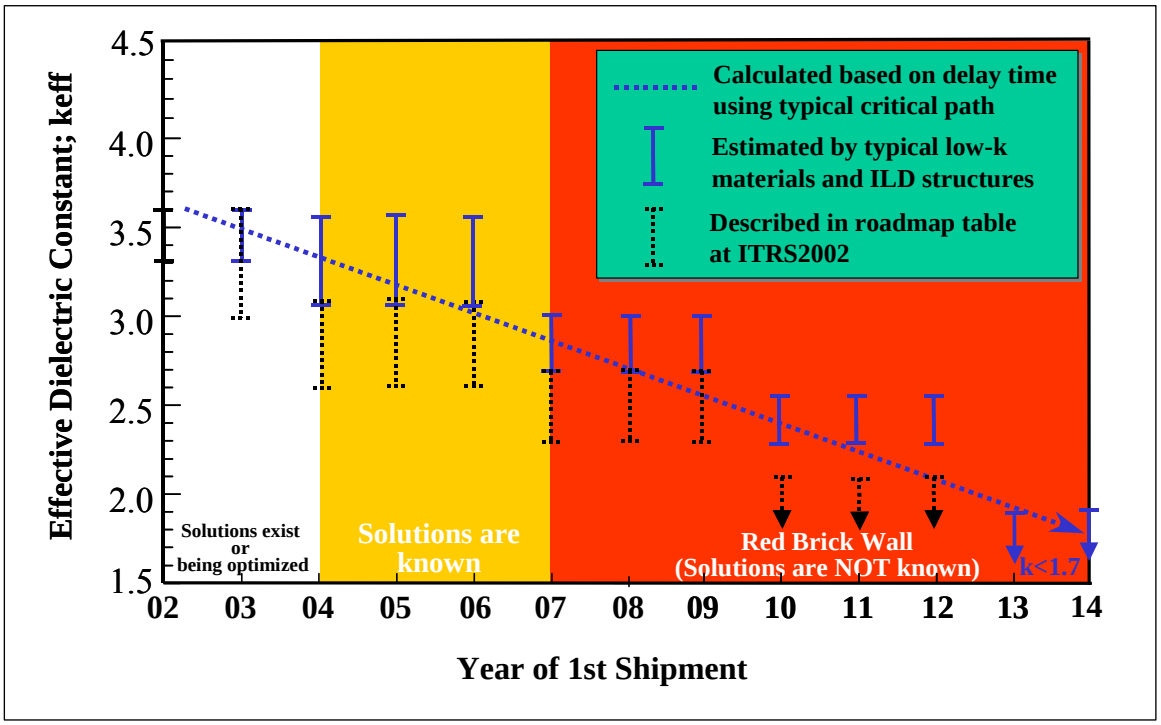


Figure A5 ITRS 2003 κ_{eff} Roadmap Revision

PASSIVE DEVICES

A new demand for current and future interconnect architectures is the inclusion of precision on-chip passive elements, such as high quality capacitors, inductors, resistors, and other components into the metallization scheme. This request is

mainly driven by advanced mixed-signal, RF and system-on-a-chip (SOC) applications.[18,19,20,21,22] The traditional method of realizing passive circuit elements (e.g., capacitors, resistors) on ICs was integration during front end processing. In this case, doped monocrystalline Si substrate, polycrystalline Si, and the respective Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during front end processing suffer increased performance degradation, especially when used at high frequencies. Therefore, we see an increasing demand for low loss, low parasitics, but high quality passive devices in the interconnect levels. For interconnect integration the key challenge is to achieve this goal in a modular and cost-effective way, without sacrificing overall interconnect performance and reliability. Currently the favored approach is the introduction of optional levels and new materials to accomplish the necessary functions and attributes. Reduction and control of substrate coupling noise and other parasitics is one of the most important tasks for mixed signal and RF CMOS applications. For the most widely used passive devices, such as capacitors, resistors and inductors, the expected future requirements at the different technology generations of analog, mixed-signal, and RF products can be found in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter.

In the following, typical applications, requirements and integration challenges of MIM capacitors, inductors and resistors are briefly discussed.

MIM CAPACITORS

Applications in CMOS, BICMOS and Bipolar chips

- Decoupling capacitors for MPUs used to reduce the transient currents across the on-chip voltage/ground-interconnects and the chip-to-package interconnects during the switching cycles of the CMOS circuits
- RF coupling and RF bypass capacitors, in high frequency oscillator and resonator circuits and in matching networks
- Filter and analog capacitors in high performance mixed-signal products, e.g., A/D or D/A converters
- Storage capacitors in DRAM and embedded DRAM/logic devices

Typical MIM requirements

- Small feature size and high charge storage density
- Low leakage currents and dielectric loss
- High dielectric breakdown voltage and reliability
- High precision of absolute and/or relative capacitance between neighboring MIMs on the same chip
- High linearity over broad voltage range (low voltage coefficients)
- Small temperature dependence (small temperature coefficients)
- Low parasitic capacitance
- Low resistivity of the electrodes and wiring to allow high switching speeds with high Q values, but without excessive heating.

Process integration challenges

- Very thin high quality dielectric films with excellent thickness uniformity and control
- Preferably high κ dielectric films in order to reduce the capacitor size. Compare to the *Dielectric Potential Solutions figure* for suitable materials
- Low defect densities for dielectric and metal films (low surface roughness)
- Low deposition temperatures (<450°C) to be compatible with overall metallization requirements, especially when low-κ intermetal dielectrics are utilized
- Smart modular integration schemes making optimal use of existing metal levels in order to reduce overall costs, such as the number of additional process steps and optional lithography levels
- Realization of MIM capacitors in the upper metal levels to reduce parasitic substrate coupling and to maintain high Q values. The use of low-κ intermetal dielectrics should also be beneficial, but may introduce other integration challenges.

Successful realizations of MIM capacitors can be found in the literature for Al-based and Cu-based metalizations as well.[18, 19, 20, 23, 24, 25, 26, 27, 28] Today most MIM capacitors in manufacturing are using silicon oxide, silicon oxynitride or silicon nitride as MIM dielectrics with sufficient material properties, reasonably good RF performance and easy

integration into Al- or Cu-based interconnect technologies.[29] Different MIM capacitor architectures, single and stacked approaches, were realized and characterized in a 130 nm multi-level Cu interconnect technology.[30]

Several papers are published with promising data on the integration of interconnect compatible high κ MIM dielectrics (e.g., Al_2O_3, Ta_2O_5, HfO_2, Nb_2O_5, TiTaO).[20, 31, 32, 33, 34, 35, 36, 37] The high κ MIM dielectrics are deposited either by PVD, followed by an appropriate anneal, or by CVD and especially atomic layer CVD processes keeping the overall temperature budget typically below 400–450°C.

However, not all approaches with record breaking capacitance densities (between 10–26 fF/μm^2) may be useful from a leakage current, voltage- and temperature-linearity or dielectric reliability point of view. Recently laminated (multi-layered) films of different high κ MIM dielectrics have been proposed to overcome these problems.[34, 38, 39, 40]

The manufacturing of MIM capacitors with high capacitance density, high quality Q, good reliability and low additional cost, is a real challenge. Therefore, in many applications, simply the parasitic or native capacitance of horizontal or vertical parallel plates or comb and finger-like structures in different metal levels are used to realize an integrated capacitor with somewhat reduced area capacitance density.[41, 42, 43] In this approach chip area is traded for a reduction in process complexity.

INDUCTORS

Applications of on-chip inductors, especially in RF circuits

- Impedance matching between different building blocks in today's microwave RF circuits. With increasing frequencies, on-chip inductors will gain even more in importance in the future.[44, 45, 46]
- RF transceivers
- Filters
- Voltage controlled oscillators (VCO)
- Power amplifiers and low noise amplifiers (LNA)

Typical inductor requirements

- High quality factors, Q at high inductance. Increasing inductance typically results in reduced quality factors Q
- High self-resonant frequency (SRF)
- Low Ohmic losses in the inductor coil (dominant at lower frequencies)
- Low capacitive substrate losses (dominant at high frequencies)
- Low eddy currents generated by inductor-substrate interactions, resulting in increasing effective resistance at higher frequencies

Process integration challenges

- Making use of thick metal lines to achieve lower coil resistances. Cu metallization is beneficial as compared to traditional Al-interconnects. For spiral inductors built in Cu-damascene technique with an improvement of Q by a factor of 2 has been reported as compared to similar Al-coils.[47] However, shunted Al-coils realized in different metal levels may also be feasible.
- Sufficient spatial separation of inductors and substrate, e.g., by putting the coils in the top metal levels or even above the passivation into the polyimide, helps to reduce capacitive and inductive parasitics and improves the Q-value. Low-κ materials help to reduce the capacitive parasitics and the substrate noise.[48, 49, 50, 51]
- Making use of higher resistive Si-substrates is also improving the parasitic substrate losses; however, this approach may not be feasible in every case.[45]
- The introduction of metallic shieldings (metal ground planes) in the lowest metal level underneath the inductors can reduce the eddy current losses in the substrate.[44, 45, 46]

Currently, spiral coils realized in single Al- or Cu- metal levels are the most common type of on-chip inductors. However, shunted multilevel spirals and solenoidal types of inductor designs, which are supposed to have lower substrate losses, may be used in the future.[47]

The influence of extreme metal thicknesses (5 μm–22.5 μm) and innermost turn diameters on Q-factors of spiral inductors as well as the questionable effect of an additional aluminum layer on top of a Cu-based inductor stack is reported.[52, 53]

A significant improvement of the quality factor was achieved by reducing the substrate coupling in making use of the airgaps in suspended aluminum spiral inductors and Al-solenoidal inductors.[54, 55] Using surface-micromachining suspended spiral inductors of 1.38 nH (at 1GHz) were demonstrated with a quality factor of 70 at a frequency of 6 GHz.[56] Another method for Q-value improvement (30%–70%) is the formation of localized semi-insulating Si-substrate areas under the inductor coils by proton bombardment after device fabrication, such as before interconnect, or even after interconnect fabrication.[57, 58] Porous silicon substrates were also reported to improve Q-values and resonant frequencies.[59] In using SOI substrates excellent inductor Q-values of ~20 were demonstrated without extra mask and processing steps.[43] Extremely high Q-values ~40 were reported for above passivation (above IC) inductors using 5 μm Cu lines in BCB dielectric (κ~2.7) on top of a multi-layer Cu/oxide interconnect manufactured in a 90 nm RF-CMOS platform technology.[60]

The successful integration of micro-inductors using magnetic materials was reported also. The introduction of a magnetic ground plane of CoZrTa increased the inductance of a square spiral inductor by 36~50%.[61] A spiral inductor sandwiched between two layers of ferromagnetic CoNbZr was demonstrated to improve the inductance by 19% and the quality factor by 23% at 2 GHz.[62] Another example is the integration of a ferromagnetic core ($Cr/Fe_{10}Co_{90}/Cr$) into a solenoidal inductor.[63] At lower frequencies (<0.2 GHz) up to an eight-fold enhancement in inductance and up to a seven-fold improvement in quality factor have been achieved by using the ferromagnetic cores. At higher frequencies, however, those improvements were significantly degraded by ferromagnetic resonance losses in the ferromagnetic core and by eddy currents.

Significant reduction in substrate noise is reported for an inductor on an ultra-thin (1.7 μm) Si-substrate top-chip with a Fe/Ni-permalloy film providing magnetic screening between the top- and bottom chip in 3D IC system in package approach.[64]

RESISTORS

Applications of on-chip thin film resistors, especially in analog and mixed signal circuits

- Clock and bus terminators
- Precision resistor arrays and networks
- Voltage dividers

Typical resistor requirements

- Excellent matching properties
- Precision resistance control
- High voltage linearity (low voltage coefficients)
- Low temperature coefficients
- Low 1/f current noise
- High Q values (low parasitics)

Process integration challenges

- Moderate and tunable sheet resistance
- Excellent thickness control (deposition uniformity)
- Modular integration scheme
- Good etch selectivity to dielectrics
- Use standard interconnect materials

Relatively little literature has been published on the integration of interconnect based thin film resistors. One interesting approach was the multi-functional use of a PVD TaN based MIM capacitor base plate as a precision TaN thin film resistor with varying resistivity based on different film stoichiometries. Low voltage linearity and temperature coefficients and excellent matching properties were reported for the TaN film.[27] Another approach using PVD WSi_x as a metallization-based resistor with reasonably good temperature coefficient values was also reported.[65]

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ENDNOTES

NEW INTERCONNECT CONCEPTS AND RADICAL SOLUTIONS

PASSIVE DEVICES

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