INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

LITHOGRAPHY

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LITHOGRAPHY

SCOPE

In 2005 and beyond, maintaining the rapid pace of half pitch reduction requires overcoming the challenge of improving and extending the incumbent optical projection lithography technology while simultaneously developing alternative, next generation lithography technologies to be used when optical projection lithography is no longer more economical than the alternatives. Significant technical challenges exist in extending optical projection lithography at 193 nm wavelength using immersion lenses and also in developing novel next generation alternative approaches. Not only is it necessary to invent technical solutions to very challenging problems, it is critical that die costs remain economical with rising design costs, process development costs, mask costs, and cost of ownership of the tool and process. Extending optical projection lithography and developing next generation lithographic technology requires advances in these areas:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask-making equipment, and materials
- Metrology equipment for critical dimension measurement, overlay control, and defect inspection

This chapter provides a fifteen-year roadmap defining lithography's difficult challenges, technology requirements, and potential solutions. Additionally, this chapter defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for *Design, Front End Processing* (FEP), *Process Integration, Devices, and Structures* (PIDS), *Environment, Safety, and Health* (ESH), *Yield Enhancement*, *Factory Integration*, *Metrology*, and *Modeling and Simulation*.

The key requirements of lithography for manufacturing integrated circuits are summarized below:

- *Critical Dimension (CD) Control*—The size of many features in a design needs to be precisely controlled. CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer. CD control is required for obtaining adequate transistor, interconnect and consequently overall circuit performance.
- *Overlay*—The placement of the image with respect to underlying layers needs to be accurate on each integrated circuit in all locations to achieve adequate yield.
- *Defect Control*—The desired pattern must be present in all locations, and no additional patterns should be present. No particles should be added to the wafer during the lithography process.
- *Low Cost*—The cost of tools, resist and masks needs to be as low as possible while still meeting the CD control, overlay, and defect control requirements. To minimize cost, the lithography step should be performed as quickly as possible. Masks should be used to expose as many wafers as possible. Equipment needs to be reliable and ready to expose wafers when needed.

Since each of the many layers in a device requires patterning, the lithography process is a major part of the cost of manufacturing integrated circuits. Typically, at least four layers are critical layers requiring the most advanced lithographic tool available. These include: the isolation or active layer; the gate layer; the contact hole layer to contact the gates, source and drain to the first interconnect layer; and the first interconnect wiring layer. Several of the initial interconnect wiring and via layers and the channel implant layers might also be exposed on the most advanced lithography tools. Novel device structures might also introduce several additional critical layers. Lithography, including masks and resist, and associated metrology currently comprises 30–40% of the entire cost of semiconductor manufacturing. This fraction depends strongly on the product mix, volume of ICs in demand per design, and age of equipment in the factory. Cost of ownership (CoO) modeling is often used to quantitatively compare lithography technology and or process options. The cost of a process is typically measured in cost per wafer, per process layer, or per die. Cost of lithography is usually quantified in terms of cost per good wafer level exposed. The cost of ownership of lithography, expressed as cost per wafer level exposed (PWLE), can be quantified as:

$$C_{pwle} = (C_e + C_l + C_f + C_c + C_r\, Q_{rw}\, N_c) / N_g + C_m / N_{wm}$$

where:

C_{pwle} = cost per wafer level exposure

C_e = yearly cost of exposure, coating, and pattern transfer equipment (including depreciation, maintenance, and installation)
C_l = yearly cost of labor
C_f = yearly cost of cleanroom space
C_c = cost of other consumables (condenser, laser diodes)
C_r = cost of resist
Q_{rw} = quantity of resist used per wafer
N_c = number of wafers coated
T_{net} = net throughput = raw throughput * utilization
N_g = number of good wafers levels exposed (GWLE) = $\int T_{net}\, Y_L\, dt$; Y_L = yield of lithography, t=time
C_m = cost of mask
N_{wm} = number of wafers exposed per mask

C_e is determined from the price of the equipment including installation costs. This cost is allocated to each year using depreciation, which is typically assumed to be accounted for as straight-line depreciation over five years. In practice, the terms that usually have the greatest effect on cost of ownership are C_e, T_{net}, C_m, and N_{wm}. Figure 66 shows the sensitivity of the normalized cost of ownership to these many factors. Yield has the largest effect followed by throughput (T_{net}) and mask usage (N_{wm}).

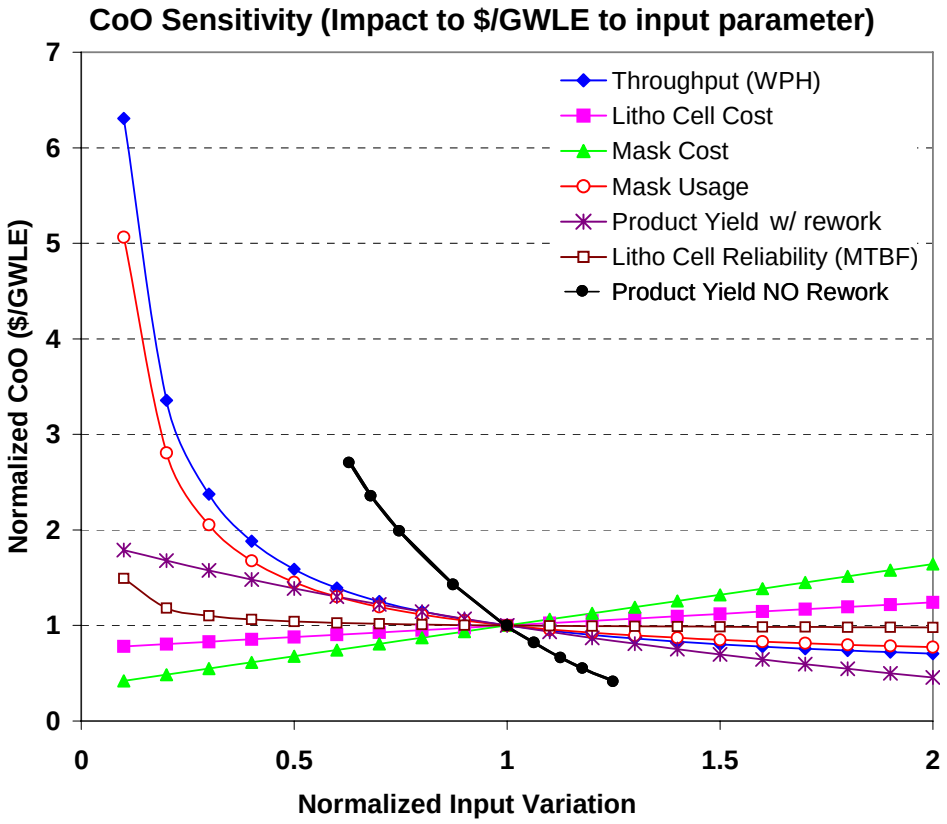


Figure 66 Plot of Normalized Cost of Ownership as a Function of Several Normalized Input Variables

Since the earliest days of the microelectronics industry, optical lithography has been the mainstream technology for volume manufacturing, and it is expected to continue as such through the 45 nm half-pitch technology generation. The resolution of optical projection lithography is limited by diffraction as described by the Rayleigh equation. The minimum half pitch, R, resolvable for a diffraction limited optical projection system is given by:

$$R = k_1 \frac{\lambda}{NA} \quad [1]$$

where λ is the exposure wavelength and NA is the numerical aperture, which equals $n\sin\alpha_0$ where n is the minimum index of refraction of the imaging medium, final lens element or resist. α_0 is the maximum half angle of rays focused by the lens to the image when the lens is used to image in air or vacuum. K_1 is a process dependent factor determined mainly by the resist capability, the tool control, reticle pattern adjustments and the process control. It should be noted that lines may be printed at dimensions smaller than the minimum half pitch. The physical limitation of lithography is the minimum distance between adjacent features, namely pattern pitch.

Focusing errors, or defocus, lower the definition and contrast of the image, alter the CDs in resist and limit exposure latitude. The focus latitude, or depth of focus (DOF), expected at a single point in a stepper field is[1]:

$$DOF = k_3 \frac{\lambda}{n \sin^2 \left[\frac{1}{2} \sin^{-1} \left(\frac{1}{n} \sin \alpha_o \right) \right]} \quad [2]$$

When n=1 and when NA<0.8, depth of focus becomes:

$$DOF \approx k_2 \frac{\lambda}{NA^2} \quad [3]$$

Constants, k_2 and k_3, are dependent on the tool, process, pattern size and pattern geometry. Therefore, the trends in optical lithography are towards using smaller wavelength, higher NA imaging systems and smaller k_1 values to allow the printing of more dense patterns. The resolution and depth of focus scaling of lithography technologies using 193 nm, 193 nm with immersion and extreme ultraviolet (EUV) lithography projection imaging systems are governed by equations 1–3.

To continue as the dominant technique for leading edge critical layer lithography, the application of resolution enhancement techniques (RET) such as off-axis illumination (OAI), phase shifting masks (PSM), and optical proximity corrections (OPC) are being used with imaging systems at 193 nm wavelength. In addition to resolution enhancement techniques, lenses with increasing numerical apertures, and decreasing aberrations will be required to extend the life of optical lithography. Liquid immersion imaging with a fluid between the final lens element and the wafer is also being used as a means of extending optical lithography. Table 74 shows the progression of RET and techniques being used to extend optical lithography. It becomes much more difficult to implement OPC and resolution enhancement at each successive technology generation.

1. [1] Burn Lin, "The k3 coefficient in nonparaxial λ/NA scaling equations for resolution, depth of focus, and immersion lithography," *Journal of Microlithography, Microfabrication and Microsystems* **1**(1), 7–12, April 2002.

Table 74 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography

MPU M1 contacted ½ pitch	*210 nm*	*160 nm*	*120 nm*	*90 nm*	*65 nm*	*45 nm*
k_1 Range [A]	*0.51–0.64*	*0.48–0.52*	*0.47–0.53*	*0.40–0.43*	*0.31–0.40*	*0.28–0.31*
Design rules	Minor restriction	Allow OPC and PSM, SRAF	Litho friendly design rules			
Restrictions (cumulative)	Minimum pitch, spacing and linewidth		Pitch and orientation	Contact locations, library cells checked for OPC compatibility and printability	Features on grid?, Restricted feature set?	
Masks (Optical proximity correction)	Rule-based OPC, MBOPC for gate, custom OPC for memory cells	Model-based OPC (MBOPC) on critical layers, SRAF on gate layer	Model-based OPC w /SRAF on critical layers, verification of entire corrected layout with simulation		Model-based OPC with vector simulation, SRAF, polarization corrections	Model-based OPC with vector simulation, SRAF, polarization corrections, variation of OPC intensity by location in circuit?, magnification increase?
(Gate and M1 layer mask type)		cPSM and EPSM		APSM, EPSM and hiT EPSM	APSM, hiT EPSM, dual dipole?	APSM, hiT EPSM, double exposure with 2× larger pitch
(Contacts/vias layers mask type)		EPSM		APSM, EPSM, HiT PSM		
Resist	Custom by layer type					
Thickness	<500 nm	<400 nm	<350 nm	<280 nm	<225 nm	<160 nm
Substrate	ARC	ARC, hard masks		ARC, hard masks, top coats		
Etch		Post development resist width reduction				
Tool		Selection based on aberrations, automated NA/sigma control		Aberration monitoring		
(Illumination)	Conventional, annular illumination	Off-axis illumination	Quadrupole	Custom illumination	Custom illumination, polarization optimization	Custom illumination, polarization optimization
(Dose control)		Cross wafer dose adjustments	Dose adjustment across the wafer and along scan			
(Process control (CD and overlay)	Offsets from previous lots	Automated process control with downloaded offsets			Automated process control with downloaded offsets, metrology integrated in lithography cell	

MBOPC—model based optical proximity correction cPSM—complementary PSM APSM—alternating PSM
EPSM—embedded PSM HiT—high transmission ARC—antireflection coating SRAF—sub-resolution assist features

Note for Table 74:
[A] Assumes that optical and immersion optical projection lithography is used.

The requirements of 32 nm half pitch and beyond are viewed as likely to be beyond the capabilities of optical lithography at 193 nm wavelength unless high-index fluids, high-index lens materials, and higher-index resist are developed. Another option to extend the lifetime of optical projection lithography with immersion to 32 nm half pitch and beyond is to decompose the pattern to use two or more masks. However, this technique must be less expensive than alternative technologies. Extension of the Roadmap will probably require the development of next-generation lithography (NGL) technologies, such as EUV, maskless (ML2), and imprint lithography. Because next generation lithographies will require the development of substantially new infrastructure, a key challenge is to implement them as economical manufacturing solutions.

DIFFICULT CHALLENGES

The ten most difficult challenges to the continued shrinking of minimum half pitch are shown in Table 75. Mask-making capability and cost escalation continue to be critical to future progress in lithography and will require continued focus. As a consequence of prior aggressive Roadmap acceleration—particularly the MPU gate linewidth (post etch), and increased mask error enhancement factor (MEEF) associated with low k_1 lithography—mask linewidth control appears as a particularly significant challenge going forward. For example, in the 1997 roadmap the 70 nm requirements showed 4× masks needing 9 nm of CD control for isolated lines and 14 nm for contacts. The 2005 requirements are 2.6 nm for isolated lines and 3.0 nm for contacts. Mask equipment and process capabilities are in place for manufacturing masks with complex OPC and PSM, while mask processes for post-193 nm technologies are in research and development. The difficulty of defect control, CD control, and pattern placement accuracy increases significantly with each technology generation, requiring the development of ever more capable mask fabrication equipment. The number of leading-edge mask fabrication facilities is small, making it difficult for suppliers of these tools to develop the increasingly complex tools. Mask damage from electrostatic discharge (ESD) has long been a concern, and it is expected to be even more problematic as mask feature sizes shrink. Progressive defect formation has become an increasing problem with organic and inorganic deposits forming on masks after exposure of many wafers.

Although 1×, 5×, and 10× magnification factors have been used, the predominant magnification factor of 4× maximizes the printed field on the wafer that can be accommodated with a single mask and balances the challenge of mask fabrication. Several issues are driving the renewed discussion of increasing magnification factor. Mask costs have increased significantly due to the prevalent use of complex RET. Masks with higher demagnification might be significantly less expensive than 4× masks. The use of NA>0.9 in air and proposed use of NA>1.0 with immersion lithography have made lens size and volume increase dramatically. Stage speeds and exposure tool productivity have significantly increased, permitting better throughput at smaller field size. Furthermore, mask feature dimensions at 4× are becoming comparable to the wavelength, and these features partially polarize the transmitted radiation. When feature sizes are in the range of 0.5 to 2 times the wavelength, the mask patterns partially polarize the transmitted radiation in the transverse electric (TE) polarization state. This polarization will be manifested as dose variation in systems that do not have purely and uniformly polarized illumination of the mask at all locations. Software for designing resolution-enhanced masks, such as embedded or alternating phase shift masks, will require more complex rigorous electromagnetic models. Polarization by mask features might eventually lead the industry to strongly consider using greater than a 4× demagnification factor. Besides lowering mask cost and lens cost, the usable exposure field size will decrease at higher magnification, impacting the size of chip designs that can be fabricated without using stitching.

To achieve demanding CD control tolerances, resolution enhancement techniques, design restrictions, and automated process control are being employed, as shown in Table 74. To further enable the extension of optical lithography, new practices are required to better comprehend the increasing variation of critical dimensions as a fraction of the feature size in the design process. These practices are usually referred to as “design for manufacturing (DFM)” practices. DFM practices will allow designers to account for manufacturing variations during circuit design optimization, and DFM will allow the IC fabrication process to be optimized to provide highest performance and minimal cost. Ultimately, the designer could optimize the circuit with knowledge of all physical variations in the fabrication process and their statistical distribution. At the simplest level, designers are being made aware of library cells that have yielded well in manufacturing. Furthermore, simulations of the lithography, etch, and CMP processes are being used to examine the full chip area for weak spots in the layout that are most susceptible to manufacturing variations. Coordinates of these weak points are provided to mask and wafer CD metrology tools. Focus and exposure are optimized for printing weak spot regions with maximum process latitude rather than for test structures. The topographical features of these printed weak spots will need to be evaluated with pattern fidelity metrology. These weak spot locations are then targeted for layout modification and monitoring in the manufacturing process. Automation of software analysis of weak spots in design and feedback to physical layout of cells is being aggressively pursued by electronic design automation (EDA) suppliers. DFM tools and techniques will be essential to minimize mask revisions and achieve adequate yield in the wafer fab. See the *Design Chapter* for more information on DFM.

While lithography has long helped significantly reduce cost per function of integrated circuits by enabling patterning at higher density, maintaining historical levels of cost control and return-on-investment (ROI) are becoming increasingly difficult. These issues of mask and lithography costs are relevant to optical as well as next-generation lithography. To be extended further, optical lithography will require new resists that will provide both good pattern fidelity when exposed under immersion in water or perhaps alternative fluids and that have improved performance during etch. More complicated masks will be required, and fabricating these masks will require new and improved mask-making equipment

and materials. Transitioning to 450 mm diameter wafers will require advances in exposure tool stage design and in coating technology on tracks. These improvements will require additional development expenditures.

MPU gate CD control requirements will stress many other aspects of lithography process control, including lenses, resist processing equipment, resist materials, and metrology. Process control, particularly for overlay and CD, is a major challenge. It is unclear whether metrology, which is fundamental to process control, will be adequate to meet future requirements as needed for both development and volume manufacturing. Resist line edge roughness (LER) is becoming significant, as gate linewidth control becomes comparable to the size of a polymer unit. Next-generation lithography will require careful attention to details as the exposure tools are based upon approaches that have never been used before in manufacturing. These tools must be developed and proven to be capable of meeting the reliability and utilization requirements of cost-effective manufacturing.

The introduction of immersion lithography has brought many new challenges. The immersion fluid must be free from bubbles that may be caused by the scanning process, by exposure, or by the fluid delivery, recovery, and recirculation system. The immersion fluid might also remain on the wafer after exposure and result in staining. Resists must be compatible with the fluid or topcoat. To enable the extension of immersion lithography at 193 nm wavelength beyond 45 nm half-pitch patterning, fluids with higher index than water (such as >1.44) and lens materials with higher index than CaF_2 or fused silica (>1.56) are required. These materials need to meet all requirements for imaging and compatibility with the immersion lithography environment.

Extreme ultraviolet lithography is expected to be used in manufacturing starting at 32 nm half pitch and possibly for 45 nm half pitch. EUV lithography is a projection optical technology that uses 13.5 nm wavelength. At this wavelength, all materials are highly absorbing, so the imaging system is composed of mirrors coated with multilayer structures designed to have high reflectivity at 13.5 nm wavelength. The significant technical hurdles for implementing EUV lithography are outlined in Table 75. These include: developing mask blank fabrication processes with low defect density; developing EUV sources with high output power and sufficient lifetime for surrounding collector optics; controlling contamination of all mirrors in the illuminator and projection optics; fabrication of optics with figure and finish compatible with high quality imaging at 13.5 nm wavelength; resist with sufficiently low line width roughness and low exposure dose, and protection of masks from defects without pellicles. EUV lithography will also be mixed with optical lithography, so appropriate strategies need to be developed for overlay.

In the longer term, even more demanding process requirements for overlay, defect, and CD control will continue to pose challenges for process control, resist development, and mask development. The possible use of maskless lithography will probably require die-to-database inspection of wafers to replace die-to-database inspection of masks. Imprint lithography templates have the same dimensions as the wafer pattern, making mask fabrication more challenging. Resist materials will also require significant improvements. To extend immersion lithography, higher index of refraction will be eventually required. Alternatives to perfluoroalkyl sulfonate (PFAS) compounds used in photoacid generators and antireflection coatings should be found. Acid diffusion in chemically amplified resist might limit the ultimate minimum half pitch achievable with high sensitivity resists unless diffusion length is reduced or new methods of sensitizing resists are found. Resist materials with inherently high dimensional control for uniform CD and low line width roughness patterning will also be needed.

Table 75 Lithography Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD, and defect control for masks
	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Understanding polarization effects at the mask and effects of mask topography on imaging and optimizing mask structures to compensate for these effects
	Eliminating formation of progressive defects and haze during exposure
	Determining optimal mask magnification ratio for <45 nm half pitch patterning with 193 nm radiation and developing methods, such as stitching, to compensate for the potential use of smaller exposure fields
	Development of defect free 1× templates
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	Sufficient lifetime for exposure tool technologies
	Resources for developing multiple technologies at the same time
	ROI for small volume products
	Stages, overlay systems and resist coating equipment development for wafers with 450 mm diameter
Process control	Processes to control gate CDs to < 4 nm 3σ
	New and improved alignment and overlay control methods independent of technology option to <11 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 50 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Control of and correction for flare in exposure tool, especially for EUV lithography
	Lithography friendly design and design for manufacturing (DFM)
Immersion lithography	Control of defects caused in immersion environment, including bubbles and staining
	Resist chemistry compatibility with fluid or topcoat and development of topcoats
	Resists with index of refraction > 1.8
	Fluid with refractive index > 1.65 meeting viscosity, absorption, and fluid recycling requirements
	Lens materials with refractive index >1.65 meeting absorption and birefringence requirements for lens designs
EUV lithography	Low defect mask blanks, including defect inspection with < 30 nm sensitivity and blank repair
	Source power > 115 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Resist with < 3 nm 3σ LWR, < 10 mJ/cm^2 sensitivity and < 40 nm ½ pitch resolution
	Fabrication of optics with < 0.10 nm rms figure error and < 10% intrinsic flare
	Controlling optics contamination to achieve > five-year lifetime
	Protection of masks from defects without pellicles
	Mix and match with optical lithography

Table 75 Lithography Difficult Challenges (continued)

Difficult Challenges < 32 nm	*Summary of Issues*
Mask fabrication	Defect-free masks, especially for 1× masks for imprint and EUVL mask blanks free of printable defects
	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair), especially for 1× masks
	Mask process control methods and yield enhancement
	Protection of EUV masks and imprint templates from defects without pellicles
	Phase shifting masks for EUV
Metrology and defect inspection	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3σ
	Metrology for achieving < 2.8 nm 3σ overlay error
	Defect inspection on patterned wafers for defects < 30 nm, especially for maskless lithography
	Die-to-database inspection of wafer patterns written with maskless lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective optical and post-optical masks
	Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products
Gate CD control improvements and process control	Development of processes to control gate CD < 1.3 nm 3σ with < 1.5 nm 3σ line width roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3σ overlay error, especially for imprint lithography
	Process control and design for low k_1 optical lithography
Resist materials	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Limits of chemically amplified resist sensitivity for < 32 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Tables 76a and b)
- Resist Requirements (Tables 77a, b, and c)
- Mask Requirements (Tables 78a–f)

Requirements for small MPU gate length after etch create significant challenges for metrology and process control. Controlling critical dimensions to historically required ± 10% tolerances is becoming increasingly difficult. As described in the Crosscut section below, the CD control requirement for MPU gates in the Roadmap has been increased from ± 10% to ± 12%. The difference between the printed pattern width in resist from contacts and MPU gates has also been increased. Post development linewidth reduction techniques are becoming more prevalent and more capable. Printing larger features in resist improves CD control by providing for a larger process window for the lithography process. Integrated circuit manufacturers are also modifying design rules to make the patterning task more feasible. Metrology will play a critical role in defining these lithography friendly design rules. The effects of line edge and line width roughness (LWR) are also becoming increasingly apparent in device performance; therefore, metrology tools need to be modified to accurately measure these variations as well. High frequency line width roughness affects dopant concentration profiles and affects interconnect wire resistance. Line width roughness at larger spatial frequency results in variations of transistor gate length over the active region of the device. This variation increases leakage of transistors and causes a variation of the speed of individual transistors, which in turn leads to IC timing issues. Because of the particular challenges associated with imaging contact holes, the size of contact holes after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gate length. The size of the bias achieved between the developed and etched contact holes has increased since 2003. Refer to Table 76a and b for the technology requirements for lithography.

Photoresists need to be developed that provide good pattern fidelity, good line width control, low line width roughness, and few defects. As feature sizes get smaller, defects and monomers will have comparable dimensions with implications for the filtering of resists. Refer to Tables 77a–c.

The requirements for masks are for critical layers. Early volumes are assumed to be relatively small and difficult to produce. The masks for all next-generation lithographies (NGL) are different from optical masks, and no NGL technology can support a pellicle. Because the requirements for NGL masks are substantially different than those for optical lithography, separate tables have been included for optical masks, EUV masks, and imprint templates (Tables 78a and b, 78c and d, 78e and f, respectively). The latter tables covering EUV and imprint requirements note the requirements that are common with optical masks and those which are specific to each technology. Imprint may take several forms, and requirements specific to ultraviolet nanoimprint lithography (UV-NIL), in which UV radiation is used to cure the liquid filling the template, are listed. EUV masks must also have tight flatness control, and there are additional requirements for various parameters associated with reflectivity of EUV masks. EUV mask blanks must be free of small defects, requiring development of new inspection tools and low defect fabrication processes. Imprint templates have surface relief features that are the same size as the wafer features, but the area that needs to be controlled for CD, pattern placement, and defects is 16 times smaller than for comparable 4× masks for other technologies. Inspection for defects on these masks will be difficult, though. Solutions for protecting the masks from defects added during storage, handling, and use in the exposure tool need to be developed and tested because there are no known pellicle options for EUV masks or imprint templates. These different NGL mask requirements can be expected to exacerbate, rather than relieve, the high costs associated with masks that are already being encountered with optical masks.

CD control and overlay tolerances are the most difficult requirements to achieve. Overlay tolerances have become more demanding to fabricate memory circuits with higher yield. To reduce the effect of lens distortion on overlay error, a single exposure tool may be used to print multiple critical layers for the same wafers. Both feed-back and feed-forward approaches need to be supported by process tools (steppers/scanners and tracks). The automation framework and CIM system needs to comply with a large set of correcting models and algorithms, which might be highly non-linear. The requirements for automated process control (APC) are discussed in more detail in the Crosscut section with Factory Integration of this chapter.

Table 76a Lithography Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	35	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	15	13	11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
MPU									
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
*MPU physical gate length (nm) **	32	28	25	23	20	18	16	14	13
Contact in resist (nm)	111	97	84	73	64	56	50	44	39
Contact after etch (nm)	101	88	77	67	58	51	45	40	36
*Gate CD control (3 sigma) (nm) [B] ***	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
Chip size (mm^2)									
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858	858	858
Number of mask levels MPU	33	33	33	35	35	35	35	35	35
Number of mask levels DRAM	24	24	24	24	24	26	26	26	26
Wafer size (diameter, mm)	300	300	300	300	300	300	300	450	450

** MPU physical gate length numbers and colors are determined by several working groups and the ORTC.*
*** Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

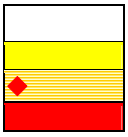
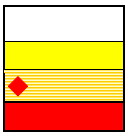


Table 76b Lithography Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
DRAM and Flash							
DRAM ½ pitch (nm)	28	25	22	20	18	16	14
Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
Contact in resist (nm)	31	28	25	22	20	18	16
Contact after etch (nm)	28	25	23	20	18	16	14
Overlay [A] (3 sigma) (nm)	5.1	4.5	4.0	3.6	3.2	2.8	2.5
CD control (3 sigma) (nm) [B]	3.0	2.6	2.3	2.1	1.9	1.7	1.5
MPU							
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
MPU gate in resist (nm)	19	17	15	13	12	11	9
*MPU physical gate length (nm) **	11	10	9	8	7	6	6
Contact in resist (nm)	35	31	28	25	22	20	18
Contact after etch (nm)	32	28	25	23	20	18	16
Gate CD control (3 sigma) (nm) [B]	1.2	1.0	0.9	0.8	0.7	0.7	0.6
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
Chip size (mm^2)							
Maximum exposure field height (mm)	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858
Number of mask levels MPU	37	37	39	39	39	39	39
Number of mask levels DRAM	26	26	26	26	26	26	26
Wafer size (diameter, mm)	450	450	450	450	450	450	450

** MPU physical gate length numbers and colors are determined by several working groups and the ORTC.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 76a and b:
[A] Overlay (nm)—Overlay is a vector component (in X and Y directions) quantity defined at every point on the wafer. It is the difference, O, between the vector position, P1, of a substrate geometry, and the vector position of the corresponding point, P2, in an overlaying pattern, which may consist of resist. O=P1-P2. The difference, O, is expressed in terms of vector components in the X and Y directions, and the value shown is three times the standard deviation of overlay values on the wafer.
[B] CD control (nm)—Control of critical dimensions compared to mean linewidth target at all pattern pitch values, including errors from all lithographic sources (due to masks, imperfect optical proximity correction, exposure tools, and resist) at all spatial length scales (e.g., includes errors across exposure field, across wafer, between wafers and between wafer lots)

Table 77a Resist Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Flash ½ pitch (nm) (un-contacted poly)	*76*	*64*	*57*	*51*	*45*	*40*	*36*	*32*	*28*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU physical gate length (nm) [after etch]	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU gate in resist length (nm)	**53**	**47**	**42**	**38**	**33**	**30**	**27**	**24**	**21**
*Resist Characteristics **									
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	**3.3**	**2.9**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**	**1.5**	**1.3**
*Resist thickness (nm, single layer) ****	**150–265**	**125–225**	**110–200**	**100–180**	**90–160**	**80–145**	**70–130**	**60–115**	**55–100**
PEB temperature sensitivity (nm/C)	**2**	**1.75**	**1.75**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1**
Backside particle density (particles/cm^2)	**0.57**	**0.57**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**
Back surface particle diameter: lithography and measurement tools (nm)	**160**	**120**	**120**	**120**	**100**	**100**	**100**	**100**	**75**
Defects in spin-coated resist films (#/cm^2) †	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
Minimum defect size in spin-coated resist films (nm)	**50**	**45**	**40**	**35**	**30**	**30**	**20**	**20**	**20**
Defects in patterned resist films, gates, contacts, etc. (#/cm^2)	**0.05**	**0.04**	**0.04**	**0.03**	**0.03**	**0.03**	**0.02**	**0.02**	**0.02**
Minimum defect size in patterned resist (nm)	**50**	**45**	**40**	**35**	**30**	**30**	**20**	**20**	**20**
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	**4.2**	**3.8**	**3.4**	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**	**1.7**

† *Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Table 77b Resist Requirements—Long-term Years

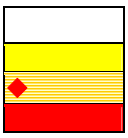
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash ½ pitch (nm) (un-contacted poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU physical gate length (nm) [after etch]	*11*	*10*	*9*	*8*	*7*	*6*	*6*
MPU gate in resist length (nm)	**19**	**17**	**15**	**13**	**12**	**11**	**9**
*Resist Characteristics **							
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) ***	**1.2**	**1.0**	**0.9**	**0.8**	**0.7**	**0.7**	**0.6**
*Resist thickness (nm, single layer) ****	**50–90**	**45–80**	**40–75**	**35–65**	**30–60**	**25–50**	**25–45**
PEB temperature sensitivity (nm/C)	**1**	**1**	**1**	**1**	**1**	**11**	**11**
Backside particle density (particles/cm^2)	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**	**0.28**
Back surface particle diameter: lithography and measurement tools (nm)	**75**	**75**	**50**	**50**	**50**	**50**	**50**
Defects in spin-coated resist films† (#/cm^2)	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
Minimum defect size in spin-coated resist films (nm)	**20**	**10**	**10**	**10**	**10**	**10**	**10**
Defects in patterned resist films, gates, contacts, etc. (#/cm$^{2)}$	**0.02**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
Minimum defect size in patterned resist (nm)	**20**	**10**	**10**	**10**	**10**	**10**	**10**
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	**1.5**	**1.3**	**1.2**	**1.1**	**0.9**	**0.8**	**0.8**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Table 77a and b:
Exposure Dependent Requirements
** Resist sensitivity is treated separately in the second resist sensitivity table.*
*** Indicates whether the resist has sufficient resolution, CD control, and profile to meet the resolution and gate CD control values.*
**** Resist thickness is determined by the aspect ratio range of 2.0:1 to 3.5:1, limited by pattern collapse.*
***** Linked with resolution.*
****** LWR_{Lf} is 3σ deviation of spatial frequencies from 0.5 μm^{-1} to 1/(2*MPU ½ Pitch).*
Note: Standard deviation is determined by biased estimate (corrected for SEM noise) of linewidth variation over a greater than or equal 2 µm measured at less than or equal 4 nm intervals.
† Defects in coated films are those detectable as physical objects, such as pinholes, that may be distinguished from the resist film by optical detection methods.
Other requirements:
[A] Need for a positive tone resist and a negative tone resist will depend upon critical feature type and density.
[B] Feature wall profile should be 90 ± 2 degrees.
{C] Thermal stability should be ≥ 130 °C.
[D] Etching selectivity should be > that of poly hydroxystyrene (PHOST).
[E] Upon removal by stripping there should be no detectible residues.
[F] Sensitive to basic airborne compounds such as amines and amides. Clean handling space should have < 1000 pptM of these materials.
[G] Metal contaminants < 5 ppb.
[H] Organic material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 193 nm lithography tool is < 1e12. Value for EUV lithography tool is < 5e13. Values for electron beam are being determined.
[I] Si containing material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 193 nm lithography tool is < 1e8. Value for EUV lithography tool is < 5e13. Values for electron beam are being determined.

Table 77c Resist Sensitivities

Exposure Technology	*Sensitivity*
248 nm	**10–50 mJ/ cm^2**
193 nm	**20–50 mJ/ cm^2**
Extreme Ultraviolet at 13.5 nm	**5–15 mJ/ cm^2**
High Voltage Electron Beam (50–100 kV) ********	**5–10 µC/ cm^2**
Low Voltage Electron Beam (1–2 kV) ********	**0.2–1.0 µC/ cm^2**

***** Linked with resolution*

Table 78a Optical Mask Requirements—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
DRAM/Flash CD control (3 sigma) (nm)	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
MPU physical gate length (nm)	32	28	25	23	20	18	16	14	13
Gate CD control (3 sigma) (nm) [B]	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
Overlay (3 sigma) (nm)	15	13	11	10	9	8	7	6	6
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Mask magnification [B]	4	4	4	4	4	4	4	4	4
Mask nominal image size (nm) [C]	214	191	170	151	135	120	107	95	85
Mask minimum primary feature size [D]	150	133	119	106	94	84	75	67	59
Mask sub-resolution feature size (nm) opaque [E]	107	95	85	76	67	60	54	48	42
Image placement (nm, multipoint) [F]	9	8	7	6.1	5.4	4.8	4.3	3.8	3.4
CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
MEEF isolated lines, binary or attenuated phase shift mask [G]	1.4	1.4	1.6	1.8	2	2.2	2.2	2.2	2.2
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] *	3.8	3.4	2.6	2.1	1.7	1.3	1.2	1.1	1.0
MEEF dense lines, binary or attenuated phase shift mask [G]	2	2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	7.1	6.0	4.8	4.3	3.8	3.4	3.0	2.7	2.4
MEF contacts [G]	3	3	3.5	4	4	4	4	4	4
CD uniformity (nm, 3 sigma), contact/vias [K] *	4.7	4.0	3.0	2.4	2.1	1.9	1.7	1.5	1.3
Linearity (nm) [L]	13	11	10	9	8	7.2	6.4	5.6	5.1
CD mean to target (nm) [M]	6.4	5.6	5.2	4.6	4.0	3.6	3.2	2.8	2.6
Defect size (nm) [N] *	64	56	52	46	40	36	32	28	26
Blank flatness (nm, peak-valley) [O]	500	500	250	250	250	175	175	175	150
Data volume (GB) [P]	260	328	413	520	655	825	1040	1310	1651
Mask design grid (nm) [Q]	4	2	2	2	2	2	2	2	2
Attenuated PSM transmission mean deviation from target (± % of target) [R]	5	4	4	4	4	4	4	4	4
Attenuated PSM transmission uniformity (±% of target) [R]	4	4	4	4	4	4	4	4	4
Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3	3	3	3	3	3	3
Alternating PSM phase mean deviation from nominal phase angle target (± degree) [S]	2	1.5	1.5	1	1	1	1	1	1
Alternating PSM phase uniformity (± degree) [T]	2	1	1	1	1	1	1	1	1
Mask materials and substrates	Absorber/attenuator on fused silica								
	Pellicle for optical masks for exposure wavelengths down to 193 nm, including masks for 193 nm immersion.								

** Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table 78b Optical Mask Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
DRAM/Flash CD control (3 sigma) (nm)	*3.0*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
MPU physical gate length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Gate CD control (3 sigma) (nm) [B]	*1.2*	*1.0*	*0.9*	*0.8*	*0.7*	*0.7*	*0.6*
Overlay (3 sigma) (nm)	*5*	*5*	*4*	*4*	*3*	*3*	*3*
Contact after etch (nm)	*28*	*25*	*23*	*20*	*18*	*16*	*14*
Mask magnification [B]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Mask nominal image size (nm) [C]	**76**	**67**	**60**	**54**	**48**	**42**	**38**
Mask minimum primary feature size [D]	**53**	**47**	**42**	**37**	**33**	**30**	**26**
Mask sub-resolution feature size (nm) opaque [E]	**38**	**34**	**30**	**27**	**24**	**21**	**19**
Image placement (nm, multipoint) [F]	**2.7**	**2.4**	**2.2**	**1.9**	**1.7**	**1.5**	**1.4**
CD uniformity allocation to mask (assumption)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
MEEF isolated lines, binary or attenuated phase shift mask [G]	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**0.9**	**0.8**	**0.7**	**0.6**	**0.5**	**0.5**	**0.4**
MEEF dense lines, binary or attenuated phase shift mask [G]	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	**2.1**	**1.9**	**1.7**	**1.5**	**1.4**	**1.2**	**1.1**
MEF contacts [G]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
CD uniformity (nm, 3 sigma), contact/vias [K]	**1.2**	**1.1**	**0.9**	**0.8**	**0.7**	**0.7**	**0.6**
Linearity (nm) [L]	**4.5**	**4.0**	**3.5**	**3.2**	**2.9**	**2.6**	**2.2**
CD mean to target (nm) [M]	**2.2**	**2.0**	**1.8**	**1.6**	**1.4**	**1.3**	**1.1**
*Defect size (nm) [N] **	**22**	**20**	**18**	**16**	**14**	**13**	**11**
Blank flatness (nm, peak-valley) [O]	**150**	**150**	**125**	**125**	**125**	**100**	**100**
Data volume (GB) [P]	**2080**	**2621**	**3302**	**4160**	**5241**	**6604**	**8320**
Mask design grid (nm) [Q]	**2**	**2**	**2**	**1**	**1**	**1**	**1**
Attenuated PSM transmission mean deviation from target (± % of target) [R]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Attenuated PSM transmission uniformity (± % of target) [R]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Attenuated PSM phase mean deviation from 180° (± degree) [S]	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Alternating PSM phase mean deviation from nominal phase angle target (± degree) [S]	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Alternating PSM phase uniformity (± degree) [T]	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Mask materials and substrates	**Absorber/attenuator on fused silica**						
	Pellicle for optical masks for exposure wavelengths down to 193 nm, including masks for 193 nm immersion.						

Manufacturable solutions exist, and are being optimized

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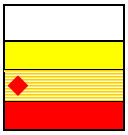
Manufacturable solutions are NOT known



Notes for Table 78a and b:
[A] Wafer Minimum Line Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
[B] Magnification—Lithography tool reduction ratio.
[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.
[E] Mask Sub-Resolution Feature Size—The minimum width of non-printing features on the mask such as sub-resolution assist features.
[F] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error. These values do not comprehend additional image placement error induced by pellicle mount and mask clamping in the exposure tool.
[G] The CD error on the wafer is directly proportional to the CD error on the mask where mask error enhancement factor (MEEF) is the constant of proportionality. An MEEF value greater than unity therefore imposes a more stringent CD uniformity requirement on the mask to maintain the CD uniformity budget on the wafer.
[H] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and isolated features on a binary mask.
[I] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a quartz shifter phase mask.
[J] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a binary or attenuated phase shift mask.
[K] CD Uniformity—The three-sigma deviation of square root of contact area on a mask through multiple pitches.
[L] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are equal to the smallest sub-resolution assist mask feature and up to three times the minimum wafer half pitch multiplied by the magnification.
[M] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.
[N] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation. Printable 180-degree phase defects are 70% smaller than the number shown.
[O] Blank Flatness—Flatness is nanometers, peak-to-valley across the 140 mm × 140 mm central area image field on a 6-inch × 6-inch square mask blank. Flatness is derived from wafer lithography DOF requirements for each printing the desired feature dimensions.
[P] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a pattern generator tool.
[Q] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[R] Transmission—Ratio, expressed in percent, of the fraction of light passing through an attenuated PSM layer relative to the mask blank with no opaque films.
[S] Phase—Change in optical path length between two regions on the mask expressed in degrees. The mean value is determined by averaging phase measured for many features on the mask.
[T] Alt PSM phase uniformity is a range specification equal to the maximum phase error deviation of any point from the mean value.

Table 78c EUVL Mask Requirements—Near-term Years

Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*57*	*50*	*45*	*40*	*36*	*32*
Flash ½ pitch (nm) (un-contacted poly)	*51*	*45*	*40*	*36*	*32*	*28*
DRAM/Flash CD control (3 sigma) (nm)	*5.9*	*5.3*	*4.7*	*4.2*	*3.7*	*3.3*
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*59*	*52*	*45*	*40*	*36*	*32*
MPU gate in resist (nm)	*38*	*34*	*30*	*27*	*24*	*21*
MPU physical gate length (nm)	*23*	*20*	*18*	*16*	*14*	*13*
Gate CD control (3 sigma) (nm) [B]	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*	*1.3*
Overlay	*10*	*9*	*8*	*7*	*6*	*6*
Contact after etch (nm)	*57*	*51*	*45*	*40*	*36*	*32*
Generic Mask Requirements						
Mask magnification [B]	**4**	**4**	**4**	**4**	**4**	**4**
Mask nominal image size (nm) [C]	**151**	**135**	**120**	**107**	**95**	**85**
Mask minimum primary feature size [D]	**106**	**94**	**84**	**75**	**67**	**59**
Image placement (nm, multipoint) [E]	**6.1**	**5.4**	**4.8**	**4.3**	**3.8**	**3.4**
CD uniformity (nm, 3 sigma) [F]						
Isolated lines (MPU gates)	**3.4**	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**
Dense lines DRAM (half pitch)	**8.2**	**7.3**	**6.5**	**5.8**	**5.2**	**4.6**
Contact/vias	**7.6**	**6.8**	**4.8**	**4.3**	**3.8**	**3.4**
Linearity (nm) [G]	**8.7**	**7.6**	**6.8**	**6.1**	**5.3**	**4.9**
CD mean to target (nm) [H]	**4.6**	**4.0**	**3.6**	**3.2**	**2.8**	**2.6**
Defect size (nm) [I]	**46**	**40**	**36**	**32**	**28**	**26**
Data volume (GB) [J]	**655**	**825**	**1040**	**1310**	**1651**	**2080**
Mask design grid (nm) [K]	**2**	**2**	**2**	**2**	**2**	**2**
EUVL-specific Mask Requirements						
Substrate defect size (nm) [L]	**38**	**36**	**35**	**33**	**31**	**30**
Mean peak reflectivity	**65%**	**66%**	**66%**	**66%**	**67%**	**67%**
Peak reflectivity uniformity (% 3 sigma absolute)	**0.69%**	**0.58%**	**0.47%**	**0.42%**	**0.37%**	**0.33%**
Reflected centroid wavelength uniformity (nm 3 sigma) [M]	**0.08**	**0.07**	**0.06**	**0.05**	**0.05**	**0.05**
Absorber sidewall angle tolerance (± degrees) [P]	**1**	**1**	**0.75**	**0.69**	**0.62**	**0.5**
Absorber LER (3 sigma nm) [N]	**3.2**	**2.8**	**2.5**	**2.2**	**2.0**	**1.8**
Mask substrate flatness (nm peak-to-valley) [O]	**75**	**60**	**50**	**41**	**36**	**32**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

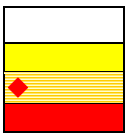
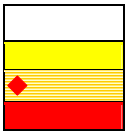


Table 78d EUVL Mask Requirements—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ pitch (nm) (contacted)	28	25	22	20	18	16	14
Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
DRAM/Flash CD control (3 sigma) (nm)	3.0	2.6	2.3	2.1	1.9	1.7	1.5
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU gate in resist (nm)	19	17	15	13	12	11	9
MPU physical gate length (nm)	11	10	9	8	7	6	6
Gate CD control (3 sigma) (nm) [B]	1.2	1.0	0.9	0.8	0.7	0.7	0.6
Overlay	5	5	4	4	3	3	3
Contact after etch (nm)	28	25	23	20	18	16	14
Generic Mask Requirements							
Mask magnification [B]	4	4	4	4	4	4	4
Mask nominal image size (nm) [C]	76	67	60	54	48	42	38
Mask minimum primary feature size [D]	53	47	42	37	33	30	26
Image placement (nm, multipoint) [E]	3.0	2.7	2.4	2.1	1.9	1.7	1.5
CD Uniformity (nm, 3 sigma) [F]							
Isolated lines (MPU gates)	1.7	1.5	1.3	1.2	1.1	1.0	0.9
Dense lines DRAM (half pitch)	4.1	3.7	3.3	2.9	2.6	2.3	2.1
Contact/vias	3.0	2.7	1.8	1.6	1.4	1.3	1.1
Linearity (nm) [G]	4.3	3.8	3.3	3.0	2.7	2.4	2.1
CD mean to target (nm) [H]	2.2	2.0	1.8	1.6	1.4	1.3	1.1
Defect size (nm) [I]	22	20	18	16	14	13	11
Data volume (GB) [J]	2621	3302	4160	5241	6604	8320	10483
Mask design grid (nm) [K]	2	2	2	1	1	1	1
EUVL-specific Mask Requirements							
Substrate defect size (nm) [L]	28	27	25	23	22	20	18
Mean peak reflectivity	67%	67%	67%	67%	67%	67%	67%
Peak reflectivity uniformity (% 3 sigma absolute)	0.29%	0.26%	0.23%	0.21%	0.19%	0.17%	0.15%
Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.04	0.04	0.04	0.03	0.03	0.03	0.02
Absorber sidewall angle tolerance (± degrees) [P]	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Absorber LER (3 sigma nm) [N]	1.6	1.4	1.3	1.1	1.0	0.9	0.8
Mask substrate flatness (nm peak-to-valley) [O]	29	26	23	20	18	16	14

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 78c and d:
EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.
[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
[B] Magnification—Lithography tool reduction ratio.
[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD, placement, and defects.
[E] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.
[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).

[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.
[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.
[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a pattern generator tool.
[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[L] Substrate Defect Size—the minimum diameter spherical defect (in polystyrene latex sphere equivalent dimensions) on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.
[M] Includes variation in median wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.
[N] Line edge roughness (LER)—is defined a roughness 3 sigma one-sided for spatial period <mask primary feature size.
[O] Mask Substrate Flatness—Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge, which may be compensated by the mask mounting and leveling method in the exposure tool. The flatness error is defined as the deviation of the surface from the plane that minimizes the maximum deviation. This flatness requirement applies to each of the front and backsides individually.
[P] The sidewall angle tolerance applies to the mean absorber sidewall angle agreed upon between mask user and supplier.

Table 78e Imprint Template Requirements—Near-term Years

Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*57*	*50*	*45*	*40*	*36*	*32*
Flash ½ pitch (nm) (un-contacted poly)	*51*	*45*	*40*	*36*	*32*	*28*
DRAM/Flash CD control (3 sigma) (nm)	*5.9*	*5.3*	*4.7*	*4.2*	*3.7*	*3.3*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*59*	*52*	*45*	*40*	*36*	*32*
MPU gate in resist (nm)	*38*	*34*	*30*	*27*	*24*	*21*
MPU physical gate length (nm)	*23*	*20*	*18*	*16*	*14*	*13*
Overlay (3 sigma) (nm)	*5.9*	*5.3*	*4.7*	*4.2*	*3.7*	*3.3*
Gate CD control (3 sigma) (nm)	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*	*1.3*
Contact after etch (nm)	*67*	*58*	*51*	*45*	*40*	*36*
Generic Mask Requirements						
Magnification [B]	1	1	1	1	1	1
Mask nominal image size (nm) [C]	38	34	30	27	24	21
Image placement (nm, multipoint) [D]	2.0	1.8	1.6	1.4	1.2	1.1
CD Uniformity (nm, 3 sigma) [E]						
Isolated lines (MPU gates)	2.2	1.9	1.7	1.5	1.4	1.2
Dense lines DRAM/Flash (half pitch)	5.5	4.9	4.3	3.9	3.4	3.1
Contact/vias	6.4	5.6	4.9	4.3	3.9	3.4
Linearity (nm) [F]	5.1	4.5	4.0	3.6	3.2	2.8
CD mean to target (nm) [G]	5.1	4.5	4.0	3.6	3.2	2.8
Data volume (GB) [H]	295	372	469	591	745	938
Mask design grid (nm) [I]	1	1	1	1	1	1
UV-NIL-specific Mask Requirements						
Defect size impacting CD (nm) x, y [J]	5.1	4.5	4.0	3.6	3.2	2.8
Defect size impacting CD (nm) z [K]	10.1	9.0	8.0	7.1	6.4	5.7
Mask substrate flatness (nm peak-to-valley) [L]	298	252	192	180	153	126
Trench depth, mean (nm) [M]	75–119	67–104	60–90	53–81	47–72	42–64
Etch depth uniformity (nm) [N]	3.8–5.9	3.4–5.2	3.0–4.5	2.7–4.0	2.4–3.6	2.1–3.2
Trench wall angle (degrees) [O]	87.0	87.3	87.6	87.9	88.1	88.3
Trench width roughness (nm, 3 sigma) [P]	2.2	2.0	1.7	1.6	1.4	1.2
Corner radius, bottom of feature (nm) [Q]	6.3	5.6	5.0	4.5	4.0	3.5
Corner radius, top of feature (nm) [R]	1.6	1.4	1.3	1.1	1.0	0.9
Trench bottom surface roughness (nm, 3 sigma) [S]	7.6	6.7	6.0	5.4	4.8	4.2
Template absorption [T]	<2%	<2%	<2%	<2%	<2%	<2%
Near surface defect (nm) [U]	51	45	40	36	32	28
Defect size, patterned template (nm) [V]	35	30	30	20	20	20
Defect density (#/cm^2) [W]	0.03	0.03	0.03	0.01	0.01	0.01
Dual Damascene overlay: metal/via (nm, 3 sigma) [X]	25	23	22	20	18	17

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table 78f Imprint Template Requirements—Long-term Years

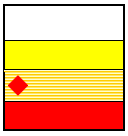
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash ½ pitch (nm) (un-contacted poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
DRAM/Flash CD control (3 sigma) (nm)	*3.0*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
MPU physical gate length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Overlay (3 sigma) (nm)	*3.0*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
Gate CD control (3 sigma) (nm)	*1.2*	*1.0*	*0.9*	*0.8*	*0.7*	*0.7*	*0.6*
Contact after etch (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*
Generic Mask Requirements							
Magnification [B]	1	1	1	1	1	1	1
Mask nominal image size (nm) [C]	19	17	15	13	12	11	9
Image placement (nm, multipoint) [D]	1.0	0.9	0.8	0.7	0.6	0.6	0.5
CD Uniformity (nm, 3 sigma) [E]							
Isolated lines (MPU gates)	1.1	1.0	0.9	0.8	0.7	0.6	0.5
Dense lines DRAM/Flash (half pitch)	2.7	2.4	2.2	1.9	1.7	1.5	1.4
Contact/vias	3.1	2.7	2.4	2.2	1.9	1.7	1.5
Linearity (nm) [F]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
CD mean to target (nm) [G]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
Data volume (GB) [H]	1182	1489	1876	2364	2978	3752	4728
Mask design grid (nm) [I]	1	1	1	1	1	1	1
UV-NIL-specific Mask Requirements							
Defect size impacting CD (nm) x, y [J]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
Defect size impacting CD (nm) z [K]	5.1	4.5	4.0	3.6	3.2	2.8	2.5
Mask substrate flatness (nm peak-to-valley) [L]	110	88	72	56	45	36	29
Trench depth, mean (nm) [M]	37–57	33–51	30–45	26–41	23–36	21–32	18–29
Etch depth uniformity (nm) [N]	1.9–2.8	1.7–2.5	1.5–2.3	1.3–2.0	1.2–1.8	1.1–1.6	0.9–1.4
Trench wall angle (degrees) [O]	88.5	88.7	88.8	88.9	89.1	89.2	89.2
Trench width roughness (nm, 3 sigma) [P]	1.1	1.0	0.9	0.8	0.7	0.6	0.5
Corner radius, bottom of feature (nm) [Q]	3.2	2.8	2.5	2.2	2.0	1.8	1.6
Corner radius, top of feature (nm) [R]	0.8	0.7	0.6	0.6	0.5	0.4	0.4
Trench bottom surface roughness (nm, 3 sigma) [S]	3.8	3.4	3.0	2.7	2.4	2.1	1.9
Template absorption [T]	<2%	<2%	<2%	<2%	<2%	<2%	<2%
Near surface defect (nm) [U]	25	23	20	18	16	14	13
Defect size, patterned template (nm) [V]	20	10	10	10	10	10	10
Defect density (#/cm^2) [W]	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Dual Damascene overlay: metal/via (nm, 3 sigma) [X]	15	14	11	10.5	10	9	8

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Table 78e and f:
[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
[B] Magnification—Lithography tool reduction ratio, N:1.
[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.
[E] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).
[F] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.
[G] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.
[H] This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
[I] Wafer design grid multiplied by the mask magnification.
[J] Defect Size (nm) x, y—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[K] Defect Size (nm) z—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[L] Flatness (nm peak-to-valley) across the 110 mm × 110 mm central area image field on a 6-inch × 6-inch square blank. Flatness is derived from empirical residual layer uniformity (RLT) and magnification.
[M] Trench depth mean—Aspect ratio of trench set to 2:1. Low end determined by printed gate length, High end determined by MPU/ASIC half pitch
[N] Trench depth uniformity in nm—Set to 5% of trench depth.
[O] Trench wall angle in degrees—Minimum wall angle necessary to keep the etch bias of the bilayer resist less than 5%. A selectivity of 10:1 between the etch barrier and transfer layer is assumed. Transfer layer aspect ratio starts at 1.5:1, and finishes at 2:1.
[P] Trench width roughness (nm, 3 sigma)—equivalent to resist line width roughness.
[Q] Corner radius, bottom of feature—critical to S-FIL/R (positive tone imprinting) where it defines the depth that the blanket ROI etch must reveal into the imprint material for good CD control (12.5% of CD). Non-critical for S-FIL (negative tone imprinting).
[R] Corner radius, top of feature—critical to S-FIL (negative tone imprinting) for good CD control, where it behaves as a resist "footing" in equivalent projection lithography (3% of CD). Non-critical for S-FIL/R (positive tone imprinting).
[S] Roughness in the bottom of an etched trenching resulting from imperfections in the plasma etch process or micromasking from the hard mask.
[T] Percent of incident light intrinsically absorbed by the 6.3 mm thick substrate at 365 nm. This is to minimize heating and thermal distortion and maximize equipment throughput.
[U] This is the maximum defect size for the quartz substrate from the surface level to a depth of 200 nm.
[V] Defect size, patterned template—Defect size in nm on finished patterned template.
[W] Number of defects per square cm on a finished template.
[X] This is the via to metal line overlay requirement on a 3D template for landed vias.

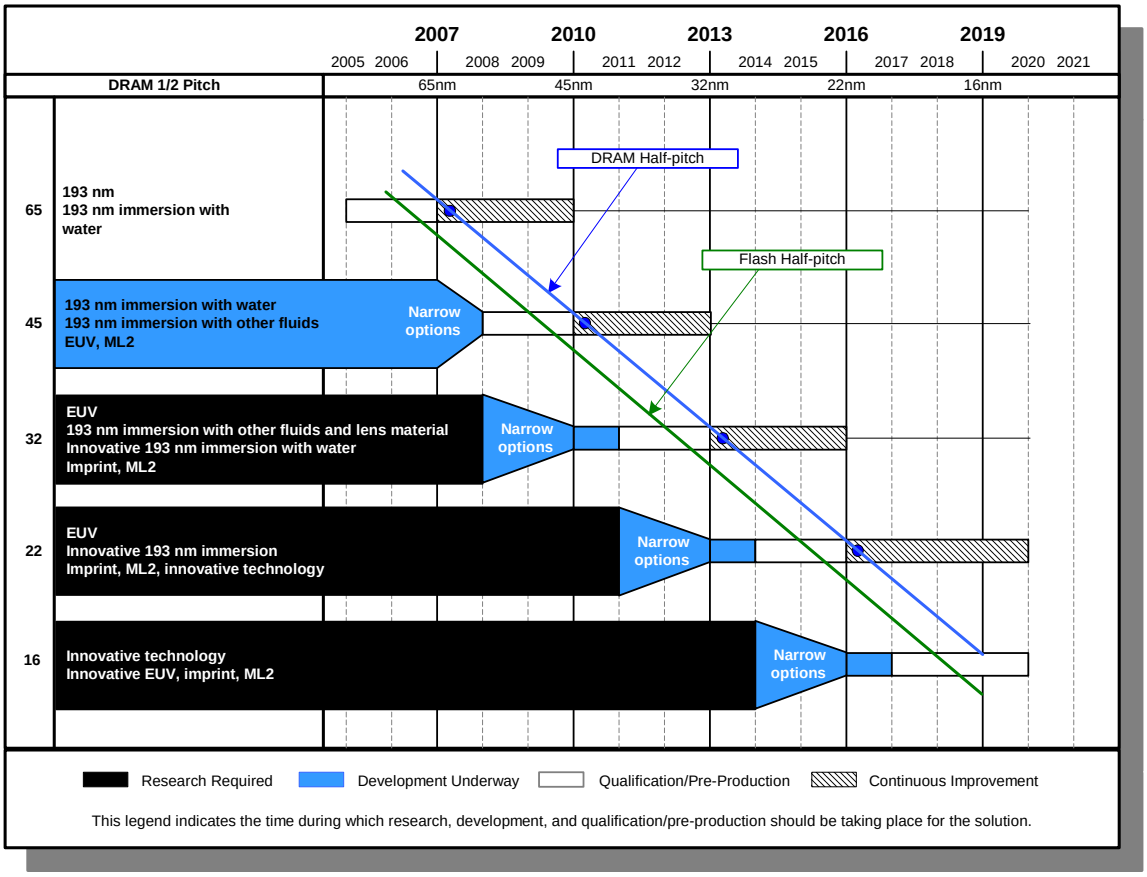
POTENTIAL SOLUTIONS

The potential solutions for leading-edge, critical layer lithography are presented in Figure 67. The order of the options represents the probability of a particular technology to be the dominant solution for a given technology generation with the most probable options listed first. All of the infrastructure required to use the lithography technologies at the time shown must be ready—including tools, masks, and resist. Optical lithography at 193 nm wavelength is expected to be the dominant approach through DRAM 65 nm half pitch, with EUV, ML2, and imprint possibly appearing at 45 nm half pitch, although more likely at 32 nm half pitch. For leading-edge semiconductor manufacturing, 193 nm lithography has replaced 248 nm lithography as the wavelength for critical layer patterning. The use of 157 nm exposure wavelength is no longer expected as a lithography solution. Immersion lithography could extend optical lithography to 32 nm half pitch if lens materials with high index and higher index fluids can be developed in time. Research is also ongoing into breaking the pattern into two masks, each mask having minimum half pitch two times the minimum half pitch to be printed on the wafer. This dual-mask exposure technique could be used to extend 193 nm immersion lithography beyond DRAM 32 nm half pitch if resists suitable for double exposure and adequate mask alignment could be developed. Software for optimally dividing the pattern into two masks would need to be developed, and the use of two masks would have to be less expensive than alternative technologies.

The post-optical alternatives are potential solutions at and below DRAM 45 nm half pitch. Of the possible alternative technologies, multiple geographical regions consider EUV, maskless, and imprint lithography as potential successors to optical lithography. EUV is viewed as the most likely for 32 nm and 22 nm half pitch patterning. Maskless lithography has been applied to niche applications in development for prototyping and transistor engineering and to low volume application specific integrated circuit (ASIC) production, but its role could be expanded. Breakthroughs in direct-write technologies that achieve high throughput could be a significant paradigm shift, eliminating the need for masks and resulting in cost and cycle-time reduction. Maskless lithography for application beyond prototyping is currently in the

research phase, and many significant technological hurdles will need to be overcome for ML2 to be viable for cost-effective semiconductor manufacturing. Imprint lithography has the potential to be a cost-effective solution, but there are a number of problems that need to be solved for this to happen, including the difficulties associated with 1× templates, defects, template lifetime, and overlay. It is unclear whether any technology currently identified as a potential solution will indeed be capable of meeting the requirements for DRAM 16 nm half pitch, necessitating innovative technology development.

Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions within industry and between industry and universities are necessary to narrow the options for these future generations and focus support to enable one or perhaps two technologies to be ready for manufacturing at the desired time. The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities that are necessary for continued adherence to Moore's Law at DRAM 32 nm half pitch and beyond. This shift will drive major changes throughout the lithography infrastructure and will require significant resources for commercialization. These development costs must necessarily be recovered in the costs of exposure tools, masks, and materials.



Notes: RET and lithography friendly design rules will be used with all optical lithography solutions, including with immersion; therefore, they are not explicitly noted.

Figure 67 Lithography Exposure Tool Potential Solutions

CROSSCUT NEEDS

The crosscut technology needs and potential solutions involving Lithography, *ESH*, *Factory Integration*, *Yield Enhancement*, *Metrology*, *Modeling and Simulation*, device and circuit performance, and *Emerging Research Devices and Materials* are outlined in this section.

ENVIRONMENT, SAFETY, AND HEALTH

The recent discussion over the continued use of perfluoroalkyl sulfonates (PFAS) in photochemicals has shown that long- and commonly used materials can have ESH issues that are being understood only recently. The introduction of new technologies necessarily means the use of materials and chemicals whose health and environmental implications are even less well known. The efficiency of EUV sources also needs to be maximized to minimize the facility and power requirements to operate these sources at the power desired for high throughput EUV lithography. Specifically, the wall-plug efficiency of the sources needs to be increased to minimize the power required to generate EUV photons and to cool the source components. Practices for use and disposal of the chemicals utilized in lithography must continue with careful regard for the safety of workers and their environment. Refer to the *Environment, Safety, and Health* chapter for comprehensive information and for a link to a new chemical screening tool (*Chemical Restrictions Table*).

FACTORY INTEGRATION

To maintain adequate process control, advanced process control capabilities are essential in the lithography cluster in the wafer fab. These capabilities are becoming increasingly important in mask making facilities as well, but their implementation for mask making are much less mature. Leveraging the learning from the wafer factory automation experience will also be essential. Several mask shops have developed custom solutions for automating data handling for

defect inspection and repair. Further opportunities for automation exist. Leveraging the use of existing standards that are used today in wafer fabs, such as the adoption of SECS/GEM into the mask making tool infrastructure, will help reduce manufacturing errors.

The configuration of the lithography cell should provide optical character recognition (OCR) or barcode readers for wafer marking recognition at the input interface to the track. An accurate wafer tracking system across various process modules is required to identify the working flow of any wafer in process. Several integrated metrology modules able to evaluate one or more than the following list of parameters—CD, litho stack thickness, target profile, overlay, macro inspection with automated defect classification and wafer flatness—are also recommended. Track and stepper/scanner should be able to use data recorded by any kind of internal or external sensors to adjust processes.

Other requirements, which may call for major upgrades of equipment software and in several cases even of related hardware, are the possibility to simultaneously manage different module flows on tracks to accommodate optimal metrology sampling plans and the ability to accept overrides to downloaded (or selected) recipe set points. Moreover, on any track module it is desirable to be able to update all relevant set points wafer by wafer, even within the same lot. On the exposure tool, the software should allow the host to update dose, focus/tilt and overlay input parameters wafer by wafer, even within the same lot or perhaps for each exposure field. Calibration, self-calibration and matching activities on metrology modules should be allowed without a significant loss in litho cell throughput.

YIELD ENHANCEMENT

Yield enhancement is expected to become a major challenge, as critical defect sizes become smaller than the limits of optical detection. Inspection systems are increasingly challenged to meet the required sensitivity and speed requirements. Non-optical methods of defect detection have not yet been demonstrated to have the acquisition rates required for controlling defects in semiconductor manufacturing. Furthermore, die-to-database inspection of wafers is probably required for using ML2.

Design for manufacturing practices are being used and need to be further developed to minimize systematic sources of yield loss. Control of airborne molecular contamination (AMC) is also critical to maximize yield by minimizing local poisoning of resist and minimizing the formation of progressive defects on masks during exposure. See the *Yield Enhancement* chapter for quantitative AMC control requirements related to lithography. Mask handling practices to maintain EUV masks and imprint templates free from defects without pellicles remains a significant challenge.

METROLOGY

The rapid advancement of lithography technology and resultant decrease in feature dimensions continues to challenge wafer and mask metrology capability. The existing precision of critical dimension measurement tools does not meet the somewhat relaxed 20% measurement precision-to-process tolerance metric for the most advanced technology generations. Precision includes measurement tool variation from short- and long-term tool variation as well as tool-to-tool matching. Wafer and mask CD technology is evolving to meet the need for 3D measurements. Potential solutions for near-term CD measurements include CD-scanning electron microscopy, scatterometry, and scanned probe microscopy. A key requirement is measurement of line width roughness. Measurement precision for LWR must be smaller (better) than that needed for linewidth. The quantitative effects of linewidth roughness on device performance need to be better understood to optimize metrology for LWR.

Overlay metrology is also challenged by future technology generations. Memory makers are requiring more stringent overlay control to achieve desired circuit yields. Traditional overlay test structures do not capture all possible overlay errors that can occur during use of phase shift and optical proximity correction masks.

The complete discussion of Lithography Metrology is located in the Lithography Metrology and Microscopy sections of the *Metrology* chapter. The lithography metrology technology requirements and potential solutions are also presented in that chapter.

MODELING AND SIMULATION

Support from modeling and simulation is critical both to push the limits of traditional optical lithography and to assess new next generation lithography technologies. The application of simulation tools in lithography largely benefits from the well-known physical basis of Maxwell's equations that govern lithographic imaging. Applying these equations to model lithographic imaging requires a problem-specific and efficient implementation in simulation tools. Furthermore, an

intimate link between equipment-scale and feature-scale simulation is required for state-of-the-art lithography simulation. Equipment scale effects often require modeling with random variables with user-defined or user-measured probability distributions. While calculation of lithographic image formation relies on physical models, the physical/chemical understanding of resist processes, particularly for chemically amplified resists, is far less advanced. Resist models are typically semi-empirical, and they require fitting and calibration with experimental data.

The key requirements for simulation of optical imaging are accuracy, speed of computation, and the capability to model the effects of non-ideal masks, non-ideal lenses, multilayer resists and non-planar substrates. Problem-specific algorithms and implementations are needed to deal with the "tricks" used when pushing optical lithography to the limits, such as off-axis illumination, complicated mask geometries including phase-shifting, and optical proximity correction. Non-idealities of the optical system used are getting more and more critical and must be appropriately addressed in simulation. The influence of defects on the mask and on the wafer is becoming more and more important and requires appropriate simulation capabilities especially for the identification of "killer defects."

New techniques used in future next generation lithography techniques, such as replacement of lenses by multilayer mirrors and the use of reflecting masks for extreme ultraviolet lithography must be appropriately modeled and included in the simulation programs. Mask pattern generators and some ML2 options involve imaging with electrons. Simulations of stochastic space charge effects, geometrical aberrations and electron optical lens design performance using either magnetic or electrostatic lens elements are needed. Support from simulation for narrowing down the technology options has been and will continue to be important.

With the current introduction of immersion lithography several additional requirements for modeling and simulation result. Optical systems with NA > 0.85 must be simulated, which especially requires the appropriate treatment of polarized illumination and partial polarization by mask structures and materials. Simulation should also help to assess whether specific defects are due to bubbles in the immersion liquid.

A specific challenge for lithography modeling and simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as line-edge roughness. Better calibration techniques are required both for model development and for customizing models implemented in commercial tools to appropriately describe the photoresists in question. Calibration obviously depends on the quality of input data, for example, CD measurements. Therefore, it is necessary to better understand and estimate measurement errors. Systematic errors should be dealt with by models of the measurement tools, such as CD-SEMs. With the growing importance of LWR and LER, lithography simulation needs to contribute to the assessment of their influence on device and interconnect performance (LER) and variability (LWR). Since the roughness of etched structures and not the resist pattern ultimately affects device performance, intimate coupling between resist and etching simulation is indispensable. Simulations of etching are important to understand the relationship between 3D edge roughness and profiles in resist features and the resulting roughness and profiles in etched gates, contacts or trenches. Intimate links with etching simulation must also be established also to predict the geometry of non-ideal mask edges that frequently result from mask-making lithography steps.

A specific requirement for lithography modeling and simulation is the need for very efficient simulation tools that allow the simulation of large areas and/or the conduction of simulation studies for a multitude of variations of physical parameters or layouts to support growing design for manufacturing needs. In fact, lithographic simulations of full-chip layouts are now needed to verify OPC and phase assignment data to avoid expensive masks being fabricated with errors or with corrections having only marginal performance. These simulations must be reasonably accurate and execute at high speed to evaluate the entire layout in a reasonable amount of time.

Besides models of image formation and resist profile generation in the lithography process, mechanical models are also critical for designing lithography tools. Refinement and application of finite element methods is important for assuring exposure tools, masks and wafers remain stable enough to meet demanding overlay tolerances. Static and dynamic models of lens mounting stability, stage stability and also aspects of exposure tool hardware design are critical. Static and dynamic mechanical models are also critical for designing adequate mounting methods for masks and wafers to maintain desired position under high stage acceleration values and to maintain desired flatness. Equilibrium and non-equilibrium models of thermal effects are also essential for exposure tool design, especially for modeling heating of the immersion fluid in immersion lithography and its effect on distortion and aberrations. Models of fluid flow for immersion have also been essential in designing fluid delivery systems that minimize immersion-specific defect formation.

Details on developments needed to satisfy these requirements are given in the *Modeling and Simulation* chapter

INTER-FOCUS ITWG DISCUSSION

Gate CD and line width roughness control capability impacts devices (process integration, devices, and structures [PIDS]), front-end processes (FEP), metrology and design. Depending upon the level of CD control that is possible, there will be more or less stringent requirements on the other processes that affect transistor performance, such as implant, diffusion and etch. Tight CD control will require metrology that is capable of supporting the control requirements. Design will need to take into account the collective capabilities of all processes that affect transistor performance. The Design TWG simulated circuit delay and power variability as a function of the most significant process and device variables. The simulations indicated that increasing the CD control requirement to ± 12% would result in a tolerable variation of circuit delay and power variation given the significant variations of all of the significant parameters affecting these circuit attributes.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES AND MATERIALS

Emerging devices are expected to impact lithography in two areas. First, a number of devices that have been considered require critical layer patterning over non-planar substrates, which will require lithographic solutions that can provide tight CD control over the topography. For example, bilayer resists represent a possible solution to this problem. Large depth-of-focus may become a compelling advantage for certain lithographic technologies. Second, emerging devices and materials could provide relief for the control of gate CDs. This will have an impact on all aspects of lithographic technology, including masks, resists, exposure tools, and metrology.