INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

ASSEMBLY AND PACKAGING

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Assembly and Packaging White Paper link: "*The Next Step in Assembly and Packaging--System-level Integration in the Package (SiP)*"

ASSEMBLY AND PACKAGING

SCOPE

This chapter addresses the near term assembly and packaging roadmap requirements and introduces many new requirements and potential solutions to meet market needs in the longer term. Assembly and Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability.

Today assembly and packaging is a limiting factor in both cost and performance for electronic systems. This has resulted in acceleration of innovation. Design concepts, packaging architectures, materials, manufacturing processes and systems integration technologies are all changing rapidly. This accelerated pace of innovation has resulted in development of several new technologies and expansion and acceleration of others introduced in prior years. Wireless and mixed signal devices, bio-chips, optoelectronics, and MEMS have placed new requirements on packaging and assembly.

The electronics industry is nearing the limits of traditional CMOS scaling. The continued growth of the industry, driven by a continuous reduction in cost per function, will require new devices types and new materials. There will be a gap between the time CMOS scaling can no longer maintain progress at the Moore's Law rate and the time a new generation of device architectures and electronic material will support a continued drop on cost per function. As traditional Moore's law scaling becomes more difficult, assembly and packaging innovation enabling functional diversification and allowing scaling in the third dimension is taking up the slack.

Assembly and Packaging provides a mechanism for cost effective incorporation of functional diversification through System-in-Package (SiP) technology. This technology enables the continued increase in functional density and decrease in cost per function required to maintain the progress of electronics.

New architectures include printable circuits, thinned wafers and both active and passive embedded devices are emerging as solutions to market requirements. The materials and equipment used in assembly and packaging are also changing rapidly to meet the requirements of these new architectures and the changing environmental regulatory requirements.

This chapter is organized in eight major sections:

- Difficult Challenges
- Single Chip Packaging
- Wafer Level Packaging
- System-in-Package
- Packaging for Specialized Functions
- Advanced Packaging Elements
- Equipment Requirements
- Cross-Cut Issues

Wherever possible we have aligned the ITRS Assembly and Packaging chapter with other industry roadmap organizations including iNEMI, JISSO and IPC.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist

in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in tables 93a and 93b below. Meeting these requirements will demand significant investment in research and development.

Table AP1 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥22 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ
Wafer level CSP	-I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design is needed now. -EDA for "native" area array is required to meet the Roadmap projections. -Models for reliability prediction
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
Thinned die packaging	- Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration

Table AP1 Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Close gap between chip and substrate Improved organic substrates	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology) -Production techniques will require silicon-like production and process technologies -Tg compatible with Pb free solder processing (including rework at 260°C)
High current density packages	-Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
Flexible system packaging	-Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
3D packaging	-Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer via structure and via fill process -Singulation of TSV wafers/die - Test access for individual wafer/die -Bumpless interconnect architecture
Difficult Challenges <22 nm	*Summary of Issues*
Package cost does not follow the die cost reduction curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
High frequency die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz -"Hot spot" thermal management There is currently a "brick wall" at five-micron lines and spaces for substrates.
System-level design capability to integrated chips, passives, and substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the "bumps" as well as the substrates.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TSV—through silicon via

The investment required to meet these challenges is greater than the current run rate and cannot be met through the current gross margin of the assembly and packaging suppliers alone. The recent increase in cooperative development represented by University programs and Research Consortia is evidence that the technical community is responding:

- University research in packaging is increasing around the world
- Materials companies have increased their investment in the new materials required to meet the future needs beyond copper metallization and low κ and high κ dielectric materials to new

polymers and nanomaterials. New materials addressing future requirements are described in the Emerging Research Materials Chapter of this Roadmap.

- Venture capital investment in packaging and interconnect technology is increasing after several years of absence.
- Equipment companies are investing in new capability to meet the needs of emerging requirements for making and handling thinned wafers/die, molding (e.g., compression molding, molded underfill), through silicon vias, wafer level packaging and 3D packaging.
- Government and Private research institutes are increasing their investment in this area. A list of consortia addressing Assembly and Packaging development can be found in Appendix A.
- Consumer product companies are driving innovation in SiP and other new system integration architectures.

Even with this increased investment the current level may be inadequate to meet the Difficult Challenges within the Roadmap time frame. The acceleration of this investment and the efficient coordination of development among groups will be necessary to achieve the scheduled Roadmap milestones for assembly and packaging. A major objective of this chapter is to encourage and facilitate the coordination and focus of these efforts on the Difficult Challenges.

SINGLE CHIP PACKAGING

OVERALL PACKAGING REQUIREMENTS

The technology requirements for single-chip packages address cost, die size, power requirements, and package pin count as well as operating characteristics and environment. These data are presented in Table AP2a and AP2b below. There are a number of parameters where a solution is not proven or unknown, as noted by the color coding in the table. In many cases the reason for the color is not that the parameter cannot be met but that the cost of doing so will not meet the cost targets.

Each parameter is divided into four classes of devices. In general the low cost category represents the lowest cost package for any device type and has the least requirement for performance. Hand-held devices and memory have been grouped together since they have nearly identical requirements for the near term. This is likely to change during the life of this Roadmap due to the rapid increase in frequency required for high performance memory circuits. The tables use the microprocessor for the cost performance and high performance categories except for pin count and die size where FPGA circuits have a higher requirement for both die size and pin count.

Table AP2a Single-chip Packages Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Cost per Pin Minimum for Contract Assembly (Cents/Pin)									
Low-cost, hand-held and memory	**.27-.50**	**.25-.48**	**.24-.46**	**.23-.44**	**.22-.42**	**.21-.40**	**.20-.38**	**.20-.36**	**.20 -.34**
Cost-performance	**.69-1.19**	**.66-1.13**	**.63-1.70**	**.60-1.20**	**.57-.97**	**.54-.92**	**.51-.87**	**.48 - .83**	**.46 - .79**
High-performance	**1.83**	**1.73**	**1.64**	**1.56**	**1.48**	**1.41**	**1.34**	**1.27**	**1.21**
Harsh	**0.27–2.11**	**0.25–2.00**	**0.24–1.90**	**0.23–1.54**	**.22-1.81**	**.21 - 1.71**	**.20 - 1.63**	**.20 - 1.55**	**.20 - 1.47**
Chip size (mm^2)									
Low-cost/hand held	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Cost performance	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
High performance (FPGA)	**662**	**695**	**729**	**766**	**804**	**750**	**750**	**750**	**750**
Harsh	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**

Table AP2a Single-chip Packages Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Maximum Power (Watts/mm^2)									
Hand held and memory (Watts)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Cost-performance (MPU)	**0.57**	**0.86**	**0.90**	**0.96**	**1.13**	**1.11**	**1.10**	**1.17**	**1.19**
High-performance (MPU)	**0.33**	**0.47**	**0.46**	**0.47**	**0.52**	**0.51**	**0.48**	**0.49**	**0.46**
Harsh	**0.18**	**0.2**	**0.2**	**0.22**	**0.22**	**0.24**	**0.25**	**0.25**	**0.27**
Core Voltage (Volts)									
Low-cost	**0.9**	**0.8**	**0.7**	**0.6**	**0.6**	**0.6**	**0.5**	**0.5**	**0.4**
Hand-held and memory	**0.7**	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**	**0.5**	**0.4**	**0.4**
Cost-performance	**0.9**	**0.8**	**0.8**	**0.6**	**0.6**	**0.6**	**0.6**	**0.5**	**0.5**
High-performance	**0.9**	**0.8**	**0.8**	**0.6**	**0.6**	**0.6**	**0.6**	**0.5**	**0.5**
Harsh	**1.2**	**1.2**	**1.2**	**1.2**	**1**	**1**	**0.9**	**0.9**	**0.9**
Package Pin count Maximum									
Low-cost	**148–700**	**150–800**	**160–850**	**170–900**	**180–950**	**188–1000**	**198–1050**	**207 - 1100**	**218 - 1150**
Cost performance	**600–2140**	**600–2400**	**660–2801**	**660–2783**	**720-3061**	**720–3367**	**800–3704**	**800-4075**	**880–4482**
High performance (FPGA)	**4000**	**4400**	**4620**	**4851**	**5094**	**5348**	**5616**	**5896**	**6191**
Harsh	**386**	**405**	**425**	**447**	**469**	**492**	**517**	**543**	**570**
Minimum Overall Package Profile (mm)									
Low-cost, hand held and memory	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.2**	**0.2**
Cost-performance	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**1.4**	**1.4**	**1.4**	**1.2**	**1.2**	**1**	**1**	**1**	**1**
Harsh	**0.8**	**0.8**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**	**0.7**
Performance: On-Chip (GHz)									
Low-cost/Hand held	**735/4676**	**808/5144**	**889/5660**	**978–6224**	**1076 - 6846**	**1183 - 7530**	**1243–7903**	**1305 - 8303**	**1370 - 8718**
Cost-performance	**4.70**	**5.06**	**5.45**	**5.88**	**6.33**	**6.82**	**7.34**	**7.91**	**8.52**
High-performance	**4.70**	**5.06**	**9827.14**	**5.88**	**6.33**	**6.82**	**7.34**	**7.91**	**8.52**
Harsh	**106**	**117**	**128**	**141**	**155**	**171**	**188**	**207**	**227**
Performance: Chip-to-Board for Peripheral Buses (MHz)									
Low-cost Logic/Memory to MPU clock	**100/667**	**100/800**	**100/800**	**125/800**	**125/800**	**125/1000**	**125/1000**	**125/1000**	**125/1000**
Cost-performance (for multi-drop nets)	**733**	**800**	**800**	**800**	**800**	**1000**	**1000**	**1000**	**1000**
High-performance (for differential-pair point-to-point nets) (GHz)	**4.88**	**6.10**	**7.63**	**9.54**	**11.92**	**14.90**	**18.63**	**23.28**	**29.10**
Harsh	**106**	**106**	**115**	**125**	**125**	**125**	**125**	**125**	**150**
Maximum Junction Temperature									
Low-cost, Hand Held and Memory	**125**	**125**	**125**	**125**	**125**	**125**	**125**	**125**	**125**
Cost performance	**95**	**95**	**90**	**90**	**90**	**90**	**90**	**90**	**90**
High-performance	**95**	**95**	**90**	**90**	**90**	**90**	**90**	**90**	**90**
Harsh**	**175**	**175**	**200**	**220**	**220**	**220**	**220**	**220**	**220**
Harsh-complex ICs	**175**	**175**	**175**	**175**	**175**	**175**	**175**	**175**	**175**
Operating Temperature Extreme: Ambient (°C)									

Table AP2a Single-chip Packages Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Low-cost, Hand Held and Memory	**55**	**55**	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**	**45**
High-performance	**55**	**55**	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Harsh	**-40 to 150**	**-40 to 150**	**-40 to 175**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**
Harsh-complex ICs	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

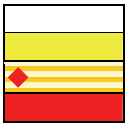


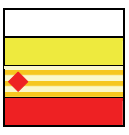
Table AP2b Single-chip Packages Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Cost per Pin Minimum for Contract Assembly (Cents/Pin)							
Low-cost, hand-held and memory	**.20-.32**	**.20-.30**	**.2-.29**	**.2-.27**	**.2-.26**	**.19-.25**	**.19-.25**
Cost-performance	**.44 - .75**	**.42 - .71**	**.39 - .68**	**.37 - .64**	**.35 - .61**	**.33-.58**	**0.32-0.55**
High-performance	**1.15**	**1.09**	**1.04**	**0.99**	**0.94**	**0.89**	**0.85**
Harsh	**.20 - 1.40**	**.20 - 1.33**	**.20 - 1.26**	**.20 - 1.20**	**.20 - 1.14**	**.19-1.08**	**.19-1.03**
Chip size (mm^2)							
Low-cost/hand held	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Cost performance	**140**	**140**	**140**	**140**	**140**	**140**	**140**
High performance (FPGA)	**750**	**750**	**750**	**750**	**750**	**750**	**750**
Harsh	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Maximum Power ($Watts/mm^2$)							
Hand held and memory (Watts)	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Cost-performance (MPU)	**1.07**	**1.12**	**1.19**	**1.27**	**1.24**	**1.63**	**1.73**
High-performance (MPU)	**0.42**	**0.42**	**0.44**	**0.43**	**0.42**	**0.43**	**0.43**
Harsh	**0.28**	**0.28**	**0.29**	**0.29**	**0.29**	**0.3**	**0.3**
Core Voltage (Volts)							
Low-cost	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Hand-held and memory	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Cost-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.9**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**
Package Pin count Maximum							

Table AP2b Single-chip Packages Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Low-cost	**229 - 1200**	**240 - 1200**	**252 - 1250**	**265 - 1250**	**278 - 1250**	**292- 1300**	**306- 1300**
Cost performance	**880– 4930**	**960- 5423**	**960– 5966**	**1050- 6562**	**1050 - 7218**	**1155- 7940**	**1155- 8337**
High performance (FPGA)	**6501**	**6826**	**7167**	**7525**	**7902**	**8297**	**8712**
Harsh	**599**	**629**	**660**	**693**	**728**	**764**	**803**
Minimum Overall Package Profile (mm)							
Low-cost, hand held and memory	**0.2**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**
Cost-performance	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**
High-performance	**0.9**	**0.9**	**0.9**	**0.9**	**0.8**	**0.8**	**0.8**
Harsh	**0.6**	**0.6**	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**
Performance: On-Chip (GHz)							
Low-cost/Hand held	**1438 - 9154**	**1510 - 9612**	**1586 - 10092**	**1665 - 10597**	**1748 - 11127**	**1835- 11683**	**1927- 12268**
Cost-performance	**9.18**	**9.89**	**10.65**	**11.47**	**12.36**	**13.32**	**14.34**
High-performance	**9.18**	**9.89**	**10.65**	**11.47**	**12.36**	**13.32**	**14.34**
Harsh	**250**	**275**	**302**	**333**	**366**	**403**	**443**
Performance: Chip-to-Board for Peripheral Buses (MHz)							
Low-cost Logic/Memory to MPU clock	**150/1200**	**150/1200**	**150/1200**	**150/1200**	**150/1200**	**150/1200**	**150/1200**
Cost-performance (for multi-drop nets)	**1200**	**1200**	**1200**	**1200**	**1200**	**1200**	**1200**
High-performance (for differential-pair point-to-point nets) (GHz)	**34.93**	**41.91**	**46.10**	**50.71**	**55.78**	**61.36**	**67.50**
Harsh	**150**	**150**	**150**	**150**	**150**	**150**	**150**
Maximum Junction Temperature							
Low-cost, Hand Held and Memory	**125**	**125**	**125**	**125**	**125**	**125**	**125**
Cost performance	**90**	**90**	**90**	**90**	**90**	**90**	**90**
High-performance	**90**	**90**	**90**	**90**	**90**	**90**	**90**
Harsh	**220**	**220**	**220**	**220**	**220**	**220**	**220**
Harsh-complex ICs	**175**	**175**	**175**	**175**	**175**	**175**	**175**
Operating Temperature Extreme: Ambient (°C)							
Low-cost, Hand Held and Memory	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**
High-performance	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Harsh	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**	**-40 to 200**
Harsh-complex ICs	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



ELECTRICAL REQUIREMENTS

Manufacturing tolerances have a major impact on the performance of electrical designs. The manufacturing tolerance roadmap reflected by the tables, for via diameter, via alignment, metal thickness, line width and dielectric thickness must be aligned with the electrical requirements. The major issues defining requirements for single chip packages are discussed below.

CROSS TALK

Circuit speed and density continue their improvements from one CMOS generation to the next. Faster circuits translate into shorter clock cycles and increased density gives rise to more closely spaced parallel threads. These device advancements demand increased package I/O at ever-increasing speed. These advanced circuits require packages that minimize device, package, and system noise

A major noise source is crosstalk between parallel signal lines. Crosstalk noise is roughly proportional to the ratio of dielectric thickness to edge spacing between adjacent signal lines. For a given signal line width and spacing, a lower dielectric constant medium requires a thinner dielectric to obtain the same characteristic impedance, resulting in smaller crosstalk noise. Cross talk issues are also associated with fine pitch bonding wires and fine pitch vias.

POWER INTEGRITY

Power integrity issues are becoming more critical for high-speed integrated circuits as frequency and increases and operating voltage decreases. Discrete decoupling capacitors are extensively used today to damp AC noise. The Equivalent Series Inductance (ESL) associated with discrete capacitors is the major factor limiting performance at high frequency. Embedded planar capacitors and on-die decoupling cells are used to reduce high-frequency noise due to high ESL in discrete capacitors. The cost and complexity of on-die decoupling will be an increasing problem. Due to resonance between package and die and package and PCB, it is difficult to control power distribution impedance over a wide frequency range. This results in a packaging related bottle-neck in high-speed power delivery system design and new technology is required.

THERMAL REQUIREMENTS

Temperature control is critical for the both operating performance and long term reliability of single chip packages. The high junction-to-ambient thermal resistance resulting from an air-cooled heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of this roadmap. Today, a massive heat sink, which may be larger than the chip by orders of magnitude, is attached to a Si chip through a heat spreader and variety of thermal interface materials (TIM). Not only does this insert a large thermal resistance between the chip and the ambient, it also limits the chip packing density in electronic products thereby increasing wiring length, which contributes to higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses. The ITRS projected power density and junction-to-ambient thermal resistance for high-performance chips at the 14 nm generation are >100 W/cm^2 and <0.2 °C/W, respectively. The main bottlenecks in reducing the junction-to-ambient thermal resistance are the thermal resistances of the thermal interface material (TIM) [1] and the heat sink. There is a need for TIMs that provide the highest possible thermal conductivity, are mechanical stable during chip operation, have good adhesion, and conform to fill the gaps between two rough surfaces. To address this need, new TIMs are being explored. The integration of carbon nanotubes (CNTs), which exhibit very high thermal conductivity, within a TIM's matrix is being investigated [1, 2]. More detail on these materials can be found in the Emerging Research Materials chapter.

HOT SPOTS

Hot spot thermal management generally dictates the thermal solution of the component. Even when the total power of a component is unchanged, hot spot power density increase could limit the device performance. While this is a critical issue for SiP it is also important for single chip devices such as SoC circuits, high power lasers and diodes, RF devices and other high power devices that have portions of the die generating thermal loads substantially higher than the die average.

New liquid and phase change (liquid to gas) active heat sinks are in limited use today and are addressed in more detail in the System in Package section of this chapter. They hold the promise of decreased thermal resistance and improved heat spreading capability to address the effect of hot spots.

MECHANICAL REQUIREMENTS

The constant drive for increased functionality and flexibility in the end product will be the key driver for the electronic industry in future. With shorter design turns and faster time to market, there is little room for error during the design, development, and validation phases. The continued geometric scaling of integrated circuits and the introduction of low-κ dielectric film materials raise concerns about mechanical stress damage in the dielectric layers due to thermo-mechanical stresses in the combined package device structure. Legislative requirements for lead free and halogen free materials in electronic products introduced higher temperature stresses and new packaging materials and materials interfaces into the package. New package types including stacked die packages, Package on Packages (PoPs), Package in Packages (PiPs), and wafer level packages have brought forth new failure mechanisms. The packaging industry will face the challenge of integrating multiple device technologies such as digital, RF and MEMS, optoelectronics, displays and others on the same packaging platform. Expanding consumer markets introduced new paradigms in reliability requirements. For example drop tests, in various forms, are being added to components to be used in cell phones and other portable electronic products. To ensure reliability of the end products, it is imperative to have focused R&D efforts in mechanical and thermal modeling and simulation tools.

MECHANICAL MODELING AND SIMULATION

Electronic packages represent a classic case of convergence of multi-scale, multi-physics, multi materials, and multi-materials interface systems. The length scale varies from nm to cm, a wide range of materials with mechanical properties from stiff and brittle inorganics like Si, glass and other dielectrics with property modifications such as micro-pores to achieve low-κ, to softer materials like solders or polymers and polymer composites with very non-linear time and temperature dependent material behaviour are combined. Material response varies from elastic to non-linear in time-temperature dependent characteristics. It is critically important to have practical and usable tools for predictive thermal mechanical and dynamic modeling of electronic packaging structures to assist packaging engineers in predicting failure modes and elucidate the failure mechanisms in the development stages. This would enable trade-offs in design, materials and manufacturing processes, and ultimately in feature, performance, cost, and time to market. Such predictive modeling tools would need to be integrated into device package co-design environments. Coupled analysis for thermal, electrical, hydrothermal, and mechanical characteristics is also needed.

To complement mechanical analysis and modeling efforts, it is necessary to develop accurate materials properties data over a range of loading and environmental conditions. Characterization of interface properties such as polymer/metal and polymer/polymer interface fracture toughness and micromechanical properties is required. A key challenge in this area is associated with the small dimensions. Bulk properties are often not usable for thin material layers. Interface effects, grain size and pre-stresses due to process or adjacent materials become very important. Metrologies are needed that can handle thin films of sub-micron thickness to measure both bulk and interfacial response. Properties of materials such as intermetallics formed from solder underbump metallurgy (UBM) metals interaction which grow and evolve over time and temperature will be required. Physical failure mechanisms such as electromigration, thermal migration in combination with mechanical stresses need to be understood and modeled for practical life assessment.

There is also a need to develop metrologies that can be used to efficiently measure either stress or strain under both thermal and mechanical loading conditions in thin films (for example in layers within Silicon) in packaged form. For example, interferometry-based techniques with sub-micron resolution are required whereas the current state of art methods have spatial resolution of 1 to 2 μm. Efforts are needed in extending other known techniques such as digital image correlations, micro-Raman spectroscopy, and PZT sensors to sub-micron length scales.

COST

The continuous reduction in cost per function has been the key to growth of the electronics industry. This has been achieved historically through scaling of the wafer fabrication processes and improvements in design. The cost of assembly and packaging has not kept pace with the cost reduction in wafer fabrication and today packaging costs often exceed silicon IC fabrication cost. The cost reduction challenge is made more difficult by several factors increasing cost of packaging. Lead-free solder materials, low-κ dielectrics,

and high-κ dielectrics are more costly than the materials they replace. Higher processing temperatures and a wider range of environmental temperature associated with portable consumer electronics require new, more expensive, substrate and interconnect technology. The increasing power density and decreasing junction temperature require more efficient thermal management.

New technology is required to meet the demand for more cost effective packaging. Wafer-level packaging and systems in a package (SiP) are among the innovative approaches to reduce cost and achieve advantages of scaling similar to the front end processes.

RELIABILITY

Rapid innovation in packaging is evident from the introduction of new package formats including area array packages; leadless packages, direct chip attach, wafer level packaging (WLP), and others. In addition there are new packaging requirements emerging such as Cu/low-κ materials, interconnects to address the need for flexibility and expanding heat and speed requirements. New environmental constraints such as Pb-free and halogen-free requirements enforced by law, and use of electronics in extreme environments also force rapid changes. The introduction of these new materials and structures are posing new reliability challenges. This comes at a time when there must be substantially higher reliability on a per transistor basis to meet market requirements.

Some new package designs, materials, and technologies will not be capable of the reliability required in all market applications. More in-depth knowledge of failure mechanisms coupled with knowledge of end product use conditions will be required to bring reliable new package technologies into the market-place.

There are many factors that determine the reliability of electronic components. The factors that must be considered are similar for all systems but the relative importance changes for consumer products. Consumer products have higher thermal cycle count due to the use pattern of consumer electronics and greater mechanical stress due to vibrations and dropping for the same reason.

The storage and use environments also have a wider range than components not used in consumer applications. Meeting the reliability requirements for future components will require tools and procedures that are not yet available. These include:

- Failure classification standards
- Identification of failure mechanisms
- Improved failure analysis techniques
- Electrical/thermal/mechanical simulation
- Lifetime models with defined acceleration factor
- Test vehicles for specific reliability characterization
- Early warning structures

The use of low-κ ILD to reduce on-chip interconnect parasitic capacitance has exacerbated the difficultly of maintaining high thermomechanical reliability of die assembled on organic substrates [3, 4]. Due to the fragile nature of low-κ ILDs and their relatively poor adhesion to the surrounding materials, it is becoming progressively critical to minimize stresses imparted on the chip during thermal cycling and wafer-level probing. The large CTE mismatch between the silicon die (3 ppm/°C) and the organic substrate (17 ppm/°C) have been shown to be destructive for ILD materials and their interfaces. This issue has motivated the investigation of new I/O interconnect technologies that minimize mechanical stresses on the chip. To this end, new underfill materials will be needed. In addition, the use of solder bumps augmented with mechanically flexible electrical leads to replace underfill is a potential solution.

In addition to compliant/flexible interconnects, thin solder interconnects and micro-bumps (diameter: <20 μm) as well as Cu pillar bump structures (Figures AP1 and AP2) are used to improve interconnect reliability. The selection of the type will depend on die sizes, thickness and interconnect density.

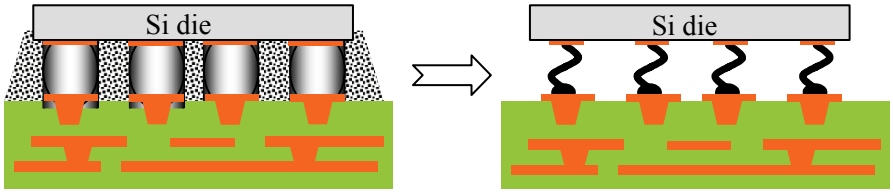
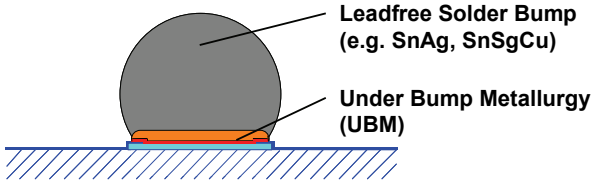
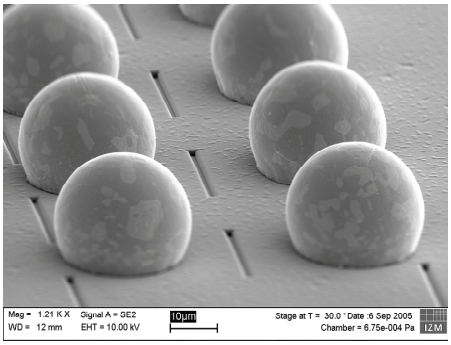


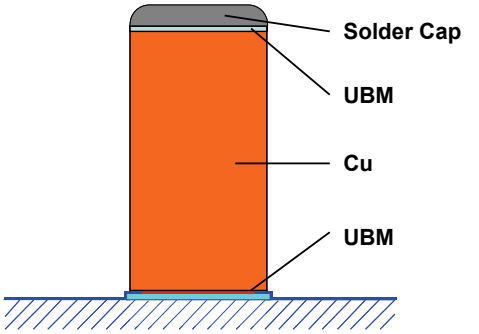
Figure AP1 The Use of Compliant/Flexible Electrical I/O Can Potentially Eliminate the Need for Underfill



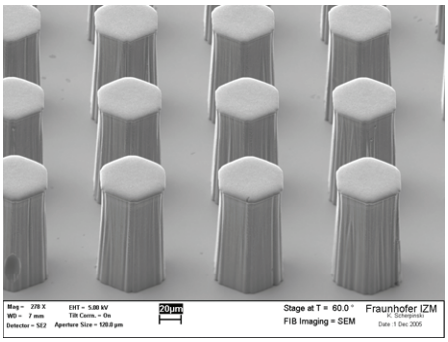
Schematic construction of a solder bump



SnAg microbump (20 µm diameter)



Schematic construction of a HAR (High Aspect Ratio) Cu pillar bump with solder cap



Cu pillar bump (height: 80 µm)

Figure AP2 Micro Bump and Pillar Bump Structures for High Reliable Chip-to-substrate Interconnects

CHIP TO PACKAGE SUBSTRATE

The number of connections types between the die and the package substrate is expanding to meet the demands of new package types. These are addressed in Table AP3a and b below. This table does not cover the characteristics of through silicon via (TSV) and direct bonding of wafers to wafers and die to wafers since these technologies are used primarily for 3D packaging and SiP applications that are covered in the System in Package section of this chapter. In addition to wirebond and flip chip, novel interconnect

approaches are emerging with the chip connected directly to a board or substrate via thin film technology and solder balls (see the Wafer Level Packaging section.

Table AP3a Chip-to-package Substrate Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Wire bond—single in-line (micron)	**40**	**35**	**35**	**35**	**30**	**30**	**30**	**30**	**25**
Two-row Staggered Pitch (micron)	**55**	**50**	**45**	**45**	**45**	**40**	**40**	**40**	**40**
Three-tier Pitch (micron)	**60**	**60**	**60**	**55**	**55**	**50**	**45**	**45**	**45**
Wire bond—Wedge pitch (micron)	**25**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Tape-automated Bonding (TAB)	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Flying Lead (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Flip Chip Area Array (both organic and ceramic substrate)(micron) (ASIC)	**130**	**130**	**130**	**130**	**120**	**110**	**110**	**100**	**100**
Flip Chip Area Array (organic substrate)(micron) (CPU, GPU, Chipset)	**160**	**160**	**150**	**150**	**150**	**130**	**130**	**130**	**110**
Flip Chip on Tape or Film (micron)	**25**	**15**	**10**	**10**	**10**	**10**	**10**	**10**	**10**

Table AP3b Chip-to-package Substrate Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Wire bond—single in-line (micron)	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Two-row Staggered Pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Three-tier Pitch (micron)	**45**	**45**	**45**	**45**	**45**	**45**	**45**
Wire bond—Wedge pitch (micron)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Tape-automated Bonding (TAB)	**35**	**15**	**15**	**15**	**15**	**15**	**15**
Flying Lead (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Flip Chip Area Array (both organic and ceramic substrate)(micron) (ASIC)	**100**	**95**	**95**	**95**	**90**	**90**	**90**
Flip Chip Area Array (organic substrate)(micron) (CPU, GPU, Chipset)	**110**	**110**	**110**	**100**	**100**	**100**	**100**
Flip Chip on Tape or Film (micron)	**10**	**10**	**10**	**10**	**10**	**10**	**10**

Notes for Table AP96a and b:

For very fine pitch chip to package bonding, alternative technologies such as TSV and bumpless interconnect will be used as alternatives to technologies in this table.

Finer pitch is technically possible for most categories but does not meet cost constraints.

WIRE BONDING

Wire bonding has been the workhorse of the semiconductor industry. It is the dominant method for interconnecting to semiconductor device. IC devices, wire bonded to various forms of lead frames and organic substrates and molded in epoxy molding compounds have been the standard of the industry for years. Despite repeated predictions that wire bond technology has reached its practical physical limit, wire bond technology continues to re-invent itself with new innovative concepts and technology improvements.

Multi-tier wire bonding has provided good practical solutions to meet increased IO requirements. Wire bonded stack die packaging has proved to be a versatile method for SiP and memory packaging.

In order to meet thinner and more densely integrated package requirements lower profile wire bond loops are necessary. Innovations such as forward bond loops with 50 µm loop height are in production. See Figure AP3.

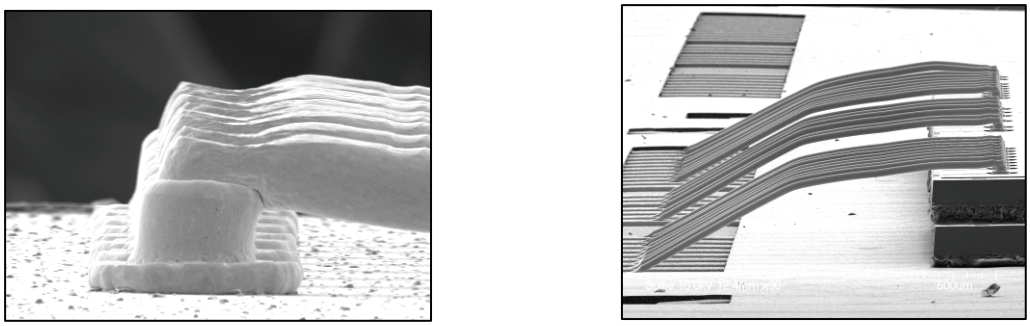


Figure AP3 Examples of Forward Bond Loop

Another alternative is to use reverse bonding where 50 µm loop heights with 20 µm wire have been successfully demonstrated. Shown below in Figures AP4–AP5 are examples of die-to-die bonding in side-by-side packages and cascade bonding die that have been stacked in a stair case.

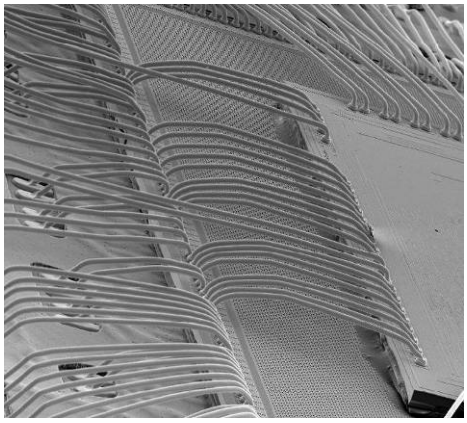


Figure AP4 Example of Die- to- die Wire Bonding

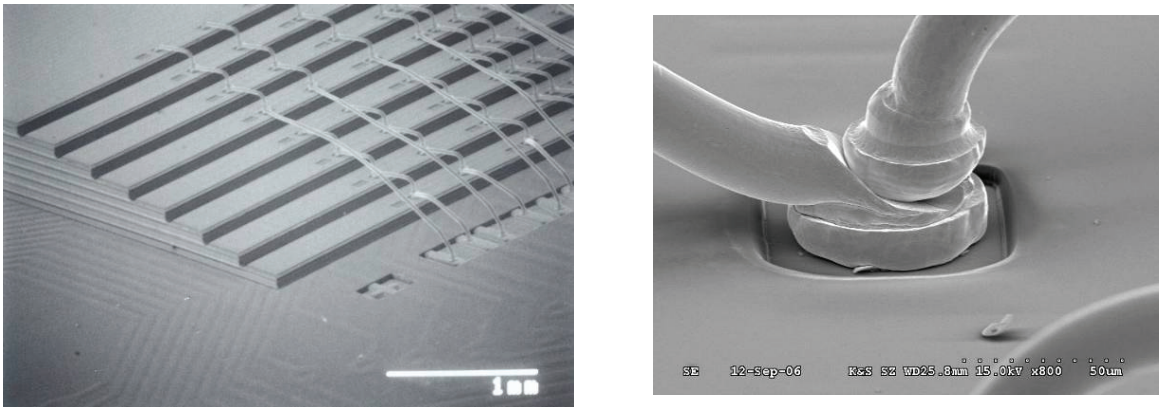


Figure AP5 Example of Cascade Bonding

Some of the technology issues being addressed are bonding overhang die and wire bonding on both sides of the lead frame shown in Figures AP6 and AP7.

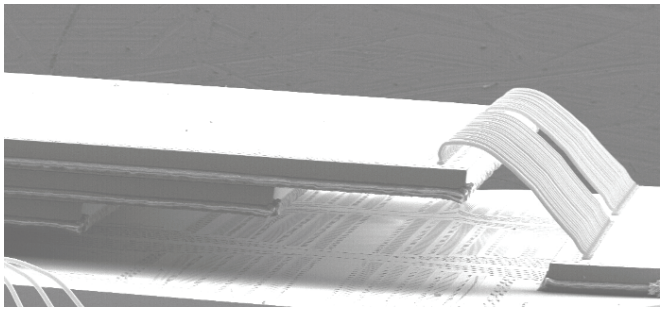


Figure AP6 Bonding Overhang Die

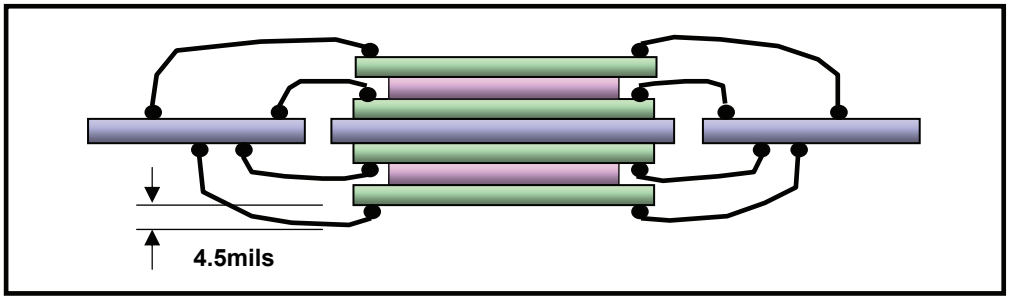


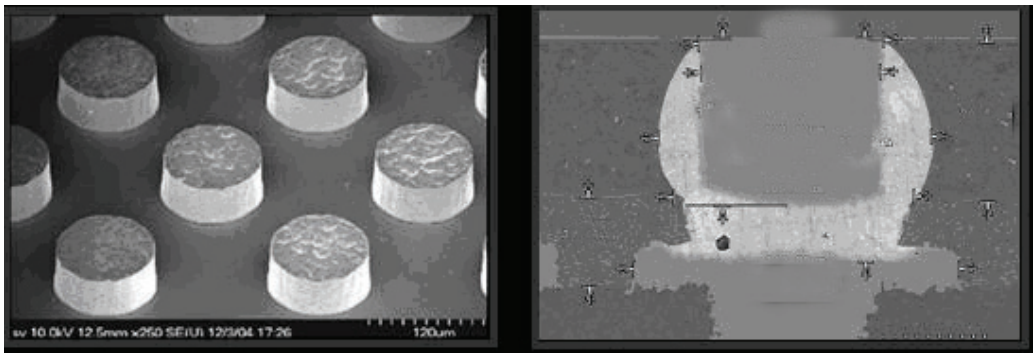
Figure AP7 Wire Bond on Both Sides of Lead Frame Substrate

There is a well established global infrastructure and supply chain for wire bonded and molded packages from design practices and tools, materials, manufacturing processes, and equipment. For die stacking the near-term challenges include lower profile bonding to meet the drive for smaller form factor and low profile consumer electronic products. Improvements in molding compound materials, i.e., flow and filler size are needed for these low profile packages. The industry has been developing faster wire bonders, larger format substrate assembly, and more efficient molding processes to address the market demand for efficiency and cost saving. In a wire bond package the cost of gold wire is a significant fraction of the total package cost. The reduction of gold wire diameter to 20 μm for lower pitch applications has provided cost

benefit in the face of historic high gold price. In the long term such cost improvements efforts are approaching their practical limits and are of diminishing returns. The work ongoing in the industry to lower cost wire bond materials, i.e., copper versus gold wire, may contribute to continue the cost reduction trend for this interconnect technology. While copper wire bond has been in use for 50 µm wire diameter and thick bond pads, for general fine pitch applications replacing gold wire with copper wire utilizing the existing infrastructure would require very significant efforts across the supply chain.

FLIP CHIP

Flip chip and wire bond are the two standard processes to connect die to a substrate. Flip chip processes were originally developed for multi-chip applications on ceramic modules. It has become the standard die interconnect solution for organic substrates for microprocessors and graphics processors. The key elements are: wafer bumping (UBM and bump metallurgy), underfill, TIM, and build-up substrates. For these applications flip chip pitch, at 150 µm, is limited by availability of high-volume cost-effective substrates and high-volume defect-free underfill processes, with higher Pb-free temperature, higher Tj, and increased current density, there are requirements to improve underfills, UBM structure, high lead solder and lead free alternatives, and TIM materials in order to meet the demands of future technology nodes and market applications. Copper pillar wafer bumping is being introduced in microprocessor applications. The advantages are in electrical/thermal performances with the potential for lead-free bump implementation.



(a) *(b)*

Figure AP8 Examples of Copper Pillar Bumps (a) and Assembled Copper Pillar (b)

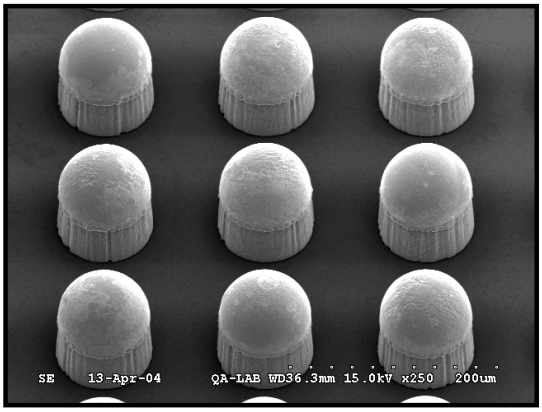


Figure AP9 Example of Copper Pillar Bumps with Solder Tips

For applications beyond the microprocessor, graphics and game processors, flip chip packages have other technical requirements. For example die are typically smaller with lower IO array pitch, smaller UBM

openings, and low profile small package format requirements. Drop tests are important in mobile applications. Relative cost of buildup substrates may be too high. These flip chip packages may be stacked onto other flip chip and wire bond packages. Analog and RF ICs have different electrical requirements than digital only applications. Potential solutions include redesigned UBM, copper pillar or flexible interconnect, large format overmolding (no underfill) processes, fluxless reflow and PoP and PiP package structures. There is an opportunity for a new generation of flip chip structures, materials, manufacturing processes and equipment sets to serve the industry for the More than Moore era.

MOLDING

Conventional bottom-gate molding has been a highly successful workhorse for the industry. For some complex stack dice and complex SiP package there is risk for excessive wire sweep and yield loss. New developments in top center mold gate (TCMG) provides a radial mold compound flow from a top gate that minimizes wire sweep and filler separation that can occur as the fine pitch bond wires filter out part of the fillers as the compound moves between them. There is also avenue for reducing stress on the substrate compound interface during de-gate as the contact is smaller and the breaking stress can be optimized by various design features. TCMG requires a smaller clearance from the top die, allowing a thinner package, particularly important for molding mold cap below 300 μm.

Also compression molding is just entering the market. The liquid mold compound is dispensed onto the substrate before it is placed into the mold die. No gate is needed and the mold flow speed is minimized preventing wire sweep. A new approach presently under investigation is underfill molding for flip chip in package solutions.

Thin packages are prone to warpage, and chips with low-κ dielectrics are more sensitive to stress. In both cases, low modulus molding compounds are in development to minimize the problems.

A novel approach to reduce or eliminate the occurrences of wire shorts in molding is the use of coated wire. Coated wire has been in development for some years and has achieved some level of technical success. However the high cost of coated wire has limited its application and prevented its broad proliferation into the industry.

To reduce stack heights, new materials that allow direct die attach to the top of the bonded wires with subsequent reflow around the wires are now being explored. This approach would adds cost to the process but may be more easily deployed as it is a substitutional cost increment and not completely additional.

PACKAGE SUBSTRATE TO BOARD INTERCONNECT

LEAD FRAMES

Lead frame carriers have thrived for their low cost and good reliability for more than 30 years. They are expected to continue to thrive with innovations in package design and processes. New material related challenges appeared because environmental and health regulatory requirements demand the elimination of Pb. The move from Pb to Sn led to the challenge of tin whiskers, a topic which is not yet fully understood. For improved reliability and low-cost new plating materials are required, e.g., based on NiPd, Cu, lead-free solder alloys. Other challenges include improved heat dissipation and higher interconnect density including increased pin count capability for platforms such as QFN and QFP.

HIGH DENSITY CONNECTIONS

The density of connections between the package substrate and the system printed circuit board continues to increase and the size of devices for a given functionality and the number of contacts required continues to increase. The increase in pin count is driven by the requirement to maintain power integrity and the increasing width of the data communication. Ensuring power integrity in an environment where operating voltage is decreasing and the number and speed of the transistors is increasing requires a larger number of contacts to handle the larger current spikes without fluctuations in power or ground. The slow improvement in board line width and spacing would provide some board routing density increase, but there is better opportunity for this density increase by reducing BGA pad pitch on board and package.

The greatest contact density in conventional packages will be available for the fine pitch ball grid array (FBGA) packages which are projected to reach 100 μm area array pitch in 2014. The higher density and resulting smaller pads bring issues related to joint reliability and package ball co-planarity requirement. The

joint reliability needs to be achieved through innovations in pad design, innovations in solder metallurgy and surface finishes, and in some cases use of board level underfill. The co-planarity issue needs to be addressed through improvements in substrate material and design, better understanding of package behavior at high temperature, and working with process flow to do key co-planarity sensitive operations prior to solder ball attach. The package to printed circuit board pitch for existing package types is presented in Table AP4a and b. Greater contact density will be in use for die-to-system substrate and die-to-die interconnect architectures using TSV structures.

Table AP4a Substrate to Board Pitch—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
BGA Solder Ball Pitch (mm) Conventional system Board									
Low-cost and hand-held*	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**
Harsh	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**
Small portable products									
Low-cost and hand-held	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
CSP area array pitch (mm)	**0.2**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.1**	**0.1**
QFP lead pitch (mm)	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.2**
SON land pitch (mm)	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
QFN land pitch (mm)	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
P-BGA ball pitch (mm)	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**
T-BGA ball pitch (mm)	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
FBGA ball pitch (mm)	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
FLGA land pitch (mm)	**0.4**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**

** Minimum number driven by hand held applications*

Table AP4a Substrate to Board Pitch—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
BGA Solder Ball Pitch (mm) Conventional system Board							
Low-cost and hand-held*	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Small portable products							
Low-cost and hand-held	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
CSP area array pitch (mm)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
QFP lead pitch (mm)	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
SON land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
QFN land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
P-BGA ball pitch (mm)	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**
T-BGA ball pitch (mm)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
FBGA ball pitch (mm)	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**	**0.15**
FLGA land pitch (mm)	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**

** Minimum number driven by hand held applications*

PACKAGE SUBSTRATES

ORGANIC SUBSTRATES

Package substrates are both the most expensive element of packages and the factor limiting package performance. Innovation in package substrate technology is required to meet the cost and performance projections of the Roadmap. The substrate properties required to meet market demand are shown in Table AP5 a through d.

Film type resins dominate as dielectrics for build-up substrates. Reinforcements of the film with fillers, mainly unwoven aramid, are being introduced. These materials improvements are driven by the need for reduced feature size, lower thermal expansion, electrical characteristics improvements, etc. Core layer materials essentially follow the trend of rigid substrates with aramid as additional reinforcing material. Liquid crystal polymers (LCP) and other thermoplastic resins as dielectric films are available but implementation in volume is only emerging.

High frequency applications drive the use of PTFE and cyanate materials. Coreless substrates are not in high volume production applications because these substrates have a tendency to warp during assembly. High volume manufacturing requires greater substrate stiffness with improved tolerance for warpage. These trends in substrate materials are progressing concurrently with the environmentally driven modifications to improve temperature robustness for lead-free assembly and to achieve halogen-free flame retardation.

High-speed transmission characteristics drive the demand for ever decreasing dielectric constant and low loss materials. Incremental materials improvements enable κ~3.4 today. Materials are available with κ down to 2.8 but are still too expensive for broad market application. There is no cost effective solution available for κ~2.5 and below. For such low κ, new reinforcement materials need to be developed. Thermoplastic resins with high heat resistance based on olefine systems seem feasible as well as new materials discussed in the Emerging Research Materials chapter of this Roadmap. These include the development of porous systems. Dielectric loss needs to be reduced by one order of magnitude. While PTFE and some cyanate resins achieve this, cost effective solutions are not yet available.

The drive to halogen-free resin systems is frequently met at the expense of dielectric properties. Therefore, a dedicated effort to develop new, low-cost materials with low dielectric constant and low loss that are halogen-free is necessary.

As copper thickness shrinks in traces and PTHs, these features become susceptible to thermal expansion in the z-direction. Hence, CTE in z-direction must be reduced to 20 ppm/degree for core materials and to 10 ppm/degree for build-up dielectrics. The typical approach is to add filler to the resin system which typically degrades other material properties or introduces process disadvantages.

Adhesion of copper traces is primarily by physical adhesion: rough, dendritic copper anchoring in the resin. The typical roughness of Rz= 5 µm is approaching the base Cu thickness and thereby becomes a significant portion of the skin of the conductor. There is a need for chemical adhesion for smooth copper to dielectric materials. Copper adhesion has to be sufficiently strong to survive processing until the traces and lands can be encapsulated with more dielectrics and/or solder mask.

BUILD-UP AND CORELESS SUBSTRATES

The advent of organic substrates changed the structure of high-performance flip chip packages to through hole technology based on printed wiring boards. The invention of build-up technology introduced redistribution layers over cores. While the build-up layers employed fine line technology and blind vias, the cores essentially continued to use printed wiring board technology albeit with shrinking hole diameters.

The next step in the evolution of substrates was to develop high density cores where via diameters were reduced to the scale of blind vias, i.e., 50 µm. The initial applications were based on PTFE dielectrics with metal alloy cores to manage package stresses. The full advantage of the dense core technology will be realized when lines and spaces are reduced to 25 µm or less. Thin photo resists (<15 µm) and high adhesion, low profile copper foils are essential to achieve such resolution.

In parallel, coreless substrate technologies are being developed. One of the more common approaches is to form vias in a sheet of dielectric material and fill the vias with metal paste to form the basic building block. A second building block is formed by laminating copper foil on both sides of the basic building block.

Subsequent circuitization completes this second building block. By laminating the appropriate selection of building blocks, a raw substrate is formed which only needs external finishing. Variations of this process are to form the building blocks on carrier sheets as single layers of circuitry which are the transferred by lamination to the composite stack. In either case, the dielectric materials have little or no reinforcing material. Control of dimensional stability during processing will be essential. While different coreless technologies with proprietary designs and processes are emerging, significant market development is required to broaden the supply base, ensure stable quality and force cost reduction.

RIGID SUBSTRATE TECHNOLOGY

Rigid substrates may be divided by their application spaces: handheld and high performance. Handhelds are driving ever thinner substrates. Total thickness has been reduced to 120 µm based on 60 µm cores in high volume manufacturing. 50 µm cores and 35 µm prepregs are available but cost is very high and improvements in handling equipment are needed to take these materials to high volume. The next stage will have to be film based materials like liquid crystalline polymers. To overcome the hurdles of processing these thin and fragile materials, roll-to-roll processing may have to be introduced.

High performance packages with wire bonded die are utilizing high density substrates with blind vias in laminate, essentially a build-up technology using prepreg instead of unreinforced resin. To achieve finer resolution, glass cloth with more uniform glass fiber density or glass mats will have to be developed while overall thickness of the resultant prepreg has to be reduced below 40 µm. Thereafter, film form resin systems with wire bonding resilience after lamination will have to be developed. In general, the lack of the latter type of materials is impeding the improvement of resolution of lines and spaces. The pattern formation itself is shifting from a subtractive process to pattern plating.

Mounting flip chip die and wirebond die on the same package, either side by side or stacked; provide challenges for substrate surface finish. A number of finishes can coexist organic solder preservative (OSP), immersion tin or pre-solder with electroplated nickel/gold versus electroless nickel immersion gold (ENIG) with electroplated nickel/gold. Each case requires a carefully tuned assembly and substrate manufacturing process to be successful in high volume. Hence, the search for a universal surface finish has been reinvigorated and electroless nickel electroless palladium immersion gold (ENEPIG) seems to be the most likely candidate. This surface can be wire bonded, flip chip soldered as well surface mount soldered. The cost of this universal finish seems to be acceptable as well.

Table AP5a Package Substrates—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Glass Transition Temperature (°C)									
Rigid Structure	220	230	230	230	230	230	230	230	230
Buildup with Reinforcement Material	220	230	230	230	230	230	230	230	230
Buildup without Reinforcement Material	200	210	210	210	210	210	210	210	210
Tape Structure	280	280	280	280	280	280	280	280	280
Dielectric Constant (at 1GHz)									
Rigid Structure	3.4	3.4	3.4	3	3	3	3	2.7	2.7
Buildup with Reinforcement Material	3	3	3	2.8	2.8	2.8	2.8	2.8	2.8
Buildup without Reinforcement Material	3	3	3	2.7	2.7	2.7	2.7	2.7	2.7
Tape Structure	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Ceramics Structure/Low Dielectric Material	4	4	3	3	3	3	3	3	3
Ceramics Structure/High Dielectric Material	100	100	100	100	100	100	100	100	100
Dielectric Loss (at 1GHz)									
Rigid Structure	0.013	0.013	0.013	0.013	0.01	0.01	0.01	0.01	0.01
Buildup with Reinforcement Material	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
Buildup without Reinforcement Material	0.007	0.007	0.005	0.005	0.005	0.005	0.005	0.005	0.005
Tape Structure	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.005
Ceramics Structure	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
Coefficient of Thermal Expansion: X-Y Direction (ppm/°C)									
Rigid Structure	12	10	10	8	8	8	8	6	6
Buildup with Reinforcement Material	12	10	10	10	10	10	10	10	10
Buildup without Reinforcement Material	40	20	20	20	20	10	10	10	10
Tape Structure	20	16	16	16	16	16	16	16	16
Ceramics Structure	3 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
Coefficient of Thermal Expansion: Z Direction (ppm/°C)									
Rigid Structure	30	25	25	25	25	20	20	20	20
Buildup with Reinforcement Material	30	20	20	20	20	20	20	20	20
Buildup without Reinforcement Material	40	20	20	20	10	10	10	10	10
Tape Structure	20	20	20	20	20	20	20	20	20
Ceramics Structure	3 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
Water Absorption at 23°C/24hrs Dipped (weight %)									
Rigid Structure	0.2	0.2	0.2	0.1	0.1	0.1	0.1	0.05	0.05
Buildup with Reinforcement Material	0.05	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Tape Structure	1	1	1	1	1	1	1	1	1
Young's Modulus (GPa)									
Rigid Structure	30	30	30	30	30	30	30	30	30
Buildup with Reinforcement Material	26	26	26	26	26	26	26	26	26
Buildup without Reinforcement Material	5	5	5	5	5	5	5	5	5
Tape Structure	3	3	3	3	3	3	3	3	3
Ceramics Structure	100-400	50–500	50–500	50–500	50–500	50–500	50–500	50–500	50–500
Peel Strength from Cu (kN/m)									
Rigid Structure	1.1	1.1	1.1	1.2	1.2	1.2	1.2	1.2	1.2
Buildup with Reinforcement Material	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4
Buildup without Reinforcement Material	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4
Tape Structure	1	1	1	0.8	0.8	0.8	0.8	0.8	0.8

Notes for Table ESH98a and b:

State of the art materials may not be compatible with cost requirements for volume production

Water absorption test is: JIS C6481

Peel strength test: IPC TM650 2.4.8

Table AP5b Package Substrates—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Glass Transition Temperature (°C)							
Rigid Structure	230	230	230	230	230	230	230
Buildup with Reinforcement Material	230	230	230	230	230	230	230
Buildup without Reinforcement Material	210	210	210	210	210	210	210
Tape Structure	280	280	280	280	280	280	280
Dielectric Constant (at 1GHz)							
Rigid Structure	2.7	2.7	2.7	2.7	2.7	2.7	2.7
Buildup with Reinforcement Material	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Buildup without Reinforcement Material	2.7	2.7	2.7	2.7	2.7	2.7	2.7
Tape Structure	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Ceramics Structure/Low Dielectric Material	3	3	3	3	3	3	3
Ceramics Structure/High Dielectric Material	100	100	100	100	100	100	100
Dielectric Loss (at 1GHz)							
Rigid Structure	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Buildup with Reinforcement Material	0.007	0.007	0.007	0.007	0.007	0.007	0.007
Buildup without Reinforcement Material	0.005	0.005	0.005	0.005	0.005	0.005	0.005
Tape Structure	0.005	0.005	0.005	0.005	0.005	0.005	0.005
Ceramics Structure	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
Coefficient of Thermal Expansion: X-Y Direction (ppm/°C)							
Rigid Structure	6	6	6	6	6	6	6
Buildup with Reinforcement Material	10	10	10	10	10	10	10
Buildup without Reinforcement Material	10	10	10	10	10	10	10
Tape Structure	16	16	16	16	16	16	16
Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
Coefficient of Thermal Expansion: Z Direction (ppm/°C)							
Rigid Structure	20	20	20	20	20	20	20
Buildup with Reinforcement Material	20	20	20	20	20	20	20
Buildup without Reinforcement Material	10	10	10	10	10	10	10
Tape Structure	20	20	20	20	20	20	20
Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
Water Absorption at 23°C/24hrs Dipped (weight %)							
Rigid Structure	0.05	0.05	0.05	0.05	0.05	0.05	0.05
Buildup with Reinforcement Material	0.04	0.04	0.04	0.04	0.04	0.04	0.04
Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Tape Structure	1	1	1	1	1	1	1
Young's Modulus (GPa)							
Rigid Structure	30	30	30	30	30	30	30
Buildup with Reinforcement Material	26	26	26	26	26	26	26
Buildup without Reinforcement Material	5	5	5	5	5	5	5
Tape Structure	3	3	3	3	3	3	3
Ceramics Structure	50–500	50–500	50–500	50–500	50–500	50–500	50–500
Peel Strength from Cu (kN/m)							
Rigid Structure	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Buildup with Reinforcement Material	1.4	1.4	1.4	1.4	1.4	1.4	1.4
Buildup without Reinforcement Material	1.4	1.4	1.4	1.4	1.4	1.4	1.4
Tape Structure	0.8	0.8	0.8	0.8	0.8	0.8	0.8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

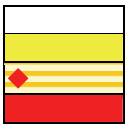


Table AP5c Package Substrate Design Parameters—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Substrate cross-section core thickness (µm)									
Handhelds	**40**	**35**	**35**	**30**	**30**	**30**	**25**	**25**	**25**
High density interconnect substrates	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**30**	**30**
Build-up substrates (4 core layers)	**200**	**150**	**130**	**100**	**90**	**80**	**80**	**70**	**70**
Coreless buildup layer	**40**	**40**	**35**	**35**	**30**	**30**	**30**	**30**	**30**
Blind via diameter (µm)									
Handhelds	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**25**	**25**
High density interconnect substrates	**50**	**40**	**40**	**35**	**35**	**30**	**30**	**25**	**25**
Build-up substrates	**40**	**35**	**35**	**30**	**30**	**25**	**25**	**20**	**20**
Coreless	**60**	**50**	**50**	**40**	**40**	**35**	**35**	**30**	**30**
Blind via stacks									
High density interconnect substrates	**3**	**3**	**3**	**3**	**4**	**4**	**4**	**4**	**4**
Build-up substrates	**5**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Coreless	**10**	**11**	**11**	**11**	**12**	**12**	**13**	**14**	**14**
PTH diameter (µm)	**75**	**70**	**60**	**50**	**50**	**45**	**45**	**40**	**40**
PTH land (µm)	**180**	**160**	**140**	**120**	**110**	**105**	**105**	**100**	**100**
Bump pitch (µm)									
High density interconnect substrates	**190**	**180**	**170**	**160**	**150**	**140**	**140**	**130**	**130**
Build-up substrates	**130**	**120**	**110**	**100**	**100**	**90**	**90**	**80**	**80**
Coreless	**130**	**120**	**110**	**100**	**100**	**90**	**90**	**80**	**80**
Lines/space width (µm)									
Rigid Structure	**35**	**30**	**30**	**25**	**25**	**22**	**22**	**20**	**20**
Build-up substrates (core layer)	**35**	**30**	**30**	**25**	**25**	**22**	**22**	**20**	**20**
Build-up substrate (build-up layer)	**15**	**10**	**10**	**10**	**9**	**8**	**8**	**6.8**	**6.4**
Coreless	**20**	**15**	**15**	**10**	**9**	**8**	**8**	**6.8**	**6.4**
Lines/space width tolerance (%)	**7**	**7**	**7**	**7**	**7**	**7**	**6**	**5**	**5**
Solder mask registration ± (µm)									
Handhelds	**20**	**15**	**15**	**15**	**12**	**12**	**11**	**10**	**10**
High density interconnect substrates	**20**	**15**	**15**	**15**	**12**	**12**	**11**	**10**	**10**
Build-up substrates	**25**	**20**	**20**	**15**	**12**	**12**	**11**	**10**	**10**

Table AP5d Package Substrate Design Parameters—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Substrate cross-section core thickness (µm)							
Handhelds	**25**	**25**	**25**	**25**	**25**	**25**	**25**
High density interconnect substrates	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Build-up substrates (4 core layers)	**70**	**70**	**70**	**70**	**70**	**70**	**70**
Coreless buildup layer	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Blind via diameter (µm)							
Handhelds	**25**	**25**	**25**	**25**	**25**	**25**	**25**
High density interconnect substrates	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Build-up substrates	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Coreless	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Blind via stacks							
High density interconnect substrates	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Build-up substrates	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Coreless	**14**	**14**	**14**	**14**	**14**	**14**	**14**
PTH diameter (µm)	**40**	**40**	**40**	**40**	**40**	**40**	**40**
PTH land (µm)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Bump pitch (µm)							
High density interconnect substrates	**130**	**130**	**130**	**130**	**130**	**130**	**130**
Build-up substrates	**80**	**80**	**70**	**70**	**70**	**70**	**70**
Coreless	**80**	**80**	**70**	**70**	**70**	**70**	**70**
Lines/space width (µm)							
Rigid Structure	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Build-up substrates (core layer)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Build-up substrate (build-up layer)	**6.0**	**5.6**	**5.3**	**5.0**	**4.7**	**4.4**	**4.1**
Coreless	**6.0**	**5.6**	**5.3**	**5.0**	**4.7**	**4.4**	**4.1**
Lines/space width tolerance (%)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Solder mask registration ± (µm)							
Handhelds	**10**	**10**	**10**	**10**	**10**	**10**	**10**
High density interconnect substrates	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Build-up substrates	**10**	**10**	**10**	**10**	**10**	**10**	**10**

WAFER LEVEL PACKAGING

Originally wafer level packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at wafer level. This WLP definition requires that all package IO terminals to be continuously located within the chip outline (fan-in design) producing a true chip size package. From a systems perspective, the limitation on WLP is how many I/O can be placed under the chip and still have a board design that can be routed. WLP can provide a solution when requirements for continued decrease in size, increase in IC operating frequency and demand for cost reduction are not met by traditional packaging e.g. wire bonding or flip chip bonding. WLP technology also includes wafer level chip size package (WLCSP), wafer capping on a MEMS, and a wafer level substrate featuring fine traces and embedded integrated passives.

Wafer Level CSP was the first generation of a wafer level package product introduced into the market place. Today WLP technology (fan-in WLP) with and without redistribution layer (RDL) is used for a large variety of products. WLPs with fan-in design today are typically for low I/O count and small die sizes. They are mainly being used in portable consumer markets where small size, thickness, and weight are an additional advantage to cost. A major trend is to work for cost efficient rerouting with multi-layer RDL.

WLP now incorporates many different structures to meet specific application targets. The variety of WLP types are shown in Figure AP10 below. Table AP6a and b present the technology requirements.

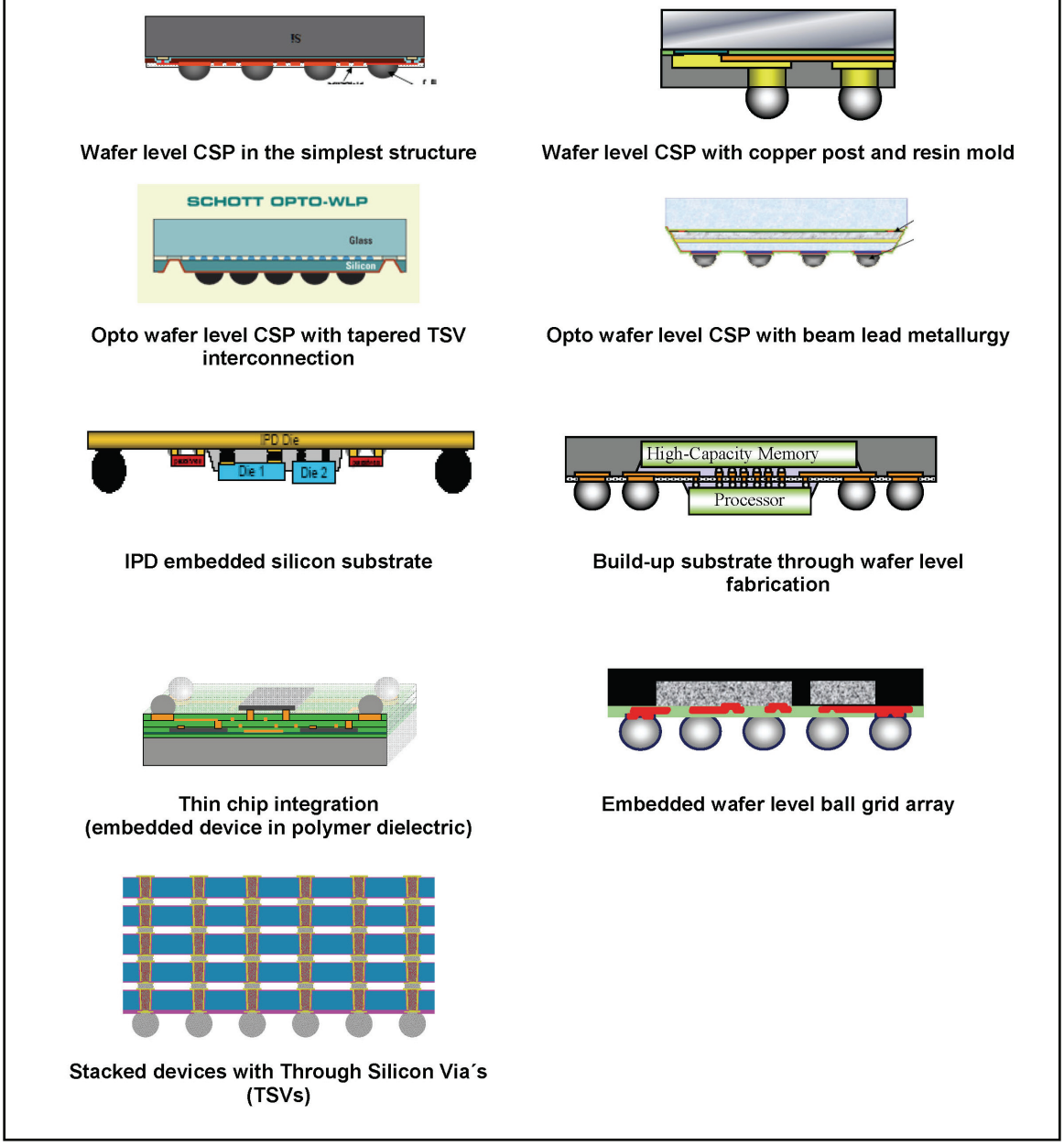


Figure AP10 Examples of Wafer Level Packaging Types

Table AP6a Wafer Level Packaging—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Cost per Ball Minimum/Maximum for Contract Assembly [1,2] (Cents/Pin)									
a. Standard Logic and Analog/Linear Min	**0.25**	**0.21**	**0.18**	**0.15**	**0.13**	**0.12**	**0.12**	**0.11**	**0.11**
b. Standard Logic and Analog/Linear Max	**0.55**	**0.47**	**0.40**	**0.34**	**0.29**	**0.27**	**0.26**	**0.25**	**0.23**
Chip size (mm^2) (Min/Max)									
a. Memory	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**
b. Standard Logic and Analog/Linear	**0.85/9**	**0.75/10**	**0.55/11**	**0.50/12**	**0.45/13**	**0.40/14**	**0.35/15**	**0.30/15**	**0.25/16**
c. Wireless: Bluetooth, FM, GPS, WIFI	**.85/16**	**.75/25**	**.55/29**	**.50/34**	**0.45/36**	**0.40/38**	**0.35/40**	**0.30/42**	**0.25/46**
Ball Metallurgy	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**
Number of RDL Layers									
a. Memory	**1**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**
b. Standard Logic and Analog/Linear	**1**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**
c. Wireless: Bluetooth, FM, GPS, WIFI	**1**	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**
UBM Thickness (μm)									
a. Memory	**1.5-10μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**
b. Standard Logic and Analog/Linear	**1.1-10μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**	**1.1-50μm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**1.5-10μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**	**1.5-50μm**
UBM Metallurgy									
a. Memory	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**
b. Standard Logic and Analog/Linear	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu, Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**

Table AP6a Wafer Level Packaging—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
c. Wireless: Bluetooth, FM, GPS, WIFI	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu, Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**
RDL Thickness									
a. Memory	**2-10µm**	**2-12µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
b. Standard Logic and Analog/Linear	**2-10µm**	**2-12µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**2-10µm**	**2-12µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
RDL Metallurgy									
a. Memory	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**
b. Standard Logic and Analog/Linear	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**
c. Wireless: Bluetooth, FM, GPS, WIFI	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**
Wafer Saw Street Width (µm)									
a. Memory	**85µm**	**75µm**	**70µm**	**65µm**	**60µm**	**60µm**	**55µm**	**50µm**	**45µm**
b. Standard Logic and Analog/Linear	**50µm**	**50µm**	**40µm**	**40µm**	**35µm**	**35µm**	**35µm**	**30µm**	**30µm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**85µm**	**75µm**	**70µm**	**60µm**	**55µm**	**55µm**	**50µm**	**45µm**	**40µm**
Package Pincount Maximµm									
a. Memory	**150**	**175**	**200**	**200**	**225**	**250**	**275**	**275**	**275**
b. Standard Logic and Analog/Linear	**36**	**64**	**64**	**144**	**151**	**159**	**167**	**175**	**184**
c. Wireless: Bluetooth, FM, GPS, WIFI	**100**	**150**	**150**	**150**	**165**	**165**	**165**	**180**	**180**
Embedded components thickness (µm) (Max/Min)									
a. Memory	**100**	**100**	**100**	**75**	**75**	**75**	**75**	**70**	**70**
b. Standard Logic and Analog/Linear	**250/100**	**225/100**	**200/100**	**175/75**	**175/75**	**175/75**	**175/75**	**150/70**	**150/70**
c. Wireless: Bluetooth, FM, GPS, WIFI	**100**	**100**	**100**	**75**	**75**	**75**	**75**	**70**	**70**
Type of WLP structure and metallurgy (bump, ball, column, solder, Cu, other)									
a. Memory	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**

Table AP6a Wafer Level Packaging—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
b. Standard Logic and Analog/Linear (P= polymer)	**2ML/2P/ Plated Cu/Solder Bump/Ball**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**
c. Wireless: Bluetooth, FM, GPS, WIFI (P=Polymer)	**2ML/2P/ Plated Cu/Solder Bump/Ball**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**
Stacked Die Wafer Level CSP (Max. dies)									
a. Memory	**1**	**1**	**1**	**4**	**4**	**8**	**8**	**8**	**8**
b. Standard Logic and Analog/Linear	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
c. Wireless: Bluetooth, FM, GPS, WIFI	**2**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Stacked Die Wafer Level CSP Interconnect method (Through silicon vias, face to face, others)									
a. Memory	**Piggyback on underside**	**Piggyback on underside**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**
b. Standard Logic and Analog/Linear	**Piggyback on underside. Std. stacked die with wire bond**	**Piggyback on underside. Std. stacked die with wire bond, F2F**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**
c. Wireless: Bluetooth, FM, GPS, WIFI	**Piggyback on underside**	**Piggyback on underside, F2F**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**

Table AP6b Wafer Level Packaging—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Cost per Ball Minimum/Maximum for Contract Assembly [1,2] (Cents/Pin)							
a. Standard Logic and Analog/Linear Min	**0.10**	**0.10**	**0.09**	**0.09**	**0.08**	**0.08**	**0.07**
b. Standard Logic and Analog/Linear Max	**0.22**	**0.21**	**0.20**	**0.19**	**0.18**	**0.17**	**0.16**
Chip size (mm^2) (Min/Max)							
a. Memory	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**	**20 / 250**
b. Standard Logic and Analog/Linear	**0.20/16**	**0.18/17**	**0.16/17**	**0.14/18**	**0.12/19**	**0.11/20**	**0.10/20**
c. Wireless: Bluetooth, FM, GPS, WIFI	**0.20/48**	**0.18/50**	**0.16/52**	**0.14/54**	**0.12/56**	**0.11/58**	**0.10/60**
Ball Metallurgy	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**	**SAC**
Number of RDL Layers							
a. Memory	**3**	**3**	**3**	**3**	**3**	**3**	**3**
b. Standard Logic and Analog/Linear	**3**	**3**	**3**	**3**	**3**	**3**	**3**
c. Wireless: Bluetooth, FM, GPS, WIFI	**3**	**3**	**3**	**3**	**3**	**3**	**3**
UBM Thickness (µm)							
a. Memory	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**
b. Standard Logic and Analog/Linear	**1.1-50µm**	**1.1-50µm**	**1.1-50µm**	**1.1-50µm**	**1.1-50µm**	**1.1-50µm**	**1.1-50µm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**	**1.5-50µm**
UBM Metallurgy							
a. Memory	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**CuNi, TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**
b. Standard Logic and Analog/Linear	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**

Table AP6b Wafer Level Packaging—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
c. Wireless: Bluetooth, FM, GPS, WIFI	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**	**TiCuNi, TiCu, Al/NiV/Cu, Ti/NiV/Cu, TiW/Cu,Cr-Cu**
RDL Thickness							
a. Memory	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
b. Standard Logic and Analog/Linear	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**	**2-15µm**
RDL Metallurgy							
a. Memory	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**
b. Standard Logic and Analog/Linear	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**	**Al;TiAlTi;Cu**
c. Wireless: Bluetooth, FM, GPS, WIFI	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**	**Al; TiAlTi; Cu; Al/Cu**
Wafer Saw Street Width (µm)							
a. Memory	**45µm**	**40µm**	**40µm**	**40µm**	**35µm**	**35µm**	**35µm**
b. Standard Logic and Analog/Linear	**30µm**	**25µm**	**25µm**	**25µm**	**20µm**	**20µm**	**20µm**
c. Wireless: Bluetooth, FM, GPS, WIFI	**40µm**	**35µm**	**35µm**	**35µm**	**30µm**	**30µm**	**30µm**
Package Pincount Maximum							
a. Memory	**275**	**275**	**275**	**275**	**275**	**275**	**275**
b. Standard Logic and Analog/Linear	**193**	**203**	**213**	**223**	**235**	**246**	**259**
c. Wireless: Bluetooth, FM, GPS, WIFI	**180**	**195**	**195**	**195**	**210**	**210**	**210**
Embedded components thickness (µm) (Max/Min)							
a. Memory	**70**	**65**	**65**	**65**	**60**	**60**	**60**
b. Standard Logic and Analog/Linear	**150/70**	**140/65**	**140/65**	**140/65**	**135/60**	**135/60**	**135/60**
c. Wireless: Bluetooth, FM, GPS, WIFI	**70**	**65**	**65**	**65**	**60**	**60**	**60**
Type of WLP structure and metallurgy (bump, ball, column, solder, Cu, other)							
a. Memory	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**	**Ball**

Table AP6b Wafer Level Packaging—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
b. Standard Logic and Analog/Linear (P= polymer)	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**
c. Wireless: Bluetooth, FM, GPS, WIFI (P=Polymer)	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**	**2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar**
Stacked Die Wafer Level CSP (Max. dies)							
a. Memory	**8**	**8**	**8**	**12**	**12**	**12**	**12**
b. Standard Logic and Analog/Linear	**3**	**3**	**3**	**3**	**3**	**3**	**3**
c. Wireless: Bluetooth, FM, GPS, WIFI	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Stacked Die Wafer Level CSP Interconnect method (Through silicon vias, face to face, others)							
a. Memory	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**
b. Standard Logic and Analog/Linear	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**
c. Wireless: Bluetooth, FM, GPS, WIFI	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**

The manufacturing process technology and high volume infrastructure enabling wide spread implementation of Wafer Level CSP in the market place have been based upon the adoption and implementation of established flip chip wafer bumping (under bump metallurgy, solder bumping, re-passivation, redistribution, wafer inspection, wafer probing) processes and equipment in the merchant market. The infrastructure has been developed to serve the high volume needs of flip chip packaging in the high performance and cost performance markets.

In contrast to flip chip assembly WLP assembly typically does not require underfill. For solder joining solder balls are used with a diameter larger than 250 μm. The smallest pitches used in the market are 0.4 mm. For standard WLP under-fill is used to meet specific reliability requirement such as drop test.

The traditional drop ball WLCSP designs and processes are being further developed with stress absorbing layers, underfill in board level assembly, and stress absorbing bump structures to allow for larger die applications. Copper trace redistribution features have been introduced for higher power and lower signal loss applications.

The processes developed for copper redistribution are being introduced and extended to the fabrication of copper studs and passive components such as inductors, to be followed by capacitors and resistors. The combination of these components will lead to capabilities for the fabrication of filters. Integration of these components into WLP-SiP packages constitutes a next step towards 3D wafer integration.

Memory devices are being used in portable consumer products such as cell phones and PDAs in increasing quantities. WLP offers advantages in these applications, due to inherent lower cost, improved electrical performance, and lower power requirements. Key enabling technologies to take full advantage of WLP for these applications will be the development of cost effective wafer level test and burn-in.

WAFER LEVEL PACKAGE DEVELOPMENTS AND TRENDS

Today, WLP developments are motivated by the recognition that wafer level processing technology, i.e., parallel processing on the wafer, open additional alternatives to traditional packaging and assembly. WLP includes not only processing on active devices, but also processing of silicon dice with integrated passives, or other substrates such as glass leading to wafer level substrates. For package substrates, fine design rules and capability of creating integrated passive devices are attractive features. Dielectric and traces are built on silicon substrate by wafer process technology and the following assembly is performed on the wafer level substrate. Some wafer level substrates are not made of silicon but dielectric layers and traces built up on a wafer, which was removed in the manufacturing process.

For the package substrate, fine design rules, and capability of creating integrated passive devices are attractive features. Dielectric and traces are built on silicon substrates by wafer process technology and the assembly is performed on the wafer level substrate. Some of the wafer level substrates are not made of silicon but dielectric layers and traces built up on a wafer.

Currently, different technologies at wafer level are in development to satisfy the need to increase performance and functionality while reducing size, power, and cost of the system. This development leads to more complex packages for both single and multi-die Wafer Level Packages.

The wafer level CSP may incorporate copper post terminals with thicker resin coat providing a package that is more durable to the rough handling and more tolerant of CTE mismatch. This package is used for a variety of the applications from power amplifier to CPU with the ball pitches as fine as 0.20 mm.

The wafer level CSP specialized for image sensing is a glass-sealed optical wafer level CSP. Die are sandwiched or laminated on the circuit side by clear glass and terminals are routed to the reverse side of the die via TSV or beam-lead metallurgy extending to the side of the die.

FUTURE TRENDS FOR WAFER LEVEL PACKAGING

Developments needed to meet the future requirements of wafer level packaging are:

- Reduction of processing temperatures, particularly for dielectric curing
- Wafer-level substrates with passives in silicon or passives in RDL

- Integrated passive structures into the RDL by thin film polymer deposition
- Embedded active and passive devices
- Wafer-level assembly—die to wafer—of Si (memory, MPU), MEMS, III/V (InP, GaAs, GaN etc.) and SiGe devices
- Integrated shielding (RF and power)
- Functional layers integration (actuators, sensors, antennas)
- Through-silicon-via (TSV) formation and metallization, wafer thinning and adjusted bonding technologies for stacked dies on wafer
- Optical chip to chip interconnects

The development of wafer level packaging (WLP) is proceeding in several directions:

- Processes for larger die and higher functionality application based on RDLs (fan-in)
- Fan-out approaches (see various Embedded Wafer Level Package approaches)
- Higher complexity applications such as System in Package (SiP) with chip to wafer and 3D configurations and passive device integration. This includes face-down and face up approaches on active Si devices, carriers with passives, etc.
- New applications such as multiple IC stacks (memories, processor-ASIC-memories, MEMS); based on through silicon via (TSV) technology.
- Wafer to wafer stacks
- These WLP technologies are driven by market demand for higher integration density and system capability (See SiP section)

DIFFICULT CHALLENGES FOR WLP

Wafer level Packages are expected to have better reliability even for larger die with small ball pitch. The physical structure and the materials used are being refined to satisfy the requirements of specific application. This is a particular challenge for MEMS devices.

Key challenges include:

- Board level reliability especially for large die
- Testing of wafer level stacked packages and new 3D architectures with multiple die
- Vias through chip (WLP) and package (for embedded wafer level architectures)
- Thin package profile using very thin silicon die for extreme thin applications
- Mechanical tolerances required for chip alignment to small pads
- Contacts on small pads
- High reliable(electromigration, drop test) I/O pad metallization (UBM; Solder)
- Topology of multilayer RDL
- Topology for thick metals for high current
- Metal roughness for RF (skin effect)
- Cross talk on chip because of small vertical distance
- Yield and defect repair possibilities for embedded WLP products

EXAMPLES FOR EMERGING WAFER LEVEL PACKAGE TECHNOLOGIES:

THROUGH SILICON VIA (TSV) FOR 3D INTEGRATION

The realization of vertical interconnected devices/chips using through silicon vias is one of the key emerging trends in wafer level packaging. This technology offers significant advantages in terms of electrical performances, e.g., signal transmission, interconnect density and reduced power consumption as well as form factor, heterogeneous integration, and manufacturing cost reduction. Today new approaches

are in development to incorporate TSVs into the Front End (FE)-CMOS process or as a post-CMOS process with VIA first or VIA last process (see Figure AP11).

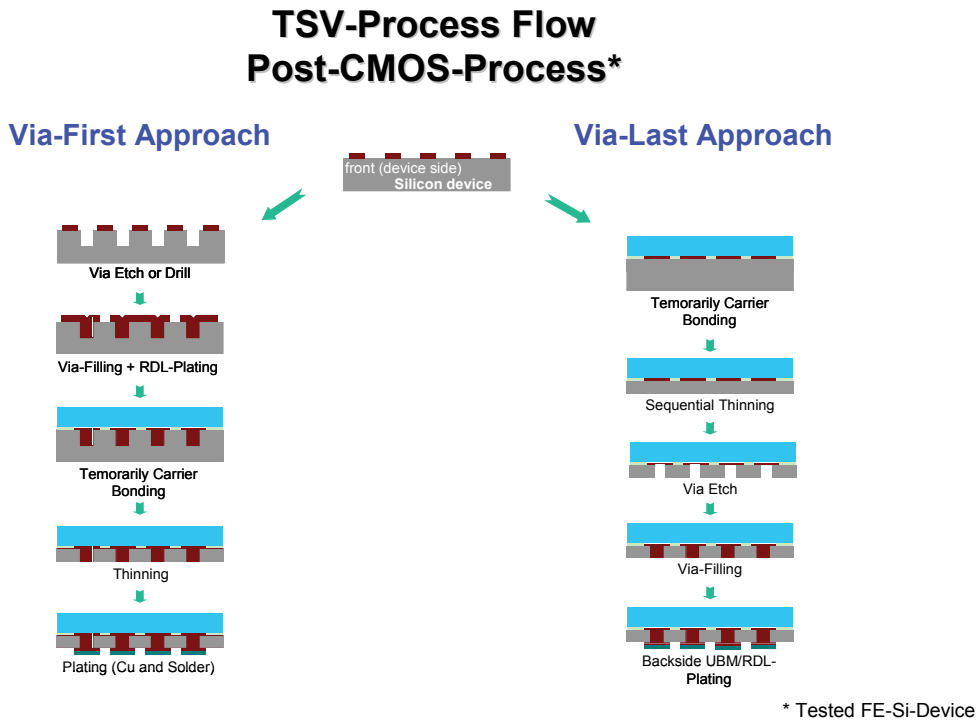


Figure AP11 Basic Process Flow Via-first versus Via Last

The implementation of TSV into the front-end processes will be covered by the Interconnect chapter of this Roadmap; here some aspects from the assembly and packaging view point will be discussed. The basic processes for the TSV formation are via etching (DRIE, laser), insulation, and metallization, which are well known from front-end processing. Additional processes which are required for the stack formation are wafer thinning, deposition of redistribution layer (RDL) and under-bump formation, wafer level bonding processes (die-to-wafer or wafer-to-wafer, e.g., micro bump soldering or Solid Liquid Interdiffusion (SOLID), as well as final encapsulation. Today the TSV process is demonstrated at the R&D level and only a few companies are running on product level. The transition from R&D demonstrations to high-volume processes requires viable business models, the development of an equipment infrastructure, and the existence of viable costs for competitiveness applications.

Key technical challenges for the TSV approach are:

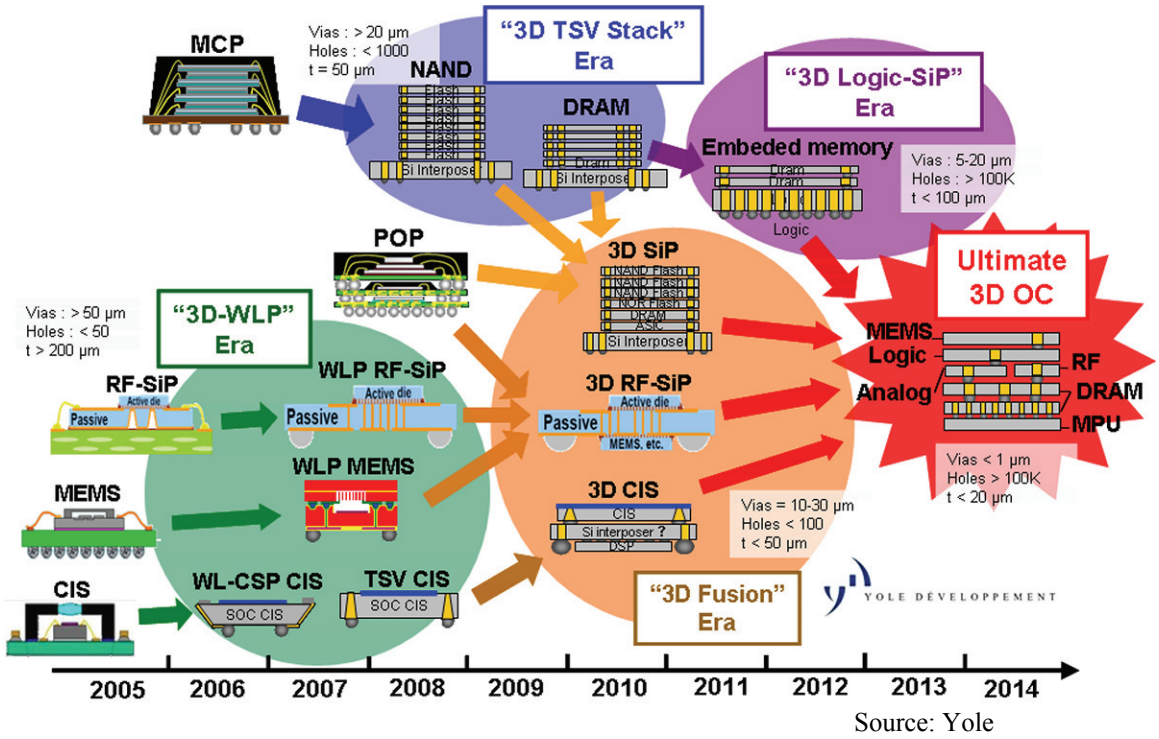
- High density and high aspect ratio via etching
- Low temperature processes for passivation and metallization
- High speed via filling (e.g., electroplating (Cu), CVD (Cu, W)
- Thinned wafer/device handling
- High speed and precise wafer level alignment and assembly processes (die-to-wafer and wafer-to-wafer)
- Testing and methodology
- Competitive cost

Table AP7 Key Technical Parameters for Stacked Architectures Using TSV

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Numbers of stacked die using TSV	3 – (8)	6	9	>9	>9	>9	>9
Minimum TSV pitch	10.0	8.0	6.0	5.0	4.0	3.8	3.6
TSV maximum aspect ratio**	10.0	10.0	10.0	10.0	10.0	10.0	10.0
TSV exit diameter(um)	4.0	4.0	3.0	2.5	2.0	1.9	1.8
TSV layer thickness for minimum pitch	50	20	15	15	10	10	10

***This applies for small diameter vias. The larger diameter vias will have a smaller aspect ratio.*

The first applications of TSV are used for CMOS image sensors and are in production today. Stacked die approaches for memory devices are in development and will be in high volume production by 2009. Future applications for stacked die with TSV will include mixed architectures like analog, logic, processor, memory, and sensors.



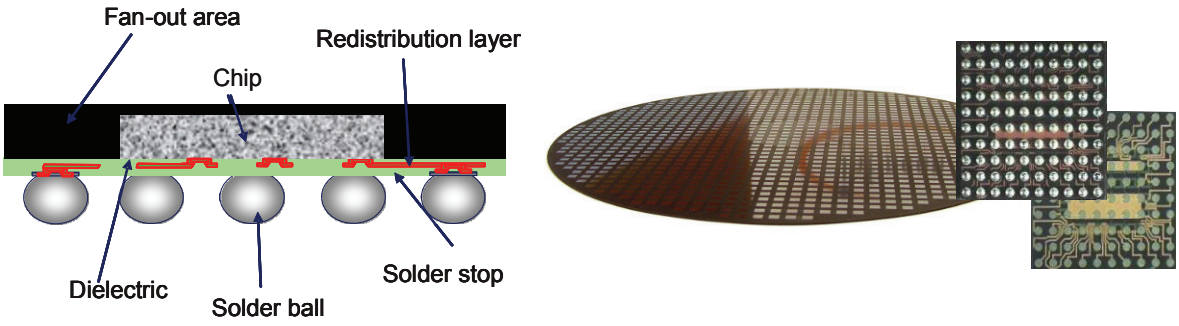
Source: Yole

Figure AP12 Roadmap for 3D Integration using TSV

FAN OUT WLP USING RECONFIGURED WAFER LEVEL TECHNOLOGIES

New package developments that appear on the horizon are fan out or embedded wafer level package technologies. These technologies allow higher integration density and fan-out solutions. For this new approach the chips are reconstituted and embedded in epoxy compound to build an artificial wafer. A thin film redistribution layer is applied (see Figure AP13) instead of a laminate substrate, which is typical for classical BGAs. Laminate substrates are reaching their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layer opens new opportunities for SiP. The possibility to integrate passives like inductors, capacitors or even active devices into the various thin film layers opens additional design possibilities for new SiP. There are other approaches that incorporate a copper pillar over ball integrated arrays. Special difficult challenges for these types of embedded wafer

level packages are their implementation in the packaging industry infrastructure from design to manufacturing, and surface mount assembly to the board and board level reliability.



Graphic courtesy of Infineon

Figure AP13 Example of a Side-by-side Solution of an Fanout WLP (a) and a Reconstituted Wafer (b)

SYSTEM IN PACKAGE

Predictions that Moore's Law has reached it limits have been heard for years and have proven to be premature. We are now nearing the basic physical limits to CMOS scaling and the continuation of the price elastic growth of the industry cannot continue based on Moore's law scaling alone. This will require "More than Moore" through the tighter integration of system level components at the package level. In the past scaling geometries enabled improved performance, less power, smaller size, and lower cost. Today scaling alone does not ensure improvement of all four items. The primary mechanism to deliver "More than Moore" will come from integration of multiple circuit types through SoC and SiP technology. The most important as the electronics industry becomes ever more dominated by the consumer will be System in Package. This will allow the efficient use of three dimensions through innovation in packaging and interconnect technology. The result will support continued increase in functional density and decrease in cost per function as the industry begins to reach the limit of conventional CMOS scaling.

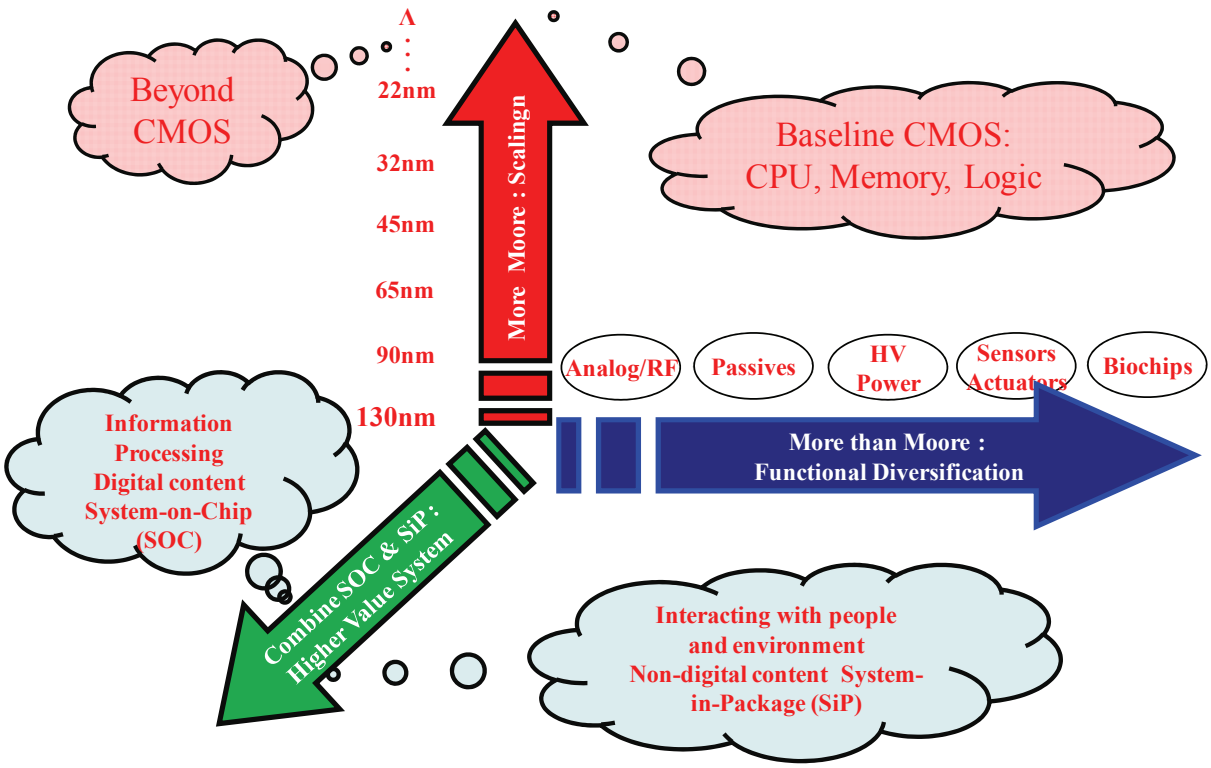


Figure AP14 Beyond CMOS Scaling

System in Package (SiP) technology is rapidly evolved from specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications. Numerous concepts for 3D SiP packaging are now emerging driven largely by the demands of portable consumer products.

A paper titled *"The Next Step in Assembly and Packaging: Systems Level Integration,"* prepared by the Assembly and Packaging Technical Working Group, addresses the requirements, challenges, and potential solutions required for continued improvement in cost and performance of electronics through systems level integration at the packaging level.[5]

The objectives are to:

- Disseminate information on the current state of the art,
- Foster formation of a consensus on the "best" SiP solutions
- Identify the areas where research is needed
- Encourage focus and industry wide cooperation to minimize technology development risks

This paper addresses the SiP technology in detail and we recommend that those interested in SiP technology use that paper as their reference.

DEFINITION OF SIP

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit, which provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components, and other packages and devices.

There are many types of SiP packages. They are divided into horizontal placement, stacked structures, and embedded structures. Examples of the major categories are shown in Figure AP15 below.

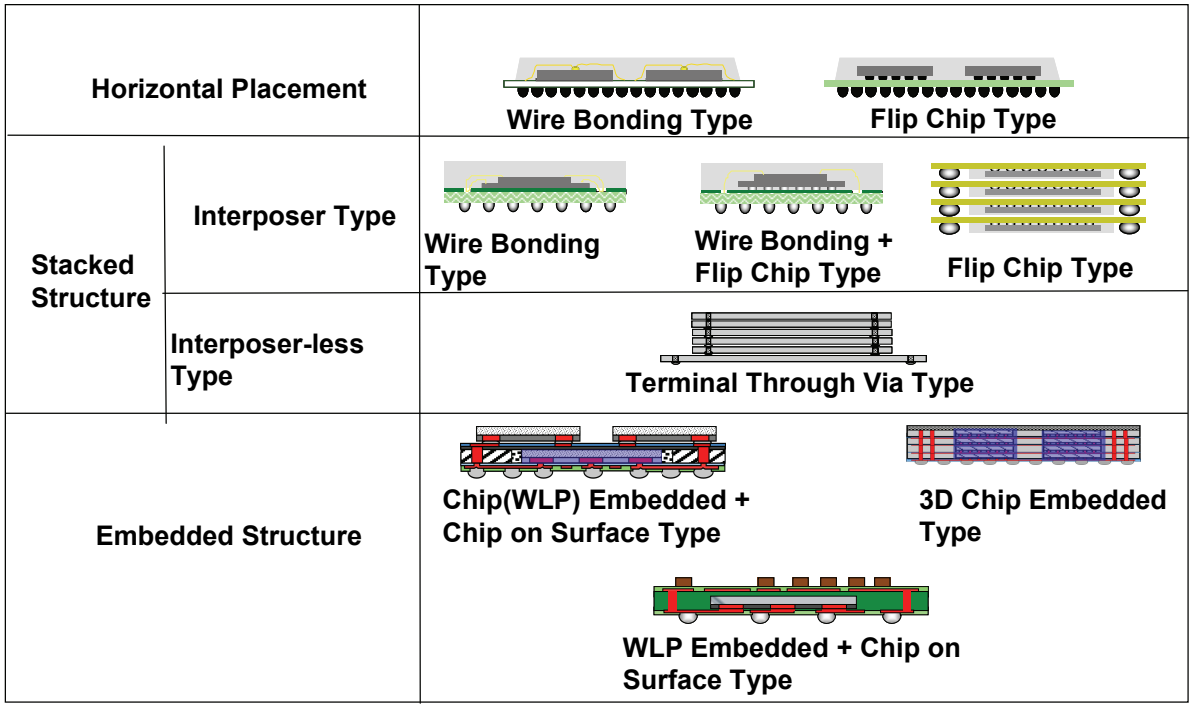


Figure AP15 Categories of SiP

SiP VERSUS SoC

The benefits of "More than Moore" can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future. The pros and cons for each architecture are outlined in the table below.

Table AP8 Comparison of SoC and SiP Architecture

Market and Financial Issues		
Item	**SiP**	**SoC**
Relative NRE cost	1×	4-10×
Time to Market	3–6 months	6–24 months
Relative Unit Cost	1×	0.2–0.8×
Technical Features PROs		
SiP	**SOC**	
Différent front end technologies; GaAs, Si, etc.	Better yields at maturity	
Different device generations	Greater miniaturization	
Re-use of common devices	Improved performance	
Reduced size vs. conventional packaging	Lower cost in volume	
Active & passive devices can be embedded	CAD systems automate interconnect design	
Individual components can be upgraded	Higher interconnect density	
Better yields for smaller chip sets	Higher reliability (not true for very large die)	
Individual chips can be redesigned cheaper	Simple logistics	
Noise & crosstalk can be isolated better		
Faster time to market		
Technical Features CONs		
SiP	**SOC**	
More complex assembly	Difficult to change	
More complex procurement & logistics	Single source	
Power density for stacked die may be too high	Product capabilities limited by chip technology selected	
Design Tools may not be adequate	Yields limited in very complex, large chips	
	High NRE cost	

SYSTEM LEVEL REQUIREMENTS

The general requirements for SiP are many and the relative importance varies with the application. These requirements include:

- Small and specialized form factors

- High functional density
- High frequency operation
- Large memory capacity
- High reliability
- Low package cost
- Low development cost
- Rapid time-to-market
- Wireless connectivity (GPS, Bluetooth, cellular, etc.)

The requirements for package level system integration are listed in Table 99 below.

Table AP9 Package Level System Integration

				2008	2010	2012	2014	2016	2018	2020	2022
				High Performance / Low Cost, Handheld							
Passives	**Capacitor**	O for YES		o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
	Resistor			o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
	Inductor			o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
Actives	**Optical**	o for YES		o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
	CCD/CMOS Sensor			-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
	MEMS			-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
Package Inner Structure	**IC to IC Connection**	o for Applicable	Wire	-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
			Flip Chip	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Via Hole	-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
	IC to Substrate Connection	o for Applicable	Wire	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Flip Chip	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Via/ TSV Hole	-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
	IC- RDL (carrier-less)			-/o	-/o	o/o	o/o	o/o	o/o	o/o	o/o
Integrated / Embedded Components		o for Applicable	IC	-/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
	Passives		Capacitor	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Resistor	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Inductor	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
Substrate Material	**Organic**	o for Applicable	Rigid	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Flexible	-/o	-/o	-/o	-/o	o/o	o/o	o/o	o/o
	Inorganic		Ceramic	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o
			Silicon	o/o	o/o	o/o	o/o	o/o	o/o	o/o	o/o

Package requirements for SiP cannot be met without modification to the single chip packaging processes and, in some cases, adopting new processes. The processes used for SiP are listed in Table AP10 and are grouped into pre-processing of wafers, die attach processes, interconnects, underfilling, via formation and metallization, wiring, and encapsulation.

Table AP10 Processes for SiP

Technologies and Processes for SiP	*Substrate / Carrier Level*	*Wafer Level / 3D Integration*
Pre-processing of wafers		
Thinning, dicing	ca.50 µm	< 20 µm
Wafer bumping	Low cost, pitch> 100 µm	Fine pitch and bumpless
Re-configured Wafer		■
Die attach		
Epoxy	■	
Tape	■	
Soldering		■
Polymer		■
Interconnects		
Wire bonding	Low-loop bonding	
Flip-chip bump bonding	Mixed WB /FC	Size/pitch (>50 µm)
Face-to-face		Fine pitch (<10 µm)
		Thin interconnects
Bumpless/Seamless	Electroless	Thin film interconnects, fusion
Via formation	Photo, drilling, laser	Through silicon etching, photo
Via metallization	Plating, electroless	Electroplating, CVD
Wiring	Substrate wiring (see chapter substrates)	Thin film redistribution
Underfilling	Dispensing, jetting, underfill molding	Dispensing, jetting, underfill molding
Encapsulation	Molding	Molding
		Wafer/wafer (glass) bonding
Second Level Interconnect	Solder balls	Solder balls, (Cu studs)

Legend: ■ most preferred used

The highest levels of integration are achieved through three dimensional packaging. Die stacking has been used for consumer products such as cell phones for several years with wire bonding used to connect the stacks to the package substrates. The newest technology to emerge is the use of TSV to allow more efficient die stacking. Table AP11a and b lists the major parameters that address SiP die stacking technology. The primary limitation that results in the coloring cells is thermal management limitations. High performance devices require management of high heat loads which is difficult to accomplish with stacked die. New approaches will be required to meet the Roadmap projections.

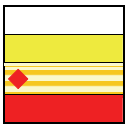
Table AP11a System in Package Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Number of terminals—low cost handheld	**700**	**800**	**800**	**800**	**800**	**800**	**800**	**800**	**800**
Number of terminals—high performance (digital)	**3050**	**3190**	**3350**	**3509**	**3684**	**3860**	**4053**	**4246**	**4458**
Number of terminals—maximum RF	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**
Low cost handheld / die / stack	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**14**
High performance / die / stack	**3**	**3**	**3**	**4**	**4**	**4**	**5**	**5**	**5**
Low cost handheld / die / SiP	**8**	**8**	**9**	**11**	**12**	**13**	**14**	**14**	**14**
High performance / die / SiP	**6**	**6**	**6**	**7**	**7**	**7**	**8**	**8**	**8**
Minimum TSV pitch	**10.0**	**8.0**	**6.0**	**5.0**	**4.0**	**3.8**	**3.6**	**3.4**	**3.3**
TSV maximum aspect ratio	**10.0**	**10.0**	**10.0**	**10.0**	**10.0**	**10.0**	**10.0**	**10.0**	**10.0**
TSV exit diameter(um)	**4.0**	**4.0**	**3.0**	**2.5**	**2.0**	**1.9**	**1.8**	**1.7**	**1.6**
TSV layer thickness for minimum pitch	**50**	**20**	**15**	**15**	**10**	**10**	**10**	**10**	**8**
Minimum component size (micron)	**1005**	**600×300**	**600×300**	**400×200**	**400×200**	**400×200**	**200×100**	**200×100**	**200×100**
Maximum reflow temperature (°C)	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**

Table AP11b System in Package Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Number of terminals—low cost handheld	800	800	800	800	800	800	800
Number of terminals—high performance (digital)	4670	4904	5138	5394	5651	5934	6231
Number of terminals—maximum RF	200	200	200	200	200	200	200
Low cost handheld / die / stack	15	15	16	16	17	17	18
High performance / die / stack	6	6	6	7	7	7	8
Low cost handheld / die / SiP	15	15	16	16	17	17	18
High performance / die / SiP	9	9	9	10	10	10	11
Minimum TSV pitch	3.1	2.9	2.8	2.7	2.5	2.4	2.3
TSV maximum aspect ratio	10.0	10.0	10.0	10.0	10.0	10.0	10.0
TSV exit diameter(um)	1.5	1.5	1.4	1.3	1.3	1.2	1.1
TSV layer thickness for minimum pitch	8	8	8	8	8	8	8
Minimum component size (micron)	200×100	200×100	200×100	200×100	200×100	200×100	200×100
Maximum reflow temperature (°C)	260	260	260	260	260	260	260

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Stacking of multiple die as defined in Table AP11 will result in package thickness that exceeds Roadmap requirements for portable consumer products. The die thickness is defined in Table AP12a and b. The thickness limitation is not in the ability to thin the silicon. It is the thickness of the interconnect layers that are part of the die and the challenge of handling extremely thin die so that they maintain their performance that limits minimum thickness.

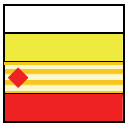
Table AP12a Thinned Silicon Wafer Thickness 200 mm/300 mm—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Min. thickness of thinned wafer (general product)	50	50	50	50	45	40	40	40	40
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)	20	20	15	15	10	10	10	10	8

Table AP12b Thinned Silicon Wafer Thickness 200 mm/300 mm—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Min. thickness of thinned wafer (general product)	40	40	40	40	40	40	40
Min. thickness of thinned wafer (For extreme thin package ex. Smart card)	8	8	8	8	8	8	8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



The progression of wafer thinning will reach 8 µm by the year 2015. This will pose a number of technical challenges for wafer thinning processes. The challenges associated with handling the thinned wafers and thinned singulated die will be even more difficult. Table AP12c lists the major challenges and potential solutions associated with the incorporation of thinned die into SiP and other electronic system architectures

Table AP12c Challenges and Potential Solutions in Thinning Si Wafers

CHALLENGES	POTENTIAL SOLUTIONS
Wafer thinning technology	Fine grinding wheel
Stress relief	Wet polishing, plasma, dry polish, CMP
Wafer handling technology	Inline B/G system
Singulation	Mechanical saw, laser saw, plasma etch
Die attach handling	Needle-less pick-up system, carrier-less wafer handling
Wire bonding on overhang thin die	Optimize O/H length and wire bonding parameters, Less dynamic impact bonding
Low loop wire bonding	Folded wire loop, Reverse wire bond
Molding thin gap	Liquid molding, compression mold, high flow molding compound, vacuum assist
Thinning on a bumped wafer	Mechanical handling innovation during and after thinning

SiP RELIABILITY CHALLENGES

Reliability, quality, and manufacturing yield are key prerequisites for the development of complex SiP applications. SiP present reliability challenges that require developments in reliability research, diagnostics, and failure analysis. These issues are covered briefly here and additional material can be found in the paper titled *"The Next Step in Assembly and Packaging: Systems Level Integration."*

The failure modes in SiP are not necessarily unique to SiP technology but the relative rate of occurrence may be influenced by the use cases and operational environment for SiP. The continued rapid increase in the number of transistors requires even more rapid increase in reliability to meet the application requirements. In addition the Classification of failure modes and failure mechanism are listed in Table AP13a and b below.

Table AP13 SiP Failure Modes

Basic Failure Mechanisms	#	Failure Origins and Driving Forces	Sip-Relevant Failure Examples	Fault Isolation and Failure Analysis Methods
A: Coherent crack formation	1	Thermomechanical mismatch	Chip solder fatigue BGA solder ball fatigue Fracture of an embedded passive component Die-to-die spacer crack Underfill crack IC metal line open	Stress analysis by thermoire-interferometry, speckle-interferometry (ESPI), deformation analysis by image correlation, x-ray diffraction Fault isolation by magnetic microscopy, time domain reflectance, lock in thermography, TIVA, OBIRCH Crack detection by scanning acoustic microscopy, cross section analysis with light microscopy, SEM or FIB/SEM
	2	Mechanical loading (application- or process-induced)	IC dielectric crack Organic substrate crack Solder ball crack (drop)	
	3	Hygroscopic swelling	Mold compound cracking, die cracking	
	4	Reaction-induced volume shrink or expansion (e.g. curing)	Mold compound cracking, die cracking	
	5	Internal pressure (e.g. moisture vaporization at increased temperature)	Mold compound cracking, die cracking	
B: Interfacial delamination	1-5	Same as 1-5	IC dielectric delamination Underfill delamination Delamination between stacked dies Organic substrate delamination Mold compound delamination	Stress analysis by thermoire-interferometry, speckle-interferometry (ESPI), deformation analysis by image correlation, x-ray diffraction Crack detection by scanning acoustic microscopy, cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM
	6	Interface reactions causing loss of adhesion (e.g. moisture-, oxidation-, contamination-related)	Underfill delamination Mold compound delamination Organic substrate delamination	Crack detection by scanning acoustic microscopy, cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM Surface analysis by TOF-SIMS, XPS, AES, TEM+EDX, TEM+EELS

Table AP13 SiP Failure Modes (continued)

Basic Failure Mechanisms	#	Failure Origins and Driving Forces	Sip-Relevant Failure Examples	Fault Isolation and Failure Analysis Methods
C: Void and pore formation	7	Mechanical creep	IC Solder ball fatigue BGA solder ball fatigue	Fault isolation by magnetic microscopy, time domain reflectance, lock in thermography, TIVA, OBIRCH Void detection by x-ray microscopy or x-ray tomography Cross section analysis with light microscopy, SEM or FIB/SEM (with EDX,WDX, EBSD and x-ray diffraction for analysis of intermetallics)
	8	Diffusion (Kirkendall void formation) and Intermetallic formation	IC UBM lift Void in IC interconnect or in via Wire bond lift BGA solder ball lift	
	9	Electromigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
	10	Thermomigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
D: Material decomposition and bulk reactions	11	Chemical corrosion	Bond wire lift	Fault isolation by magnetic microscopy, time domain reflectance, lock in thermography, TIVA, OBIRCH Failure analysis by Cross section analysis with light microscopy or based on FIB/SEM with EDX or WDX, TEM, TOF-SIMS, XPS, FTIR spectroscopy, , mechanical testing, TGA, DMA, DSC (ageing), EBSD (grain analysis)
	12	Galvanic corrosion	Bond wire lift	
	13	Ageing (UV, …)	Organic substrate cracking or delamination Underfill cracking or delamination	
	14	Grain coarsening, phase separation	Wire bond rupture IC solder ball fatigue BGA solder ball fatigue	

THERMAL MANAGEMENT

SiP has to provide the same thermal management for each component as in single chip packages. The SiP will generally have the most extreme variation in thermal density due to different power levels for difference classes of active components and the incorporation of passive components with little or no heat generation. This results in hot spots and potentially damaging stress levels due to thermal gradients and TCE mismatch between the materials. The move to three dimensional SiP with direct bonded TSV structures can multiple the heat load by the number of stacked die and reduce the surface area available for heat removal. The high junction-to-ambient thermal resistance resulting from an air-cooled heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of the roadmap.

COMPONENT TEMPERATURE LIMITS

The component temperature must be controlled because:

- The higher temperature will impact device performance (lower frequency)
- The higher temperature may result in higher leakage power, which is a waste of energy
- The higher temperature will result in faster degradation of the material property and reliability
    - The higher component temperature may also impact to its neighbors which may be sensitive to high temperatures

The component temperature limit is determined by its function, architecture, and design. For example, the typical Tj_max for microprocessor is about 100°C, while the typical Tj_max for memory device is about 85°C. Since the different devices inside the same SiP may have different functions, their Tj_max will be different from each other. In addition, the thermal design requirement for SiP needs to comprehend both the total package power dissipation and the individual component power dissipation.

The potential solutions must incorporate two elements. First is an improved thermal interface material (TIM) such as carbon nanotubes for efficiently spreading heat and removing thermal energy from the heat source to the heat sink. This alone cannot resolve the problem if the heat source produces more thermal energy than the heat sink can dissipate. This will require fluid heat transfer and several approaches have already in prototype.

Methods of forming CMOS process compatible thermofluidic heat sinks and the use of flip-chip microfluidic (micropipe) I/O interconnects have been recently reported [6, 7].

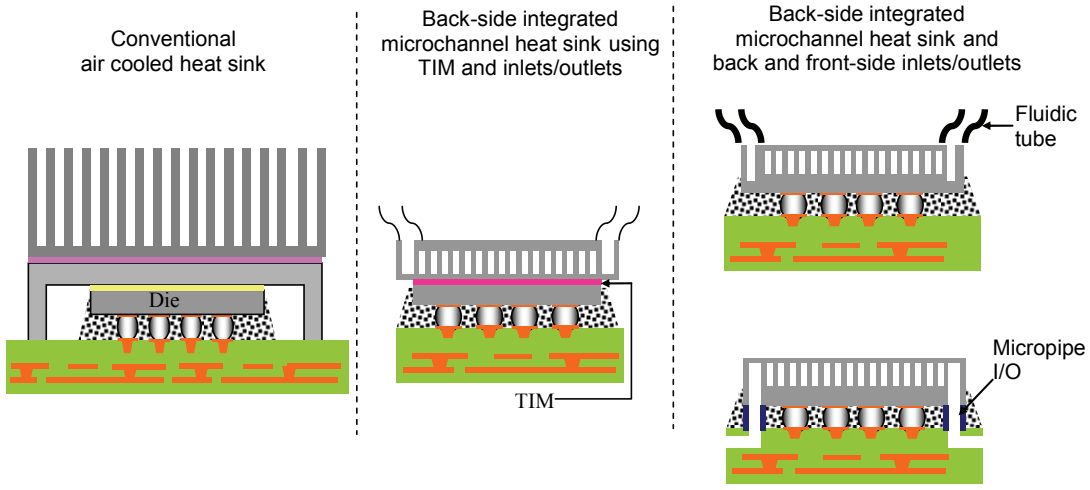


Figure AP16 Examples of Heat Sink Technologies and Integration of Fluidic Interconnections with CMOS Chips

3D silicon stacked modules will require integrated liquid cooling solutions and are in development today. For example, the consortium IME is developing an integrated cooling subsystem able to cool 3D modules with heat dissipation of 100

W for each layer (total 200 W for two-layer modules). (See Appendix A for a listing of more research consortia efforts.) The cooling solution includes carriers that act as substrate having electrical interconnects and fluidic micro-channels. The development of leak-proof carrier is one of the challenges in this project. Currently, the research team has developed processes for the fabrication of carriers, including micro-channels, through silicon via (TSV) and electrical routings. These carriers can deliver a flow rate of 340 mL / minute to meet the requirements of 3D packaging of high power devices.

THE NEED FOR CO-DESIGN TOOLS

Chip-package-system co-design methodology is a vital enabler for integrating SoCs efficiently into System-in-Package. Chip-package-board design collaboration is essential to reduce cycle time and cost and to optimize performance for stacked die, PoP, PiP, and 3D packaging in general. A more detailed overview is available in the paper titled *"The Next Step in Assembly and Packaging: Systems Level Integration."*

Failure to identify and meet essential system-level requirements and to apply lessons-learned, will result in lower-than-expected performance. Understanding design trade-offs and the performing critical system-level analysis is essential to produce designs that can meet the desired cost and performance targets. Incomplete feasibility studies and failure to capture some key interaction at the system level can result in extra iterations before the package design is finalized. It is important to identify essential system-level requirements and to apply lessons-learned for good optimal design. Without the benefit of co-design and simulation, there is risk that a device will be late to market with an expensive, overly conservative package.

Implementing co-design methodology requires iterative design reviews; collaboration between chip and package design; application development; electrical, thermal, and mechanical modeling; simulation, and high-density substrate design teams. Some key challenges in 3D packaging are design for manufacturability, design for low cost, reducing iteration time, design for reliability, complex wire bond and/or flip chip rules checking, chip design flexibility trade-offs. Also critical are interface/alignment with tools and flows such as those provided by EDA design software tools, IDM specific design flow and tools, and alignment with substrate suppliers and assembly sites.

COLLABORATION, COST AND TIME TO MARKET

Expert users of each tool environment chip/package/board must collaborate to optimize the design. Thus, for the future, appropriate user interfaces are required. Co-design can improve performance while reducing costs and cycle time dramatically—often by 2×. Without the benefit of extraordinary collaboration within the design team, the package is almost impossible to optimize at the system level. The cost trade-offs are not clear, system level performance impacts are uncertain, and changes are cumbersome to implement. To avoid this, designers often use overly conservative design margins and assumptions that lead to higher package costs. Without co-design analysis tools that function across design environments, "what-if" analyses are difficult and time-consuming, leading to longer design cycle times.

IMPORTANCE OF RELIABILITY FOR SIP

Effective co-design should comprehend the interaction between physical, thermal, mechanical, electrical design, and reliability. Many of the trade-offs between design areas and reliability that are evident in conventional packaging become more complex for SiP configurations. Thus, it is not good practice, especially in SiPs, to run the electrical, mechanical, and thermal and reliability design portions separately. Because of the complexity of sub-component interactions, there is not a universal or specific list of parameters to design for reliability. In general, one needs to examine the sub-component interactions, design goals, trade-offs, design rules, specifications, and existing design for reliability practices in order to select the appropriate design for reliability guidelines.

NEED FOR A SYSTEMATIC APPROACH

Package design requirements and changes originate from many different functional areas and usually end up being applied in stages. A potential solution would be for the chip-package co-design to borrow methods and tools from modern systems design. This approach can head off constant iteration and other challenges. One way to reduce iterations is to use "look-ahead" test and modeling vehicles to support system-level reliability and manufacturability testing, as well as system-level electrical and thermal modeling. Look-ahead vehicles come in two forms: an actual mechanical vehicle for reliability and manufacturability testing, and a paper design vehicle for feasibility, thermal and electrical modeling analysis. These vehicles require a certain discipline and commitment. This approach could help to answer many general design questions early in the process, and at a fraction of the cost of using production test vehicles.

NEED FOR CO-DESIGN TOOL DEVELOPMENT

SoC and SiP package design requires 3D capable thermal, electrical, and mechanical modeling tools that allow integration and analysis of chip, package and system level requirements, and interactions. We also need electronic design automation (EDA) tools for powerful chip-package-system design and routing capability, built-in checks, standards and reporting features like design rule checks (DRC), standard net list syntax, and connectivity reports.

Custom automation tools can provide fast and efficient communication and verification of design data between different design environments. Spreadsheets are a common platform for these automation tools since they are available in almost all design environments and readily scale to handle large volumes of data. These tools have three primary uses: 1) convert data to pictures, 2) convert data to standard formats, and 3) compare the standard format datasets. This type of automation is essential on typical SoC designs to reduce the time spent manipulating relatively large datasets, and to reduce possible manual errors in handling large amounts of raw data.

The development of chip-package co-design methods and tools is an ongoing process. A comprehensive, user-friendly, and tightly integrated tool(s) that can seamlessly span all the different design environments is not yet available. Nevertheless, existing chip-package co-design tools, with the right methodology and custom-developed internal tools can provide useful benefits including reduced package costs, and design and verification cycle time.

GENERIC CHIP-PACKAGE-SYSTEM CO-DESIGN TOOL DEVELOPMENT REQUIREMENTS

- Improve design cycle time, accuracy and design-for-manufacturability
- Align with critical tools, flows and rules such as: IDM's internal tools die design tools, suppliers, assembly sites, electrical constraints and modeling tools
- Reduce iterations, less manual/more automated checking, capture complex design rules and enable more chip-package-PCB trade-off capabilities
- Forward-looking: better methods, more complexity, collaboration, and technology combinations
- Easier verification: Substrate, substrate plus die, manufacturability, electrical, functional, thermal, and mechanical verification. Import/export to IDMs internal tools
- Easier and more rapid feasibility analysis
- Collaboration with die and system design teams. Good data formats, chip plus package plus system verification tools, etc.
- Comprehend the interaction and I/O planning of multiple functions within a single package (also passives)
- Great complexity—amount of design data, multiple layers, elaborate patterns, multiple net lists
- Complicated electrical constraints (long traces/wires, crossing traces/wires…). Enhanced constrain management
- Allow minor tweaks in IC or package design without leading to significant cycle time hit
- Need faster design iterations in early phase to avoid more costly design iterations in the later phase
- Capture complex mechanical, wire bond and flip chip bond assembly-rule constraints driven by smaller and thinner packages
- Better design for manufacturability and cost analysis. More and easier to use manufacturability constraints
- Real-time chip-package-system design trade-offs
- Interface and alignment with internal tools and flows
- Shortening design cycle of complex designs
- Cost-weighting of constraints
- More flexibility to handle frequent design changes
- Tighter integration with chip, system and manufacturability design teams
- System-level electrical modeling, including high-speed applications
- Complexity drives verification tools that work across different design environments
- Tight collaboration with suppliers, support, development, production, and customers to enable better methods and tools for complex package co-design
- More powerful user-friendly scripting capabilities
- Common, technology independent database to enable reuse

CO-SIMULATION OF RF, ANALOG/MIXED SIGNAL, DSP, EM, AND DIGITAL

SiPs that combine RF, analog/mixed signal, DSP, EM, and digital bring not only design and manufacturing challenges but also simulation challenges. Usually different functions of an IC require a different simulation technology. For instance,

frequency domain simulations such as Harmonic Balance are adequate simulation technologies for RF circuit designs; whereas time domain simulations are typically used to predict nonlinearity and VHDL or C based system simulation for digital applications. It is important to understand the system's behavior with packages and interconnect parasitics. Simulation and Modeling of Embedded Passives and Integrated Passive Devices in SiP applications need to be considered. Embedded passives are used to replace traditional surface mount parts.

WIRE AND DIE BONDING FOR SIP

A number of approaches have been develop for attaching die mechanically to the SiP package substrate and making electrical contact between the die and substrate electrical traces. Figure AP17 shows the wire bonding technology for SiP.

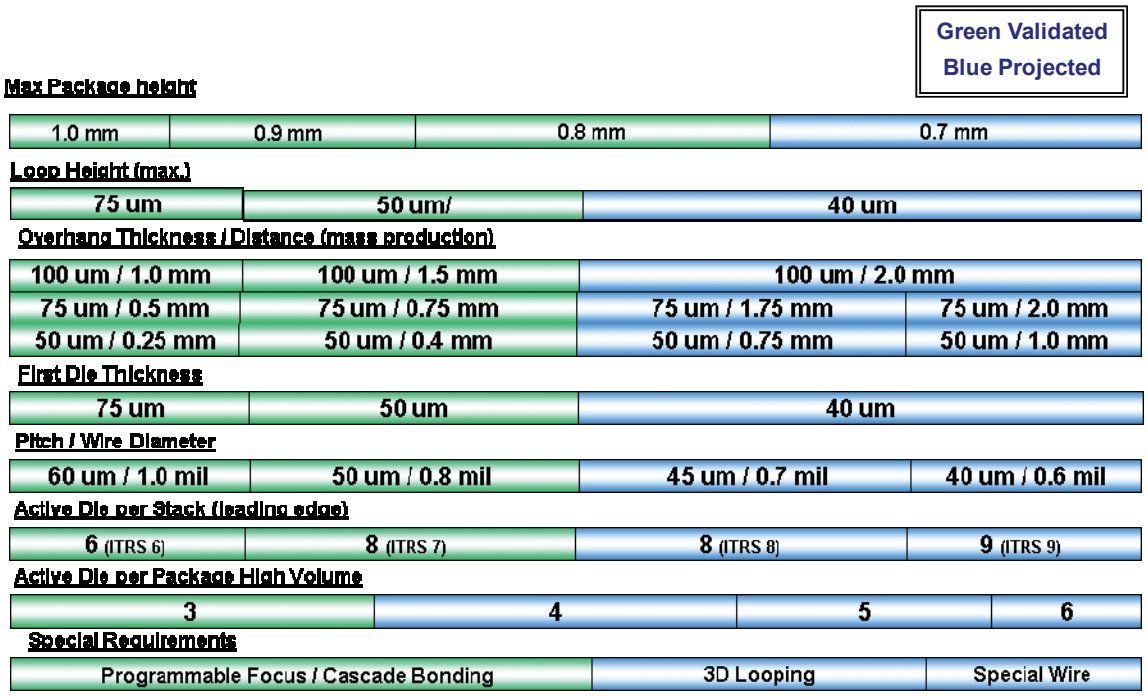


Figure AP17 Wire Bonding for SiP Packaging

DIE BONDING

Picking thin die is a new technology that is required for stacked die. Methods are being developed. To stay within standard package heights, the stacked chips need to be thinned. The backgrinding process is used to reduce the die thickness to the range of 50–125 µm. As a result, wafer handling needs special attention. A gentle and controlled die pick-up procedure is needed. These designs often involve sequenced needles or telescoping mechanisms.

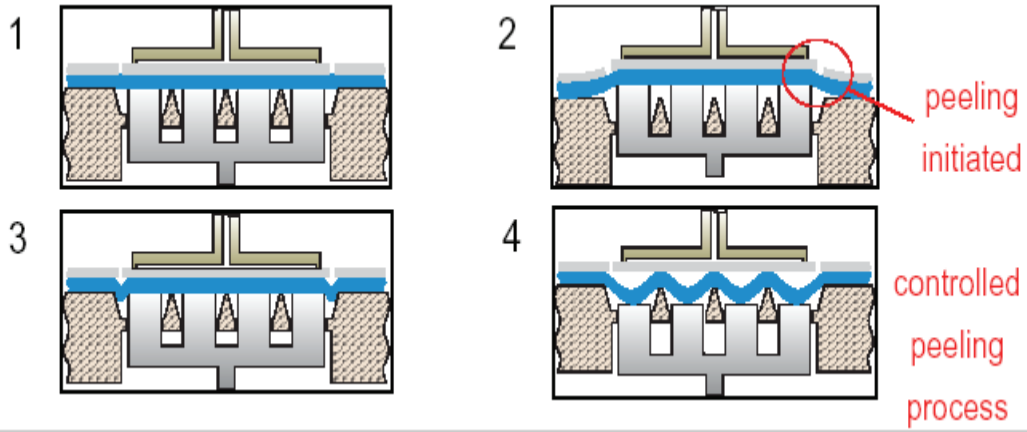


Figure AP18 Mechanism and Technique for Picking Thin Die

Another new technology under development for same size stacked die is called “film over wire” or “chip over wire.” This technology is already used in mass production by some companies. In this technology film is attached to the bottom of the wafer. In the die bonding process a heated collet picks up the die and places it directly over a previously wire bonded die. The heated film becomes the consistency of oil and if proper force is applied the liquid film will encapsulate the wires. The die must be held in place for 3 to 5 seconds for curing. In order for this process to work the wire bonding temperature must be lower than normal less than 120 or 100°C.

Figure AP19 Film over Wire Technology

There are many innovative approaches using wire bonding that are extending the life of this technology. The example given below in Figure AP20 of bonding on both sides of die illustrates the ability to build complex interconnect structures using the 3D routing for SiP implementations that is available with wire bonds.

Note:
This device is bonded in four passes..

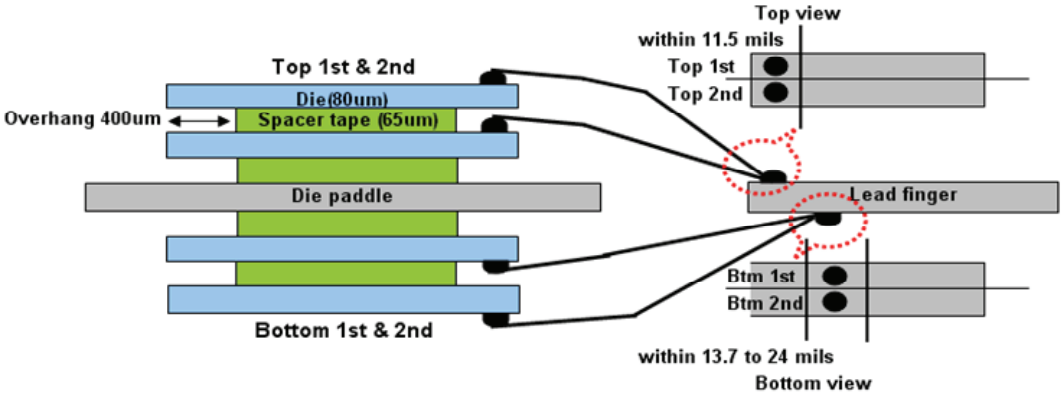


Figure AP20 Wire Bonding on Both Sides

TESTING OF SiP

There are three major issues with SiP test—known good die, system-level test, and test cost. Each are described in this section.

KNOWN GOOD DIE

A known good die (KGD) may be defined from practicality point of view as a die good enough for SiP integration. It must be functionally good before assembly and reliable as well. To satisfy the first condition of goodness, the circuit probe (CP or wafer sort) yield criterion should be upgraded to its final test level. The challenges to be met are:

- The ability to probe wafers at full speed. There are technical challenges associated with 15GHz and above (see the Test chapter of this Roadmap). An alternative is to embed a comprehensive set of built in self test (BIST) circuitry so that high frequency core transistors can be tested by core transistors of the same speed. A combination of both may be needed to test both high speed core transistors and off chip drive transistors at the frequency required in their use case.
- Known reliability before assembly which will require a wafer-level burn-in methodology equivalent to its packaged burn-in test.

SYSTEM LEVEL TEST

Final test solutions for SiP must provide similar test to those of conventional packages. This will pose a number of challenges not encountered with conventional single chip packages:

- Custom socket designs for non-standard or high-pin count SiPs
- Failure analysis for a 3D sip with TSVs
- Probe access to the internally sandwiched die particularly in the case of failure of an SiP component in final test
- DFT development (BIST and other techniques) for 3D-TSV SiPs

COST OF TEST

These test challenges must be met with low cost. Most SiP are today are used in consumer electronics. These markets are very price sensitive and any SiP for the consumer market with excessive test cost will not be successful. The major elements of conventional test cost are applications programming, test time, cost of ATE equipment, and cost of probe cards. Complex SiPs may require both conventional test and BIST testing to accomplish adequate testing. This is due to test access limitations in high component density, the very high speed of RF and digital communications circuits, and the requirement to test system level characteristics.

PACKAGING FOR SPECIALIZED FUNCTIONS

OPTOELECTRONIC PACKAGING

UNIQUE REQUIREMENTS FOR OPTICAL ELECTRONIC CHIP PACKAGING

There are three major unique requirements for packaging optical elements. They are minimal light loss, high precision alignment, and thermal management.

1. Minimize light loss. This requires:
    a. Clever, robust designs to maximize output
    b. Minimal absorption by optical and/or semiconductor elements
    c. Minimizing refractive index interface difference losses and undesired scattering
    d. Achieving and maintaining good coupling to optical sources and detectors
2. Sub micron alignment and stability in operation of the optical chain, especially of single mode fiber coupled to edge emitting laser die
3. Dissipate heat from high power laser die and high brightness LEDs to minimize temperature changes, maximize performance and minimize wavelength drift

HIGH BANDWIDTH OPTICAL INPUT AND OUTPUT FOR CHIPS

A key bottleneck to the realization of high-performance microelectronic systems is the lack of low-latency, high-bandwidth, and high density off-chip interconnects. Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include the high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to crosstalk.

As a result, the motivation for the use of microphotonics technology to overcome these challenges and leverage low-latency and high-bandwidth chip-to-chip communication has been presented in the literature (for example, [8, 9]).

Significant progress has been made in developing chip-to-chip optical interconnects [10, 11, 12], which include fiber-to-the-chip schemes (in one example, an optical signal is coupled to a silicon-based taper), have been reported. Free-space optical interconnects are also being pursued for chip-to-chip communication. Susceptibility to misalignment and complexity in packaging are challenges yet to be fully addressed for these optical interconnection technologies.

Guided-wave interconnects using polymer waveguides, which are batch fabricated on the substrate, are being pursued as yet another alternative to enable optical interconnection. Polymer-based waveguides offer some advantages that include high density, optical confinement, and ease of fabrication.

In one approach, the optical devices, such as detectors (PDs) and sources, are integrated within the package substrate and are interconnected using the polymer waveguides. If the optical devices are integrated on the Si through either monolithic or heterogeneous integration, the polymer optical waveguides route the optical on the substrate to a point directly beneath the chip where the optical sources and photodetectors (PD) are located.

A coupler, such as a mirror, is used to couple the light vertically from the substrate to the chip, and vice-versa. Depending on I/O power budget and bandwidth, such a free-space optical I/O places constraints on the tolerated vertical and horizontal offsets between the optical devices on the chip and the substrate. The use of lenses to alleviate some of these tolerances have been demonstrated but at the expense of fabrication complexity and density. Lateral alignment deviations may be caused either during assembly or thermal cycling, which is important due to the coefficient of thermal expansion (CTE) mismatch between the chip and substrate. Such misalignments could severely reduce the optical power delivered to the PD thereby increasing the bit error rate (BER) and reducing bandwidth. Moreover, such free-space optical I/O schemes have not been shown to be compatible with underfill processes. The use of vertical optical waveguides, or polymer pins (or pillars), between the chip and the substrate has also been proposed. Some of the optical interconnection technologies are illustrated in Figure AP21.

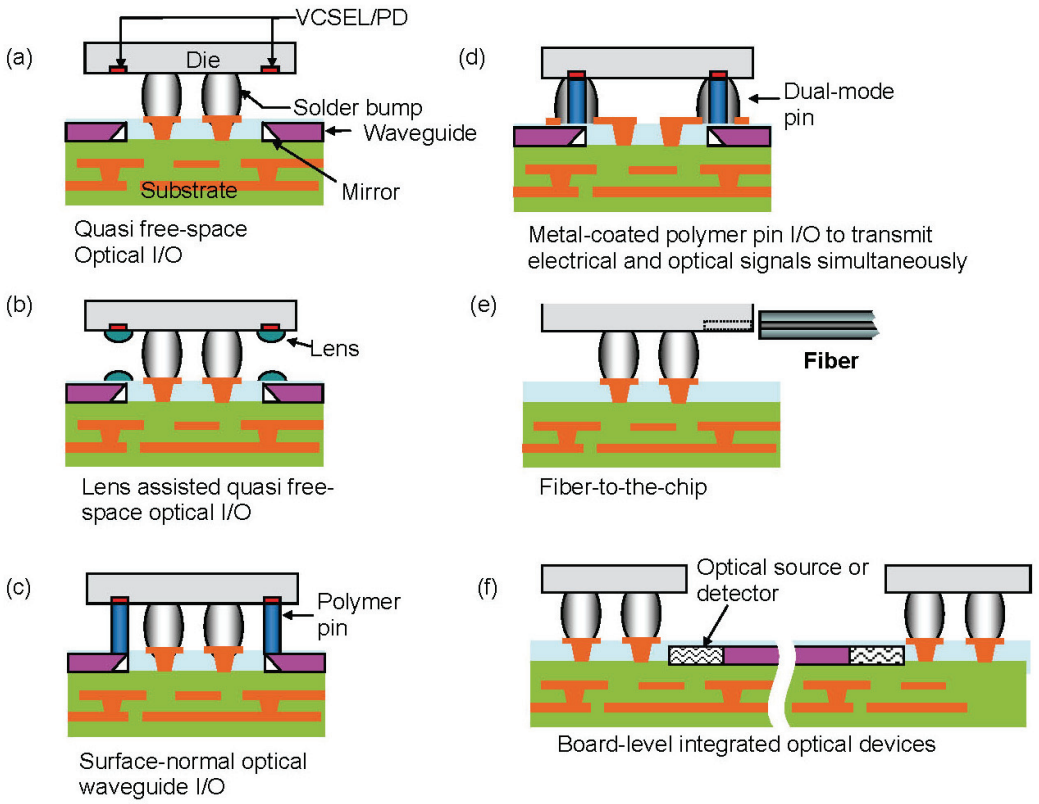
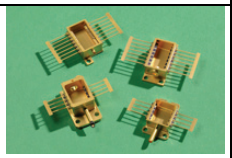
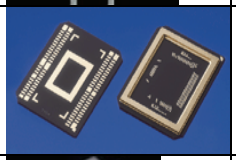


Figure AP21 Examples of Representative Guided Wave Optical Interconnects

COMMON OPTOELECTRONIC PACKAGES

Optical semiconductor devices are packaged in a broad variety of configurations, both standard and custom. Some of these packages and their characteristics are shown and listed in Table AP14.

Table AP14 Some Common Optoelectronic Packages and Their Applications

Package Type	*Example*	*Applications*	*Package Characteristics*	*Comments*
Butterfly Packages		Telecommunications and data transceivers and laser sources	Metal ceramic hermetic SMT package Rigid; sub-micron stable	Contains edge emitting laser, TCE cooler, monitor, lens, etc.
TO Can with Molded in Connector		Optical source or detector die	Sizes TO-05, -18, -46, etc.	Built in optical chain.
TO Can with Window/Lens		Optical source or detector die	Hermetic, Sizes TO-05 and TO-18	Welded cap with optical chain.
Ceramic Package with Interconnect and Heat Sink		LED packages, especially for high power LEDs Used for light engines, backlights, etc.	High thermal conductivity, Reflective cavity/s, usually optical clear encapsulants	Single and multiple die, sometimes of different colors. Up to ~ 100 cavities with hundreds of die
Overmolded Die on Lead Frame		Single LED or detector die	Non-hermetic, few leads	Very low cost. Made in high volume.
Ceramic Package with Glass Cover		MEMS devices with movable elements, like mirrors	Multiple leads, highly hermetic. Devices highly ESD sensitive.	Variety of sizes. Used in DLPs.
Surface Mount Package		LED indicators	SMT sizes; 0804, 0603, etc.	Low power, low cost, multiple colors.
Wafer Scale Optical Packages		Camera modules	Small. Built on wafers in arrays.	Low cost. Saw singulation

STATUS AND PACKAGING OF OPTICAL TRANSCEIVERS

Data Rates—Interconnect challenges are across the board at all data rates from 622Mb/sec to 100 Gb/sec and beyond. At the low data rates the packaging size has been reduced driving more automation into the assembly process, concurrently with new environmental and mechanical demands for outside plant (OSP) applications. Carriers are pushing new developments and tougher environmental standards onto pluggable optical devices for use in FTTX applications (fiber to the "X," X is for P – premise, H – home, etc). Higher data rates with greater densities have spurred the development of low loss optical waveguides and new interconnect technologies including the free-space optics with less reliance on physical interconnects within the design.

Distances—Primary drivers on the reach of the devices is cost and bandwidth (greater data rates for lower costs at each distance.) Key reaches are Very short reach (VSR), less than 300 meters, and LR(SONET)/ER(GE), 40 km or greater. Data in Table AP15 shows variation in descriptions and distances for some of the common protocols (SONET and GigE). Similar variations in descriptions and distance are present in fiber channel and copper applications.

Table AP15 Protocol with Distance

Protocol	*VSR*	*SR*	*SX*	*IR1 1310nm*	*IR2 1550nm*	*LR1 1310nm*	*LR2 1550nm*	*LX*	*ER*	*ZX*	*ZR*
Sonet/ SDH	**<2km**	**10km**		**20km**	**20km**	**40km**	**80km**		**X**		**X**
GigE	**300m**	**2km**	**500m**		**10km**	**20km**	**X**	**10km**	**40km**	**80km**	**80km**

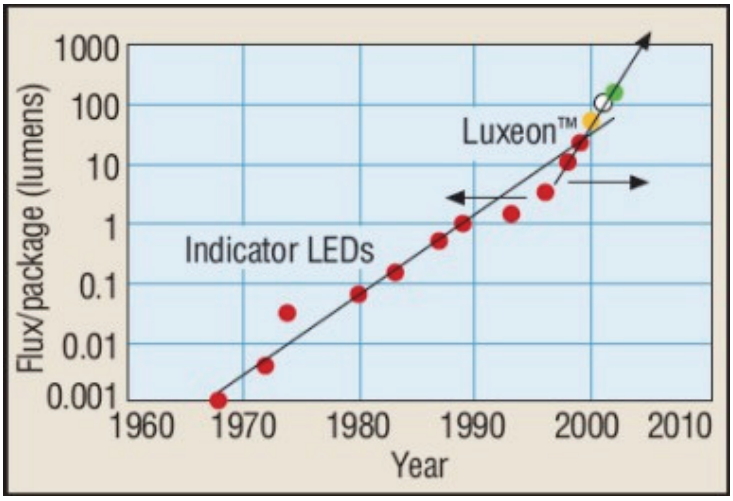
Packaging Methods for Optical Transceivers—Module and discrete packages are the primary types, with module style dominating the market. Discrete packages are reserved for the newer technology at initial deployment, and for legacy production from early parts of this decade. Electronics and optical subassemblies are all automated, with final assembly being manual for most designs.

PACKAGING HIGH BRIGHTNESS LED DIE

High brightness LEDs offer important technical advantages;

- High efficiency converting electricity to light (>25% and growing. See "Haitz's Law" below in Figure AP22.)
- fast response (<1 microsecond)
- Physically small (500 micron square die)
- Long life (>10,000 hrs.)
- Other advantages specific to an application.

The disadvantages are primarily economic; today, high brightness LEDs are initially more expensive than conventional sources such as incandescent and fluorescent bulbs. In some cases, however, LEDs save money over the lifetime of the products compared. The challenge is to continue reducing the total installed cost and, specific to this discussion, the cost of packaging the LEDs. Figure AP22 shows the technology improving the light output (lumens) from LEDs. In addition, the efficiency of converting power to light also continues to improve and is approaching that of fluorescent sources.



LED flux per package has doubled every 18–24 months for the last 30 years

Figure AP22 Haitz's Law for LED flux.[1]*.*[2]

[1] *Lumileds*

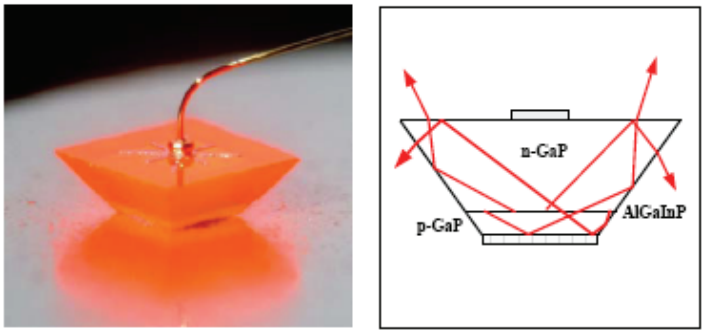
[2] *Paul Greenland and Werner Berns. "Powering Next-Generation Solid-State Lighting." National Semiconductor Corp. in Power Electronics. May 1, 2004.*

LED die are made from III-V semiconductor materials that are brittle and expensive. Thus die are small (down to 250 microns square with a comparable height), fragile and environmentally sensitive.

LED packaging requires the device/package structure to allow the maximum amount of light to exit in the pattern desired. The light extraction efficiency from small die is greater than from large die because limited light is able to escape from the sides of large die. Light extraction is improved in flip chip designs because no light is attenuated by semi-transparent metal electrodes, absorption of light is dramatically reduced through the use of highly reflective metallization schemes, and no light is obscured by bond pads or wires.

Some products require multiple die, often of different colors. Different colors mean different semiconductor compounds which means different die. Thus, the assembly process must accommodate the resulting different die size, both wire bonding and flip-chip attach and sometimes different orientations. Equipment to "pick" these small, high aspect ratio die from many different wafers and place these die on a substrate within 25 microns of the desired location at high speed (>1 die/second) is available only on a custom basis.

Assembly is complicated by the shape of some LED die. For example, optical efficiency can be improved by shaping the die as an inverted pyramid as shown in Figure AP23. This geometry minimizes light absorption in the package. This unusual die shape, however, requires specific assembly processes and equipment.



Graphic courtesy of Lumileds. Reference for credit is in footnote.[3]

Figure AP23 AlGaInP/GaP Truncated Inverted Pyramid

LED die are sometimes only 250 µm square and may have high power dissipation per unit area. Thus, high thermally conductive substrates and materials are often required in the package.

LED die are sometimes encapsulated with an organic optical material to protect them from the environment, or, frequently, to adjust the emitted spectrum. . White sources are often made using a blue emitting LED that excites a white emitting phosphor added to the transparent encapsulation material.

Total cost is complicated by the need for power conditioning and control circuitry. LEDs do not run on 110VAC; high brightness LED die require 3.5 to 4.0 volts at 0.25 to 0.5 amps. Color and brightness are often controlled with pulse width modulation. Thus, packaging these electronics with the LED die offers the potential for cost reduction.

OPTICALLY BASED SENSOR PACKAGING

Many of these devices utilize optical electronics as sensors of the presence of, or changes in, some parameter. These sensors usually have a light source/s often LED/s, an optical chain of some sort that enables the light to interact with the environment or sample, a detector or detectors, and signal processing electronics to determine the level of some parameter, whether or not a specific compound is present or if an event has occurred. These challenges and potential solutions are listed in Table AP16.

[3] *http://www.lumileds.com/pdfs/TP41_IESNA_Buffalo_6-04.pdf. Link to a Lumileds presentation covering a broad range of High Brightness LED topics.*

Table AP16 Optoelectronic Packaging Challenges and Potential Solutions

Challenges	*Potential Solutions*
Optical Transceivers	
New technology at high data rates is mostly discrete assembly	Greater integration at subassembly with automation
Higher densities in applications	Further reduction in size by increasing densities of optical signal by use of new interconnect technology. Use of more free space interconnects.
Increased mechanical and environmental stresses for FTTX applications	Lower reliance on direct contact lens applications, increased development in mirror and bandsplitter technology
Chip level interconnects	Material selection, development of low loss waveguides, use of free-space optics
High Brightness LEDs	
Raise the electrical to optical conversion efficiency	Improve the semiconductor materials, packaging materials and package design
Dissipate the heat	Improve the package materials and design
Reduce the cost	Improve assembly processes and equipment. Configure factories to produce these products
Optically Based Sensors	
Find needs and create economically viable solutions.	Develop a broad understand of the optical technologies, the components available and the economics of the application.
Methods to build stable optical chains	Materials that do not change from exposure to water, UV, heat, aging, or the chemistry of the application environment.
Develop standards for the optical components	Industry collaboration

RF AND MILLIMETER WAVE PACKAGING

Mobile phones are the driver for RF packaging up to a frequency of 5 GHz. Today mobile phones include more and more frequency bands for the various standards like GSM, GPRS, EDGE, UMTS or the new HSDPA (High Speed Downlink Package Access) standard. In addition mobile phones include more and more functionalities like GPS, WLAN, WiFi or Bluetooth, which are related to RF. Typically the RF part of a mobile phone consists of an RF front-end, a transceiver and a power amplifier (+ power management) chip including passive components like SAW and BAW filters or RF MEMS. General trend is higher system integration. Today already SoC solutions for RF parts which include GSM, GPRS, EDGE, and HSDPA exist.

Today for transceiver with less I/Os (often single band transceiver) VQFN type packages, which are comparable cheap, are typically used today. But also due to improved front-end chip design VQFN type packages appear for multi-band applications, because less I/O are achieved. LFBGA type packages are typically used for more complex transceiver, which include multi-bands. Transceivers are also set-up for higher integration as System-in-Package, including e.g. SAW filters or even baseband parts. In today's new mobile phones one can also find transceiver with WLP type devices, which offer the advantages of low cost, miniaturisation and RF performance, but have less integration capability.

Power amplifiers are especially designed as modules. Some solutions also integrate the power amplifier with the front-end antenna switches in the module.

The main interconnect technology used for RF parts is wire bonding and it is expected that this technology will still be important for the future up to 5 GHz. Flip chip is used for some more complex SiP set-ups. A clear trend for transceiver is increasing integration of passives. Here passives integrated in Si substrates offer interesting solutions.

A challenge for the RF part is the ongoing increase of complexity. Thus, for the future new package approaches are required. A promising new solution could be a thin film technology which allows reduction of complexity by appropriate rerouting. Embedded wafer level ball grid array solutions based on reconfigured wafers and thin film technologies are a promising example for future complex RF devices in various frequency ranges. They allow integration of passive components and open interesting possibilities for combining baseband and RF parts. For the future with increasing Si technology performance also software radio based architectures are discussed which require appropriate package solutions.

RF CMOS and CMOS based technologies like SiGe or CMOS on SOI substrates meanwhile are investigated up to 100 GHz region and even beyond. Regions for investigations are automotive radar in the 24 and 77–81 GHz region. For these high frequencies packaging is extremely difficult: The most important challenges are as follows:

- Material constraints (high frequency data for many of the new materials are not available)
- Heat dissipation (~ 3w/mm^2 needs to be removed)
- Shielding
- Transmission lines (coplanar or micro strip lines)
- Crosstalk

These high frequencies packaging technologies involving thin film are highly attractive because of their capability for transmission line design. At frequency beyond 40 GHz integration of antennas to the package becomes very attractive. An integrated SiP based solution has the advantage that the internal transmission lines need not be adjusted to 50 Ohm, which allows performance improvement.

MEDICAL AND BIO CHIP PACKAGING

The requirements of medical electronics are often best met with SiP solutions. This is particularly true for implantable and wearable devices such as biosensors, hearing aids, pacemakers, implantable cardioverter defibrillators and similar products. Additional implantable electronic and electromechanical systems are being developed and qualified at a rapid pace. The emerging applications range from drug delivery through integration of biomaterials with integrated circuits for neurostimulation. Future products will incorporate telemetry for real time data monitoring which incorporate RF circuitry and antenna structures that are biocompatible. The requirements for SiP based medical products are similar to those of SiP based products for other applications with two important exceptions. First the reliability required for medical SiP based products is at the highest possible level since a failure may be fatal for the user. Second the environmental requirements of the package have to include exposure to body fluids. There are several areas where additional development is needed for medical SiP. Among those are:

- Low power, biocompatible radios with a signal that can reliably penetrate the human body and package to reach a remote receiver. This receiver is most likely worn by the user.
- Reduced power consumption through improved interconnect
- Power scavenging from the user's body temperature (up to 30 micro Watts/cm2) or motion (up to 10 micro Watts/cm2) to extend battery life of implantable products. This will require research and development of biocompatible MEMS SiP components
- Biological and silicon integration such as neurons grown on silicon. This allows silicon to monitor brain waves to detect seizures and provide counteracting neurostimulus.
- Reliable interoperability of wireless telemetry for medical devices in a world where RF devices operating across a number of frequencies have become ubiquitous.

One common method used in biomedical devices is to illuminate a sample with a suitable light source, then look for the presence, absence, or difference in intensity between two or more wavelengths with photo detectors that may require narrow band optical filters.

Many of the biomedical devices incorporating this sensor concept are disposable products made to detect pregnancy, glucose levels, blood oxygen levels, CO or NOx levels in the air, etc. Thus, they must be rugged, small, required minimal amounts of power to operate on batteries and be manufactured for low cost.

The packaging issues with these products are:

- Mechanical design, especially of the optical elements, to
- ensure optical alignment is achieved initially
- ensure alignment is retained for the life of the product
- protect the optical chain integrity over the lifetime of the device
- Materials selection, especially adhesives
- Protection of the optical system and related electronics from external light and EMI effects
- Protection of the device from the environment including from fluids that are samples either to be evaluated or used in the detection process.
- Selection of the processes and assembly methods for the optical alignment.

MEMS DEVICE PACKAGING

MEMs devices are packaged in an unusually wide variety of ways due to the great variation in requirements. These requirements, and the resulting package solutions, go well beyond those of microelectronic packaging and result in an unusual variety of packages. Examples include MEMs packages for the following:

- Devices, such as transmit/receive switches, must exclude moisture to prevent deterioration or corrosion and might require an inert atmosphere to remain stable
- Pressure sensors must be open to atmospheric pressure but not be susceptible to moisture damage
- Optical devices, such as camera modules, must exclude particles, must not have organics that can condense on optical surfaces over time, require optical windows and must maintain optical chain alignment over the product life.
- Devices requiring controlled atmosphere; vacuum, inert gas, etc.
- Devices that analyze fluids require containment of those liquids and must not leak
- Devices requiring ESD protection greater than that required by CMOS devices

Even though the term MEMS means “micro electro mechanical system”, many devices that are considered to be MEMS devices have no moving mechanical parts.

The first choice for a MEMS device package is a standard, off the shelf microelectronic package. Unfortunately, those packages are often inadequate for specific MEMS applications, so engineers must modify the design or design a unique package for manufacturing.

MEMS devices are sometimes designed to use wafer level packaging. Some wafer level methods use overmolding; some use wafer to wafer bonding; some build a cavity within the MEMS structure and seal it at the device fabrication level. The selection and design of a MEMS package can be a major portion of the effort needed to bring a MEMS product to market.

One key emerging technology used to reduce cost and improve performance of MEMS devices is the integration of MEMS devices with standard semiconductor devices which provide drive, control, and signal processing functions. This approach enables increased integration and reduction in cost. This may be enabled for many MEMS device types through a low cost wafer level package which can provide cavities. Technologies which enable the decoupling of package stress through the bump or die attach to the MEMS structure are also a critical challenge for MEMS in wafer level packages.

The two following tables provide a broad overview of the MEMS packaging methods and some specific examples.[4]

Table AP17 MEMS Packaging Methods

Type of Package	Applications	Characteristics
Plastic Overmolded, Leaded and Leadless	Resonators, accelerators, inertial sensors	Low cost
Premolded Plastic Air Cavity, Leaded and Leadless	Pressure sensors, accelerators, microphones	Low cost cavity package
Ceramic With Metal Lid or Metal Cap	Lab on a chip, optical devices, RF switches	Highly stable, costly, complex to engineer and fabricate. Control of cavity environment; dry, vacuum, inert gas, etc.
Ceramic with Glass Cover	Optical applications; CCD packages, DLP	Stable, moderate cost, optical window.
TO-5 with Hole or Window	Pressure sensors, some optical devices	Low cost, widely available
Glass on Glass	Optical applications; displays	Large cavity packages, sometimes with standoffs
MEMS on Organic Substrate with Glass Cover	Optical switches, displays	Quick to market, low cost.
MEMS on Substrate organic, Ceramic, etc. Wire Bond, Partial or Total Encapsulation	Inkjet print heads, fingerprint readers	
Wafer Level (structure built, then singulated)	Camera modules	Lowest cost in volume.

Table AP18 MEMS Packaging Examples

Market	Automotive	Consumer	2D Optical Switch	3D Optical Switch	Network Switch	Wireless
Application	Acceleration, airbag sensor	Video games, appliances	OADM, enable	WAN, LAN Networks	Electronic Switches	Saw Filters
MEMS Type	2 axis accelerometer	3 axis accelerometer	64 Mirrors, 90° motion	1800 Full motion mirrors	Contact switch	Planar filter
Package Size	TO8, 14 ld CerDip	Surface mount CLCC	Custom metal, 82 mm^2	Custom Ceramic, 184 mm^2	LTCC, 27mm^2	PWB, 40mm^2
Clean Room	100, 10000	100, 10000	100, 10000	100, 10000	100	10000
Die Bond	Epoxy	Epoxy	AuSn Eutectic	Epoxy	AgSEutectic	Epoxy
Wire Bond	0.7 – 1.0 Au ball	0.7 – 1.0 Au ball	1.25 Al, 1.25 Au, 6.0 m Al	1.25 Au Wedge/ball	1.0 – 1.25 Au ball	1.0 Au ball
Seal	Seam seal	Molded	Seam seal	Seam seal	Epoxy	Epoxy lid seal
Leak Test	Gross/fine	None	Gross/fine	Gross/fine	Gross/fine	None
Additional	-	-	Fiber optics, connectors	Flex circuit, connectors	PWB connectors	SMT connector
Manufacturing Level	Production	Production	Pre-production	Pre-production, R&D	Pre-production, Proto	Pre-production, Proto
Package	Ceramic, CERDIP, Hermetic	Plastic, ceramic, hermetic, CLCC	Custom-68 I/O	Custom – 800 I/O	LTCC Panel	PWB Panel

[4] *Based on Amkor data from a Gartner Presentation at the MEPTEC 2007 MEMS Symposium*

ELECTRONICS IN TEXTILES AND WEARABLE ELECTRONICS

WEARABLE ELECTRONICS

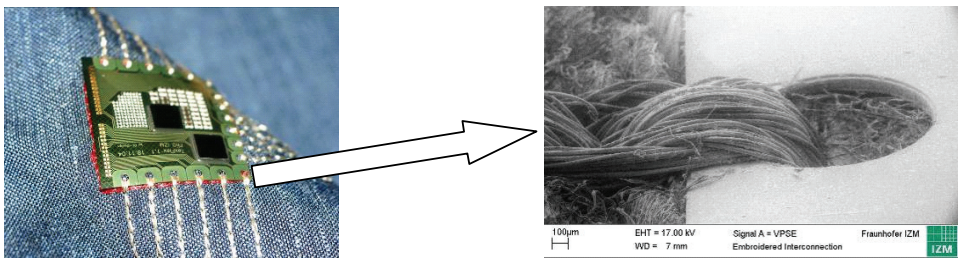
The integration of electronics into textiles requires four important issues to be solved:

- Interconnection of electronics with conductive textiles
- Encapsulation of electronics and interconnections
- Isolation of conductive textiles or the local removal of pre-isolated textile conductors
- Development of reliability tests for electronics in textiles in different applications
- High volume low cost manufacturing

The most popular interconnection approaches are soldering, adhesive bonding, crimping, and embroidering. Some R&D in this field is covered by research institutes, e.g., Fraunhofer IZM. Encapsulation technologies that are currently investigated for the use in electronics in textiles are transfer molding, hot-melt encapsulation, liquid encapsulation, and dam-and-fill and glob top encapsulation. The main challenge for the interconnection and the encapsulation are ensuring the reliability during textile typical treatment, be it for wearable electronics or for technical textiles applications.

A critical issue that has not been investigated much is how to isolate conductive textiles or alternatively how to locally remove the isolation of pre-isolated conductive textiles. Ideas include lamination or liquid coating. Materials in focus are polyurethane or silicone either in solvent or as two component material that cures. Even more challenging is the development of a smart coating that coats only metallic parts and leaves the non-conductive textiles unchanged.

Before manufacturers incorporate electronics in textiles developing wash tests, wear tests and other reliability tests for textile integrated electronics is essential. This is not simply summing up electronics test standards and textile test standards since they are not compatible. New reliability tests and test standards have to be developed based on the real stress on electronics in textiles. See Figure AP24.



Graphic courtesy of Fraunhofer IZM

Figure AP24 Texflex Embroidered Interconnects

Standard flex circuit assemblies only allow for bending deformation along one dimension, allowing for cylindrical and conical shapes. More complex surface shapes, such as spheres, cannot be realized. This requires stretching of circuit surface. Elastomeric polymers, such as silicones and polyurethanes, can be used to make the flexible substrate "stretchable." However, an electronic interconnect also requires electric interconnects that run on or inside this polymer matrix. The challenge is to realize stretchable electrically conductive interconnect lines on/in stretchable polymer materials.

Techniques used to achieve flexible conductors:

- The use of metal interconnects incorporating electrical conductors in spring shapes (e.g., horseshoe meandering lines). This typically results in longer interconnect lines with a lower interconnect density. Good results are shown for stretchable conductors in a single direction. More challenging designs are needed for stretchability in two perpendicular directions, as follows:

1. Use of conductive particles in the polymer matrix. This requires a high filling density, above the percolation limit for conductivity, which may fundamentally limit its stretchability. Conductivity will vary significantly with applied strain.
2. Use of conductive polymers to render part of the polymer body conductive. Obtaining a high conductivity is a key challenge.

Combinations of metal tracks and conductive polymers or embedded conductive particles: normally conductive metal tracks are used in parallel to the higher resistance conductive polymer solutions. Stretching of the conductors occurs mainly in localized parts of the polymer matrix. Most of the current is conducted through the parallel conductor straps.

FLEXIBLE ELECTRONICS

Flexible electronics is projected to grow into a multibillion-dollar industry over the next decade and will revolutionize our view of electronics. The unique properties of flexible electronics, such as its compliant structures, ultra-thin profiles, low weight, and potential low cost and high reliability could have enormous impact on consumer electronics, aviation and space electronics, life sciences, military applications and telecommunications. Flexible electronics will enable a broad range of devices and applications not possible today. Smart clothing with integrated electronics and displays will have many consumer, medical and military applications. Realizing the possibility of smart active bandages, and other medical devices such as reconfigurable systems and sensors, micro drug-delivery systems, active/integrated prostheses and massively parallel secure and fault free distributed environmental field sensors will have the potential to change the way people detect and deal with disease and pathogen exposure. Some examples are:

- Energy: large area, low cost photovoltaic devices; energy efficient lighting
- Military: soldier portable power products and rugged, lightweight imaging devices
- Medical: medical sensors, intelligent bandages and soft tissue implants
- Agriculture and civil infrastructure: large area sensor nets; food safety
- Transportation: hazard warnings; automated roadways; cargo container tracking

The application areas and products shown above will require significant infrastructure development in the areas of tooling, processes, and materials. Many of products identified will require large area flexible electronics, with feature scales ranging from meters to the sub micron on the same product. Tools and processes to build such products do not currently exist. There will also be a need to develop new substrate materials, new barrier materials, new coatings, and adhesives. For example medical applications that require implanting electronics will have to be constructed of materials that are non toxic, stable and that withstand specific harsh chemical environments. Avionic and space applications will require specific radiation hardening. Wearable textile electronics will require ability to withstand common laundry process.

AUTOMOTIVES ELECTRONICS

High performance automotive electronic systems are a prerequisite for the design of next generation automobiles. High precision management, reduction of wiring harness, and greater energy efficiency need more and more electronics. State of the art IC packaging will be used for electronic systems, which will become small in size and require low power loss, light weight, and multi-functionality. A close connection between automobile manufacturers, electronic manufacturers and semiconductor manufacturers is essential. The automobile will make a revolutionary change in developing new power sources, improving car intelligence and information services.

The worldwide car vehicle sales will have a growth of about 4% per year between 2000 and 2010. Compared to this the electronic system growth is expected to be over about 10% per year between 2000 and 2010. Major categories of automotive systems are: power train, chassis, safety, security, body, and drive information. Highest growth rate is expected in safety and drive information. Newly developed electronic systems are: Night view systems (supports, e.g., senior drivers), pre-crash safety systems, and hybrid vehicle systems (enable high efficient use of fuel). Advantage of the hybrid system is that acceleration performance and fuel efficiency can both be improved.

Today the cost of electronic parts in cars is 15% for compact cars, 28% for luxury cars and 47% for hybrid cars (source: M. Hattori., Toyota, Semicon Japan 2006). Reducing size for automotive electronic systems is crucially important. The installation space that can be equipped with electronic systems is limited. The numbers of automotive electronic systems will rapidly increase during the next few years and thus minimum volume of the electronic systems is required.

The most difficult issue is development of small sized electronic systems at reasonable costs. Both hardware and software will be important. BGA and CSP packages are seen to replace conventional QFP. Automotive electronic systems will push downsizing of electronic systems in the future. Automotive targets to catch the technologies used in cellular phones and digital consumer applications. A hybrid car supplier for example developed an optimized IGBT to control the 30 kilowatt motor.

In respect to reliability the car is divided into passenger room and engine room. In the passenger room LSI are required for maximum 85°C operation temperature. In the engine room there are three types of required operation temperatures: At special designed positions with cooling systems LSI are required for 105°C operation temperature. Near the engine cylinder block 125°C operation temperature is required. At the connected engine cylinder block 140°C is required. In respect to semiconductor technology under conditions the SOI device structure is very attractive for future use.

OPERATING ENVIRONMENT SPECIFICATIONS

Metric	*Specification*
Automotive Maximum Temperatures (Ambient Temperatures)	
Passenger Compartment Dashboard, panel Hatrack	 +85°C +120°C
Chassis Isolated areas Exposed to heat source	 +85°C +125°C
Transmission Exposed to heat source Exposed to oil/hydraulics (today always bare die on ceramic substrate)	 +125°C +175°C
Engine Compartment Moderate areas Attached to Engine (today always bare die on ceramic substrate)	 +125°C +155°C
Storage Range	-55°C to 125 °C
Operating Range	-40°C to 150°C
Typical Mission Profile	-40 to - 20°C / 300h -20 to + 20°C / 600h 20 to +130°C / 4000h 130 to +140°C / 1000h +150°C / 100h
Vibration	40g / 10–1000Hz (depending on customer)
Mechanical Shock	50g / 11ms (depending on customer)

Components in a future smart power technology (as single components) for engine control or chassis (exposed to heat source) will have an ambient temperature range from -40 to +125°C. These components will have embedded Flash, µC, and LDMOS. This means that the LDMOS circuits add a temperature of about 20–40°C and as well the silicon as the package has to cover a temperature (ambient + power dissipation) of -40°C up to 165°C. (This is very critical for controllers and flash memory such that the package heat dissipation must be extremely good). In addition packages and silicon for such applications have to withstand thermal hot spots of 350 to 400°C.

Another example concerning future applications will be automotive radar. In the future all components will be integrated in a SiP. This means an ambient temperature range of 105°C and in addition heat from power dissipation of 10 to 20 Watts.

SOLAR CELL PACKAGING

The rapid growth of the solar power has generated a need to address the unique packaging requirements for packaging solar cells and solar cell arrays. Solar cell modules face temperature extremes and must have a very long life compared to

almost any other packaging requirement. The current state of the art for the photovoltaic modules used in solar cell arrays is:

- Semiconductor thickness 180 µm
- Soldered with high-throughput tabber-stringer
- Vacuum lamination
- EVA as encapsulant
- Guaranteed lifetime of 25 years

The continued expansion of solar power and the changes anticipated in the solar cells will require focus on additional parameters to meet the packaging requirements. These new requirements include:

- Low-stress interconnection for very thin solar cells (between 100 and 150 µm thick)
- High throughput lamination technology
- Pb-free soldering solutions
- 30 years lifetime
- Design for easy recycling at end of life

ADVANCED PACKAGING ELEMENTS

EMBEDDED AND INTEGRATED ACTIVE AND PASSIVE DEVICES

Integrated passive devices (IPD) are subcomponents, which exclusively contain passive components. They contain all three types of passives (R, L, and C) as well as only two or one type or any combination. The elements can be connected to each other in order to realize certain network, matching or filter functions or stand for their own to realize only single resistive, inductive, or capacitive functions.

The introduction of new materials like thin oxides or filled polymers as dielectric extends the value range for capacitors to maximum values in the micro farad range. Besides standard redistribution wiring systems it is also possible to realize ground planes and transmission lines to create impedance controlled RF-signal transmission.

The use of wafer level thin film processes (polymer-metal-oxide) technology offers the possibility to manufacture application specific WL-IPDs with passives in the following value ranges:

- Resistors: 10 Ohm–150 kOhm (e.g., NiCr 100 Ohm/sq; TaN 25 Ohm/sq.)
- Inductors: 1 nH–80 nH (Q: 30–150)
- Capacitors: (3–6) pF/ mm² (er=2.65, e.g., polymer BCB)
- Capacitors: (1–3) nF/ mm²(er=23, e.g., Ta_2O_5)

With this value range nearly 70 % of capacitors and 95% of resistors and nearly all inductors of the required passive elements for a wireless cellular can be realized, which demonstrate the large potential for system miniaturization.

WL-IPDs are designed as flip chip mountable as well as wire bondable components by using different thin film substrates like silicon, alumina, or glass. Figure AP25 shows an example of an integrated passive device as a CSP with 2× low-pass filter with 3× inductors 3.9 nH, 2× capacitors 1.8 pF realized with a multi-layer polymer-metal (Cu) redistribution layer on Pyrex.

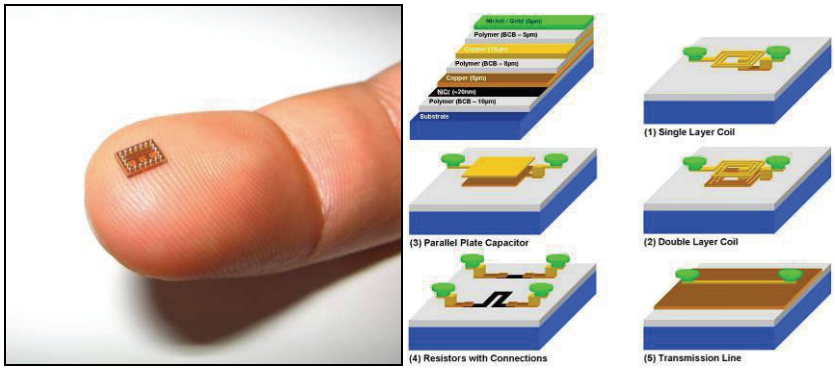


Figure AP25 CSP with Integrated Passive Devices and Thin-film Build-Up Passive Elements

Today's bottleneck for the realization of integrated passive devices are capacitors, In combination with high aspect ratio DRI etching in silicon deep trench capacitors with an value of (20–30 nF /cm^2) can be realized. This very promising technology is currently in development by multiple companies with focus to wafer level System in Package approaches. With respect to cost and form factor, larger passive devices are implemented as SMD devices on top or embedded into substrates for System in Package approaches. Refer to the System in Package section of this chapter.

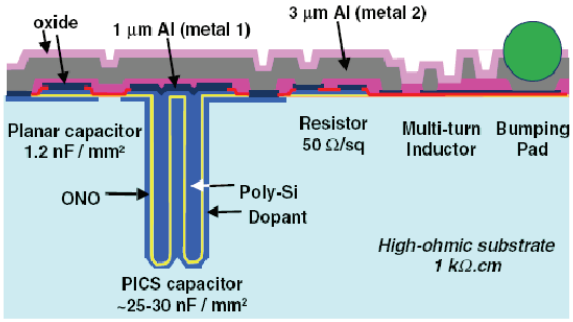


Figure AP26 PICS Substrate with High Density "Trench" MOS Capacitors, Planar MIM, Multi-Turn Inductors, and Poly-Si Resistors [13]

EMBEDDED ACTIVE AND PASSIVE DEVICES

Currently applications on embedded active devices are cellular phone related products e.g., TV tuner, finger print ID sensor. Cellular phone manufacturers and semiconductor manufacturers are expects next generation products on embedded active devices for communication modules e.g., GPS and wireless LAN with passive devices on surface which uses free real estate by embedded active devices. In addition, power supply units with embedded actives and surface mounted passives have also strong demands from market place. Also, image sensor device such as CMOS sensor and strobe light for cellular phone camera will adopts embedded active devices with surface mount passives for reducing form factor. In the very near future, ASICs and graphic processor with stacked memory devices as well as DSC will use embedded active and passive devices.

At this time, two different type of active device are common for embedded applications. One is wafer level package with thinned embedded active devices without copper post for enhanced mechanical strength which are directly interconnected by thin film RDLs, and the other is flip chip with stud bump or copper posts embedded in organic laminates substrates. Figure AP27 represents a schematic overview.

For the economical production of embedded active and passive devices in organic substrates, a chip bonder compatible with printed circuit board work panel size is required. The major issues for embedded technologies are test, yield and quality assurance. Test standard and responsibility of supply chain players are required for embedded active and passive devices to adopted by the markets.

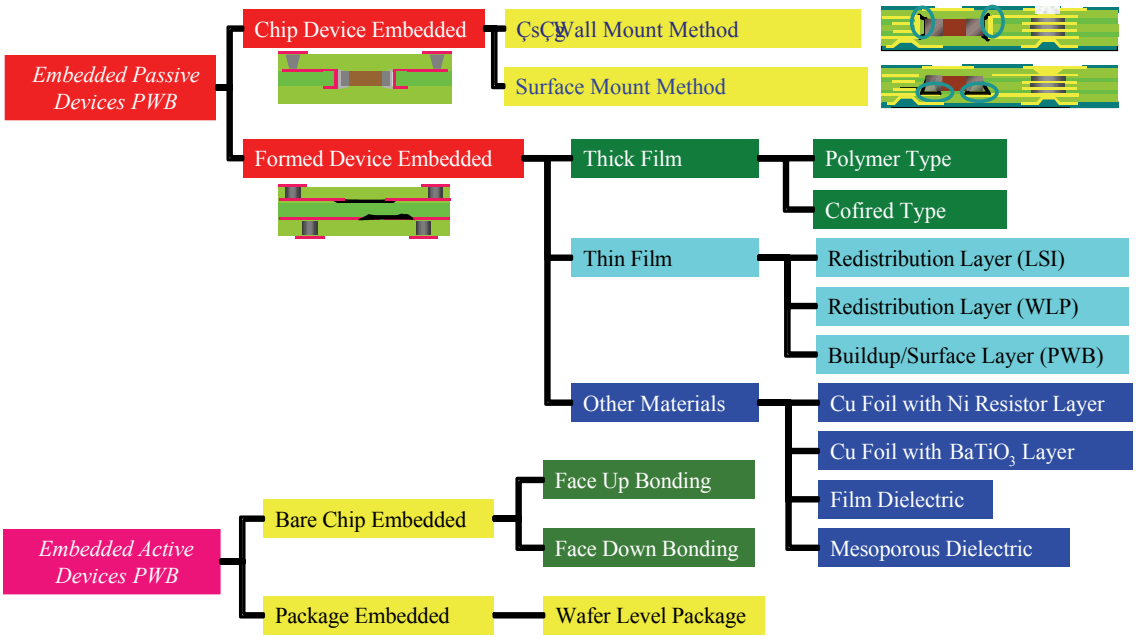


Figure AP27 Overview Embedded Active Devices and Passive Devices

WAFER THINNING AND SINGULATION

The technical challenge for the wafer thinning is not how to grind the wafer but how to retain the die strength after thinning. There are mainly three technical developments; a stress relief after grinding, a dicing before grinding method (DBG), and a wafer carrier support. The entire die must be protected from the chipping or crack damage caused by wafer thinning or die singulation. The DBG and fine wafer-grinding methods, such as wafer grinding by resin bonded wheel, have been introduced. Additional polishing and stress relief processes are required to keep the thinned dice with thickness of 20 µm in 2007 and 8 µm in 2015, durable to the external stress in a package. Singulation of a wafer is another key technology to retain the die strength. Wheel dicing has been the main stream of the singulation, but chipping at the side of the die may induce cracks of the die by external stress at a later stage.

New singulation methods including new laser cut methods or plasma etching will be required. One such method is to focus an infrared laser beam below the surface of the silicon wafer, thus creating a fault line for controlled cracking of the wafer from the inside outwards. Complete breakage may be either spontaneous or by means of expanding the tape upon which the wafer is mounted.

PACKAGING MATERIALS REQUIREMENTS

Packaging materials are at the heart of Assembly and Packaging Technology. Packaging material contributes significantly to the packaged device performance, reliability, and workability as well as to the total cost of the package. With the advent of the "More Moore" and "More than Moore" initiatives, the challenges for packaging materials have broadened from requirements for traditional packages for future generations devices as well as for new package types such as the SiP package families, wafer level packaging, IPDs, TSVs and for applications in RF, MEMs, and optoelectronics.

The Assembly and Packaging industry has been in the midst of a sea change in materials. The bill of materials in packages only yesterday may not be the same tomorrow. And these changes are expected to accelerate in pace and scope in the coming years. Much of the near-term new materials introduction is driven by environmental regulatory compliance requirements including Pb-Free and RoHS compliance (European Union Directive for Reduction of Hazardous Substances). The migration to "green" materials that are lead-free and halogen-free compatible are in full swing. Industry has been adopting "green" materials for the new products packages when they transition to new packaging materials to meet RoHS requirements. . Materials for the traditional wire bond and flip chip packages including molding compound, die attach materials, underfill materials, thermal interface materials (TIM), and package substrates, will have to be improved to meet lead-free, halogen-free, and low-κ/ULK requirements.

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly advanced next generation devices. While wirebond and flip chip remains to be the two basic interconnect methodologies, the introduction of low-κ dielectric materials, increasing power density and hand held

consumer products, imposes additional requirements to traditional materials applications. For example, with the mechanically weak low-κ and the still weaker ultra low-κ dielectrics in the device, comprehensive design of underfill materials properties compatible with the bump materials properties are crucial in addressing the risk for interface stress damage to the dielectric layer. With the increasing thermal output and uneven temperature distribution of many IC device applications, thermal interface materials represent an important opportunity for innovation. The drive for miniaturization through die stacking, package stacking, and low profile packages requires improvements in molding compounds, underfill materials and die attach materials originally developed for traditional single chip packages.

The developments of potential solutions, such as SiP, wafer level packaging, embedded die and passives, and TSV, will call for innovations in design of materials and materials processing innovations beyond what is available today. Wafer level packaging will require materials with improved or different properties as it evolves to meet new packaging applications. Different metallization systems for both redistribution traces and under bump metallization, as well as new dielectric polymers, are needed to meet the ever changing reliability requirements for portable electronic devices. The development of fanout WLP and embedded passives/actives will require new low-temperature embedding polymers and low-temperature cure redistribution layer polymers. TSVs will benefit from new dielectric insulators and conductive via filling media for improved low cost manufacturability. Integrated passive devices (IPDs) will also require better materials, with improved electrical properties, for both resistive and capacitive devices. The major materials challenges are summarized in Table AP19.

Table AP19 Materials Challenges

Materials Challenges for discrete packages	*Issues*
Wirebond	Materials and processes for low profile wirebond loop. Materials and process for multilevel stacked die without wire sweep. 30 um fine pitch wire bond
Underfills	Support higher Tj operation, low-κ die, and compatibility with lead free reflow temperature. Optimal Cu piller underfill
Thermal Interfaces	Increased thermal conduction, lower interface resistance, improved adhesion, higher modulus for heat sink applications
Materials Properties	Methodology and characterization database for frequencies above 10 GHz
Molding Compound	Molding compound for low profile multi-die package. Compatible with low-κ wafer structures with low moisture absorption for high temperature lead free applications Molding compound for hybrid wirebond and flip chip without underfill Gate leakage associated with charge storage in halogen free mold compounds Metal particle contamination and carbon black causing shorts and assembly yield problems for fine pitch interconnect.
Leadfree Solder Flip Chip Materials	Solder and UBM that supports high current density and avoid electromigration
Low Stress Die Attach Material for Tj >200C	No feasible solution known to compensate for TCE mismatch with high thermal and electrical conductivity
Rigid Organic Substrates	Lower loss dielectric, lower TCE, and higher Tg at low cost
Embedded Passives	Improved high frequency performance of dielectrics with κ above 1000; high reliability, better stability resistor materials. Ferromagnetics for sensor and MEMs applications
Environmental Regulatory Compliance	Cost, reliability and performance compatible materials must be identified to replace those banned
Solder Bump Replacement	Flexibility in joining to accommodate stress associated with TCE mismatch over the operating range
Die Attach Film	Thin wafers will suggest combination of dicing film and die attach film in a single film thin material. Lower thickness film Embedded wiring in film
Through Silicon Via Materials Challenges	Low-cost via filling material and process (e.g., low-cost seeding and plating process) Thin wafer handling carrier material and compatible attach material

NEW MATERIALS

Continued evolution of wirebond interconnects as the industry work horse calls for new material sets (wire, capillary, molding compound, die attach materials) to enable 30 μm pitches, low profile multi die stacked packages and multi-row wirebond interconnect without wire sweep. Due to increased assembly reflow temperature for Pb-free package, heat

resistance and package warpage have become major issues for molding compound materials. Molding compound materials are composed of base resin, filler, hardener, and other additives. Improve heat resistivity, proper characteristics of water absorption, good fracture toughness will be required while maintaining excellent workability and surface adhesion to die and substrate surfaces. For handheld and portable applications drop test requirements are now common.

The projected reduction of flip chip bump pitch to 100 µm and below will result in corresponding reduction in UBM via size, bump diameter and gap size. Innovations such as copper piller, alternate solder bump replacement materials and UBM materials set, and underfill materials, thermal interface materials (TIM) will be important for flip chip assembly package structures meeting requirements in environmental excursions, current density (electromigration), high Tj, increasing thermal output, and thermomechanical stresses.

The packaging structure is a heterogeneous materials structure of metals, intermetallics, polymers, and fillers, integrated with the different devices of diverse technologies. Introduction of new materials introduces new materials interfaces. Materials interface science and engineering addressing physical interface properties and thermal, mechanical, and electrical properties of the die-package structure will be of prime importance. With decreasing package profile and decreasing pitch, excellent materials workability to maintain high yield and lower defects are of prime importance.

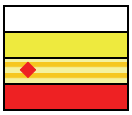
New classes of materials will be introduced into the packaging structure to enable new package features such as embedded and integrated passives, stacked and thinned dies, wafer level process, TSV, flexible interconnect, MEMS, medical and bio chip applications. Metrology and knowledge of packaging materials properties are critically needed for modeling and simulation of electrical, thermal, and reliability performance for package design release and new package development. Methods for accurate characterization of materials properties and materials interface properties for packaging materials in their use environment will be needed. Establishment of materials data bases to make the materials information available to the community will be important for simulation in the drive for consistent and uniform device-package co-design. Materials requirements for package substrates are described in Table AP20.

Table AP20 Package Substrate Physical Properties

	Year of Production	2007	2008	2009	2010	2011	2012
	DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	68	59	52	45	40	36
	MPU Physical Gate Length (nm)	25	23	20	18	16	14
	Glass Transition Temperature (°C)						
State of the Art	Rigid Structure	300	350	350	350	350	350
State of the Art	Buildup Structure	220	250	250	250	250	250
State of the Art	Tape Structure	350	350	350	350	350	350
	Dielectric Constant (at 1GHz)						
State of the Art	Rigid Structure*	3	3	2.7	2.7	2.7	2.7
State of the Art	Buildup Structure	2.8	2.8	2.5	2.5	2.5	2.5
State of the Art	Tape Structure	2.2	2.2	2.2	2.2	2.2	2.2
State of the Art	Ceramics Structure/Low Dielectric Material	4	4	3	3	3	3
State of the Art	Ceramics Structure/High Dielectric Material	100	100	100	100	100	100
	Dielectric Loss (at 1GHz)						
State of the Art	Rigid Structure	0.01	0.01	0.006	0.006	0.006	0.006
State of the Art	Buildup-Structure	0.002	0.002	0.002	0.002	0.002	0.002
State of the Art	Tape Structure	0.0002	0.0001	0.0001	0.0001	0.0001	0.0001
State of the Art	Ceramics Structure	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
	Coefficient of Thermal Expansion: X-Y Direction (ppm/°C)						
State of the Art	Rigid Structure	10	9	8	6	6	6
State of the Art	Buildup Structure	5	4	4	4	4	4
State of the Art	Tape Structure	10	10	10	10	10	10
State of the Art	Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
	Coefficient of Thermal Expansion: Z Direction (ppm/°C)						
State of the Art	Rigid Structure	20	20	15	15	15	15
State of the Art	Buildup Structure with core layer	10	10	10	10	10	10
State of the Art	Tape Structure	10	10	10	10	10	10
State of the Art	Ceramics Structure	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12	4 – 12
	Water Absorption at 23°C/24hrs Dipped (Weight %)						
State of the Art	Rigid Structure	0.04	0.04	0.04	0.04	0.04	0.04
State of the Art	Buildup with Reinforcement Material	0.04	0.04	0.04	0.04	0.04	0.04
State of the Art	Buildup without Reinforcement Material	0.1	0.1	0.1	0.1	0.1	0.1
State of the Art	Tape Structure	0.2	0.2	0.2	0.2	0.2	0.2
	Young's Modulus (GPa)						
State of the Art	Rigid Structure	45	45	45	45	45	45
State of the Art	Buildup with Reinforcement Material	35	35	35	35	35	35
State of the Art	Buildup without Reinforcement Material	6	6	6	6	6	6
State of the Art	Tape Structure	3	3	3	3	3	3
State of the Art	Ceramics Structure	50-400	50 – 400	50 – 400	50 – 400	50-400	50 – 400
	Peel Strength from Cu (kN/m)						
State of the Art	Rigid Structure	1.6	1.6	1.6	1.6	1.6	1.6
State of the Art	Buildup Structure Buildup Layer	1.6	1.6	1.6	1.6	1.6	1.6
State of the Art	Tape Structure	1.4	1.4	1.4	1.4	1.4	1.4

State of the art materials may not be compatible with cost requirements for volume production
Water absorption test is: JIS C6481
Peel strength test: IPC TM650 2.4.8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



SILICON CARRIERS

Organic laminate substrates are large parts of area array type package cost, typically between 30–60% of the package cost depending on application. Because of continuously increasing integration density including integration of active and

passive devices, new carrier solutions are required. Organic laminate based packages today are reaching their limit with respect to integration density at appropriate cost.

Si carriers with metal filled vias (TSV) for use in high density single chip packages and SiP(e.g., for silicon stacking), this approach is an interesting alternative. Si carriers allow higher integration density, better performance, and improved heat removal when compared to other alternatives. The use of IC fabrication technology for redistribution layers allows very dense rerouting and also excellent RF performance at modest cost. High Q inductors and capacitors can be designed. The major challenges for Si carriers are:

- Formation of vias through the Si and filling these via with metal at appropriate cost
- Fabrication of redistribution layers on both sides of the Si carrier Incorporation of stacked device configurations on the silicon carrier

NANOMATERIALS

Materials in use today cannot meet the requirements of future packaging requirements. This is particularly true for complex SiP structures where hot spots, high currents, mechanical stresses for very thin die and every shrinking geometries require electrical, thermal, and mechanical properties that are not available from existing materials. The Emerging Research Materials chapter of this Roadmap describes the materials emerging to meet these needs. The leading candidates for new materials in packaging include the following:

- Low dimensional materials (LDM) may provide nanotubes for improved thermal conduction and improved electrical conductivity to meet the needs of future high density packages
- Macromolecules may provide control of electrical and thermal/mechanical properties of polymer materials such as low k materials to reduce power and improve speed in complex packages
- Self assembled materials may enable high performance capacitors

Many of the materials in use today will be replaced by nanomaterials to meet future needs. Some examples are illustrated in Figure AP28.

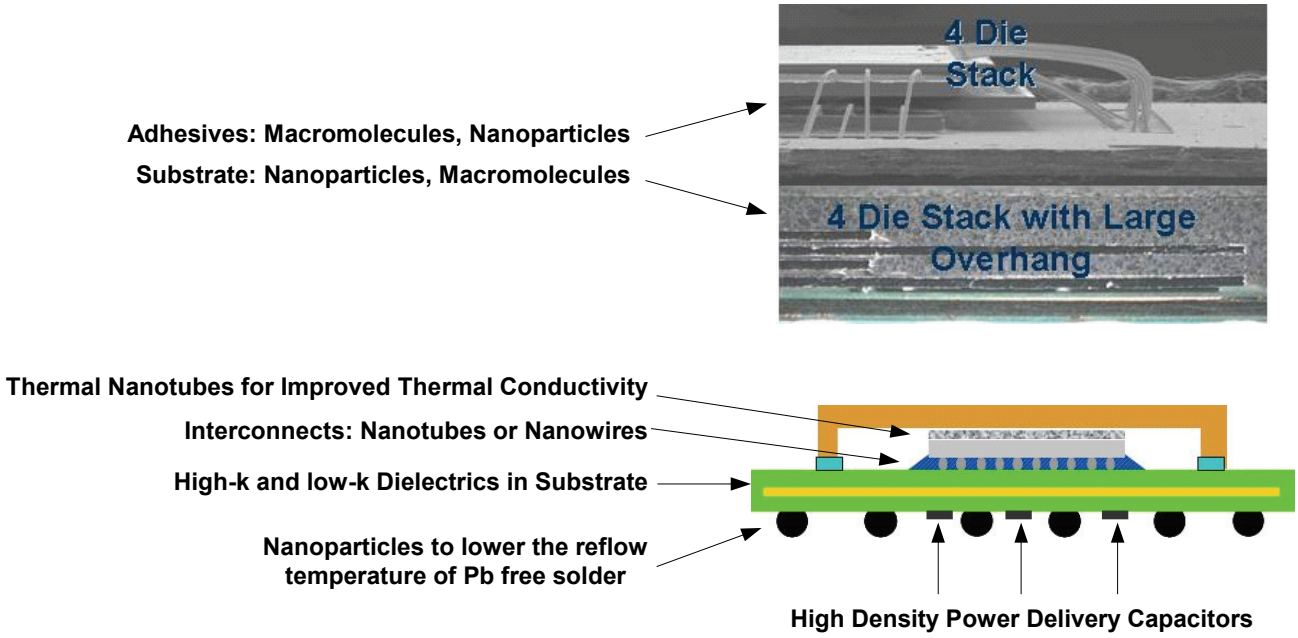


Figure AP28 Emerging Packaging Materials

ENVIRONMENTAL ISSUES

There are important environmental issues that are covered by legislation and additional regulatory actions should be anticipated as new materials are developed and the health and safety issues associated with materials currently in use are better understood. The regulations impact the cost, reliability, and performance of electronics products and have a significant impact on the industry. The history of regulatory constraints is shown in Figure AP29.

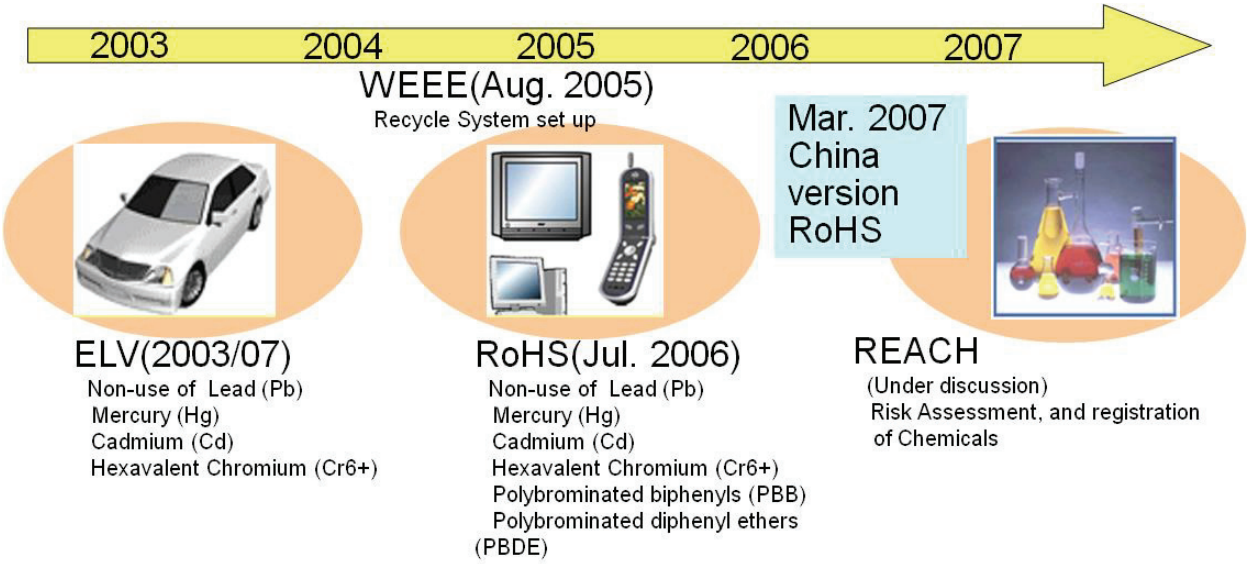


Figure AP29 The History of Environmental Regulation for the Electronics Industry

There are several regulatory activities resulting from environmental considerations that will impact the future SiP technology as well as all other parts of the electronics industry. These include:

ELV	Directive on end-of life vehicles
RoHS	Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment
WEEE	Directive on waste electrical and electronic equipment
EuP	Directive on the eco-design of Energy-using Products
REACH	Registration, Evaluation and Authorization of Chemicals

EQUIPMENT REQUIREMENTS FOR EMERGING PACKAGE TYPES

Assembly and packaging innovations such as wafer level package and system in package have specialized equipment requirements. Current equipment used for wafer level packaging is often modified front end processing equipment. New generations of equipment will be required for wafer level interconnects structures and specialized under bump metallurgy, TSV, and embedded wafer level structures. Examples include: solder bumping, passivation, redistribution, through via interconnect, integrated passives, backside metallization, optical interconnect, dies to wafer and wafer to wafer bonding and post processing thinning. Improvement in throughput and operating cost (cost of ownership) are essential for meeting the cost reduction requirements of the Roadmap.

Wafer thinning equipment exists today but new equipment will be needed as wafer diameter increases and the die thickness continues to decrease. The principal issues will be stress relief and surface thickness variation including roughness. Wafers thinned to 10 µm or less will require improved processes, such as dry polishing, dry etching, and other process combinations.

Another important equipment requirement will be for wafer or chip handling after thinning. Equipment for ultra thin wafer handling, singulation and ultra thin die handling (e.g., pick and place) will require new technology. In addition, a

new generation of die and wafer carriers such as wafer tape and glass plates must be provided to enable safe handling after thinning in all wafer processing equipment.

Emerging System in Package products require assembly equipment with greater versatility and precision. Assembly of SIP with a variety of IC types, optical devices, MEMS devices, and biochips on the same substrate will require substantial extension of current assembly equipment capability.

It is important that the interface between process steps is well defined as packaging technology expands from single chip packaging to system integration (SiP). The boundary between front end processing (wafer fabrication) and the back end of the process (assembly and packaging) is blurring and may differ from one company to another. In order to understand the issues and cost drivers for these overlap processes such as wafer level packaging and through silicon vias, materials, and equipment suppliers are creating alliances or consortia. One example addressing 3D integration using through silicon via technology is the EMC-3D consortium (www.emc3d.org). This consortium will develop processes for creating TSV structures using both via-first and via-last techniques with the goal of reducing today's 3D integration manufacturing cost by 50%. Processes being integrated into the EMC-3D program include:

- Via etch and laser drill
- Insulator/barrier/seed deposition
- High aspect ratio cu plating
- Sequential wafer thinning
- Backside processing
- Chip to wafer assembly and stacking

CROSS-CUT ITWG ISSUES

Assembly and Packaging has become an integrator of the activities and resulting components from all areas into systems and/or subsystems that meet market needs increasingly dominated by the consumer. Cross-cut TWG issues exist with most of the other TWGs however only the most important are covered in this section.

DESIGN

The expansion of packaging to include system level integration embodied in the SoC and SiP technologies brings with it many new challenges that require new approaches in design. The most important need is for co-design tools that will allow co-design and simulation for thermal, mechanical, and electrical properties of complex SiP structures. This is issue is discussed in this chapter and more detail can be found in the paper "*The Next Step in Assembly and Packaging: Systems Level Integration*."

INTERCONNECT

The emergence of wafer level packaging and 3D integration has blurred the boundaries between where the front end process stops with completion of global on-chip interconnect and wafer passivation and the assembly process begins. There are elements of the use of through silicon vias that are addressed on both chapters. TWGs are working together to coordinate the treatment of this important technology to minimize duplication of work and to ensure accurate information is contained in the Roadmap. You will find the issue of through silicon vias addressed on both chapters. The Interconnect TWG is focused on its potential applications in on-chip global interconnect and Assembly and Packaging is focused on its potential applications for 3D integration of multiple die.

RF/AMS WIRELESS

The most common SiPs today are found in cell phones and other wireless communications devices. The continued drive for smaller size, lower power, and higher performance of portable communications devices requires coordinated roadmaps for wireless components and the associated passive components and packaging. The issues that must be addressed include:

- Cross talk and system level noise in the package
- Quality and size of passive components required to support RF components
- Integration of components including devices embedded in package substrates
- Common design tools that address RF/wireless circuits and their integration in SiP architectures

ENVIRONMENT, SAFETY & HEALTH

The introduction of new materials has been both driven by ESH considerations and generated new activity in ESH to identify potential problems with new materials before they are introduced. The ESH TWG is the primary source of guidance for Assembly and Packaging on the environmental regulations and issues we need to address. Examples in the past are the move to lead-free solder and the halogen-free package materials, substrate, and PCB materials. The introduction of not only new materials but different forms of materials already in use pose ESH hazards and cross TWG cooperation is key to addressing these issues. The coming introduction of nanomaterials and the new hazards associated with particle of old materials at that level will be an area of cooperative work for the future.

MODELING & SIMULATION

System level integration at the package level poses many new thermal and mechanical challenges. Reliable products cannot be built unless we understand these issues and design to accommodate them. In the past we could build physical prototypes and characterize those prototypes to ensure they met performance and reliability requirements. The consumer dominated market demands short lead time and low cost. The only possibility for meeting these demands and delivering the required performance and reliability is to do the prototype build and characterization through modeling and simulation. The needs are a key element of cross TWG activity between Assembly and Packaging and Modeling and Simulation.

TEST

New structures bring new failure modes that must be tested and new challenges for testing the failure modes already known. As we integrate system level functionality we must incorporate system level testing. One example of these changing requirements is the drop tests that are now a standard for cell phones and many other portable consumer device applications that contain SiP. The SiP and other multi-chip packages such as stacked memory are increasing demand for known good die. Wafer level packaging places a similar requirement for testing. The issues that must be addressed include:

- Test access for SiP components
- Cost of test for SiP
- High frequency probing for speeds with more than 15GT/s
- Integration of BIST with conventional test resources for SiP
- Contactors for very high pin count devices
- Contactors for wafer level packaging

Cross TWG cooperation to identify the emerging test problems associated with new packaging and interconnect requirements is ongoing. Solutions to these problems will come in part from design, in part from test and in part from assembly and packaging. The challenges of delivering on the promise of “More than Moore” cannot be met without these cross TWG efforts.

GLOSSARY

System in package (SiP)—System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system.

Wafer level packaging (WLP)—Wafer level packaging (WLP) is a technology in which all the IC packaging and interconnection is performed on the wafer level prior to dicing. All elements of the package must be inside the boundary of the wafer. Chips mounted on a structured wafer (e.g. by face to face technologies) and packaged at wafer level before dicing are also considered as wafer level packages.

Integrated passives—Integrated passives are arrays or networks of passive elements including resistors, capacitors, and inductors integrated on a single substrate to form a single passive component.

Embedded passives—Embedded passives are passive components that are incorporated into an IC, added on top of an IC through the addition of a layer, embedded in a build-up polymer interconnect layer or embedded in a package substrate.

3D packaging—3D packaging refers to packaging technologies where a substantial fraction of the die to die interconnections are not planar to the package substrate.

QFP—A ceramic or plastic chip carrier with leads projecting down and away from all sides of a square package. Usually, the back side of the die is bonded to the lead frame substrate, and the electrical connections are made on the active top side of the die through wirebonding process and the whole package is encapsulated by a molding process.

QFN—A ceramic or plastic chip carrier with contact leads underneath the four sides of the package. Usually the backside of the die is bonded to the lead frame substrate, and the electrical connections are made to the die active surface through the wirebonding or flip chip process.

P-BGA—A plastic package employing an array of solder balls for physical connection to the next level which is usually a printed circuit ball. Usually the back side of the die is bonded to a laminate substrate, and the electrical connections are made on the active top side of the die through wirebonding process, and the top side of the package is encapsulated by a molding process.

T-BGA—Tape BGA. Similar to P-BGA where the substrate are made of a circuitized metal on a polymer tape. The interconnection to the die may be made by thermocompression bonding in a single step.

FC-BGA—Flip Chip BGA. Similar to P-BGA where the die to substrate interconnection is made with the flip chip process, i.e. the die faces down with interconnection made through metal (solder) bumps on the die. Usually the space between the die and the substrate is filled with an underfill material.

FC-LGA—Flip Chip Land Grid Array. Similar to FC-BGA, without the solder balls on the array of contact lands on the substrate

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APPENDIX A: CONSORTIA ENGAGED IN PACKAGING

A number of consortia addressing the packaging needs of the semiconductor industry exist. In this Appendix, we summarize some of the consortia activities in table format.

Consortium	Headquarters (Date Formed)	Website	Areas of Interest
CALCE (Center for Advanced Life Cycle Engineering)	University of Maryland, University park, Md (1983)	www.calce.umd.edu	Strategies for Risk Assessment, Mitigation and Management of electronic products and systems -Physics of Failure, Failure Mechanisms and Material Behavior -Design for Reliability and Virtual Qualification -Accelerated Testing, Screening and Quality Assurance -Diagnostic and Prognostic Health Management (failure precursors, stress sensors, condition-based prognostics in semiconductors, components and assemblies) -Supply Chain Assessment and Management (Electronic part obsolescence forecasting and management) -Life Cycle Risk, Cost Analysis and Management (Maintenance, refresh and sustainability planning, cost modeling)
EPACK Lab/CAMP (Electronic Packaging Laboratory/Center for Advanced Microsystems Packaging)	Hong Kong University of Science & Technology (1997)	www.ust.hk/epack-lab	R&D, technical training and industrial services in the following areas: - wafer bumping and flip chip technologies - wafer level and chip scale packaging - through silicon vias and 3D packaging - LED packaging for solid state lighting - silicon bench for passive alignment of optical fibers - lead-free soldering and solder joint reliability computational modeling and simulation
Fraunhofer IZM (Fraunhofer Institute for Reliability and Microintegration)	Berlin, Germany (Headquarters)	www.izm.fhg.de	Non-profit scientific institute for applied research. Areas of interest revolve around: - Packaging and system integration technologies, - Micro Reliability and Lifetime Estimation - Wafer Level System Packaging - 3D System Integration - Thermal Management - RF & Wireless - Photonic Packaging - Large Area Electronics - MEMS Packaging - - Sustainable Technical Development
Fraunhofer IWMH (Fraunhofer Institute for Mechanics of Materials at Halle)		*www.iwmh.fraunhofer.de*	- Failure detection and analysis - Metal physics

HDPUG (High Density Packaging Users Group)	Arizona	www.hdpug.org	Projects include: -Power Cycling/Temperature Cycling Correlation -Flip Chip Reliability Characterization -Flip Chip Reliability Characterization -Lead Free Soldering -Low Temperature Lead Free Soldering -Wafer Scale CSP Reliability -Advanced Flip Chip -Optical Workgroup
IEEC	Binghamton University, NY (1984)	www.ieec.binghamton.edu/ieec/	New York State Center for Advanced Technology Areas of research interest include: -Electrical/Thermal/Mechanical analysis and measurements - Novel materials for packaging - 3D stacked systems - Small Scale Systems Integration and Packaging - Reliability and failure analysis - Roll-to-roll flexible electronics - Product tear down analysis
IFC (Interconnect Focus Center)	Atlanta, Georgia (1998)	www.ifc.gatech.edu	Multi-university research effort addressing long-term exploratory research into the interconnect problems. Headquarted on Georgia Tech campus Research interests include electrical and optical interconnects, thermal dissipation and power management, and circuit and system design and modeling
IME	Singapore (1991)	www.ime.a-star.edu.sg	Non-profit R & D organization established by Agency of Science Technology and Research (ASTAR) focuses on upstream research areas in microelectronics. Three core laboratories: Semiconductor Process Technologies Laboratory Micro system, Modules and Components Laboratory Integrated Circuits & Systems Laboratory Focused research programs in - Silicon Photonics - Nano electronics - Bioelectronics and Biomedical - MEMS & NEMS technology - RF & Wireless systems
IMEC (Interuniversity Microelectronics Centre)	Leuven, Belgium (1984)	www.imec.be	Independent research center IMEC aims to bridge gap between fundamental research at universities and technology development in industry Area of interest include: -CMOS and post-CMOS nanoelectronics -Solar cells -Advanced packaging and interconnection technologies -Bioelectronics and organic electronics -RF devices and technology
ITRI (Industrial Technology Research Institute)	Hsin Chu, Taiwan (1973)	www.itri.org.tw	Non-profit R&D organization established by the Ministry of Economic Affairs Six core laboratories and research interests: -Communication and Optoelectronics -Precision Machinery and MEMS -Materials and Chemical Engineering -Biomedical Technology -Sustainable Development -Nanotechnology

JIEP (Japan Institute of Electronics Packaging)	Japan	www.e-JISSO.jp	Material for 3D assembly CAE research for JISSO system -EMC modeling -Extremely high frequency board design -Noise reduction -PWB fabrication -Micro and nano fabrication -EPADs -Next generation circuit board research -Evaluation method for ion migration -Tin whisker -Advanced JISSO technology -DFT -Optoelectronics JISSO technology -Environmentally friendly JISSO technology -Nano-bio device JISSO technology -Semiconductor packaging
KAIST (Korea Advanced Institute of Science and Technology)	South Korea (1971)	www.kaist.edu	The Center for Electronic Packaging Materials (CEPM) at KAIST (Korea Advanced Institute of Science and Technology) addresses advanced electronic packaging materials, processing technologies, design and reliability of electronic systems. CEPM's main thrust is research and development of the electronic packaging technologies with emphasis on the packaging materials. Their fields of study include Materials Science & Engineering, Mechanical Engineering, Chemical Engineering, and Electrical Engineering.
LETI (Laboratoire d'électronique et de technologie de l'information)	Grenoble, France	www-leti.cea.fr	A CEA (French Atomic Energy Commission) Research lab Areas of interest include: Micro and nano-technologies for electronics and bio Technologies, design and integration of microsystems Imagery technologies Communication technologies and nomad objects
PRC (Packaging Research Center)	Atlanta, GA (1994)	www.prc.gatech.edu	University-industry consortium Headquarter located on Georgia Tech campus Research interests revolve around developing System-on-Package technologies relating to mixed signal design, test, materials, processes, assembly, thermal and reliability
SEMATECH (Semiconductor Manufacturing Technology)	Austin, Texas (1987)	www.sematech.org	Share risks, and increase productivity. Research interests include lithography, materials and processes, manufacturing, 3D interconnects, and workforce development share risks, and increase productivity. Research interests include lithography, materials and processes, manufacturing, 3D interconnects, and workforce development
SRC (Semiconductor Research Corporation)	Durham, NC (1981)	www.src.org	-US semiconductor industry university research management consortium with objectives of solving the technical challenges facing the semiconductor industry and developing technical talent for its member companies -Research interests span short and long term research as well as span from front-end devices to system level issues