INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS

2007 EDITION

EMERGING RESEARCH MATERIALS

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EMERGING RESEARCH MATERIALS

SCOPE

This chapter provides the material research community with guidance on specific research challenges that must be addressed in a laboratory setting for an emerging family of candidate materials to warrant consideration as a viable ITRS solution. Each international technology working group (ITWG) identified needs for new materials to meet future technology requirements and assessed the potential for low dimensional materials (carbon nanotubes (CNTs), nanowires, graphitic systems, and nanoparticles), macromolecules, self-directed assembled materials, spin materials, complex metal oxides, and selected interfaces. For these emerging materials, this chapter also presents requirements for their interfaces, and supporting metrology, modeling, and simulation. While many potential applications were identified for carbon nanotubes, and semiconductor and metallic nanowires because of their unique properties, significant technical challenges must be overcome for them to be useful. As more is understood of other material capabilities, additional applications may be identified for other materials in future roadmaps. Many of the other materials have the potential to be used in multiple applications (e.g., complex metal oxides are considered in both the Spin Materials and the Complex Metal Oxide sections). Similarly, macromolecules for resists may also be used in self assembling materials, so intentional overlaps exist between materials and applications.

As more is understood about the properties and capabilities of other emerging research materials, the mix of materials and applications will change, which will be reflected in future roadmaps. For example, subsequent revisions of this chapter will include quantitative metrics and state-of-the-art results integrated into a table for each family of emerging materials. These tables will summarize, for each potential application, the most likely materials and techniques and sets of performance, interface compatibility, and materials integration requirements.

The scope of emerging research materials (ERM) covers materials properties, synthetic methods, metrology, and modeling required to support future emerging research devices (ERD), lithography, front end process (FEP), interconnects, and assembly and package (A&P) needs. ERD memory and logic devices include evolutionary MOS device technology and more revolutionary devices. Many of the evolutionary and some of the revolutionary ERD can be fabricated with conventional materials and process technologies that are already covered in other sections of the ITRS. Consequently, the ERM chapter will not cover these materials and processes. Emerging lithographic materials include novel molecules that exhibit the potential to enable ultimate feature patterning with resist, imprint, or self assembled technologies. FEP materials include ERM required for future device technologies, as well as novel materials to support selective etch, deposition, and cleaning of future technologies. Interconnect materials include emerging materials for low resistance sub-20 nm electrical contacts, interconnects, vias, and ultra-low κ inter level dielectrics (ILD). Assembly and Packaging materials include novel materials to enable reliable electrical and thermal interconnects, ultra-high power density high speed capacitors, and polymers with unique and potentially useful combinations of electrical, thermal, and mechanical properties.

This year's ERM chapter includes the following material families: low dimensional materials, macromolecules, self assembly mechanisms and self-assembled materials, complex metal oxides, spin materials, interfaces, and heterointerfaces. Many of these materials exhibit potential to address projected requirements in multiple application areas. Table ERM2 in the Introduction section maps families of ERMs to potential applications identified by the above Focus ITWGs. Future editions of this chapter also will comprehend and evolve projected ERM requirements for targeted functional diversification related applications.

DIFFICULT CHALLENGES

The current set of sub-22 nm ERM Difficult Research Challenges is summarized in Table ERM1. Perhaps ERM's most difficult challenge is to deliver material options, with controlled and desired properties, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, interconnect fabrication and operation at the nanometer scale, and packaging options. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled directions. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. For novel nanometer scale materials emerging within the research environment, methodologies and data also must be developed that enable the hierarchical assessment of the potential environment, safety, and health impact of new nanomaterials and nanostructures.

Table ERM1 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤ 22 nm	*Summary of Issues*
Control of nanostructures and properties	Ability to pattern sub 20nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.) Control of surfaces and interfaces Control of CNT properties, bandgap distribution and metallic fraction Control of stoichiometry and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of growth and heterointerface strain Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability Control of interface properties (e.g., electromigration)
Control of self assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components Control of line width of self-assembled patterning materials Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.) Characterization of spin concentration in materials Characterization of vacancy concentration and its effect on the properties of complex oxides 3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the electrical contacts of embedded molecule(s) Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides
Compatibility with CMOS processing	Integration for device extensibility Material compatibility and process temperature compatibility
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

The difficult challenges listed in Table ERM1 may limit the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and nanostructure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish quantitative relationships between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the design and optimization of the required materials properties. The need for validated models requires strong alignment between experimentalists and theorists when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

INTRODUCTION

Emerging device, lithographic, interconnect, assembly, and packaging technologies will require materials with new and dramatically improved properties. The Emerging Research Materials Working Group anticipates and identifies the critical materials properties required for high priority applications in each of these areas. Achieving optimal performance with many of these new materials may require fabrication methods that incorporate novel chemicals, synthetic techniques, and metrology methods. The evaluation and successful integration of emerging materials within targeted applications will depend on our ability to design in and control specific sets of critical material and interface properties. Therefore, the development of a characterization and modeling infrastructure that supports the evolution of robust quantitative structure property correlations represents a strategic priority. These integrated tools would generate a more foundational understanding of novel switching mechanisms, contact formation, and transport mechanisms and drive new synthetic methods and device concepts. Similarly, the fabrication of nano-structured materials, such as nanotubes or nanowires, for devices or interconnects would benefit from an improved understanding of the impact of process and structure on the resulting electronic, mechanical, thermal, and interface properties. For example, spin-related devices may require unprecedented levels of synthetic control, material and isotopic purity, crystal structure, and dopant incorporation to optimize potentially viable spin relaxation, interface spin transmission, and spin de-coherence mechanisms. Self assembling systems must demonstrate the feasibility of high density device, interconnect, or packaging assembly in desired patterns, with the projected dimensional control, beyond what can be achieved by top down lithography. These challenges also will require new measurement capabilities to characterize critical material and interface properties across a hierarchy of temporal and dimensional scales, from atomic through mesoscopic domains. In addition, modeling and simulation, aligned with validation experiments, will be needed to optimize the chemical and structural attributes that improve critical material properties and performance in targeted applications.

POTENTIAL ERM APPLICATIONS

The current set of emerging research materials exhibits potential to impact a wide array of emerging applications. During the past year, several ITWGs identified multiple potential application opportunities for each ERM family, including low dimensional materials (LDM), macromolecules, and self-assembled materials. Conversely, the potential impact of other emerging materials, such as complex metal oxides and spin materials, appears to be more focused on emerging device applications. Consequently, this year’s ERM chapter identifies projected structural and property control requirements for these identified application opportunities. Also, where sufficient published data exist, it benchmarks the status of candidate material capabilities. Table ERM2 provides a matrix of ERM families and selected ITRS Technology Working Groups. Each matrix element contains the ITWG-identified potential application opportunities for the specified ERM family of materials included in this year’s chapter.

Table ERM2 Applications of Emerging Research Materials

MATERIALS	ERD MEMORY	ERD LOGIC	LITHOGRAPHY	FEP	INTERCONNECTS	ASSEMBLY AND PACKAGE
Low Dimensional Materials	Nano-mechanical Memory	Nanotube Nanowire Graphene and graphitic structures	High-index immersion liquids		Nanotubes Metal nanowires	Electrical applications Thermal applications Mechanical applications
Macromolecules	Molecular memory	Molecular devices	Resists Imprint polymers	Novel cleans Selective etches Selective depositions	Low-κ ILD	Polymer electrical and thermal/ mechanical property control
Self Assembled Materials			Sub- lithographic patterns Enhanced dimensional control	Selective etch Selective deposition Deterministic doping	Selective etch Selective deposition	High performance capacitors
Spin Materials	MRAM by spin injection	Semiconductor spin transport Ferromagnetic (FM) semiconductors FM metals Tunnel dielectrics Passivation dielectrics				
Complex Metal Oxides	1T Fe FET Fuse-anti-fuse	Multiferroics (Spin materials) Novel phase change				High performance capacitors
Interfaces and Heterointerfaces	Electrical and spin contacts and interfaces	Electrical and spin contacts and interfaces			Contacts and interfaces	

LOW-DIMENSIONAL MATERIALS

Low-dimensional nanostructured materials [LDM], such as nanotubes, nanowires, and nanoparticles, have unique properties that may enable their use as potential solutions for future devices, interconnects, lithography, and packaging technologies. These nanomaterials exhibit a diverse array of novel properties. For example, carbon nanotubes may offer high thermal conductivity and ballistic electronic transport. Semiconductor nanowires may enable efficient surround-gate transistors, and metal nanowires may be useful for low-resistance metal interconnects. Metal nanoparticles, with a high surface-to-volume ratio, can melt at temperatures well below that observed for the corresponding bulk metal and may enable future packaging options. Additionally, quantum confinement in semiconductor nanoparticles and nanowires may enable efficient bandgap engineering, as their optical bandgap energies appear to vary inversely with LDM size. Table ERM3 identifies potential applications and key research challenges, which gate their adoption as potential solutions.

Table ERM3 Potential Applications and Challenges for Low Dimensional Materials

APPLICATION	POTENTIAL MATERIAL VALUE	KEY CHALLENGES
Devices: 1D Memory and Logic Devices	Nanotubes exhibit ballistic transport and potential high performance	Control of bandgap and metallic versus semiconducting Control of carrier type and concentration Electrical properties must not degrade when embedded in a dielectric Control of location and orientation Control of contact resistance
	Nanowires could enable surround gate structures and novel heterostructures	Control of location and orientation Performance exceeding patterned materials Catalyst and processing temperatures compatible with CMOS
Devices: Planar CMOS	Graphene and related graphitic structures have high mobility without CNTs alignment challenges	Compatibility with CMOS Edge passivation Control of dielectric interfaces
Interconnects and Vias: Nanotube	Nanotubes have ballistic transport, high current carrying ability, and resistance to electromigration (EM)	Ability to place CNTs in precise locations and with controlled direction Ability to grow with high density Conductivity must not degrade when embedded in a dielectric Low contact resistance
Interconnects: Nanowire	Single crystal smooth metal nanowires could reduce grain-boundary and sidewall scattering	Ability to grow long single-crystal high-conductivity nanowires Ability to place the nanowires in precise locations and with controlled direction
Lithography: High Index Immersion Fluids	High refractive index nanoparticles increase solution refractive index (>1.8)	Identifying high refractive index nanoparticles that have low absorption at 193 nm and are insoluble in the liquid Achieving low solution viscosity Low 193 nm radiation scattering Low abrasion to optics
Packaging: Nanotube Chip-to-package Interconnects	Nanotubes can carry high current density, have high mechanical strength and thermal conductivity Compensation for materials with dissimilar CTEs	Temperature compatibility with CMOS or package Low contact resistance High density for low resistance Low cost
Packaging: Nanotubes for Thermal Heat Spreading	Nanotubes have a high intrinsic thermal conductivity and high flexibility	Integrating a high density of aligned CNTs in a polymer matrix Achieving a low thermal contact resistance Functionalizing and integrating the CNTs in the polymer without degrading thermal conductivity
Packaging: Nanoparticles to Modify Package Polymer Properties	Nanoparticles can change polymer CTE, modulus, toughness, and reduce diffusion of impurities	Ability to integrate multiple nanoparticle types and predictably achieve all required properties (rule of mixtures) Effective functionalization to keep different nanoparticles from agglomerating Cost
Packaging: Nanoparticle solders	Metal nanoparticles can sinter at low temperatures and result in high conductance, high reliability solders	Integration and infrastructure

CTE—coefficient of thermal expansion

Table ERM4 Emerging Research Materials—Demonstrated and Projected Parameters

Low Dimensional Materials			*Nanotubes for Vias*	*Nanotubes for Interconnects*	*Nanotubes for FET Channels*	*Nanowires for FET Channels*	*Nanowires for Interconnect*
Materials and Techniques	*Operating Mechanism*		Ballistic transport	Ballistic transport	Ballistic transport	Drift/diffusion	Drift
	Material System		MWCNT or SWCNT	MWCNT or SWCNT	SWCNT	Si, Ge, or III-V compounds	Metal (especially. Cu)
	Synthetic Method		In situ thermal CVD Hot filament CVD Plasma CVD	Thermal CVD Hot filament CVD Plasma CVD	Thermal CVD Plasma CVD	CVD	CVD or ECD
	Critical Material Property		Diameter, density, metallic	Diameter, density, metallic	Semiconducting bandgap	Diameter, doping	Resistance
ITRS Performance Requirements	*Diameter (nm)*	Goal	≤ 5	≤ 5	≤ 2	3–200	M1 (14 nm half pitch)
		Demonstrated	0.4–10	0.4–10	0.4–3	<5 [g] –200 [h]	
	Density or angular placement accuracy	Goal	Density (≥ 0.05 MWCNT/nm^2)	Density (≥ 0.05 MWCNT/nm^2)	Density (0.5 SWCNT/nm^2)	~10^{-2} radians (0.6 deg)	~10^{-3} radians (0.06 deg)
		Demonstrated	~0.01 MWCNTs/nm^2 [a]	In progress	In progress		[k]
	Direction /Orientation	Goal	Perpendicular to the substrate	Parallel to the substrate	Controlled direction (TBD)	Controlled direction (TBD)	Parallel to the substrate
		Demonstrated	MWCNTs: Good SWCNT: Poor	MWCNTs: Fair[d] SWCNT: Poor	Controlled using SAM template or electric field	Mainly (111), Also (100 and 110) [i]	
	Length (μm)	Goal	0.05–0.30	M1: 1–5	≤1	2	M1: 1
		Demonstrated	0.06–0.52 [b]	>100	Good	Si: >20 (12 nm diameter)	Cu: ~6 [l]; 40 [m]
	Doping [electrically active] (cm^{-3})	Goal	Metallic	Metallic	n and p type	~10^{18}–10^{19}	N/A
		Demonstrated	Mostly Metallic	Mixed	Demonstrated by Chemical Functionalization	Si ~2×10^{18} [h]	
	Resistivity (μΩ-cm)	Goal	TBD	M1: ≤8 (for 14 nm half pitch)		5000-40,000	Cu:≤3
		Demonstrated				30,000 [h]	Cu(ECD): 5.7 (D=15 nm), [l]
	Contact resistance (kΩ/LDM)	Goal	≤ 0.50 /MWCNT	≤ 0.50 /MWCNT	≤ 10 /SWCNT	<10% NW resistance	<10% NW resistance
		Demonstrated	10–200 /CNT[c]	10–200 /CNT		Ohmic [h]	
	CMOS compatibility	Goal	T = 400°C, compatible catalyst	T=400°C, compatible catalyst		Non-Au catalyst	T < 450°C
		Demonstrated	T = 400°C Co catalyst[d]	In progress	In progress	Ti, Pt, etc. for Si Not for Ge	100°C for Cu [l]
	Electro-migration (10^6 A/cm^2)	Goal	>10	>10		Bulk	Bulk
		Demonstrated	CNT: >3 [e]	None			
	Maximum current density (A/cm^2)	Goal	≥ 10^7	≥ 10^7		Bulk	
		Demonstrated	≥ 10^9 [f]	≥ 10^9		I_{dsat} = 1.94mA/μm (pFET) I_{dsat} = 1.44mA/μm [j]	

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MWCNT—multiwire CNT SWCNT—single wire CNT SAM—self-assembled material

Each demonstrated result posted in Table ERM4 requires support from at least two published papers. "Demonstrated results" with one referenced citation warrant confirmation and should be considered as preliminary.

Notes for Table ERM4:

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[f] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes", Appl. Phys. Lett. 79, 1172 (2001).

[g] N. Singh, A. Agarwal, L. K. Bera, T. Y.Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, "High-performance fully depleted silicon nanowire (diameter ≤5 nm) gate-all-around CMOS devices", IEEE Electron Device Letters 27, 383-6 (2006).

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[i] M. Kobayashi, and T. Hiramoto, "Experimental study on quantum structure of silicon nano wire and its impact on nano wire MOSFET and single-electron transistor," IEDM Technical Digest (2006), paper 6.7

[j] K. Hwan Yeo, S. D. Suk, M. Li, Y.-y. Yeoh, K. H. Cho, K.-H. Hong, S. K. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D.-W. Kim, D. Park, and B.-I. Ryu "Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires," IEDM Technical Digest (2006), paper 20.2.

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[l] A. Bid, A. Bora, and A. K. Raychaudhuri, "Temperature dependence of the resistance of metallic nanowires of diameter >15 nm: Applicability of Bloch-Gruneisen theorem", Phys. Rev. B 74, 035426(2006).

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CARBON NANOTUBES

Carbon nanotubes can exhibit many unique properties, including high thermal conductivity, mechanical strength, and current carrying ability. Additionally, their long ballistic transport lengths are valued for device and interconnect applications. Mobilities of 79,000 cm^2/V-sec[1] have been reported for SWCNTs over 300 µm long and ballistic transport has been reported for ~300 nm SWCNTs.[2] For MWCNTs synthesized at low temperatures, the ballistic transport length can be as long as 80 nm,[3] while MWCNTs grown at higher temperature have ballistic lengths over 1 µm.[4] In the ballistic-transport regime, the resistance corresponds to the quantum resistance, which is independent of the length. This section defines the CNT related research requirements for potential applications identified this year by the other ITWGs. While there is much interest in their properties, many challenges remain. For electronics applications, chemical vapor deposition (CVD) is currently the dominant fabrication technology because of its cleanliness and relatively low growth temperature. CNTs can be formed as single-walled nanotubes (SWCNTs) and multi-walled nanotubes (MWCNTs).

DEVICE APPLICATIONS

A key challenge for carbon nanotubes to be viable in high performance FETs is the requirement for processes that provide a tight distribution of semiconductor bandgaps, with each nanotube placed in a desired location, with a specified direction, and a low contact resistance. Please refer to the 2007 ITRS ERD chapter for detail on these devices.

Nanotube Bandgap Control

Carbon nanotube FET-related applications are motivated by their high mobility and ballistic transport.[5] For SWCNTs to be viable for future CMOS applications, the ability to grow them with a tight bandgap distribution must be demonstrated. To achieve *in situ* bandgap distribution control, the diameter and chirality must be controlled in the growth process. While the diameter of single-walled nanotubes scales controllably with decreasing catalyst size, as discussed in the Catalyst Design Section, chirality control remains a significant synthetic challenge. Recent reports show that CNTs grown by plasma CVD tend to exhibit a relatively high ratio (~90%) of semiconducting CNTs,[6, 7] however, this level of bandgap distribution control is far short of the projected requirements. Considerable research is needed to develop understanding that will enable design of catalysts and processes for *in situ* growth of CNTs with sufficiently controlled bandgap distributions.

An alternate approach to achieving tight bandgap control is to chemically purify the nanotubes after growth. Methods that show some promise for enabling post-growth separation include selectively reacting and evaporating metallic CNTs within a mixed nanotube bundle. Hydrogenated metallic SWCNTs can be selectively etched over semiconducting SWCNTs by passing a high-current through the bundle in the presence of hydrogen and laser irradiation. Key challenges include the development of separation schemes that can differentiate between nanometer structures that are chemically the same, but structurally and electronically different, and achieving parts per trillion purity for bandgap control. A promising set of metallic/semiconducting CNT separation techniques includes dielectrophoresis,[8] selective precipitation,[9] ion exchange chromatography,[10] and compaction/centrifuging.[11, 12]. The purity achieved with these techniques is far short of the parts per trillion required for CMOS applications. More work is required to improve the effectiveness of these or other techniques, but off wafer purification techniques also required processes that enable accurate placement control.

Control of Carrier Concentration (Nanotube "Doping")

A critical device challenge is carrier concentration control in embedded p-type and n-type materials. Typically, semiconducting CNTs tend to be p-type after growth. Research is needed to develop a mechanistic understanding of selective and controllable n- and p-type CNT doping. While CNT carrier concentrations can be modulated by exposure to NO_2 and $NH_{3,}$[13] this modulation does not appear to be stable in the absence of the gas. Schottky-barrier CNT transistors treated with trifluoro-acetic acid (TFA) exhibit improved device performance over untreated CNTs.[14] These approaches may be suitable for chemical-sensor applications, but not for embedded-device applications. The ability to control hole concentrations in CNTs by surface functionalization[15] has been demonstrated to be stable in air. However, guiding principles are needed to satisfy projected p- and n-type doping-control requirements for CNTs embedded in dielectrics. Research also is needed to explore different mechanisms for controlling carrier type, such as chemical substitution during or after growth, as well as charge transfer through interface layers.

Gate Dielectric Interface

High-performance CNT-FETs have been reported with high-permittivity dielectrics, such as $SrTiO_{3,}$ employed as the gate insulator.[16] Since a CNT's sidewall is relatively inert, the surface may be chemically functionalized to improve dielectric adhesion. The behavior and operational stability of the CNTs can be influenced by functionalization and by the nature of the local passivation film environment. CNT-FETs that use SiN as the passivation layer appear to exhibit very low I-V curve hysteresis.[17] Research and guiding material design principles are needed for enhancing functionalization, interface passivation, and dielectric deposition. This is discussed in more detail in the Interface and Heterointerface section.

NANOTUBES FOR ELECTRICAL INTERCONNECT AND VIA APPLICATIONS

For nanotubes to be used as interconnects or vias, high densities of highly conducting nanotubes in desired locations must be demonstrated, with controlled direction and low-resistance contacts. Both SWCNTs and MWCNTs are potentially viable candidates for electrical interconnects. SWCNTs exhibit ballistic transport over longer distances,[18,19] but consist of a mixture of metallic and semiconducting tubes, while the MWCNTs are metallic.

A potential advantage of CNTs for vias is their ability to carry high current density without electromigration. For via applications, achieving a competitive resistivity is a critical challenge, which requires a high packing density of highly conducting SWCNTs or MWCNTs and good electrical contacts. In the case of MWCNTs, tradeoffs may need to be made in the diameter and number of walls to achieve the highest density. For SWCNTs, processes are needed that enable a higher fraction of metallic tubes. Both types of CNTs need to form low resistance contacts that are resistant to electromigration, as is discussed in more detail in the Interface and Heterointerface Section.

The low resistivity of CNTs may offer potential advantages for interconnect applications. This low resistivity may be attributed to their ability to achieve ballistic transport, high current carrying ability, and potential electromigration resistance. SWCNTs also exhibit quantum limited contact resistance. Consequently, their length must be sufficient to yield favorable effective resistivities, as described in the Interconnect chapter.

Similarly, for via or interconnect applications, CNT conductivity must remain high and stable during operation. Research and guiding material-design principles are needed for improved CNT functionalization, deposition, and positional control.

GROWTH IN CONTROLLED LOCATIONS WITH ALIGNMENT

For CNTs to be used as either devices or interconnects, they must be grown in precise locations and aligned in required directions. Since interconnects span relatively long distances, i.e., ~1 micron, the alignment requirements for this application are more stringent than for individual devices. While progress has been made in growing nanotubes in desired locations,[20] directional alignment remains a challenge. Recent results suggest that CNTs grown in a directed electric field or along crystal steps could achieve general directional alignment;[21, 22] however, the practical implementation of this concept to manufacturing remains elusive.

Synthetic methods have yet to be developed that ensure the growth of CNTs in desired locations with the required alignment and performance. Post-growth assembly options also are being explored, as will be discussed in the Directed Self Assembly section; however, these approaches also lack the required positional control or alignment accuracy.

CONTACT FORMATION (OHMIC AND SCHOTTKY BARRIERS)

A critical challenge for device and interconnect applications is the ability to form reliable, low-resistance electrical contacts between the CNT and the metal electrode. For device applications, reproducible Schottky barriers are needed. Low contact resistance can be achieved by selecting metals that form a low-resistance carbide layer and/or a low Schottky barrier, as is described in more detail in the Interface section. In the case of MWCNTs, it is important to obtain low contact resistance and good electric contact between the electrode and the inner layers of the MWCNT. In CNT vias, it has been proposed to cut a CNT perpendicularly to its axis by chemical mechanical polishing (CMP) and to form an electrode across the entire cross section, thereby making use of the inner layers as well as the outer layer for electric conduction.[23] Refer to the Interface section for more details

NANOWIRE SYNTHESIS AND PROPERTIES

SEMICONDUCTOR NANOWIRES FOR DEVICES

Nanowires may enable new device functionality with surround gate structures and novel heterostructures. The most important challenges for nanowires are to 1) position the nanowires during growth or reposition them after growth at the desired location and with the desired direction; 2) provide performance exceeding patterned materials; and 3) have CMOS compatible catalysts. Several techniques may enable nanowires to be grown in predefined locations with controlled crystal orientation; however, selective nanowire growth in a preferred direction remains a challenge. (Refer to the Emerging Research Devices chapter.)

Catalytic CVD methods can be used to grow single crystal nanowires of many semiconductor materials, including Si,[24, 25] Ge,[26, 27, 28] and compound semiconductors such as InP, InAs,[29, 30, 31, 32] and ZnO.[33] A metal-catalyst nanoparticle accelerates the decomposition of a gaseous precursor to form the nanowire at a temperature lower than the normal decomposition temperature of the precursor gas. Larger diameter nanowires often grow in the <111> orientation, which can be used to define a growth direction; however, very thin nanowires may grow with different crystal orientations[34, 35, 36] and consistent control is not routine. While sidewall growth can be limited by the choice of growth conditions or chemical passivation, more research is needed to understand the factors that drive sidewall growth and passivation. Because of the limited contact area between a nanowire and the substrate on which it is grown, nanowires can be grown on substrates with different lattice parameters. Additionally, defects that propagate at angles to the growth axis can terminate on the sides of the nanowires, so their impact appears to be limited.

Like CNTs, nanowires either can be grown in the location where they are to be used, or they can be positioned after growth. Advanced techniques, such as nanoimprint lithography or the application of an electric field, can be used to position the catalyst nanoparticle and, consequently, determine where the nanowire will grow. By forming the catalyst nanoparticle at the desired location, nanowires can be grown in place, so the position of the nanowire and its ends are known accurately.

The electrical properties of larger-diameter nanowires (i.e., >8 nm for Si) appear to be similar to those observed in bulk materials. However, surface scattering may reduce carrier mobility, as observed for nanostructures formed by other techniques. The electronic structure of very narrow nanowires (i.e., <6 nm for Si) appears to be modified by quantum confinement, increasing the effective band gap.[37]

Dopant atoms can be incorporated into nanowires, either during growth or subsequent to growth; however, doping mechanisms can vary, depending on the material and the dopant incorporation technique. Dopant atoms may be incorporated through the catalyst nanoparticle, which is preferred,[38] or may be diffused though the sidewalls after growth. Preliminary experiments with Si nanowires indicate that techniques used to control surface states on bulk silicon should be applicable to nanowires, with the added complication that many different crystal lattice planes are exposed on the nanowire's surface. For example, thermally grown silicon dioxide reduces the Si nanowire surface-state density.[39] To form low-temperature nanowire devices, Ge often is used in conjunction with atomic layer deposition (ALD) techniques that deposit a high-permittivity gate dielectric after removing the unstable germanium oxide *in situ*.[40] Nanowire interfaces and contacts are critically important for any electrical application, as will be discussed in the section on Interfaces and Heterostructures.

Nanowire Heterostructures

Axial nanowire heterostructures can be formed by sequentially depositing regions of different semiconductor materials when the same catalyst can be used.[41, 42] The transition region from one semiconductor material to another during nanowire growth may limit the possible useful combinations of semiconductors,[43] as interface grading may occur at high temperatures or with a molten catalyst due to slow removal of previous species from the catalyst nanoparticle. In other cases, spatially abrupt transitions occur when atoms of the element whose concentration is decreasing rapidly escape from the nanoparticle into the gas phase, when the gas-phase partial pressure of that species is reduced.

In addition to forming axial segments of different semiconductors, a “core-shell” nanowire heterostructure can be formed.[44] For these heterostructures, a nanowire of one semiconductor is first grown by metal-catalyzed CVD. Then the growth conditions are changed so that a layer of a different semiconductor is grown by uncatalyzed CVD on the sides of the nanowire to form the “core-shell” structure. For example, a Si shell can be grown around a Ge nanowire [44] to create a structure that confines holes away from the surface of the composite nanowire because of the valence-band offset between Si and Ge. Heterostructures are discussed in more detail in the Interfaces and Heterostructures section.

METAL NANOWIRES

If single crystal nanowire metals could be grown with smooth surfaces, they could reduce many of the issues associated with grain boundary induced resistivity increases and sidewall roughness scattering, as illustrated in the Interconnect Cu Resistivity chart in the Interconnect chapter. Metal nanowires typically are produced by electrochemical deposition in a template, often made of porous Al_2O_3 or polycarbonate,[45] containing pores of the desired nanowire diameter. Nanowires also can be formed by reaction in a liquid solution without using a template.[46] Nanowires of several different low-resistivity metals have been formed, e.g., Au, Ag, Cu, but only limited electrical resistivity data are available. Resistivities of 3–6 μΩ-cm are reported for Cu nanowires, with diameters of 15–50 nm, grown by electrodeposition within templates,[45] which is consistent with the normal Cu interconnect resistivities cited in the Interconnect Cu Resistivity chart in the Interconnect chapter. Self-assembly methods may produce nanowires with smoother surfaces, reducing surface scattering. Hydrogen passivation might reduce diffuse surface scattering and the diameter-dependence of resistivity.[47] In polycrystalline nanowires, hydrogen passivation also might reduce grain-boundary scattering.

NANOWIRE POST-GROWTH ASSEMBLY TECHNIQUES

Consensus has yet to be reached on preferences for *in situ* versus *ex situ* growth and placement processes. In principle, growing nanowires and then positioning them allows a wider range of nanowire deposition and growth conditions. A critical challenge for this approach is to position and bond each nanowire on the substrate, precisely where it is needed and in the right orientation. Nanowire suspensions that are flowed across a substrate can deposit nanotubes or nanowires on a substrate surface, but in random positions and directions. Defined 3D structures, such as channels, or external electric field gradients can provide some one-dimensional order and control over nanowire positioning. For more information, please see the Self Assembly topic in the Nanomaterials section.

CATALYST DESIGN AND CONTROL FOR NANOTUBES AND NANOWIRES

The synthesis of nanotubes and nanowires often relies on catalytic processes. Consequently, catalyst design represents an emerging challenge for enabling the controlled synthesis of these potentially useful low-dimensional materials. SWCNT catalysts typically are composed of varying compositions of Fe, Co, and/or Ni. Catalysts used to synthesize MWCNTs also are made from these elements, as well as refractory metals, such as Pt. Nanowire growth is catalyzed by a range of metals. One commonly used catalyst, Au, is known to introduce deep levels near the middle of the Si bandgap, which raises serious concerns about contamination in the nanowire or in the nearby devices. Other metals, such as Ti, Pt, Pd, Ni, and Ga, also promote Si nanowire growth and should be more compatible with CMOS processing. Catalysts for Ge nanowire growth are more limited, with Au being used almost exclusively.

Nanotube[48, 49, 50] and nanowire diameters roughly correlate with catalyst diameter. Correlations of catalyst nanoparticle composition, catalyst nanoparticle morphology, and the growth process with nanotube or nanowire location, orientation, structure, electronic properties, and performance also appear to be significant; however, many of these correlations are not well understood. Guiding principles are needed that enable robust catalyst design and growth processes, which yield nanotubes with controlled dimensions, orientation, placement, chirality, and electrical properties.

Catalyst nanoparticles can be pre-formed by solution or gas-phase techniques and then dispersed on the surface where the nanowires are to be formed. Gas-phase techniques allow *in situ* nanoparticle formation, size selection, and placement on the substrate surface prior to nanowire growth. Solution techniques also tend to yield nanoparticles with narrow diameter distributions. Alternatively, surface tension and heating can cause catalyst material evaporated on a substrate to agglomerate into nanoparticles, although with broader diameter distributions. None of these techniques guarantee catalyst particles with identical nanostructure. Electrochemical and block co-polymer techniques have also been used to form and position the nanoparticles. This is discussed in more detail in the *Self Assembly* section.

GRAPHITIC SYSTEMS

Graphitic materials, such as graphene, have potential for circumventing many of the integration challenges that face CNT technology for fabricating high mobility planar devices. (Refer to the Emerging Research Devices chapter.) The key challenges are to identify viable CMOS compatible processes, edge, and interface passivation control, and the formation of structures with geometries suitable for devices. Graphene[51] may enable novel and complementary applications to carbon nanotubes (CNT), its 1D counterpart. Graphene is receiving considerable attention because it exhibits ambipolar carrier conduction,[52] a carrier mobility as high as $\sim 2\times10^6$ cm^2/V-sec, and a defect density of $\sim1\times10^{10}/cm^2$.[53] This mobility is better than the mobility reported for small gap InSb and also is practically independent of temperature, thus opening the possibility of room temperature ballistic transport at the submicrometer scale. Currently, graphene films are fabricated by silicon sublimation from SiC, chemical vapor deposition, or by physical transfer deposition onto a substrate.

Graphene on SiC can be patterned and etched by conventional planar lithography techniques and has the best reported transport properties,[54] but processing temperatures, 1200–1400°C, are incompatible with CMOS fabrication. Planar graphene layers have been grown by CVD on nickel substrates,[55] but they are over twenty graphene layers thick.[56] Physical transfer of small sheets of graphene film onto an insulating substrate,[52] typically SiO_2, yields monolayer transfer,[57] but it is a complex process involving multiple micro cleaving steps. To date, physical transfer deposition of graphene films is the most reliable technique to obtain monolayer graphene films for further electronic device fabrication, but the process is very cumbersome.

Since the bandgap of nanoribbons varies inversely with the ribbon width, it is possible to pattern and tune their electronic properties, such as bandgap opening due to lateral size quantization, though dimensional control. Additionally, the states at the edges of the graphene ribbons significantly affect graphene's electronic properties.[58, 59] A foundational understanding of the factors that control graphene's properties is needed.

In contrast to nanotubes, graphene's planar structure is expected to display more interactions with the substrate on which it is deposited, showing sensitivity to the substrate trapped charge.[58] The ability to deposit high-permittivity dielectric on graphene is just emerging,[59] and needs more research.

NANOPARTICLES FOR HIGH REFRACTIVE INDEX IMMERSION FLUIDS

Lithography is seeking a high refractive index, $n_D>1.8$, immersion fluid for 193 nm applications, with low absorption and low viscosity. It also must be non-corrosive and exhibit optimal resist and lens wetting properties. Viable candidates have yet to be identified.

A liquid suspension of transparent ultra-high refractive index nanoparticles[60] represents one potential approach for increasing a liquid's refractive index. For nanoparticle immersion fluids to be viable, the refractive index of the suspension must exceed 1.8. This suspension also must not increase the 193 nm scattering or absorption, have reasonable viscosity, and not be abrasive to the optics or resist. Research is needed to design ultra high refractive index nanoparticles and compatible liquids that satisfy these requirements.

NANOSTRUCTURES FOR PACKAGE APPLICATIONS

Future packaging applications require new materials that provide low electrical resistance, high reliability, chip-to-package interconnects, improved thermal management, and packaging polymers with improved mechanical properties. Potential material solutions are needed that enable chip-to-package electrical connections with high electrical conductivity, low inductance, high electromigration resistance, and low mechanical stress on the chip. Efficient heat removal requires new materials and engineered contacts, with high thermal conductivities, i.e. > 400W/m-K, and low thermal contact resistance. Additionally, packaging polymers, nanoparticles, and additive composites are needed that exhibit sufficient toughness, along with low coefficients of thermal expansion and decreasing modulus, to demonstrate the feasibility of satisfying projected ITRS packaging requirements. Certain families of nanoparticles have properties that may support these requirements, but significant material and integration challenges must be overcome for these low-dimensional materials to be viable as potential solutions.

CHIP-TO-PACKAGE ELECTRICAL INTERCONNECTS

Low-dimensional materials, such as carbon nanotubes or nanosolder alloys, may provide electromigration resistant chip interconnects. However, key challenges will be for the assembly of these materials to be compatible with packaging processes and to provide the required electrical resistance, reliability including interface electromigration, and low assembly cost. The magnitude of electromigration is a function of the carrier material and the current density, which is expected to increase with future generations of interconnect technology. Electromigration in chip to package interconnect solders [61] occurs at current densities above $\sim10^4$ A/cm^2. Correspondingly, electromigration[61] occurs in copper above current densities of $\sim10^6$ A/cm^2. Carbon nanotubes and novel low melting point nanosolders may provide high resistance to electromigration.

The important challenges for SWCNT or MWCNT interconnects include controlled contact resistance, accurate nanotube and bundle placement, low-temperature growth methods, mechanical and thermal performance, and package reliability.

Lowering the nanotube growth temperatures to <250 °C is challenging. While nanotubes are reported to be stable at current densities $>10^7$ A/cm^2,[62] it remains to be demonstrated whether they can be integrated to achieve sufficiently high densities of reliable low-resistance and low-inductance contacts. Consequently, while significant research challenges remain, nanotubes show promise for enabling higher current density package-interconnect applications.

For many metallic nanoparticles, e.g., Cu, Sn, In, Bi, Ga, Au, their melting points decrease with particle size.[63] This behavior is attributed to increasing surface to volume ratios and the emerging significance of surface energy. For example, five nanometer diameter gold nanoparticles are observed to melt at <150°C.[64] These low-melting point metal nanoparticles could be useful for low-temperature interconnect and packaging assemblies, forming relatively soft, compliant interconnects and contacts; however, their current-carrying capability, electromigration resistance, and scalability remain to be understood.

THERMAL INTERFACE MATERIALS

The intrinsic high thermal conductivity[65] of nanotubes justifies their consideration as potential candidates for thermal interface materials. The key challenges that must be overcome for this application to be viable are to achieve low thermal contact interface resistance and a high density of nanotubes that provide a direct thermal path between the heat source and the sink. Significant research is needed to understand the fundamental nature of thermal contact resistance and to validate emerging theoretical hypotheses, reported in the literature.[66] Macromolecules or self assembly techniques that could enable nanotubes to be integrated at high density in a polymer matrix, without degrading their thermal conductivity, are needed. Alternatively, recent experiments demonstrate that aligned nanotube arrays under pressure also exhibit decreased thermal contact resistance.[67]

PACKAGE POLYMER PROPERTIES

Package polymers need to have a coefficient of thermal expansion (CTE) of <16 ppm/K, controlled mechanical modulus, high toughness, and low moisture absorption. Several nanoparticles have properties that could aid in achieving low CTE, improved mechanical toughness, and reduced molecular diffusion.[68], [69] Unfortunately, these fillers also may increase the composite's modulus and reduce the polymer's flexibility. Significant improvements in several composite material properties, such as its modulus, CTE, and toughness, may be effected by the addition of certain nanoparticles to the polymeric formulation. The key challenge is to develop guiding principles to integrate multiple nanoparticle types in a polymer and achieve all of the required properties simultaneously.

Significant research is needed to develop guiding principles for designing and tailoring the nanoparticle-matrix interface; achieving the desired nanoparticle dispersion within the polymer matrix;[70] and developing an appropriate "rule of mixtures" for nano-composites. Since the nanoparticle-matrix interface appears to control a nanocomposite's properties, novel and appropriate chemistries are needed to optimize the design of a nanoparticle-matrix interface to obtain a specified combination of composite properties. Finally, empirical "rules of mixtures" exist for only a few nanocomposite systems, but global, predictive, "rule of mixture" guidelines for nanocomposites are needed to enable designed nanomaterials with optimized sets of specified properties.

MACROMOLECULES

Conventional macromolecules, in the form of polymers, enable a wide range of competitive applications in the semiconductor industry. New molecular architectures, including functional design, molecular glasses and novel molecules, such as dendrimers, may provide solutions to emerging material challenges. Macromolecular materials with new properties are needed for future lithography, devices, ultra low-κ interlevel dielectrics, and package applications. While new macromolecular techniques and macromolecular architectures may provide solution options, significant challenges must be overcome for these to be viable. The most significant challenge for all of the identified applications is to establish models that correlate macromolecular structure with the functional performance of material matrices in complex environments. Table ERM5 presents Macromolecules applications, potential values, and challenges.

Table ERM5 Potential Applications and Challenges for Macromolecules

APPLICATION	POTENTIAL VALUE	KEY CHALLENGES
Resist	Extend lithography	Ability to simultaneously achieve (resolution, sensitivity and line edge roughness) Compatibility with immersion fluids
High refractive index immersion fluids	Extend 193nm immersion lithography	Refractive index of >1.8 Low absorption at 193 nm
Imprint lithography	New lithography technique	Low viscosity Fast expose and cure Dimensional stability
Molecular Devices	High density beyond CMOS Device	Low contact barrier for transport Repeatability of switching mechanisms
Low-κ ILD	Enable high speed electrical interconnects	High mechanical strength Low water absorption Low process integration complexity
Selective Etch and Cleans	Improved process stability	Identifying a material that can attach to a specific material, protect against etch or cleans, and then be easily removed
Package Polymer Adhesion	Improved package reliability	Low viscosity in application Increased adhesion to heterogeneous materials including Cu, silica, etc. after cure
Package polymer properties	Improved mechanical properties, reduced moisture absorption	Controlled CTE, modulus and toughness Low electrical loss Low moisture absorption and transport
Nanomaterial Functionalization	Reliable integration of nanomaterials	Good nanomaterial to polymer adhesion No degradation of nanomaterial properties (e.g., thermal conductivity)

MACROMOLECULES IN LITHOGRAPHY

The biggest challenge for resist is to simultaneously achieve the required resolution, speed, line edge roughness, and stability during the patterning process. As highlighted in the Lithography chapter, resists with the ability to pattern increasingly small features are required for future technology generations, whether with 193 nm, 193nm immersion, EUV, or imprint technologies. Also, higher refractive index liquids are needed to extend immersion lithography. New macromolecular architectures and designs exhibit the potential to enable improved control of resist feature sizes and properties. It is important to develop the correlations between molecular structure and functional performance that will enable materials fabrication methods that simultaneously satisfy all required properties.

The dynamic nature of today's lithography environment requires continued research focus on chemistry and functional materials. Given the broad array of future lithographic options under consideration, strategic patterning materials research warrants organization along common themes, such as immersion, resist, and imprint materials. This section highlights several critical issues and discusses potential research pathways for enabling future patterning related materials.

MACROMOLECULES FOR IMMERSION LITHOGRAPHY

The Lithography chapter notes significant effort on extending water-based 193 nm immersion lithography through the creative incorporation of enabling materials and processes. The interaction of water with 193 nm photoresists creates a new set of immersion-specific defectivity mechanisms.[71] Initial immersion resist processes used functional fluoropolymer topcoats to protect tools from resist component leaching and for defect reduction.[72] While the topcoat provides barrier properties to a limited extent, water still is able to penetrate into the resist; however, the amount of extracted photoacid generator is greatly reduced. Recent attention has been focused on two areas: 1) the need for improved resist surfaces for immersion lithography[73] and 2) simplified processes involving topcoat-free resists. Improved surfaces and simplified processes have been achieved through the development of a class of surface active resist additives that provide controlled hydrophobicity to 193 nm resist surfaces.[74] Ultimate extension of water immersion lithography involves the use of immersion resist materials and more complex processes in double patterning applications.

HIGHER INDEX IMMERSION FLUIDS AND RESISTS

One method for extending the resolution of immersion lithography is through the introduction of higher refractive index fluids and resists. For a more detailed description of this requirement, refer to the Lithography chapter. Several cycloalkanes show promise as "Generation 2" fluids, with an index of ca. 1.64 at 193 nm and acceptable transparency.[75] On the other hand, resists with refractive indices above 1.85 have remained elusive. While rational incorporation of sulfur into acrylic polymers increases the resist's refractive index,[76] resist optical density and imaging performance are not maintained. Getting all three, i.e. transparency, high refractive index, and imaging performance, with one material is a significant challenge that remains to be achieved. The sulfur-substituted polymers also have very high optical absorbance.

BEYOND IMMERSION (EUV)

EUV lithography remains a leading candidate to extend lithography beyond the 193 nm wavelength, as discussed in the Lithography chapter. The relatively low output of current EUV sources requires fast, high resolution resists for this wavelength that exhibit low line edge roughness (LER). In chemically amplified resist, changes in chemistry to enhance speed tend to degrade resolution and LER, while similar changes of chemistry to improve resolution tend to reduce speed and possibly LER. This triangular relationship of speed, resolution, and LER[77] identifies the competing factors that must be managed. A recent focus on molecular glass resists has been directed toward understanding the role of polymer architecture on LER. Merging low activation energy resist design,[78] with molecular glasses, has produced low temperature bake resists from non-polymeric macromolecules.[79] Recent modeling predicts that line edge roughness decreases with reduced molecular weight of the photoresist polymer, for classical and chemically amplified photoresists. The radius of gyration (RG) of a photoresist polymer also has been directly correlated to LER,[80] such that a smaller RG appears to yield a smaller LER. Recent work demonstrates that compared to a polymeric system, certain molecular glass resists will consistently have lower LER, due to their distribution of free volume in small packets that inhibits acid diffusion.[80] Based on this theoretical work, a new class of molecular resists based on polycarbocycles is being investigated.[81]

Single Component/Pixelated Resist Materials

The basic concept of a pixilated resist is that each molecule has complete functionality to absorb a photon, change solubility, and locally be "photoexposed," This contrasts with conventional resist, where a photoacid is generated diffuses in the resist, and catalytically modifies the solubility of other molecules. A single component resist, based on polymeric dehalogenation, was developed and investigated for e-beam lithography applications.[82] This resist shows reasonable resist sensitivity of 25 μCcm^{-2} and resolves 50 nm isolated lines. Photoacid generated (PAG)-bonded resists have demonstrated a LER of 3.5 nm for 75 nm line and space (L/S) features and resolved 55 nm lines and 25 nm spaces.[83] A natural extension to a single component resist is the development of molecular glass (MG) resists, with a photo acid generator [PAG] group attached.[84] This family of materials show excellent sensitivity, e.g. ~4mJcm^{-2}, and LER of 3.96 nm for 50 nm lines," during EUV exposure, and exhibits improved etch resistance compared to conventional resist. The modification of the sulfonium core with t-BOC-protected phenyl groups also helps to lower the outgassing relative to unsubstituted triphenylsulfonium salts. Though very low LER values are observed, PAG diffusion induced changes in feature sizes can be significant. Pixelated resist materials endeavor to combine structural disintegration, catalyst preorganization, as well as polarity changes.[85] Their current chemistry involves a scissionable pixilated resist architecture, based on bile acids bound by acid-sensitive tertiary ester linkages into dendrimeric arrays. Preliminary e-beam studies show submicron features for these materials. These materials were also tested for outgassing at the EUV wavelength and found to perform within the required specification. Initial results demonstrate the concept, but the benefits of pixilated resist options on resolution and LER have yet to be demonstrated. Single component chemically amplified resist approaches and materials demonstrate the potential of novel designs, but require further improvements to be viable for robust manufacturing processes.

Resists that undergo chain scission or photo-induced solubility changes have a greater potential to suppress line edge roughness because of the absence of catalytic mobility. These materials, non-chemically amplified resists (non-CAR), show improved line edge roughness, but materials based on chain scission process show higher resist outgassing. In addition, these materials require higher exposure energy to resolve sub micron features. Ideally, single component molecular glass resists that undergo photon induced chain scission or chemical changes should be potential materials for NGL. Molecular glass resists containing cleavable and cross-linkable functional groups have been demonstrated for e-beam lithography.[86] These resists resolved 70 nm lines upon exposure to e-beam radiation. Resist sensitivities for these materials were in the range of 3 to 3.5 μCcm^{-2}. Recently, a single component molecular glass resist, based on DNQ chemistry, has been demonstrated.[87] Exposure to electron-beam radiation, followed by flood exposure to 366 nm radiation, resulted in negative tone images as small as 60 nm. Currently, however, the energy required to resolve 60 nm lines is approximately 600 μC cm^{-2}. For these non-CAR molecular resists to be useful in high volume manufacturing, resist sensitivity must increase and outgassing issues must be resolved. However, non-CAR molecular glass resists, which combine the non-diffusive process and the benefit of a molecular glass, represent a potential pathway that warrants research consideration as an alternative to CARs. Patterning of surface attached polymer monolayers, i.e., polymer brushes is another approach to obtain high resolution features.[88]

Polymer Brushes

A combination of various patterning techniques (contact printing, scanning probe microscopy, photon or high energy radiation), a self-assembled monolayer (SAM) of initiators, and surface-initiated polymerization (SIP) allows for superior pattern formation control at various length scales, from several the hundred micrometer to nanometer scale.[88] (this reference is a duplicated and is correct) In one approach, a combination of styrene based e-beam, SAM, and SIP components results in 200 nm and 70 nm lines of patterned polystyrene brushes. In another approach, a combination of styrene based EUV-IL, SAM and SIP components results in 50 nm patterned polystyrene brushes.[89] SIP applies a significantly thicker layer of flexible polymer brush,[90] which reduces the effect of topological variations on the substrate surface and reduces defects present in all self assembled monolayer systems (SAM). The final resulting structures obtained from a combination of patterning techniques/SAM/SIP display a better contrast between the functionalized and unfunctionalized areas, in terms of their chemical and physical properties, e.g., interfacial roughness, wetting behavior, thermal stability, etch resistance. The wide variety of recently developed patterning techniques SAM/SIP systems enables the patterning of sub-micron and nanometer scale features with different surface structures and material contrast. Several areas need further understanding or improvements, including flexibility in the chemistry, process compatibility, fidelity, pattern roughness, and defects.

IMPRINT LITHOGRAPHY MATERIALS

Imprint lithography requires low viscosity materials that can be converted to nanometer scale features with reproducible shrinkage and good etch resistance without leaving residue on the imprint tool. Particular attention in these studies is focused on mechano-chemical properties of the resist during cure and the influence of the release chemistry. Work is underway to demonstrate the feasibility of functional patterning materials for back end low-κ applications, based on polystyrene sulfonate (PSS) crosslinkers[91] and vinyl ether polymerizations,[92] with satisfactory mechano-chemical release properties.

MOLECULAR STATE DEVICE MATERIALS

The greatest challenge for molecular state electronics is to fabricate low potential barrier electrical contacts that enable reproducible electronic molecular switching. Molecular state devices are reported to exhibit a range of useful properties, including non-linear IV and bi-stable behavior. While a given device's characteristics may be reproducible, significant device to device variations are observed, even when fabricated under "identical" conditions. The electrical performance of many molecular-based devices currently under study appears to be dominated by the high potential barriers of each molecule-electrode contact or defect-like processes. Recent results suggest that changes in molecule-contact conformations or near neighbor interactions may be responsible for observations of electrical switching or negative differential resistance (NDR).[93, 94, 95] In order to understand the complex behaviors of these macromolecular devices, well-designed collaborative experiments are needed that determine and validate the role of contact formation in molecular switching and identify potential contact formation strategies that enable molecular switching with less energetic electrons. Despite significant challenges and knowledge gaps, these emerging macromolecular systems show some promise for reducing device variability and enabling very high density circuit functionality.

MOLECULAR STATE CONTACTS

Understanding and engineering atomic level contacts is critical for molecular scale devices. For these systems, nanoscopic factors, such as bond formation and configuration significantly impact contact potential barriers[96], and metal molecule interactions[97] and variability occurring in deposition may dominate nanoscale device operation. Research is needed to understand the structure and properties of metal-molecule interactions. The nature of the metal-molecule orbital overlap will be important in determining the properties of their combined occupied states and available conduction pathways.

The fabrication techniques currently used for making the top electrode-molecule contact can effect defect-like reactions, such as bond breaking or undesired intra-device redox reactions. These undesired reactions can disrupt or mask molecular device switching behavior. Currently, many nanoscopic bottom contacts are fabricated on Au, with a thiol sulfur bond, linkage to the molecule. While this contact exhibits significant mechanical strength, it may not be optimal for expressing optimal electrical contact behavior. Also, many reported molecular contacts appear to allow for molecular movement and conformational changes about the molecule-electrode bond.[97] In order to minimize the contribution of contact variability on observed molecular device properties, the designed molecule-electrode docking geometry must lock in a specific conformation. Recent results show that molecule-electrode assemblies on Si need not use a thiol linkage. New molecule-electrode material systems are needed that enable stable, reproducible low potential barrier contacts.

For good mechanical or electrical contacts to be established with a low potential barrier[96] significant orbital overlap between the molecule and the electrode is needed. Sigma type bonding tends to enhance the mechanical strength of the molecule-electrode bond, and this will likely result from end-on bonding with s, sp, sp^2, or sp^3 type molecular orbitals. Conversely, to form low barrier electrical contacts, in-plane π-like bonding, such as p-p or p-d, appears to be a prerequisite for low energy and low bandgap contacts. In-plane π bonding typically forms from p orbitals, found in some sp and sp^2 hybridized molecular structures. Good electrical contact is expected through in-plane bent "banana" bond type conjugation, observed for back-bonded overlap with two lobes of a d orbital. Recent work with molecular contacts demonstrates that the orientation of a molecule's orbitals, with respect to those of the contact atom to which it bonds, can change significantly the operation of a molecular device. Consequently, atomic level control of bonding and hybridization may be needed at this interface. In summary, in-plane orbital alignment is critical for low barrier interfaces and molecular scale devices. Contact formation issues and metrology needs are discussed in more detail in later sections.

TRANSPORT AND IV NON-LINEARITY

As mentioned above, contact resistance and tunneling can dominate the transport properties of molecular wires. Other mechanisms, such as polaron state carrier trapping, also may impact charge transport, even for delocalized molecules with extended conjugation, such as polyethylenes with more that twenty carbon atoms. While individual IV characteristics may be reproducible over millions of cycles, sample to sample onset voltage variations can be significant. Recent results demonstrate that these variations can be due to contact metal and contact bonding hybridization. Since IV characteristics are driven by the lowest resistance mechanisms, nanoscale devices are extremely sensitive to undesired nonuniformities, such as defects, high electric field excursions, and local contact architecture. Currently, Scanning Tunnel Microscopy (STM) and Conductance Force Microscopy [CFM] serve as the primary tools for characterizing variability, molecule-electrode interfaces, and nonlinear tunneling, rectification, and transport through individual or groups of molecules and contacts. These methods enable the characterization of transport variations over dimensionally appropriate regions.[93] Research is needed to understand the role of the contact potential barrier and potential molecule-contact interactions in transport and IV nonlinearities. Furthermore, contacts with lower potential barriers may allow evaluation of electronic transport, nonlinearities, and potential changes in molecular states.

BI-STABLE STATES

Though low variability bi-stable molecular systems have yet to be demonstrated, they show some promise for memory or logic device applications. Recent results suggest that local conformational changes in the molecule or electrode environment,[97] metal migration, telegraph switching,[94, 95] or other extrinsic factors, such as transient fields, may control molecular bistability and NDR.

Again, a non destructive, *in situ*, 3D test suite needs to be developed that enables a more fundamental understanding of the factors that control bistability and the primary charge management and decay mechanisms.

METROLOGY

Currently, it is difficult to look through the top contact into the geometry and electronic structure of a molecular device. Collaboration is needed between the metrology, molecular modeling, and synthesis communities to design material systems with required properties. New metrology capabilities such as inelastic electron tunneling spectroscopy and backside FTIR to study vibrational states, STM, Conductive AFM, and Kelvin Probe AFM are beginning to enable understanding of the transport through individual molecules and interfaces. However, additional research is needed to develop new metrologies, such as nondestructive, *in situ*, 3D methods, to resolve these issues.

MACROMOLECULES FOR LOW-κ ILD

As described in the Interconnect chapter, the most difficult challenges for ultra low-κ interlevel dielectrics (ILD) are to simultaneously have a dielectric constant <2.0, good adhesion and mechanical properties (e.g. modulus and toughness), no moisture absorption, and compatibility with interconnect processing, such as CMP, etch, plasma O_2, etc.

As identified in the interconnect chapter, macromolecular low-κ ILDs have employed pores to achieve the required dielectric constant. However, their mechanical properties, integration issues and process compatibility, and moisture absorption have limited their adoption in manufacturing. Due to these challenges, alternative macromolecular designs should be investigated that have the potential to overcome these issues.

POTENTIAL SOLUTIONS

Silicon –carbon covalent bonds are strong nonpolar bonds that are not prone to environmental degradation and, thus, may be candidates for new ultra low-κ (ULK) ILD materials. Unlike silicon-oxygen bonds, which are also strong, but are prone to attack by nucleophiles, acids, bases, etc, the SiC bond is not readily attacked by chemical reagents. One approach for improving chemical compatibility and mechanical strength is the introduction of silicon-carbon covalent network bonds into low-κ dielectrics. The presence of a network of strong bonds should result in improved mechanical properties (modulus, cohesive energy, fracture toughness) for both dense and porous samples. Oxycarbosilane- based ultra low-κ materials have exceptional mechanical properties[98] compared to solution deposited polymethylsilsesquioxane based low-κ materials and chemical vapor deposition (CVD) deposited carbon doped oxide (CDO) materials of comparable densities. Excellent process chemical compatibility of this new polyorganocarbosilane ULK material has been demonstrated as well. Likewise nanocrystalline pure silicon zeolite materials deposited by spin-on processes have been demonstrated with and without porogen to produce ULK dielectrics with elastic moduli > 14GPa.[99, 100] Processing and control of surface roughness and hydrophobicity remains a challenge for back end integration and little integration data has been reported. New classes of materials, with chemical backbones that differ from the organosilicates, also have been proposed as low-κ dielectrics. For example, Borazine derivatives,[101] which are comprised of ring structures containing boron and nitrogen double bonds, display a κ value of 2.3 and an elastic modulus of 60 GPa. Properties of CVD and spin-on[102] variants of these materials also are reported. Since this represents a totally new family of chemical backbone, simultaneous process technology development (including etching, polishing, etc.) will be needed for these materials. Computer aided chemistry and modeling predict that new low- κ materials, with κ values of 1.5,[103] can be achieved without the introduction of porosity, but new synthetic routes to such materials are needed.

MACROMOLECULES FOR PACKAGE APPLICATIONS

For packaging polymers, macromolecules are needed to improve the adhesion of a wide range of materials, including nanoparticles; improve required mechanical properties, such as CTE, toughness, modulus, flow; reduce moisture absorption and diffusion; and meet cost requirements.

As is highlighted in the Assembly and Packaging chapter Material Challenges table, polymers are needed with a range of properties, such as mechanical, adhesion, electrical, moisture absorption and transport, depending on the application to support future package requirements. Polymers are used in a wide range of package applications, with most being thermosets because they retain their dimensional stability. These polymers include epoxies and silicones.[104] Epoxies are used for under-fills, mold compounds, substrate build-up layers, and die attach adhesives. Silicones usually serve as compliant adhesives physically attach materials with dissimilar coefficients of thermal expansion and mechanical properties, such as attaching metals to polymers or metals to ceramics. As packages increase in complexity and as multiple components are integrated into the package, the epoxies and silicones need reduced viscosity during application; improved mechanical properties, e.g., modulus, toughness, etc.; increased adhesion to various heterogeneous materials; and reduced moisture absorption and diffusion and enhanced dimensional stability. Novel macromolecules may provide potential solutions to overcome this challenge of achieving multifunctional properties simultaneously in future package polymers.

Epoxy systems must satisfy a set of pre-cure requirements, including low viscosity, and the ability to wet different materials. They also must exhibit specific cure properties, such as mechanical properties (CTE ~16 ppm; modulus, toughness, etc.); electrical properties (κ and loss); adhesion to a set of materials (metals, polymers, ceramics); moisture absorption, and diffusion after cure. Since each application in the Assembly and Packaging chapter has a different set of requirements, macromolecules that could improve viscosity and wet package and chip materials, while achieving high ultimate toughness post cure, would be valuable. Adhesion to copper is of critical importance, since in many cases, the copper must be roughened to achieve adhesion, which increases electrical loss at high frequency. Consequently, macromolecules that increase polymer adhesion to smooth copper would be important. Adhesion to silicon or other ceramic materials integrated in a future package would also be very important. Delamination of the polymer from the silicon or a ceramic would increase stress on the ceramic. This likely would induce cracking during thermal cycling in operation or reliability tests, since there would be no epoxy-polymer to help dissipate the stress. Moisture is known to be particularly detrimental to the performance of under-fill epoxies. Because of moisture diffusion and absorption, the dangling bonds at the corner fillet crack tip get saturated, causing catastrophic fillet cracking of underfills.[105] For MEMS packages, hermetic sealing of the MEMS device is required. Otherwise, the moisture diffusion can cause corrosion of the fine metal lines. Since packages must function in humid environments, macromolecular additives that reduce moisture absorption or diffusion would be valuable. Since novel nanometer size fillers may be added to epoxies to reduce CTE, macromolecules that could improve integration (dispersion) and adhesion of the nanoparticles within the matrix without degrading their properties while increasing toughness are needed.

Research is needed to understand correlations between the structures of designed macromolecular additives and cross linked polymer systems and designed sets of desired properties, including thermomechanical, adhesion, electrical loss, viscosity, and thermal stability attributes.

Silicone-based resins or composites are used as adhesives, sealants, and thermal interface materials. Their critical properties include low-moisture absorption; high adhesion with heterogeneous materials; good compliancy to allow for package expansion, and contraction during assembly, reliability tests, and operation. For thermal interface applications, the required thermal conductivity typically is achieved by the addition of thermally conducting fillers, such as aluminum, phase change materials, etc. Guiding principles are needed to design macromolecules that enable the integration of dense nanotube arrays, without introducing defects and degrading thermal conductivity. In a separate study, aligned individual polymeric chains have been observed to exhibit higher thermal conductivity than bulk polymers. In fact, gyration effects, which dampen phonon vibrations, appears to contribute to poor thermal conductivity of bulk polymers.[106, 107] In order to realize single macromolecules that exhibit an interdependent set of required attributes, predictive material design methods must be developed that leverage emerging metrology, material database, and modeling capabilities

Interface control is critical to achieving improved mechanical properties,[108] such as viscosity, toughness, modulus, adhesion, and thermal conductivity. Higher interface adhesion implies higher toughness, due to a more efficient load transfer to fillers. Another aspect that indirectly controls nanocomposite properties is filler dispersion. Because of high surface areas, nanofillers typically tend to segregate in a given matrix. Segregated fillers reduce the effective surface area, and also make resin infiltration difficult. Thus, filler segregation gives rise to potential voids which could be on the order of the crack lengths, thereby drastically lowering the fracture toughness of the composites. Thus, macromolecules are needed for nanocomposites to provide a robust filler-matrix interface, and improve interfacial properties, and filler dispersion.

DIRECTED SELF ASSEMBLY

Self assembly is a natural process driven by intermolecular repulsion that can deposit a monolayer of aligned molecules on surfaces in processes such as atomic layer deposition [ALD], or cause phase separation into locally ordered structures in block copolymers. It also exhibits potential for generating lithographic features, such as contacts or lines, in block co-polymers. Research has demonstrated the ability of top down lithographically generated features to force alignment of self-assembled patterns in desired locations with predicted shapes. Furthermore, these techniques enable registration of the self-assembled structures to the lithographically generated pattern. Annealing times, which are thermodynamically driven, have been reduced from multiple days to hours, so this option is becoming more realistic for potential processing applications. Self-assembled structures have been generated with <15 nm dimensions and the ability to generate sub-10 nm structures may be possible.

While self assembly has made considerable progress, it faces significant challenges before it can become a viable lithographic extension option; however, other less challenging, nearer term applications may be able to benefit from these capabilities. Directed self assembly shows some potential for enhancing etch selectivity, placing dopants in ordered arrays, or to generating high density close packed electrodes in capacitor arrays. The requirements for these applications are less complex and less severe than those for lithography extension applications. This section will review the potential and challenges for different applications. Refer to Table ERM6.

Table ERM6 Potential Applications and Challenges for Self Assembly

APPLICATION	POTENTIAL VALUE	KEY CHALLENGES
Lithography Extension	Higher density features than lithography Reduced line edge roughness	Ability to generate required features at 2× lithographic density Ability to align features to previous structures Ability to achieve low defect density Reducing process complexity Etch selectivity
High Charge Density Capacitors	Assembly of close packed electrodes separated by dielectric	Electrically connecting adjacent electrodes to opposite polarity contacts at low cost Achieving high dielectric constant for thin dielectrics
Selective Etch	Ability to selectively protect materials during etch or cleaning operations	Ability to design polymer brushes to selectively coat and protect new materials against chemical etches
Deterministic Doping	Reduced variation in transistor performance	Ability to pattern dopant array with periodicity required for device operation Mechanism to reproducibly introduce dopant from self assembled material into transistor structures
Directed Assembly of Low Dimensional Materials	Robust and affordable pattern placement and matching capability, with low dimensional variability	Accurate placement of nanomaterials Achieving required throughput Achieving the required yield

DIRECTED SELF ASSEMBLY FOR EXTENDING LITHOGRAPHIC TECHNOLOGIES

The biggest challenge for directed self assembly (DSA) as an extensible patterning option is to be able to assemble a desired set of structures with 2× lithographic resolution in predefined locations with respect to existing structures with low defect density (Refer to Figure ERM1.). More information is provided for DSA at this link. Polymer self-assembly can easily define a limited set of highly symmetric patterns. Even such simple patterns as line/space (L/S) and cylindrical hole arrays may be useful in defining circuit elements, but they must be positioned accurately with respect to previous lithography levels. To be competitive, self-assembly must demonstrate the formation of features that are at least twice as small and twice as dense as can be achieved by top down lithographic methods. This corresponds to resolution, LWR, and LER targets of <12 nm, <1.3 nm, and < 1.7 nm, respectively. The net time required to form and fix a pattern must be short, less than 4 minutes, and compatible with processing one hundred twenty 300 mm wafers/hour. No current material satisfies all of these requirements. Defect densities represent a significant research challenge, as the best results observed to date are orders of magnitude larger than the requirement of <.01/cm^2. The ability to achieve controlled alignment and registration, while minimizing defects and line roughness, are critical barriers to inserting self assembly as a potentially competitive lithography solution.

Directed self assembly is a hybrid top-down/bottom-up approach for achieving positioning accuracy and dimensional control. The two leading methods are to either generate a trench to confine self assembly, topological alignment, or chemically pattern neutral and selective regions, chemical patterning and alignment, will be discussed below.

SURFACE PROPERTIES FOR PATTERN GENERATION

For lithographic feature generation, the wafer surface must enable lateral phase separation, the surface must be neutral and not have preferential adhesion to one part of the molecule or block co-polymer. Lithographically generating these “neutral” regions enables pattern formation to occur in predefined locations. Demonstrated substrate modification approaches for generating neutral regions include exposure to radiation (such as X-rays) or reactive species (oxygen plasma, HF, etc.); binding specific molecules (self-assembled monolayers of octadecyltrichlorosilane) to the surface; or coating with a designed polymer, such as a random copolymer or random copolymer brush. Requirements for a useful neutral interface layer include ease of application, effectiveness as a very thin layer, insignificant etch resistance or removable by the process that removes the developable block.

TOPOGRAPHIC ALIGNMENT

For topographically induced ordering, or "graphoepitaxy," lithographically-defined topographic features and boundaries direct the ordering of a self-assembled block copolymer film. The self-assembled patterns self register to the lithographically defined pattern and subdivide into features with sublithographic resolution. Patterns of spherical and both parallel- and perpendicularly-oriented cylindrical features have been studied. Perpendicularly-oriented lamellar patterns are more difficult to self-align, although a few examples are reported.[109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124]

The number of features *n*, fitting within each lithographically defined groove is determined by commensurability between the lithographic width, *w,* and the intrinsic polymer period, L_0. Defect-free polymer patterns form when the lithographic width satisfies the condition $w{\sim}nL_0$. For example, striped cylindrical patterns of polystyrene-*b*-poly (ethylene-*alt*-propylene) (PS-*b*-PEP)[123] or PS-b-PMMA exhibit a single-valued number of stripes within each channel for widths as wide as $9L_o$, ~300 nm. For wider lithographic trench width, $>9L_0$, dislocation defects generate multi-valued numbers of stripes within a given channel.[121, 122] Defect levels, spacing distributions, and line straightness are strongly sensitive to small deviations from commensurability. Lines also tend to reproduce and track defects in the lithographically defined wall. A key challenge for high resolution patterning is to develop systems that are tolerant to small variations in the lithographically patterned trench width.[121, 122, 124]

These self assembled block copolymeric systems exhibit placement errors that depend upon template edge roughness and polymer domain non-uniformity. Registration accuracy is dictated by phase-separation thermodynamics, composition, and polydispersity effects.[120] The projected requirement of 1.4 nm registration accuracy for 16 nm half pitch corresponds to a spacing accuracy of .04 L_0, the intrinsic polymer period. This is considerably smaller than typical domain size/spacing distributions of 3σ ~0.09–$0.3L_0$ for sphere or cylinder-forming patterns.[125] The formation of lamellar structures currently requires a planarization step, as pattern formation is particularly sensitive to film thickness. Research is needed to develop less sensitive material systems or methods that maintain constant film thickness over substrate topography.

CHEMICAL PATTERNING AND ALIGNMENT

Directed block copolymer assembly on lithographically defined chemically nanopatterned substrates offers another potential route for aligning and registering patterns.[126] In this process, a molecular monolayer, e.g., a self-assembled monolayer or polymer brush, is deposited on a substrate, lithographically patterned, and oxygen plasma etched to define regions with distinct chemistry and surface energy. Subsequently, the surface modified substrate is coated with a thin block copolymer film and thermally annealed. During the anneal process, preferential wetting drives each block to migrate towards chemically compatible surface regions that minimize the film's free energy. Final useful patterns reflect equilibrium morphologies at lithographic dimensions. Improved CD control and LER at nanoscale dimensions are key drivers for this directed self-assembly approach.

An example of this pattering approach is the formation of periodic arrays of lines by lamellae-forming block co-polymer films on chemically patterned surfaces. The lamellae, with a bulk period of L_o, can assemble perpendicular to the substrate and align with the axis of the underlying chemical surface pattern, if the period of the surface pattern, L_s, is commensurate with L_o. When $L_s = L_o$, the block copolymer film assembled patterns will be defect free, if the corresponding chemically defined surface pattern also is free of defects.[127] Wafer scale statistics may be required to decouple surface patterning related defects from other factors, such as contaminants. Furthermore, each block copolymer domain aligns with the underlying chemical surface pattern, implying registration and overlay are determined by the lithographic tool capability. If interfacial interactions between the chemical pattern and the polymer film are strong, then the same polymer can create equal line and space patterns, with a variation of $L_s = L_o \pm {\sim}10\%$ (for example, 21 nm–26 nm period for $L_o = {\sim}24$ nm).[128, 129] Over this range, the polymer also appears to exhibit some self healing behavior. Such films can correct for line width variations in the chemical surface pattern and maintain the copolymer pattern CD equal to 0.5 Ls.[130] Block copolymer domains can be directed into many of the essential features required for manufacturing integrated circuits with regular fabric architectures, including dense and isolated bends, jogs, spots, line terminations, and T-junctions,[126, 131] as shown in Figure ERM1 below.

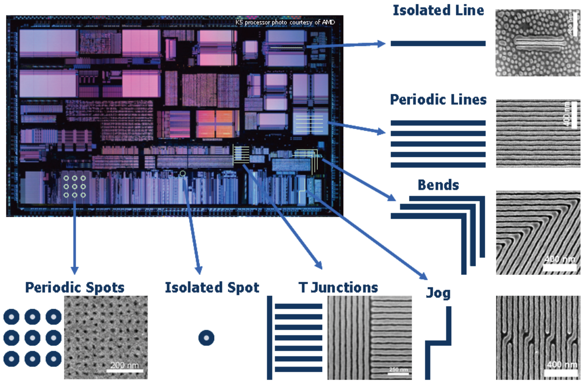

Figure ERM1 Current State-of-the-Art of Self-assembled Shapes required by the Design Community

A particular challenge for chemically directed self assembly is demonstrating subdivision of the chemical pattern into desired features with sub-lithographic resolution. Thus far, only 1-to-1 reproductions of the chemically modified surface patterns have been reported. This approach depends upon a multi-step process to produce the local alterations of the neutral layer's chemical properties. Research is needed on materials and methods that would enable direct lithographically induced spatial variation in surface chemistry and functionalization in one step.

APPLICATIONS WHERE RANDOM PATTERNS ARE USABLE

Some applications do not require pattern registration to underlying features. The easiest are those that require only an array of similar sized holes, which can be created from spherical or cylindrical phase separation. Examples include capacitors, nanocrystals for flash memory, air gap masks, and low refractive index cladding for optical waveguides.[126, 132] The primary challenges are the ability to make uniform sized features with adequate etch selectivity. Though patterns of spherical domains are the easiest to form, they place exceptional requirements on the etch selectivity of the two phases.

In extremely scaled CMOS, the trend in the number of channel electrons suggests that by the year 2014 there may be less than one hundred active dopants in the channel region.[133] This low number of dopants in the channel may emerge as a critical performance and yield limiter. (A more detailed discussion on the number of dopants in the channel can be found in the supplemental document.)

Under this scenario, device engineers no longer can assume that large numbers of dopants are stochastically and uniformly distributed in the channel. Recent results show that in this regime, small differences in the number and positions of the dopants impact device to device performance and variability. These results suggest that deterministic doping, which would enable precise control of the numbers and positions of channel dopants, could provide several orders of magnitude improvements in device to device variability.[134]

It is debatable whether fully depleted devices avoid the deterministic patterning challenge; however, their performance also remains susceptible to subtle variations in device structure. Figure ERM2a defines the natural dopant wavefront at the source-channel and channel-drain interfaces. Within this region, the dopant concentration is ~10^{18}cm^{-3}, which no longer is high enough to provide a uniform field for the carriers. At the natural dopant wavefront, transiting carriers experience localized point charges, approximately three to six nanometers apart, extending into the channel region like random arrays of atomic lightening rods, as shown in Figure ERM2b.[135] (More detailed discussion on the natural dopant wavefront can be found in the supplemental document.)

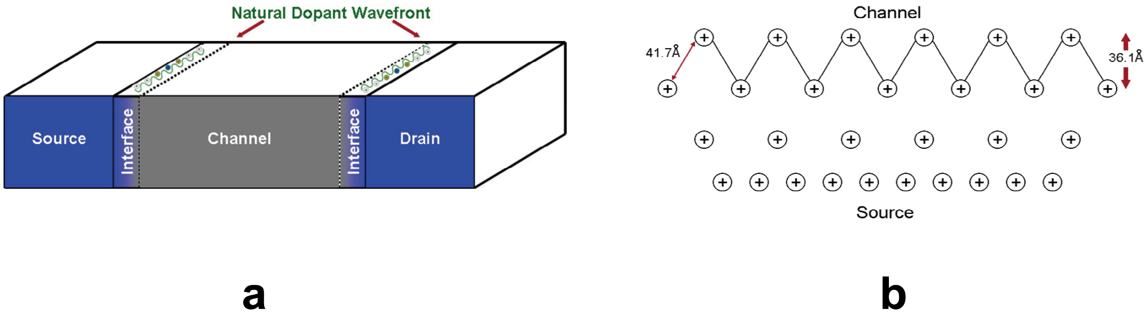

Figure ERM2 Schematics of the natural dopant wavefront: a. Macroscopic perspective and b. a 2D atomic scale perspective

Local random variations within the natural dopant wavefront will induce uncontrolled scattering of carriers entering and exiting the channel. This scattering will induce variations in the spread of carrier transit times within a given device. Additionally, this dopant roughness at either edge of the channel will present to the carriers local variations in the effective channel length. A three to six nanometer dopant roughness at either edge of the channel implies that carriers will experience net intra-device variations in local effective gate lengths of six to twelve nanometers. The magnitude of this dopant roughness may exceed projected ITRS MPU physical gate lengths by the end of the next decade[136] unless the challenge of controlling the structure of this natural dopant wavefront is resolved. Recent studies suggest that inter-device variability also may be exacerbated by the concurrent scaling of device line widths.[137] These emerging sources of variability suggest a need for a deterministic patterning option in extremely scaled CMOS devices. Considerable research is needed to develop materials and fabrication methods that would enable deterministic doping to warrant consideration as a potential solution for extending extremely scaled CMOS technology and to control doping of nanowires for novel applications.

DIRECTED SELF ASSEMBLY OF LOW DIMENSIONAL NANOMATERIALS

DIRECTED ASSEMBLY OF NANOMATERIAL, INCLUDING NANOTUBES

Whether used for device, interconnect, or in packaging applications, useful nanomaterials must assembled in predefined locations, orientations, and morphologies, with low thermal or electrical resistance. Several strategies for achieving these goals are under consideration and include 1) patterning the surface with a chemical that selectively inhibits or promotes the bonding of the nanomaterial in the patterned areas, 2) chemically treating the nanomaterial surface to selectively bond to specific surfaces to enable selective bonding in predefined locations and orientations. Chemicals used to promote assembly must be removed from or integrated into the final component structure. Substrate specific strategies may be employed to selectively place and align the nanomaterials in desired conformations. For example, hydrophobic and hydrophilic surfaces, respectively, prevent and promote the adhesion of carbon nanotubes to SiO_2.[138] Amine terminated nanotubes selectively bind to oxidized metal areas on the surface. Additionally, surfactant treated nanotubes will not adhere to untreated areas of the surface. However, methyl terminated phosphonic acid prevents nanotube adhesion and eliminates the need for a surfactant. Such layers can be patterned with conventional lithographic or imprint processes.[139] Alternatively, nanotube surfaces functionalized with acidic groups, such as phosphonic or hydroxamic acid, can selectively deposit on a metal oxide surfaces, but not to acidic surfaces, such as SiO_2. The original nanotube functionality can restored, after a 600 C anneal in N_2. Recent results suggest the feasibility of larger scale integration.[140, 141] While progress is being made, this approach requires considerable improvement before it warrants consideration as a potential solution to fabricate nanotube based devices.

SELECTIVE ETCH, CLEAN OR DEPOSITION

With the wide range of new materials potentially being integrated into future technologies, there are significant needs for materials that enable selective and customized etching, cleaning or material deposition. Either macromolecules or self assembly processes that can enable coating of a specific material in the presence of other chemical processes, such as etching or chemical mechanical polishing could improve process selectivity and yield. Similarly, as feature sizes are reduced, cleaning processes will need to be more selective in removing particles without disturbing the desired structures. Thus, there are opportunities for macromolecules and self assembled materials to enable the enhanced selectivity of future manufacturing processes.

SPIN MATERIALS

Electron spin orientation, like its charge, can be used to represent information. The ERD chapter describes the spin-based devices and their challenges. This section describes spintronics materials, their critical properties, and the issues of preparation that are important for realizing the spin-based devices. In order to realize spin-based logic devices one needs to control (1) equilibrium spin properties (such as tunneling magneto resistance (TMR)) or (2) induced (out of equilibrium) spin polarization and magnetization. For the class "2" devices using induced (non-equilibrium) polarization to become practical, there is an urgent need to develop spin-based materials and structures and to characterize and understand their critical properties. It is necessary to have materials with properties that enable spin injection, spin coherent transport, spin manipulation via field effects (e.g., external fields, magnetic or electric or by current), and operate above room temperature, Curie temperature >350 K. The spin-based materials along with their critical properties and challenges are covered as illustrated in Table ERM7.

The development of spin-based devices will require an understanding of spin-based phenomena, especially in the nanometer scale structures. There are also metrology needs for spintronics materials. However, unlike the measurement of electron charge, single spin reading and writing is still in its infancy.[142] This section covers important spintronic materials and their properties, summarizes some of the significant results, and provides insight to the research directions needed for development of spintronics materials.

SPIN MATERIAL CHALLENGES

The key challenges for spintronic materials to meet device needs are 1) magnetic semiconductor materials with T_C (Curie temperature) >350 K with carrier mediated spin exchange; 2) semiconductor materials with long spin coherence time; 3) material properties and tailored interfaces to enable effective spin injection from magnetic materials to semiconductors; 4) compatibility with CMOS processing, and 5) have interfaces with low spin decoherence. In addition, the synthesis must produce materials with consistent properties. It is critical to understand the mechanisms and physical principles that control these properties. The methods for characterizing critical attributes at the nanometer scale, including structural, temporal magnetic, electrical, and optical properties need to be assessed for their accuracy and reproducibility.

SPIN FUNCTIONS AND MATERIAL PROPERTIES

The set of critical properties for different spintronics materials will depend on the specific device applications, as discussed in ERD. (See Table ERM7.) The following properties will be described along with the challenges for each material:

- Ferromagnetic transition temperature (T_C)
    - Dilute magnetic semiconductor Tc (ability to achieve T_C>350K)
    - Size dependence of T_C
    - Wide bandgap magnetic doped oxides and nitrides
- Spin decoherence time
    - Semiconductors
    - Tunnel barrier materials
- Spin Injection efficiency
- Electric field coupling to spin
    - Rashba effect
    - Spin torque
    - Spin dynamics
    - Spin Hall effect
- Spin amplification or gain
    - Properties TBD

(For more information on materials and T_C refer to the supplemental file).

Table ERM7 Critical Properties of Spintronics Materials

Emerging spin based materials	*Material Examples*	*Mechanism to read computational state*	*Critical Properties*	*Challenges*
Ferromagnetic metals	Co, Ni, Fe	Spin injection/extraction	Spin polarization and band symmetry	Interface stability, Schottky barrier control
Half Metals	Fe_3O_4, CrO_2 Heusler–LSMO Mixed mangantites NiMnSb	Spin polarization	Interface properties and spin band symmetry,	Stoichiometry control Method of characterization Reproducible material fabrication
Multiferroic materials	$BiFeO_3$ PZT/$NiFe_2O_4$ $CoFe_2O_4$/$BaTiO_3$ PZT/Terfenol-D	Voltage Magnetic field	Magnetic and electrical coupling coefficients	High electric and magnetic coupling
(Diluted) Magnetic Semiconductors (Collective ferromagnetic spin orientation	Ferromagnetic semiconductors EuO DMS (II,Mn)/VI (III,Mn)/V DMS IV,Mn Silicides	Electrical, control of spin alignment	T_C, Carrier control of ferromagnetism Spin orbit coupling (as manifest in spin lifetimes, and diffusion lengths) g-Factor** Coercivity	Achieving Curie temperature above room temperature Structural homogeneity
Semiconductors	GaAs, etc. Nanotubes Nanowires, etc.	Spin transport	Spin decoherence time	
Dielectric Barrier	MgO	Spin transport or spin selective filter	Spin band symmetry	Control of interfacial properties

*** The g-Factor relates the total magnetic moment to the electron spin angular momentum and the Bohr magneton.*

FERROMAGNETIC TRANSITION METALS/ALLOYS AND HALF METALS

Metallic ferromagnetic materials are important for spintronics device applications, as sources of spin polarized electrons. To overcome the conductivity mismatch between the metal and the semiconductor, the spin polarized electrons are injected through either a modified Schottky barrier or a tunnel dielectric into a semiconductor material. The most important properties of these materials are that they have a very high electron spin polarization and a spin state band symmetry that is close to that of the tunnel and semiconductor materials. Both ferromagnetic metals and alloys, such as Fe, CoFe, and half metals like CrO_2, Fe_3O_4,[143, 144] are considered for this application.

The principal difficulty of spin injection into a semiconductor from a ferromagnet is that the materials in FM-semiconductor junctions usually have very different electron affinities and, therefore, high Schottky barriers form at the interface.[145] Thus, in GaAs and Si, a barrier height of $\Delta \approx 0.5$–0.8 eV is formed with practically all metals, including Fe, Ni, and Co [145, 146] and the barrier width (d) is large, $d \geq 100$ nm for doping concentrations $N_d \leq 10^{17} cm^{-3}$. The spin-injection corresponds to a reverse current in the Schottky contact, which is saturated and usually negligible due to such large d and barrier height Δ.[145, 147] Therefore, a thin heavily doped n-layer between FM metal and the semiconductor is used to increase the reverse current, determining the spin-injection in lattice-matched systems like Fe/GaAs.[147, 148, 149] This layer sharply reduces the thickness of the barrier and increases its tunneling probability. Injection is shown to be quite efficient and there appears to be a path to electrically controlled devices that can potentially work at room temperature.[150]

When using an insulating tunneling barrier, similar to that used in the tunneling magneto resistance, the band symmetry of crystalline MgO on Fe, on the [001] crystal surface, of tunneling states is such that the minority spin tunneling may be totally suppressed, leading to very large tunneling magneto resistance (TMR).[151] While large TMR is observed through MgO, the calculations predict the TMR to be several orders of magnitude larger than is observed. Temporal response of the magnetic tunnel materials is of great importance for switching applications, and has been measured in a metal insulator metal (MIM) tunneling junction to be less than 500ps. using X-ray magnetic circular dichroism (XMCD) effect with a resolution of sub 200ps.[152]

MULTIFERROICS

Multiferroic materials may offer potential spintronic devices the ability to control spin via optical, magnetic, and electrical methods. Materials that have coupled electric, magnetic, and structural order parameters that result in simultaneous ferroelectricity, ferromagnetism, and ferroelasticity are known as multiferroics.[153] These compounds present opportunities for potential applications for information storage and logic devices; however, the understanding of ferroelectricity remains limited, especially when the vertical and lateral dimensions decrease to small dimensions in thin films. For example, structural analysis of $BiFeO_3$ indicates that the crystal structure of the film is monoclinic in contrast to the bulk, which is rhombohedral. The films display a room-temperature spontaneous polarization (50-60 $\mu C\ cm^{-2}$) almost an order of magnitude higher than that of the bulk (6.1 $\mu C\ cm^{-2}$). The observed enhancement is corroborated by first-principles calculations and found to originate from a high sensitivity of the polarization to small changes of lattice parameters, due to lattice mismatch. The films also exhibit enhanced thickness-dependent magnetism compared with the bulk. These enhanced and combined functional responses in the thin film form present an opportunity to create and implement thin film devices that actively couple the magnetic and ferroelectric order parameters.[154]

The first observation of electrical control of antiferromagnetic domain structure in a single-phase multiferroic material at room temperature has been demonstrated.[155] High-resolution images of both antiferromagnetic and ferroelectric domain structures of (001)-oriented multiferroic $BiFeO_3$ films show a clear domain correlation, indicating a strong coupling between the two types of order. The ferroelectric structure was characterized using piezo force microscopy, whereas X-ray photoemission electron microscopy, as well as its temperature dependence, was used to verify the antiferromagnetic configuration. Antiferromagnetic domain switching (unusable for storage) induced by ferroelectric polarization has been achieved in agreement with theoretical predictions.[156] Strong magnetoelectric coupling does not imply the possibility of switching of magnetic domains by electric field or that an extra bit can be stored in a magnetic subsystem.

There are only a few multiferroic materials with T_C>350 K known today,[157] e.g., $BiFeO_3$ (1 μ_B per formula unit, ~50–60 $\mu C\ cm^{-2}$) and its derivatives, but hybrid material approaches may enable this coupling. An alternative method for engineering enhanced magnetoelectric effects is to introduce indirect coupling between two materials such as a ferromagnet and a ferroelectric.[158] Each material may then be independently optimized for room temperature performance. The combination of piezoelectric-magnetoresistive materials represents an artificial multiferroic, whose magnetization can be controlled by an electric field. There are several promising candidates for the piezoelectric-magnetostrictive structure, which have been experimentally studied: $PZT/NiFe_2O_4$ (1,400 $mV\ cm^{-1}\ Oe^{-1}$),[159] $CoFe_2O_4/BaTiO_3$ (50 $mV\ cm^{-1}\ Oe^{-1}$),[160] PZT/Terfenol-D (4,800 $mV\ cm^{-1}\ Oe^{-1}$).[161] The understanding of multiferroic-ferromagnetic coupling mechanisms may have significant impact on the development of novel spin-based memory devices, allowing for information encoding independently in electric and magnetic polarizations

DMS MATERIALS AND THEIR PROPERTIES

Dilute magnetic semiconductors (DMS)—semiconductors doped with 3d transition metals, like (Ga,Mn)As Table ERM7—enable electrically controlled electron spin for either injection into a semiconductor or as part of an active device. Since the DMS band and crystal structures may be compatible with other semiconductors, they could offer significant integration advantages, but they currently are ferromagnetic only at low temperatures (T_C <200K) The dilute magnetic semiconductors listed in the supplemental document for materials and T_C afford electric control via carrier mediated exchange interactions for emerging research devices.[162, 163, 164] In DMS, the structural homogeneity is critical for assessing the contributions from other separate phases, if present. For the determination of T_C using superconducting quantum interference devices (SQUID), the Arrott plot (vertical axis is magnetization squared (M^2) and horizontal axis is B/M) is critical to determine T_C correctly.[165] These data should be corroborated and validated with those of the Anomalous Hall effect.

Much attention has been devoted recently to exploring the possibility of a three-terminal spin injection logic device,[166, 167, 168] where spin is injected into semiconductor from either metallic ferromagnetic electrode or from magnetic semiconductor electrode. Relatively high spin injection from ferromagnets into nonmagnetic semiconductors was recently demonstrated at low temperatures.[169]; however, the magnetization in ferromagnetic semiconductors (FMS) usually vanishes or is too small at room temperature. Although attempts to achieve efficient room-temperature spin injection face substantial challenges, spin injection efficiencies greater than 10% are reported in metal insulator semiconductor (MIS) structures.[170, 171] Furthermore, the ability to inject and measure spin in silicon was recently demonstrated at low temperatures,[172, 173, 174] which offers hope for integration of spin devices with CMOS. Attempts to calculate T_C based on basic principles of carrier-mediated exchange[175, 176] have been unsuccessful with computed Curie temperatures being significantly different than experimental results. Therefore, improved models are needed.

DMS TO ACHIEVE T_C > 350 K

Since the discovery of DMSs, their Curie temperatures have increased, as a result of research to increase substitutional magnetic impurity composition in existing well-established DMS, such as (Ga,Mn)As.[176, 177] Further research to increase the solubility limit and self compensation effect of magnetic elements in semiconductors has further increased T_C.[178] More radical techniques, such as simultaneously using delta-doped magnetic structure with modulation doping,[179] are being investigated. An alternative approach to achieving high-T_C DMS uses wide bandgap semiconductor host nitrides and oxides, such as GaN, AlN, ZnO, TiO_2, doped with 3d transition metal impurities, Fe, Co, Ni, Mn, V, etc. In these materials, high magnetic impurity concentrations are needed, due to the lack of long-range interaction among magnetic spins.[175, 180, 181] In order to firmly establish whether the observed ferromagnetic order is intrinsic and produced by carrier mediated exchange, a series of measurements is needed to carefully rule out the possibility of having magnetic precipitates.[182, 183]

The nonuniform distribution of magnetic ions was studied theoretically[184] and observed in several DMSs.[185, 186, 187] The magnetically condensed region has nanometer dimensions and often has the same crystal structure as the host semiconductors. This nanoscale phase separation is suggested to be controlled by charge state.[187] In an effort to monolithically integrate ferromagnetic materials to nonmagnetic semiconductors, ferromagnetic materials that have the same crystal structure as the host in semiconductors are under investigation. So far, zinc blended CrAs and CrSb grown by molecular-beam epitaxy were confirmed to show ferromagnetism over 400 K.[188, 189]

Nanostructures of MnGe[186] were observed to have a $T_C > 400$ K, which seems to suggest a size effect. Likewise, the electric field control of similar structures using MOS also suggests the importance of the size.[190] Clearly the challenge will be to have these data repeated and to improve the understanding of these effects.

COMPLEX METAL OXIDES

Complex metal oxides cover a wide range of materials that include transition metal oxides alone or in combination with group II and lanthanide metal oxides. Many of these materials exist in a perovskite crystal structure and their functionality depends on the existence of bi-stable locations of the transition metal. The properties of these materials depend on the stoichiometry of the cations and anions and their properties can be dramatically changed by stress and oxygen vacancies. Furthermore, hydrogen can diffuse through these materials and change properties in the materials and at the interfaces. These materials are of interest for potential application to nonvolatile memories, by use of ferroelectric, resistance change or other properties. They are also of interest for a wide range of applications, including high dielectric constant capacitors in devices. Their more complex properties, such as coupled ferroelectric and ferromagnetic and anti-ferromagnetic properties, are of interest for potential application in novel memory or logic applications. Recently, complex properties of heterointerfaces between these materials have been observed and have stimulated interest for potentially enabling novel logic applications. Refer to Table ERM8.

Table ERM8 Potential Applications and Challenges for Complex Metal Oxides

APPLICATION	*POTENTIAL MATERIAL VALUE*	*KEY CHALLENGES*
FE FET	Static polarization	Control of defects and interfaces during fabrication Degradation of materials properties during use
Fuse-antifuse Memory	New high density memory cells	Reliability of the fuse mechanism
High Performance Capacitor	High dielectric constant	Dielectric constant decreases with thickness(<150 nm)
Spin Tunnel Barriers	See Spin Materials section	See *Interfaces* section
Novel Logic Devices	Strongly correlated electron state materials and heterostructures: novel coupling of electric and magnetic properties	Identification of dynamic properties compatible with logic applications Control of stoichiometry, vacancy concentration, and stress Material compatibility with CMOS processing

ELECTRICAL PROPERTIES AND DEFECTS

Most complex metal oxides are very wide bandgap semiconductors and their properties can be modulated by the concentration of oxygen vacancies or hydrogen. At any given growth temperature, there will be an equilibrium concentration of oxygen vacancies. This equilibrium concentration can be increased if the oxygen partial pressure is too low, so growth conditions are important for determining vacancy concentration. Depending on the material, oxygen vacancies can act as donors or traps that can change the conductivity of the material. Hydrogen can be a source of fixed positive or negative charge.[191] Defects can also serve to create fixed charge in dielectrics, which can impact leakage as they change the Fermi level.

ELECTRICAL INTERFACES AND DEFECTS

Defects at interfaces can pin the Fermi level and cause the band offsets to be different than expected, based on work function differences. Whether interfacial defects, such as oxygen vacancies or hydrogen, are introduced during the growth or deposition of interfacial materials, this Fermi level pinning[192] by defect levels in the bandgap may produce barriers that allow carrier tunneling,[193] which may make them undesirable for their chosen application. These issues are discussed in more detail in the Interfaces and Heterointerfaces section.

MATERIALS FOR MEMORIES

These complex metal oxides are being explored in Ferroelectric FET (FeFET), ionic, fuse-antifuse, and some versions of the electron injection memory with device requirements explained in more detail in the Emerging Research Devices chapter, Memory section. While each of these memories use different materials and mechanisms that require different properties, the stoichiometry of the materials, oxygen vacancies, and stress state have a significant role in the properties of these materials and their interfaces for all applications.

FERROELECTRIC RANDOM ACCESS MEMORY (FEFET MEMORY)

FeFET memories have gained interest due to their unique way of storing data based on the polarization states available in ferroelectric materials ($Pb(Zr_{1-x}Ti_x)O_3$). There are two stable polarization states available in $Pb(Zr_{1-x}Ti_x)O_3$ thin films where the Ti atom can move up or down based on the applied program electric field, the electric field must exceed a critical magnitude to move the Ti atom between the states. Perovskite (lead zirconate titanate, or PZT) and layered (Strontium Bismuth Tantalate, or SBT) ferroelectric materials are currently employed in FeFET memories. In FeFET memory fatigue, a loss of polarization under electric field cycling[194, 195] is a major issue that must be resolved. The interfaces to silicon and the conductive electrode are critical in this failure mode. Refer to the Emerging Research Devices chapter.

The FeFET has the ferroelectric material deposited on silicon with a conductive electrode deposited on top of the ferroelectric material. For the ferroelectric interface to silicon, since PZT and SBT do not form passivating interfaces with silicon, a dielectric buffer must be used, but this requires larger operating voltages and results in shorter retention time.[196] The top conductive electrode uses either a refractory metal or a conductive metal oxide, but both approaches have significant challenges with the refractory metals (Pt, Ir, Ru) catalyzing the dissociation and diffusion of hydrogen that degrades the ferroelectric material, and the conducting oxides (IrO_2, RuO_2)[194, 197] causing high leakage currents in the ferroelectric materials. The most commonly studied electrode is Pt with a Ti adhesion layer. But due to the high processing temperatures the oxidation of Ti to TiO_2 and interdiffusion of Pt and Ti leads to the interface degradation.[198] PZT thin films on Pt electrodes have good polarization and low leakage currents, while the fatigue is very poor. In order to avoid fatigue associated with oxygen vacancies, conductive oxides such as IrO_2 and RuO_2 have been used to replace the Ti layer in the electrode stack,[199] but they have higher leakage currents. Thus, to have better fatigue resistance, high remnant polarization and low leakage current electrodes, consisting of Pt films (10nm) grown on conductive oxide (e.g., RuO_2 or IrO_2)[198, 199] are being employed.

FUSE ANTI-FUSE MEMORIES

Recently, transition metal oxides have been used to demonstrate bi-stable resistance states that can serve as a basis for high density, low voltage non-volatile memory. In all cases, OFF-state current is driven by some form of defect-mediated transport, including defect mediated hopping transport and trap assisted tunneling. While the conduction mechanisms are not clearly understood in the ON-state, two classes of mechanisms are proposed to be involved: 1) defect mediated conduction, and 2) random localized filamentary conduction . In the first case, the conduction occurs first in the ON-state because the Fermi-level in the metal is pinned and aligned to donor type trap states that are typically oxygen vacancies,[200] so it is necessary to control and form the oxygen vacancies during processing. Further, the Fermi level pinning can be modified by deliberately having an appropriate interfacial layer between the metal electrode and the dielectric. In the case of filamentary conduction systems,[201] the oxides are doped with a metal, such as copper, and single or multiple random conduction filaments form in the oxide when a high electric field is applied. These conducting filaments may be broken by reversing the bias or re-formed by reapplying the programming bias. In this case, it is desirable to make the oxide defect-free to eliminate alternate conduction paths that can increase OFF state leakage. Oxygen electro-migration in these materials may produce device reliability issues, because it produces time dependant changes in oxide resistance that vary with electric field and current density,[202] which can be detrimental in device applications. Further, the dopant/dielectric combination must be chosen to increase dopant mobility, which impacts switching speed. An added materials challenge is that lateral diffusion barriers may be required to keep dopants in place within the memory cell. In all of these cases, control of oxygen vacancies and stoichiometry are crucial.

HIGH DIELECTRIC CONSTANT (K) MATERIALS

Key requirements for high performance capacitors include 1)high capacitance density, 2)linearity or very weak if any dependence of capacitance on voltage, 3)low temperature or very weak dependence of capacitance on temperature, and 4) minimal or no dispersion that represents the dependence of capacitance on frequency, high break-down field, and low cost.[203] A critical issue that may limit the ability to increase charge storage of high-κ dielectrics is the decreasing dielectric constant with film thickness and grain size. In experiments with several thicknesses of $BaTi_4O_9$ capacitors, the dielectric constant was found to decrease significantly below a thickness of about 50 nm.[204] Thickness dependence is important because the expected increase of capacitance density by scaling thickness is offset by decrease of dielectric constant. The dielectric constant of BST drops by a factor of 5–10 as the film thickness is decreased from 950- 145 nm.[205]

A critical property for MIM capacitors is linearity or weak dependence of capacitance on applied voltage. A primary cause for this is that the polarization inside the dielectric is no longer strictly proportional to the electric field.[206] More materials work needs to be focused on developing materials that are linear at higher electric fields. The trade-off is a reduction in the dielectric constant.

In conclusion, the most important need is for films with near perfect stoichiometrically and dispersion; however, deposited films tend to be imperfect due to limited oxygen in the ambient. Interface engineering is very important, as interface states in the bandgap can pin the Fermi-level of the electrode and modify charge transport barriers. Fundamental understanding of the switching mechanisms is critical to develop single high-κ materials with desired properties.

STRONGLY CORRELATED ELECTRON STATE MATERIALS

Strongly correlated electron state (SCES) materials have complex phases where the spin, charge, lattice, and orbital hybridization are coupled simultaneously. Complex phase transitions exist where charge ordering and electric properties change, and ferromagnetic and anti-ferromagnetic states occur Also, heterointerfaces formed between correlated materials have new state properties and interfaces to ferromagnetic materials have enabled coupling between ferroelectric properties and ferromagnetic properties in these structures. Most of the existing applications of these materials utilize relatively slow processes for high T_C superconductors, colossal magnetoresistance (CMR), and ferroelectric memories. The challenge is to determine whether these complex interactions can be controlled at high enough speeds and densities to enable new logic device functionality at the nanometer scale. Parameters such as energy, phase switching speed, field required to switch the state, dynamics of the states, and size dependencies need to be quantified to determine if SCES materials could be employed as a building block for an information processing system. Further, these electronic complexities in SCES materials occur due to charge (semiconducting electronic), or charge and spin (spintronics), and lattice and orbital degrees of freedom in the oxide system that result in several competitive metallic and insulating phases, increasing the potential for novel behavior. For details on emerging research devices, refer to the ERD chapter.

SCES materials exhibit correlated functions via their charge, spin and orbital symmetry. The challenge is to create a phase change through an external stimulus that will result in a dramatic change in electrical or magnetic properties. [207, 208] The ionic radius can also be varied to tune the phase transition and behaviors in oxides, such as manganites. In doing so, it has been shown that phase transitions of charge order, spin glass, and ferromagnetic phases[209] can be controlled, which could induce CMR and colossal electroresistance (CER).[210]

An interesting proposal is for *orbitronics,* which aims at controlling the electric current and, possibly, spin by triggering changes in d-electron orbital hybridization that propagate as a wave. This orbital wave could potentially transfer information and is called an *orbiton.* Orbital waves are characterized by peaks in orientation dependent Raman spectra that occur at approximately a few times the phonon frequency in $LaMnO_3$ (e.g., electron system).[211] Experimental evidence of orbitons being controlled by an electric field is still required, as is the understanding of orbiton dynamics and the energy required to generate an orbiton.

An important parameter that comes from spin-orbit interactions is the toroidal moment, which is the product of polarization and magnetization. For instance, a material such as $GaFe_2O_3$ has been shown to possess magnetoelectric properties in an optical frequency region, as revealed by nonlinear Kerr rotation detection.[212] This may have value in electro-magneto-optical devices. This optical technique has also been shown to be applicable for detecting interface magnetism of SCES heteroepitaxial structures.[213]

The ability to initiate CMR via electric control of a frustrated, frustration is a situation where a system cannot simultaneously minimize interaction energies and may have multiple effective ground states, spin-structure has been demonstrated. Competition between ferromagnetic, paraelectric, antiferromagnetic, and ferroelectric phases causes a phase change at a bi- or multi-critical point by applying an electric or a magnetic field on a multiferroic material.[214] $TbMnO_3$ exhibits gigantic-magnetoelectric and magnetocapacitance effects, which can be attributed to switching of the electric polarization induced by magnetic fields. Frustrated spin systems provide a new area to investigate for magnetoelectric media.

STRONGLY CORRELATED ELECTRON STATE HETEROINTERFACES

Heterointerfaces between strongly correlated electron state (SCES) materials have been found to have new properties that may enable new functionality for device applications. For example, the conductivity of the interface between two insulators, $LaAlO_3$ and $SrTiO_3$, can be dynamically tuned across a metal-insulator transition by applying an external gate field. The result is a system that can be switched from highly insulating to highly conducting.[215] The switching has been demonstrated to have a seven-order of magnitude change in resistivity and has a hysteretic effect. It has been shown that a critical thickness of four-six unit cell layers is required for the increased interface conductivity and carrier density to occur.[216, 217]

By growing precise structures that incorporate an external gate, the interface can be statically and dynamically tuned over many orders of magnitude - R_{on}/R_{off} 10^7.[217] Due to the long time constant, it was hypothesized that this may be controlled by creation and migration of defects, such as oxygen defects. The switching voltages used were very high (60-100V)[217] due to the thick insulating substrate, but it is important to understand the local fields required to cause the formation and elimination of the conductive interface. Electronic switching has also been reported in manganite materials with nanometer scale thicknesses of $Sm_{0.7}Ca_{0.3}MnO_3$ deposited on $La_{0.7}Sr_{0.3}MnO_3$.[218] Alternating $LaMnO_3/SrMnO_3$ heterostructures, with thicknesses of 6 and 4 unit cells, respectively, exhibited properties different than the alloy with the same average composition.[219] It is important to determine the fundamental mechanism that enables these new states and determine the role of interfacial strain and oxygen related defectsOxide heterostructure property control and challenges are discussed in more detail in the Interfaces and Heterointerfaces section.

New metrology is needed to characterize charge, potential, and spin properties at these interfaces simultaneously. Scanning probe techniques are used to characterize ferroelectric interfaces at the nanometer scale,[220, 221, 222] but this also needs to include characterization of spin and magnetic properties to correlate these effects. These requirements are discussed in more detail in the *Metrology* section of this chapter. .

INTERFACES AND HETEROINTERFACES

Interfaces provide charge and spin access to low-dimensional nanoscale materials and devices and also serve as barriers. Interfaces are of long-term importance, because their properties dominate the performance and limit the reliability of electronic devices, particularly at the nanoscale. It is critical to understand the correlation of interface physical and compositional nanostructure to electronic and spin properties. Also, the underlying physical and chemical mechanisms of interface factors that control reliability must be understood.

The types of interfaces considered here include on-chip device and interconnect structures, as well as packages with electrical and thermomechanical constraints. This section summarizes the key issues and challenges involved in controlling interface structures, composition, and properties for various emerging research device types. The major issues for each device type are organized as heterostructure interfaces (semiconductor-semiconductor, oxide-oxide, and organic-organic), contacts (electrical and magnetic), and dielectric interfaces (passivation, barriers, low-κ and high-κ dielectric interfaces). Recent research on interfaces discussed in this section has emphasized the use of engineered interfacial molecular monolayers to ameliorate some of the adverse effects of abrupt compositional, phase, and bond changes inherent to interfaces. Refer to the ERD chapter.

HETEROINTERFACES

For heterostructure interfaces, control of the charge and spin transfer, transport, and modulation requires that the electronic band structures be properly aligned in the presence of interface band bending and that no defects are generated that pin the Fermi levels. Furthermore, any stress effects that can occur due to lattice mismatch of the materials or other factors must be controlled, since they can change the electronic properties of the materials. Typically, for nanoscale heteroepitaxial film thicknesses, the films remain elastically strained and do not relieve stress through misfit dislocation formation. At these stress levels, the electronic properties of the films can be affected.

For compound semiconductors or complex metal oxides, the stoichiometry at the interface must be controlled, since composition and stress can change the electronic properties. For semiconductor heterostructures, carrier transport is affected by both phonon scattering and interface scattering, due to topological roughness and heteroepitaxial elastic stress and defects. For nanoscale lengths, carrier dynamics are well within the scattering lengths typical for bulk materials and must be treated as electromagnetic waves rather than particles obeying Boltzmann statistics.

In the case of complex metal oxide heterointerfaces, stress can cause one material to change crystal structure and produce dramatic changes in properties. Furthermore, since properties of complex metal oxides depend on stoichiometry and vacancy concentration, control of both cationic and anionic stoichiometries, including the oxygen vacancy concentration in each material and at the interface is needed. Characterization of oxygen vacancy concentration down to the 1E10 cm^{-2} level in these materials and at their interfaces is very difficult, which makes analysis of the role of vacancies at the interface difficult. In addition, the role of atomic hydrogen, [H], in neutralizing vacancies must be carefully understood. Apart from stoichiometry concerns, the control of band offset in oxide heterostructure interfaces, through the use of *interfactant* compositional layers, has been reported.[223] For organic-organic heterostructures, charge transport layers require bonding and conformational transformations from pi to sigma bonds across relatively large molecular distances and impurity effects must be minimized.[224]

ELECTRICAL CONTACTS AND SCHOTTKY BARRIERS

For electrical contacts, the energy required to inject charge into the active material becomes critical and is determined by alignment of metal work functions to the energy bands of the active material when interface states or interface reactions don't occur. To achieve Ohmic contacts to semiconductor devices, degenerate doping of the semiconductor has produced low-resistance contacts, but as devices approach the nanometer scale, electrical contacts may need to be formed without degenerately doping the semiconductor contacts. The lack of degenerate doping creates challenges for the formation of reliable contacts to semiconductor nanowires. In the case of carbon-based structures, whether molecular, nanotube or graphitic structures, high contact resistances or high tunnel barriers may limit electrical performance in device or interconnect applications. For carbon nanotube FETs, the contact resistance is modulated by the gate voltage.[225] Thus, it is important to understand the interfacial bonding and how this controls the interface electrical properties and barriers. For example, the use of intermediate amide linkers on carbon nanotubes has been shown to affect the deposited coverage of contact metals.[226, 227, 228] Also, at the nanoscale, dipole moments and charge screening exist at the or near the interface , their affect on contact behavior is poorly understood.

In the case of complex metal-oxide interfaces, the metal must not react with the oxide.[229] Oxygen vacancies and hydrogen can dramatically change the properties of the contacts. This is especially important during the life of the device structures as electric fields in the presence of hydrogen may affect electronic properties. Detection of vacancy concentrations and hydrogen at these interfaces is extremely difficult and limits the ability to determine their role in interface formation and reliability. In some cases, metals are known to catalyze the formation of atomic hydrogen which can interact with oxygen and oxygen vacancies to change the behavior of the interfaces. This formation of atomic hydrogen is believed to be associated with a failure mode for devices based on these materials, so metals that catalyze the formation of atomic hydrogen may be of limited value. In addition to unwanted chemical and electrochemical behavior, the metal-dielectric interfaces usually show dipole effects associated with interface charges and contamination effects.

Another issue in ferroelectric oxide-metal interfaces is the effect of bottom electrodes on the crystalline structure of the deposited oxides and a resultant degradation of ferroelectric properties. In addition, problems of metal adhesion and diffusion of metals into ferroelectric oxides can be significant and interface adhesion promoters and diffusion barriers such as Ti or conductive oxides (IrO_2 and RuO_2) interlayers between Pt and the ferroelectric oxides have been developed. Conductive oxides also improve the fatiguing of the ferroelectric bit at the expense of higher leakage current.[230]

For metal-organic interfaces, contact properties may be determined by whether the metal is deposited on the organic or organic deposited on metal since metal deposition processes are more energetic and may result in damage to the organic material. The challenge is to fabricate low-impedance top contacts with reliable, repeatable properties. Interface energy barriers are determined by various factors such as molecular hybridization, matching of metal work functions to organic highest occupied and lowest unoccupied molecular orbital [HOMO and LUMO respectively] levels, and the control of dipole energy barriers [228, 231, 232, 233, 234] Any uncontrolled interface chemistry will introduce variability in the contact properties and affect the performance of devices such as transparent organic FETs and LEDs. In addition to interface compositional control, the molecular conformation at the interface is a critical factor in determining the contact electrical properties.[235, 236] The current through molecular films can vary by more than one order of magnitude depending on the angle between the axis of the molecules and the interface normal. This is a consequence of the strong directional character of the *p* binding orbitals that determine the transport of electrons through the conjugated molecules.

SPIN INJECTION OR SPIN FILTER INTERFACES

Spin injection interfaces are of two basic types: 1) ferromagnetic metals on non-magnetic semiconductors and 2) magnetic semiconductors on non-magnetic semiconductors. The key physical process involves injecting spin polarized current from the magnetic metal or semiconductor to the non-magnetic semiconductor or preferentially extracting electrons with certain spin direction. It has been found that the interface defect densities do not need to be as low as for FETs or laser diodes because of the relative inefficiency of spin flips induced even by substantial numbers of interface defects.[237] Thus, spin flip scattering does not become a problem until interface defect densities are relatively high. In addition to the band alignment required for electron transport in epitaxial systems, in spin transport, the symmetry of the spin bands in the materials need to align, limiting the choices of material combinations that can be used. Heterointerfaces between a magnetically doped semiconductor and an undoped semiconductor have demonstrated high injection efficiency, because the symmetry of the bands is similar, but these systems currently only operate at low temperatures, due to low Curie temperatures. Iron (Fe) and iron-cobalt (Fe-Co) have good spin-band symmetry, with the bands of group IV and III-V semiconductors, but they have much higher conductivities than the semiconductors and need to form either a Schottky barrier or have a tunnel barrier between the ferromagnetic metal and the semiconductor. The Schottky barrier between the ferromagnetic metal and the semiconductor must be very thin[238] and may be in series with an insulating tunnel barrier of another material. In the epitaxial metal-semiconductor case, the bands in the tunnel barrier must align and have spin symmetry compatible with the metal and the semiconductor bands. Epitaxial Fe/MgO appears to be the current best-choice interface material[239] that satisfies these constraints. In addition to proper band alignment, tunneling spin filters with extremely well controlled barrier thicknesses and very small interface roughness are needed.[240]

DIELECTRIC INTERFACES

For dielectric interfaces, such as gate dielectrics and metal-low-κ dielectrics, the major issue is to control the dielectric properties at the interface to preserve the desired electrical properties. For high-κ gate dielectrics, unwanted chemical reactions and stoichiometry changes can occur that degrade the electrical behavior. For low-κ dielectrics, interface adhesion stress effects are significant because of the very low elastic modulus of such dielectrics, the low adhesion energies, and the resulting enhancement of metal electromigration. One remedy is to increase the Cu-low-κ interface toughness by 6× through the use of molecular monolayers, where one end of the molecule has a thiol (sulfur) termination for binding to Cu and the other end has a siloxane bridge for binding to the dielectric.[241]

For ferroelectric oxide-semiconductor interfaces, defects can cause a loss of polarization, known as fatigue, due to charge trapping. Dielectric interface buffers have been explored to improve the interface characteristics and reduce fatigue.[234] However, larger operating voltages are required and charge retention times are shortened.

PACKAGE INTERFACES

Package interfaces dominate the electrical impedance, thermomechanical stress, and heat-transfer characteristics. The main opportunities are in package designs that minimize the number of interfaces and configure them to minimize electrical, thermal, and stress effects. Interface engineering will be required to optimize the performance of future packages.

SUBSURFACE INTERFACE MEASUREMENTS

Subsurface interface measurements are critical to the control of interface properties through the various stages of fabrication, packaging, and operation. Detailed requirements are described in the Metrology embedded interfaces section.

Modeling of embedded interface electron and spin properties is needed to provide a proper basis for the design of future devices, interconnects, and circuits. In particular, modeling is needed to separate the probe-specimen interactions to determine the unperturbed interface properties. Phenomena such as interface chemical bonding, interdiffusion and reactivity, physical scattering mechanisms, mechanical adhesion energies, and charge/spin injection behaviors need to be modeled and included in future CAD capabilities.

ENVIRONMENT, SAFETY, AND HEALTH

Emerging research materials covers a very broad range of materials with wide potential applicability. Even with the potentially broad range of applications, these could be classified as 1) new materials deposited by a conventional deposition process and then patterned and processed with conventional technology; 2) new chemicals that would be integrated onto the wafer or package or used in processing; 3) nanostructured materials that are deposited with conventional technology and embedded in a layer on a wafer or in a package, and 4) nanostructured materials that are produced in a powder or in a liquid suspension to be used in processing or integrated with structures on a wafer or in a package.

In cases where existing or new chemicals are used to fabricate thin films or materials with conventional processes, existing environmental safety and health protocols should be applied in the assessment of their hazard and risk. In the case where "free" nanoparticles are produced in either powder or liquid form, research has raised concerns that these nanoparticles may be mobile in biological organisms and humans and potentially have unknown toxicological effects.[242, 243, 244, 245, 246, 247, 248, 249, 250] Thus, it is important for researchers working with these materials to employ conservative procedures that reduce the potential for direct human exposure to these materials. The semiconductor and chemical industries have identified a joint set of research needs to improve detection of nanomaterials and the understanding of their potential for bio-interaction. For further details on these needs, refer to the supplemental online document.

EMERGING MATERIALS SYNTHESIS

In the cases where new chemicals or materials are used to deposit an emerging research material, conventional protocols should be used to assess the hazards and risk of the material in handling, processing, and disposing of the material or process waste. Researchers should be aware of and follow these protocols in evaluating new chemicals and materials. Refer to the ESH chapter.

NANOMATERIALS

Evidence is emerging that "free" nanoparticles may be mobile in biological organisms, but more work is needed to understand the concentration and dose dependence of these effects. Nanomaterials or nanoparticles chemically bonded to substrates and embedded in a structure would have a significantly lower risk for exposure than free nanoparticles. Some studies have indicated that some nanoparticles can induce tissue inflammation and possible toxic responses under some circumstances, and the size dependence is not understood. Although further research is needed to understand the potential for exposure, exposure concentration thresholds, and dose rates that may produce hazards, researchers should be conservative in their management of these materials. They should employ conservative practices in handling these materials and limit direct exposure. As these materials are further processed, researchers should ensure that nanoparticle byproducts formed in processes are contained to limit researcher and environmental exposure. Furthermore, when maintenance is performed on equipment where nanoparticles were processed or generated, procedures should be employed to reduce direct human exposure. Finally, as waste is generated, disposal processes should be employed to minimize human and environmental exposure.

As new research on potential environment, safety, and health effects emerges, researchers and their Environment, Safety, and Health organizations should monitor advances in understanding potential hazards and risks, and new technologies and methodologies to reduce risk. A broad range of research on instrumentation to monitor potential exposure, to understand factors affecting potential mobility of nanoparticles in biological organisms and the factors affecting the potential for inflammation and toxicological reactions is under way and should be monitored in technical journals. Furthermore, the several groups are establishing databases in technical publications on these topics. Also, a number of organizations are assessing current practices and developing best practices to manage these materials. For further details regarding one example, see the linked report of current practices.

As fundamental principles of nanomaterial interactions with biological organisms are identified and understood, improved protocols need to be developed that enable hierarchical assessment of hazard and risk of new nanomaterials, as they are evaluated in research, integrated in manufacturing processes, and potentially used in products. Since increasing material volumes would be used in each of these stages of the manufacturing lifecycle, additional considerations would need to be incorporated in the assessment process. Metrology to detect the presence of nanoparticles is critically needed to improve risk assessment capabilities; details are described in the Metrology section of this chapter.

A hierarchy of risk assessment methodologies needs to be developed that comprehends the different potential exposure risk in research, technology development, product development, product applications, and product end-of-life. In research, sample sizes would be small, with a small number of people involved in a controlled environment. If the material moves to technology development, the volume of material and number of people involved would increase, so risk assessment would need to cover more operational functions and increased material disposal issues. If nanomaterials are to be developed into a product, the risk assessment would need to include manufacturing, distribution, potential consumers, and product end-of-life or recycling. Thus, the risk assessment would need to be expanded in scope with each stage of the technology life cycle. This assessment would need to comprehend learning from recent research. Researchers should continue to improve their processes for managing ESH on conventional and nanomaterials as hazard and risk research progress.

METROLOGY

Metrology is needed to support emerging research materials (ERM), by imaging chemical composition and structure at sub nanometer dimensions, characterizing structures and properties of embedded interfaces, simultaneously measuring complex properties at nm dimensions, and measuring defect concentrations and distributions on nm scale structures. Further discussion about metrology for ERM can be found in the Metrology chapter, in the section titled *Metrology for Emerging Research Materials and Devices*.

IMAGING STRUCTURE AND COMPOSITION AT THE NANOMETER SCALE

ERMs potentially will be integrated into nanometer scale structures, so metrology is needed to image the composition and structure of a wide range of complex materials, including low z materials, with atomic scale dimensional accuracy. Other complex materials of interest include nanostructured materials and insulating films with complex properties, etc. If low-dimensional materials, such as carbon nanotubes, are to be used in devices or interconnects, then integrated metrology is needed to measure their *in situ* structure, composition, and orientation. Examples include the placement and alignment accuracy of patterned gate materials, contacts on nanotubes, and nanotube interconnects over microns in length. Similarly, for self-assembled materials to be a viable option for extending conventional lithographic technologies, accurate measurement methods are needed to characterize ultra-thin films of patterned materials, such as block co-polymers, and measure their alignment to previously patterned structures, with sub nm accuracy. Furthermore, accurate ferromagnetic and magnetic material characterization is needed for developing potential spin structures, decoupled from the impact of the structure's magnetic properties. Complex metal oxides [CMOs] are being investigated for a wide range of applications. The dimensions of structures fabricated with CMOs and other materials on them will need to be measured accurately, even though they may be highly insulating or have ferroelectric and magnetic properties. Recent advances in materials characterization methods needs to continue to meet these needs. Examples of these advances in the area of microscopy include aberration corrected electron microscopy, atom probes, and advances in scanned probe microscopy. Advances in X-ray and optical methods also provide critical compositional and structural information for films and arrays of nano-structures.

EMBEDDED NANO-INTERFACE CHARACTERIZATION

The ERMs being investigated for applications in devices or interconnects will be integrated with other materials that form interfaces, where understanding and control of the structure, composition, stress, and properties is critical. For carbon nanotubes or nanowires to be viable in transistor applications, the ability to characterize structural and electronic properties of passivation interfaces and contacts when embedded in other structures is difficult and important. In the case of carbon nanotubes, imaging the interface is made even more difficult, because electron beams do not have adequate sensitivity or resolution to locate the carbon atoms. For nanowire transistors, the effect of small diameter, curvature, and different exposed crystal planes on surface- and interface states needs to be determined. Characterization of the in-situ contact-molecule structure and properties in molecular devices is very difficult because any sample preparation such as cross-sectioning will destroy the interface. Determining electronic properties and bonding at the interface are even more difficult to measure, as described in the Macromolecule section. Spin material interfaces require the ability to nondestructively investigate the spin states on each side of an interface and the spin transport across the interface, but often devices must be fabricated to characterize this indirectly. Complex metal oxides have a wide range of properties including electrical, magnetic, polarization and others, so it is important to not only characterize the structure, but also the electronic, polarization and electronic states at these interfaces and understand whether interface states are affecting their operation. Both physical and electrical measurement methods need to advance. Advances in several methods are necessary, if functionally robust nano-interfaces between materials are to be developed. In addition, the use of arrayed test structures should not be overlooked.

Current subsurface interface imaging and measurement techniques are marginally adequate for understanding interface phenomena, and many current techniques are destructive, since they require cross-sections. Although these have been extremely useful for structural examinations,[251] other interface properties are of equal interest.

Some of the non-destructive techniques used for subsurface interface measurements include the following:

- Internal photoelectron emission electron spectroscopy for energy level shifts[252]
- X-ray photoemission spectroscopy (XPS) for compositional changes[253]
- High resolution X-ray diffraction
- Scanning near-field ultrasound microscopy for mechanical measurements[254]
- Raman and FTIR for chemical changes such as hydroxyl (OH] ion measurement and buried nanotube imaging[255]
- Ballistic electron emission microscopy (BEEM)[256, 257, 258] and impedance spectroscopy for electron transport interface behavior
- Spectroscopic ellipsometry and force probe ellipsometry for dielectric property changes
- Scanning electron microscopy with polarization analysis (SEMPA)[259, 260]
- Nonlocal electrical detection of spin injection[261] and magnetic resonance force microscopy for spin state changes[262]

In addition, there is emerging interest in correlated, multimodal microscopies to maximize information return from nanoscale objects and interfaces. Here techniques are combined either simultaneously or asynchronously through nanoscale registration techniques. Modeling of embedded interface electron and spin properties is needed to provide a proper basis for the design of future devices, interconnects, and circuits. In particular modeling is needed to separate the probe-specimen interactions to determine the unperturbed interface properties.

PROPERTY MAPPING

The ability to measure or map properties of a large number of low-dimensional materials is needed to support improvement in materials synthesis for a wide range of applications, such as nanotubes and nanowires for transistors or interconnects, high refractive index nanoparticles for use in immersion fluids, and other applications. For nanotubes to be viable in transistors, they must be fabricated with a tight distribution of threshold voltages. Robust fabrication requires an ability to map bandgap distributions across a wafer and to identify those regions with properties outside of the target. While fluorescence and other spectroscopic techniques are sensitive to the local chemical environment, alternative options are needed to support this capability. Similarly, the conductivity of metallic or multiwalled nanotubes would need to be mapped to determine whether a specified synthetic approach is producing a uniform and satisfactory product distribution. Numerous methods require advancement. These include optical, X-ray, electron and ion beam, and scanned probe. For example, determining the optical (THz to VUV) and low-frequency dielectric properties of low-dimensional materials is critical to enabling rapid optical metrology and measuring property uniformity. Another need is for electrical measurement test structures that allow mapping uniformity across a large area.

SIMULTANEOUS SPIN AND ELECTRICAL PROPERTIES

For spin state materials and complex metal oxides, the ability to simultaneously measure the electrical and magnetic properties at the nanometer scale is critical. These materials and their interfaces have coupled electronic and magnetic properties, which may be affected by local material defects. Scanning probe techniques can measure the electrical properties or magnetic properties independently, but the maps of properties may not align physically. Hence, methods are needed that are capable of measuring coupled properties simultaneously and providing insight into the local coupling of magnetic and electronic properties to an applied stimulus.

CHARACTERIZATION OF VACANCIES AND DEFECTS IN NM SCALE STRUCTURES

The properties of most nanostructured materials, including nanotubes, nanowires, spin materials, and complex metal oxides for applications in devices, are dramatically affected by small concentrations of vacancies and defects. In the case of carbon nanotubes, a missing carbon atom locally can change the electronic properties of the nanotube. Alternatively, functionalization also can result in the formation of vacancies, or rehybridization, of the carbon that introduces states in the gap. Such material perturbations can dramatically change these materials' electronic or thermal properties. Complex metal oxide properties, including electrical, ferroelectric, and ferromagnetic, are strongly affected by the presence of oxygen vacancies, since the vacancy creates local distortions of the crystal structure that can break symmetry and induce different electronic states. In some cases, interface conductance properties of insulating oxide heterostructures are reported to be enhanced by the presence of oxygen vacancies in planar structures. The challenge will be to detect the presence of small concentrations of vacancies and defects in nanometer scale structures. In the case of normal transistors, statistical changes in dopant distribution are causing changes in threshold voltage distributions. Therefore, the ability to map vacancies, defects, and dopant atoms may be needed to enable future emerging device options. In addition to the further development of microscopy, other physical measurement methods should also be advanced so that the relationship between defects and properties can be measured, quantified, and understood.

MODELING AND ANALYSIS OF PROBE-SAMPLE INTERACTIONS

Nanometer scale measurement tools, such as electron microscopes or scanning or optical probes, exhibit significant coupling between the probe and sample states. Significant research is needed to develop methods for decoupling these interactions and accurately determine nanoscopic structures and properties. Also needed are sample-probe interaction models for characterizing nanoscale structure, defect locations, and electronic, magnetic, and optical properties. At first, these models could be used to simulate probe signals with hypothetical structures and properties. However, algorithms need to be evolved that enable the extraction of actual structures and properties from the coupled signals.

METROLOGY NEEDS FOR LOW-DIMENSIONAL MATERIALS

New metrologies are needed to determine the feasibility of using carbon nanotubes in devices and on-chip interconnects, as well as in deterministic doping, passivation, gate, and contact applications. For nanotubes to be viable as high-performance transistors, the ability to grow or assemble nanotubes in precise locations with a tight bandgap control across a wafer must be demonstrated, with no metallic nanotubes present. This application requires measurement methods that can differentiate easily between metallic and semiconducting nanotubes. Such devices also will require an ability to measure accurately dopant placement and distribution that enable controlled p-and n-type doping and surface passivation for gate structures. Other low-dimensional materials, including nano-dots and nanowires, may be used in devices. Metrology needs to be developed to elucidate the physical and electrical properties of these materials. Measurement methods need to be developed for observing and quantifying the impact of defects and stress on low-dimensional materials. Other phenomena such as excitons may be used in new devices. Metrology for the measurement of excitons and other properties needs to be developed.

VIA METROLOGY NEEDS

For single or multiwalled carbon nanotubes to warrant consideration for via applications, their resistivity must be competitive with existing technology. Nanotubes have yet to achieve adequate density for low resistivity and demonstrate competitive low resistance contacts. The ability to measure nanotube densities in vias would enable researchers to determine whether process conditions specifically correlate with effective nanotube density. Scanning electron microscopy (SEM) requires significant time to measure the density. Once synthetic techniques yield adequate nanotube densities, then non-destructive in-situ methods to measure effective contact resistance across the via and nanotube resistivity distributions in the via will be needed.

SELF ASSEMBLY METROLOGY NEEDS

For directed self assembly to be viable as a lithography extension or to assemble nanostructured materials in predefined locations and alignment, metrology is needed to evaluate the size and location of features and the registration to previously patterned structures. For block co-polymer based directed self assembly to be viable for extending lithography, metrology must be able to measure feature sizes, line width roughness, alignment to existing structures, and defects. However, these thin, sub 100 nm thick organic films are difficult to image with electron microscopy. These thicknesses likely will decrease as dimensions continue to scale. Thus, electron microscopy enhancements or techniques, such as helium ion microscopy, should be explored to determine whether they can provide increased image contrast between ultrathin polymer films and existing structures. Other methods such as X-ray and optical scattering should not be overlooked as means of providing information about dimension, shape, stress, and array structure, e.g., location of nano-dots with respect to each other.

COMPLEX METAL OXIDE METROLOGY

Complex metal oxides are of interest for potential application as ultra-high-κ dielectrics for device gate dielectrics, package capacitors, and possibly for logic devices, where possible dynamic transitions of coupled electrical and magnetic properties may exist close to phase transitions. The properties of these materials are strongly dependent on the presence and concentration of oxygen vacancies and also on cation stoichiometry. While existing metrology is capable of characterizing the concentration of oxygen vacancies[263] and cation stoichiometry in uniform thin films or bulk samples, metrology methods are just emerging to measuring these in nanometer scale structures.[264] Furthermore, some of these methods are destructive in that a small sample must be prepared. For example aberration corrected high resolution TEM can observe single oxygen vacancies in single crystal oxides when it is linked to simulations.[265] Thus, metrology is needed to characterize the oxygen vacancy and cation stoichiometry at the nanometer scale and also enable the characterization of electrical and magnetic properties at the nanometer scale.

Characterization of ferroelectric properties and magnetic properties at the nanometer scale is possible with state of the art scanning probe metrology, but carrier concentration is limited to tens of nanometers. Consequently, it currently is not possible to characterize simultaneously multiple properties, such as electric and magnetic properties at the nanometer scale. Even if instruments were capable of measuring the electric and magnetic forces, models may be needed to decouple and separate the signals from the electrical and magnetic probes and to extract the magnitude and direction of the electric and magnetic fields. Further development of measurement methods for carrier properties in complex oxides is required. In addition to nano-probe based electrical testing, magneto-optic Hall effect measurements can provide non-contact measurements. In addition, electro-optical measurements can determine coupling between the spontaneous polarization in Wurtzite structures and the ferroelectric polarization in perovskite structures and interfaces. The possible use of advanced electron microscopy for observation of shifts in atomic positions should not be overlooked. Further research in the application of all of these methods to complex oxides is necessary.

PACKAGE NEEDS

Microelectronic packages have a complex assembly of heterogeneous materials such as metals, ceramics, and polymers and large stresses can develop due to a thermal expansion (CTE) mismatch between these materials. Metrologies are needed for measuring these internal thermo-mechanical stresses and strains within bulk package materials and at various interfaces of the microelectronic package, with accuracy and scalability in use conditions.

MODELING AND SIMULATION

The complexity of materials modeling in nanotechnology is increasing due to the following three factors: 1) the number of materials has continued to increase (over 3× increases over a period of 20 years), 2) the ratio of surface-to-volume of the material is inversely proportional to the dimension of the structure, and 3) smaller numbers of atoms that could lead to larger statistical variations. These lead to more atoms of different chemical nature being packed in smaller dimensions. As a result, the measured bulk material properties differ from observed materials behavior in nanostructures. The behavior of devices and materials are directly correlated to their electronic structure. This correlation is equally valid for both charge-based and non-charge-based technologies, as physical and chemical effects at these dimensions are directly related to the electronic structure. Physical modeling and numerical simulations are critically needed: 1) to explain observed phenomena, 2) to predict new phenomena, 3) to direct experimental studies to desired outcomes, and 4) to interpret the metrology. In addition, they enable a fundamental understanding of the mechanisms and the interactions between processes and materials.

Application of materials for ERM requires a fundamental understanding and characterization of *synthesis, structure, and properties (Figure ERM3)*. This understanding comes from the natural logical flow of interactions in integrating newer materials to develop a new device, whether it is for device, interconnects, or packaging. The methods and conditions of synthesis determine the structure and composition of the engineered materials. Structure then determines the material properties and performance.

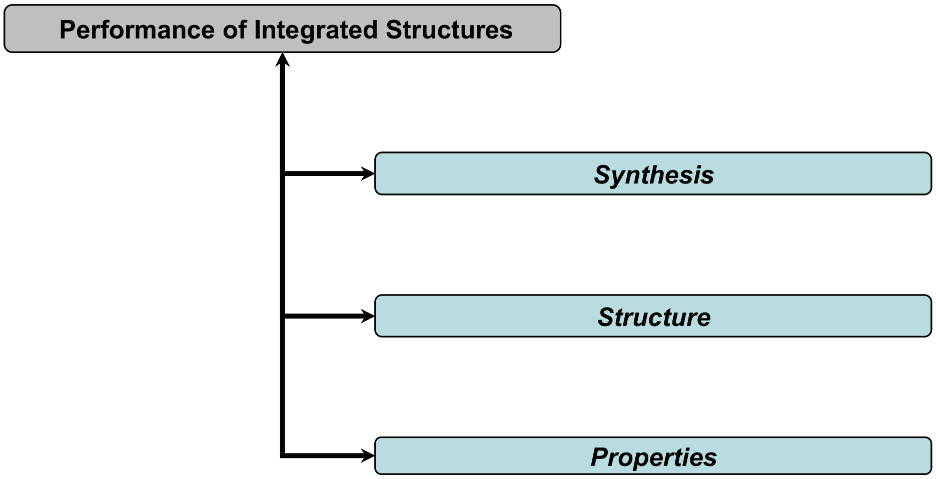

Figure ERM3 Design Factors that Drive the Performance of Integrated Emerging Research Materials

Materials synthesis is determined by the class of materials and the desired application. For example, nanotube growth and functionalization are determined by the chemical and electrical conditions in the reactor and the interactions with the substrate. Depending on the method of synthesis, *in situ* and *ex situ* requirements are different. From a modeling perspective, a key requirement is the understanding of the roles/mechanism of processing and the specific structure resulting from the synthesis. As an example, in atomic layer deposition, the physical model must comprehend gas phase and surface chemistry in addition to mass and energy transport. Film nucleation and subsequent growth, which determine morphology, also require modeling. In addition to description of the temporal evolution of a new phase, it becomes necessary to describe the spatial ordering in many systems (e.g., quantum dots, nano-wires.[266] Classical nucleation and growth concepts adequately describe phase transitions in some nanoscale phase change memory materials.[267] Controlling the morphology of the nanoscopic material requires detailed information on phase stability and dynamics of atomistic processes. In small nanoscale systems, in which dimensions may not be significantly larger than the range of interatomic interactions, classical thermodynamic concepts such as extensive and intensive properties may no longer be valid. In these cases, the classical concept of a phase transition, including the Gibbs Phase Rule that occurs in the thermodynamic limit of an infinitely large system, may not hold.[268, 269] Development of a theory of phase transition in such finite sized systems for understanding the dynamics of phase transition may be critical to control nucleation and growth of certain nanoscale materials. The description and prediction of fragmentation, a process by which phase transitions have been observed to occur in nanoscopic systems, presents a significant challenge in statistical mechanics. Density functional theory,[270, 271] which is based on density fluctuations rather than the existence of clusters of classical and atomistic nucleation, should be investigated as a tool for describing phase transitions in small systems and fragmentation. More details of the other scales are covered in the Modeling and Simulation chapter.

Synthesis determines the structure and composition of thin films. To predict the material properties, both characterization and physical modeling of the structures are needed. The materials may be crystalline, poly-crystalline, semi-crystalline, amorphous, or visco-elastic. The structure of the materials determines their behavior.[272] For example, the resistivity of films in (100) orientation is different from (111) crystallographic orientation. Realistic structures are not ideal single crystalline films and need advanced metrology for their complete characterization. These characterized structures serve as inputs into the physical models. Given the limited size of problems that can be solved, a combination of techniques spanning different length and timescales are needed to model structures effectively.

The material properties are based on the electronic structure of condensed matter. For a given structure, the Schrodinger equation determines chemical, electrical, mechanical, and thermal properties. In turn, the nature of the hyper-dimensional Schrodinger equation is determined by the number of electrons in the structure. As the number of electrons are very high in condensed matter ($\sim 10^{23}$ in an unit volume of material), any solution of the equation for realistic macroscopic system is generally accomplished using one of two techniques; 1) single particle approximation and/or 2) multi-scale techniques with distinct formalisms representing different scales.

An example of hierarchy of these models is given below. The models have different scales based on the specific physical phenomena, as follows:

1. Atomic or molecular scale is based on self-consistent solutions of Schrödinger equation as mentioned above.
2. Nanostructural scale uses multi-scale techniques based on kinetic and quantum formalism (e.g., device, or interconnect with barrier layers).
3. The thin film scale (e.g., gate oxide or barrier layer) is mesoscale in nature, and links with kinetic models at the macroscopic level.

In the macroscopic scale (e.g., die, package), bulk properties are used in constitutive models that describe the response of materials to different stimuli. For the area of ERM, the main focus of research should be on the top three levels, with an emphasis on atomic or molecular and nanostructural scale. Since structural dimensions are currently at 45 nm or below, the materials properties at this scale may behave differently when integrated than in bulk. In addition, optimization of the performance reliability of devices or materials in nanodimensions during ambient and accelerated usage conditions requires model extensions that include phonon interactions as well as electronic interactions. More details of the other scales are covered in the Modeling and Simulation chapter in the roadmap.

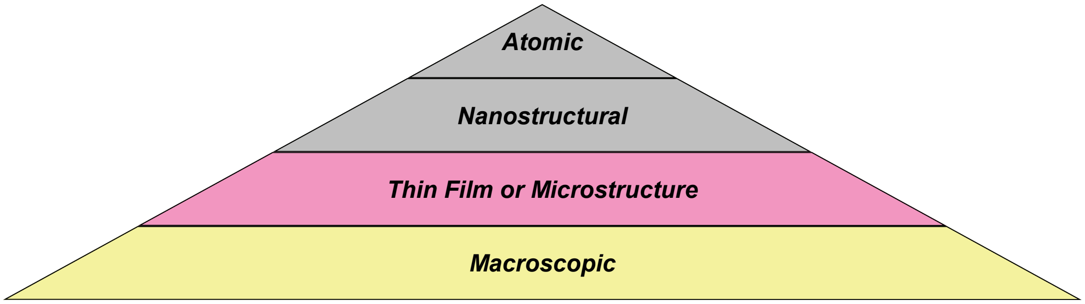

Figure ERM4 Hierarchy of Models for Emerging Research Materials

Despite recent advances, theory has many limitations that gate applicability to systems of practical interest for quantitative correlations. Current applications include equilibrium energies, density of states, reaction rates, effects of defects, and transport within nanostructures and through interfaces. At present, empirical methods can simulate up to 1,000,000 atoms and density functional theory (DFT) and quantum Monte Carlo methods can simulate up to 1000' atoms, although some researchers have demonstrated application of *ab initio*-based DFT method on a million atoms using large clusters.[273] At the quantum scale, the current applicability of available models is rather limited. Major issues that need to be addressed in the quantum models are:

1. Extension to larger scales for equilibrium calculations and understanding the temperature dependence of properties and processes. (This could be enabled by linear scaling of DFT methods or multi-scale methods)
2. Metallic systems, specifically transition and inner transition metals. These need specific functionals that could be tested with more rigorous techniques.
3. More generalized extension for band gaps. Currently, hybrid and metal functionals are being developed, which need to be thoroughly characterized.
4. Strongly correlated systems require model development to explain the interaction between spin, charge, and lattice changes for potential use in spin wave propagation. This requires quantification of the energy associated with spin switching and transport and the identification of speed limitations.
5. Extension or linking of quantum models from femtoseconds to microseconds or longer to emulate realistic synthesis and transport.

As mentioned previously, when new material properties are characterized, models must be developed to guide synthesis to further enable exploration of new structures and more complex interactions between materials. Establishment of an experimental database with results from well-characterized structures could accelerate the development of more accurate full *ab initio* and self-consistent reduced models. More quantitative material property mapping at the nanometer-scale requires development of models to probe interactions of nanostructured materials. Improved structure and property mapping for more accurate TEM, AFM, conductance AFM, Kelvin Probe AFM, magnetic force microscopy (MFM), and other new techniques could improve development of nanometer scale material models.

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