# INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

## 2007 EDITION

## FACTORY INTEGRATION

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# FACTORY INTEGRATION

Factory Integration[1] section of the ITRS focuses on integrating all the factory components needed to produce the required products efficiently in the right volumes on schedule while meeting cost targets. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, and other manufacturing productivity improvements. This in turn requires a factory that can fully integrate all other factory components. Preserving the decades-long trend of 30% per year reduction in cost per function also requires capturing all possible cost reduction opportunities. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs.

The success and market growth of semiconductors have been driven largely by continuous improvement to cost per function. Many factors have led to these productivity gains including process technology shrinks, wafer size changes, yield improvements, and manufacturing productivity. The era of non-incremental technology introductions (high-κ gate dielectric, metal gates, Cu/low-κ interconnect, etc.), complex product designs and large-scale transistor integration, and process complexity (such as System On a Chip (SOC) and System In a Package (SIP)) is making the pace of productivity improvements harder to sustain when compared with historical norms. Fab investment costs continue to increase driven both by the cost of technology as well as the desire to build larger factories to get economies of scale.

Overall Factory Integration scope addresses several challenges that threaten to slow the industry's growth, including:

1. *Integrating complex business models with complex factories*—Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high mix, and volatile market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. The factory now must integrate an even larger number of new and different equipment types and software applications to meet complex market objectives and customer requirements. High mix and low-volume product runs are making mask cost, fabrication, and factory integration extremely difficult in a market where average selling prices (ASPs) are declining. Lack of robust and fully featured and integrated software systems to manage the complexity of factory and equipment control is also adding to our challenges.
2. *Production equipment reliability, utilization, and extendibility*—Production equipment is not keeping up with availability and utilization targets, which has an enormous impact on capital and operating costs. Intrinsic equipment losses needed to be understood and reduced. The industry is unable to reuse equipment or skills effectively due to the rapid introduction of new equipment (EUV lithography) and materials (SOI, high-κ gate stack, low-κ dielectrics, etc.).
3. *Continuing 300 mm factory challenges—We have addressed several 300 mm challenges but it is necessary to continue to focus on improving and sustaining 300 mm efficiency targets such as*: 1) Cycle time improvement, 2) yield improvement, 3) 100% automated materials handling system (AMHS) systems for operational flexibility and cost improvements, 4) the ability to track and run different recipes for each wafer within a carrier for operational flexibility and 5) reduction in utilities, power consumption and emission.
4. *Post Bulk CMOS and next wafer size manufacturing paradigm*—the conversion to novel devices and transition to 450 mm wafers represent key inflection points for semiconductor manufacturing. Novel devices beyond bulk CMOS and their potential impacts to equipment and manufacturing are not well defined, but are expected to be significant. Transition to 450mm wafer provides an opportunity to improve manufacturing cost effectiveness and will be an important factor in the semiconductor industry's ability to continue realizing Moore's law.

In order to address these challenges the following fundamental semiconductor manufacturing attributes must be improved:

- Cost per unit area of silicon—manufacturing cost per unit area of silicon is a measure of productivity. The capital cost of a factory has grown significantly each year, from $50M US in the 1980s to over $3B US in 2007.[2]
- Time to ramp a factory to high-volume production with high yields—decreasing time to ramp a factory to high-volume production and high yield has more economic impact than reducing operating costs. New factories must be

[1] *Factory integration is the combination of factory operations, production equipment, facilities, material handling, factory information and control systems, and probe/test manufacturing working in a synchronized way to produce complex products profitably for a time-sensitive market.*

[2] *Strategies for determining or dealing with the upper limit of factory cost are beyond the scope of this chapter.*

built and ramped to mature production at a much faster rate as reflected in Technology Requirements tables. Existing factories must be upgraded faster without impacting ongoing production. Factory reuse and embracing green concepts are also becoming important.

- Increasing flexibility to accommodate technology and business changes—Technology advances and the globalization of manufacturing enterprises have led to a decrease in cost for electronic components. This enables new markets to open and creates the need to increase the pace of new product introduction. The flexibility to accommodate these changes in business expectations must continue to improve without significant cost impacts.

## SCOPE

Semiconductor factory extends across several manufacturing domains (Figure FAC1), and include wafer manufacturing or fabrication, chip manufacturing that involves probe/e-test, backgrind, singulation, and product manufacturing where the final package is assembled and tested. Silicon substrate manufacturing and product distribution are outside the scope of factory integration.

In order to clearly understand the integrated factory requirements and at the same time define measurable and actionable metrics, the factory integration is divided into five thrusts, or functional areas, that are required to perform semiconductor manufacturing. They are Factory Operations, Production Equipment, Material Handling, Factory Information & Control Systems, and Facilities. Factory Operations, and its associated factory business model, is a key driver of requirements and actions for the other four thrusts. Overall, these five thrusts are used to clarify how difficult challenges translate into technology requirements and potential solutions. In addition to these five thrust areas, the factory integration section also addresses the cross-cut issues and key focus areas that cut across all these five thrusts.

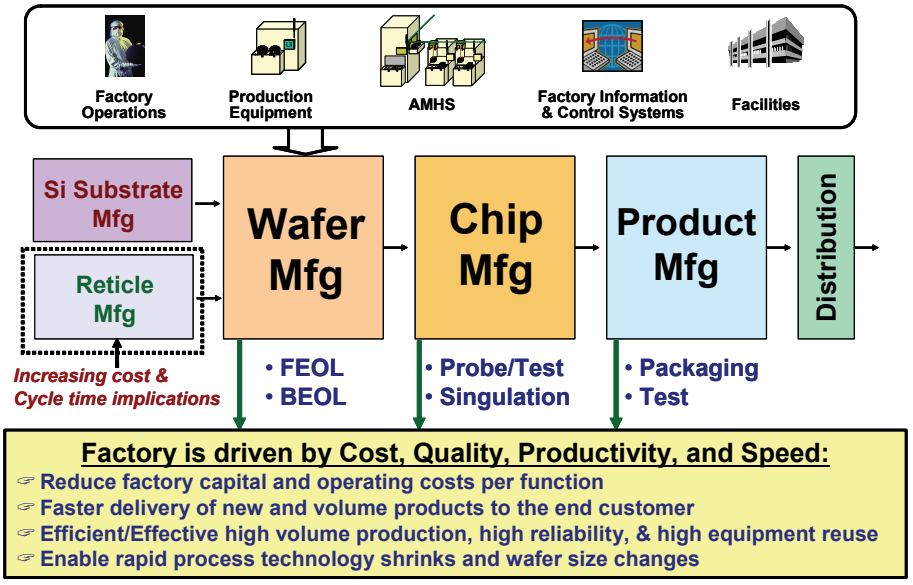



*Figure FAC1 Factory Integration Scope*

## DIFFICULT CHALLENGES

Difficult challenges associated with factory integration span multiple technology generations and cut across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry convenience to minimize disruptions to operating factories. Near-term difficult challenges for the factory include business, technical, and economic issues that must be addressed.

*Table FAC1a Factory Integration Difficult Challenges—Near-term*

| *Difficult Challenges ≥22 nm* | *Summary Of Issues* |
|---|---|
| Responding to rapidly changing, complex business requirements | Many new and co-existing business models including IDM, foundry, fabless, joint ventures, collaborations, other outsourcing, etc., need to be considered in the Factory Integration<br>Increased expectations by customers for faster delivery of new and volume products<br>Need for improve integration of the entire product design and manufacturing process<br>Faster design → prototype and pilot → volume production<br>Enhanced customer visibility into outsourced production operations<br>Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment<br>Building 30+ mask layer System on a Chip (SoC) with high-mix manufacturing as the model in response to diversified customers' requirement<br>Rapid and frequent factory plan changes driven by changing business needs<br>Ability to model factory performance to optimize output and improve cycle time for high mix factories<br>Ability to constantly adjust equipment loading to keep the factory profitable<br>Manufacturing knowledge and control information need to be shared as required among disparate factories |
| Achieving growth targets while margins are declining | Implications of rising wafer, packaging, and other materials cost on meeting cost targets<br>Meeting high factory yield much faster at startup<br>Addressing increased complexity while keeping costs in check<br>Reducing complexity and waste across the supply chain<br>Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers<br>High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs<br>Increasing dedication of masks and equipment causing manufacturing inefficiencies<br>Challenges introduced with sharing of mask sets<br>Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency |
| Managing ever increasing factory complexity | Quickly and effectively integrating rapid changes in process technologies<br>Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors<br>Comprehending increased purity requirements for process and materials<br>Need to run aluminum and copper back end in the same factory<br>Increasing number of processing steps coupled with process and product complexity<br>Need to concurrently manage new and legacy software and systems with increasingly high interdependencies<br>Explosive growth of data collection/analysis requirements driven by process and modeling needs<br>Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes |
| Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap | Process equipment not meeting availability, run rate, and utilization targets out of the box<br>Stand alone and integrated reliability for equipment and systems to keep factories operating<br>Increased impacts that single points of failure have on a highly integrated and complex factory<br>Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements<br>Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs<br>Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors<br>Small process windows and tight process targets at >45 nm (DRAM contacted half pitch)in many modules make process control increasingly difficult<br>Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems |

*Table FAC1b Factory Integration Difficult Challenges—Long-term*

| *Difficult Challenges <22 nm* | *Summary of Issues* |
|---|---|
| Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory | Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills<br>Minimizing downtime to on-going operations while converting factories to new technologies<br>Scalability implications to meet large 300 mm factory needs [40K–50K WSPM]<br>Continued need to improve both throughput and cycle time<br>Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations<br>Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability)<br>Comprehending increased purity requirements for process and materials<br>Accelerating the pace of standardization to meet industry needs |
| Meeting process requirements at 65 nm and 45 nm generations running production volumes | Small process windows and tight process targets at 32 nm generations in many modules make process control increasingly difficult<br>Complexity of integrating next generation lithography equipment into the factory<br>Overall development and volume production timelines continuing to shrink<br>Device and process complexity make the ability to trace functional problems to specific process areas difficult<br>Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals<br>Reducing the impacts of parametric variation |
| Increasing global restrictions on environmental issues | Need to meet regulations in different geographical areas<br>Need to meet technology restrictions in some countries while still meeting business needs<br>Comprehending tighter ESH/Code requirements<br>Lead free and other chemical and materials restrictions<br>New material introduction |
| Post-conventional CMOS manufacturing uncertainty | Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design<br>Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition<br>Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency<br>Need to run CMOS and post CMOS processes in the same factory |
| Emerging factory paradigm and next wafer size change | Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness.<br>Traditional strategies to scale wafers and carriers for the 450 mm wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes<br>Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost |

# TECHNOLOGY REQUIREMENTS

To achieve the primary goals listed above, we need to evaluate the technology requirements and identify potential solutions to the difficult challenges. This is accomplished in the Factory Integration by breaking up the section into the following five integrated and complementary functional areas:

- Factory Operations (FO) covers the set of policies and procedures that are used to plan monitor and control production within a factory.
- Production Equipment (PE) covers process and metrology equipment and their interfaces to other factory elements. It also focuses on addressing equipment variability losses.
- Automated Material Handling Systems (AMHS) covers transport, storage, identification, tracking, and control of direct and indirect materials.

- Factory Information and Control Systems (FICS) includes computer hardware and software, manufacturing execution and decision support systems, factory scheduling, control of equipment and material handling systems, and process control.
- Factory Facilities include the infrastructure of buildings, utilities, and monitoring systems.

Table FAC2 provides a summary of key focus areas and issues for each of the factory integration functional areas beyond 2007. The challenges stemming from Next wafer size (NWS) will be addressed in a separate table.

*Table FAC2 Key Focus Areas and Issues for FI Functional Areas Beyond 2007*

| *Functional Area* | *Key focus and issues* |
|---|---|
| Factory Operations (FO) | 1) Reduce manufacturing cycle times, 2) Improve equipment utilization, 3) Reduce losses from high mix |
| Production Equipment (PE) | 1) NPW reduction, 2) Reliability improvement, 3) Run rate (throughput) improvement, 4) Equipment variability losses. |
| Automated Material Handling Systems (AMHS) | 1) Increase throughput for traditional and unified transport, 2) Reduce average delivery times, 3) Improve reliability |
| Factory Information and Control Systems (FICS) | 1) Increase reliability, 2) Increase factory throughput and yield, 3) Reduce costs |
| Facilities | 1) Factory extendibility, 2) AMC, 3) Rapid install/qualification, 4) Reduce costs |

## FACTORY OPERATIONS

Factory operations refers to the efficient and effective application of resources and integration of other facets of manufacturing such as information and control system, material handling, equipment, and facilities in order to maximize throughput, minimize cycle time, work-in-progress (WIP) and maintain lower operating cost. Equipment metrics, particularly, run rate improvement, availability, and utilization are also included in the technology requirements table.

The Factory Operations Technology Requirements table lists the high-level production metrics and their required improvement targets through time in order for a semiconductor factory to achieve competitive performance characteristics. The factory operational metrics are cycle time per mask level, X-factor for hot lots and non-hot lots, lots per carrier, and wafer layers per day per headcount. These metrics are further segmented to differentiate between two kinds of factories: high volume, high mix and high volume, low mix. These metrics are primarily focused around 40K WSPM high-mix factories with short life cycle products. In addition, there are a set of factory ramp-up metrics—first tool move-in to first full-loop wafer out, technology-generation-to-technology-generation change over, and floor space effectiveness.

Cycle time now is gaining more importance both in high mix and low mix manufacturing. Cycle time shall have two different view “axes” from which it is to be evaluated; from utilization of the factory resources, especially production equipment utilization and from product view point.

Resource utilization viewpoint has been well studied and historically used to improve the throughput in order to maximize the profit. Product view “axis” is important for the delivery and cycle time management and control. Fab control methodology is also decisive to the cycle time.

Twelve W lot size has been added to the metrics table for cycle time and relevant metrics as a representing point for the smaller lot sizes. Because of this cycle time requirement the process tool performance is expected to be measured for 12W and 25W lot sizes to see if there is any deterioration pronounced for the small lot sizes. This would promote improvement of the tool performance in terms of cycle time and tool availability for the small lot sizes. Such improvement is also effective and applicable to low mix production characteristics.

The performance characteristics of a factory that best defines its competitive posture will depend on a number of factors. For example, there is a well-established trade-off between cycle time and asset utilization, with higher asset utilization leading to higher cycle times. Thus, each factory must balance the value of lowering cycle time for the business segment(s) in which it participates versus the cost of the lower asset utilization. Similarly, a high-mix factory will have operational characteristics and will need decision support tools that will be different than those for a factory that is low mix and high volume. Asset utilization is captured in the form of equipment utilization, availability, and capacity

degradation. Another metric, overall equipment effectiveness (OEE) is not explicitly mentioned in the operations table since the key elements of OEE namely, utilization and availability are captured in the technology tables.

Once the fundamental performance characteristics have been established for a factory, there is a continuing need for increased productivity. This increased productivity is reflected either in lower cycle times or in increased throughput for the same capacity investment. It is also essential to address average number of wafers processed before a reticle change since the high-mix factory coupled with next wafer size (such as 450 mm) wafer would demand lesser number of wafers processed between reticle changes.

These requirements are meant to provide guidance so that research can be better focused toward the innovations required to achieve these objectives. These innovations are envisioned to be in the form of new concepts, policies, models, algorithms, etc. These will be expressed in the form of software applications that would be developed and released to manufacturing. These software applications will be integrated into the overall factory information and control systems, either as decision support tools or as execution tools. These tools will help to drive factory productivity improvements to achieve Factory Operations objectives.

Another aspect that is becoming critical to factory operations is the mask operations influence on factory operations. Mask operations can be considered as one of the key components of the semiconductor supply chain that produces the mask or reticle sets that are used by the fabs. The complexity, shrinking and demand to keep die cost low influences mask manufacturing. Some of the key challenges in mask operations that need to be comprehended are: data explosions (time for OPC calculations and data preparation for mask writer; time to send and load tape-out data into mask shop data system, etc.); rising cost of E-beam; supply chain synchronization with fabs, and better process control needs.

The Factory Operations potential solutions are classified into planning decision support (DS) tools at the strategic level and tools for running the factory at the tactical or execution level. The solution components for these two levels are quite different but are essential in order to manage high-mix factories effectively. The tactical tools need quick access to transactional data whereas the DS tools need large sets of data with several analysis/reporting options. The stringent engineering requirement is driving need for more data that would be resulting in data explosion. It is critical to not only collect necessary data but also to develop intelligent analytics and algorithms to identify and use the right signals to make data driven decisions, and reuse such intelligence as models in later occasions. The factory data shall be designed in accordance to these models for usages for high data utilization efficiencies.

Demand information propagated over the factory network (Fab/sort/assembly/test) is neither accurate nor responsive, which results in poor factory and supply chain planning. Successful determination of where, when, and in what quantities the products are needed is essential for improving manufacturing productivity. The cost of capital equipment is significantly increasing and now constitutes more than 75% of wafer Fab capital cost and via depreciation a significant fraction of the fixed operating costs as well.

Reducing the impact of these increasing costs on overall wafer costs requires improvements in equipment utilization, availability, and capacity loss due to set up (for high mix), tool dedication, etc. Effective factory scheduling also plays a key role in improving equipment utilization and it also leads to improved cycle time and on-time-delivery (OTD). In order to utilize the expensive production equipment effectively, it is imperative that effective scheduling and dispatching tools be utilized. Several factors complicate Fab scheduling. These include AMHS that is not fully integrated with lot scheduling tools as well as scheduling policies that are not effectively integrated into lot scheduling tools. A real-time scheduling and dispatching tool integrated with AMHS and incorporating predictive maintenance, preventive maintenance (PM) scheduling, and resource scheduling policies are required to reduce WIP, improve OTD, and improve capacity utilization. (Refer to the Factory Operations Potential Solutions Figure FAC2.*)*.

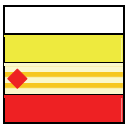
*Table FAC3a Factory Operations Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *35* | *32* | *28* | *25* |
| *Wafer Diameter (mm)* | *300* | *300* | *300* | *300* | *300* | *450* | *450* | *450* | *450* |
| *Non-hot lot (average of 94% lots)* | | | | | | | | | |
| Cycle time per mask layer (days) 25 wafer lot | 1.5 | 1.5 | 1.4 | 1.4 | 1.2 | 1.2 | 1.2 | 1.13 | 1.13 |
| Cycle time per mask layer (days) 12 wafer lot | 1 | 1 | 0.84 | 0.84 | 0.72 | 0.72 | 0.72 | 0.68 | 0.68 |
| X-Factor [1] | 3.1 | 3.1 | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 |
| *Hot lot (average top 5% of lots)* | | | | | | | | | |
| Cycle time per mask layer (days) 25 wafer lot | 0.55 | 0.55 | 0.51 | 0.51 | 0.47 | 0.47 | 0.47 | 0.44 | 0.44 |
| Cycle time per mask layer (days) 12 wafer lot | 0.50 | 0.50 | 0.42 | 0.42 | 0.36 | 0.36 | 0.36 | 0.34 | 0.34 |
| X-Factor [1] | 1.3 | 1.3 | 1.3 | 1.3 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| *Super hot lot (average top 1% of lots)* | | | | | | | | | |
| Cycle time per mask layer (days) | 0.32 | 0.32 | 0.31 | 0.31 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| High-mix capacity degradation | 8.33% | 6.67% | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| *Bottleneck equipment [2] [3]* | | | | | | | | | |
| Utilization | 92% | 92% | 94% | 94% | 94% | 94% | 94% | 94% | 94% |
| Availability | 94% | 94% | 96% | 96% | 96% | 96% | 96% | 96% | 96% |
| Wafer layers/day/head count | 61 | 61 | 67 | 67 | 73 | 73 | 73 | 81 | 81 |
| Number of lots per carrier (high mix) [4] | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple |
| *Facilities cycle time (weeks)* | | | | | | | | | |
| 1st tool to 1st full loop wafer out | 13 | 11 | 11 | 11 | 9 | 9 | 9 | 7 | 7 |
| Generation-to-generation change-over (weeks) | 12 | 12 | 11 | 11 | 10 | 10 | 10 | 9.5 | 9.5 |
| Floor space effectiveness | 1× | 1× | 1× | 1× | 1× | 1× | 1× | 1× | 1× |
| Average number of wafers between reticle changes 25 wafer lot | 30 | 25 | 20 | 20 | 20 | 20 | 20 | 15 | 15 |
| Average number of wafers between reticle changes 12 wafer lot | 15 | 13 | 10 | 10 | 10 | 10 | 10 | 8 | 8 |
| New non-product wafers (NPW) as a % of wafer starts per week | <12% | <11% | <11% | <11% | <10% | <10% | <10% | <9% | <9% |

*Table FAC3b Factory Operations Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *Wafer Diameter (mm)* | *450* | *450* | *450* | *450* | *450* | *450* | *450* |
| *Non-hot lot (average of 94% lots)* | | | | | | | |
| Cycle time per mask layer (days) 25 wafer lot | 1.13 | 1.05 | 1.05 | 1.05 | 1.05 | 1.05 | 1.05 |
| Cycle time per mask layer (days) 12 wafer lot | 0.68 | 0.63 | 0.63 | 0.63 | 0.63 | 0.63 | 0.63 |
| X-Factor [1] | 3.05 | 3 | 3 | 3 | 3 | 3 | 3 |
| *Hot lot (average top 5% of lots)* | | | | | | | |
| Cycle time per mask layer (days) 25 wafer lot | 0.44 | 0.39 | 0.39 | 0.39 | 0.39 | 0.39 | 0.39 |
| Cycle time per mask layer (days) 12 wafer lot | 0.34 | 0.32 | 0.32 | 0.32 | 0.32 | 0.32 | 0.32 |
| X-Factor [1] | 1.2 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 |
| *Super hot lot (average top 1% of lots)* | | | | | | | |
| Cycle time per mask layer (days) | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| High-mix capacity degradation | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| *Bottleneck equipment [2] [3]* | | | | | | | |
| Utilization | 94% | 94% | 94% | 94% | 94% | 94% | 94% |
| Availability | 96% | 96% | 96% | 96% | 96% | 96% | 96% |
| Wafer layers/day/head count | 81 | 89 | 89 | 89 | 89 | 89 | 89 |
| Number of lots per carrier (high mix) [4] | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple | Multiple |
| *Facilities cycle time (weeks)* | | | | | | | |
| 1st tool to 1st full loop wafer out | 7 | 5 | 5 | 5 | 5 | 5 | 5 |
| Generation-to-generation change-over (weeks) | 9.5 | 9 | 9 | 9 | 9 | 9 | 9 |
| Floor space effectiveness | 1× | 1× | 1× | 1× | 1× | 1× | 1× |
| Average number of wafers between reticle changes 25 wafer lot | 15 | 13 | 13 | 13 | 13 | 13 | 13 |
| Average number of wafers between reticle changes 12 wafer lot | 8 | 7 | 7 | 7 | 7 | 7 | 7 |
| New non-product wafers (NPW) as a % of wafer starts per week | <9% | <9% | <9% | <9% | <9% | <9% | <9% |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*



*Notes for Tables FAC3a and b:*

*[1] X-factor is shown for continuous improvement. Actual X-Factor values will depend heavily on raw process time for a given process technology or generation.*

*[2] A bottleneck tool usually refers to a lithography tool.*

*[3] Utilization and Availability are shown for continuous improvement.*

*[4] High mix is defined as the followings:*

- *Running > three technology generation concurrently in the same Fab*
- *Running > ten process flows within the same technology generation*
- *Running > 50 products concurrently through the Fab*
- *Many of small lots of 1–10 wafers in size*
- *Running an average of < 50 wafers between Reticle changes for each lithography expose equipment*
- *Lot starts are based on customer orders. There is a daily variation in the number of lots you start with different products and process flows*
- *At least five large volume products (product flows) with no one product having >50% of production volume*

*Explanation of Items for Factory Operations Requirements*

| *Item* | *Explanation* |
|---|---|
| Factory cycle time per mask layer (non-hot lot) | A key metric of time to money and measure of total time to process a lot cycle time per mask layer. For example, if a process has 20 masking layers, and cycle time per mask layer is 1.5, then total factory (fabrication) cycle time based on 25 wafers per lot is: 20 × 1.5 = 30 days. Cycle time for a 12 wafer lot would be calculated accordingly. |
| Factory cycle time per mask layer (hot lot) | Same definition as of above. Factories typically prioritize these lots over non-hot lots. As a result, the cycle time for hot lots is < 50% of non-hot lots. Assume full lot size (either 25 wafers per lot or 12 wafers per lot). New product lots can be processed as hot lots. |

| *Item* | *Explanation* |
|---|---|
| Factory cycle time per mask layer (super-hot lot) | Assume ~ 5 wafers per lot. Factories typically prioritize these lots over conventional lots, hold tools downstream to rapidly move them through the process flow and reduce sampling rates. As a result, the cycle time for super hot lots are shorter than hot lots. |
| X-factor [1] | X-factor is the total cycle time (queue time + hold time + raw process time + travel time) divided by the raw process time (RPT). Raw process time for a lot at a tool is the time it takes to process a lot on the tool. Generally this time will be from when the tool starts to process the lot (and thus cannot be moved to another tool for processing) until the lot is finished and can be moved to the next operation. Raw process time for a technology is the sum of the raw process times for each of the tools in the processes in the technology plus the total travel time. Raw process time is not shown in the technology table since X factor and cycle time per mask layers are shown.<br>The relationship is: cycle time = raw process time × X-factor<br>Assume current cycle time is 1.6 days/mask level and the X-factor for normal lots is 3.2 at 80% utilization. Thus RPT for normal lots = 1.6/3.2 = 0.5<br>Assume same RPT for normal and hot lots. X-factor for hot lots is determined by "last-in-first-out" priority |
| High-mix capacity degradation | The penalty paid by factory operations in terms of lost capacity due to high mix (measured in %). This capacity loss is caused by reduced batch sizes, increased set ups, etc. This is the average for all tool sets in the line. Degradation increases from 5% (low mix, 25 wafers/FOUP, change recipe/setup every ten lots, single product on a wafer) to maximum. Of 15% (high-mix, <25 wafers/FOUP, change recipe/setup for every FOUP, multiple product in a lot). This metric impact the utilization of effective capacity, which is best, defined as being (1–(Idle No WIP)).<br>Idle-No WIP is the fraction of a tool's capacity that is idle when the tool is up and there is no WIP either waiting to be run on the tool or in transit to the tool. In some cases, No operator can also contribute to utilization of effective capacity. |
| Bottleneck equipment utilization and availability [2] [3] | Availability is defined in SEMI E10[3] as "the probability that the equipment will be in a condition to perform its intended function when required."<br>Utilization is defined in SEMI E10 as "the percentage of time the equipment is performing its intended function during a specified time period." Availability includes setup, idle and processing time, utilization is considered as time directly adding value of constraint equipment (usually lithography tools) measured in % without sacrificing cycle time. Constraint equipment utilization (normally lithography) is the pulse of the Fab and usually determines the output capacity. |
| Wafer layers/day/head count | Measure of productivity that includes equipment output and direct labor staffing.<br>Equation = total wafer processed per day in the factory × number of lithography mask layers/total number of direct labor employees per day. |
| Number of lots per carrier (high mix) [4] | The number of lots in each carrier that need to be tracked, monitored, and processed. For high-mix factories, the number of wafers can be <25 per lot and the production equipment must be able to run a different recipe and/or parameters for each wafer within the carrier. It also requires the factory information and control system to be able to track, monitor, and control the wafer at each point the factory and within the equipment. The factory information and control system must have the ability to drive the production equipment to run different recipes and/or parameters for each wafer. Multiple lots per carrier mean more than one product lot. High mix is at least five large volume products (product flows) with no one product has >50% of production volume. |
| Time to 1st wafer out time (weeks)<br>–1st tool move-in to 1st full loop wafer out | A key metric of new factory ramp-up time. This is the time elapsed in weeks from first tool move-in to first full loop wafer out. |
| Generation-to-generation change-over (weeks) | The time in weeks for a new product or process to be implemented in a working factory (production equipment move-in to first lot out). About 80% of the current equipment is reused and 20% is new. Equipment already in place or available and may need to be qualified. Furnace and wet process equipment are not replaced. Not serial number 1 equipment |
| Floor space effectiveness | This is a measure of equipment installation density in the clean room, and drives the requirement for the smallest footprint and the fastest run rate for production equipment.<br>Equation = (Number of processing steps in the Fab × WSPM/ (floor space area × 30 days).<br>For every major generation, one additional metal layer is added, and assuming a 4% increased run-rate improvement each year (by reduced processing time per wafer), the best that can be mathematically achieved is getting the same output per square meters of clean room for each new generation. |
| New non-product wafers (NPW) as a % of wafer starts per week | Ratio of new non-production wafer consumption divided by total production wafer started for the same period. Typical non-product wafers include test wafers, monitor wafers, calibration wafers, dummy wafers. |
| Average number of wafers between reticle changes | This is a measure of how efficiently high-product mix can be handled in the factory.<br>As the metric indicates, it is the average number of wafers processed before a reticle is changed. |

*FOUP—front opening unified pod*

[3] *SEMI E10-0699E: Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM).*

## PRODUCTION EQUIPMENT

The scope of the production equipment section includes all process and metrology equipment in the factory. Also included are tool embedded controllers, front-end module (EFEM) and load ports, carrier, and wafer handling, software and firmware interfaces to host systems, and all facilities interfaces of the equipment. Equipment metrics, particularly, availability and utilization, are also included in the technology requirements table.

Effective design and control of production equipment is central to controlling the cost of processing each unit area of silicon, and throughput improvements as measured in terms of processing time per wafer are an expected attribute of typical continuous improvement efforts. The industry's growth rate will not be sustainable in the future if increasing capitalization cost trends continue without significant improvement in productivity. There are several factors that impact productivity of the equipment. They include the following:

1. Reducing intrinsic setup time that comes with high-mix factories through quick turn around setup options
2. Improving equipment design to reduce losses from high product mixes (i.e., set-up time reduction or elimination), and reducing the percentage of non-value added time associated with equipment operation
3. Finding breakthrough solutions for increasing equipment reliability, availability, and utilization.
4. Reducing variation within and between equipment and attaining chamber and tool matching.
5. Extending equipment lifetime to support multiple technology generations.
6. Achieving more effective use of utilities and consumables, including reduction of non-product wafers, while simultaneously reducing environmental impacts.
7. Reducing "relative or normalized equipment capital cost" (rate at which equipment cost increases vis-à-vis requirements for process capability) by speeding up the processing rate. This will drive reduced cost of ownership.

The Production Equipment potential solutions are prioritized towards attaining the improvements listed above. End-user understanding and analysis of equipment non-value added time, leading to targeted areas for improvement in intrinsic setup time reduction and other non-value added operations, can be realized through the development, standardization, and implementation of reliable and comprehensive equipment engineering data control systems. Improvements in the flexibility and agility of the equipment will also reduce cycle time and increase tool utilization. Reliability and utilization improvements can also be achieved by innovative solutions in the area of *in-situ* monitoring, advance process control capability, design for manufacturing, smarter embedded controllers, self-diagnostics, remote diagnostic capability, and single-wafer level tracking and control. More energy-efficient equipment designs are achieved through the use of higher efficiency power distributions systems within the tool, more efficient tool-heat-load removal methods, and optimized recycling and reuse of water. An additional emerging area of opportunity for reducing utilities consumption is the concept of a "smart idle" or "sleep mode" operational model for equipment. Another high priority area is finding ways to extend the life of the equipment to support multiple technology generations. Other important areas are finding innovative solutions for ramp-up cycle time reduction and spares cost reduction. An additional emerging focus area requiring innovate solutions is the preventive control of Airborne Molecular Contamination (AMC). Lastly, efficient and cost-effective equipment development will be a critical milestone in the industry transition to the next wafer processing size. (See the Production Equipment Potential Solutions Figure FAC3.)

*Table FAC4a Production Equipment Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *35* | *32* | *28* | *25* |
| *Wafer Diameter (mm)* | *300* | *300* | *300* | *300* | *300* | *450* | *450* | *450* | *450* |
| Overall NPW activities versus production wafers activities | 7% | 7% | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| % capital equipment reused from previous node | >90% | >90% | >90% | >90% | >90% | >90% | Limited | Limited | >70% |
| Wafer edge exclusion | 2 | 2 | 2 | 2 | 2 | 1.5mm | 1.5mm | 1.5mm | 1.5mm |
| Lithography Equipment Qualification Duration | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks |
| Process equipment availability (A80) | >92% | >94% | >95% | >95% | >95% | >95% | >95% | >95% | >95% |
| Metrology equipment availability (A80) | 96% | >96% | >97% | >98% | >98% | >98% | >98% | >98% | >98% |
| Equipment-induced non-value added time as a % of total processing time (high mix) | 10% | 10% | 8% | 8% | 8% | 8% | 8% | 6% | 6% |
| Ability to run different recipes and parameters for each wafer | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| 248 nm lithography scanner productivity (wafers outs per week per tool) | 7700 | 7700 | 8000 | 8000 | 8000 | 8000 | 8000 | 8000 | 8000 |
| 193 nm lithography scanner productivity (wafers outs per week per tool) | 5600 | 5600 | 6000 | 6000 | 6000 | 6000 | 6300 | 6300 | 6500 |
| Maximum allowed electrostatic field on wafer and mask surfaces (V/cm) | 70 | 63 | 55 | 50 | 44 | 38 | 35 | 31 | 28 |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

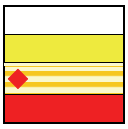


*Table FAC4b Production Equipment Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *Wafer Diameter (mm)* | *450* | *450* | *450* | *450* | *450* | *450* | *450* |
| Overall NPW activities versus production wafers activities | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| % capital equipment reused from previous node | >70% | >70% | >70% | >70% | >70% | >70% | >70% |
| Wafer edge exclusion | 1.5mm | 1.5mm | 1.5mm | 1.5mm | 1.5mm | 1.5mm | 1.5mm |
| Lithography Equipment Qualification Duration | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks | 4 wks |
| Process equipment availability (A80) | >95% | >95% | >95% | >95% | >95% | >95% | >95% |
| Metrology equipment availability (A80) | >98% | >98% | >98% | >98% | >98% | >98% | >98% |
| Equipment-induced non-value added time as a % of total processing time (high mix) | 6% | 6% | 4% | 4% | 4% | 4% | 4% |
| Ability to run different recipes and parameters for each wafer | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| 248 nm lithography scanner productivity (wafers outs per week per tool) | 8000 | 8000 | 8000 | 8000 | 8000 | 8000 | 8000 |
| 193 nm lithography scanner productivity (wafers outs per week per tool) | 6500 | 6500 | 6500 | 6500 | 6500 | 6500 | 6500 |
| Maximum allowed electrostatic field on wafer and mask surfaces (V/cm) | 25 | 22 | 20 | 18 | 15 | 13 | 10 |

*Explanation of Items for Production Equipment Requirements*

| *Item* | *Explanation* |
|---|---|
| Overall NPW activities versus production wafers activities | Total equipment-driven non-production wafers processed on equipment divided by total production wafers processed on equipment, for the same time period, assuming that equipment is running at designed availability and planned utilization rates. Typical non-production wafers include test wafers, monitor wafers, calibration wafers, test fire wafers. The requirement as shown is for all production (non-metrology) equipment. |
| Percent capital equipment reused from previous generation | Percent of capital (production) equipment quantity that is reused from generation N to N+1. Example: if X number of production equipment of generation N can be reused for generation N+1 and the total number of production equipment for generation N+1 is Y, then equipment reuse % is defined as X/Y. |
| Wafer edge exclusion | Dimension in millimeters measured from wafer edge that is not used for printing saleable chips. Includes front and rear sides of wafer. |
| Lithography Equipment Qualification Duration | The time needed for a tool to ramp up to full operation, from completion of physical installation. This requirement is for repeat installation instances of existing equipment types. |
| Process availability ($A_{80}$) | Availability is defined as 100% minus (scheduled downtime% + unscheduled downtime%). The metric in the table is the requirement for an 80% confidence (i.e., equipment is at or above this value 80% of the time) for each individual process (non-metrology) equipment, over a period of one week of 7 × 24 operations. Scheduled and unscheduled downtimes are defined in SEMI E10. Note: The value shown in the process equipment table is the minimum A80 value for all equipment – please refer to the Factory Operations requirements table for availability requirements specific to factory bottleneck equipment. |
| Metrology availability ($A_{80}$) | Availability is defined as 100% minus (scheduled downtime% + unscheduled downtime%). The metric in the table is the requirement for an 80% confidence (i.e., equipment is at or above this value 80% of the time) for each individual metrology equipment, over a period of one week of 7 × 24 operations. Scheduled and unscheduled downtimes are defined in SEMI E10 |
| Equipment-induced non-value added time as a percent of total processing time (high mix environment) | The total time associated with processing each lot that is not directly processing wafers, as a percent of overall processing time. Examples of non-value added time include first wafer delays, equipment configuration changes related to product or layer changes of lots being processed, recipe changes, intra-equipment wafer transport, and impacts of equipment transition from idle state to processing. The requirement as defined is applicable to all equipment types, and assumes that equipment is running at specific availability and without unplanned interruption. |
| Ability to run different recipes and parameters for each wafer | Ability for production equipment to run a different recipe and/or parameters for each wafer within a carrier. This facilitates the ability to have multiple lots per carrier. Base requirements also include the ability to track, monitor, and control the wafer at each point the factory or within the equipment. For production equipment, it impacts the extent of "recipe cascading" that enables equipment to run in a continuous (non-stop) mode between lots in the same carrier and between sequential carriers. |
| 248 nm lithography scanner productivity (wafers outs per week) | The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 248 nm scanners in the Fab. |
| 193 nm lithography scanner productivity (wafers outs per week) | The average number of good photo wafer alignments performed per machine per work day, considering only photo wafer alignments performed on 193 nm scanners in the Fab. |
| Maximum allowed electrostatic field on wafer and mask surfaces (V/cm) | Wafer and mask surface electric fields measured when they are removed from their carriers. Refer SEMI standards E78[4] and E43[5] for measurement methods. |

## MATERIAL HANDLING SYSTEMS

Ergonomic and safety issues coupled with the need for efficient and rapid material transport are the major drivers in defining material handling systems for the 300 mm wafer generation and beyond. The automated material handling systems (AMHS) must have acceptable Return on Investment (ROI) and must interface directly with all inline (i.e., used in normal process flow) production equipment. With the increase in 300 mm production equipment size, the utilization of floor space in the factory must improve. Solutions to provide short lead and install times, and better utilization of floor space through integration of process and metrology equipment must be developed.

The potential solutions table is based on the premise that as demands on the material handling system continues to increase, the drive toward combining interbay and intrabay transport function into one integrated capability, known as a direct or tool-to-tool direct transport system, will be a reality. This does not imply overall one system or even one system

[4] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*
[5] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

from one supplier. The system may be composed of interoperable sub-systems from multiple (best of breed) suppliers and will have the ability to avoid sending lots through stockers.

For efficient production in such an environment, there will be a need to integrate WIP scheduling and dispatching systems with storage and transport systems with the goal to reduce product processing cycle time, increase productivity of process tools, reduce storage requirements and reduce total movement requirements. The priority for direct delivery will be as follows:

1. Super hot lots (< 1% of WIP) and regular hot lots (~5% of WIP).
2. Ensure bottleneck production equipment is always busy.
3. Utilize direct tool-to-tool moves for gating metrology process steps, send-ahead wafers and other lots opportunistically.

Potential solutions for reticle transport systems must not negatively impact the lithography equipment's footprint, run rate, and ease of installation or de-installation. The adoption of automated reticle transport systems by IC makers will depend on the business model employed at the factory.

Throughput must be increased substantially and achieved with reduced delivery time. Furthermore, the material handling system needs to be designed so that it can accommodate the extendibility, flexibility, and scalability demands on the factory. Need to investigate the potential impact of high mix operations and smaller lot sizes. Also need to investigate the potential impact of increasingly larger factory sizes that require AMHS transport between multiple buildings and floors.

Initial discussions for the 450 mm have begun and initial concepts for carrier capacity have implications on AMHS that needs to be researched over the next few years and potentially developed/qualified by 2012. The trade off between lot size and MPH increase needs to be evaluated. The AMHS design may have to be revisited along with investigation into whether the wafer transport/storage (near tool) will be within the scope of the AMHS (i.e., EFEM, shared EFEM, on-tool storage). Other items that will impact AMHS design will be the 450 mm factory size, factory layout, AMC needs and factory throughput requirements (See Material Handling Potential Solutions Figure FAC4).

*Table FAC5a Material Handling Systems Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *35* | *32* | *28* | *25* |
| *Wafer Diameter (mm)* | *300* | *300* | *300* | *300* | *300* | *450* | *450* | *450* | *450* |
| Transport E-MTTR (minutes) per SEMI E10 | 10 | 10 | 10 | 10 | 10 | 5 | 5 | 5 | 5 |
| Storage E-MTTR (minutes) per SEMI E10 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 15 |
| Transport MMBF | 15,000 | 25,000 | 25,000 | 35,000 | 35,000 | 45,000 | 45,000 | 45,000 | 55,000 |
| Storage MCBF | 60,000 | 60,000 | 60,000 | 60,000 | 60,000 | 70,000 | 70,000 | 70,000 | 80,000 |
| *Peak system throughput (40K WSPM)* | | | | | | | | | |
| Interbay transport (moves/hour) | 2538 | 2626 | 2713 | 2800 | 2891 | 2983 | 3074 | 3112 | 3150 |
| Intrabay transport (moves/hour) — high throughput bay | 277 | 288 | 300 | 311 | 324 | 337 | 350 | 365 | 379 |
| Transport (moves/hour)—unified system | 5512 | 5701 | 5891 | 6080 | 6220 | 6359 | 6499 | 6579 | 6659 |
| Stocker cycle time (seconds) (100 bin capacity) | 12 | 12 | 12 | 12 | 12 | 10 | 10 | 10 | 10 |
| Average delivery time (minutes) | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| Peak delivery time (minutes) | 12 | 12 | 12 | 10 | 10 | 10 | 10 | 10 | 10 |
| Hot lot average delivery time (minutes) | 4 | 3 | 3 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMHS lead time (weeks) | 12 | 12 | 12 | <8 | <8 | <8 | <8 | <8 | <8 |
| AMHS install time (weeks) | 24 | 24 | 24 | <10 | <10 | <10 | <10 | <10 | <10 |
| Downtime to extend system capacity when previously planned (minutes) | 15 | 15 | 15 | 10 | 10 | 10 | 10 | 10 | 5 |
| Time required to integrate process tools to AMHS (minutes per LP) | 15 | 12 | 12 | 10 | 10 | 5 | 5 | 5 | 5 |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

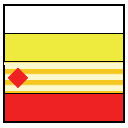


*Table FAC5b Material Handling Systems Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *Wafer Diameter (mm)* | *450* | *450* | *450* | *450* | *450* | *450* | *450* |
| Transport E-MTTR (minutes) per SEMI E10 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| Storage E-MTTR (minutes) per SEMI E10 | 15 | 15 | 10 | 10 | 10 | 10 | 10 |
| Transport MMBF | 55,000 | 55,000 | 65,000 | 65,000 | 65,000 | 65,000 | 65,000 |
| Storage MCBF | 80,000 | 80,000 | 100,000 | 100,000 | 100,000 | 100,000 | 100,000 |
| *Peak system throughput (40K WSPM)* | | | | | | | |
| Interbay transport (moves/hour) | 3188 | 3285 | 3383 | 3480 | 3520 | 3560 | 3600 |
| Intrabay transport (moves/hour) — high throughput bay | 394 | 410 | 427 | 443 | 449 | 455 | 461 |
| Transport (moves/hour)—unified system | 6740 | 6879 | 7019 | 7159 | 7241 | 7323 | 7406 |
| Stocker cycle time (seconds) (100 bin capacity) | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| Average delivery time (minutes) | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| Peak delivery time (minutes) | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| Hot lot average delivery time (minutes) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMHS lead time (weeks) | <8 | <8 | <8 | <8 | <8 | <8 | <8 |
| AMHS install time (weeks) | <10 | <10 | <10 | <10 | <10 | <10 | <10 |
| Downtime to extend system capacity when previously planned (minutes) | 5 | 5 | 5 | 5 | 0 | 0 | 0 |
| Time required to integrate process tools to AMHS (minutes per LP) | 5 | 5 | 5 | 5 | 5 | 5 | 5 |

*Explanation of Items for Material Handling Systems Requirements*

| *Item* | *Explanation* |
|---|---|
| Transport E-MTTR (min per SEMI E10) | Mean time to repair equipment-related failures (AMHS Transport); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.<br>Notes: Refers to unscheduled, supplier dependent failures. Includes interbay and intrabay transport systems. Offline repair of components is not included in this time. Includes embedded software control systems (transport controllers). Does not include storage AMHS equipment or errors induced by the storage equipment. Does not include load port, FOUP carrier, or MES level software issues. Does not include reticle system. |
| Storage E-MTTR (min per SEMI E10) | Mean time to repair equipment-related failures (AMHS Storage); the average time to correct an equipment-related failure and return the equipment to a condition where it can perform its intended function; the sum of all equipment-related failure time (elapsed time, not necessarily total man hours) incurred during a specified time period (including equipment and process test time, but not maintenance delay downtime), divided by the number of equipment-related failures during that period.<br>Notes: Refers to unscheduled, supplier dependent failures. Includes storage equipment load ports and embedded software. Does not include interbay or intrabay transport or incidents induced by these errors. Does not include FOUP carrier or MES level software issues. Does not include reticle system. |
| Transport MMBF (mean move between failure) | Average number cycles (delivery from point A to point B) made by AMHS interbay or intrabay transport equipment before a person has to intervene to fix a failure. Number of transport moves / Number of supplier dependent unscheduled failures. Reference transport MPH definition for details on move. |
| Storage MCBF (mean cycle between failure) | Average number cycles (delivery from point A to point B) made by AMHS storage equipment before a person has to intervene to fix a failure. Number of storage cycles / Number of supplier dependent unscheduled failures per quarter. Reference cycle time definition for details on stocker cycle. |
| Interbay transport (moves/hour) | Number of material handling moves per hour performed by the interbay transport system. An interbay transport move is defined as a carrier move from the loading of an interbay system at a stocker interbay port to the unloading of the same load at the destination stocker. Moves are counted by the host (MCS). |
| Intrabay transport (moves/hour) | Number of material handling moves per hour performed by an intrabay transport loop. An intrabay transport move is defined as a carrier move between loadports (between stocker ports and production equipment load port, between two production equipment load ports). Moves are counted by the host (MCS). |
| Tool-to-Tool Direct transport (moves/hour) – Unified system | A transport move is defined as a transfer of a carrier between any two loadports (stocker, process tool or transfer point between transport systems). Note that stocker robot moves from/to load ports are not assumed concurrent with nor included in system throughput moves. Moves are counted by the Host (MCS). |

| *Item* | *Explanation* |
|---|---|
| Stocker cycle time (seconds) (100 bin capacity) | Stocker cycle time is defined as the time (in seconds) from when the Host(MCS) issues the move command to the time the stocker signals completion with the move complete command to the host. The physical motion is the stocker internal robot moving to a carrier at a port or storage bin, picking up the carrier, and delivering it to another port or storage bin within the same stocker. Stocker cycle time shall be determined as the average of several different types of moves over a period of time. The moves should include all ports and all shelf locations. Each move needs to alternate between different carriers. The maximum MCS communication time is assumed to be 1 second. |
| Average delivery time (minutes) | The time begins at the request for carrier movement from the MES and ends when the carrier arrives at the load port of the receiving equipment. |
| Peak delivery time (minutes) | Peak delivery time is considered the peak performance capability defined as the average delivery time plus two standard deviations. |
| Hot lot average delivery time (min) | Reference definition for average delivery time. Refer to the Factory Operations section for further details on hot lots. |
| AMHS lead time (weeks) | Time elapsed, in weeks, between when a purchase order has been placed for a material handling system until the time the first shipment is FOB at supplier's dock. This assumes that at the time of PO placement the equipment configuration is fixed. This lead time should not be affected by market demand on supplier. |
| AMHS install time (weeks) | Time elapsed, in weeks, between when the first component of the system is moved in from the dock until the final component is fully installed, started up, and tested to meet full designed throughput capability. Assume new factory and uninterrupted installation of the material handling system (assume no facility, MCS or tool delays). Based on 20K WSPM fab of approximately 200 meters by 80 meters, with 15–20 short bays. Does not include reticle systems. |
| Downtime to extend system capacity when previously planned (minutes) | Impact to material handling system in terms of downtime, in minutes, of the material handling system, required for making connections to system track extensions or a new storage when previsions for this expansion were incorporated in the original design. |
| Time required to integrate process tools to AMHS (minutes per LP) | The downtime to the transport system when a process tool is integrated to the AMHS. Addition of tool occurs on a track with existing vehicle traffic (no bypass units around tools). Assume tool is placed correctly and physical tool move in does not impact the AMHS. System not stopped for PIO install (tool side). Time includes: hardware install on track, teaching LP, software updates, and delivery testing. Scope ends when all vehicles have capability to deliver to new LP. |

## FACTORY INFORMATION AND CONTROL SYSTEMS

The scope of Factory Information and Control Systems (FICS) includes computer hardware and software, manufacturing execution and decision support systems, factory scheduling, control of equipment and material handling systems, and process control. FICS serves as an essential infrastructure and technology enabler to a number of critical functional areas addressed by the ITRS; including Yield, Factory Operations, Production Equipment, and Material Handling.

Yield improvement will rely heavily on FICS solutions. Process Control Systems (PCS) which utilize Advanced Process Control (APC) technologies including Run-to-run (R2R) control, Fault Detection (FD), Fault Classification (FC), Fault Prediction (FP) and Statistical Process Control (SPC) will become more pervasive and an integral part of FICS solutions. Highly integrated PCS solutions will enable yield and process capability improvement, while reducing cycle time, ramp-up (re)qualification time, scheduled and unscheduled downtime, non-product wafers, scrap, and rework levels. R2R control at the wafer and increasingly the sub-wafer level will utilize virtual metrology and efficiently adapt to product changes, maintenance events, and missing data. Module and cross-module control solutions such as litho-to-etch CD control will become more prominent and R2R control capabilities will be linked to fab-level parameter targets such as yield, throughput, and electrical characteristics. Fault Detection systems will continue to trigger at recipe step boundaries but as equipment data sampling rates increase real-time alarming will see greater utilization and also provide input for virtual metrology systems tied to R2R control. Fault Classification and Fault Prediction can reduce problem resolution time and the severity of process excursions but widespread use will evolve slowly due to technology and standards hurdles. SPC is a mature technology with its current use rate and domain space continuing.

Production Equipment and Factory Operations will depend on the FICS infrastructure and applications to drive continual improvements to equipment performance and eliminate idle time. FICS systems utilizing highly integrated APC capabilities will enable increased data collection and analysis, monitoring of equipment health, remote diagnostic capabilities, prediction of future failures and equipment reliability improvement by equipment suppliers to minimize unscheduled equipment downtime. The FICS will provide collaborative integration between APC, manufacturing execution system (MES), equipment performance tracking (EPT), factory scheduler/dispatcher, and the automated material handling system (AMHS). This level of system integration is required to drive ensure timely material delivery maximizing equipment utilization and will be enabled by event-driven, reconfigurable supervisory control capabilities at the heart of the FICS, common data warehouse and data models, adoption of Interface 'B' and associated standards for application integration, proliferation of networks for control diagnostics and safety signals across the fab. Innovative collaborative solutions that are expected to emerge include, FD + R2R control + scheduling/dispatch, FD + maintenance

management, FD utilized as a health monitor for other systems such as R2R control, virtual metrology techniques utilized to predict higher level parameters such as line yield, FD utilized to enhance safety information and vise versa.

Predictable delivery of the right material, lot, and wafer at the right time is becoming increasingly important and critical to meeting cycle time improvements from Factory Operations. Higher product mix, smaller or variable lot sizes, time consuming setup times, recipe changes, and equipment constraints will impact the processing time necessary to maintain a high level of equipment utilization and achieve throughput targets. Factories must be able to adjust schedules and dispatching schemes rapidly to quickly respond to unexpected equipment downs or product scrap to maximize productivity and maintain target production rates and production times of high priority (hot) lots. Scheduling components will be required to produce and re-configure schedules based on data that is gathered from FICS applications throughout the factory enabling predictive vs. reactive scheduling capabilities. This provides the capability for optimization models to include impacts of operational or configuration changes to other FICS applications such as maintenance management, transport management, process control, and yield management. Whether scheduling is done in real-time or run as a short-term batch process the objective is to make the best choice of what to process looking beyond the boundaries of a single tool or cluster tool. With a global view of factory activity the scheduling component can make decisions beyond a small area in the factory. The effect will be greater factory utilization, higher throughput, and reduced cycle time variability.

Increasing levels of collaborative integration and exchange of data between key FICS system components, smaller lot sizes, and tighter process windows will lead to increased message and data load that must be managed by the FICS. Production equipment will be providing increased volumes of data: sensor data required for fault detection, advanced process control data, and tool performance data; including critical equipment actuators such as mass flow, pressure, and temperature controllers. The FICS must be scalable to accommodate increasing data rates and manage the collection, storage, and retrieval of this increase in data collection. While distributed systems are not novel; FICS architectures will increasingly distribute data and applications below the factory level. Distributed data and applications will decrease factory bandwidth competition and enhance the FICS ability to filter through large quantities of data, to identify the specific set of information required to make decisions for factory operation and business-level decisions. Integration of FICS applications with business-level software systems provides accurate factory floor data for supply management, and improved product tracking. Potential solutions will require the standardization of technologies (*e.g.*, SOAP / XML) that enable this level of integration.

Achieving these FICS requirements will necessitate alignment to industry standards for data acquisition, data interchange, and recipe management. Specific tool, supplier, or manufacturing-defined proprietary interfaces lead to custom solutions which increase implementation time and cost to both the IC manufacturer and the FICS supplier. New standards will be required to support agile manufacturing and process control initiatives. Time to develop these new standards must be decreased, through collaboration between IC makers and FICS suppliers. Lead time for FICS conformance to standards will need to decrease through parallel development of standardized FICS with development of new standards, to ensure that standards-based FICS applications are available to meet factory requirements. ITRS factory and university groups will need to conduct research to determine time to develop and integrate factory-wide applications and control systems applications, and identify additional opportunities for improvement. Ultimately, the improved time-to-market for standards-compliant applications will reduce time and cost of integration, allowing IC makers and suppliers to focus on improved capabilities rather than customized integration, and decreasing the risk introduced with integrating new applications into an existing factory.

The increasing reliance of the factory on the FICS infrastructure will continue to drive increased factory system complexity. There will be increased attention to maintaining the gains to overall factory system availability and to further decreasing the occurrence of full fab downtime incidents caused by a failure of a single, mission critical application. Mission critical FICS components, both software and hardware, must provide fault tolerant solutions that eliminates unscheduled factory system failures as well as scheduled downtime to install or upgrade. Potential solutions include software applications and databases that are capable of dynamic upgrades, software applications that can monitor health of factory systems and that can induce load-balancing, and fault tolerant computer systems with transparent hardware switching for failovers.

Cyber security continues to remain a high priority from the factory operations perspective. Cyber attacks have become more sophisticated and well-integrated with software. Within the last two to three years, IC manufacturers have greatly matured in handling cyber security and have effectively integrated cyber security methods into their day to day standard operating procedures to the extent that there are has been generally no downtime from cyber security incidents. Cyber security guidelines for were first published by ISMI in March 2005 documenting available methods for cyber security. An update to these guidelines has been published where the focus has shifted to publication of use cases associated with different methods of cyber security. The guidelines clearly show the diverse strategies employed to counter cyber attacks. With cyber security posing less of a threat to semiconductor manufacturing, the focus is turning to protecting intellectual

property (IP) within the equipment. Semiconductor equipment is now well integrated into the FICS infrastructure with engineers and technicians now managing and servicing the equipment over the network. Equipment contains IP both for IC manufacturers and suppliers. Ensuring IP protection is critical to overall financial success in an environment where there is a significant amount of operations-level overlap.

As shown in Table FAC6, increased reliance on factory information and control systems places greater emphasis on system availability. Increased factory complexity leads to increased integration of factory information and control systems. Because of this, there will be added attention to decreasing the occurrence of full fab downtime incidents caused by a failure of a single application. Furthermore, scheduled downtime to install or upgrade mission critical systems and databases must have minimal impact on the factory operations. Potential solutions include software applications and databases that are capable of dynamic upgrades, software applications that can monitor health of factory systems and that can induce load-balancing, and fault tolerant computer systems with transparent hardware switching for failovers. FICS potential solutions will also focus on providing integrated data for solving cross-cut issues to improve wafer cost, yield, and productivity.

*Table FAC6a Factory Information and Control Systems Technology Requirements—Near-term Years*

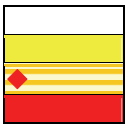
| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *35* | *32* | *28* | *25* |
| *Wafer Diameter (mm)* | *300* | *300* | *300* | *300* | *300* | *300* | *450* | *450* | *450* |
| Availability of mission critical applications (% per year) | **>99.99%** | **>99.99%** | **>99.99%** | **>99.99%** | **>99.99%** | **>99.99%** | **>99.995%** | **>99.995%** | **>99.995%** |
| Downtime of mission critical applications (minutes per year) | **<53 min** | **<53 min** | **<53 min** | **<53 min** | **<35 min** | **<35 min** | **<26 min** | **<26 min** | **<26 min** |
| Unscheduled downtime of mission critical applications (minutes per year) | **<15 min** | **<15 min** | **<15 min** | **<15 min** | **<15 min** | **<15 min** | **<10 min** | **<10 min** | **<10 min** |
| Scheduled downtime of mission critical applications (minutes per year) | **<40 min** | **<40 min** | **<40 min** | **<40 min** | **<20 min** | **<20 min** | **<15 min** | **<15 min** | **<15 min** |
| MCS design to support peak number of AMHS transport moves (moves/hr) | **14.7K** | **15K** | **15K** | **15K** | **15K** | **15K** | **15K** | **15K** | **15K** |
| Wafer-level (within-lot) recipe / parameter adjustment | **Partial** | **Partial** | **Partial** | **Yes** | **Yes** | **Yes** | **Yes** | **Yes** | **Yes** |
| Within-wafer recipe / parameter adjustment | **No** | **No** | **No** | **Partial (Litho)** | **Partial (Litho)** | **Partial (Litho)** | **Yes (Litho)** | **Yes (Litho)** | **Yes (Litho)** |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

*Table FAC6b Factory Information and Control Systems Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *Wafer Diameter (mm)* | *450* | *450* | *450* | *450* | *450* | *450* | *450* |
| Availability of mission critical applications (% per year) | ≥99.999% | ≥99.999% | ≥99.999% | ≥99.999% | ≥99.999% | ≥99.999% | ≥99.999% |
| Downtime of mission critical applications (minutes per year) | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min |
| Unscheduled downtime of mission critical applications (minutes per year) | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min | ≤5 min |
| Scheduled downtime of mission critical applications (minutes per year) | 0 min | 0 min | 0 min | 0 min | 0 min | 0 min | 0 min |
| MCS design to support peak number of AMHS transport moves (moves/hr) | 15K | 15K | 15K | 15K | 15K | 15K | 15K |
| Wafer-level (within-lot) recipe / parameter adjustment | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Within-wafer recipe / parameter adjustment | Yes (Litho) | Yes (Litho) | Yes (Litho) | Yes (Litho) | Yes (Litho) | Yes (Litho) | Yes (Litho) |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*



*Explanation of Items for Factory Information and Control Systems Requirements*

| *Item* | *Explanation* |
|---|---|
| Availability of mission critical applications (% per year) | Availability (A) is the probability that the equipment will be in a condition to perform its intended function when required as defined in SEMI E10-0304E and is calculated as 100% minus (scheduled downtime % + unscheduled downtime %). Scheduled downtime and unscheduled downtimes are defined in SEMI E10-0304E. |
| Downtime of mission critical applications (minutes per year) | The time when mission critical applications is not in a condition, or is not available, to perform its intended function. Mission critical applications are those required to keep the entire wafer factory operational. Depending on factory configuration, these include: MES, scheduler / dispatcher, MCS, PCS, recipe download, reticle system, and facilities control systems. Hardware, system, and software upgrades are part of non-scheduled time as defined in SEMI E10-0304E, Section 5.10.1, and are not included in downtime. |
| Unscheduled downtime of mission critical applications (minutes per year) | The time when the equipment is not available to perform its intended function due to planned down time events as defined in SEMI E10-0304E. Scheduled down time includes maintenance delay, production test, preventive maintenance, change of consumables, setup, and facilities related events. |
| Scheduled downtime of mission critical applications (minutes per year) | The time when the equipment is not available to perform its intended function due to unplanned down time events as defined in SEMI E10-0304E. Scheduled down time includes maintenance delay, repair, change of consumables, out-of-spec inputs, and facilities related events. |
| FICS design to support peak number of AMHS transport moves (moves/hr) | Able to support: peak # of moves for unified transport system * 1.5 (to translate to separate interbay / intrabay system) * 2 (safety factor for FICS). See the Material Handling Systems Technology Requirements for Peak System Throughput (40K WSPM) – Transport (moves/hour) – unified system. |
| Wafer-level recipe / parameter adjustment<br>Within-wafer recipe / parameter adjustment | Ability for factory information and control systems to run a different recipe and/or parameters for each wafer within a carrier. This facilitates wafer-to-wafer recipe and parameter adjustment and supports the ability to have multiple lots per carrier. This requirement includes wafer traceability which provides the ability to track, monitor, and control the wafer at each point in the factory or within the equipment. |

## FACILITIES

Facilities include the overall physical buildings, cleanroom, and facility infrastructure systems, up to and surrounding the production equipment, directly associated with semiconductor manufacturing operations (does not include adjacent general office spaces and corporate functional areas are not included). Production equipment requirements, manufacturing goals, management philosophies, environmental, safety, and health (ESH) requirements, building codes and standards, defect-reduction targets and wafer cost reduction targets will affect the facility and supporting facility infrastructure systems requirements, complexity, and costs.

The industry continues to demand facilities that are increasingly flexible, extendable, and reliable, come on-line more quickly, and more cost effectively; however, production equipment requirements, ESH compliance and factory operational flexibility are continuing to drive increased facility capital and operating costs. Factory size is continuing to increase with more complex, larger, and heavier production and support equipment. New and different process steps are increasing the cleanroom size faster than factory production output increases. Consequently, the increasing size and complexity of the factory, the production equipment and material handling systems, as well as the pressure to reduce time to market and facility costs will make maintaining many of the current factory requirements a challenge (as described in Table FAC7a and b). Better coordination among production equipment operation, maintenance, and environmental requirements, facility infrastructure system design, installed utility capacities, and facility space (volume) is necessary to achieve these goals, improve system and space utilization, and control facility capital and operating costs.

Facility complexity and costs are also rising due to impacts from many other areas including the greater variety in gases/chemicals, more stringent ESH regulations, and more stringent electrostatic discharge (ESD) and electromagnetic interference (EMI) controls. Accommodating all these complexity drivers will require early collaboration with production equipment manufacturers to provide innovative and cost effective solutions for maintenance, abatement, and reclaim/recycle. Meeting production equipment requirements (vibration, purity) at point-of-use may be a more cost-effective approach to meeting future requirements without increasing facility costs or sacrificing flexibility. For example, reducing facility vibration requirements and then working with production equipment manufacturers to ensure proper vibration control at the tool will control facility vibration at the tool and reduce facility costs without decreasing the facility's flexibility. Reduction of gas and chemical purity and piping installation specifications on central supply systems and concentrating ultra purity requirements to the specific equipment or areas required can also help control costs, improve flexibility, and enhance operating reliability. The rise of airborne molecular contamination (AMC) will require revisiting contamination control procedures with new methods and materials, which could also affect facility components used during construction. Facility operations will also require coordination with production equipment vendors to ensure proper AMC control.

Production equipment installation costs and time continue to be driven higher by increasing gas, chemical and utility connections and ESH compliance requirements. Development and installation of tool adapter plates will help ensure production equipment installation consistency, reduce changing PE design requirements, and provide accurate installation documentation. Earlier awareness of new production equipment designs and standardizing production equipment connections and materials of construction would allow for a base-build construction "Design for Facilities" emphasis.

To meet the demand to reduce time from groundbreaking to first full loop wafer out while production equipment increases in complexity, factory operations seek more flexibility and global codes, standards, and regulations increase in variability will require a paradigm shift in the way facilities are provided. This shift entails complete integration of the IC manufacturer, the factory designers/builders, and the production equipment vendors into the entire project team. As a minimum, the project team must be assembled early and include process engineers, manufacturing engineers, facility engineers, design consultants, construction contractors, vendor/suppliers and process equipment manufacturers. Development of techniques such as standardized design concepts, generic fab models, and off-site fabrication will be required to relieve construction site congestion, to reduce construction time, and to control facility costs to meet desired cost reduction goals. Challenging the production equipment suppliers and factory design teams to develop and conform to a standardized utility infrastructure will also help control capital cost and reduce facility time to market.

Factory operating costs are continuing to be driven by higher facility depreciation, higher utility consumption, and higher labor costs. Development of sustainability concepts for Fab construction and operation will improve resource usage and reduce the environmental impact, for example:

- Construction costs can be reduced by lowering exhaust/makeup air requirements, raising process equipment cooling water temperatures, and using higher voltage power for production equipment.
- Operating costs can be reduced by innovative reuse and recycling concepts for UPW, implementing equipment "sleep" mode, raising cooling water temperatures, relaxing cleanroom cleanliness requirements through the use of mini-environments and isolation technologies (SMIF, FOUP) and implementing operational visualization through real time monitoring and control of utility utilization.

Upfront initial capital costs may increase, but life cycle costs and environmental impact will be reduced through sustainability efforts. With this resource conservation efforts, care must be exercised that facility and production equipment operational requirements are not compromised. For example, reductions in cleanroom airborne particle cleanliness and associated airflow may cause temperature, humidity, cleanliness, and PE maintenance concerns. These concerns must be addressed in collaboration with ESH, Yield Enhancement, and PE. As the general fab cleanliness reaches ISO Class 6, the production equipment maintenance needs could be built into the equipment, through the use of a

portable vertical flow hood. This would provide localized clean air as well as prevent maintenance activities from contaminating the fab environment.

Although reliability of facility infrastructure systems is currently sufficient to support manufacturing, much of this reliability has been achieved through costly redundancy. Improvement is still needed in the design and operation of individual electrical, mechanical and control components and systems to reduce manufacturing interruptions. Collaboration with facility equipment manufacturers may modify the N+1 philosophy for redundancy and positively affect costs without sacrifice to reliability.

Finally, any significant change in the production equipment set [such as new chemistries and wafer environment or handling requirement (nitrogen or vacuum atmospheres, single wafer processing)] both for post CMOS or for next generation wafer size, will have an impact on future factory requirements, schedules, and costs. These cannot be reliably predicted from current 300 mm technology. (Refer to the Facilities Potential Solutions Figure FAC6.)

*Table FAC7a Facilities Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *35* | *32* | *28* | *25* |
| *Wafer Diameter (mm)* | *300* | *300* | *300* | *300* | *300* | *450* | *450* | *450* | *450* |
| Manufacturing (cleanroom) area/wafer starts per month ($m^2$/WSPM) (low mix only) | **0.6** | **0.625** | **0.65** | **0.675** | **0.7** | **0.725** | **0.75** | **0.775** | **0.8** |
| SubFab to Fab ratio (see definition) | **1** | **0.75** | **0.75** | **0.75** | **0.75** | **0.75** | **0.75** | **0.75** | **0.75** |
| Facility service life (in three-year nodes) | **3** | **3** | **3** | **3** | **3** | **3** | **3** | **3** | **3** |
| Facility cleanliness level (ISO 14644) [1] | **Class 6 at rest** | **Class 6 at rest** | **Class 6 at rest** | **Class 6 at rest** | **Class 6 at rest** | **Class 7 at rest [2]** | **Class 7 at rest [2]** | **Class 7 at rest [2]** | **Class 7 at rest [2]** |
| *Facility cleanliness level (Airborne molecular contamination AMC) - ppt* | Discussed in Yield Enhancement Chapter | | | | | | | | |
| Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [3] | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** | **6.25 (VC D)** |
| Facility non-critical vibration areas (micrometers per second) [3] | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** | **50 (VC A)** |
| *Temperature and Humidity Specifications* | Discussed in Yield Enhancement Chapter | | | | | | | | |
| Maximum allowable electrostatic field on facility surfaces (V/cm) | **70** | **63** | **55** | **50** | **44** | **38** | **35** | **31** | **28** |
| *Gas, water, chemical purity* | Discussed in Yield Enhancement Chapter | | | | | | | | |
| Factory construction time from groundbreaking to first tool move-in (months) | **12** | **11** | **11** | **10** | **10** | **9** | **9** | **9** | **9** |
| Production equipment install and qualification cost as a % of capital cost [4] | **10%** | **9%** | **9%** | **8%** | **8%** | **8%** | **8%** | **8%** | **7%** |
| *Facility power, water, and chemical consumption* | Discussed in ESH Chapter | | | | | | | | |
| *Energy Consumption Total Fab Support System ($kWh/cm^2$ per wafer out)* | Discussed in ESH Chapter | | | | | | | | |
| Ratio of tool idle versus processing energy consumption (kWh) | **0.75** | **0.75** | **0.60** | **0.50** | **0.5** | **0.5** | **0.5** | **0.5** | **0.5** |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

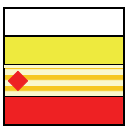
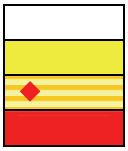


*Table FAC7b Facilities Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *Wafer Diameter (mm)* | *450* | *450* | *450* | *450* | *450* | *450* | *450* |
| Manufacturing (cleanroom) area/wafer starts per month ($m^2$/WSPM) (low mix only) | 0.825 | 0.85 | 0.875 | 0.9 | 0.925 | 0.95 | 0.975 |
| SubFab to Fab ratio (see definition) | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 | 0.75 |
| Facility service life (in three-year nodes) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Facility cleanliness level (ISO 14644) [1] | Class 7 at rest [2] | Class 7 at rest [2] | Class 7 at rest [2] | Class 8 at rest [2] | Class 8 at rest [2] | Class 8 at rest [2] | Class 8 at rest [2] |
| *Facility cleanliness level (Airborne molecular contamination AMC) - ppt* | Discussed in Yield Enhancement Chapter | | | | | | |
| Facility critical vibration areas (lithography, metrology, other) (micrometers per second) [3] | 6.25 (VC D) | 6.25 (VC D) | 6.25 (VC D) | 6.25 (VC D) | 6.25 (VC D) | 6.25 (VC D) | 6.25 (VC D) |
| Facility non-critical vibration areas (micrometers per second) [3] | 50 (VC A) | 50 (VC A) | 50 (VC A) | 50 (VC A) | 50 (VC A) | 50 (VC A) | 50 (VC A) |
| *Temperature and Humidity Specifications* | Discussed in Yield Enhancement Chapter | | | | | | |
| Maximum allowable electrostatic field on facility surfaces (V/cm) | 25 | 22 | 20 | 18 | 15 | 13 | 10 |
| *Gas, water, chemical purity* | Discussed in Yield Enhancement Chapter | | | | | | |
| Factory construction time from groundbreaking to first tool move-in (months) | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Production equipment install and qualification cost as a % of capital cost [4] | 7% | 6% | 6% | 5% | 5% | 5% | 5% |
| *Facility power, water, and chemical consumption* | Discussed in ESH Chapter | | | | | | |
| *Energy Consumption Total Fab Support System ($kWh/cm^2$ per wafer out)* | Discussed in ESH Chapter | | | | | | |
| Ratio of tool idle versus processing energy consumption (kWh) | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |

*Note: Facilities technology requires table make the following assumptions with respect to legends:*



*Current solutions provide cost effective trade off between facilities and equipment installation*

*Does not prevent manufacturing, but use of space is not optimized.*

*Does not prevent manufacturing, but impact on space, time to manufacturing, and cost of ownership is not known.*

*Explanation of Items for Facilities requirements:*

| *Item* | *Explanation* |
|---|---|
| Manufacturing (cleanroom) area ($m^2$) | "Manufacturing (cleanroom) area" is defined as the space in square meters containing the process and metrology equipment used for direct manufacturing processes such as photolithograph, diffusion, etch, thin films, CMP, excluding subfab spaces containing support equipment and facility infrastructure systems. Foreseeable technologies that will impact cleanroom size are such as additional metal layers and double exposure for litho. |
| Wafer starts per month (WSPM) | Wafer starts per month is defined as the number of new 300 mm wafers introduced into production for processing during a given 30 day period. |
| Sub-Fab to Fab ratio | "Sub-Fab to Fab ratio" is defined as the footprint of the production equipment support plan area to the manufacturing area above. The 25% reduction in floor space allows for columns and safety equipment in the subfab that is required by the facility. Relates to and extends factory operations "floor space effectiveness." |
| Facility service life (in three-year nodes) | Facility service (system) life is the number of nodes (process changes) that the system is available before major renovation is required to meet process requirements. |
| Facility cleanliness class (ISO 14644) | Cleanliness classification of wafer factory manufacturing (cleanroom) area as defined by ISO 14644-1[6]. |
| Facility critical vibration areas (litho, metro, other) (micrometers per second) | "Vibration critical" is defined as area of the primary manufacturing floor in which a significant portion of the equipment is highly sensitive to floor vibration, the mitigation was not provided at the tool itself, and excessive vibrations can have serious deleterious effects on product. Extensive measures may be required in the facility's structural and mechanical equipment design based upon the needs of this space category. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-CC0012.2[7] |
| Facility non-critical vibration areas (micrometers per second) | "Vibration non-critical" is defined as area of the primary manufacturing floor in which all or some of the equipment is only moderately vibration sensitive, and the structural system performance can be reduced. Vibration criteria are limits on vibration amplitudes at the floor or other support of a tool, given as VC-x, where x is a letter designation from A through E, each corresponding to a specific vibration amplitude spectrum. Refer to IEST-RP-CC0012.2. |
| Maximum allowable electrostatic field on facility surfaces (V/cm) | Facility surface electric field limits apply to all factory materials-construction materials, furniture, people, equipment, and carriers Refer to SEMI standards E129[8], E78,[9] and E43[10] for measurement methods. |
| Factory construction time from groundbreaking to first tool move-in (months) | Factory construction time is defined as the period of time in months from first horizontal structural concrete placement to the time that the first tool is moved into the manufacturing area and is ready for hookup, i.e., building systems(i.e., Building, Fire and Life Safety Systems) have passed chem. ready inspections sufficient to begin the tool installation process. |
| Production equipment install and auxiliary facility and process systems qualification cost as a % of total capital cost | "Production equipment installation cost" is defined as the cost of all labor and materials necessary to accept, move-in, and connects production equipment to the facility infrastructure systems to make the production equipment operational. This includes facility system qualification, but excludes facility infrastructure systems and upgrades, and the cost of the production equipment. Excludes production equipment qualification. |
| Total capital cost | "Total capital cost" is defined as all labor and material costs necessary to complete a new semiconductor factory including production equipment and facility capital cost. This excludes costs for land. |
| Ratio of tool idle versus processing energy consumption (kWh) | Ratio of energy consumption of process tool and support equipment when not processing wafers over energy consumption while tool is processing wafers per SEMI S23 application guide. |

# POTENTIAL SOLUTIONS

The principal goals of factory integration are maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs. the difficult challenges of 1) responding to complex business requirements; 2) achieving growth targets; 3) managing factory complexity;4) meeting factory and equipment reliability; capability or productivity requirements; 5) meeting the flexibility, extendibility, and scalability needs; 6) meeting process requirements at 65 nm and 45 nm at production volumes; 7) increasing global restrictions on environmental issues; 8) post-conventional CMOS manufacturing uncertainty, and 9) emerging factory paradigm and next wafer size must be addressed to achieve these goals. Potential solutions are identified for Factory Operations, Production

[6] *ISO 14644-1.: Cleanrooms and controlled environments, Part 1: Classification of air cleanliness*
[7] *IEST-RP-CC012.2: Considerations in Cleanroom Design.*
[8] *SEMI E129: Guide to Assess and Control Electrostatic Charge in A Semiconductor Manufacturing Facility.*
[9] *SEMI E78: Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment.*
[10] *SEMI E43: Guide for Measuring Static Charge on Objects and Surfaces.*

Equipment, Material Handling Systems, Factory Information and Control Systems, and Facilities. Note that the bars containing wafer diameter data represent potential solutions that are wafer-size specific.

Potential solutions are shown as "*Research required*," "*Development underway*," and "*Qualification/pre-production*." The purpose is to provide guidance to researchers, suppliers, and IC makers on the timing required to successfully implementing solutions into factories. Several research efforts are being planned (Ex: FORCe) in order to address the technology requirements and to develop these potential solutions. For simplicity, these activities are serial in each table; however, they overlap each other in practice.

The potential solution tables have been updated for 2007 to reflect progress made and it also includes a few potential solutions to address new and emerging factory integration technology requirements. The potentials solutions are shown in five tables with each table representing the individual potential solution needed for individual factory integration sub-section.

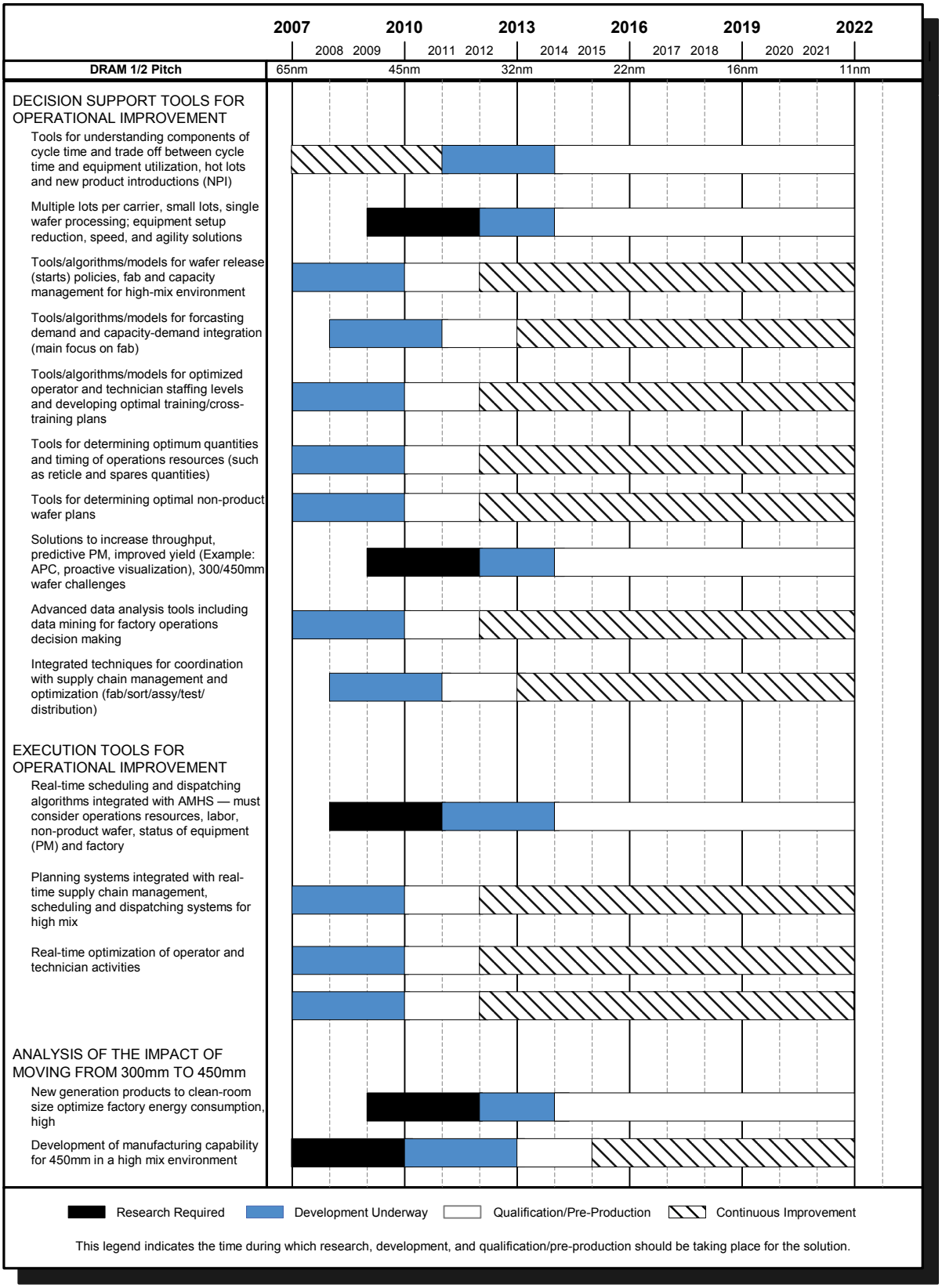



*Figure FAC2 Factory Operations Potential Solutions*

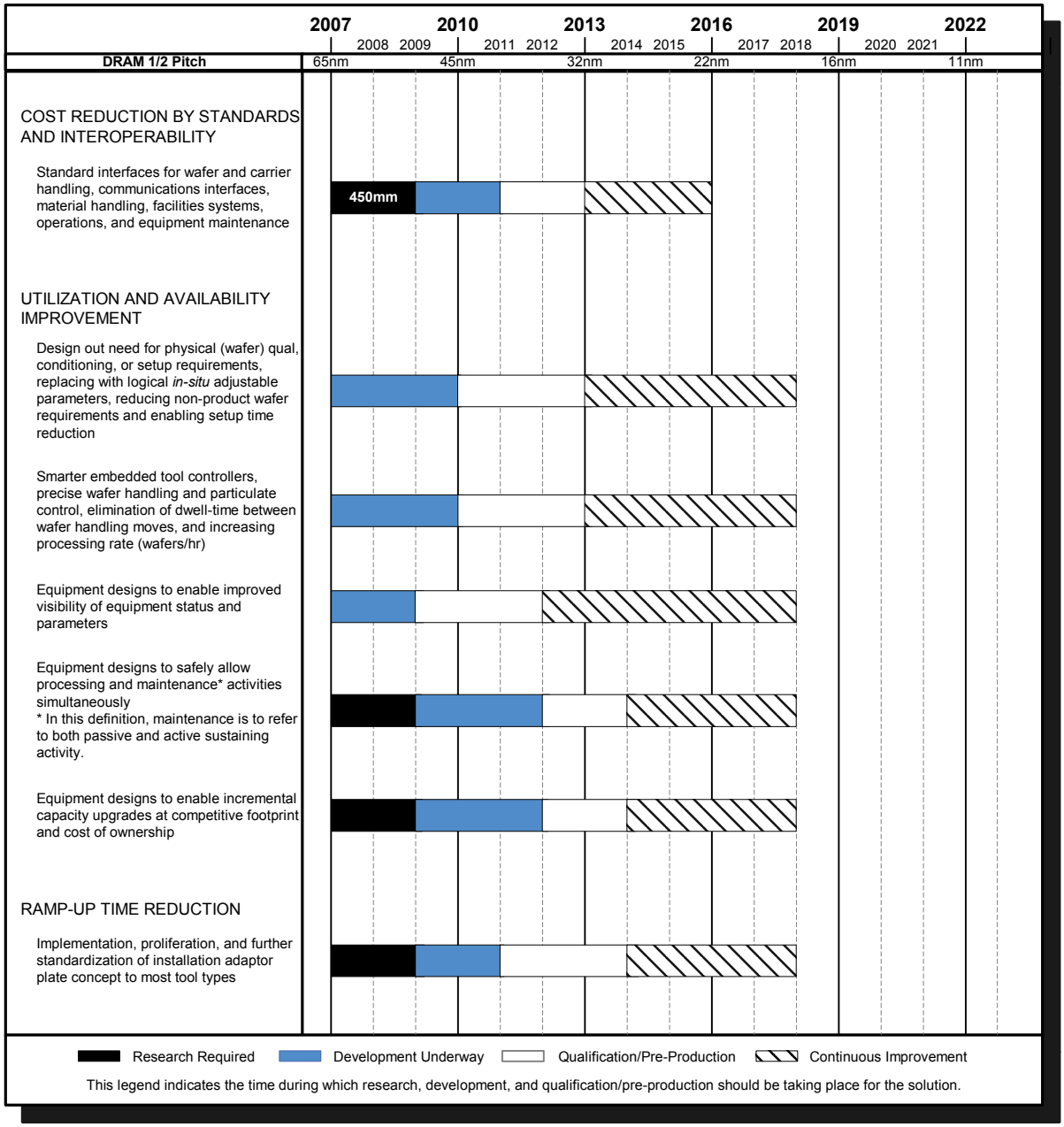



*Figure FAC3 Production Equipment Potential Solutions*

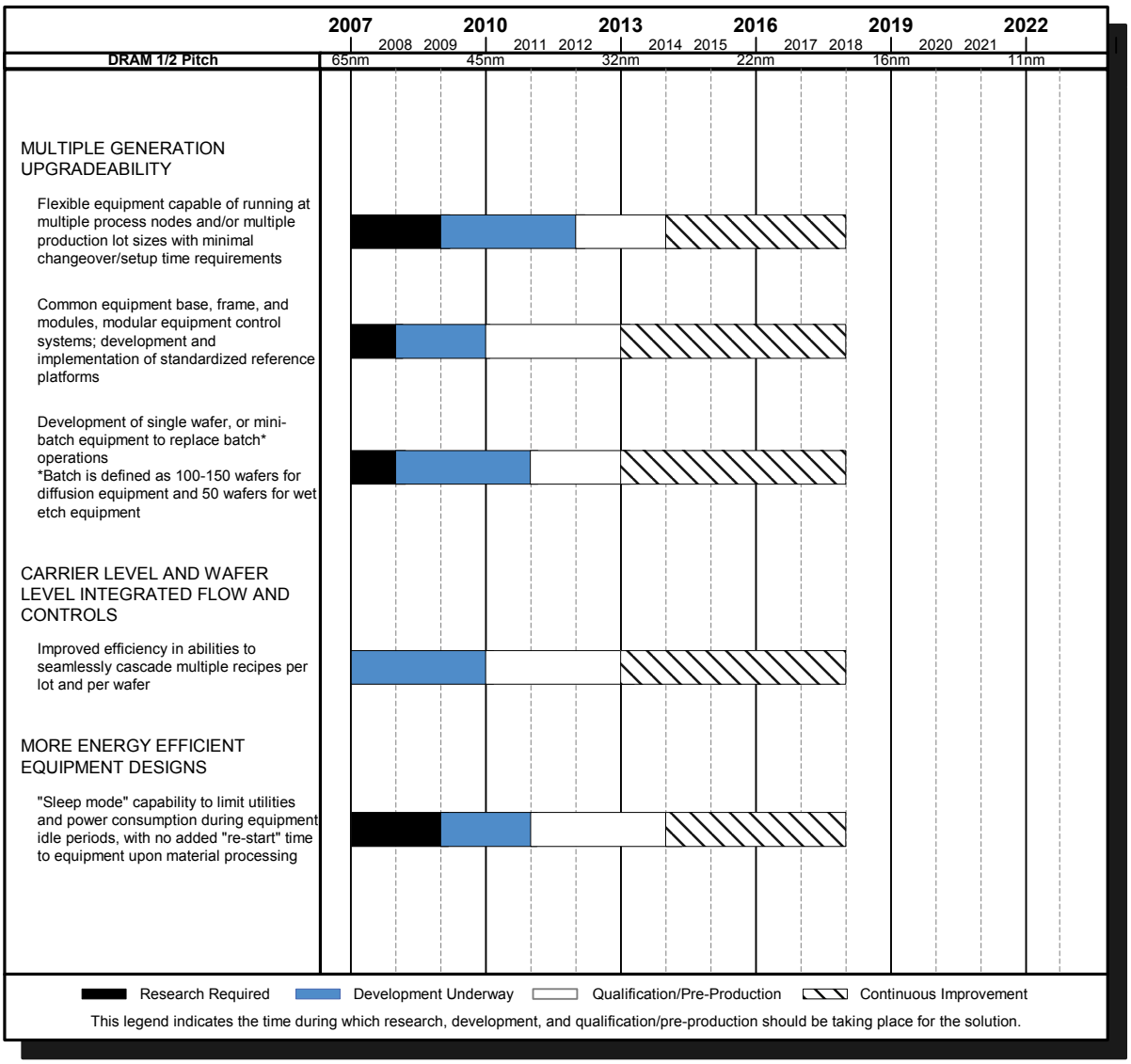



*Figure FAC3 Production Equipment Potential Solutions (continued)*

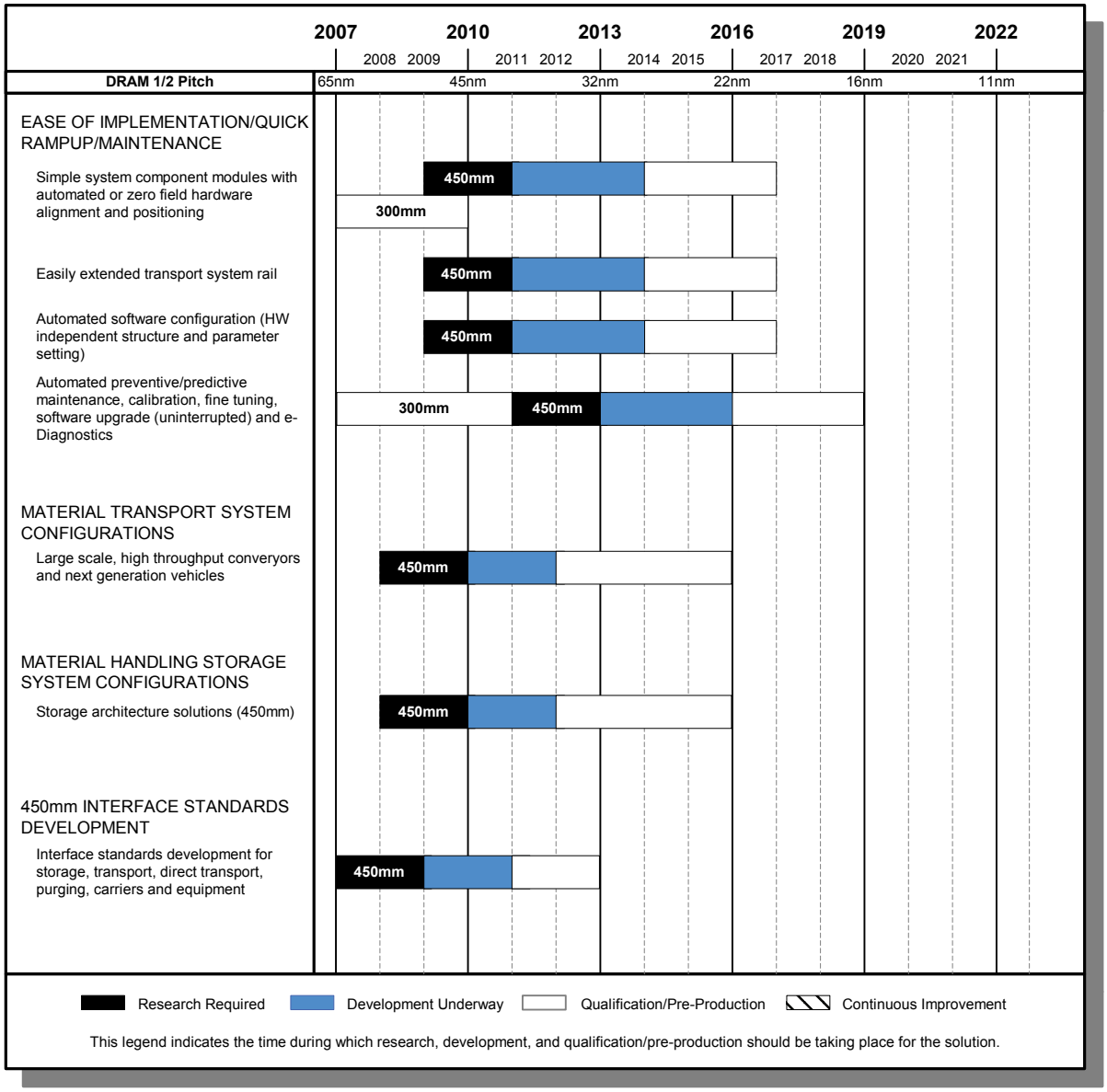



*Figure FAC4 Material Handling Potential Solutions*

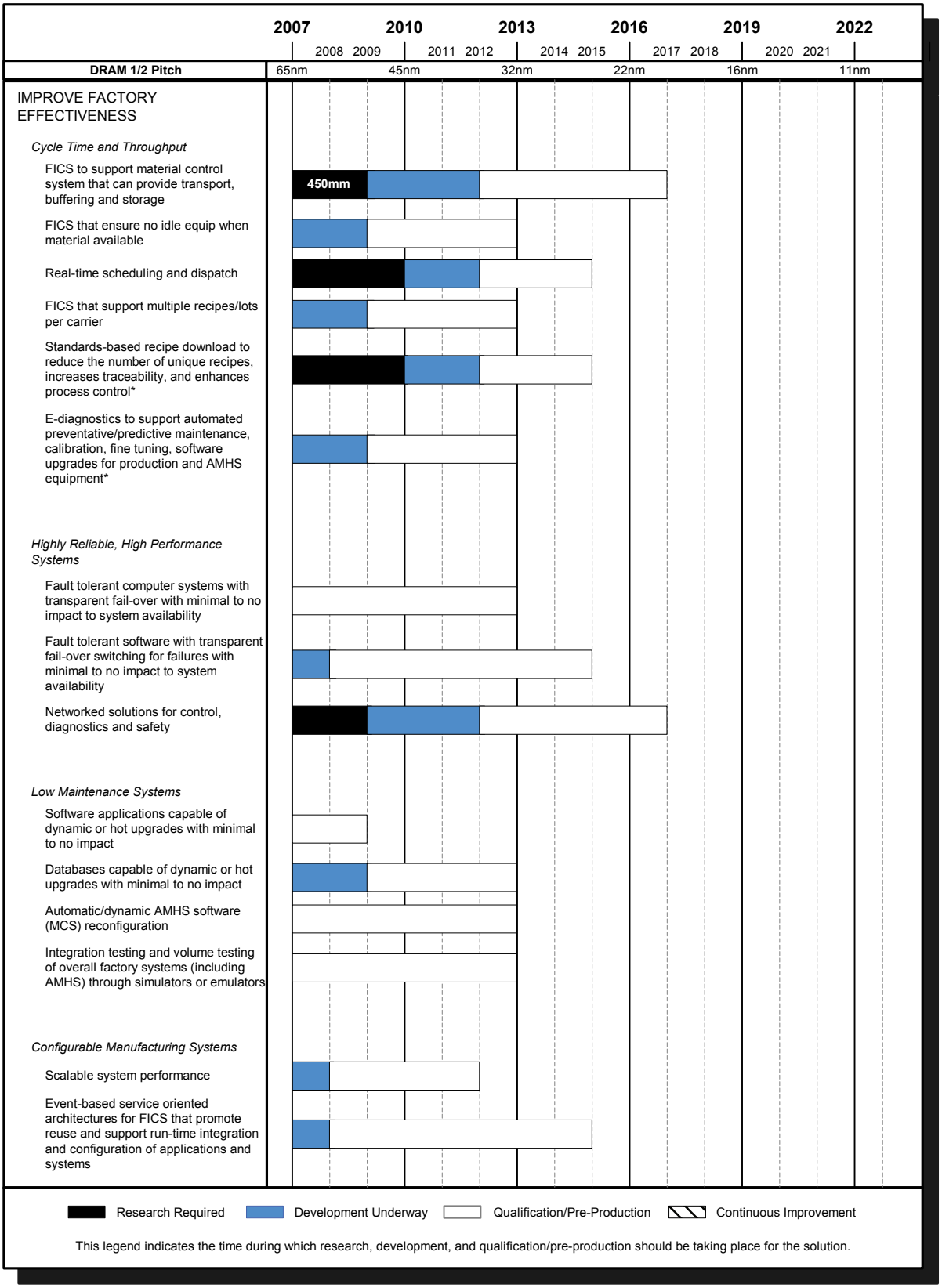



*Figure FAC5 Factory Information and Control Systems Potential Solutions*

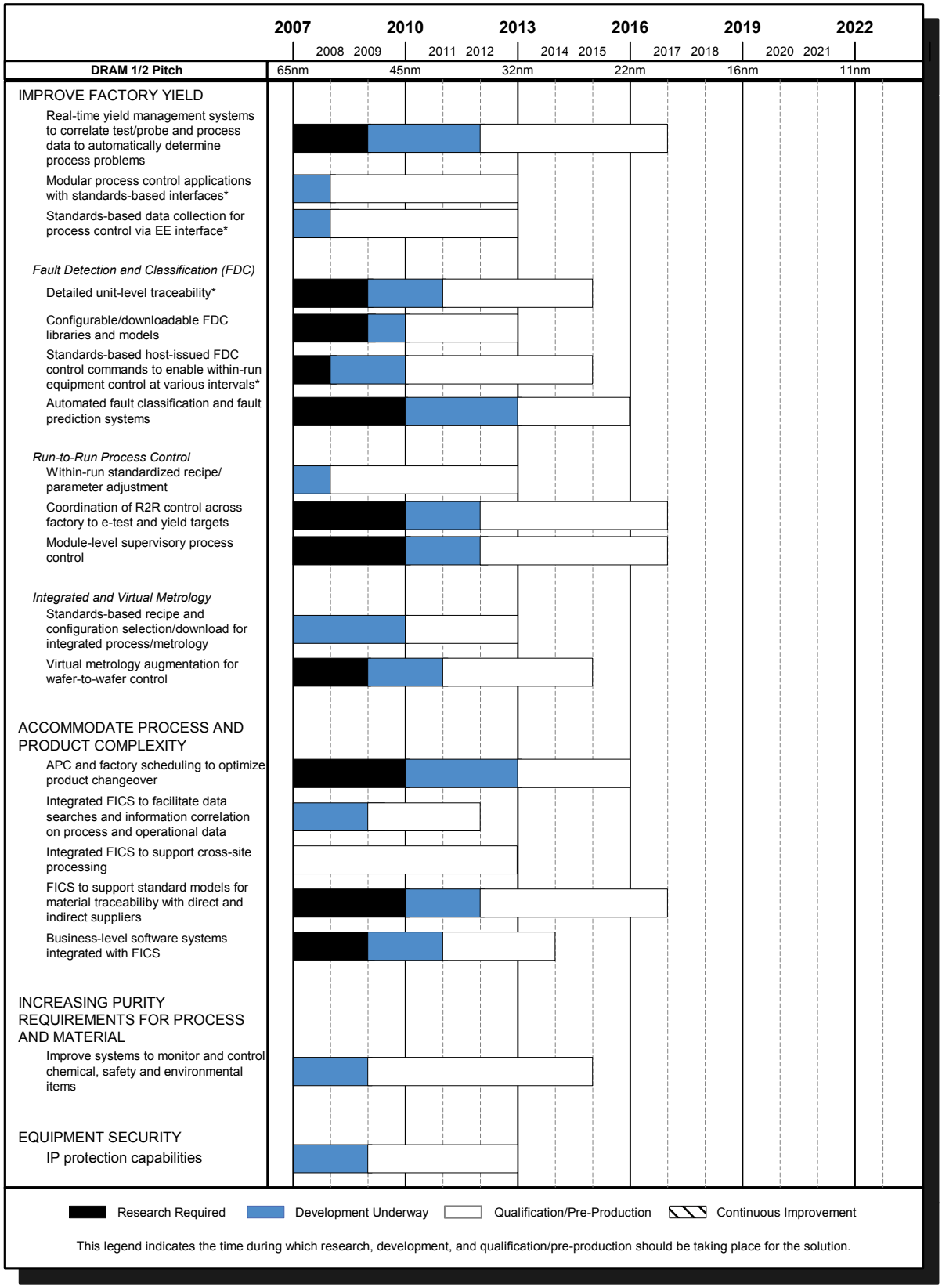



*Figure FAC5 Factory Information and Control Systems Potential Solutions (continued)*

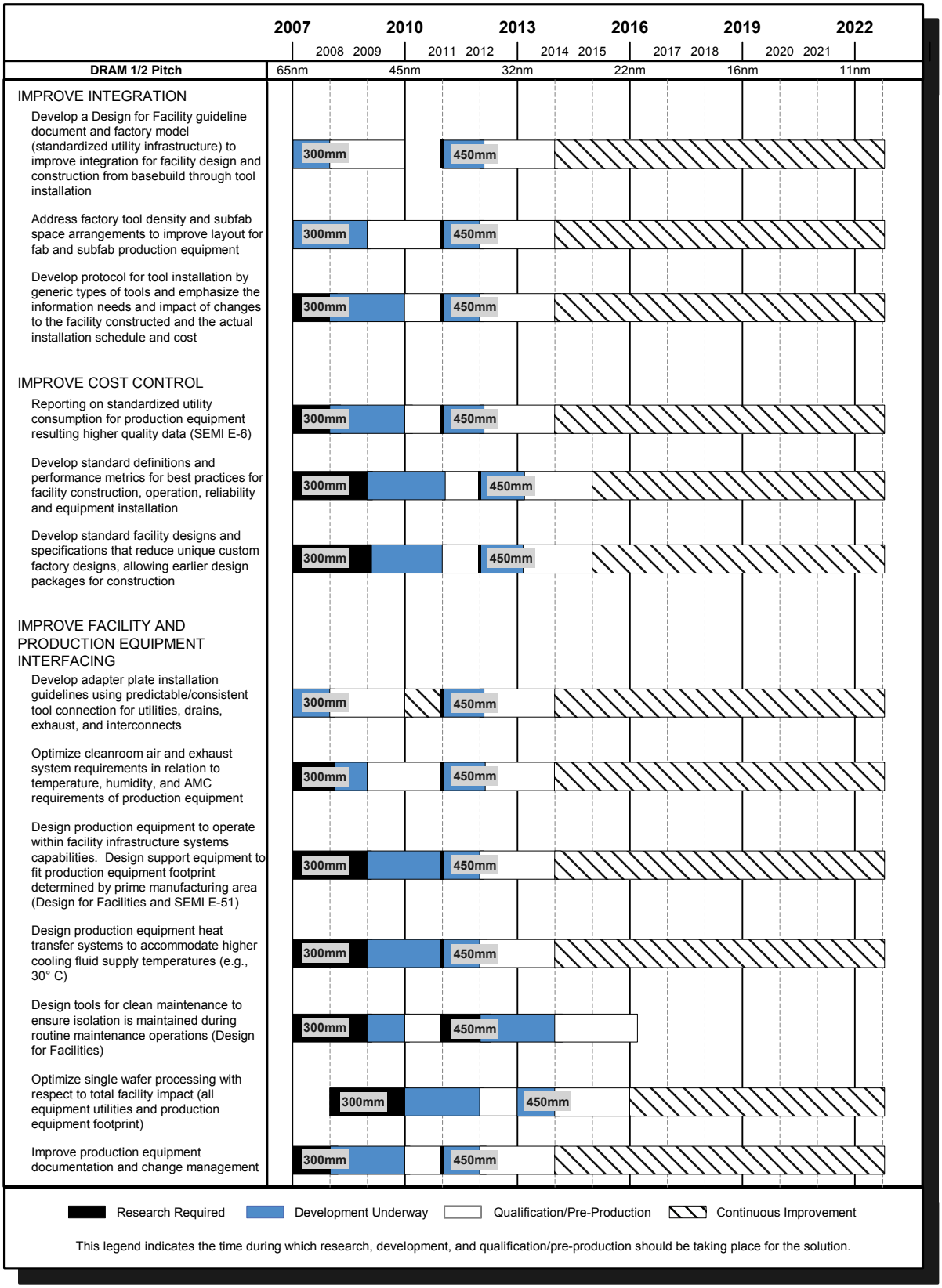



*Figure FAC6 Facilities Potential Solutions*

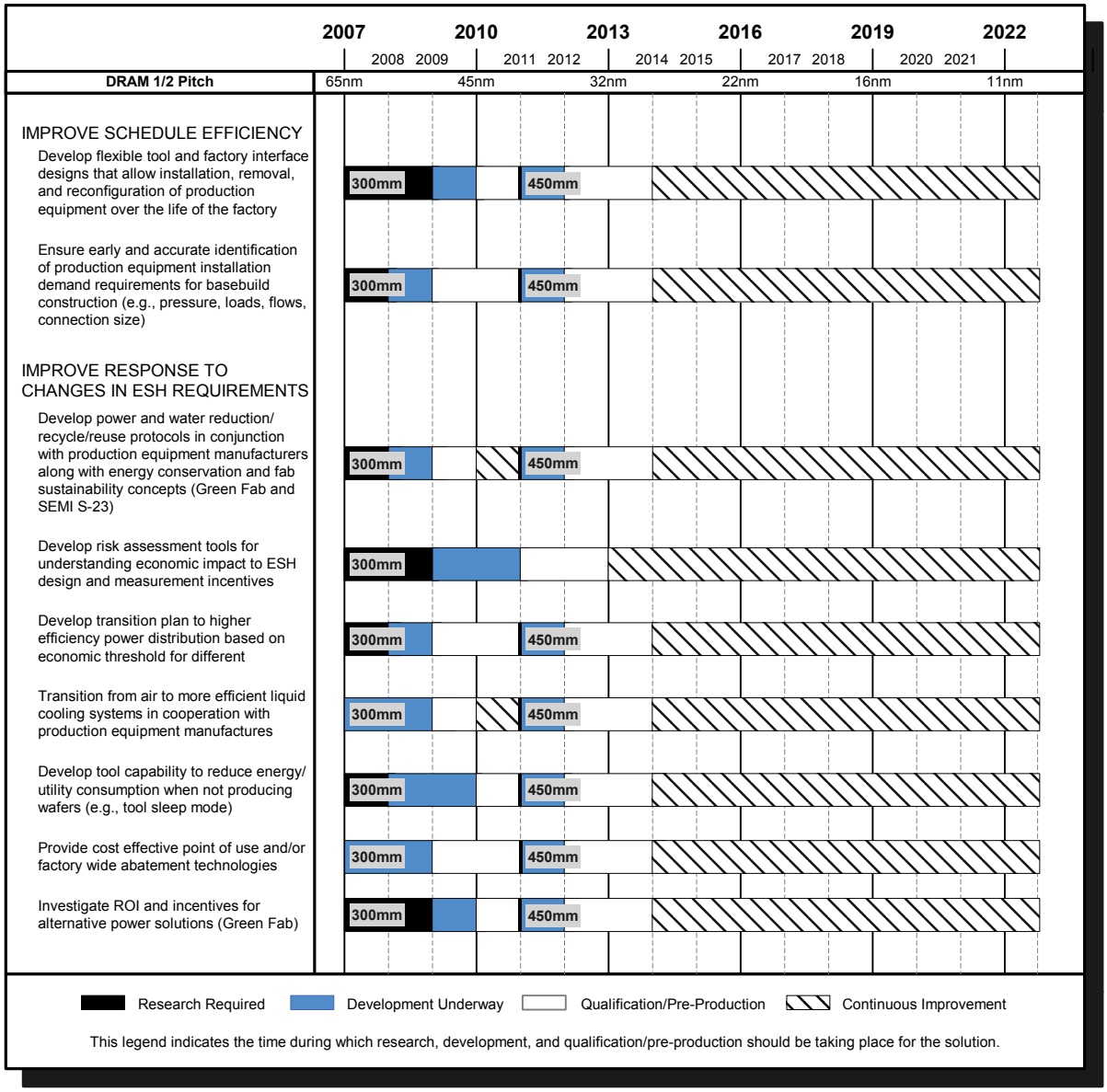



*Figure FAC6 Facilities Potential Solutions (continued)*

# CROSSCUT ISSUES

Factory Integration technology requirements is often driven by the device, processing, yield, metrology, ESH, lithography, and other technology working group (TWG) requirements. In order to understand the crosscut issues fully, Factory Integration interfaces with the other technology working groups and puts together a list of key crosscut challenges and requirements. Several crosscut issues listed in the previous years were effectively addressed and in 2007 Factory Integration primarily worked with the FEP, Lithography, ESH, Metrology, and Yield technology TWGs and the key issues are listed in Table FAC8 below. Factory Integration will continue to address these key crosscut challenges and requirements generated in the year 2007 and beyond (450 mm crosscut issues are addressed in the later pages).

*Table FAC8 Crosscut Issues Relating to Factory Integration*

| *Crosscut Area* | *Factory integration related key challenges* |
|---|---|
| Front end Process (FEP) | Wafer edge exclusion was changed from 1.5 mm to 2 mm for near-term years since no feasible solution exists.<br>Factory and FEP teams will continue to work on AMC requirements.<br>Working with FEP on what process equipments are suitable for equipment sleep mode for energy conservation. |
| Lithography | Continuing to understand EUVL (power, consumables) requirements from Factory Integration perspective;<br>Fast reticle change; reticle storage issues and reticle buffering due to small lots;<br>Need to coordinate yield inputs on temperature and humidity requirements (particularly temperature variation inside the tools);<br>AMC relative to the reticle and tighter process control needs.<br>Lithography DFM needs. |
| ESH | Primary focus is on energy and resource conservation.<br>Co-sharing of metrics for energy and resource sharing need to be in-sync.<br>Ergonomics, tool design, chemical consumption concerns;<br>AMC and particulate levels to be maintained;<br>Regulations;<br>ESH chemical abatement analysis needed. |
| Metrology | Industry wide wafer map coordinate standards are needed.<br>Comprehensive metrology roadmap to be jointly defined.<br>AMC, temperature, and humidity control will also be a crosscut issue |
| Yield Enhancement | Maintain temperature control at the lithography and metrology area.<br>Propose to relaxation of the control on absolute humidity (energy savings).<br>Factory Integration to work with the Yield team on specifying particle and AMC targets for equipment, AMHS, and FOUP.<br>Yield will provide Factory Integration information on gas and chemical process control. |

## FRONT END PROCESSING (FEP)

The Front End Processes (FEP) Roadmap focuses on future process requirements and potential solutions related to scaled field effect transistors (MOSFETs) and DRAM storage capacitors, as well as Flash and ferroelectric RAM (FeRAM) devices. The key issues FEP is working with Factory are wafer edge exclusion and 450 mm challenges. Other crosscut issues are equipment sleep mode for energy conservation and the1.5 mm wafer edge exclusion for long term is a challenge to starting material and SOI. FEP will communicate special facility AMC requirements.

## LITHOGRAPHY

The Lithography chapter deals with the difficulties inherent in extending optical methods of patterning to physical limits, and also evaluates the need to develop entirely new, post-optical lithographic technologies capable of being implemented into manufacturing. Key challenges that need to be addressed by the Factory Integration team are to ensure the infrastructure (power and water) readiness for EUVL and to improve Advanced Process Control (APC) for lithography equipment (e.g., tighter control is needed for overlay and edge roughness). Other issues to be addressed include Design for Manufacturing (DFM) and temperature variation inside the tools AMC impact on reticle.

## ENVIRONMENTAL, SAFETY AND HEALTH (ESH)

ESH continues to play a very important role in factory design and operation. Decisions made at the earliest stages of factory planning will have a dramatic impact on the ability of that factory to meet rigorous safety and environmental requirements economically. Early consideration of safe and environmentally responsible design is essential to develop

factories that comply with ESH requirements while achieving rapid start-up schedules and avoiding costly redesigns and retrofits.

Equipment suppliers have made good progress integrating point of use abatement devices and the tool. However, tool footprint in the sub-Fab has increased significantly as a result. An immediate challenge, therefore, is to find an efficient tool design that incorporates point of use devices without an overall increase in footprint both in the Fab as well as in the sub-Fab.

A plan for continuous improvement of safety in future factories must be established. A thorough understanding of safety risks associated with automated equipment will lead to standards that assure safe working conditions for both people and product. These standards must be directed at the integrity of automated systems, the tools with which they interface, and the interfaces as well.

Our industry faces increasing environmental limitations. The availability of adequate water supply already places restrictions on the size and location of factories. The goal is to build factories that minimize resource consumption and maximize resource reclamation. Effluents of environmentally toxic materials need to be reduced to near zero—perhaps to zero levels.

Conservation of energy is very critical. The constraint to this is the size of the factory, which then puts a very large potential pollution burden on the energy provider and the wafer fabrication plant. Starting this year, the Factory Integration and ESH teams will work together on equipment energy conservation (i.e., equipment sleep mode).

While much of the responsibility for ESH programs rests with the equipment suppliers, application of advanced resource management programs will have a significant impact. International ESH standardization and design programs can be greatly enhanced through training programs established for and by the industry. Consideration of ESH standards in equipment design, maintenance, de-commissioning, and final disposition will reap substantial rewards in ESH performance as well as cost. Refer to the Environment, Safety, and Health chapter for comprehensive information.

## YIELD MANAGEMENT

Development of good yield management strategies reduces costs and investment risks. A factory yield model defines typical operational performance and permits a Pareto of performance and yield detractors. A factory model based on experimental mapping of process parameters and process control strategies reduces the need for increased metrology tools and monitor wafers. It is also critical to determine tolerance variations for process parameters and interactions between processes to reduce reliance on end-of-line inspections. Factory models should also be capable of handling defect reduction inputs to assure efficient factory designs for rapid construction, rapid yield ramp, high equipment utilization, and extendibility to future technology generations. Temperature and humidity metrics alone with AMC requirements will be jointly worked out by Factory Integration and Yield TWGs.

Yield management systems (YMS) must be developed that can access and correlate information from multiple data sources. YMS should also work with measurement/metrology equipment from multiple suppliers using pre-competitive standards based data formats. Refer to the Yield Enhancement chapter for a more comprehensive discussion on YMS.

## METROLOGY

Metrology systems must be fully integrated into the factory information and control systems to facilitate run-to-run process control, yield analysis, material tracking through manufacturing, and other off-line analyses. The scope of measurement data sources will extend from key suppliers (masks and silicon wafers) through Fab, probe, assembly, final test and be linked to business enterprise level information. This data-to-information capability should exist as early as possible in a factory's history to minimize the time spent qualifying equipment and ramping the factory to production. Data volumes and data rates will continue increase dramatically due to wafer size increases and process technology shrinks. Analysis of this data will require connectivity and correlation to multiple data sources across the factory (Fab, probe, etc.). In 300 mm factories, review and classification tools may eventually appear in clusters or integrated clusters to create a more efficient factory interface. Some 300 mm process equipment will include integrated measurement (IM) capabilities to reduce cycle time and wafer-to-wafer process variance. The Factory and Metrology TWGs will continue to work on the Virtual Metrology (VM) and IM requirements. Also, both the TWGs recognize a need for industry-wide wafer map coordinate standards. Integrated management costs must be carefully balanced against benefits to make specific implementation decisions that improve the overall factory productivity. Refer to the Metrology chapter for overall metrology topics.

### STATIC CHARGE AND ELECTROMAGNETIC INTERFERENCE CONTROL

Electrostatic charge adversely impacts every phase of semiconductor manufacturing, causing three basic problems, as follows:

1. Electrostatic attracted (ESA) contamination increases as particle size decreases, making defect density targets more difficult to attain. Electrostatic attraction of particles to masks will become a more serious problem if future lithography methods eliminate the pellicle used to keep particles away from the mask focal plane.
2. Electrostatic discharge (ESD) causes damage to both devices and photomasks. Shrinking device feature size means less energy is required in an ESD event to cause device or mask damage. Increased device operating speed has limited the effectiveness of on-chip ESD protection structures and increased device sensitivity to ESD damage.
3. Equipment malfunctions due to ESD-related electromagnetic interference (EMI) reduce OEE, and have become more frequent as equipment microprocessor operating speeds increase.

These three problems occur where bare wafers and photomasks are produced, where devices are produced in wafer fabs, and where individual devices are produced in backend packaging, assembly, and test.

In addition to static charge control, electromagnetic interference (EMI) (see the standard SEMI E33 for definition)[11] causes variety of problems for semiconductor manufacturing, including, but not limited to, equipment lockup, and malfunction, sensor misreading, metrology errors and others. There are many sources of EMI in semiconductor environment that include electromagnetic emission from ESD, operation of equipment, especially high-energy tools, wireless communication and alike. Co-location of sensitive equipment with high-energy tools, cabling, ground problems, improper maintenance of equipment and others further aggravate EMI problems.

As feature sizes decrease, the impacts described above are likely to become more pronounced, particularly for metrology equipment that utilizes beam-based processes to perform its intended functions. Therefore, understanding EMI phenomena, its impacts, and how to mitigate it in a cost effective fashion becomes more important as process technology progresses into the future.

Currently EMI is not well understood by the end user and thus leads to misdiagnosed problems and misapplied EMI mitigation/controls. This needs to be addressed at a global level to prepare for what is expected to be more electromagnetic-related impacts in the future. To control and reduce the negative impact of EMI on wafers, materials and equipment, more comprehensive studies, advanced methods and measurement tools are needed.

### FACTORY INTERFACE STANDARDS REQUIREMENTS

Standards work best when applied to pre-competitive areas and when there is a benefit to all participants. Successful development, implementation, and testing of non-proprietary standards have major ramifications on the factory ability to rapidly come online and ramp to full volume in a cost-effective manner. Standardization of inter-operating elements, especially interfaces between different systems in a factory, improves the industry's ability to manage rising factory complexity.

Global cooperation among IC manufacturers and equipment suppliers for 300 mm factories has resulted in the definition and implementation of many non-proprietary factory integration standards. This activity has provided enormous industry benefits by minimizing equipment development time, reducing the cost and risk of development, and has helped reduce factory complexity.

In the past year, facilities sub-team of Factory Integration worked with SEMI to kickoff a standards team to define Adaptor standards in order to improve equipment install time.

## FACTORY INTEGRATION FOCUS AREAS

In addition to working on the five factory integration sub-sections and cross-TWG challenges, the factory integration team also evaluated key technology focus areas that impact the Factory Integration near term and longer term needs and also cuts across all the Factory Integration sub-sections in 2007. This section provides details on the three key focus areas of 1) Airborne Molecular Contamination, 2) Proactive Visualization, 3) Energy Conservation, and 4) 300′/450 mm challenges.

[11] *SEMI E33-94 - Specification for Semiconductor Manufacturing Facility Electromagnetic Compatibility.*

## AIRBORNE MOLECULAR CONTAMINATION (AMC)

Airborne Molecular Contamination (AMC) (see SEMI Std F21 for definition)[12] needs to be controlled in front-end and back-end of line operations in semiconductor fabs. This control may be achieved fab-wide or at certain critical processes, potentially also at different levels for different processes. The "wafer environment contamination control" tables of the Yield Enhancement Chapter provide recommended contamination levels as follows:

- AMC as measured/monitored in the cleanroom air and /or purge gas environment
- Surface Molecular Contamination (SMC) on monitoring wafers

Cost effective integration of AMC controls into factory design and operation should incorporate a variety of measures all the way from detection of AMC sources through control methods up to the active protection of the wafer environment. In 2005 Factory Integration addressed the fab AMC requirements such as such as air handling units, chemical filters, and reticle carriers. In addition, Factory Integration also and also defined the needs but AMC at the equipment and FOUP level needs to be understood and defined since they play a critical role in fab managing yield.

Visualization, modeling and simulation tools are required to determine and validate the most appropriate integrated AMC control solutions. Furthermore, these tools should deliver a fair basis to estimate the cost effectiveness of the proposed solutions.

To keep the AMC under control multi-facetted programs are recommended to monitor and control AMC. The challenge and the essential goal is to elaborate a data management system, which links these measurements to metrology and provide feedback for APC and run-to-run control via a compatible data interfaces.

## PROACTIVE VISUALIZATION

Device makers are required to adapt their manufacturing resource and operation models to more complex and diversified business environment with flexibility and agility. SoC (System on Chip) manufacturing is a good example of the typical challenging manufacturing business models that expose distinct production deficiencies. Proactive visualization is an effort to grasp the manufacturing problems and requirements by breaking down and recapturing with a high degree of abstraction and the finer information granularity. Figure FAC7 shows a comprehensive and integrated visualization matrices and relationship. The table structure is a typical matrix with *manipulation* axes and *value* axes with layered structure.

Another aspect of proactive visualization is the delivery time structure. The possible trade-offs between delivery time and cost or between cycle time and device quality assurance need to be investigated. Delivery time can be broken down along with three viewpoints of; the fab resource, the fab operation, and, the product lot. Resource and fab operation viewpoints are usually used for maximization of throughput and minimization of manufacturing cost in LM/HV production model, whereas the product lot and fab operation viewpoints are usually used for cycle time reduction or delivery time conformance purposes. HM/LV production model requires all of these viewpoints for the higher level optimization. Some of the delivery time elements are lot size dependent. It is necessary to describe fab ability to handle the smaller lots.

The mean SoC order sizes are believed to shrink continuously as the larger diameter wafer transition proceeds and the short delivery time is persistently required. The cycle time trend needs to be captured along with the order size trend and the available maximum wafer diameters for volume production in ITRS. In order to capture these needs, Factory Integration technology requirements tables have included small lot cycle time metrics in 2007. Averaged cycle time for one mask layer can be a good metric, and is expected to decrease together with the decreasing trend in the hypothetical default lot size.

The current semiconductor fabrication equipment is very complex in terms of the discrete capabilities and a composite functionality. The reliability assurance is becoming a big challenge both for the equipment suppliers and users. The equipment activity may be divided into the following three hierarchical consecutive abstract activity domains;

1. Parametric process conditions,
2. Control activity in internal devices,
3. Subsystems or functional devices activity.

Currently the top domain activity is monitored and examined with limited parametric data for the process conditions. Since the underlying domains have not been well visualized, these three domains are not consecutively related in terms of process execution reliability.

[12] *SEMI F21-1102 - Classification of Airborne Molecular Contaminant Levels in Clean Environments.*

Equipment Engineering Capability Guidelines by Selete/JEITA and ISMI (2002)[13] call for necessary collaborations between equipment suppliers and device makers with using high quality EE (equipment engineering) data collected through "the second port" on the equipment.

The gap in the process execution reliability chain may be fulfilled if effective collaborations between these consecutive domains and across the business boundary are established with the help of fine information granularity. Equipment reliability assurance contents (such as evidence data, data model, and verification specification) are to be exchanged between the equipment suppliers and the device makers for this to happen. EE data required in EEC guidelines will help provoke proactive visualization across the intra-company and the business boundaries in the industry to enable more strategic task sharing.

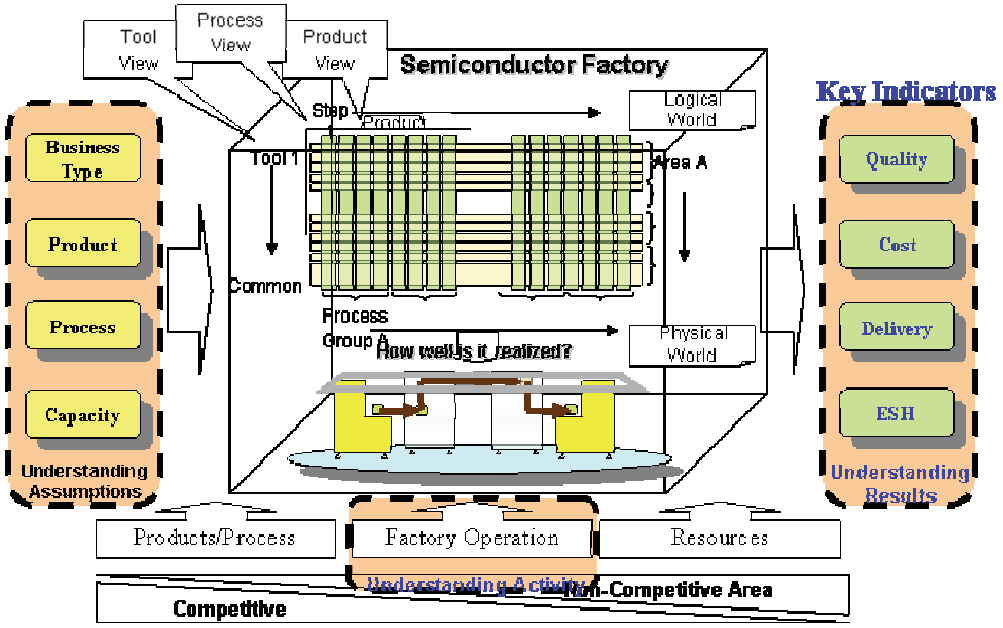



*Figure FAC7 Comprehensive Analysis and Decision Makings Need Matrix Table with Manipulation and Value Axes*

The requirement of equipment supplier's involvement in proactive visualization has been well discussed and organized as a strategic proposal as Equipment Engineering Quality Assurance (EEQA). It necessary to obtain equipment model-based data for better understanding of intrinsic equipment losses. Equipment engineering data is generically defined as any data generated by the equipment that can be used to describe the equipment's capabilities, status, or performance. Equipment engineering data allows equipment suppliers to adjust, tune, and validate equipment performance and allows device makers to validate equipment is functioning as expected in a production environment. The scope of equipment engineering data must be re-defined to be effective and meaningful for equipment suppliers as well as IC makers, and must enable device makers to manage factory performance more proactively. The introduction of the so-called "2nd port" for non-Factory control data is expected to provide more bandwidth and "better engineered" data transmission and data utilization.

Equipment engineering data should support five areas of critical use:

- Data usage for description of production control by the factory and relevant generic equipment activities (e.g., context of GEM300 data)
- Data usage for description of process conditions generated as a result of wafer processing
- Data usage for calculation and host/external visual monitoring of equipment activity, to enable improvements in equipment productivity (intrinsic equipment loss) and agility
- Data usage for analysis and improvements of energy, material, and consumable parts consumption
- Data usage for description of process actuator and inter-tool activities to enable performance tuning, adjustment, and measurement, and validation of equipment performance and health

[13] *Equipment Engineering Capability Guidelines by Selete/JEITA and ISMI (2002).*

In all these cases, data should be provided for each wafer and each equipment chamber (where applicable) as shown in Figure FAC8. Equipment engineering data must be well designed for systematic, automated, and should be accompanied by enough context information (including, synchronized time stamping where necessary) to ensure ease-of-use by both device makers and equipment suppliers. Standardization of equipment engineering data should allow reusable information extraction of high-level equipment performance metrics (example: run rate) and low-level equipment performance evaluation of critical process actuators (examples: pressure control, mass flow control, temperature control, etc.). Equipment suppliers will benefit from improved equipment engineering data by validating tools at an individual capacity/capability level. Capability level validation can be integrated to allow assessment of the whole equipment performance against designed capacity and ultimately visualize equipment quality. This solution will also promote development of third party data analysis applications.

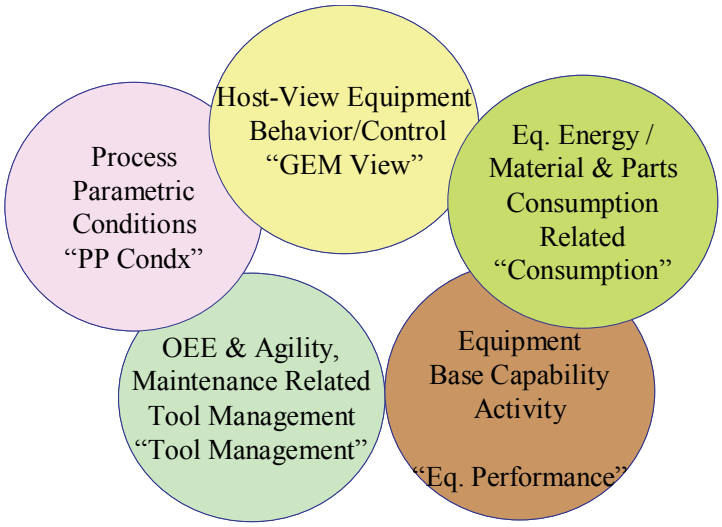



*Figure FAC8 Areas of Usage for Equipment Engineering Data*

## ENERGY CONSERVATION

The primary goal of energy conservation is to reduce facility operation cost by enabling facility demand based utilization model in which energy conservation plays a pivotal role. In 2007 the Factory Integration team worked on several initiatives within the facilities and production equipment sub-team to define energy conservation related challenges and the outcome of this work is reflected as a metric (tool idle versus processing energy consumption) in the Facilities technology requirements table. Also, the production equipment and facilities sub-teams are evaluating equipment sleep mode as a viable solution for energy conservation. Equipment sleep mode means that the equipment support units such as pumps will be shut down when no wafers are processed (i.e., when the tool is idle). However, it is also critical to ensure that shutting equipment components during idle mode should not impact productivity or yield. The facilities sub-team is also evaluating energy efficient solutions to facility units such as chillers, effluent systems etc. The factory integration team will work on energy conservation as one of the focus areas in 2008 and beyond to define technology requirements and potential solutions.

## 300′/450MM TRANSITION CHALLENGES

In keeping up with the Moore's law the semiconductor industry looks at increasing the wafer size as one viable option in addition to device innovations such as transistor design improvements, new materials, and lithography feature size reductions to reduce cost per function by ~30% each year over the past 30 years, while enabling factories to be highly productive. The last wafer size transition from 200 mm to 300 mm occurred 10 years ago and it is showing clear indication of ~30% cost improvement. As 300 mm wafer production enters its 4$^{th}$ major technology generation (45 nm), the industry must work on transition to 450 mm, in a seamless manner from the current 300 mm and the planned 450 mm. The 300′ activity is expected to address the seamless transition and to ensure the solutions are backward compatible as shown in Figure FAC9. The key goal of 450 mm transition is 30% improvement in cost/cm$^2$ (primary goal) and 50% cycle time reduction in days per mask layer.

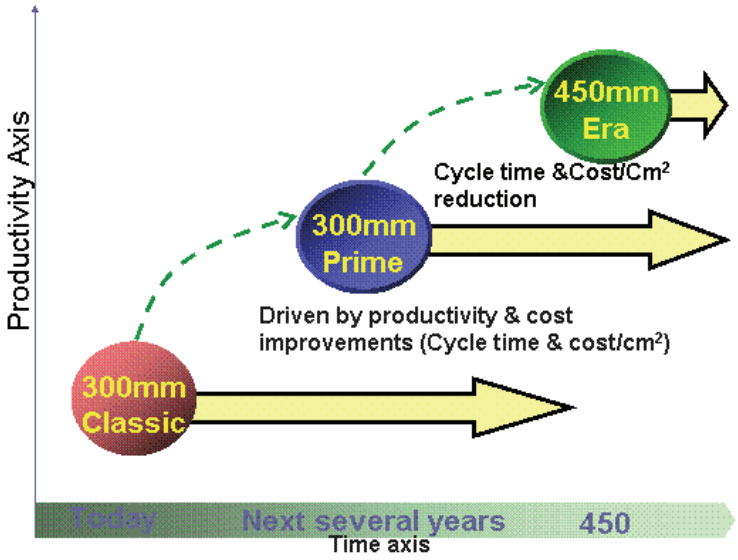



*Figure FAC9 Transition to 300' and 450 mm*

The Factory Integration team defined the 450 mm attributes and timeline needed for transition in Figure FAC10 and now it is mapping the ISMI and JEITA guidelines to each Factory Integration sub-teams areas of expertise from technology requirements and potential solutions perspective.

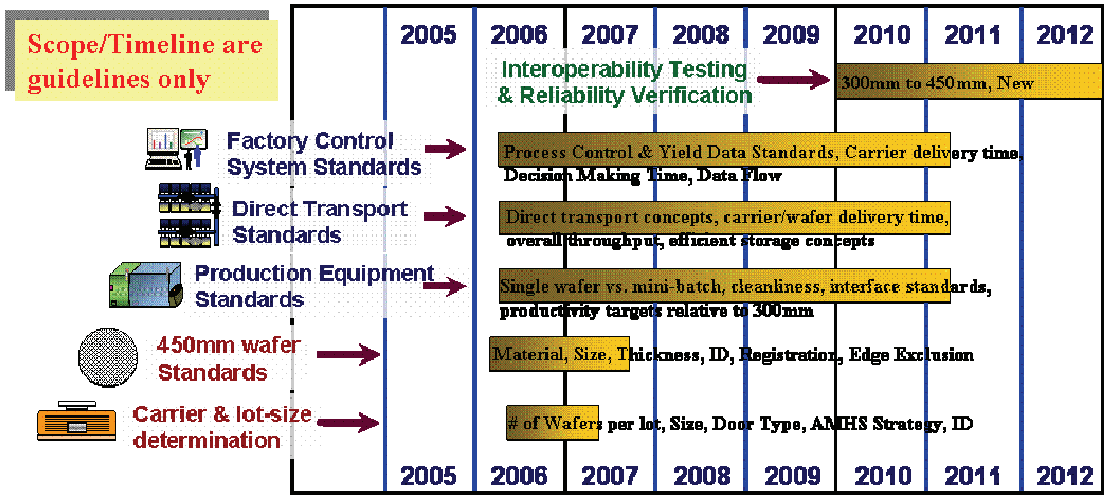



*Figure FAC10 450 mm Timeline and Key Attributes*

Ongoing discussions on the 450 mm wafer transition within the Factory Integration team and also with the other TWG uncovered several technical as well as business challenges. Table FAC9 lists the challenges captured from these discussions.

*Table FAC9 List of Next Wafer Size Challenges*

| *Technology WG* | *450 mm challenges* |
|---|---|
| FI – Factory Operations | Business model: Need to define operations axes:<br>High volume versus low volume<br>High mix versus low mix<br>Front end versus backend (Metal layers)<br>Cu/Al<br>Logic versus DRAM<br>WSPW (small versus large)<br>Transportation lot size versus carrier lot size<br>More single wafer processes<br>2–10 wafer lots<br>High mix issues<br>Cycle time issues |
| FI – Production Equipment | Mix use a certain small capacity mini-environment carrier<br>Conveyor transport<br>Small footprint tool buffering<br>300 mm to 450 mm conversion<br>Equipment platform concept and use of adaptor plate<br>Wafer gripping and edge exclusion<br>Alpha tool development, energy conservation |
| FI – Factory Information and Control Systems | Factory automation (load lock, transportation method, etc.)<br>Stringent process control needs for high mix small lot production |
| FI – AMHS | Conveyor transport may be required for 20k to 30k WSPM Fabs running small (5–10 wafer) lot carriers<br>Impact on MPH<br>Transport batch size |
| FI – Facilities | Extendibility of current fabs<br>Awareness of increased sub-fab area<br>Abatement point-of-use and new material issues<br>Height, vibration, and floor density<br>Energy conservation |
| Interconnect | Need a common team working on 450 mm issues (similar to 300i)<br>Wafer edge exclusion (1.5 mm?)<br>Cost of abatement due to NWS and new materials |
| Front end Process (FEP) | <br>Technical: meeting specs over larger areas)<br>Economic: for wafer, equipment, and metrology suppliers<br>Critical path definition: already late to meet development cycle<br>Standardization: wafer spec (type, thickness, diameter tolerance)<br>FEP will investigate at what generation we may have to switch to single wafer processing versus mini-batch and batch |
| Lithography | Current focus on Immersion and EUVL (power, consumables)<br>Fast reticle change<br>Vibration targets<br>Reticle storage issues<br>Stringent overlay requirements |
| ESH | Ergonomics, tool design, and chemical consumption concerns<br>AMC and particulate levels to be maintained<br>Regulations |
| Metrology | Need for Integrated Metrology continues<br>Data standards |
| Yield Enhancement | Wafer size configuration; traceability |
| Assembly & Packaging | Wafer package (FOSB, FOUP, door configuration, etc.) traceability |
| Other | Need a common team working on 450 mm issues (similar to 300i) and applying lessons learned from the 200 mm to 300 mm transition.<br>We need to learn from LCD manufacturers. |

It is imperative to start with defining key wafer attributes since in most cases, it drives the rest of the factory design decisions. To meet high-mix and fast cycle time requirements, it is likely that the industry may adopt a single-wafer processing strategy for all production equipment that would pose several challenges to equipment manufactures and operations that needs to be addressed in the coming years. In addition to single wafer processing versus mini-batch, it is necessary to evaluate the following: vehicle-based versus conveyor transport system; need for on-tool buffering; mini

environment carriers that allow mix use of different capacities (for example, bottom opening carriers), and flexible lot size. These critical decisions should be followed up by development of open industry standards in order to reduce the number of design permutations and to achieve cost-efficiency within the factory. It is imperative that the entire semiconductor members including the IC makers, foundry and suppliers work in unison to enable this timeline to keep up with Moore's law from an economics perspective.

## SUMMARY

Factory Integration chapter of the ITRS focuses on integrating all the factory components needed to efficiently produce the required products in the right volumes on schedule while meeting cost targets. In 2007, the Factory Integration chapter provides the technical requirements by the five sub-groups and also the proposed potential solutions. This section also provides Factory Integration related challenges from the crosscut issues and key focus areas (AMC, proactive visualization and energy conservation and 300′/450 mm challenges) that need to be addressed in order to keep up with the technology generation changes, productivity improvements and at the same time maintaining decades-long trend of 30% per year reduction in cost per function. The challenges addressed in the Factory Integration chapter is a combination of manufacturing, process and business related issues that needs to be comprehended collectively by the ITRS Factory Integration global team.