# INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

# 2007 EDITION

# MODELING AND SIMULATION

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# MODELING AND SIMULATION

## SCOPE

Technology Modeling and Simulation covers the region of the semiconductor modeling world called extended TCAD, and it is one of the few enabling methodologies that can reduce development cycle times and costs. Extended TCAD, within the scope of this document, covers the following topical areas, as shown in Fig. MS1: 1) *Equipment/feature scale modeling*—hierarchy of models that allows the simulation of the local influence of the equipment (except lithography) on each point of the wafer, starting from the equipment geometry and settings; 2) *Lithography modeling*—modeling of the imaging of the mask by the lithography equipment, the photoresist characteristics and processing; 3) *Front end process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding lithography; 4) *Device modeling*—hierarchy of physically based models for the operational description of active devices; 5*) Interconnect and integrated passives modeling*—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 6) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 7) *Package simulation*—electrical, mechanical, and thermal modeling of chip packages; 8) *Materials modeling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 9) *TCAD for design, manufacturing and yield*—the development of additional models and software to enable the use of TCAD to study the impact of inevitable process variations and dopant fluctuations on IC performance and in turn design parameters, manufacturability and the percentage of ICs that are within specifications; 10) *Numerical methods*—all algorithms needed to implement the models developed in any of the other sections, including grid generators, surface-advancement techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines. As shown in Figure MS1, these areas can be grouped into equipment-, feature and IC-scale. Items 8 to 10 are unique because they in fact cross-cut almost all other topics in Modeling and Simulation. Material and equipment issues are becoming more and more important in all processes as well as for active devices and interconnects. Numerical algorithms are shared by most of the areas in simulation.

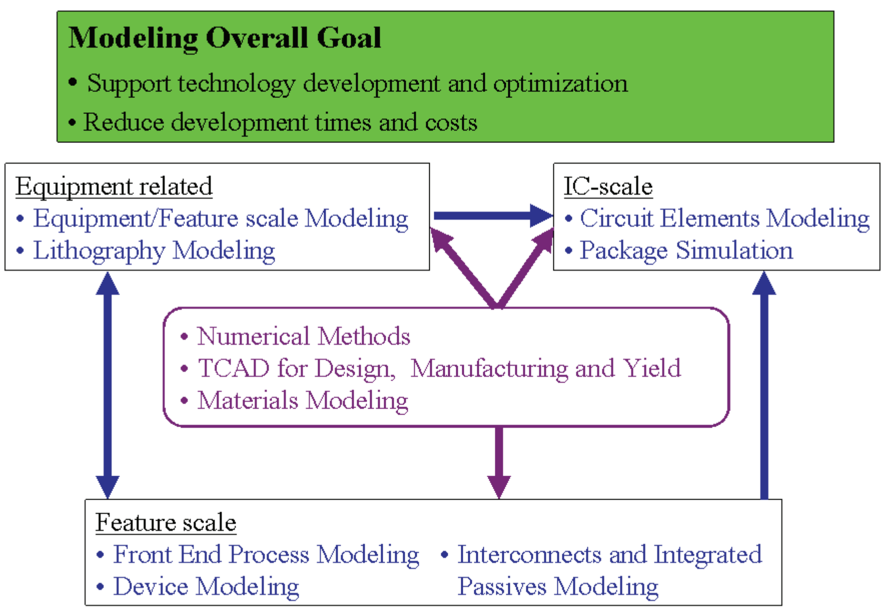


*Figure MS1 Modeling and Simulation Scopes and Scales*

Suppliers of modeling and simulation capability are mainly universities and research institutes funded by government and/or projects. TCAD vendors play an important role in the development of those capabilities, and are in most cases the interfaces between R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the development and optimization of technologies, devices, and ICs.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs. Currently, the shortage of such research funds is even more severe than the technical difficult challenges summarized below. For example, several Modeling and Simulation requirements listed in the 2005 ITRS had in this 2007 issue to be pushed out and delayed in time because sufficient R&D could not be done due to insufficient research funding.

# DIFFICULT CHALLENGES

The difficult challenges highlighted in Table MS1 are those Modeling and Simulation requirements which on one hand must be met in time to support the high-level progress of the roadmap and on the other hand are most critical to fulfill due to their technical difficulty and the R&D resources needed. Additionally, it should be noted that a key difficult challenge present across all the modeling areas is that of experimental validation. This challenge is especially difficult because for most processes many physical effects interact with each other and must be appropriately separated by well-selected experiments, in order to be able to develop predictive models and not simply fit experimental data. As devices shrink and new materials are introduced into the technology arena, new and enhanced analytical techniques are vital that can extract the necessary information for this model development and evaluation validation from the experiments. This critical need is mentioned as a cross-cut item with the Metrology ITWG.

*Table MS1 Modeling and Simulation Difficult Challenges*

| *Difficult Challenges ≥ 22 nm* | *Summary of Issues* |
|---|---|
| Lithography simulation including EUV | Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system |
| | Models and experimental verification of non-optical immersion lithography effects (e.g., topography and change of refractive index distribution) |
| | Simulation of multiple exposure/patterning |
| | Multi-generation lithography system models |
| | Simulation of defect influences/defect printing |
| | Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography |
| | Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects and ultra-high NA effects (oblique illumination) |
| | Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, mechanical stability, and time-dependent effects in multiple exposure |
| | Resist model parameter calibration methodology (including kinetic and transport parameters) |
| | Simulation of ebeam mask making |
| | Simulation of directed self-assembly of sublithography patterns |
| | Modeling lifetime effects of equipment and masks |

*Table MS1 Modeling and Simulation Difficult Challenges*

| *Difficult Challenges ≥ 22 nm* | *Summary of Issues* |
|---|---|
| Front-end process modeling for nanometer structures | Diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers<br>Modeling of epitaxially grown layers: Shape, morphology, stress<br>Modeling of stress memorization (SMT) during process sequences<br>Characterization tools/methodologies for ultra shallow geometries/junctions, 2D low dopant level, and stress<br>Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces<br>Efficient and robust 3D meshing for moving boundaries<br>Front-end processing impact on reliability |
| Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability | Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...), and simplified but physical models for complex chemistry and plasma reaction<br>Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)<br>Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)<br>Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling<br>Efficient extraction of impact of equipment- and/or process induced variations on devices and circuits, using process and device simulation |
| Ultimate nanoscale device simulation capability | Methods, models and algorithms that contribute to prediction of CMOS limits<br>General, accurate, computationally efficient and robust quantum based simulators including fundamental parameters linked to electronic band structure and phonon spectra<br>Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS<br>Models (including material models) to investigate new memory devices like MRAM, PRAM, etc.<br>Gate stack models for ultra-thin dielectrics<br>Models for device impact of statistical fluctuations in structures and dopant distribution<br>Efficient device simulation models for statistical fluctuations of structure and dopant variations and efficient use of numerical device simulation to assess the impact of variations on statistics of device performance<br>Physical models for novel materials, e.g., high-k stacks, Ge and compound III/V channels …: Morphology, band structure, defects/traps...<br>Reliability modeling for ultimate CMOS<br>Physical models for stress induced device performance |
| Thermal-mechanical-electrical modeling for interconnections and packaging | Model thermal-mechanical, thermodynamic and electronic properties of low κ, high κ, and conductors for efficient on-chip and off-chip including SIP layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension<br>Model effects which influence reliability of interconnects/packages including 3D integration (e.g., stress voiding, electromigration, fracture, piezoelectric effects)<br>Models to predict adhesion on interconnect-relevant interfaces<br>Simulation of adhesion and fracture toughness characteristics for packaging and die interfaces<br>Models for electron transport in ultra fine patterned interconnects |
| Circuit element and system modeling for high frequency (up to 160 GHz) applications | Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies and package:<br>- possibly consisting of different technologies,<br>- covering and combining different modeling and simulation levels as well as different simulation domains |
| | Scalable active component circuit models including non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling |
| | Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, RF MEMS switches, … |
| | Physical circuit element models for III/V devices |
| | Computer-efficient inclusion of variability including its statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently |
| | Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations |

*Table MS1 Modeling and Simulation Difficult Challenges*

| *Difficult Challenges < 22 nm* | *Summary of Issues* |
|---|---|
| Modeling of chemical, thermomechanical and electrical properties of new materials | Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following:<br>1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions.<br>2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties<br>3) Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. Modeling-assisted metrology.<br>4) Accumulation of databases for semi-empirical computation. |
| Nano-scale modeling for Emerging Research Devices including Emerging Research Materials | Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), quantum dots, molecular electronics, multiferroic materials and structures, strongly correlated electron materials)<br>Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …) |
| Optoelectronics modeling | Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling.<br>Physical design tools for integrated electrical/optical systems |
| NGL simulation | Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects and impact on LER); heating and charging effects), including impact on device characteristics (e.g., due to local crystal damage by electron scattering or charging effects)<br>Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process) |

## DIFFICULT CHALLENGES ≥ 22 NM

*Integrated modeling of equipment, materials, feature scale processes, and influences on devices*—Inhomogeneities of the results of a process step caused by the fabrication equipment used are key issues for manufacturability and yield of a technology. This refers especially to inhomogeneities across the wafer or between different wafers, and to drifts of process results between maintenance of equipment, for example, due to coating of chamber walls. Processes where these effects are especially important are presently plasma deposition and etching, chemical vapor deposition, electroplating, and chemical mechanical polishing (CMP). Generally, predictive simulation is still limited by lack of knowledge of the physical properties of materials and the chemical processes involved. The development of accurate models for reactions paths, the extraction of reliable values for the required parameters, and also the development of reduced chemistry models that include only the primary mechanisms needed for practical applications is an important challenge. For better linking with feature-scale simulation, surface chemistry and plasma-surface interactions must be appropriately modeled. Integrated equipment and feature scale simulation has become increasingly important for processes where a clear separation and interface between equipment- and feature-scale effects cannot be defined. Furthermore, statistical variations of the processes are getting more and more important. The impact of equipment and/or process induced variations on devices and circuits must be assessed, which needs corresponding improvements of process and device simulation tools. This challenge is being addressed below in the subchapter on Equipment/Feature Scale Modeling.

*Lithography simulation including EUV*—Various tricks have been introduced to extend the applicability of optical lithography to even smaller dimensions, with substantial support from lithography simulation. The further technological development also requires large additional improvements in the area of lithography simulation, among others because the number of available resolution enhancement techniques increases. Simulation of immersion lithography must be further improved by inclusion of various effects which were so far not considered. Compared with the 2005 ITRS, the most important new aspect of this challenge is the simulation of the various options of multiple exposure/patterning. Creation of improved modeling approaches for optical proximity correction (OPC) and phase shifting masks (PSM) synthesis is an important challenge, including the combined optimization of light sources and masks. Developing predictive models for chemically amplified resists is a continuing challenge, which further grows due to the need to cope with time-dependent effects in multiple exposure. But if the models were developed, they would greatly expand the application area of lithography modeling. The lithography simulation challenge extends from feature scale to full chip, from equipment and mask effects to defect printing on the wafer, and from prediction of nominal CD values and resist shapes to process windows, and lifetime effects of equipment and masks. It is being addressed below in the subchapter on Lithography Modeling.

*Front-end process modeling for nanometer structures*—This is the key challenge for the prediction of result from device fabrication. It overlaps to some extent with the challenge "Ultimate nanoscale CMOS simulation capability," which also includes materials and device simulation. Most important and challenging in the area of front-end process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants. As an alternative the formation of doped epitaxial layers must be simulated, including their shape and morphology, defect status, and stress. Due to the strongly reduced thermal budgets needed for shallow junctions, that process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of these two. Implantation damage, amorphization, re-crystallization, and silicidation must be accurately simulated. Anisotropy in models and parameters potentially introduced by thin layers must be investigated. In view of the need to increase carrier mobilities in the channel, the modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and for SOI structures. Moreover, stress history and memorization during process sequences is important and must be simulated. Model development, calibration, and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects, and stress, especially regarding two- and three-dimensional measurements. To enable efficient and accurate three-dimensional simulation, meshing for moving boundaries needs to be strongly enhanced. This challenge is being addressed below in the subchapter on Front-End Process Modeling.

*Ultimate nanoscale CMOS simulation capability*—A fundamental question of the microelectronics industry continues to be what the ultimate limits of CMOS technology and devices are. The key requirement to deal with this challenge is predictive simulation of materials, processes, and device behavior including reliability. Material models are needed especially for gate-stacks including high-κ materials, for stress-engineered and Ge or compound III/V channels, for interconnects including size-dependent resistivity of copper and low-κ dielectrics, and for nonlinear photoresists. Due to the short-term need, such material models may in part still be phenomenological rather than derived from first principles. In addition, quantum-based and non-equilibrium (ballistic) device simulations are needed. Simulations must also be applicable beyond standard planar CMOS. Stress engineering must be enabled. Besides accuracy, efficiency and robustness are key issues. Both atomistic and process-induced fluctuations critically affect the manufacturability of the ultimate CMOS devices and must therefore be dealt with in simulation. This challenge crosscuts most of the subchapters below.

*Thermal-mechanical-electrical modeling for interconnections and packaging*—Performance and reliability of integrated circuits is increasingly affected by interconnects and packaging. Electrical, thermal, and mechanical properties highly interact with each other and must therefore be simulated together. Reliability issues requiring modeling include electromigration, stress voiding, integrity and adhesion of thin films, surface roughness, package fracture, and corrosion. The capability to withstand the heat produced in the IC and to transport it off the chip is getting a top-level concern with further increasing densities. New materials such as low-κ are being introduced to meet the targets of the roadmap. Thermal modeling of high-κ materials in gate stacks is also required. Due to their variety and lack of knowledge of their properties these two kinds of materials require large efforts on the development of models. Processing affects both material properties and the three-dimensional shape of interconnects. These non-idealities must be considered in the simulations. This challenge is being addressed below primarily in the subchapter on Interconnects and Integrated Passives Modeling.

*Circuit element and system modeling for high frequency (up to 160 GHz) applications*—Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS-, and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

## DIFFICULT CHALLENGES < 22 NM

*Modeling of chemical, thermomechanical, and electrical properties of new material s*— Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Devices (see the ERD and the ERM chapters). In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Furthermore, computational material science needs to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations. This challenge crosscuts most of the subchapters below.

*Nano-scale modeling*—Within the Emerging Research Devices chapter new device structures such as nanowires, carbon nanotubes, nanoribbons, quantum dots, molecular electronic, multiferroic materials and structures, and strongly correlated electron materials are being discussed as good candidates to complement CMOS in the long-term. For the assessment and optimization of such devices and their fabrication technologies suitable process and device simulation tools must be developed, including e.g., quantum transport, tunneling phenomena, and spin transport. This challenge crosscuts many of the subchapters below.

*Optoelectronics modeling*—Further increasing frequencies and the upcoming limitations of metal interconnects make the link between electrical devices and optical interconnects an interesting option. Tools for the simulation of the fabrication of optical interconnects and of the performance of integrated electrical/optical systems must be developed. Also in this area material models must be included. This challenge refers primarily to the subchapter on Interconnects and Integrated Passives Modeling below.

*NGL simulation*—The modeling and assessment of next generation lithography options—beyond optical and EUV lithography—is vital to help to make choices and to make the introduction efficient. Currently the prioritized options include mainly mask less lithography by e-beam direct writing, and nano imprint. In both cases, again advanced resist modeling is very important and substantially different from the optical and EUV lithography options preferred in the short-term domain.

# TECHNOLOGY REQUIREMENTS

In the following paragraphs the needs for each of the ten topical areas mentioned in the Scope are discussed in more detail. As mentioned above the areas "Materials Modeling," "Equipment/Feature Scale Modeling," "TCAD for Design, Manufacturing and Yield," and "Numerical Methods" are crosscutting all the other areas. Therefore, in addition to being discussed in their specific sections, they are also mentioned in many of the other paragraphs.

## EQUIPMENT / FEATURE SCALE MODELING

Equipment and feature-scale modeling involves simulation of reactor-scale effects such as geometry and extrinsic process variables like pressure, pad roughness, etc. in combination with pattern and feature-related effects, such as surface chemistry and local temperature variations, to accurately predict process results. So far feature scale simulation and equipment models have mostly been addressed separately in the context of multi-scale-length modeling with various approximations developed to link scales. The mission of equipment modeling is evolving in its scope and now includes unit process simulation (such as quantitative simulation of individual process steps) through to integration of hierarchical simulation levels and process steps. In this respect, the entire manufacturing life-cycle starting with the concept and feasibility and ending in continuous improvement will be increasingly impacted by equipment simulation that is based on fundamental phenomena and mechanisms. Many of these themes are being addressed concurrently within the various technical communities where there are logical interfaces. New efforts require multidisciplinary approaches and tight coupling to associated technical areas such as lithography, metrology, front-end TCAD, material sciences, mechanics, and *ab initio* computations methods.

Though the task of integrating the various disciplines into one comprehensive approach accounting for physics and chemistry on a microscopic level is formidable, it appears, in view of the skyrocketing cost of experimentation and in view of the multitude of variables, only prudent. Equipment design with the aid of computational electromagnetism and computational fluid dynamics including plasma and chemical reactions is becoming more significant. Analysis and design of nano-scale process will be improved with modeling and simulation of chemical and surface reactions at the feature scale. The technological issues for the equipment / feature scale modeling are summarized below.

- *Data needs*

  The first-principles nature of the advanced process and equipment simulation requires a more comprehensive process characterization and fundamental data input both in terms of material and surface as properties as well as in terms of parameters characterizing the underlying microscopic mechanisms.

  In the realm of CVD and ALD the required data starts with the description of the precursors, species transport, bulk reactions, and surface interactions. Quantum chemistry tools are available to characterize most reactive systems. However, they are inadequate without streamlined computational approaches linking *ab initio* data to macroscopic models for a self-consistent simulation capability. The streamlining is also imperative to speed up the rate of mechanism calibration. A good example is the required quantum chemical characterization of precursors used for high-κ dielectric deposition.

  In plasma processes, electron impact cross-section and kinetic data for radicals, dissociation fragments, and excited states are crucial ingredients for predictive simulation. Emphasis should be placed on realistic determination of dissociation pathways leading to important precursors. Judicious approximations will be required to characterize excited states of the species and product decay cascades. It is obvious that such data requirements will put a heavy burden on special experimental arrangements and novel test vehicles to provide viable model input data. The most neglected area in this regard is the lack of fundamental data for plasma-surface interactions (especially for photoresist, ULK materials, metal composites, and alloys). One approach is the employment of molecular dynamics. It should target metal alloys deposition processes for advanced metallization in interconnect and gate stack applications for MOSFETs. Specific needs include microscopic representation of metallic systems in terms of improved inter-atomic potentials and a microscopic representation of amorphous surfaces and doped films.

  In the CMP arena, basic process characterization is poorly understood and more systematic and fundamental approaches to characterize these systems are required. Experimental data is needed to characterize the wear of polishing pads and conditioners as a function of process conditions, along with their dynamic impact on polish rates. In the case of electro-CMP, the adsorption/desorption behavior of slurry additives on the deposition surface and in the presence of an electric field is largely unknown, and their temporal decomposition characteristics in the bath poorly understood.

  In addition to its importance in ECMP, electroplating would benefit from quantum chemistry calculations being extended to liquid systems, particularly in the presence of electro-magnetic fields. The modeling of electroless deposition with complex bath and surface chemistries for the deposition of CoWPM system materials has an especially strong need for fundamental quantum chemistry derived bath-kinetic and surface kinetic parameters.

- *Model validation and empirical model development*

  One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films and ultra-fine structures. Cost-effective verification of process chemistry models is needed. For CMP, measurements of the various physical parameters related to processes involving consumables such as polishing pads, conditioner disks, and slurries are at an immature state. For plasma, CVD and ALD models, surface process chemistry diagnostics such as pin hole experiments that characterize the transport of species to the wafer and through a facsimile of a feature need to be proliferated. Approaches whereby surfaces may be probed *ex situ* and returned to an *in situ* state in real time should be exploited for highly non-equilibrium processes. Standards of test structures (such as overhang cavity structures) and wafers dedicated to specific diagnostics such as temperature measurement are also needed for model calibration and process control. Enhanced capability real time FTIR, interferometry, and improved post-mortem diagnostics such as XPS and SIMS will be needed to validate coupled atomistic-scale to chamber-scale models of device fabrication.

- *Feature scale simulation and integrated model development*

  Internal dynamic equipment settings or preconditions require a high degree of fidelity in the coupling between equipment chamber models and feature scale models. For example, the impact of chamber condition on feature evolution is a well-known phenomenon though a minimally researched topic. In the case of plasma processes (including plasma ALD), particular attention needs to be paid minimizing numerical roughness for better resolution of the topography evolution of thin films. In general, new materials introduced at an ever more rapid pace at advanced technology generations entails inherently more complex process-surface material combinations and reactions. Specific experiments and an increasing reliance on atomistic simulation will be required to sort through the myriad processes on surfaces. Related aspects of plasma etching include line edge roughness (LER), gate profile control, process induced damage (PID), and maintenance of electrical and mechanical integrity (stress) of devices.

Feature-scale models can often provide basic understanding of process details such as trench fill and etch residue effects, but the full benefit is often realized by integration with an associated equipment-scale model. Reactor-scale effects can often have a first order effect on feature-scale results and linking between atomistic feature-scale simulations and reactor-scale models needs to be standardized to help accommodate this linking.

Related to the feature/reactor linking problem are the problems of integration of models for various processes. Numerical infrastructure of process integration is complex and by no means standard. Communication between various unit process simulation tools (including layout tools) is of crucial importance. Specific opportunities exist in first-principles based tiling design and integration guided mask design. Models capturing process variations (lot-to-lot or tool-to-tool) present even a bigger challenge.

- *Multi-generation equipment / wafer model*

  Historically equipment models have been very module focused with various researchers using different solvers, discretization methods, and mesh generators. The area would benefit from uniformization of these various components allowing the physics of the problem and boundary conditions to be the only focus. This has happened to some extent but an effort to move in the direction of a standardized workbench for physical model development could be beneficial for faster development of new module simulations as well as for smoother development of integrated models, as discussed above.

- *Removal process*

  Although the algorithms for modeling of plasma etching seem to be mature, the capability of quantitative prediction strongly depends on the fundamental data of physical, chemical, and surface reactions. Similarly, modeling of the removal processes for CMP and electrochemical polishing (ECP) are becoming important. In each process, predictions on full wafer, chip level, and pattern dependent effects are required.

- *Deposition process*

  Similar to removal processes, modeling for CVD process including PECVD has matured. However, as new materials are introduced for MOCVD process, fundamental chemical data for these materials are indispensable. Material modeling is expected also from process modeling. Modeling for other deposition processes like ALD, electroplating and electroless deposition are expected to be developed.

## LITHOGRAPHY MODELING

Lithography modeling and simulation needs have been sub-divided into five areas: 1) image modeling, 2) electromagnetic scattering analysis, 3) resist modeling, 4) integrated modeling systems, and 5) coupling of metrology and modeling. These areas are discussed below.

- *Image modeling*—More accurate, flexible, and efficient imaging models are needed for simulation support in the development of new process technology, e.g., double patterning. The existing models and software implementations have to be critically evaluated with respect to their capability to describe polarization effects that occur at extreme numerical apertures, especially in immersion lithography, including effects at the lens-liquid interface for high index materials. Advanced image models must cover all types of polarization effects such as spatial variation of polarization inside source and projector pupils, birefringence of lenses and mask blanks, the spatial variation of lens transmission, and polarization aberrations. For EUV lithography, high NA and innovative illuminator designs that are able to address the requirements of high volume production tools pose extra modeling challenges. Additional polarization (variation) effects introduced at interfaces such as lens or mirror surfaces, mask backside, or mask pellicle need to be considered as well. Improved simulation approaches are required to describe flare effects resulting from physically rough surfaces in lithographic imaging systems, where the different nature of EUV and optical flare needs to be reflected in the model.

- *Electromagnetic scattering analysis*—Electromagnetic scattering analysis must become part of the mainstream investigation capability. Scattering from topographic (even binary) masks and from wafer topography underlying more or less planarizing layers or resist are two examples of applications requiring rigorous electromagnetic capability. The performance of different modeling approaches such as finite difference time domain algorithms (FDTDs), modal methods (WaveGuide, rigorous couple wave analysis [RCWA]), and finite element methods have to be critically evaluated in terms of accuracy, memory requirement, and computing speed. More efficient modeling techniques are needed for the critical evaluation and optimization of reticle-related optical resolution enhancements and for the description of light scattering from mask defects. The accuracy of approximative methods such as mask decomposition techniques and boundary layer models must be evaluated over a wide range of lithographic process parameters. For EUV masks in particular, a fully rigorous treatment of the electromagnetic fields propagating through the reflective multi-layer sandwich structure or the absorber layer(s) and investigation of mask shadowing effects, especially for various OPC schemes, which may be needed for patterning at 22 nm and below, is required. The severity (or printability) of inherent multi-layer and absorber defects needs to be analyzed carefully, as well as the impact of defects or particles added on surfaces during handling. Phase effects (due to structured multi-layers) or incoherence effects (due to the finite size of the light source and the variation of the incidence angle across the exposure slit) and their impact on OPC need to be taken into account. With smaller mask structures, effects due to absorber roughness and their impact on line edge roughness (LER) and wafer CD variation become more important.

- *Resist modeling*—Predictive, quantitative resist modeling will continue to be the bottleneck in lithography simulation. Accurate models for chemically amplified resists, which include solvent diffusion, post-apply bake, post-exposure bake, diffusion (or acid and quencher), line edge roughness, and surface interactions, are needed and must be capable of correctly predicting three-dimensional resist patterns. Model extensions are required to describe immersion-specific effects such as leaching of different chemical species from the resist into or back from the immersion fluid. New process technologies such as double patterning might require materials with advanced properties such as non-linearity or reversible bleaching and multilayer resist systems, which need to be captured by the corresponding models. The performance of simplified resist models such as diffused aerial image approaches or a lumped parameter model must be evaluated in comparison to full resist models. Thin and multilayer resist models that link the lithography to the etch process are becoming important. Photoresist patterns must be evaluated with respect to their etch resistance and mechanical stability. Because of the increasing importance of polymer-size effects, e.g., their impact on line edge roughness and line width variation, there is a growing need for resist studies based on mesoscopic models and/or computational molecular modeling and stochastic modeling. The modeling of the trade-off among LER, resolution, and sensitivity requires special attention.

- *Integrated modeling systems*—For lithographic imaging close to the theoretical resolution limits, the interaction among different components of the lithographic system such as the illumination system, the mask, the projection system, and the resist over wafer topography becomes increasingly complex. With so many independent parameters, and an avalanche of data to understand, computer-based optimization systems are a requirement to fine-tune future technologies that will operate near the limit of diffraction optics. Specifically, this includes the optimization of mask and source parameters in optical resolution enhancement techniques and the ability to understand how the resist response influences these optimal parameters. New integration techniques like double patterning come along with additional etch, deposition, or planarization techniques that need to be considered in lithography simulation. The influence of underlying wafer topography must be understood and eventually taken into account. Integrated modeling systems are also required for extensive defect printability studies from the mask through the final product. Further, as double exposure approaches become more popular, optimization becomes even more difficult and resource-consuming.

  The link between lithography simulation and OPC application becomes more important: OPC model generation requires assistance by predictive, rigorous simulation models in order to generate accurate OPC models for the most advanced nodes within adequate time. Corresponding standardized interfaces between tools need to be provided.

- *Model calibration: coupling of metrology and modeling*—More predictive process simulation requires a stronger connection between models and metrology tools. Methods have to be developed that translate the output of metrology tools into appropriate simulation parameters. A more fundamental understanding about the generation of metrology data, eventually through simulation, is necessary to extract meaningful evaluation parameters from simulation results. While aberration data for lenses and the measurement of illumination source shapes have become common, full polarization-specific characterization of sources and lenses is required. With the use of electromagnetic scattering simulations, accurate three-dimensional shapes and optical parametric descriptions of all mask materials are now required. Experimental schemes for the measurement of resist parameters, especially for 193 nm immersion and EUV, have to be devised or improved. Methods that are developed to simulate lithographic processes can also be used to evaluate metrology tools. This includes mask inspection, modeling of wafer alignment signals to analyze the process impact on overlay, aberration measurement, and the extraction of resist modeling parameters from appropriate measurements.

Besides the classical application areas of lithography simulation mentioned above, simulation activities in associated fields are becoming increasingly more important. Light sources are key drivers of any lithography technique; however, modeling related to their development, above all EUV source-related, should require particular attention, especially with respect to sources for high volume manufacturing. On the mask manufacturing side, in defect inspection, modeling is used to determine the potential impact on patterning. Modeling also helps in on-going discussion of actinic vs. non-actinic defect inspection.

Simulation models must be validated across multiple lithographic conditions and multiple feature types, sizes, and pitches for 2D and 3D profiles by appropriate experiments. Extensive benchmarking can help to evaluate the accuracy of models to identify the most efficient modeling approaches. Specifications for numerical accuracy and overall simulation uncertainty historically have been vague and not well understood. Careful attention to calibration and validation will allow the use of simulation results with an appreciation for their uncertainty.

The massive application of optical resolution enhancement techniques such as OPC, PSM, polarization, and off-axis illumination will increase the importance of lithography simulation for process development and optimization. The combination of well planned experiments and predictive lithography simulation will help contain process development costs and accelerate the process development cycle.

An important application of simulation for the next few technology generations will be the evaluation of trade-offs for the various lithography options (such as EUV versus 193 nm double patterning/exposure water immersion vs. single exposure high index immersion lithography) with respect to commercial viability. For next-generation lithography technologies, reliable simulation tools are needed in EUV for direct e-beam, maskless lithography (ML2) techniques, and nano-imprint, here especially for the associated resist process.

In general, the computational needs of simulations are becoming more challenging: smaller patterns including sub-resolution features or higher accuracy requirements push algorithms to finer resolution, increasing memory and CPU time consumption significantly. Simulation steps or algorithms being time-critical for generating results need to comply with 64 bit requirements and should support parallelization on high performance computation clusters.

## FRONT-END PROCESS MODELING

Front-end process modeling includes the simulation of the physical effects of manufacturing steps used to build transistors up to metallization. However, lithography simulation is discussed here in a separate subchapter, see above. These areas are important for understanding and optimizing transistor fabrication, pushing the limits of scaling traditional planar devices, and evaluating process issues in alternative device architectures. The needs for modeling are driven by the reduction of feature size in scaling transistors and by the increasing number of new materials being considered to overcome scaling roadblocks. These not only cause higher demands on model accuracy but also require models for effects considered as second order effects in the previous node, or models of new materials, material properties, and doping techniques as well as the introduction of new simulation flows.

With the reducing thermal budget, accurate lateral doping and damage distributions need to be modeled. Monte Carlo implant models are definitely required for application that cannot be adequately addressed by analytic models, for example, doping of sidewalls of narrows trenches, channel doping steps including S/D, LDD, and pocket. Analytic models will need to be refined with respect to lateral dopant and damage distributions. Modeling needs to be extended to include damage kinetics during the ion implant process step especially for “cocktail ion implant” and subsequent annealing process in silicon and silicon-related materials. The range in energy is large from very low energy (less than 1 KeV) where the interface has a large contribution to high-energy (some MeV). Model-based evaluation of alternative doping processes such as solid source and plasma immersion ion implantation (PIII) will also play a valuable role.

An optimum trade-off between minimized dopant diffusion and sufficient (maximized) dopant activation is the key for the formation of shallow junction and low device access resistance. Improved physical understanding of the related mechanisms is therefore directly important for technology development and also the prerequisite for any work on physical modeling. For doping diffusion and activation, continuum models still remain the mainstay of process simulators even if Kinetics Monte Carlo techniques are very promising. These continuum models need continued refinement to be able to adequately capture technologies with reduced thermal budgets and a wider range of impurity species, including the effect of the pre-amorphization techniques. Point-defect based diffusion models will need to be considerably refined especially concerning the kinetics of dopants and defects in clustering and activation, in addition to capturing traditional transient enhanced diffusion effects. RTA ramp rates are an important factor, and the simulation of their influence in diffusion/activation models needs to be improved. Models also need to consider experimental conditions different from traditional furnace or rapid thermal anneals, especially flash annealing and ms laser annealing. The effect of interfaces, especially non-$SiO_2$ interfaces, is becoming increasingly important. Here, the segregation and trapping of impurities needs to be modeled for all kinds of dielectrics, including high-κ material stacks, taking the influence of N, C, F, Ge, and metallic impurities and of knock-on oxygen into account. Moreover, as the mechanical stress engineering plays a crucial role in the CMOS technology improvement roadmap, all these models on diffusion, clustering, and dopant activation must take into account locally the effect of the mechanical stress.

Advanced process models will be needed for the modeling of metastable dopant activation (above solid solubility). These should include activation kinetics considering the reduced front-end thermal budget and deactivation kinetics during subsequent backend processing. Models for surface and interface diffusion will be needed. These include interactions with $SiO_2$ and new gate dielectric materials. Process models for diffusion/activation in alternative materials (such as SiGe or SiGe:C) need also to be improved, as well as those for very thin body (such as SOI) needed with or without any intrinsic mechanical stresses where interaction with interfaces is of first order.

Atomistic process models are beginning to play an important role, both as direct simulation approaches for front-end processes and as a pathway to improved continuum model or Kinetic Monte Carlo model development and parameter extraction. Detailed insight into dopant-defect interactions using *ab initio* methods will be needed for understanding the kinetics of reduced thermal budget processes and the role of other impurities such as Fluorine, Carbon, or Germanium. Computational materials science will also allow atomistic studies of new processes, materials, and interfaces, such as high-κ dielectric deposition and interface properties. Hierarchical modeling from ab initio calculations to continuum needs still to be developed and incorporated into mainstream TCAD flows.

As engineering of mechanical stress effects for device mobility improvement is becoming increasingly important, models for the effect of stress on reliability, dislocation generation, and dopant diffusion need to be developed. Stress resulting from all process steps including those coming from material texture modification and including stress generated by the presence of impurities, clusters and extended defects must be considered over the full range of temperatures used in processing and must be transferred to device simulation tools. Thin film growth needs to be better modeled, such as silicide film, including the reliability impact of stress in corners and small 3D structures, as well as the defect generation in such a structure.

For advanced gate stacks, modeling of high-κ dielectric film properties, interactions with substrates, and properties/ interactions with metal gates is a critical need to enable continued equivalent oxide thickness (EOT) scaling. Models should span from deposition conditions through geometrical shape of the gate stack to structural properties such as interface defect density for use in device simulation or for reliability issue such as the NBTI in thin oxide films.

Feature-scale models for deposition and etching, including CMP, need to be linked to equipment simulation. This linkage will allow determination of the influence of equipment settings on feature topography as well as on inhomogeneities on the wafer and from wafer to wafer. This should also result in more physical feature scale models in particular for the last introduced deposition techniques such as MOCVD or ALD and for epitaxial growth of semiconductors and dielectrics. Modeling of these processes will become more critical as the industry moves beyond planar MOS to more complex device structures and 3-D integration schemes.

For each of these front-end modeling areas, approaches need to be developed to enable estimation of the performance impact of variation in critical front-end process steps. These include random effects such as random dopant fluctuation and systematic effects such as within-wafer etch variation. These effects, tightly linked to modeling of equipment such as lithography variations due to proximity effects and line edge roughness, are required for a better DFM strategy.

Improved metrology and analytical techniques are essential for the determination of accurate process models, especially tools for these ultra shallow geometries, thin films and dopant levels. Novel materials/interface measurement techniques for these new materials systems are also required.

## DEVICE MODELING

Device modeling refers in general to a suite of models and methods describing carrier transport in materials. Models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and CPU intensive ones as the energy balance, which solve some higher moment simplification of the Boltzmann equation. In addition, the complex physics of today's devices mandates at times the usage of Monte Carlo codes, which stochastically solve the Boltzmann equation, and the usage of Schrödinger solvers that account for quantum effects. The choice of the appropriate model depends on the problem and the level of details required and it is therefore left to the user. Despite the significant advances of recent years in both numerics and physics, continuing development is required to meet the increasingly challenging industry needs for device exploration and optimization. Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount. What follows is a list of the most outstanding limitations.

*Gate stack*—Gate dielectrics have become so thin that tunneling gate current is today an important design factor. Comprehensive quantum modeling of the entire gate stack (channel-dielectric-electrode) is needed to represent the behavior of oxides and nitrided-oxides that are only a few atomic layers thick. It must include details of tunneling and charge transport in the dielectric, effective dielectric constants of complex dielectric stacks, interface states and trap distribution in high-κ materials. Fundamental material modeling should be intensified to aid in the search for alternative, high-κ gate dielectrics and their evaluation. The focus has to be on their resulting flat-band shift and hysteresis effects by Fermi-level pinning and oxygen vacancies, threshold and capacitance characteristics, channel mobility and reliability.

*Stress and strain*—Different materials in source-drain and layer stacks and thermal budget of processing result in stress and strain fields that increasingly determine the device characteristics. In order to predict currents correctly for all possible channel orientations a full-tensorial description of arbitrary stress fields has to be included. Comprehensive models must include the effect on band-structure (band-edges, effective density-of-states, effective masses). The effects on mobility are of paramount importance. They include anisotropic piezoresistivity, which is caused mostly by the effective masses but also by momentum relaxation times, as well as stress dependence of saturation velocity.

*Contact resistance*—With shrinking device dimensions, the contact resistance contribution to the total device resistance (channel, S/D, contact) will increase and thus will play a more important role in predictive simulation of the current-voltage characteristics and transconductance. A correct modeling of contact and sheet resistance (high doping activation and mobility) is a prerequisite for a correct device description.

*3D modeling*—Especially for narrow devices (e.g., Flash or SRAM memory cells) the coupling among the various spatial directions require a full three-dimensional device modeling taking into account realistic 3D geometries and doping distributions. Effects such as gate line edge roughness or width dependence greatly impact devices output characteristics and they need to be taken into account during device optimization studies. This implies that 3D simulations are no longer reserved for occasional, limited use but are a real need for everyday tasks. Therefore, device editors productively coupled to process emulators and simulators, meshing algorithms and solvers have to be enhanced to the point that 3D tools have complexity and computational requirements similar to 2D.

*Dopant fluctuations*—The ever shrinking geometries have created a singular problem unlike any other: Because of the small volumes involved modest fluctuations of implanted dopants will give rise to considerable differences in doping concentration, which in turn will have a tremendous impact on devices characteristics. Similar effects arise from fluctuations in trap concentrations, poly grains size, as well as of gate oxide and UTB-SOI silicon layer thickness. Such fluctuations will broaden the device parameters distribution and will therefore need to be taken into account for any optimization or manufacturability study. In this regime, each single device will have to be represented by an entire distribution of devices with random doping concentration (producible, for example, via Monte Carlo methods) and preferably in 3D, which re-emphasize the need of fast 3D simulators. A suitable description of this distribution with accurate results for the tails is mandatory for assessments of key figures of merit like SRAM noise margin, etc.

*RF*—Development of bipolar specific models lags behind that of models aimed at conventional CMOS scaling despite being as much or possibly more necessary. Consequently, support of RF, analog and mixed-signal CMOS, BiCMOS, and bipolar circuit design requires enhancements, especially in the numerical treatment of small signal analysis (AC) and large signal behavior (transient). Efficient tools are needed to analyze device performance, to characterize non-quasistatic effects, to minimize the requirement for time- and cost intensive RF measurements and to provide predictive data in the downscaled regime. Device simulation integrated with RF circuit or mixed-mode simulation could ease optimization but will require efficient algorithms. When coupling circuit and device simulations, calculations for different devices will need to be run in parallel, thus requiring the necessary hardware and software support. The employed models will have to take into account all models needed for DC, like surface-quantization, direct gate tunneling, stress effects etc. Comprehensive internal noise modeling must cover all the important internal noise sources from the sub-KHz up to at least the 100-GHz regime. Efficient models for substrate noise coupling have to be provided to couple comprehensive descriptions of external noise sources to the transport equations in a flexible way. Finally, self-heating of devices and circuits and frequency dependency of physical parameters must be taken into account.

*CMOS scaling*—Novel device architectures and ultimate CMOS scaling require more rigorous modeling. Channel lengths or silicon films of a few nanometers cannot be accurately represented without partially ballistic transport models, which also include quantum effects. Several approaches have been suggested so far, but they lack rigorous justifications in their approximations and are prohibitively computational intensive. Simpler schemes are based on self-consistent Poisson-Schrödinger equations, whereas more advanced methods exploit Green's or Wigner's functions to solve the Wigner transport equation, the Kadanoff-Baym equation, or the many-particle quantum Liouville equation. Of special importance is a consistent mobility model for the modified local density approximation (MLDA) and the density gradient model. With transport, i.e., stress and channel orientation, engineered devices becoming mainstream and the introduction of novel gate stacks these topics are of central importance. See the corresponding paragraph above.

*Novel devices*—In recent years, a large variety of CMOS compatible new device architectures has been proposed. A promising method to suppress the short-channel effect exploits thin films. Therefore fully depleted, ultra-thin body SOI, multiple-gate FETs, and various forms of double-gate or all-around gate structures have been investigated. For these structures the partially ballistic and quantum transport models discussed above are as indispensable as comprehensive mobility models for arbitrary channel directions. Additional device features being explored include non-planar or elevated S/D structures, transport engineered devices with strained Si, SiGe, or Ge, or even hybrid substrates, for which a correct and comprehensive description of stress and strain effects becomes an essential requirement. The same applies to novel gate stacks. Again, we refer to the corresponding paragraphs. Self heating will be important especially for devices fabricated on SOI wafers. Emerging memory technologies employ magnetic, paramagnetic, and ferroelectrics materials, therefore they require the modeling of spin, magnetic interaction and electrical polarization phenomena. Phase change memories require the modeling of transport in amorphous materials and phase transitions (crystal nucleation and growth).

*Miscellaneous*—Good progress was made in the last decade for the modeling of substrate current and hot carrier injection effects. Applications of microscopic simulators have allowed a detailed understanding of the generation and dynamics of hot carriers. However, because of their thin dielectric layers, scaled devices require further development, especially concerning trapping and de-trapping mechanisms or transport in dielectrics. Furthermore, models of charge trapping, de-trapping and transport in dielectrics for Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) like non-volatile memories still need significant improvements. Highly demanded degradation and reliability analysis relies on similar models taking into account a structural modification during device operations due e.g., to hydrogen or metallic ions migration, trap states creation/transformation, or stress induced voiding. Prediction of reliability under steady state and transient conditions or ESD has become an important aspect of the technology scaling analysis. Unfortunately, only post-processing or empiric models are available. For low power devices, the junction leakage current due primarily to band-to-band and trap-assisted generation seriously limits the process window. Therefore, existing models as well as their parameters will need to be revisited. To address design for manufacturability issues representation of devices variability (doping, gate line width etc.) has to be developed and interfaced to circuit design. Simulation for large area devices also needs to be explored. Power amplifiers or optical devices are usually built from many transistor cells connected together through a huge interconnect system. The impact of distribution effects on device parameters is not well understood and modeled, especially when thermal and electromagnetic effects are at play. Large signal behavior would be required but traditional TCAD is prohibitive because of the number of grid points necessary to discretize the whole system.

## INTERCONNECTS AND INTEGRATED PASSIVES MODELING

Interconnects play an increasingly important role as a limiting factor for staying in pace with Moore's law to double the maximum clock frequency every 1.5 years. This refers both to their electrical performance and to their reliability, and in turn requires coupled electrical, mechanical, and thermal simulation. Concerning reliability, electromigration, stress voiding and extrusion are most important aspects. Both electrical performance and reliability are critically influenced by process conditions, material properties including the microstructure of copper and (porous) low-κ materials. Performance and reliability critically depend on design, but with further shrinking distances and cross sections the deviations from ideal structures resulting from real fabrication processes is another important factor. Similar to front-end technology, both the modeling of the fabrication and then the modeling of the performance and reliability of interconnects is required. Whereas other subchapters deal with the first aspect, the latter one is addressed in this section.

As the operation speed of devices is increasing to the multiple GHz range and the complexity of interconnect systems continuously increases, software tools with higher accuracy and better efficiency become necessary. The ability to predict the electrical and parasitic properties of complex interconnect structures continues to be a challenge. Software tools and methodologies that link process results to results at the IC level, that identify reliability issues or design deficiencies, that give the designer capabilities to explore alternative interconnects easily are needed.

Potential solutions exist, but all these solutions need further development for being suitable to a day-by-day use in the design flow. The potential for the advanced modeling of the electrical performance falls in two categories:

- First, if the semiconductor substrate is low Ohmic, then the electromagnetic response can be captured in linear dependencies. In that case the substrate can be treated as a low conductive medium that is characterized by its conductivity and permittivity. Numerous modeling approaches are available that are based on a full wave approach. The method-of-moments (MoM) and the partial-element-equivalent-circuit (PEEC) method are pursued as a valuable scheme to simulate the electromagnetic environment. The finite-difference-time-domain method is also pursued for characterized interconnects and integrated passives in the high-frequency regime.
- The second category deals with the situation that the substrate is fully taken into account as a semiconductor, thereby responding in a non-linear manner to electromagnetic fields. Moreover, a second non-linearity is induced by the fact that the field-source dependency needs to be addressed self-consistently. Some attempts have been presented that considers the self-consistent coupling of the Maxwell equations to the semiconductor device equations. The feasibility of the solution is demonstrated, however in order to convert this solution into a practical tool, a series of developments are still required. Questions that need to be addressed are: "How can one extract, preferably in a (semi-) automatic way, the equivalent circuit representation, that is, the net list and the SPICE parameters or S parameters from the full wave solution?" Reduced-order modeling techniques have high potential and deserve to be further developed and explored.

All full wave solutions suffer from a severe computational burden. A typical simulation of the electromagnetic behavior requires an about ten-fold larger set of node variables to be solved as compared to a steady-state simulation. Due to the dynamic character, the vector potential for the magnetic field must be included. In order to deal with the frequency dependence both the phases and amplitudes of the variables need to be stored. Therefore, fast linear solvers play a key-role in implementing full wave solutions in the design flow.

Besides the demand to understand in sufficient detail these high-frequency effects, an increasing need is to simulate integrated passive elements. In order to characterize these passive elements it is needed to simulate these components in realistic circumstances. This aspect is a generic trend in future IC design: the electromagnetic properties of the passive components and the presence of semiconductor layers that respond in a highly non-linear way to the electromagnetic stimulus pose high demands on the simulation capabilities.

Of high priority are the coupled thermal and mechanical performance properties of thin multi-layer films. Structural and compositional properties of thin films need to be obtained and related to reliability effects not only for thin multi-layer films but also for thin multi-layer films patterned for critical dimensions. The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling can trigger fractures that may not be foreseen. Simulation tools are needed to study these effects more effectively than by experiment alone. The interplay with equipment and feature scale simulation becomes an increasingly important factor for being successful. The change to low-κ dielectrics with low thermal conductivity has placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development.

Modeling can definitely address these concerns, particularly thanks to the increasing capabilities of numerical tools. However, new physical phenomena might be expected and included in simulations:

- Delamination occurrences have drastically increased following low-κ integration. Brittle fractures, located at interfaces, cannot be address anymore with commonly used stress based analyses. Continuum mechanic laws do not remain valid and tools dedicated to fracture mechanics, such as energy based ones, must be developed. Despite the fact that several new failure indexes have been published, numbers of uncertainties and assumptions are still questionable. Furthermore, the actual state of the art does not allow to go from qualitative to quantitative simulation insights, which is required in the frame of interconnect architectures optimizations.
- As for the need to define worst cases of test structures and ensure that experimental reliability results indeed correspond to real life conditions of devices, the electromigration related issues must be simulated. As the size reduction leads to increase the influence of interfaces, hence both bulk and surface mechanisms must be considered and calibrated.

- Even in thermo-mechanical induced stress, critical dimension reduction also tends to invalidate the commonly used approaches in material models: For example, microstructural effects in copper lines, or pore effects in dielectrics will became a dominant factor. Multiscale and multi-physics simulation must be precisely carried out to bridge these scales.

Interconnect performance simulation is getting especially difficult because the problem widely spans in four respects, as follows:

1. An increased coupling of electrical and thermal-mechanical simulation is necessary.
2. The final target is performance and reliability at least at chip level. However, with shrinking dimensions and increasing aspect ratios this is more and more influenced by process details leading to deviations from ideal interconnect shapes, the problem spans from few Angstroms to several mm.
3. In the end details on feature level as well as the physical effects discussed above increasingly influence the performance of the actual design. In turn, the various levels of interconnect simulation need suitably to be coupled with design in a bi-directional manner.
4. Simultaneous simulation of interconnects and packaging becomes more important.

To solve these issues hierarchical simulation methodologies and tools must be developed.

## CIRCUITS ELEMENTS MODELING

An important task for circuit modeling is to achieve concurrent device/circuit development, dealing with the increasing amount and intensity of interactions between e.g., devices, layout, density, parasitics and so on.

Accurate modeling of circuit behavior, including parasitics, is crucial for first-time-right designs. Process and device simulations can support the extraction of early information for new technologies. Models that relate material properties to electron transport strongly enhance the predictability of these models for future technologies. The models should take into account statistics and variations of the processing, including statistical correlations for feasibility of manufacturability. Preferably, these (statistical) models should be available long before process qualification. This enables chip design before technology release, enabling a fast product ramp-up once the technology is qualified.

Circuit element models for circuit simulation are key to chip design productivity. Many challenges can be found in the Design chapter. Examples are the increase of clock frequency, the decrease of supply voltage, the increased importance of weak inversion, and the exponential increase of the circuit complexity. Model accuracy and CPU efficiency are two opposing requirements leading to a hierarchy of models. The most accurate models are used to simulate small circuits. Less accurate models are derived to simulate larger circuits, and so forth. Similarly, this dichotomy implies a hierarchy of models at several structural levels - device level, cell level, and block level, although it may also be possible to simulate a whole chip with accurate models without hierarchal simulations.

Historically analog simulation needs have driven the development of circuit element models. Both analog and digital designers then use these models. The increasing number of (analog and digital) devices per chip necessitates faster models and improved convergence in the simulation tools. Device models will include many more detailed effects. Parasitic effects, like series resistance, inductance and capacitance, as well as quantum effects, leakage, noise, distortion and non-quasi-static effects have become of more importance. Robust and accurate parameter extraction algorithms are becoming more essential for each model.

The trend is to go to physics based surface-potential-based modeling, which also provides a simple connection from the device simulation to the circuit simulation. This enables reduction of model parameters resulting in fast parameter extraction and easy inclusion of variability and statistics. This is important for digital circuits, for example, static noise margin in SRAM. However, it is still crucial for analog and RF applications where accurate description of derivatives is of prime importance. Such applications often operate in weak inversion, where threshold-based models rely on mathematical fitting. For some applications longer-channel devices are used at high frequencies, making non-quasi-static models essential. For analog and RF applications the modeling of noise and distortion will need more attention. A strong request is that RF (noise) measurements are avoidable and compact models can predict noise without extra parameter extraction.

Compact models for future CMOS generations should model new effects correctly. Examples are mobility-enhanced channels and high-κ gate leakage. Non-classical CMOS devices (see the PIDS chapter) will pose additional modeling challenges. Many devices have fully depleted channels, like FD SOI-CMOS, FinFET, dual gate FET, etc. This enables shorter channels, which means more ballistic effects. Moreover, two channels close to each other (10 nm) will have quantum mechanical interactions. This is important in multi-channel devices like FinFET and dual gate FET. Given the small dimensions, variability and statistics will be more prominent is this class of devices. Local variations will become more important than global variations for these generations. This will affect the way statistics and e.g., static statistical timing analysis are treated in circuit simulations. A consistent treatment of local and global variations is required to allow for a computer-efficient inclusion of statistics in circuit simulations, preferably before process freeze.

For non-CMOS devices it is hard to specify the detailed modeling challenges. The number of options in the PIDS chapter is still very large, requiring huge efforts in the modeling domain. For bipolar devices, models will be extended towards extreme HBTs, either in SiGe(C) or in III-V materials. For memories models are needed for new memory concepts like FRAM, MRAM, and phase-change, as mentioned in the PIDS chapter.

The circuit modeling of RF will extend to the 100 GHz range. Either extreme RF applications (77 GHz car radar, 60 GHz WLAN) or 30–40 GHz applications where (third harmonic) distortion is important. Models for scalable active and passive devices, such as inductors, transmission lines, varicaps and interconnects, including their parasitic elements, are crucial for good RF circuit modeling. For several larger (active or passive) elements the non-quasi-static effects will be significant and should be modeled accurately. To support heterogeneous integration, CAD-tools must be enhanced to better handle simulations with different technologies and in different simulation and application domains (RF, digital and mixed signal). They will need to handle multiple interactions between circuit models, building block models, interconnect, dies and packages.

The importance of interconnect modeling increases with the stronger contribution to circuit delays and cross talk. The complexity and the size of the interconnect network poses serious challenges. Different applications need models for different effects, like cross talk, matching, inductive coupling (also in 3D), skin effects, and size effects (see the Interconnect chapter). A hierarchical interconnect simulation approach is necessary to keep simulation times reasonable. The consideration of the inductances is important for fast-clocked circuits. For RF applications it is an essential part of the circuit behavior. Full wave description of interconnect devices, like transmission lines and antennas, will be common for high speed or high frequencies. If the full-wave description of interconnect gets important beyond the device level, serious efforts are needed on complexity reduction algorithms.

Increased integration density causes non-negligible interactions between neighboring devices. This must be modeled on the basis of the layout of a circuit. Three-dimensional parasitic effects such as fringing effects may also strongly influence RF circuit performances. In large circuits even long-range effects will gain an importance. Examples are the substrate-coupling effects, e.g., a digital clock signal that propagates to the analog and RF parts and disturb their specifications. Temperature effects will get more important for SOI-based and thin-film devices. Hence, self-heating and mutual heating and cooling effects should be modeled in more detail over the full chip. For RF applications, large-scale electromagnetic field effects will gain in importance. This should be taken into account beyond the device level on the circuit level. An efficient simulation methodology is key for this task.

Predictive reliability simulation will be more important as more designs will be close to the hard reliability limits. ESD is becoming one of the most serious reliability problems in future processes. Predictive circuit-level simulation, based on device level compact models, is essential to guarantee ESD-safe chip-design. In addition, the prediction of electromigration from interconnect layout needs improvements to avoid super-worst-case margins. Simulation of oxide reliability, hot-carrier effects, and EMC compatibility might pose constraints in some cases. Predictive models require good solutions for measuring the material physics properly.

## PACKAGE SIMULATION

IC-package co-design is a key crosscut issue with system-level considerations becoming increasingly important. In the past a package designer might have been presented with the die footprint including the placement of the die I/O pads as well as the placement of the I/O connections to the printed circuit board (PCB). With increasing pin counts and overall size constraints, this practice often results in packages that are unreasonably expensive or that cannot be manufactured. Beyond being routable and manufacturable, a package must meet demanding requirements with respect to signal integrity, power, temperature, and mechanical integrity. The required electrical, thermal, and mechanical simulations must be performed with consideration of the die and the system, and this is possible only with communication enabled by co-design tools. A properly designed co-design tool will interact directly with both the package and die databases and have the capability of communicating results between the two.

The more common package models today are lumped discrete models such as IBIS, SPEF, or SPICE. There will continue to be demand for such models due to their simplicity and speed of simulation. In the near term these simple models need to be improved to describe the package better. SPEF models are appropriate for the IC when the self-inductance of small short connections is important, but the absence of large current loops renders mutual inductance negligible. In a package with relatively long traces, large current loops, and bond wires, mutual inductance can be extremely important, and it is becoming more important in the IC. IBIS models describe the cross-coupling well, but all die pins on a given package net are generally shorted together, significantly limiting the possibilities for simulation. Neither of these formats properly addresses power and ground issues. With SPICE one can build more complex models of the ground and power structures, but the models tend to be cumbersome and slow.

Modeling of power and ground structures in the package is extremely important. Current bottlenecks, noise, and simultaneous switching issues are critically important with repercussions for thermal analysis. It is difficult to ascertain if enough decoupling capacitors have been placed in the correct places to guarantee performance, or perhaps too many have been added, thereby negatively impacting cost and package size.

There is a clear need to move beyond models based upon discrete elements to distributed and transmission line models. In simple packages there may be very limited power and ground structures, while in a typical ball grid array (BGA) package only half of a given trace may cross a ground plane. In a more complex flip-chip design there may be many ground and power planes on alternating layers. Especially with increasing initiatives for package re-use, models for these packages may be generated once, and then passed to many consumers. Hence, there is a need to form a consensus on packaging model formats that are generally useful and easily shared. Alternative modeling schemes such as reduced-order models should be investigated. To allow for the increasing complexity and interactions of the IC-package-PCB system, a modular approach that allows for different implementations of different component models may likely be required, especially when considering system-in-package or system-on-chip solutions. It may be necessary to simultaneously consider digital, analog, RF, and even micro-electro-mechanical systems (MEMS) and optical components. Refer to the Assembly and Packaging chapter.

Generating models for simulation is creating new challenges with regard to numerical methods. Package geometries are such that there is no substitute for fully three-dimensional field-solver extraction. In a flip-chip package there are sometimes so many layers and power and ground structures that the extraction of a single signal net may be very costly. In a multi-chip module (MCM) there may be longer traces that couple many nets together, requiring a very large minimal set for extraction. In either case, decomposing the problem into smaller pieces introduces significant fictitious fringing spoiling the power/ground extraction. The development of scalable field-solver engines that can manage full-package extraction is essential; scalability will likely be achieved through implementation on a parallel cluster. At the same time efficiencies with regard to time and memory consumption need to be further improved.

The introduction of low-κ dielectrics with low thermal conductivity increases the need for thermal analysis. ICs generating increasing amounts of heat will transfer more of that heat to packages that will be challenged to dissipate it, and in turn the package will transfer heat to the system. This attribute also requires co-design tools that facilitate simultaneous analysis. Furthermore, current flow through ground and power structures must be understood because current bottlenecks can lead to hot spots.

Inherent and thermally induced mechanical stresses throughout the layer stack must be identified and modeled. The low-κ dielectrics often have reduced mechanical integrity, while at the same time thermal stresses are more severe. The stresses are especially enhanced with non-uniform heating induced by the die, by current bottlenecks in the ground and power planes, and with reduced thermal conductivity.

In addition to specific failure mechanisms and front end back interactions induced by new material integrations, the increasing complexity of packaging options confirms the need to reduce test vehicles thanks to modeling. Since process windows and main influent parameters are definitely dependent on the packaging options, generic modeling cannot be applied anymore and actual product configurations must be considered. Furthermore, the whole process flow, including front end, assembly and packaging steps, must be simulated to examine precise residual stresses, critical loading conditions, and thus optimize both package and interconnect features. This would finally lower the cycle time to introduce new products while ensuring device integrity. In order to allow such requirements, dedicated modeling procedures must be carried out at the several simulation levels involved. This includes multi-scale methods, consideration of dynamics and multi-physics phenomena that particularly occur during assembly processes, and non-linearity of the material behaviors. As a consequence, thanks to the development of the whole modeling flow and helped with a limited amount of experimental validations, a major role would be played by thermal and mechanical simulations. Finally, since interactions from front end to packaging features are increasingly closer, a co-design in between the related teams is definitely required.

## MATERIALS MODELING

The determination of the physical properties of thin film and bulk materials and the impact of these properties on the electrical, mechanical, and thermal properties of devices and integrated circuits is becoming more significant across all aspects of semiconductor technology as new materials are being explored. The strong driving forces behind this are the physical limits of material systems used to date.

Many alternate materials are being suggested as possible solutions for some of the critical semiconductor roadmap roadblocks. Materials simulation tools that give insight to inter-relationships between the physical properties of multi-layer thin films and the electrical, thermal, and reliability aspects of the device or integrated circuit would allow the selection of options without the need for many and complex experimental characterizations.

Both empirical and fundamental materials modeling and simulation are needed to aid in this understanding. Whereas at short time scales, for example, for the near-term challenge "Ultimate nanoscale CMOS simulation capability," insufficient availability of fundamental materials modeling capability will frequently require the use of phenomenological models, in the long-term first principle simulations will be indispensable. A special emphasis needs to be placed on the development of the material properties in this mesomaterial (between bulk and atomistic) range.

Modeling and simulation tools in the equipment, process, device, package, patterning, and interconnect topical areas are only as good as the input materials parameters. In many cases, these parameters are not known or only weakly approximated. Databases are needed that contain both experimental and, where not available, material parameters calculated from first principles. In general, to efficiently create and maintain such databases, problems regarding the materials modeling tools to be addressed include the following:

- To calculate an increasingly large number of model parameters required in the databases demands an increasingly large computational and organizational effort. Therefore, the calculation process must be automated to a large degree, enabling an efficient workflow and a rapid reaction to changing technological requirements.
- In many areas of materials modeling, a key problem is the approximate solution of Schrödinger's equation that leads to discrepancies between first-principle simulations and experiment, possibly requiring readjustment and validation of the approximations. A second key problem is then to extract the desired physical parameters, using as few evaluations of the approximate solutions as possible. Often, both problems are solved within one monolithic simulation tool. A modularization of the simulations tools with respect to these two key problems would enable a faster and independent development and improvement of solution approaches for the two problems.
- With device active regions continuing to shrink to several tens of nanometers for the physical channel length and to the nanometer range for the effective oxide thickness of high-κ gate dielectric materials, materials simulation and modeling tools that go from atomistic descriptions to continuum results will become more and critical. In the long term, the relevant materials modeling approaches might be integrated into the modeling toolsets of the various topical areas. The materials modeling tools must be prepared for this integration.

Specific materials modeling problems to be addressed for the different topical areas include the following:

- Materials models are needed for improved (especially chemically amplified) resists, for advanced mask making and for multilayer mirrors to be used in EUV lithography. The impact of molecule sizes on the resist structure must be incorporated in the determination of line edge and line width roughness.
- Interconnect performance and reliability will be strongly affected by the microstructure and the resultant change in conductance of copper, which must be taken into account in the simulation. Another issue for materials modeling is low-κ dielectrics.
- For processing, needs include codes with pre-determined adjustable model parameters for ion implantation, dopant diffusion and activation and interdiffusion in thin films. A wide variety of dopants and co-dopants must be considered.
- Most models used in device simulation can be considered as material models, because they are based, for example, on the electronic structure of the semiconductor, for example dielectric properties, and channel transport properties, including quasi-ballistic transport. Here also, major progress is needed due to shrinking dimensions, higher local

electrical fields and especially due to the use of global and local strained channels including, for example, strained substrates (sSi), SiGe, Ge, III-V, SOI, sSOI, GeOI and other new materials. See the Device Modeling section.

## TCAD FOR DESIGN, MANUFACTURING AND YIELD

With devices shrinking into the deca-nanometer range, the variability of process results due to fluctuations of fabrication parameters or statistical variations of a small number of dopant atoms gets increasingly important. As mentioned in several of the focal ITRS chapters and their cross-cut texts, this variability increasingly challenges further device scaling and the overall progress of the roadmap. For dopant distributions in the transistor channel fluctuations scale with the square root of the number of ions *n*, causing the relative error to scale inversely proportional to the root of *n*, and therefore to increase with decreasing *n*. A similar effect holds for geometries where it is generally very difficult to reduce absolute variations in the same way as the nominal values such as of gate CD. In turn, the variation in percent of the nominal value increases.

As pointed out in the cross-cut texts between Modeling and Simulation and the technologies of Design, PIDS, FEP, Lithography, Interconnects, Factory Integration, Yield Enhancement, and Metrology, TCAD must contribute to the assessment and minimization of the impact of such process variations and dopant fluctuations on the performance and reliability of devices, ICs, and systems. The key advantage of TCAD is that well-defined variations can be very easily introduced into a simulation run on a computer, and subsequently their impact on performance and reliability figures can be calculated. Integrated process/device/circuit simulation employing sufficiently predictive physical models could then be used to calculate the spread of relevant results such as physical channel length, CDs, threshold voltages, off- and drive currents, signal delay, etc. Compared with this the experimental study of the impact of such variations is at least very difficult and expensive, if not impossible. This is due to the inherent difficulties to produce experimentally and to characterize reliably a well-defined nanometer scale variation of a patterning process and the resulting geometry, or the number of dopant atoms in the channel region, and their precise locations.

There are large areas of application and potential merits of TCAD for Design, Manufacturing, and Yield (TCAD for DMY):

- Assessment of layout dependent device performance by use of coupled process and device simulation which for example enables the study of layout-dependent stress effects, proximity effects in lithography, or large-scale CMP effects.
- Sensitivity analysis of device performance changes caused by process variations: This would enable the identification of the maximum variations of certain process parameters that are still acceptable to keep the variations of the device performance within specifications. Compared with the state-of-the-art of the available technology this allows judgement of whether the device variability specifications (for example, 3σ spread of $V_{th}$) can be achieved, which processes need to be improved, and which are already sufficient.
- Starting from a given technology and its variations TCAD could be used not only to assess the nominal performance of certain device architectures but also their spread. This enables a much better assessment of the device architectures because with further shrinking features and higher integration moderate improvements of nominal performance may be far less important than the selection of processes and architectures which cause less variations in the performance of the final device or IC.
- Complement standard SPICE models that currently bridge between process technology and design by information on the impact of process variations on design. This would enable a much more accurate assessment of the manufacturability of a design. For example, instead of global values and tolerances of design parameters such as gate length and $V_{th,}$ the requirements may be relaxed in some areas and tightened in others, allowing the manufacturing of ICs with better performance, smaller size or higher reliability without changing the technology used by just adapting the design to the local neighborhoods.
- Assessment of the impact on devices and ICs of the variations introduced by a certain piece of equipment. This assessment would complement traditional advanced process control (APC) methods to decide about feed-forward and feed-backward equipment control and about when equipment maintenance is needed to limit drift or variations of process parameters.
- Finally, completing the loop and calculating the spread of the final IC parameters due to the known variations and fluctuations of the technology. This approach enables the assessment of the impact of process variations on yield

and, by identifying those processes which are most critical for that yield, also the increase of the yield by appropriate changes of those processes or the design.

In summary, there are large prospects for “TCAD for Manufacturing,” “TCAD for Design,” and “TCAD for Yield.” However, the potential merits of the application of TCAD to study the impact of process variations and dopant fluctuations can only be gained if several challenges are met by TCAD:

- First, sufficiently general and predictive physical models must be available and be implemented in the TCAD tools used. The general requirements on these models are discussed in the other sections of this Modeling and Simulation chapter. However, two aspects are specific to TCAD for Manufacturing, Design, and Yield: Firstly, the primary objective is the study of the impact of the variations, not the prediction of the absolute performance figures. Therefore, calibration of the models prior to their use is acceptable. The basic requirement is, however, that the models correctly capture the trend, which means that the direction of the variations of the performance figures as well as their size must be predicted. Additionally, several kinds of variations can still not be studied with models available within commercial process simulation tools, like line edge roughness and line width roughness introduced in a patterning step.
- Second, for TCAD for DMY, the level of integration between process, device and circuit simulation must be drastically improved: For example, the integration of physical 3D simulation of the patterning steps lithography, etching, deposition, and CMP with each other and with doping processes and 3D device simulation is not yet available in commercial simulation tools. Adaptive meshing for non-planar and especially time-dependent geometries is still a key limiting factor. For TCAD for DMY this integration challenge is drastically increased because all kinds of numerical errors—resulting from discretizations in space and time and from the change between different meshes used in different simulation modules, for example—must be controlled to make sure that the final calculated device or IC variations are not significantly falsified by numerical noise.
- Finally, the most difficult challenge for TCAD for DMY is the need to bridge between microscopic process and device simulation on the nanometer scale and the design of an IC with millions to billions of components on some ten square millimeters. 3D process simulation requires at least some ten thousand meshpoints to describe a device. Extending this to chip level would require in the order of magnitude of $10^{14}$ mesh points, which will be impractical for use in simulation also in the long term. In consequence, suitable strategies and algorithms must be developed for hierarchical simulation: Nanoscale process and device simulation is only carried out for small critical areas. Then appropriate data on the level of SPICE parameters including their variations are extracted, and communicated to design. This link has to be bi-directional because critical areas have to be identified based on the design data and layout.

## NUMERICAL METHODS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena to be addressed by extended TCAD. For example, more accurate solutions of the Boltzmann transport equation in device simulation are required. To include stress and strain and several defect species and complexes in the simulation of dopant diffusion and activation requires dealing with an increasing number of coupled partial differential equations over the device grid. Moreover, physical processes with different intrinsic time- and/or length scales critically influence each other, and have to be simulated adequately in a coupled manner—point-defect diffusion occurs on a several orders of magnitude faster time scale than macroscopic process time. The gas flow, depletion, and reaction in a deposition furnace on a macroscopic scale are the basis for the chemical vapor deposition in a contact hole, there also critically affected by the local geometry on a deep sub-micrometer scale. More recently, an increasing demand has been put on the simulation of electromagnetic effects such as the skin effect in conductors, the proximity effect and the substrate coupling. These are examples of how increased requirements on predictability and accuracy of models induce more complex models and, in turn, drive the discretization methods and linear solver technology.

Increasing numbers of independent variables or accuracy requirements lead in many domains of modeling to the transition to a completely different level of approach, such as Monte-Carlo instead of analytical simulation of ion implantation; atomistic modeling instead of continuum diffusion equations; and rigorous solutions of Maxwell equations instead of the traditional thin mask approximation to enable the simulation of advanced masks (phase shifting masks, optical proximity correction) in optical lithography. These advanced approaches frequently require the development of new problem-specific and efficient algorithms, as the application of standard algorithms would result in prohibitive time and memory requirements. Not only the linear solvers as stand-alone libraries demand continuous improvement, but also research is required on how the set of discretized equations are scheduled and organized before submission to the linear solvers is done. In consequence, the state-of-the-art of the numerical methods and algorithms available or being developed mainly in other domains of science must be permanently checked from the point of view of the application requirements of all domains of simulation, described in this roadmap, and be used to influence and kick-off developments required.

Meshing, although always important for the efficient and accurate solution of differential equations, has become a major issue because device architectures are now essentially three-dimensional. The increase of the numbers of steps to be included in process simulation, and especially the frequent use of automated simulation splits to investigate process options and the sensitivity of electrical device data on process details requires completely automated grid generation. This automated grid generation must be reliable for all kinds of device geometries and distributions of volume variables, with a failure rate at least two orders of magnitude below current tools. In addition, meshing tools must be capable of resolving all critical features of the device or equipment, like small geometry features or steep dopant gradients, without unacceptable drawbacks in terms of mesh nodes, computation time needed for mesh generation, or adaptation in the refinement as well as the coarsening direction.

Mesh generation time is especially critical in case of simulation splits or simulation runs with a large number of process steps. Considerable problems are caused especially in three-dimensional simulations by moving gradients of volume variables and even more by moving geometries: These require parallel mesh refinement and unrefinement or the use of moving mesh nodes, in most cases with additional requirements on the shape or quality of the mesh elements to be met to enable an appropriate solution of the physical model equations to be solved.

Meshing algorithms must guarantee that discretization errors caused by the removal or by the movement of mesh nodes do not negatively affect the simulation results: Especially for applications in sensitivity analysis it must be guaranteed that changes of the results are due to physical reasons and not critically affected by changes of the meshes used in the different simulations.

A promising solution to this problem is that a new mesh should use as many nodes and elements of the preceding mesh as possible and appropriate, such as during the simulation of oxidation. Stable and efficient algorithms are needed to trace the change of device geometries especially in the three-dimensional simulation of process steps like etching where multiple layers have to be considered. Such algorithms must reliably avoid artifacts in device topology and allow for appropriate volume meshing. Currently, none of the several approaches used (triangulated surfaces, cells, level set; delooping) has demonstrated to solve all relevant application problems.

These meshing requirements outlined above are further extended by the growing demand for equipment and material simulation. While in this case the problem of moving geometries hardly exists, adaptation to time-dependent volume variables is still critical. A major concern is to combine the very different scale in the simulation problem: the on-chip features are on the nanometer to micron scale whereas the equipment scale is in the centimeter range. Automatic mesh generation and adaptation is especially important to resolve critical features of equipment geometry and the wafers to be processed, while avoiding a too high number of mesh nodes. This problem gets severe when coupling equipment and feature scale simulation. Several current tools for computational fluid dynamics (CFD) calculations suffer from a complicated procedure to define the geometry to be simulated and to provide necessary information for mesh generation.

Particle-based Monte-Carlo codes need an increase in raw CPU speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more GFLOPS will at least be partly met by improving hardware, provided current trends continue. Parallel solution strategies are also needed in order to address computationally intensive 3D simulation needs and simulation of large circuits. This especially includes the use of distributed systems (e.g., workstation clusters or PC farms). These systems are currently standard in industry. However, it has to be critically investigated which kind of simulations will only be possible with large shared-memory computers, and whether and how sufficiently powerful systems will be accessible to industry and research.

Linear solvers are often the bottleneck in the computation. Many millions of algebraic equations need to be solved simultaneously by a two-fold iterative scheme. For example, the unification of the drift-diffusion model and the Maxwell equations demands that ~10 variables are solved for each grid node. The outer loop that is needed to address the non-linear coupling can be substantially speeded up by intelligent forward guessing strategies. Further improving of these methods will drastically reduce the number of iterations. The inner loop that is required for obtaining the updates can be improved considerably by re-ordering strategies, optimal preconditioning, and partitioning of the equation set. Speeding up direct solution of the linear system is very helpful when iterative methods face convergence problems. This latter applies especially for circuit simulation, in the time domain as well as in the frequency domain. All the mentioned methods need to be exploited and optimized for TCAD applications.

A serious complication results from recent trends in microprocessors. Performance gains in the past were mostly achieved by increases in processor clock rates and memory bandwidth. This allowed conventional numerical algorithms to port easily to each successive generation of hardware. In many cases higher performance hardware was binary compatible with earlier generations and not even a recompilation was needed. This is likely to change with the transition to multi-core processors. Current performance improvements are achieved by increased numbers of processor cores on a single die, while core clock rates are no longer increasing. This means that most TCAD applications will no longer automatically benefit from hardware improvements. Instead, significant work must be spent on algorithm architectures and implementation to make solvers execute efficiently on multi-core processors. In addition special purpose floating point processors based on graphical processing units could speed up numerical calculation a lot which is currently demonstrated in many physical applications.

Research is also needed on arriving at robust solution techniques: Effectively this means that in general an optimization sequence avoids local minima where the flow gets trapped. Techniques need to be developed for how to escape from these traps without fully destroying the result achieved so far. These strategies should then be implemented in the software tools in order to facilitate their respective ease of use.

Research is also needed on developing robust and efficient parameter extraction algorithm. Without a well-calibrated parameter set, simulators lose their practical values. However, calibration work is frequently a time consuming and delicate issue, due to a large number of parameters and the so-called "local minimum problem." Some algorithms, such as genetic algorithm (GA), may be good candidates to solve this problem, but only if remarkable improvements in its efficiency are realized. Furthermore, it is not always guaranteed to obtain a set of complete measurements for calibration. A sophisticated scheme for interpolation from randomly measured results is also needed.

A continuous challenge is inverse modeling, which has a potential capability of providing us with information of parameters that are difficult to measure such as two-dimensional dopant distribution, the dominant chemical-reaction-path, etc. From the mathematical point of view inverse modeling is a delicate issue because a limited set of data has to be correlated to a large collection of configurations that could reproduce the restricted data set, in other words the problem is underdetermined. This means that in many cases, no satisfactory solution can be obtained, or in other cases, the obtained solution represents one example of millions of configurations. However, it has the potential of opening a new way of application for modeling and simulation. Preferring one configuration over another one should be guided by objective criteria. The latter may be found by entropy principles or information theoretical considerations.

A breakthrough for efficiently calculating stochastic variations in models is needed to meet the strong requirements of evaluating and/or simulating deviations of device performances due to uncontrollable fluctuation under device fabrication. Traditional computing approaches such as the Monte-Carlo method require a prohibitively large number of trials, as the number of fluctuating variables increases. It will be necessary to introduce new algorithms for this purpose, such as numerical methods to solve stochastic partial-differential-equations.

# POTENTIAL SOLUTIONS

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. This document presents specific needs to increase this effectiveness and to provide impact on our industry in the future. Whereas the discussion on the requirements given above implicitly included the potential technical solutions to meet them, some general actions are needed to enable Modeling and Simulation to fulfill these needs and in this way to provide the forecasted benefits to the semiconductor industry:

- Increase cross-discipline efforts will be vital in order to leverage on the expertise of fields that were originally not related and are now needed to work together to cope with the challenges outlined in this document.
- Adequate resources for research must be mobilized and directed to efficiently work towards the technical solutions for the challenges and requirements defined. In addition to the definition of the top-level requirements in the ITRS, interactions between industry and research institutes both at universities and at independent laboratories must continue to be enhanced and extended to guide the activities towards the industrial requirements detailed in this roadmap. Especially, this interaction must also include the promotion and enabling of mid- to long-term research actions needed in Modeling and Simulation, which is generally pre-competitive and therefore an excellent field for broad cooperation. Nevertheless, near-term needs and financial boundary conditions in industry have so far frequently led to strong reductions of such activities, with the consequence of endangering the mid- to long-term success of the roadmap. This became also apparent during the preparation of the 2007 ITRS where it was found that several requirements stated in the 2005 ITRS have so far not been met due to missing support for the necessary R&D work.
- Software houses, research institutes and universities must be strongly encouraged to standardize and/or open up some of their universally used modeling and simulation modules to avoid multiple work in the pre-competitive area. In the ideal case there should be supplier-independent standard interfaces that allow for the combination of tools from different sources, or at least standardized model-interfaces that allow R&D institutes to focus on the development of added-value features, like new models, while being compatible with supported software environments from the beginning and in this way reduce time-to-application. Existing proprietary model interfaces of some commercial tools have already proven to strongly promote cooperation with research institutes and universities and, in turn, strongly accelerated model development and its use in industry. Standardization of interfaces would largely enhance that benefit. The semiconductor industry can have a central role in this respect by requesting such standardization when deciding about their software investments.
- With equipment suppliers playing an ever larger role in process development, the target should be that not only a basic process is sold with the equipment but also an appropriate simulation tool (or at least a model with well-established parameters) to describe this equipment and process. For a well-characterized and stabilized process sufficient data should be available to enable the development of these features with high added value. Cooperation of equipment suppliers with university and independent research institutes is vital for this process. Compatibility with overall simulation environments generally offered by software houses should be achieved via the standardized or open interfaces mentioned above, or via direct cooperation with relevant software vendors. In order not to limit the semiconductor industries' choice of equipment and software either the standardized interfaces or non-exclusive cooperation would be preferred. Related IPR problems need to be solved well in time.
- To further optimize the industrial benefit from simulation, the methodologies for evaluating the impact of Modeling and Simulation must be improved. The target should be to identify more in detail in which way simulation can most efficiently support the industrial development ("value for money"), but also to get a more clear view of the overall cost benefit as already estimated in Table MS3. Making the cost benefit from Modeling and Simulation more transparent should also help to get sufficient resources for the required R&D work without which the cost benefit cannot be achieved.

The most important general technical development needed in the field of Modeling and Simulation is that of integration—not only between equipment and process, between different processes, process to device, device to circuit, layout and design, but also between different levels of description. In some cases the Modeling and Simulation software tools are linked together (such as traditional TCAD process and device simulators, design tools), while in many other areas the software tools are still separated. If one examines the cycle time for development of a new technology, much of that time and cost is not in the individual module development, but at the integration level. There is a continued strong need for Modeling and Simulation tools to be better linked for determining unforeseen interactions of one step on the next. This type of effort is needed for the following:

- The interfacing or integration of individual equipment/feature scale simulation tools. An example is the linking of a lithography simulation tool that predicts exposure characteristics in photoresist with a plasma-etching tool that predicts etch profiles for process latitude and sensitivities.
- The interfacing of materials structural simulation tools with software that predicts electronic properties. An example where these tools would be useful is in the development of high-κ dielectric thin films. Future software tools in this area then might treat the gate stack as a system rather than as individual components. Unforeseen materials interaction issues, better "what-if" analyses, and reliability effects could be studied.
- The integration of chip performance tools with package thermal, mechanical, and electrical simulation tools to create a co-design environment.
- Structured data sets that contain needed physical constants that facilitate parameter passing between tools.
- The integration of device simulators with robust methods for creating compact models and device files for design.
- Generally, a hierarchy of closely coupled simulation tools must be developed - from spreadsheet to *ab initio*. This would allow the industry to select the most appropriate level of description for their simulation problem in question, along with appropriate and efficient data transfer when the application requires investigations at different levels (for example, for influence of process variations on design). The growing need of such an approach is underlined by the subchapter on TCAD for Design, Manufacturing and Yield in this Modeling and Simulation chapter newly introduced in the 2005 ITRS, and by the 2005 long-term challenge "prediction of dispersion of circuit parameters" being pulled in to short-term and distributed there across several short-term challenges.

# CAPABILITIES AND ACCURACY/SPEED REQUIREMENTS

Modeling and simulation encompasses a variety of applications with widely varying requirements. For example, in applications closely associated with design, speed and accuracy of phenomenological models are the primary requirements, while predictability in uncalibrated regimes is secondary. Examples are circuit modeling and the lithography models built into OPC systems. In applications associated with technology development, the requirement may be considered a mixture of physically based models and calibrated/parameterized empirical models. Traditional TCAD applications, when used to optimize technology development (using highly calibrated simulators), fit this description. Finally, there are modeling areas in which the basic physics are being explored. Examples are Monte Carlo device simulators, or first principles calculations of diffusion parameters for dopant diffusion in silicon. To give useful guidance for all these application areas, the technology requirements tables for Modeling and Simulation have been divided into tables for simulation "Capabilities" and tables for "Accuracy and Speed." Refer to Table MS2a and b, and Table MS3, respectively. It should be stated, however, that there is an overall trend to require more predictive physical models that need less calibration. Moreover, integration between different process steps (which influence each other) and between feature- and equipment scale becomes more important and close, and makes it increasingly difficult to specify single items without taking others into consideration simultaneously.

The "Capabilities" requirements table (Table MS2a and b) is meant to describe the technology requirements for Modeling and Simulation that demand new features of modeling to be developed, or describe where existing models and tools are still largely unsatisfactory. An example would be the capability to model chemically amplified photoresists. In this case, the basic ability to simulate predictively the performance of such a nonlinear resist needs to be developed. This type of requirement is often tied either to the introduction of new technologies or to new regimes of physical phenomena at smaller dimension.

In contrast, the "Accuracy and Speed" requirements table (Table MS3) describes the level of simulator accuracy needed for process/circuit design or optimization. For TCAD applications, this level of accuracy is needed to achieve the overall TCAD cost reduction goals listed in the first row of the table. The cost reduction goal should be interpreted more generally as a cost and development time reduction, as it is understood that TCAD should speed up the process development schedule. For ECAD and design applications, these are the accuracy levels needed for designers to create new products effectively. Note that accuracy requirements are specified only for the near-term technology requirements; for the long term, investigation of new technologies is the overall priority. It should be recognized that at a given point in time, several technology generations are being simulated in parallel, with differing accuracy requirements for each.

Note that the accuracy requirements in Table MS3 refer to accuracies obtained after calibration of the simulation tools to a particular technology generation. It is generally understood that for TCAD simulation tools in particular, calibration is required for each technology generation, because new technologies, materials, dopant species, and process regimes are introduced.

Cost saving figures given in Table MS3 are estimates for the cost saving by use of extended TCAD during the development of new processes, devices, and ICs. They are based on a questionnaire-based survey held in Japan in 2002, which gave estimates of 26% reduction in time during development, 30% in numbers of lots, and 34% in numbers of process options. These numbers are the averages across the most impressively successful cases, which were evaluated not by modeling engineers but by more than 70 integration/device-engineers and managers of about ten semiconductor companies in Japan. An update and extension of this study is in progress.

*Table MS2a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *23* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| *Lithography* | | | | | | | | | |
| Exposure | **Simulation of immersion lithography for high NA liquids (NA about 1.5) [1]** | | **Simulation of EUV including optical flare, optical lithography for very high NA (about 1.7), ML2, imprint lithography options; models bridging OPC and predictive feature scale simulation [2]** | | | **NGL models and modeling of materials and components (immersion, EUV, ML2 lithographic processes, imprint)** | | | |
| Resist models | **Predictive chemically amplified resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters** | **Multiple exposure; EUV resists; finite polymer-size effects; line collapsing; lithography on topography; coupling with etch models** | | | **Meso-scale resist models with finite molecule effects; resist flare** | | | **Non-conventional photoresist models and coupling with etch models** | |
| Large area lithography simulation* | **TCAD-based methods to detect weak spots in lithography and etching across whole exposure field** * | | | **TCAD-based inverse lithography modeling** | | | | | |
| *Front End Process Modeling* | | | | | | | | | |
| Gate stack* | **◆ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [3]** | | **Model material properties and electrical behavior of prioritized alternative dielectrics (e.g., Hf-based) and gates (interfaces, defects, impurities, work function and band gap offset, mobility, leakage - including metal gates and FUSI) [4]** | | | | | **Modeling of new process steps / processing and properties of alternative materials** | |
| Continuum diffusion and activation models | **Calibration of present models for Si based materials including stress/strain, silicidation and new annealing steps (e.g., millisecond anneal)** | | **Refined and predictive models with better accuracy for upcoming process steps and applications** | | | | | | |
| Atomistic modeling for activation and diffusion* | **◆ Speedup of Kinetic Monte-Carlo** | | **Inclusion of stress, extension to other materials used in active device, calibration of atomistic modeling on first-principle calculations and experiments, integration with continuum process simulation** | | | | | | |

*Table MS2a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *23* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| *Topography and Material Modeling [5]* | | | | | | | | | |
| Etching / deposition | **(Surface) physics based feature scale models (including redeposition and stress)** | | **Integration of feature-scale simulation with equipment (plasma) models; electrical properties and stress including microstructure in deposition; layout dependence; process integration (coupling of etch-deposition-plating-CMP-lithography)** | | | **Including data beyond topography to also include surface and sub-surface material property prediction, full molecular dynamics (or atomistic) feature scale models** | | | |
| Alternative material modeling | **Calculation of thermodynamic and electronic properties** | | **Calculation of mechanical properties; process impact on intrinsic material behavior, integrity and electrical performance under strain** | | | | | | |
| Equipment impact on process results including material properties | | | | **Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale** | | | | | |
| *Numerical Device Modeling [6]* | | | | | | | | | |
| Transport modeling [7] | **Orientation-dependent mobility models including. field-dependent nonlinear strain effects, surface roughness effects of nitrided oxides and orientation of the channel** | | **Mobility models for high-κ gate stacks; efficient inclusion of quasi-ballistic transport** | | **Mobility models consistent with QM confinement in thin films (esp. SOI)** | | | | |
| Additional requirements for non-classical CMOS | **Device models to include additional interfaces (especially mobility in thin films)** | | **Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models** | | | | | **Nanoscale simulation capability including accurate atomistic and quantum effects** | |
| Novel devices * | ◆ **Single-cell modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs** | | **Material properties and reliability modeling of novel memory devices** | | | **Modeling of nanowires, graphene, etc.** | | | |
| Reliability and noise modeling | **HF, 1/f and RTS noise modeling** | | **Trap generation during operation (HCI, NBTI, PBTI, ….)** | | | | | | |

*Table MS2a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years*

<table>
<tr><td>Year of Production</td><td>2007</td><td>2008</td><td>2009</td><td>2010</td><td>2011</td><td>2012</td><td>2013</td><td>2014</td><td>2015</td></tr>
<tr><td>DRAM ½ Pitch (nm) (contacted)</td><td>65</td><td>57</td><td>50</td><td>45</td><td>40</td><td>36</td><td>32</td><td>28</td><td>25</td></tr>
<tr><td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)</td><td>68</td><td>59</td><td>52</td><td>45</td><td>40</td><td>36</td><td>32</td><td>28</td><td>25</td></tr>
<tr><td>MPU Physical Gate Length (nm)</td><td>25</td><td>23</td><td>20</td><td>18</td><td>16</td><td>14</td><td>13</td><td>11</td><td>10</td></tr>
<tr><td colspan="10">Circuit Component Modeling [8]</td></tr>
<tr><td>Active devices*</td><td colspan="2">◆ Compact models for non-classical CMOS/ non-quasi-static models for CMOS</td><td colspan="5">Circuit models for non-classical CMOS devices including reliability and influences of statistics; circuit models for classical CMOS including quasi-ballistic effects</td><td colspan="2">Circuit models for nanoscale devices and interconnects</td></tr>
<tr><td>Interconnects and integrated passives*</td><td colspan="2">Hierarchical process-aware full chip RLC [10]</td><td colspan="5">Include self-healing and reliability</td><td></td><td></td></tr>
<tr><td>Process and materials impact on electrical performance of interconnects *</td><td colspan="5">◆ Models that relate material properties (process related or fundamental) to electron transport (e.g., in conducting lines). Includes models for electron scattering. Models that predict paths to material property repair (e.g., low-κ repair, capacitance repair)</td><td colspan="4"></td></tr>
<tr><td colspan="10">Package Modeling</td></tr>
<tr><td>Electrical modeling*</td><td colspan="2">◆ Unified RLC extraction and multiscale modeling for package / chips</td><td colspan="2">Reduced order models</td><td colspan="2">Full-wave analysis</td><td colspan="3">Mixed electrical/optical analysis</td></tr>
<tr><td>Thermal-mechanical modeling *</td><td>◆Thermo-mechanical-integrated models</td><td colspan="2">◆ Include non-bulk and porous/air gap materials properties</td><td colspan="2">Include reliability (esp. life prediction)</td><td colspan="4"></td></tr>
<tr><td>Material properties *</td><td colspan="2">◆ Improved material models (visco-elasticity, creep, plasticity), interfaces</td><td colspan="2">Full die simulation</td><td colspan="5"></td></tr>
<tr><td colspan="10">Numerical analysis</td></tr>
<tr><td>Meshing *</td><td colspan="3">◆ Robust, reliable, efficient and user-friendly 3D grid generation including moving boundaries</td><td></td><td></td><td colspan="4"></td></tr>
<tr><td>Algorithms</td><td colspan="2">More robust and more parallelizable algorithms</td><td colspan="2">Discretization schemes alternative e.g., to box methods</td><td colspan="5">Efficient atomistic/quantum methods; ab initio or molecular dynamics based topography simulations</td></tr>
</table>

*Manufacturable solutions exist, and are being optimized* (white)
*Manufacturable solutions are known* (yellow)
**Interim solutions are known but research is still needed towards mature commercial solutions* (◆ yellow/red striped)
**Solution is not known, but this does not stop manufacturing* (red)

***Notes for Table MS2a and b:***

*[1] Non-standard final lens / standard resists*

*[2] Non-standard final lens / non-standard resists*

*[3] Models that at least roughly predict effects like oxygen vacancies and Hf-Si interface states are required, as those effects cause flatband shifts and fermi-level pinning. Currently there are no commercial tools available in a typical TCAD environment. Thus very phenomenological, a posteriori approaches are used. They are limited also to only some effects and by using models that were originally not designed for those effects.*

*[4] "Alternative" refers to materials so far not prioritized in PIDS*

*[5] Emphasis in topography steps shifted to material aspects towards long-term years*

*[6] In Numerical Device Modeling equations are solved that are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect to spatial coordinates) are employed. The goal is technology optimization and device insight*

*[7] This row includes all aspects important for all devices, that is, especially classical CMOS bulk devices*

*[8] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give guidance for the used relations between electrical quantities. The goal is a description of device behavior (currents, charges, noise) in circuit simulators*

*[9] This refers to a minimum of functional sub-circuits*

*Table MS2b Modeling and Simulation Technology Requirements: Capabilities—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *MPU Physical Gate Length (nm)* | *9* | *8* | *7* | *6.3* | *5.6* | *5* | *4.5* |
| *Lithography* | | | | | | | |
| Exposure | **NGL models and modeling of materials and components (immersion, EUV, ML2 lithographic processes, imprint)** | | | | | | |
| Resist models | **Models for non-conventional photo-resists and coupling with etch models** | | | | | | |
| *Front End Process Modeling* | | | | | | | |
| Gate Stack | **Modeling of new process steps / processing and properties of alternative materials** | | | | | | |
| Diffusion and activation models | **New technology needed** | | | | | | |
| *Topography and Material Modeling* | | | | | | | |
| Alternative material modeling | **Atomistic material model** | | | | | | |
| Equipment impact on process results including material properties | **Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale** | | | | | | |
| *Numerical Device Modeling [6]* | | | | | | | |
| Additional requirements for non-classical CMOS | **Nanoscale simulation capability including accurate atomistic and quantum effects** | | | | | | |
| Additional requirements for devices beyond non-classical CMOS | **Nanoscale simulation capability including accurate atomistic and quantum effects for ERD and ERM** | | | | | | |
| *Circuit Component Modeling [8]* | | | | | | | |
| Active devices | **Circuit models for nanoscale devices and interconnects** | | | | | | |
| Interconnects and integrated passives | **Mixed electrical/optical simulation** | | **Reliability prediction in coupled modeling** | | | | |
| *Package Modeling* | | | | | | | |
| Electrical modeling | **Reliability prediction in coupled modeling** | | | | | | |
| *Numerical analysis* | | | | | | | |
| Algorithms | **Multi-scale simulation (atomistic-continuum); fast coupling of equipment-topography-electrical-reliability models; hierarchical full-chip simulation** | | | | | | |

| | |
|---|---|
| *Manufacturable solutions exist, and are being optimized* | (white) |
| *Manufacturable solutions are known* | (yellow) |
| *Interim solutions are known* | (yellow hatched with red diamond) |
| *Manufacturable solutions are NOT known* | (red) |

*Table MS3 Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *23* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| ***Technology development costs reduction potential if TCAD is appropriately used [1]*** | **40%** | **40%** | **40%** | **40%** | **40%** | **40%** | **40%** | **40%** | **40%** |
| *Lithography Modeling* | | | | | | | | | |
| Absolute CD prediction accuracy (including OP effects) for dense and isolated lines – % of actual CD (=printed gate length) [2] | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** |
| Accuracy of sensitivity of CD vs. relevant technology parameters (dose, defocus, pitch, …. ) [3] | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** |
| *Front End Process Modeling* | | | | | | | | | |
| Vertical junction depth simulation accuracy (% of physical gate length) | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** |
| | **(2.5 nm)** | **(2.3 nm)** | **(2.0 nm)** | **(1.8 nm)** | **(1.6 nm)** | **(1.4 nm)** | **(1.3 nm)** | **(1.1 nm)** | **(1.0 nm)** |
| Lateral junction depth simulation accuracy: (% of physical gate length) | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| Accuracy of sensitivity of junction depth with respect to implantation and anneal conditions [3] | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| Total source/drain series resistance (accuracy of activation) | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** |
| *Topography Modeling* | | | | | | | | | |
| Wafer scale deposition/etching/CMP accuracy [4] | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| General 2D/3D topography accuracy (% accuracy of feature dimensions) | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| Gate 2D/3D topography accuracy (% accuracy of the MPU physical gate length) | **1.80%** | **1.80%** | **1.80%** | **1.80%** | **1.80%** | **1.80%** | **1.80%** | **1.80%** | **1.80%** |
| | **(0.45 nm)** | **(0.40 nm)** | **(0.36 nm)** | **(0.32 nm)** | **(0.29 nm)** | **(0.25 nm)** | **(0.23 nm)** | **(0,20 nm)** | **(1,8 nm)** |
| Gate sidewall spacer 2D/3D topography accuracy (% accuracy of sidewall width) | **5.00%** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** |
| | **(1.4 nm)** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** |
| Interconnect 2D/3D topography accuracy (% accuracy of MPU/ASIC Metal 1 (M1) ½ Pitch | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| | **(3.4 nm)** | **(3.0 nm)** | **(2.6 nm)** | **(2.3 nm)** | **(2.0 nm)** | **(1.8 nm)** | **(1.6 nm)** | **(1.4 nm)** | **(1.3 nm)** |
| *Numerical Device Modeling [5]* | | | | | | | | | |
| Accuracy of ft and fmax | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** |
| Gate leakage accuracy (% of Ig) [6] | **25%** | **25%** | **25%** | **25%** | **25%** | **25%** | **25%** | **25%** | **25%** |
| Ion accuracy | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** | **3%** |
| Leakage current accuracy including S/D gate leakage and band-to band tunneling | **30%** | **30%** | **30%** | **30%** | **30%** | **30%** | **30%** | **30%** | **30%** |
| Length-dependent Vt accuracy (mV) [9] | **10 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** |
| Width-dependent Vt accuracy (mV) [10] | **10 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** | **7 mV** |
| Accuracy of Gm and Gd at Vt +150mV versus L, Vbs, Vds and T | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** | **10%** |
| *Circuit Element Modeling/ECAD [11]* | | | | | | | | | |
| I-V error in saturation region | **6%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |
| I-V error in saturation region | **6%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** | **5%** |

*Table MS3 Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *23* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| I-V error in linear region | 3% | 3% | 3% | 3% | 3% | 3% | 3% | 3% | 3% |
| Leakage current including $I_{off}$ and gate current accuracy. | 10% | 10% | 10% | 10% | 10% | 10% | 10% | 10% | 10% |
| Intrinsic MOS C-V accuracy | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| Parasitic C-V accuracy | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| Accuracy of Gm and Gd at Vt +150mV versus L, Vbs, Vds and T | 10% | 10% | 10% | 10% | 10% | 10% | 10% | 10% | 10% |
| Circuit delay accuracy (% of 1/maximum chip frequency) | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% | 5% |
| *Package Modeling* | | | | | | | | | |
| Package delay accuracy (% of 1/off-chip clock frequency) | 1% | 1% | 1% | 1% | 1% | 1% | 1% | 1% | 1% |
| Temperature distribution for package (accuracy) | 3% | 3% | 3% | 3% | 3% | 3% | 3% | 3% | 3% |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

*Notes for Table MS3:*

*[1] This line does not give a quantitative assessment of the industrial requirement but gives the average of estimates obtained from companies on cost reductions in best practice cases through use of TCAD in development*

*[2] CD averaged - LER not included. After calibration of resist parameters*

*[3] Influence of process parameters on CD, etc. should be predicted with that maximum relative error*

*[4] For gate oxide this means atomistic precision*

*[5] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight*

*[6] Not including effects of high-κ / metal gate*

*[7] Absolute values strongly differ for HP and LSTP. Important aspects for nominal devices also included in rolloff accuracy*

*[8] (Positive) difference in Vth of nominal and subnominal device*

*[9] Difference between simulated and measured Vth for different channel lengths*

*[10] Difference between simulated and measured Vth for different channel width*

*[11] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give guidance for the used relations between electrical quantities. The goal is a description of device behavior (currents, charges, noise) in circuit simulators.*

# REFERENCES

The most recent version of other roadmaps including some future Modeling and Simulation topics for semiconductors is the iNEMI Technology Roadmap 2007 produced by the International Electronics Manufacturing Initiative[1]. Although the Technology Roadmap for Nanoelectronics[2] produced by the European Commission's IST programme (Future and Emerging Technologies) was already published in 2000 it still contains relevant information. Simulation issues addressed in the iNEMI roadmap are largely related to systems and products and therefore focus on reliability, electrical, and thermal simulation, furthermore on optoelectronics, microelectromechanical systems, and nanoscale/spintronics. The EU Nanoelectronics Roadmap elaborates especially on emerging devices beyond CMOS and the nanofabrication techniques needed for them. Whereas this gives relevant information for simulation on the long-term scale, molecular modeling is described in some detail. The working group received contributions to its discussion from the European Specific Support Action "SUGERT,"[3] funded by the European Commission within the ICT programme. SUGERT focuses on specifications and promotion of R&D actions in the area of TCAD. These three external activities well complement each other.

# INTER-ITWG ISSUES

In the following, links between Modeling and Simulation and all other ITWGs are outlined. These are based on a thorough investigation of the material from these ITWGs and broad cross-ITWG discussions.

## DESIGN / SYSTEM DRIVERS

One of the key problems that challenges design in connection with further shrinking feature sizes is the increasing variability of design-related parameters, resulting either from fluctuations of fabrication parameters or from the intrinsic atomistic nature, affecting for example, channel doping. This problem is discussed in detail throughout the Design chapter, and especially in the part on Design for Manufacturability. Modeling and Simulation can and must help to ease this problem by assessing the quantitative impact of such variabilities on the relevant design parameters: Statistical variations as well as drifts of fabrication parameters must be translated via appropriate equipment, process, and device simulation as well as parameter extraction into the resulting distribution of design parameters, such as size and spacings of active and passive devices, transistor characteristics, and coupling of interconnects leading to signal delay and distortion. Increasingly important is the atomistic nature of dopants which in some cases results in just one or a few dopant atoms being at average present in the channel region, giving rise to enormous relative fluctuations of doping and, in turn, electrical device parameters. Especially important are the interactions between different subsequent process steps, such as lithography and etching, which may either amplify or smoothen out such process fluctuations. Simulation should further contribute to the assessment of the impact of parasitics, delay variations, noise, and reliability issues, including thermal effects during operation. The treatment of such "second-order" effects is especially important for analog design where, for example, matching is a key issue. The overall target is to link design parameters more closely to the technology and device architectures used, especially including their process-induced variations, in order to help designers to select appropriate safety margins, which may vary within the layout. The added value which only simulation can provide is that a wide set of variations may be investigated largely automatically, within relatively small time, and at relatively small costs. In this way Modeling and Simulation must contribute to the solution of the problem that historical process tolerances can in future no more be met, and that therefore realistic estimates of the new tolerances and their implications must be provided. To achieve this goal, appropriate methodologies must be developed to extract from the microscopic TCAD simulations which are mostly carried out on device or cell level relevant information in a format which allows further processing with design tools—e.g., via SPICE parameters and their statistical distribution.

On short-term time scale especially issues related with mask making, e.g., the efficient definition and assessment of assist features needed to transfer features from layout into the photoresist, and variations of electrical data such as threshold voltage, are especially important. Simulation must not only contribute to the correction and adaptation of masks to make sure that the feature printed on the wafer approximates well enough the "ideal" structure intended by the designer, but also help to avoid costly overcorrection of the mask features, for example, by complicated assist structures and to select

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[1] *See http://www.inemi.org.*
[2] *R. Compano, ed. Technology Roadmap for Nanoelectronics. Second Edition. November 2000, see http://www.cordis.lu/ist/fet/nidqf.htm.*
[3] *See http://www.iisb.fraunhofer.de/en/arb_geb/sugert.htm.*

the most cost efficient mask structure for the printing of the required features on the wafer. Besides this, a long-term challenge will be especially the uncontrollable CD and dopant variability. In the end Modeling and Simulation should contribute to the design challenge of yield prediction and optimization, by providing the information on the impact of process variations and of dopant fluctuations, and on the printability of defects which would allow the designers to adapt their design to be less sensitive to these non-ideal effects and in this way maximize yield. Links to the Design and System Drivers chapters.

## Test and Test Equipment

Modeling and simulation of test equipment instrument, electrical delivery path, probe card or loadboard, and the device-under-test are required by the Test ITWG. Most important for Test is the signal integrity of power delivery and high speed signals. Whereas modeling of these issues can build especially upon the field of interconnect and package simulation, some of the issues (e.g., probe card and test socket) to be described are outside the classical domains of simulation considered by the Modeling and Simulation ITWG. It is, however, encouraged that the simulation community would extend their activities to contribute also to these problems which are important to support test activities. Another important aspect is the changing circuit sensitivity which may transfer an originally benign defect into a killer defect in future technology generations. Support from simulation would be important to assess the effect of defects especially on circuit performance. This may help Test to define criteria for defect detection. Furthermore, support from Modeling and Simulation is needed to differentiate between a good die which is influenced by intrinsic process variations and a defective die. Especially, a die may be influenced by process variations in a way that is still functional under standard application conditions, but due to insufficient margin fails after temperature or voltage stress employed in reliability tests. Here, support from Modeling and Simulation is needed to provide reliable models for these stressing mechanisms – similar to the link with metrology such models are needed to calculate the reliability data aimed at from the measurement data which are only available under the test conditions which are different from the later use of the circuits. Link to the Test and Test Equipment chapter.

## Process Integration, Devices, & Structures (PIDS)

The key innovations requested by the PIDS chapter include enhanced mobility (leading to strained Si), high-κ dielectrics, metal gate, Non-Classical CMOS (such as Fully Depleted SOI), and enhanced saturation current which requests ballistic transport. Other more long-term issues include atomic-level fluctuations, statistical process variations including line-edge and line-width roughness, new interconnect schemes, mixed signal device technology which will drive major changes in process, materials, physics, design, etc. With further shrinking feature sizes, new process steps, architectures and materials reliability issues on device, interconnect and circuit level are getting even more important and need support from Modeling and Simulation to achieve the development speed required. Especially for devices which use SOI material, existing models, such as for dopant diffusion and activation, carrier transport or for stress must be extended to cope with interface effects which get increasingly important compared with bulk properties. Design for Reliability needs simulation tools for concurrent optimization of circuit performance and reliability, and for the simulation of electromigration, thermal-mechanical stress, and process induced charging.

These issues are especially included in the Modeling and Simulation subchapters on “Front-End Process Modeling,” “Device Modeling” and “Interconnects and Integrated Passives Modeling.” Furthermore, Non-Classical CMOS devices require the development of appropriate compact models to support their introduction. Link to the PIDS chapter.

## Emerging Research Devices

Emerging Research Devices increasingly utilizes state variables different from charge (e.g., spin), which require a substantial extension of the current scope of modeling and simulation to the atomic scale. Modelling and simulation are critical in both providing fundamental understanding of the physical mechanisms and processes for both charge-based and non-charge-based information processing technologies and in interpreting metrology for nanotechnology structures. As the size of materials for devices continues to decrease, the impact of interfaces on the measured material properties will make separation of “bulk” and interface properties much more difficult. This increased role of interfaces together with new quantized physical phenomena caused by the nano-scale device structures drives improvement of first principle or *ab initio* modeling. This will allow predictive simulation of nanometer scale material properties and of nanoscale devices with non-charge state variables.

Due to the diversity of the Emerging Device Architectures being considered, and its long-term nature, required modeling and simulation cannot be just an extension of current models and tools needed within other areas of the ITRS. New modeling and simulation in the cross disciplinary nano domain must comprehend considerable contributions from other areas such as biology and chemistry. Link to the Emerging Research Devices chapter.

## EMERGING RESEARCH MATERIALS

Emerging Research Materials require basic models that correlate composition, structure, and synthesis to material properties. Especially, this needs improvement of first principle modeling to allow predictive simulation of nm scale material properties. A key problem here is that frequently the simulation of excited states is necessary, but not possible with state-of-the-art tools. Due to the diversity of the Emerging Device Materials being considered, and its long-term nature, required modeling and simulation cannot be just an extension of current models and tools needed within other areas of the ITRS. More details are given in the body of the ERM text. Link to the Emerging Research Materials chapter.

## RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

The requirements on simulation from RF and Analog/Mixed Signal Technologies for Wireless Communications include not only silicon-based substrates but also III-V compounds, certain device architectures beyond MOSFET, and the capabilities to simulate frequencies up to 100 GHz and beyond, higher levels of integration, cross-talk among circuit blocks, noise, and signal isolation. These requirements, in turn, increase the need for coupled device/circuit/system simulation of System-on-Chip (SoC) and System-in-Package (SiP); analog device modeling including the protection against electrostatic discharge; accurate and fast 3D electromagnetic and RF simulation and visualization; computationally efficient physical models for carrier transport; bandgap engineering, accurate, fast and predictive Analog/RF compact models. Device matching is an important issue. Simulation of heat generation and removal and thermal dissipation is even more important than for standard CMOS due to the higher power densities typically present in the wide bandgap semiconductors and wafer thinning used. The description of analog performance requires process and device simulation to be able to provide sufficient accuracy for prediction of mismatch and 1/f noise, e.g., for new high-κ gate dielectrics. The higher operating frequencies require simulations of the epitaxy steps and the alternative dopants (e.g., C). These aspects are to some extent addressed in the "Device Modeling," the "Interconnect and Integrated Passives Modeling," the "Circuit Element Modeling" and the "Materials Modeling" sections of this chapter. In addition, there is a role for modeling and simulation to assist in design strategies for RF isolation. RF signal isolation must be carefully managed to prevent performance degradation as the wireless communication schemes become more complicated. Link to the Wireless chapter.

## FRONT-END PROCESSES

The FEP challenges surround the introduction of new materials and of non-classical CMOS. This raises various requirements on Modeling and Simulation. Especially, in the coming era of material-limited device scaling, material issues need to be addressed in most modeling areas. This includes among others strained materials – so the importance of modeling of stress and strain is further growing. New device architectures request especially large progress in numerical device simulation, together with improvements of the simulation of the process steps used to fabricate these devices, e.g., the formation of shallow junctions. Both shrinking device dimensions and the non-planar architectures, especially also SOI devices, increase the impact of interfaces because the volumes in between are decreasing. These effects must be appropriately included in the physical process and device models. Process variations are getting increasingly important as devices further scale – a premier example is the redistribution of variance allowance between lithography and etching in the 2005 roadmap – and simulation can and must contribute to assessing the impact of such variants on the final device and chip. High-κ dielectrics are required to be introduced by 2008, so modeling must be able to describe them appropriately as soon as possible. The formation of ultra-shallow, abrupt, highly activated drain extensions continues to be a major challenge, and support from modeling is required both to improve the physical understanding for the processes used (e.g., kinetics of dopants and point defects during annealing) and to subsequently optimize them by numerical simulation. This knowledge is also needed for defect engineering, which aims at achieving shallower junctions by the exploitation of the interaction between dopant atoms and defects. Furthermore, the reduction of critical dimensions (CD) and the control of their variations including LWR and LER are generally a key issue, and it is highly desirable to use simulation to identify among the many parameters influencing CD the most important ones, in order to minimize experimental effort. Link to the Front end Processes chapter.

## LITHOGRAPHY

Support from Modeling and Simulation is critical both to push the limits of traditional optical lithography and to assess new Next Generation Lithography technologies. Furthermore, an intimate link between equipment-scale and feature-scale simulation is required for state-of-the-art lithography simulation. Equipment scale effects often require modeling with random variables with user-defined or user-measured probability distributions. While calculation of lithographic image formation relies on well-established physical models, the physical/chemical understanding of resist processes, particularly for chemically amplified resists, is far less advanced. Resist models are typically semi-empirical, and they require fitting and calibration with experimental data.

The key requirements for simulation of optical imaging are accuracy, speed of computation, and the capability to model the effects of non-ideal masks, non-ideal lenses, multilayer resists and non-planar substrates. With mask feature sizes at 4x reduction during imaging becoming comparable with the wavelength, polarization effects and the exact mask topography need to be included. Problem-specific algorithms and implementations are needed to deal with the "tricks" used when pushing optical lithography to the limits, such as off-axis illumination, complicated mask geometries including phase-shifting, and optical proximity correction (OPC). Non-idealities of the optical system used are getting more and more critical and must be appropriately addressed in simulation. The influence of defects on the mask and on the wafer is becoming more and more important and requires appropriate simulation capabilities especially for the identification of "killer defects".

New techniques used in future next generation lithography (NGL) techniques, such as replacement of lenses by multilayer mirrors and the use of reflecting masks for extreme ultraviolet (EUV) lithography must be appropriately modeled and included in the simulation programs. Mask pattern generators and some NGL options - including proximity electron lithography and maskless lithography - involve imaging with electrons. Simulations of stochastic space charge effects, geometrical aberrations and electron optical lens design performance using either magnetic or electrostatic lens elements are needed. Support from simulation for narrowing down the options for future Next Generation Lithography has been and will continue to be important.

Since the introduction of immersion lithography several additional requirements for Modeling and Simulation got important. Optical systems with NA > 0.85 must be simulated, which especially requires the appropriate treatment of polarization effects, including the use of polarized illumination and partial polarization by mask structures and materials. Simulation should also help to assess whether specific defects are due to bubbles in the immersion liquid. Additional requirements result from current research on various versions of double exposure techniques, which require the rigorous treatment of wafer topography in the simulation.

A specific challenge for lithography Modeling and Simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as Line-Edge Roughness (LER) and Line-Width Roughness (LWR). Better calibration techniques are required both for model development and for customizing models implemented in commercial tools to appropriately describe the photoresists in question. Calibration obviously depends on the quality of input data, e.g., CD measurements. Therefore, it is necessary to better understand and estimate measurement errors. Systematic errors should be dealt with by models of the measurement tools, for example, CD-SEMs. With the growing importance of LWR and LER, lithography simulation needs to contribute to the assessment of their influence on device and interconnect performance (LER) and variability (LWR). Since here not the roughness of the resist patterns is important but that of the etched structures, intimate coupling with etching simulation is indispensable. Simulations of etching are important to understand the relationship between 3D edge roughness and profiles in resist features and the resulting roughness and profiles in etched gates, contacts or trenches. Intimate links with etching simulation must also be established also to predict the geometry of non-ideal mask edges which are frequently result of the mask-making lithography steps.

A specific requirement for lithography Modeling and Simulation is the need for very efficient simulation tools which allow the simulation of large areas and/or the conduction of simulation studies for a multitude of variations of physical parameters or layouts to support growing design for manufacturing (DFM) needs. In fact, lithographic simulations of full-chip layouts are now needed to verify OPC and phase assignment data to avoid expensive masks being fabricated with errors or with corrections having only marginal performance. These simulations must be reasonably accurate and execute at high speed to evaluate the entire layout in a reasonable amount of time. Furthermore, simulation must contribute to the increased integration between design, modelling, lithographic resolution enhancement techniques and extensive metrology needed to maintain expected circuit performance.

Besides models of image formation and resist profile generation in the lithography process, mechanical models are also critical for designing lithography tools. Refinement and application of finite element methods is important for assuring exposure tools, masks and wafers remain stable enough to meet demanding overlay tolerances. Static and dynamic models of lens mounting stability, stage stability and also aspects of exposure tool hardware design are critical. Static and dynamic mechanical models are also critical for designing adequate mounting methods for masks and wafers to maintain desired position under high stage acceleration values and to maintain desired flatness. Equilibrium and non-equilibrium models of thermal effects are also essential for exposure tool design, especially for modeling heating of the immersion fluid in immersion lithography and its effect on distortion and aberrations. Models of fluid flow for immersion have also been essential in designing fluid delivery systems that minimize immersion-specific defect formation. Link to the Lithography chapter.

## CROSS-CUT BETWEEN INTERCONNECT AND DESIGN AND MODELING AND SIMULATION

The interconnect performance of future technology generations can no longer be provided by material and technology improvements alone. Therefore the interaction between material science, wafer technology, design, modeling, and simulation is becoming of even greater importance in supporting the continuing interconnect scaling. Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Furthermore, the models are largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and choose the correct interconnect routing, (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to utilize both the near term and far term proposed interconnect systems effectively. The upcoming new interconnect challenges are especially:

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1cm). This capability will also be needed for systems using RF or terahertz wave interconnections.
2. The impact of the Cu resistivity increase on delay time must be considered in realistic models. These models need to take into account line width, line aspect ratio, sidewall roughness, metal grain size, and the respective coefficients for grain boundary-, surface- and impurity-scattering.
3. Signal delay uncertainties because of crosstalk effects between neighboring interconnects and the impact of dummy metal features need to be considered in appropriate models. Because of increasing line aspect ratios these effects may become major issues.
4. Process variations (e.g., CD tolerances, line height variations, sidewall roughness, etc.) will become of ever increasing importance with further shrinking of interconnect line and via sizes. Therefore variation tolerant designs and variation sensitive models and simulations are needed to support the upcoming technology generations.
5. A means to optimally place function blocks will be needed for the '3D" integrated circuits not only on an individual die but also now on a stack of die.
6. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
7. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurrences of reliability critical 'hot spots' within the die. Predictive thermal models, that can accommodate thermal impacts of low-κ dielectrics with reduced heat conductivity, RF standing waves, the multiple heat generating layers embedded in the 3D IC stack, and heat generated by, as well as thermal performance of optical devices and quantum well devices will be needed

Modeling and Simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to prediction of resistivity increase of further shrinking copper interconnects (due to grain structures, Cu/barrier interfaces and impurities) and the physical structure and properties of new low-κ dielectrics and other more exotic interconnect materials.

In all of these cases Modeling and Simulation should provide predictions accurate enough to reduce as much as possible the need and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for Modeling and Simulation is ever increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical, and electrical modeling.

Specific interconnect needs for modeling and simulation include: performance prediction (including high frequency effects and reliability) for complex (e.g., 3-D) structures fabricated with real non-idealized processes (including etching, PVD, CMP), with hierarchical capability to choose the appropriate tradeoff between speed and accuracy for the application in question; tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; tools to calculate the degradation of electrical circuit performance due to resistivity increases over time of interconnect wires and vias, and materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier and dielectric). Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, and copper thinning and dishing in CMP. The treatment of the variability associated with line edge roughness, trench depth and profile, via shape, etch bias, and thinning due to cleaning is a key challenge to interconnects and their simulation. Links to the Interconnect and Design chapters.

## FACTORY INTEGRATION

The Modeling and Simulation chapter deals with the physical processes occurring during device fabrication and within an equipment, a device, or circuit. This physical simulation is very different from the discrete simulation of wafer flow, equipment usage, or lot scheduling which are within the core of Factory Integration. Nevertheless, also the physical Modeling and Simulation can and must contribute to the strategic goal of Factory Integration: cost, productivity, and speed.

Especially, the overall objective of physical Modeling and Simulation, to reduce the development times and costs of new technologies and ICs, is in line with one of the Factory Integration goals: to enable rapid process technology shrinks and wafer size changes. Physical Modeling and Simulation can and must contribute to this goal by exploiting equipment, process, device and circuit simulation tools especially to investigate the possibilities and impacts of shrinking the technology initially introduced in a fabrication line to smaller feature sizes, which is vital for the reduction of fabrication costs. Moreover, similar to the Yield Enhancement chapter also for Factory Integration the use of physical Modeling and Simulation to investigate the influence of process variations on the amount of devices and ICs which are within product specifications is highly important. This can also help to increase the productivity of equipment: Simulation can be useful to quantify the impact on device or IC performance of variations within an equipment or between different pieces of equipment as well as of process variations (for example, in lithography) and in this way contribute to the right strategy for efficient use of the equipment (TCAD for DFM) or appropriate optimization of the process flows to achieve the highest yield (TCAD for Yield). Especially, one potential solution defined already since some years in the Factory Integration chapter is the “automated design rule checking to ensure that masks are designed for manufacturability.” Here, especially lithography simulation can be used to predict the feature generated on the wafer for a given mask and process, and moreover to optimize mask and/or process to achieve best results on the wafer with least mask complexity. Specific support from physical Modeling and Simulation is needed in the area of APC (Advanced Process Control) and Forward/Backward Control: Here, efficient physical process models are needed to be able to adapt process steps to compensate for deviations which occurred in preceding steps or for process drifts which frequently occur between the regular maintenance and calibration processes of the equipment used. In this context the key requirement on physical Modeling and Simulation is not the development of predictive (sometimes even three-dimensional) models but of simplified and computer-efficient tools which in the ideal case allow for in-line and real-time application, coupled with in-situ or in-line metrology and APC software. Link to the Factory Integration chapter.

## ASSEMBLY AND PACKAGING

The cross-cut needs from Assembly and Packaging to Modeling and Simulation consist of co-design in two respects: Between chip and package, and including as well mechanical, electrical, and thermal simulation. They are closely related to the requirements on Modeling and Simulation raised from the Interconnect chapter. Additionally, lower voltages and higher currents have significantly increased the need for chip-package co-design to minimize the effects of high-current transients on very low-level signal lines. RF/mixed signal models are needed, and modeling tools need to be extended to enable the simulation of complex SoC and SiP packages.

Assembly and Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Advanced modeling tools covering the related electrical, thermal, and mechanical aspects are needed to support the development and optimization of these technologies.

Especially important is that these effects can no longer be treated separately and must, in turn, also simultaneously be simulated. Whereas the requirements in terms of processes, materials, and effects to be included in Modeling and Simulation are rather similar to those raised by the Interconnect chapter, the key additional requirement is the need to manage the large complexity and configurations of chip-package co-designs. This requests memory and CPU efficient hierarchical simulation capabilities to be able to deal with the high clock frequencies and high densities occurring. Reduction techniques in time-domain or frequency-domain are needed as well as computationally efficient full-wave simulation tools. Thermal and mechanical models used must be based on realistic material data, including air flow, stress predictions in accelerated test, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. Understanding material interfaces for metal/polymer, polymer/polymer, and intermetallics for process development and reliability projection will be extremely important. Thinned die, low-κ and other new materials and new package types such as stacked die and other 3D circuits must be included. Models need also to include manufacturing and assembly processes such as adhesive/undersell flow or BGA rework. Simulation methods to predict reliability are needed to speed up development processes. From the view of packaging, design and process tolerances should be taken into account especially for backend of the line. Also for packaging simulation faster simulation capability is needed because currently simulation sometimes takes days.

The proliferation of new package architectures combining multiple active and passive devices in a single package SiP have increased the need for modeling and simulation tools. Such structures cannot meet cost and reliability requirements without the ability to simulate thermal, mechanical, and electrical properties of the complete SiP.

It is anticipated that near-term Modeling and Simulation needs of Assembly and Packaging will be addressed by non-optimally combining available capabilities, or by evolutionary extension of these capabilities. In the longer term it is desired that a more complete system approach will be provided. Link to the Assembly and Packaging chapter.

## ENVIRONMENT, SAFETY AND HEALTH

Also Modeling and Simulation is requested to respond to ESH issues. It is not sufficient to limit the impact of simulation to the reduction of the numbers of wafers needed during process development and optimization, which saves costs and (partly ESH-relevant) resources. Moreover, simulation should also contribute to the reduction of resources including critical chemicals during production, by minimizing deposited wafer thicknesses, material removal in CMP, and the frequency of cleaning processes to the amount really needed to achieve the desired result in terms of device and IC performance and reliability. To this end not only appropriate modes and simulation tools must be available, similar to the requests by the other chapters, but also resource conservation must be introduced as an additional target figure and metric for simulation.

For the optimization of ESH issues, the elementary chemical reactions in each relevant process must be understood as far as possible, and new measurement and evaluation methods must be implemented for developing processes which have the lowest ESH impact. Similarly, availability of these measurement methods and knowledge of the reactions is also a key requirement for the development of predictive models for those processes, which are dealt with in the Modeling and Simulation chapter. In turn, many enabling measurement techniques can be shared between ESH and the Modeling and Simulation community, although the final targets of the two areas are different: Assessment of material consumption and occurrence of hazardous species for ESH versus the geometry, doping, and morphology of layer stacks in Modeling and Simulation. Moreover, the implementation of such models in equipment simulation programs, especially for plasma processes, also offers the possibility to ESH to obtain quantitative data for the generation of hazardous species and in the ideal case also for optimization of equipment and process conditions to minimize the generation of these species or their release from the process equipment. Moreover, simulation can frequently contribute to characterization techniques by converting measured data (like spectra) into quantitative data (for example, on gas composition). See the cross-cuts with Metrology. In this way ESH and Modeling and Simulation have the potential to support each other well. Link to the ESH chapter.

## YIELD ENHANCEMENT

Besides the standard use of Modeling and Simulation to reduce development times and costs, links between Yield Enhancement and Modeling and Simulation are twofold: First, Modeling and Simulation can contribute to the assessment of the influence of defects on the ICs. An obvious example is the question whether mask defects of a specific size, kind, and position are printed during an optical lithography and subsequent etching steps. This can be studied by state-of-the-art simulation tools for optical lithography, which also allows identification of critical defect sizes above which the device or IC is destroyed, for example because the defect will cause otherwise separate lines to be connected. Especially for the investigation of defect limits for patterning steps simulation offers very good prospects provided the simulation tools are further developed accordingly. The propagation of defects in subsequent process steps through to devices and ICs and the mutual interactions of defects can be studied with various other Modeling and Simulation tools to monitor and minimize their impact. In this way Modeling and Simulation could in many cases best answer the question whether a certain kind of defect at a certain stage of processing is critical or not, and what could be its corresponding threshold size.

Another important problem is the assessment of the impact of largely inevitable process fluctuations on the performance of devices and ICs. Many parameters in a fabrication line are distributed around their nominal values with some tolerances, like anneal temperatures, times, and ramp profiles, or have some drift in time. Advanced process control (APC) is frequently used to reduce the impact of such fluctuations by feeding metrology data back into process recipes. Control models are largely based on silicon data that is expensive to generate and might be available for mature processes only. Coupled process and device simulations can help to develop more accurate APC models in shorter time. By using process and device models calibrated in the process integration phase, APC models can already be developed for process transfer and production ramp up.

A second method addressing the problem of process fluctuations uses coupled process and device simulation to calculate the spread of critical product parameters resulting from such distributions of fabrication parameters, or the intrinsic variability of process steps (e.g., line edge roughness and other CD variations) or dopant fluctuations. Using this method statistical SPICE models can be derived before statistical fabrication data is available, and in this way contribute to the early assessment and optimization of the yield for a specific product and fabrication technology. Effects which are of most concern to yield enhancement have already in 2005 included line edge roughnesses, the impact of which can be well assessed with (especially lithography) process simulation. Moreover, process variations and defects are frequently closely related: A variation may gradually change a continuous variable like a line width in a way that devices or ICs suffer a discontinuous change, e.g., that a line if interrupted in a subsequent process step. In such cases a defect which seems to be random in nature can in reality be due to a systematic mechanisms, like limited depth-of-focus in optical lithography. Simulation can be used to detect and quantify such effects.

Obviously, these contributions from Modeling and Simulation to Yield Enhancement require sufficient generality, accuracy, and speed of application of the simulation tools to be used, and are a challenge for the future development of Modeling and Simulation. Link to the Yield Enhancement chapter.

## METROLOGY

Strong bi-directional links exist between Metrology and Modeling and Simulation. A key issue in the development of physical models for semiconductor fabrication processes and equipment as well as devices is the availability of measurement techniques and methodologies that are capable of characterizing quantities such as geometry and chemical composition of layer stacks, dopant distributions, (point) defects, stress/strain, carrier concentrations, lifetime and mobility with the high accuracy and spatial resolution, and low detection limit required to enable model development and evaluation. Metrology is needed that gives sufficient information for true three-dimensional structures. In many cases it must be applicable to real structures rather than test structures designed for that specific purpose. A further complication results from the required measurement and model accuracy approaching or even getting lower than the distance between individual (dopant) atoms. In these cases the interpretation of measurement results becomes questionable, whereas in simulation the transition from continuum models based on partial differential equations to atomistic calculations is being accomplished.

The requirements of Modeling and Simulation contribute to driving the development of Metrology. However, simulation not only raises requirements but also can and must contribute to the development and use of metrology itself. The physical understanding of the processes occurring in the semiconductor and other materials considered is in many cases extremely valuable or even indispensable to interpret data collected in metrology and to convert them into quantitative information, to give realistic error estimates, and even to design or customize a measurement method. Generally speaking, Metrology has repeatedly confirmed it's requirement to "use modeling to connect what you can measure with what you can see" —and related issues mentioned in the Metrology chapter are manifold, see the Metrology chapter. For example, simulation can be used to relate variations of process parameters or atomic fluctuations to spreads of quantities that are measured, and in this way help to correctly interpret measurements: Quantify how much the variation of the variable to be measured on one hand side and the error of the measurement method on the other hand side contribute to the variation and repeatability of the measurement signal recorded. Some other examples are the use of simulation to support and complement mask metrology, scatterometry, and the application of metrology for APC. Frequently a layer or a device is during characterization stressed by temperature or voltage, for example, in a way which is quite different from its standard operation conditions, but needed to shorten measurement times to acceptable values, or specific test structures are used which however change the quantity to me measured, e.g., in case of mechanical stress. Also in such cases reliable modeling tools are needed to calculate the quantity of interest from the signal which was more or less modified by the measurement itself—currently, insufficient knowledge about the physical mechanisms involved and in turn the lack of appropriate simulation support frequently invalidates the measurement result.

Frequently modeling groups directly contribute to the development and customization of measurement methodologies required to provide the data needed for model development. For example, with the increasing variety of new materials and processes in gate etch processes and complexity of gases and materials involved in dielectric etch and process cleans, simulation is called for creating a reliable means to characterize process emissions. In most cases, what evolves from surfaces or in the gas phase is unknown or difficult to synthesize outside of the particular process set-up and equipment. An emerging means of identifying species of potential environmental risk is through computational spectra generation. Synthetic reference spectra for materials can be generated with relative ease using computational chemistry approaches. For example, FTIR (Fourier-Transform Infrared Spectroscopy) spectra have been used to identify radicals of the RuOx system in Ruthenium etch processes and to scan for noxious gases to ensure they are not produced in highly polymerizing dielectric etch gas chemistries. In both these cases, experimental reference spectra are difficult to generate or difficult to obtain.

Furthermore, it is frequently possible to verify simulation models and tools using measurement methods available (such as 2D measurement of cross sections), and then to use them beyond the domain directly accessible to measurement techniques (for example, for 3D profiling) because in that cases the physics has not changed and the difference between the two situations can reliably be handled by the algorithms in the simulator (solving partial differential equations in three instead of two dimensions). To conclude, Metrology and Modeling and Simulation must continue and even further extend their efforts to cooperate closely to take best advantage from each other. Link to the Metrology chapter.