INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

SCOPE

Radio frequency and analog/mixed-signal (RF and AMS) technologies now represent essential and critical technologies for the success of many semiconductor products. Such technologies serve the rapidly growing wireless communications market. They depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe and others of which are not compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table.

Recognizing wireless applications, which are enabled by RF and AMS technologies, as a major system driver for the ITRS, we include semiconductor market requirements that are likely to be met by products from CMOS compatible processing and those that are likely to be met by products from processing that is not compatible with CMOS processing. The latter becomes more significant as today's emerging research devices, especially those devices based on the More than Moore (MtM) technologies described in this 2007 ITRS, are deployed in the marketplace.

The purposes of this 2007 ITRS RF and AMS Chapter are as follows:

1. Present the challenges that RF and AMS technologies have in meeting the demands of wireless applications for cellular phones, wireless local area networks (WLANs), wireless personal area networks (PAN), phased array RF systems, and other emerging wireless communication, radar, and imaging applications operating between 0.8 GHz and 100 GHz.
2. Address the intersection of Si complementary oxide semiconductor (CMOS), bipolar CMOS (BiCMOS), and SiGe heterojunction bipolar transistors (HBTs) with III-V compound semiconductor devices.

This 2007 RF and AMS Chapter continues with the structure it had for the 2005 ITRS in that it provides consistent requirements of the basic technology elements (CMOS, bipolar devices, and passives) used in wireless communication front-end circuits and that it still maintains the original 2003 ITRS applications driven roadmap. This 2007 RF and AMS Chapter has five main sections. The four sections on RF and AMS CMOS, RF and AMS Bipolar Devices, On-Chip and Embedded Passives for RF and Analog, and Power Amplifiers (PAs) cover primarily but not exclusively the 0.8 GHz to 10 GHz applications and one section on millimeter wave covers the 10 GHz to 100 GHz applications. These frequencies refer to the nominal carrier frequencies for communications and are not necessarily the clock or operating frequencies of the individual devices and circuits. Even though the millimeter wave spectrum is considered to start at 30 GHz, this section has been extended down to 10 GHz because the challenges, technical requirements, and technologies for the 10 GHz to 30 GHz spectrum are similar to those for the 30 GHz to 100 GHz spectrum.

In addition to the five sections mentioned above, this Chapter has a new Section on "More than Moore" that includes discussions on solutions to realize multi-band, multi-mode, portable applications via all-digital radio design or a hybrid approach which uses a wideband amplifier with switching and filtering network. RF microelectromechanical systems (RFMEMS) and Embedded Laminate Passives (incorporated in the Passives Section) requirements are added to the roadmap as essential technologies needed to realize the switching and filtering network.

The drivers for wireless communications systems are cost, frequency bands, power consumption, functionality, size of mobile units, very high volumes of product, and standards and protocols. Also, RF technologies often require additional headroom with respect to performance because several conflicting or competing requirements have to be met simultaneously. These include power added efficiency (PAE), high output power, low current, and low voltage. Increased RF performance for silicon is usually achieved by geometrical scaling. Increased RF performance for III-V compound semiconductors is achieved by optimizing carrier transport properties through materials and bandgap engineering. During the last two decades, technologies based on III-V compounds have established new business opportunities for wireless communications systems. When high volumes of product are expected, silicon and more recently silicon-germanium replace the III-Vs in those markets for which these group IVs can deliver appropriate performance at low cost.

The wireless communication circuits considered as application drivers for this roadmap may be classified into AMS circuits (including analog-to digital and digital-to analog converters), RF transceiver circuits (including low noise amplifiers (LNAs), frequency synthesizers, voltage controlled oscillators (VCO), driver amplifiers and filters) and PAs.

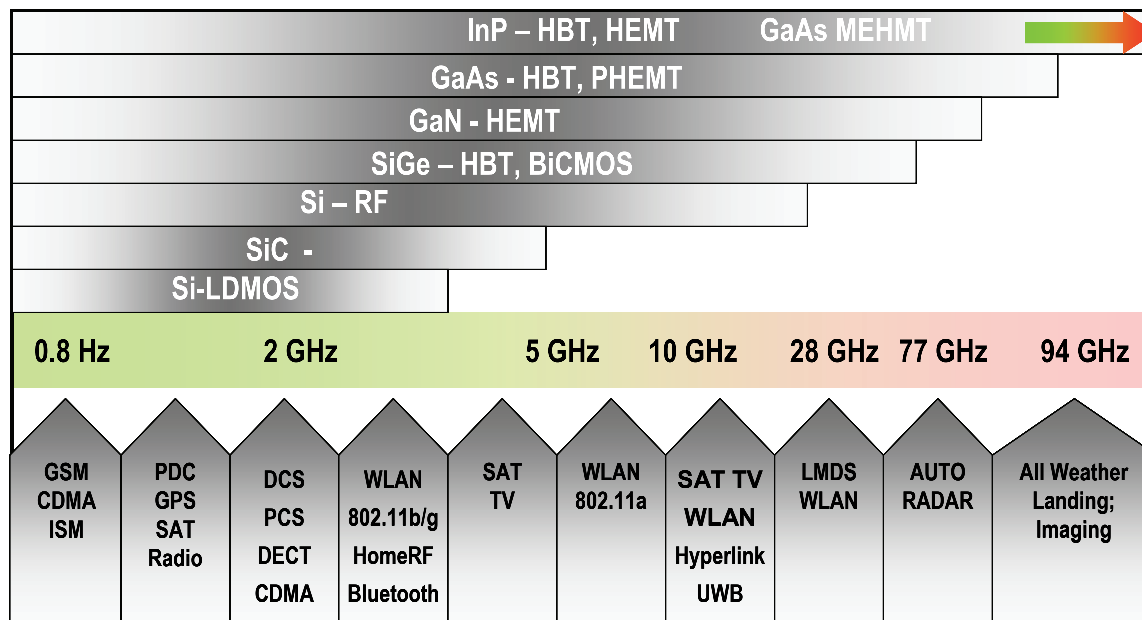


Figure RFAMS1 Wireless Communication Application Spectrum

Compound III-V semiconductors have traditionally dominated the millimeter wave spectrum over the past several decades. However, today, with the drive to low-cost high-volume applications such as auto radar, along with scaling to sub-100 nm dimensions, the group IV semiconductors Si and SiGe are rapidly moving up to frequencies that were once the exclusive domain of the III-Vs.

Wireless applications and technologies capable of addressing them are illustrated in Figure RFAMS1. Compared to the same chart in the 2005 Roadmap, all the technologies have moved to higher frequencies. Nevertheless, with the exception of GaN high electron mobility transistors (HEMTs), the relative positioning of the technologies remains essentially the same.

The consumer portions of wireless communications markets are very sensitive to cost. As a result, developing RF and AMS technology roadmaps for such applications is not straightforward. Cost is one of the key factors determining the choice of technologies among the kinds of RF semiconductor and device technologies shown in the top part of Figure RFAMS1. The boundaries are not as well defined as Figure RFAMS1 may suggest, but are broad, diffuse, and change with time.

The boundary between the group IV semiconductors Si and SiGe and the III-V semiconductor GaAs has been moving to higher frequencies with time and for other applications the boundary between GaAs and InP is tending to shift to lower frequencies. Eventually, metamorphic high electron mobility transistors (MHEMTs) may displace both GaAs pseudomorphic high electron mobility transistors (PHEMTs) and InP high electron mobility transistors (HEMTs) for certain applications. In fact, InP HEMTs and GaAs MHEMTs show promise well into the sub THz spectrum (which is beyond the scope of this roadmap). While the wide bandgap semiconductor GaN currently competes with silicon discrete laterally diffused metal oxide semiconductor (LDMOS) (Si-LDMOS) for infrastructure such as base stations at frequencies around 2 GHz, recent research papers suggest that GaN will be capable of significant power and efficiency through 60 GHz, and perhaps even to 94 GHz, by the end of this decade. While Si-based technologies will prevail for high volume, cost sensitive markets in the millimeter wave range, they are unlikely to replace III-Vs in applications where either high power, gain or ultra low noise is required. Conversely, for low volume applications, III-Vs are likely to prevail due to the high initial costs in fabrication infrastructure [e.g. mask sets] for Si technologies.

In future years, it is expected that the frequency axis in Figure RFAMS1 will lose its significance in defining the boundaries among technologies for some of the applications listed therein. This expectation occurs because most of the technologies in Figure RFAMS1 can provide very high operating frequencies. The future boundaries will be dominated more by such parameters as noise figure, output power, power added efficiency, and linearity. Two or more technologies may coexist with one another for certain applications such as cellular transceivers, modules for terminal PAs, and

millimeter wave receivers. Today, BiCMOS in cellular transceivers has the biggest share in terms of volume compared to CMOS. But, the opposite may occur in the future as evident by the expanding wireless local area network (WLAN) connectivity market that is dominated by CMOS transceivers. Today, both GaAs HBT and LDMOS devices in modules for terminal power amplifiers have big market shares compared to GaAs PHEMTs and GaAs metal semiconductor field effect transistors (MESFETs) but these are being displaced by a maturing GaN technology. In the future, silicon-based technologies having higher integration capabilities will gain importance as systems require higher degrees of functionality. Today we see GaAs PHEMTs and InP HEMTs in millimeter wave receivers. In the future, we may see competition from SiGe heterojunction bipolar transistors (HBTs), GaAs MHEMTs, and GaN HEMTs.

RF AND AMS CMOS

The scope of this section includes RF and analog characteristics of CMOS devices in the Low Standby Power (LSTP) Roadmap and higher voltage devices that are required for precision analog applications or for driving RF signals off-chip. The LSTP Roadmap was selected as the basis for this section of the RF and AMS Roadmap because portable applications require low standby power and higher bias voltages than High Performance (HP) or Low Operating Power (LOP) CMOS. The devices in this roadmap are identical to those in the LSTP roadmap, but they are placed into production one year later to allow development of high-frequency models and other tools to support RF and AMS design. These devices are in circuits for transceivers, frequency synthesizers, and LNAs. Although analog speed is mainly driven by RF, there are certain analog-specific needs for analog precision MOS. Therefore, this section also includes discussions on analog precision MOS device scaling, but with relatively high voltages to achieve high signal-to-noise ratios and low signal distortion. Such devices are typically available in CMOS technology offerings to support interfacing to higher-voltage input/output (I/O) ports.

A millimeter-wave table is introduced in this section that includes RF characteristics of CMOS devices in the High Performance (HP) Roadmap being placed into production two years after the digital roadmap to allow for development of high-frequency models and design tools necessary to support the design of millimeter wave applications. The HP Roadmap was selected as the basis for this table assuming early designers would select the inherent higher performance of the aggressively scaled CMOS. The LSTP Roadmap may be adopted as designer confidence grows or mobile applications emerge and require lower standby power. The entries for the near-term years of this table are also included in the table for the Millimeter-Wave Section.

RF AND AMS BIPOLAR DEVICES

The scope of this section is to provide requirements for bipolar performance. Bipolar performance is being driven by two distinct applications: millimeter wave, which requires very high speeds, and power amplifiers, which require a more balanced combination of speed and voltage handling capability. Wireless transceiver applications in the 0.8GHz to 10GHz range continue to be the largest market for bipolar and BiCMOS technology but are no longer driving the leading edge performance since existing bipolar performance levels are sufficient for these lower frequency levels.

To reflect the two distinct driving forces, the roadmap includes two primary devices (the high-speed and the PA NPN) and a derivative device (the high-voltage NPN). The high-speed device is driven by the requirements of millimeter wave applications while the PA device is driven by the requirements of power amplifiers. The high-voltage device is derived from the high speed device typically by modifying the collector in the same technology.

ON CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

The scope of the on-chip passives section includes passive components used in RF and AMS circuits for wireless communications: 1) capacitors, 2) resistors, 3) inductors, 4) varactors, and 5) other passives for power amplifiers. Unlike digital CMOS circuits, the performance of many RF and AMS circuits are mainly determined by the performance of passive elements. Voltage and temperature coefficients are key parameters for capacitors and resistors. Also, capacitors and resistors are used in AMS circuits such as analog-to-digital and digital-to-analog converters that have clock frequencies below 0.8 GHz.

The passives section is expanded in the 2007 roadmap to include embedded passive devices that have growing applications in RF front-end modules, especially as the wireless market migrates to support multi-standard handsets. The scope of this section covers discrete components or chips integrated into package substrates to form passive devices. The substrates can be organic, such as printed circuit boards (PCBs) or in-organic, such as silicon or ceramic for both thick and thin film processes known either as multilayer substrate or high density interconnection (HDI) technology.

POWER AMPLIFIERS (0.8 GHZ–10 GHZ)

The scope of this section includes: III-V HBTs, III-V PHEMTs, Si metal oxide semiconductor field effect transistors (MOSFETs) and SiGe HBTs for terminal PAs. High voltage devices in base station power amplifiers, such as Si-LDMOS, GaAs FET, SiC FET and GaN FET, are also described in this Section. The key driving forces are integration of components and cost.

HANDSET PA

Wireless communications require both portable and fixed transmitters and receivers to form a connected network. The public is most familiar with portable devices that take the form of cellular telephones and wireless personal digital appliances (PDAs). Power amplifiers (PAs) for these portable devices will be discussed first. The PA in handheld devices is always a PA module (a multifunctional component that may contain a Si power management chip, RF matching networks, RF switches, and PA chips) capable of supplying 1-4 Watts of RF power to the antenna of the portable device. Si CMOS or BiCMOS is typically used for power control circuitry (when there is no on-chip bias) and can also include the switch logic control functions. The RF matching components are used in the form of discrete components or custom integrated passive devices (IPDs) which are specially designed chips containing only passive elements in combination. These components are combined with transmission lines or passives embedded in a laminate structure to form the matching networks. GaAs PHEMTs are the most commonly used RF switch technology with silicon on sapphire (SOS) only recently becoming popular. GaAs HBT, Si-LDMOS, SiGe HBT, and GaAs PHEMT technologies are used for the power amplifier chip. Several components may be combined on the same semiconductor chip. A recent trend is to combine the PA controller function with the switch function or the switch function with an integrated passive device (IPD). By combining several different PA module functions on a single chip component count and wire bonding complexity can be reduced which, hopefully, leads to lower cost modules. These technology combination approaches will become more prevalent as PA modules are required to service an increased number of frequencies and modulation formats in years to come. The choice of which technology to use for each function depends on the RF performance specifications, die size, availability, and most importantly total product cost.

BASE STATION POWER AMPLIFIERS

The cellular base station which also contains power amplifiers completes the communications link between the portable device and the wire-line telephone network. However substantially higher RF power (600 W) is required to achieve the desired cellular phone coverage. A single base station may contain ten's of these 600 W transmitters to handle all of the cellular phone traffic at a particular base station site. The heart of these transmitters is the RF semiconductor power device that must provide the final amplification to the data signal in order to achieve the desired output power. Typically, several semiconductor devices are connected in parallel to achieve these high powers. Silicon LDMOS transistors are now the technology of choice for cellular systems at 900 MHz and at 1900 MHz because of their technological maturity and low cost. The typical operating voltage of LDMOS devices is 28V, but these 28V devices can actually be operated at 32V in order to increase their output power. LDMOS devices operating at 48V are also becoming available. Gallium arsenide RF power transistors are also used at these frequencies and will be used more as wireless infrastructure frequencies move above the 3500 MHz range. Gallium arsenide devices are more expensive, but offer higher efficiency and higher power density than silicon LDMOS. The higher power density is important because it reduces the complexity of the RF matching networks required to efficiently connect the power transistor to the other parts of the transmitter circuitry. A less complex matching network has lower loss. Gallium nitride, another technology coming over the technological horizon, offers even bigger improvements over gallium arsenide. Gallium nitride has power densities four times larger than either SI-LDMOS or gallium arsenide. This tremendous increase in power density is the result of GaN's higher breakdown voltage and the higher current density. SiC RF power devices have been removed from consideration for base station applications because their performance is substantially inferior to that of Si LDMOS, GaAs, and recently GaN devices.

MILLIMETER WAVE (10 GHZ–100 GHZ)

Commercial interest in the millimeter wave spectrum has grown steadily over the past decade. Unlike most of the lower frequency spectrum, where silicon based technologies dominate, there are a number of distinct semiconductor and device technologies which compete for the applications marketplace, each offering unique tradeoffs in cost, performance and availability, .Currently, devices and integrated circuits are manufactured on four substrate materials: GaAs, InP, SiC, and Si. While the III-V compounds dominated the millimeter wave spectrum a decade ago. Si-based device technologies have crept into this applications arena, driven primarily by advantages in cost and integration level. In the future, we may see other III-V compound semiconductors, and even C-based semiconductors [including diamond] being developed for this spectrum [cf. Emerging Research Devices].

In this section, we present transistor technologies which are, or are forecast to be in commercial production for millimeter wave applications in Near-term Years, Because this field is rapidly expanding, and because performance in not tied so tightly to lithographic dimensions as are digital integrated circuits, we have purposely omitted projections into the Long-term Years. Compound semiconductors do not enjoy the long-term heritage of silicon-based devices, nor do they follow Moore's Law. As the millimeter wave spectrum markets and products develop and become more of a technology driver, it may be more plausible to carry the roadmap for millimeter waves into the Long Term for future ITRS editions.

The scope of this section includes low noise and power transistors that are based on the following device and material technologies: GaAs PHEMT, GaAs MHEMT, InP HEMT, GaN HEMT, InP HBT, SiGe HBT, and RF CMOS. Except for SiGe HBTs and RF CMOS, all device types employ epitaxial layers that are composed of ternary or quaternary compounds derived from column III and V of the periodic chart. There is great diversity in the nature and performance of these devices because device properties are critically dependent on the selection of materials, thickness, and doping in the epitaxial layers, which are proprietary to the manufacturer. Trade-offs among power, efficiency, breakdown, noise figure (NF), linearity, and other performance parameters abound. One consequence of these trade-offs is that the "lithography roadmap" is not the primary driver for millimeter wave performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit, such as maximum transit frequency (F_t) and maximum frequency of oscillation (F_{max}). Performance trends are driven primarily by a combination of desirable trade-offs and "bandgap engineering" of the epitaxial layers in concert with shrinking lithography

DIFFICULT CHALLENGES

RF AND AMS CMOS

The steady improvement in the digital performance of the basic devices in the LSTP Roadmap derived from scaling will also result in continuous improvement in RF and analog performance. As dimensions shrink new tradeoffs in physical design optimization will be necessary as different mechanisms emerge as limiting factors determining parasitic impedances in local interconnects to the device. Furthermore, the requirement of low standby power for digital circuits limits the rate of reduction in gate oxide thickness relative to gate length and, for conventional device structures, drives ever increasing doping concentration in the device channel. These trends degrade voltage gain and increase the threshold mismatch between adjacent devices. The introduction of new materials such as high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes makes forecasting trends uncertain for threshold and current mismatch and for 1/f noise. Eventually, fundamental changes in device structures such as the introduction of dual-gate, fully-depleted SOI will be required to sustain continued performance and density improvement. The fully-depleted SOI structure prohibits a contact to the device body. Thus, the electrical characteristics of these devices are fundamentally different from that of conventional CMOS. These differences include benefits for circuit designers as well as obstacles to be overcome. Potential benefits include higher voltage-gain and lower coupling between the drain and body. Furthermore, SOI device behavior degrades at high bias due to accumulation of channel charge due to avalanche current. Finally, the steady reduction in analog supply voltage poses a significant circuit design challenge. Thus, the fabrication of conventional precision analog / RF driver devices and resistors and varactors may require separate process steps with the attendant increase in die cost.

RF AND AMS BIPOLAR DEVICES

For the high-speed device the primary challenge is in continuing to drive F_t by more aggressive vertical profiles while still maintaining manufacturing control and punch-through margin. The second major challenge is in being able to handle the large current density and power density that results from the aggressive vertical profiles.

For the PA device the major challenge is in improving the tradeoff between F_t /F_{max} and breakdown voltage to provide voltage handling and power densities at performance levels that can effectively complete with alternative technologies.

ON-CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

ON-CHIP PASSIVES

Passive components include resistors, capacitors, inductors, varactors, transformers, and transmission lines. They are frequently used for impedance matching, resonance circuits, filters, and bias circuits in radio frequency integrated circuits (RFICs), such as LNAs, VCOs, mixers, and PAs. Even in some RF circuits, the performance of RF CMOS transistors is usually good enough for most of the applications well beyond 10 GHz. Therefore, the RF performance of passive devices always plays a key role in determining the overall characteristics of the entire circuit. For instance, integrating VCOs into RF transceivers with standard CMOS technologies is usually one of the most challenging design tasks, because there are

many critical parameters that must be considered. Examples of such critical parameters are large frequency tuning range, low power consumption, and low phase noise. All these parameters are primarily determined by the passives used in VCO circuits (see also the AMS Section in the *System Drivers Chapter*).

Integrating passives into RF chips is progressing in this era of system on chip (SoC) in order to realize high-performance low-cost RF CMOS technology, especially for some consumer electronics. When incorporating passives into a standard CMOS process, there are typically some additional photolithography and processing steps needed. Moreover, new materials may be required for better passive performance. Therefore, there are always tradeoffs between processing cost and device performance. Nevertheless, this is quite a complex and application-dependent topic, because capacitors and inductors usually occupy much more Si area than active devices. Consequently, another optimization scheme should be implementing extra process steps or adding process complexity to increase the unit capacitance for smaller die size. Long-term challenges for passive elements will include the need to integrate new materials in a cost-effective manner to realize compact high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap.

EMBEDDED PASSIVES

Packaging and assembly are considerable challenges for embedded passive. Two other well-known are testing and tuning. The requirements for embedded components are similar to those of surface mount components. However, the process technology of the embedded components, the I/O interconnects and the process compatibility differ from those of surface mount components. Embedded passives technology often involves additional material such as high-κ dielectric for capacitors, resistive film or paste for resistors, and high-permeability material for inductors. The different material may also require special processing. The large variation in embedded passives options increase complexity and cost. In general, IPDs based on silicon substrate offer smallest size and highest precision. However, these devices also have higher substrate loss and higher cost that are the disadvantages for this method. Ceramic substrates usually provide low loss and high Q passives, but the variations and tolerances during the sintering process will cause mismatch and degrade circuit performance. Organic substrates such as PCB are the most cost effective and support a variety of different applications, but the loss, tolerance, and size make this approach still rarely used in mass production. The lack of accurate models, especially for process tolerance and parasitic effects, and computer assisted design (CAD) tools also are challenges to using these devices in RF and AMS circuits.

POWER AMPLIFIERS

HANDSET PA

The major challenge facing power amplifier devices and modules for portable communication devices is the need to increase their functionality in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity requirements at the same or lower cost. The consumer expects increasing portable device functionality without a substantial increase in portable device cost. Meeting these conflicting requirements is the biggest challenge facing the development of future PA modules. Some examples of recent customer requirements that impact technology choices are listed below.

For linear PAs used for such protocols as code division multiple access (CDMA), personal communications services (PCS), wideband CDMA (WCDMA) and the like, there is increasing focus on mid-power (16 dBm) efficiency. There are two popular solutions to this problem currently. The first is using a balanced architecture (no new process development required). The second is including on-chip switching to by-pass one or all of the PA stages (this drives the integration of RF FETs and HBTs on the same die).

Load-insensitivity is another challenging requirement. Phone manufacturers are asking PA vendors to develop modules that are not sensitive to the load that the PA module sees. Previously, the major requirement was that the PA should be robust enough to withstand the voltage standing wave ratio (VSWR) withstood the VSWR when the isolator was removed. The current challenge is to meet performance specifications (e.g., noise figure, linearity, and PAE) over the same VSWR condition. The responses to this challenge will be varied and place differing demands on the selected technology.

Increasingly sophisticated bias circuits are being requested by PA users. Some examples are enable pins/mode control, temperature compensation circuitry, automatic bias control (PA senses power and resets bias based on this – this may require integration of power detector/coupler into PA module), and circuits that do not require a reference supply voltage. This last request is challenging to meet using only npn transistors and the ability to meet these demands is the driver for BiFET integration where the FET is required to be a high quality analog FET. Continued emphasis on this area also makes BiCMOS, although it has RF shortcomings, an attractive alternative to GaAs HBT.

Enhanced data rates for global system for mobile (GSM) (EDGE) PAs are typically integrated with GSM PAs, so there will be some convergence of the needs of linear PA, and saturated PAs as PA designers must now provide linear operation as well.

Another challenge that is presented to all handset PAs is the migration of battery technology. The end-of-life battery voltage will likely decrease in the near future, presenting a major technology and design challenge to PA vendors. This has huge implications for what has to happen at a system level. The PA will still need to work on a 4-5 volt charger, but also to lower voltage (like 2.4 V) – increasing the range of operation. If the required output power remains unchanged, then some form of load-line switching will need to be employed (and whether or not this is supplied by the phone manufacturer or the PA supplier will impact the choice of technology used). Another consequence will be that the transistors used in the power amplifier will be required to operate at a much higher current density to meet the same requirements and this will also have ramifications for which technologies can be used.

The incredible cost sensitivity and the fact that PAs tend to use a system-in-a-package (SiP) approach make the technology trends difficult to forecast.

BASE STATION POWER AMPLIFIERS

One of the biggest challenges facing the base station semiconductor technologies is the continual need for performance enhancements in the face of continual product price pressure. LDMOS technology which owns over 95% of the base station market has seen components cost drop from over a dollar per Watt to less 30 cents per Watt. In addition the price press will continue dropping the component cost to 10 cents per Watt in 2013. The move to plastic packaging has enabled this component cost reduction that puts more pressure on LDMOS chip cost because now it is a larger fraction of the component cost than when ceramic packaging was used.

The biggest technical challenge for LDMOS base station technology is the move to higher frequencies while at the same time maintaining or even increasing device efficiency. Over the last seven years LDMOS performance has increased steadily through reduction in gate length from 0.8µm in 2000 to 0.4µm in 2006 and improved device design. LDMOS application space has expanded to include 3.7 GHz. This frequency range use to be dominated by GaAs, but no more. The challenge for LDMOS is to continue this push to higher frequencies.

Improving amplifier efficiency is also a challenge for base station technology. This is primarily being addressed by exploring more efficient amplifier designs: Doherty, drain modulation, and higher efficiency classes of operation (Class D, Class E, and Class S). However these approaches must continue to meet the stringent linearity performance requirements and cannot substantially increase system cost. Adaptive pre-distortion designs where a portion of the output signal is feed back to the input will help meet the linearity requirements. The adaptive behavior of the pre-distorter also mitigates issues with thermal time constants and device performance drift over time. GaN may offer advantages over LDMOS in these more highly efficient amplifier designs.

Finally, there is a move in the LDMOS technology space towards higher levels of integration. This is complicated somewhat by the fact that LDMOS technology typically includes a heavily doped acceptor (P^+ doped) substrate. The doped substrate limits the frequency performance of passive components integrated into the standard LDMOS wafer. Several approaches are being investigated to mitigate the deleterious effect of the commonly used doped substrate.

MILLIMETER WAVE

Compound semiconductor technologies have a number of similarities with silicon technologies and yet in many ways are distinctly different. While III-Vs have benefited from the advances in manufacturing equipment and chemistries, the development of these tools and chemicals is focused on the silicon industry and is not necessarily optimum for compound semiconductor processing. Additionally, the need to thin wafers to 0.002-inch thickness for thermal dissipation for some power devices and the more fragile nature of GaAs and InP make wafer breakage a yield issue that must be addressed.

Six-inch diameter semi-insulating GaAs wafers are routinely available and are becoming the *de facto* standard, although some foundries are still at four-inch. The move to larger diameter substrates will be driven not only by economies of scale and chip cost but also by equipment availability. GaAs tends to be two generations behind Si in wafer size, with InP and SiC one and two generations, respectively, behind GaAs. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from the advances in processing equipment. This continued pace in substrate size is particularly true for SiC, which still suffers from high defect density, although that is improving. Today there is no production source of semi-insulating GaN substrates. Most GaN device epitaxy is done on SiC substrates. Significant technology breakthroughs will be required before GaN becomes commercially viable. Advances in high resistivity Si substrates must also be addressed as SiGe HBT and RF CMOS push toward the millimeter wave spectrum.

Device challenges, some of which are unique to III-Vs include the following:

- The requirement for substrate vias for low inductance grounds in microstrip millimeter wave circuits;
- Techniques for heat removal including wafer thinning and for low parasitic air-bridge interconnects;
- High breakdown voltages for power devices; and 4) non-native oxide passivation.

While these issues have been mostly solved for GaAs, they need to be applied successfully to the emerging III-V technologies of InP, SiC, and GaN. One of the critical challenges for high power III-V devices is thermal dissipation. This challenge is especially true for high-power density devices such as GaN.

TECHNOLOGY REQUIREMENTS

Major changes in the technology requirements tables for each of the five sections in this chapter for the 2007 ITRS are detailed in each section below.

RF AND AMS CMOS

- Continue linkage to Low Standby Power (LSTP) CMOS Roadmap with one-year lag with minor adjustments to F_t /F_{max} to be more consistent with published trends.
- No update for Precision Analog CMOS roadmap
- Added CMOS requirements for millimeter wave, link to High Performance CMOS Roadmap with two-year lag. Added RF parameters: F_t /F_{max} and Noise Figure (NF) at 24GHz and 60GHz

The trends of the CMOS roadmap to support higher integration and performance levels for logic with mixed-signal circuitry have continued. Continued focus on 1/f noise, passive component density, and device matching is imperative to satisfy the increasing demands on power and area efficiency. Emerging issues from this increased integration level are analog device modeling, protection against electrostatic discharge and optimization of physical design to minimize parasitic impedances.

Performance and cost considerations will continue to drive modularity of process features in order to adapt the technology to specific SoC architectures. However, the more stringent mixed-signal transistor requirements may force the addition of process complexity to achieve integration goals. CMOS technology is gaining importance in the field of mixed-signal at the cost of bipolar and Si or SiGe-based BiCMOS processes. Technology requirements today are driven by the need for lower power consumption, lower noise, and lower cost in RF transceivers. Additional technology requirements will also be driven by the need to enable reconfiguring the RF transceiver in a software-defined radio and to enable higher level synthesis in RF transceivers (refer to the *More-that-Moore* discussion below).

Table RFAMS1a RF and Analog Mixed-Signal CMOS Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*
Performance RF/Analog [1]									
Supply voltage (V) [2]	**1.2**	**1.1**	**1.1**	**1**	**1**	**1**	**1**	**0.95**	**0.85**
T_{ox} (nm) [2]	**2**	**1.9**	**1.6**	**1.5**	**1.4**	**1.3**	**1.2**	**1.1**	**1.2**
Gate Length (nm) [2]	**53**	**45**	**37**	**32**	**28**	**25**	**22**	**20**	**18**
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	**32**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	**160**	**140**	**100**	**90**	**80**	**70**	**60**	**50**	**60**
σ V_{th} matching ($mV \cdot \mu m$) [5]	**6**	**6**	**5**	**5**	**5**	**5**	**5**	**5**	**5**
I_{ds} ($\mu A/\mu m$) [6]	**13**	**11**	**9**	**8**	**7**	**6**	**6**	**5**	**4**
Peak F_t (GHz) [7]	**170**	**200**	**240**	**280**	**320**	**360**	**400**	**440**	**490**
Peak F_{max} (GHz) [8]	**200**	**240**	**290**	**340**	**390**	**440**	**510**	**560**	**630**
NF_{min} (dB) [9]	**0.25**	**0.22**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Precision Analog/RF Driver [1]									
Supply voltage (V)	**2.5**	**2.5**	**2.5**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**
T_{ox} (nm) [10]	**5**	**5**	**5**	**3**	**3**	**3**	**3**	**3**	**3**
Gate Length (nm) [10]	**250**	**250**	**250**	**180**	**180**	**180**	**180**	**180**	**180**
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$ [11]	**220**	**220**	**220**	**160**	**160**	**160**	**160**	**160**	**160**
1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$) [4]	**500**	**500**	**500**	**180**	**180**	**180**	**180**	**180**	**180**
σ V_{th} matching ($mV \cdot \mu m$) [5]	**9**	**9**	**9**	**6**	**6**	**6**	**6**	**6**	**6**
Peak F_t (GHz) [7]	**40**	**40**	**40**	**50**	**50**	**50**	**50**	**50**	**50**
Peak F_{max} (GHz) [8]	**70**	**70**	**70**	**90**	**90**	**90**	**90**	**90**	**90**
									switch to DG device
CMOS NFET [1 HP CMOS lag 2 yrs]	-								
V_{dd}: Power Supply Voltage (V) [13]	**1.1**	**1.1**	**1.1**	**1**	**1**	**1**	**0.95**	**0.9**	**0.9**
EOT: Equivalent Oxide Thickness (Å) [13]	**12**	**11**	**11**	**9**	**7.5**	**6.5**	**5.5**	**5**	**6**
L_g: Physical L_{gate} for High Performance logic (nm) [13]	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
Peak F_t (GHz) [7]	**280**	**320**	**360**	**400**	**440**	**490**	**550**	**630**	**670**
Peak F_{max} (GHz) [8]	**340**	**390**	**440**	**510**	**560**	**630**	**710**	**820**	**880**
NF_{min} (dB) at 24GHz[14]	**2**	**1.8**	**1.6**	**1.4**	**1.3**	**1.2**	**1.1**	**1**	**0.9**
NF_{min} (dB) at 60GHz[14]	**5.1**	**4.5**	**4.0**	**3.6**	**3.3**	**3.0**	**2.7**	**2.4**	**2.3**
									switch to DG device

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

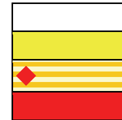


Table RFAMS1b RF and Analog Mixed-Signal CMOS Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Performance RF/Analog [1]							
Supply voltage (V) [2]	0.8	0.8	0.8	0.8	0.75	0.75	0.7
T_{ox} (nm) [2]	1.1	1.1	1	1	0.9	0.9	0.8
Gate Length (nm) [2]	16	14	13	12	11	10	10
g_m/g_{ds} at $5\cdot L_{min\text{-}digital}$ [3]	30	30	30	30	30	30	30
1/f-noise (µV²·µm²/Hz) [4]	50	50	40	40	30	30	30
σ V_{th} matching (mV·µm) [5]	4	4	4	4	3	4	5
I_{ds} (µA/µm) [6]	4	3	3	3	2	2	2
Peak F_t (GHz) [7]	550	630	670	730	790	870	870
Peak F_{max} (GHz) [8]	710	820	880	960	1050	1160	1160
NF_{min} (dB) [9]	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
Precision Analog/RF Driver [1]							
Supply voltage (V)	1.8	1.8	1.8	1.5	1.5	1.5	1.5
T_{ox} (nm) [10]	3	3	3	2.6	2.6	2.6	2.6
Gate Length (nm) [10]	180	180	180	130	130	130	130
g_m/g_{ds} at $10\cdot L_{min\text{-}digital}$ [11]	160	160	160	110	110	110	110
1/f Noise (µV²·µm²/Hz) [4]	180	180	180	135	135	135	135
σ V_{th} matching (mV·µm) [5]	6	6	6	5	5	5	5
Peak F_t (GHz) [7]	50	50	50	70	70	70	70
Peak F_{max} (GHz) [8]	90	90	90	120	120	120	120
	switch to DG device						
CMOS NFET [1 HP CMOS lag 2 yrs]							
V_{dd}: Power Supply Voltage (V) [13]	0.9	0.8	0.8	0.7	0.7	0.7	0.65
EOT: Equivalent Oxide Thickness (Å) [13]	6	6	5.5	5.5	5.5	5	5
L_g: Physical L_{gate} for High Performance logic (nm) [13]	11	10	9	8	7	6	5.5
Peak F_t (GHz) [7]	790	870	960	1080	1220	1420	1550
Peak F_{max} (GHz) [8]	1050	1160	1300	1470	1690	1990	2180
NF_{min} (dB) at 24GHz[14]	0.8	0.7	0.6	0.6	0.5	0.4	0.4
NF_{min} (dB) at 60GHz[14]	2.0	1.8	1.6	1.4	1.2	1.0	0.9
	switch to DG device						

Notes for Table RFAMS1a and b:

[1] Year of first digital product for a given technology generation as given in overall roadmap technology characteristics (ORTC) tables. Lithographic drivers for key technologies are indicated. Year of first RF and mixed-signal product at the same technology lag the low-standby power roadmap by one year. Beyond Planar CMOS, performance RF/Analog CMOS reflect DG CMOS, Precision Analog/RF driver device color change to yellow reflecting uncertainty on device integration. The supply voltage, Tox, Gate Length and Ids, Ft, Fmax color codes reflected the low-standby power roadmap. Any discrepancies, please refer to those of low-standby power roadmap.

[2] Nominal supply voltage, V_{dd}, SiO_2 equivalent physical CMOS gate dielectric thickness, T_{ox}, and minimum nominal gate length from low-standby power digital roadmap. For simplicity, only the Extended planar and DG technology options were used and the value was interpolated in the transition years.

[3] Measure for the low frequency amplification of a 5X minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$. The minimum value of 30 exceeds the projected technology capability with continued scaling for the standard logic device. When this occurs, the standard logic device should be replaced with an unique device designed for specifically for superior gain.

[4] Gate-referred 1/f noise spectral density, at a frequency of 1 Hz, normalized to an active gate area of 1 µm^2. Operation point taken at 200 mV above the threshold voltage, Vth, and at Vds = Vdd/2.

[5] Matching specification for the NMOS transistor's threshold voltage, assuming "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity, e.g. by using dummy structures, are required. Statistical dopant fluctuations start limiting further improvement with SiO_2. Matching behavior of high-κ gate dielectrics very may be problematic. This parameter determines the lower boundary for the size of transistor in a mixed-signal circuit for a given accuracy and will limit dimensional, performance, and DC power consumption.

[6] I_{ds} for F_t of 50 GHz for a minimum transistor length. F_t of 50 GHz is chosen for being 10X the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[7] Peak Ft measured from H21 extrapolated from 40 GHz with a 20 dB/dec slope.

[8] Peak F_{max} measured from unilateral gain extrapolated from 40 GHz with a 20 dB/dec slope.

[9] This is the minimum transistor noise figure at 5GHz. 0.2dB represents the limitation of commercially available measurement equipment.

[10] This device is required to achieve direct modulation of the PA for applications from 2 to5 GHz and to support precision analog applications. Device with higher voltage tolerance are typically integrated with logic devices to support input-output interfaces. With continued scaling of logic devices alternate device structures may be required to support the required specifications.

[11] Measure for the low frequency amplification of a 10× minimum length, low-standby power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 200 mV above the threshold voltage, V_{th}, and at $V_{ds} = V_{dd}/2$.

[12] Nominal supply voltage, V_{dd}, SiO_2 equivalent electrical CMOS gate dielectric thickness, EOTelec and minimum nominal gate length from high-performance digital roadmap. For simplicity, only the Extended planar and DG technology options were used and the value was interpolated in the transition years.

[13] Nominal supply voltage, V_{dd}, SiO_2 equivalent physical CMOS gate dielectric thickness, T_{ox}, and minimum nominal gate length from high performance digital roadmap. For simplicity, only the Extended planar and DG technology options were used and the value was interpolated in the transition years.

[14] This is the minimum transistor noise figure at 24 and 60GHz.

RF AND AMS BIPOLAR DEVICES

- Continued table format with three separate bipolar devices, using high-speed and PA devices as drivers for the roadmap with a high voltage device derived from the high-speed device by a collector change.
    - High-speed NPN is driven by requirements for millimeter wave applications
    - PA NPN is driven by requirements for power amplifier applications
    - High-voltage NPN (was "RF NPN" in 2006 table) is the "typical" bipolar device used for 0.8 to 10GHz applications and is derived from the high-speed device by a collector change to increase breakdown voltage while sacrificing F_t /F_{max}.
- Reduced F_t for the high-speed device by delaying introduction of the 300 GHz device by one year. Also adjusted F_{max}, J_c, and BV_{ceo} accordingly and added noise figure at 60 GHz.
- Revised PA device parameters and aligned with PA battery voltage

Major changes to the roadmap relative to the 2006 version were driven by the change in focus toward millimeter wave and power amplifiers as drivers of the bipolar roadmap. Millimeter-wave applications will continue to drive improvements in F_t and F_{max} of the bipolar transistor while PA applications will drive an improved tradeoff between F_t /F_{max} and breakdown voltage. With this new focus, a 60 GHz noise figure was added to the high-speed device and its F_t /F_{max} trajectory was adjusted to better reflect recent data.

Table RFAMS2a RF and Analog Mixed-Signal Bipolar Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
General Analog NPN Parameters									
Emitter width (nm) (HS and HV NPN)	**130**	**120**	**100**	**100**	**100**	**90**	**90**	**90**	**80**
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	**2**	**2**	**2**	**1.5**	**1.5**	**1.5**	**1**	**1**	**1**
σ current matching (%·µm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
High Speed (HS) NPN (Common to mmWave Table)									
Peak F_t (GHz) [V_{cb}=1V]	**250**	**275**	**300**	**320**	**340**	**360**	**380**	**395**	**415**
Peak F_{max} (GHz)	**280**	**305**	**330**	**350**	**370**	**390**	**410**	**425**	**445**
Nfmin (dB) at 60GHz	**3.0**	**2.5**	**2.2**	**1.9**	**1.7**	**1.5**	**1.4**	**1.3**	**1.2**
BVceo (V)	**1.8**	**1.7**	**1.65**	**1.6**	**1.55**	**1.5**	**1.45**	**1.4**	**1.35**
J_c at Peak F_t (mA/µm^2)	**13**	**15**	**17**	**18**	**19**	**21**	**22**	**23**	**24**
High Voltage (HV) NPN									
Peak F_t (GHz) [V_{bc}=1V]	**90**	**90**	**100**	**100**	**110**	**110**	**120**	**120**	**130**
Peak F_{max} (GHz)	**170**	**180**	**190**	**200**	**210**	**220**	**230**	**240**	**250**
BV_{ceo}	**3.1**	**3.1**	**2.9**	**2.9**	**2.8**	**2.8**	**2.6**	**2.6**	**2.5**
NF_{min} (dB) at 5GHz	**0.26**	**0.24**	**0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
I_c (µA/µm) at 50GHz F_t	**28**	**22**	**16**	**15**	**14**	**13**	**12**	**11**	**10**
Power Amplifier (PA) NPN (Common to PA Table)									
Peak F_t (GHz) [V_{bc}=1V]	**35**	**35**	**40**	**40**	**40**	**40**	**40**	**40**	**40**
Peak F_{max} (GHz)	**60**	**60**	**80**	**80**	**80**	**80**	**80**	**80**	**80**
Bvceo (V)	**8.5**	**8.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**
BV_{cbo} (V)	**18**	**18**	**16**	**16**	**16**	**16**	**16**	**16**	**16**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

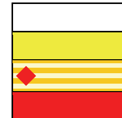


Table RFAMS2b RF and Analog Mixed-Signal Bipolar Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
General Analog NPN Parameters							
Emitter width (nm) (HS and HV NPN)	**80**	**80**	**70**	**70**	**70**	**70**	**70**
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	**1**	**1**	**1**	**1**	**1**	**1**	**1**
σ current matching (%·µm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
High Speed (HS) NPN (Common to mmWave Table)							
Peak F_t (GHz) [V_{cb}=1V]	**430**	**445**	**455**	**470**	**480**	**490**	**500**
Peak F_{max} (GHz)	**460**	**475**	**485**	**500**	**510**	**520**	**530**
Nfmin (dB) at 60GHz	**1.1**	**1.0**	**1.0**	**0.9**	**0.9**	**0.9**	**0.8**
BVceo (V)	**1.35**	**1.3**	**1.3**	**1.3**	**1.3**	**1.25**	**1.25**
J_c at Peak F_t (mA/µm^2)	**25**	**26**	**27**	**28**	**29**	**29**	**30**
High Voltage (HV) NPN							
Peak F_t (GHz) [V_{bc}=1V]	**130**	**140**	**140**	**150**	**150**	**160**	**160**
Peak F_{max} (GHz)	**260**	**270**	**280**	**290**	**300**	**310**	**320**
BV_{ceo}	**2.5**	**2.4**	**2.4**	**2.4**	**2.4**	**2.3**	**2.3**
NF_{min} (dB) at 5GHz	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
I_c (µA/µm) at 50GHz F_t	**9**	**8**	**7**	**6**	**5**	**5**	**5**
Power Amplifier (PA) NPN (Common to PA Table)							
Peak F_t (GHz) [V_{bc}=1V]	**40**	**40**	**40**	**40**	**40**	**40**	**40**
Peak F_{max} (GHz)	**80**	**80**	**80**	**80**	**80**	**80**	**80**
Bvceo (V)	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**	**7.5**
BV_{cbo} (V)	**16**	**16**	**16**	**16**	**16**	**16**	**16**

ON-CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

ON-CHIP PASSIVES

- Continue table format with three applications: Analog, RF, and Power Amplifier
- Devices include: Capacitors, Resistors, Inductors, Varactors
- Add Metal-Oxide-Metal (MOM) interdigitated capacitor to RF capacitor

Analog MOS Capacitors for decoupling are based on the roadmap specifications for the analog precision device in the CMOS tables. As the gate oxide thickness is being scaled for this MOS transistor, capacitor density increases but leakage current becomes an issue. In the year 2010, a gate oxide thickness of 3 nm is required, but this results in unacceptable high leakage current. This might require the use of high-κ dielectrics in the MOS capacitors to reduce the leakage current to acceptable levels.

Resistors are used in all analog and mixed signal circuit blocks. Highly doped p-type polysilicon resistors are preferred in most cases for mixed signal and analog applications due to their good matching, low parasitic capacitance to the substrate and excellent temperature coefficient. These resistors consist of gate polysilicon doped with a high dose boron implant, which is normally the p-channel FET (PFET) source and drain (SD) implants. A 200–300 Ohm/square resistor is ideal for these applications. As CMOS is scaled further, the associated shallow and lower dose SD implants result in resistances that exceed 500 Ohm/square for these devices. This may require an additional mask for analog applications in the future and lower tolerance devices with smaller resistances. These devices have an excellent temperature coefficient that is less than 100 ppm/C.

A thin-film back-end of line (BEOL) resistor has several attractive features such as low tolerance, low parasitics, and the ability to make design changes with short lead times. These are excellent for use in RF and analog applications, especially in I/O circuits and current biasing. A typical thin film resistor is comprised of TaN, a common material in the copper BEOL process. It is integrated above Metal 1 or other upper metallization levels and contacted with metal vias. These devices have excellent matching and are attractive for analog applications.

The key parameters for metal-insulator-metal (MIM) capacitors for RF applications are capacitance density, voltage linearity, leakage, matching and Q factor. Higher capacitance density is required for capacitor area scaling. The matching tolerances become smaller as the capacitance area scales down. The capacitance density value in the table indicates the value for one capacitor and does not include the stacking of two capacitors on top each other that is sometimes done and requires doubling the mask levels and process steps. The value also is for Cu back-end process that poses significantly more challenges compared to Al back-end in terms of integration and reliability.

Metal-Oxide-Metal (MOM) capacitors have the same key parameters as the MIM capacitors. The capacitance density of the MOM capacitors is determined by the width and space of multi level metal systems in the backend, and cannot be optimized independently of the back-end-system. Because the dimension control (space in particular) of the back-end-system is not as good as the control of the thin film thickness of the MIM capacitor, the matching of the MOM capacitors is usually significantly worse than that of the MIM capacitors.

The need for high performance on-chip monolithic spiral and multi-level spiral inductors in RF technologies recently has become increasingly important due to the technology and integration requirements of high functionality and low cost RF circuit applications. The typical interconnect scaling associated with digital circuit technologies, that is, BEOL scaling, is inconsistent with the need to keep series resistive losses low for high quality inductors. Additionally, minimizing substrate losses due to eddy currents and capacitive coupling is desired to increase Q. Integrating the inductors in the last, thick-metal levels of the BEOL and using large vias to provide a thick dielectric between the inductor and substrate help reduce these effects. Thick low-resistance metal wiring is needed for high Q applications such as in VCO circuits where high Q inductors are needed to reduce phase noise. Thick aluminum or copper inductors can be used to achieve peak Q performance of 25–30 for a 1 nH inductor at 3 GHz – 5 GHz.

Accumulation and depletion mode MOS varactors offer attractive tuning ranges and Q-factors. The requirements listed in the table are for MOS varactors based on gate oxide for performance RF/analog transistors. They are updated with respect to the tuning range cited in the previous 2006 ITRS Update because higher tuning ranges have been achieved with the CMOS scaling. The continuous improvement in inductor Q-factors requires the varactor Q-factor to further increase, otherwise the varactor Q-factor becomes the limiting factor for VCO performance improvements. It is not clear to what extent varactors with additional gate length reductions can achieve the required Q-factors in the range of 50 and higher and how the varactor characteristics will be affected by the introduction of high-κ dielectrics.

Table RFAMS3a On-Chip Passives Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Analog									
MOS Capacitor									
Density (fF/μm^2) [1]	**7**	**7**	**7**	**11**	**11**	**11**	**11**	**11**	**11**
Leakage (A/cm^2) [8]	**<1e-9**	**<1e-9**	**<1e-9**	**<2e-6**	**<2e-6**	**<2e-6**	**<2e-6**	**<2e-6**	**<2e-6**
Resistor									
Thin Film BEOL									
Parasitic capacitance (fF/μm^2)	**0.03**	**0.03**	**0.05**	**0.05**	**0.05**	**0.05**	**0.08**	**0.08**	**0.08**
Temp. linearity (ppm/ºC)	**<100**	**<100**	**40-80**	**40-80**	**40-80**	**40-80**	**30**	**30**	**30**
1σ Matching (% μm)	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.15**	**0.1**	**0.1**	**0.1**
Sheet resistance, Rs (Ohm/sq)	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**
P+ Polysilicon									
Parasitic capacitance (fF/μm^2)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
Temp. linearity (ppm/ºC)	**<100**	**<100**	**40-80**	**40-80**	**40-80**	**40-80**	**30**	**30**	**30**
1σ Matching (% μm)	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1.7**	**1**	**1**	**1**
Sheet resistance, Rs (Ohm/sq)	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**
RF									
Metal-Insulator-Metal Capacitor									
Density (fF/μm^2) [2]	**2**	**4**	**4**	**5**	**5**	**5**	**7**	**7**	**7**
Voltage linearity (ppm/V^2)	**<100**	**<100**	**<100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**
Leakage (A/cm^2) [9]	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**
σ Matching (%·μm)	**0.5**	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**
Q (5 GHz for 1pF)	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**
MOM Capacitor									
Density (fF/μm^2)	**3.7**	**5.0**	**5.3**	**6.2**	**7.0**	**6.5**	**7.5**	**8.6**	**9.9**
Voltage linearity (ppm/V^2)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
s Matching (% for 1pF)	**<0.15**	**<0.15**	**<0.15**	**<0.15**	**<0.15**	**<0.15**	**<0.1**	**<0.1**	**<0.1**
Inductor									
Q (5 GHz, 1nH) [3]	**29**	**30**	**32**	**34**	**36**	**38**	**40**	**42**	**44**
MOS Varactor									
Tuning Range [4]	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**
Q (5 GHz, 0 V)	**35**	**35**	**40**	**40**	**45**	**45**	**50**	**50**	**55**
PA									
PA III-V Passives									
Inductors Q (1GHz, 5nH) [5]	**15**	**25**	**25**	**25**	**25**	**30**	**30**	**30**	**30**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**1.2**	**1.2**	**1.2**	**2**	**2**	**2**	**2**	**2**	**2**
PA Silicon/SiGe Passives									
Inductors Q (1GHz, 5nH) [5]	**10**	**14**	**14**	**14**	**14**	**18**	**18**	**18**	**18**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**2**	**4**	**4**	**5**	**5**	**5**	**7**	**7**	**7**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

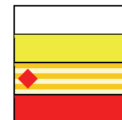


Table RFAMS3b On-Chip Passives Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Analog							
MOS Capacitor							
Density (fF/μm^2) [1]	**11**	**11**	**11**	**13**	**13**	**13**	**13**
Leakage (A/cm^2) [8]	**<2e-6**	**<2e-6**	**<2e-6**	**<2e-5**	**<2e-5**	**<2e-5**	**<2e-5**
Resistor							
Thin Film BEOL							
Parasitic capacitance (fF/μm^2)	**0.08**	**0.08**	**0.08**	**0.08**	**0.08**	**0.08**	**0.08**
Temp. linearity (ppm/ºC)	**30**	**30**	**30**	**20**	**20**	**20**	**20**
1σ Matching (% μm)	**0.1**	**0.1**	**0.1**	**0.08**	**0.08**	**0.08**	**0.08**
Sheet resistance, Rs (Ohm/sq)	**50**	**50**	**50**	**50**	**50**	**50**	**50**
P+ Polysilicon							
Parasitic capacitance (fF/μm^2)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
Temp. linearity (ppm/ºC)	**30**	**30**	**30**	**30**	**30**	**20**	**20**
1σ Matching (% μm)	**1**	**1**	**1**	**0.08**	**0.08**	**0.08**	**0.08**
Sheet resistance, Rs (Ohm/sq)	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**	**200–300**
RF							
Metal-Insulator-Metal Capacitor							
Density (fF/μm^2) [2]	**10**	**10**	**10**	**12**	**12**	**12**	**12**
Voltage linearity (ppm/V^2)	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**
Leakage (A/cm^2) [9]	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**	**<1e-8**
σ Matching (%·μm)	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
Q (5 GHz for 1pF)	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**
MOM Capacitor							
Density (fF/μm^2)	**11.4**	**13.1**	**15.1**	**17.4**	**20.0**	**23**	**26.4**
Voltage linearity (ppm/V^2)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
s Matching (% for 1pF)	**<0.1**	**<0.1**	**<0.1**	**<0.08**	**<0.08**	**<0.08**	**<0.08**
Inductor							
Q (5 GHz, 1nH) [3]	**46**	**48**	**50**	**52**	**54**	**56**	**58**
MOS Varactor							
Tuning Range [4]	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**	**>5.5**
Q (5 GHz, 0 V)	**55**	**60**	**60**	**65**	**65**	**70**	**70**
PA							
PA III-V Passives							
Inductors Q (1GHz, 5nH) [5]	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**2**	**2**	**2**	**2**	**2**	**2**	**2**
PA Silicon/SiGe Passives							
Inductors Q (1GHz, 5nH) [5]	**18**	**18**	**18**	**18**	**18**	**18**	**18**
Capacitor Q [6]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
RF capacitor density (fF/μm^2) [7]	**10**	**10**	**10**	**10**	**12**	**12**	**12**

Notes for Table RFAMS3a and b:

[1] This capacitance density corresponds to the highest end of the gate oxide thickness for precision analog device in the CMOS table.

[2] No stacking (two capacitors on top of each other) is included. Coloring reflected MIM capacitor meeting all requirements including density, voltage linearity, leakage and matching on copper metallization.

[3] Q at 5 GHz for a single-ended 1nH inductor with a dedicated thick metal (analog metal).

[4] Defined as Cmax/Cmin in C-V curve of the varactor. Varactor align with performance RF device in the CMOS table.

[5] Inductor Q-quality factor of a 5nH inductor at 1 GHz achievable with the technology with a metallization suitable for handling the power requirements of the PA.

[6] Capacitor Q-quality factor of a 10 pF capacitor at 1 GHz achievable with the technology. Capacitor breakdown voltage must be rated for appropriate power amplification function.

[7] RF capacitor density-capacitor used for all other functions (matching, harmonic filtering, coupling, etc.). Capacitor must have adequate breakdown for the given application. No stacking.

[8] Leakage current is defined at room temperature and for the highest end of the supply voltage range and thickness end of the gate oxide thickness for precision analog device in the CMOS table.

[9] Leakage current is defined at room temperature and for the highest end of the supply voltage range for precision analog device in the CMOS table.

EMBEDDED PASSIVES

- Three device elements (Resistors, Capacitors and Inductors) for both organic and inorganic package substrate material
- Requirements for Density, Tolerance, Temperature linearity, Resonance frequency and Breakdown voltage.

Embedded passives using buried discrete components need to move to the Roll-to-Roll manufacturing process in the next three years. As to process control, especially for organic PCB, the untrimmed total tolerance including material and process need to be below 10% for capacitor and resistor and 5% for inductor. Testing and tuning methodologies during processing are available but need to be standardized. Though not specifically listed on the requirement tables, water absorption and reliability of organic printed circuit boards are also important parameters to consider.

Resistors will be required to support sheet resistance ranges from 100 Ohm/square to 1K Ohm/square and will be extended to higher and lower sheet resistance values for both the thick and thin film processes. Temperature linearity is a key parameter for embedded resistors and must be less than 300ppm/ºC.

Precise control of capacitance lower than 3pF is required for matching circuits. The parallel plate Metal-Insulator-Metal (MIM) structure of embedded capacitors will be affected by the inter-layer misalignment especially as the capacitor area shrinks. High-κ material is needed for increased capacitance density. For organic high-κ material, the dielectric constant of about 50 is currently used in production, dielectric constant as high as 100 will be needed for the future. As application frequency increases, the capacitor Q factor and self resonance frequency (SRF) will limit the high-κ MIM capacitor performance. Smaller electrode sizes or special structures that minimize the parasitics of embedded capacitors will be needed to improve SRF performance.

The key advantage for embedded inductor is high Q factor >40 and low process cost. The high-permeability material will become a key technology to increase the inductance density. Also, since the size of embedded inductors is relatively large, the coupled parasitic capacitance between wires will limit the SRF. Fine line process with good process tolerance or special structure will be needed for the embedded inductors especially as application frequency increases.

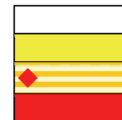
Table RFAMS4a Embedded Passives Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	***2014***	***2015***
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	***28***	***25***
Resistor [1]									
Max Sheet resistance, Rs (Ohm/sq)	1K	1K	1K	10K	100K	100K	500K	500K	500K
Tolerance (%) [2]	<10%	<10%	<5%	<10%	<10%	<5%	<10%	<10%	<5%
Temp. linearity (ppm/ºC)	<500	<300	<300	<500	<300	<300	<500	<300	<300
Min Sheet resistance, Rs (Ohm/sq)	100	100	100	100	10	10	10	10	5
Tolerance (%) [2]	<10%	<5%	<3%	<1%	<10%	<5%	<3%	<1%	<10%
Temp. linearity (ppm/ºC)	<300	<200	<200	<200	<300	<200	<200	<200	<300
Capacitor [3]									
Density (nF/cm²)	>2	>2	>5	>5	>5	>5	>10	>10	>10
Tolerance (%) [2]	<10%	<7%	<10%	<7%	<7%	<5%	<10%	<7%	<5%
TCC (ppm)	<500	<300	<500	<400	<400	<300	<500	<300	<300
Breakdown Voltage (V)	>500V	>1KV	>300V	>500V	>700V	>1KV	>500V	>700V	>1KV
max Q [4]	>25	>30	>25	>30	>30	>30	>25	>25	>30
Self Resonance Freq (GHz) [5]	>0.5	>0.5	>0.1	>0.1	>0.2	>0.2	>0.05	>0.1	>0.1
Inductor [3]									
Density (nH/mm2)	0.4	0.4	0.8	0.8	0.8	0.8	2	2	2
Tolerance (%) [2]	<5%	<5%	<5%	<5%	<5%	<5%	<5%	<5%	<3%
max Q [6]	>40	>40	>40	>40	>40	>40	>40	>40	>40
Self Resonance Freq (GHz) [7]	>10	>10	>10	>10	>10	>10	>10	>10	>10

Table RFAMS4b Embedded Passives Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Resistor [1]							
Max Sheet resistance, Rs (Ohm/sq)	500K	500K	500K	500K	500K	500K	500K
Tolerance (%) [2]	<5%	<5%	<5%	<5%	<5%	<3%	<1%
Temp. linearity (ppm/ºC)	<300	<300	<300	<300	<300	<200	<200
Min Sheet resistance, Rs (Ohm/sq)	5	5	5	1	1	1	1
Tolerance (%) [2]	<5%	<3%	<1%	<10%	<5%	<3%	<1%
Temp. linearity (ppm/ºC)	<200	<200	<200	<300	<200	<200	<200
Capacitor [3]							
Density (nF/cm^2)	>100	>100	>100	>1000	>1000	>1000	>1000
Tolerance (%) [2]	<10%	<7%	<5%	<10%	<10%	<7%	<5%
TCC (ppm)	<300	<300	<200	<300	<200	<200	<200
Breakdown Voltage (V)	>500V	>500V	>700V	>500V	>500V	>700V	>1KV
max Q [4]	>15	>20	>25	>10	>15	>20	>25
Self Resonance Freq (GHz) [5]	>0.001	>0.005	>0.01	>0.001	>0.001	>0.001	>0.001
Inductor [3]							
Density (nH/mm^2)	2	4	4	4	4	8	8
Tolerance (%) [2]	<3%	<3%	<3%	<3%	<3%	<3%	<3%
max Q [6]	>45	>45	>45	>45	>45	>45	>45
Self Resonance Freq (GHz) [7]	>10	>10	>10	>10	>10	>10	>10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table RFAMS4a and b:
[1] For both thick and thin film process
[2] Untrimmed total tolerance including material and process
[3] For all material and process (lamination, buried, etc.)
[4] Maximum Q for 1cm^2 capacitor
[5] SRF for 1cm^2 capacitor
[6] Maximum Q for 10nH inductor
[7] SRF for 25mm^2 inductor

POWER AMPLIFIERS (0.8 GHZ–10 GHZ)

HANDSET PA

- Add end-of-life battery voltage.
- Add FET/HBT integration for integrated bias circuit design and on-chip switch integration for stage by-passing.

The trends in handset power amplifiers (PAs) respond directly to customer (phone manufacturers) demands and requirements, which are, in turn, driven by the desire to optimize the entire handset system. Optimizing the system leads to new technologies first being adopted at a power amplifier module (PAM) level that is integrated in the package. Package level integration can happen faster than new technology development for the system. However, system optimization may eventually be pushed back to the fundamental technology. Of course, since the life-span of a handset

model is approximately 18 months, time to market and lowest cost are always two of the top considerations in technology choice. There are three major trends that phone manufacturers will be driving:

1. The first is the use of battery technologies that have a lower end-of-life voltage than present systems have. This means that the PA will be have to operate over a wider voltage range. Customer expectations of what the low-end-voltage performance requirements are have not been clearly defined. The specifications for low-end-voltage performance will determine the new technologies for load-switching and voltage control. The particular system partitioning that companies select will influence whether GaAs or silicon technologies are used. In addition, other technologies that provide a switching function will be needed at the module level.
2. A second trend, for linear handset applications (CDMA, WCDMA, PCS, etc.) is the desire for greater functionality bias circuits to simplify system insertion and high mid-power efficiency at about 16 dBm. To meet these requirements, several companies have co-integrated FETs and HBTs in the same technology, similar to the BiFET process in silicon. This co-integration allows bias circuits to operate to lower reference voltages, some flexibility in system insertion, no reference voltages, and some shut-off switching function on the bias circuit – all features that customers have requested. Enabling these features and applications require a high-quality analog FET. Stage by-passing is another application that requires FET-HBT co-integration. In this case, the FET must be a higher quality RF FET because it performs a RF switching function. The integration and refinement of FET-HBT technologies will certainly continue in the next few years.
3. Finally, in the next several years, there will be an increasing trend to integrate more bands and more modes onto a PAM. One of the interesting questions is whether or not wireless-LAN will be included in this integration. This question is important since wireless-LAN PAs use predominantly Si or GaAs at 2.4 GHz and GaAs at 5.8 GHz. As these PAs need to be folded into the system, new technology requirements might arise. A greater number of bands and modes also has an impact on switch technology used for PAMs. In order to save board real estate, it is desirable to have the switch logic controller directly integrated with the switch. Such integration reduces the number of bond pads and routing traces. This makes E/D pHEMT, SOS, and SOI, attractive switch technologies in the future.

The PA passive values are also updated. The decision of product designers on where to put output matching components for the PA will drive the requirements for the passives. Currently, most PAMs are using either embedded passives or SMT components that can be selected with the best performance/cost trade-off. Placing some of these components on the PA will require MMICs to have similar precision and performance. Inductors are examples of this real world consideration where excellent Q values can already be obtained, but where the layout area required does not make sense from a cost standpoint.

Table RFAMS5a Power Amplifier Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Nominal battery voltage	**3.2**				**2.4**				
End-of-life battery voltage	**2.85**	**2.4**			**1.6**				
PA product solutions	**Radio/Baseband SIP [2]**								
PA frequency (GHz)	**0.8-6**								
III-V HBT transistor									
F_{max} (at V_{cc}) (GHz)	**45**		**55**			**65**			
BV_{CBO} (V)	**25**		**18**						
Linear efficiency (%) [1]	**52**		**55**						
Area (mm^2) [2]	**2.5**		**2.2**						
Cost/mm^2 (US$) [3]	**0.32**	**0.3**	**0.28**			**0.25**			
III-V HBT integration									
Bias Control	**MESFET**								
Power management [4]	**N/A**								
Switch [5] (by-pass)	**HEMT**								
Filter [6]	**N/A**								
III-V PHEMT transistor									
F_{max} (at V_{dd}) (GHz)	**45**		**75**						
BV_{DGO} (V)	**20**		**16**						
Linear efficiency (%) [1]	**55**		**58**						
PA Area (mm^2) [2]	**4**	**4**	**3.5**						
Cost/mm^2 (US$) [3]	**0.28**	**0.25**	**0.24**			**0.22**			**0.15**
III-V PHEMT integration									
Power management [4]	**N/A**								
Switch [7] logic integration	**E/D pHEMT**								
Filter [6]	**N/A**								
Silicon MOSFET transistor									
T_{ox} (PA) (Å) [8]	**60**		**35**						
F_{max} (at V_{dd})	**45**		**60**						
BV_{DSS} (V)	**12**		**10**						
Linear efficiency (%) [1]	**45**								
PA Area (mm^2) [2]	**6**		**4.5**						
Cost/mm^2 (US$) [3]	**0.08**		**0.06**			**0.05**			
Silicon MOSFET integration									
Power management [4]	**Yes**								
MEMS switch [5]	**NO**		**Stack**	**Above IC**		**Integrated**			
MEMS filter [6]	**Stack**		**WLP**			**Above IC**			
SiGe HBT transistor [9]									
F_{max} (GHz)	**60**		**80**						
BV_{CBO} (V)	**18**		**16**						
Linear efficiency (%) [1]	**50**		**52**						
PA Area (mm^2) [2]	**2.5**		**2.2**						
Cost/mm^2 (US$) [3]	**0.12**		**0.11**						
SiGe integration									
Power management	**Yes**								
MEMS switch [5]	**NO**		**Stack**	**Above IC**		**Integrated**			
MEMS filter [6]	**Stack**		**WLP**			**Above IC**			

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

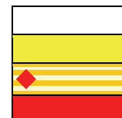


Table RFAMS5b Power Amplifier Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Nominal battery voltage	**2.4**						
End-of-life battery voltage	**1.6**						
PA product solutions	**Radio/Baseband SIP [2]**						
PA frequency (GHz)							
III-V HBT transistor							
F_{max} (at V_{cc}) (GHz)	**65**						
BV_{CBO} (V)	**18**						
Linear efficiency (%) [1]	**55**						
Area (mm^2) [2]	**2.2**	**2**					
Cost/mm^2 (US$) [3]	**0.25**						
III-V HBT integration							
Bias control	**MESFET**						
Power management [4]	**N/A**						
Switch [5] (by-pass)	**HEMT**						
Filter [6]	**N/A**						
III-V PHEMT transistor							
F_{max} (at V_{dd}) (GHz)	**75**						
BV_{DGO} (V)	**16**						
Linear efficiency (%) [1]	**58**						
PA area (mm^2) [2]	**3.5**						
Cost/mm^2 (US$) [3]	**0.15**						
III-V PHEMT integration							
Power management [4]	**N/A**						
Switch [7] logic integration	**E/D pHEMT**						
Filter [6]	**N/A**						
Silicon MOSFET transistor							
T_{ox} (PA) (Å) [8]	**35**						
F_{max} (at V_{dd})	**60**						
BV_{DSS} (V)	**10**						
Linear efficiency (%) [1]	**45**						
PA Area (mm^2) [2]	**4.5**						
Cost/mm^2 (US$) [3]	**0.05**						
Silicon MOSFET integration							
Power management [4]	**Yes**						
MEMS switch [5]	**Integrated**						
MEMS filter [6]	**Above IC**						
SiGe HBT transistor [9]							
F_{max} (GHz)	**80**						
BV_{CBO} (V)	**16**						
Linear efficiency (%) [1]	**52**						
PA area (mm^2) [2]	**2.2**	**2**					
Cost/mm^2 (US$) [3]	**0.11**						
SiGe integration							
Power management	**Yes**						
MEMS switch [5]	**Integrated**						
MEMS filter [6]	**Above IC**						

Notes for Table RFAMS5a and b:

[1] Linear efficiency—power added efficiency of the final PA stage under personal communication service (PCS) CDMA (IS-95) modulation.

[2] Area—total semiconductor area necessary for the implementation of the quad-band GSM/general packet radio service (GPRS)/ Enhanced Data rates for GSM Evolution (EDGE) PA function, including matching/filtering.

[3] Cost/mm^2—approximate commercial foundry cost of the area mentioned in [4].

[4] Power management—capability of the technology to provide RF power detection/DC power management for the PA.

[5] Switch—capability of the technology to integrate cost-effectively a stage by-pass switch into the PA active die.

[6] Filter—capability of the technology to integrate high-quality band selection filters needed for the assumed PA solution; currently performed with surface acoustic wave (SAW) filter technology.

[7] Switch Logic Integration—capability of the technology to integrate cost-effectively a control circuitry with the Tx/Rx antenna switch.

[8] T_{ox} (PA)—thickness of the MOSFET transistor in the RF power amplifier function.

[9] Ideally, the Si requirements and GaAs requirements would be the same, but we use different values to account for the state-of-the-art performance differences between the technologies.

BASE STATION PA

- Covers cellular and emerging worldwide interoperability for microwave access (WiMAX) applications
- SiC technology was removed from the base station table because of the rapid commercialization of GaN technology which provides significantly superior RF performance in terms of frequency, power density, and RF total power.

The general trends in the base station market have not significantly changed in the last two years. Base station application frequency continues to move to higher frequencies, but with continuing demand at lower frequencies. The WiMAX application at 3.55 GHz is receiving much attention as power device manufacturers continue to upgrade their technology and compete for the available sockets. Rapid price erosion continues unabated and is being driven by lower cost packaging and increased manufacturing efficiencies. Si LDMOS continues to be the dominant technology in the base station application space. Moreover, it is being utilized for WiMAX application even though its power added efficiency is lower than that of GaAs based devices. This has occurred because base station customers prefer the higher operating voltage of Si LDMOS, the lower cost, and the familiarity with LDMOS built on many years of use at lower frequency. In addition the operating voltage of LDMOS devices is moving to higher values (32V, 48V) to increase RF power density. At this time GaAs is preferred for lower power driver and pre-driver stages of the amplifier lineup.

The interest in GaN HFET technology continues to increase both for commercial and military applications. US government funding for the technology continues to be strong and is driving all aspects of the technology toward manufacturability. Commercial products are available from several companies. The attraction of GaN technology is its substantially higher RF power density which comes in part by its higher operating voltage (48V). This coupled with a higher device current density enables power densities two to four times that of LDMOS and GaAs. This high power density reduces the complexity of passive matching circuits which in turn reduces power loss in the amplifiers. However this technological advantage comes at a higher device cost which will slow adoption of the GaN in commercial applications.

SiC MESFET technology has been removed in 2007 because its RF performance has lagged behind that of GaN and there is little evidence that the performance superiority of GaN will be challenged. SiC MESFETs have the high operating voltage of GaN, but not the high current density which limits their RF power density to less than half that of GaN. They also have no cost advantage over GaN.

Table RFAMS6a Base Station Devices Technology Requirements—Near-term years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Application frequency (GHz) [1]	**0.8–3.5**	**0.8–3.5**	**0.8–3.5**	**0.8–5**	**0.8–5**	**0.8–5**	**0.8–5**	**0.8–8**	**0.8–8**
Cost ($$/Watt)	**0.3**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.1**	**0.1**	**0.1**
Packaging (C-Ceramic, P-Plastic)	**C, P**	**C, P**	**C, P**	**Plastic**	**Plastic**	**Plastic**	**Plastic**	**Plastic**	**Plastic**
Si LDMOS									
Operating voltage (V)	**32, 48**		**32, 48**	**32, 48**					
Saturated power (Watt)	**240**	**300**	**400**	**500**					
Saturated power density (W/mm)	**1.8**		**1.8**	**1.8**					
Saturated PAE (%)	**55**	**57**	**60**	**55**	**57**	**60**			
Linear power (Watt)	**120**	**150**	**200**	**250**					
Linear PAE (%)	**39**	**40**	**42**	**39**	**40**	**42**			
GaAs FET									
Operating voltage (V)	**28**			**28**				**28**	
Saturated power (Watt)	**240**			**240**				**240**	
Saturated power density (W/mm)	**1.5**			**1.8**				**1.8**	
Saturated PAE (%)	**65**	**67**	**70**	**65**	**67**	**70**		**70**	
Linear power (Watt)	**120**			**120**				**120**	
Linear PAE (%)	**46**	**47**	**50**	**46**	**47**	**50**		**50**	
GaN FET									
Operating voltage (V)	**48**		**48**					**48**	
Saturated power (Watt)	**200**		**300**		**400**		**500**	**500**	
Saturated power density (W/mm)	**4**		**5**					**5**	
Saturated PAE (%)	**60**	**62**	**65**	**60**	**62**	**65**		**65**	

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

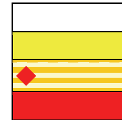


Table RFAMS6b Base Station Devices Technology Requirements—Long-term years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Application frequency (GHz) [1]	**0.8–8**						
Cost ($$/Watt)	**0.1**						
Packaging (C-Ceramic, P-Plastic)	**Plastic**						
Si LDMOS							
Operating voltage (V)	**32, 48**						
Saturated power (Watt)	**500**						
Saturated power density (W/mm)	**1.8**						
Saturated PAE (%)	**60**						
Linear power (Watt)	**250**						
Linear PAE (%)	**42**						
GaAs FET							
Operating voltage (V)	**28**						
Saturated power (Watt)	**240**						
Saturated power density (W/mm)	**1.8**						
Saturated PAE (%)	**70**	**72**					
Linear power (Watt)	**120**						
Linear PAE (%)	**50**	**51**					
GaN FET							
Operating voltage (V)	**48**						
Saturated power (Watt)	**500**						
Saturated power density (W/mm)	**5**						
Saturated PAE (%)	**65**						

Note for Table RFAMS6a and b:
[1] Application frequencies affected device saturated PAE scaling.

MILLIMETER WAVE (10 GHZ–100 GHZ)

- Deleted GaAs MESFET
- Added F_{min} and associated gain at 24, 60 and 94 GHz for low noise technologies
- Added Pout at peak efficiency and gain at 1 dB compression for power technologies at 24, 60 and 94 GHz.
- Added RF CMOS, including F_t, F_{max} and NFmin at 24 and 60 GHz base on HP CMOS roadmap

The millimeter wave tables show a projection of both key parameters intrinsic to the device such as breakdown voltage, maximum current, and transconductance, as well as performance factors for low noise and power transistors at fixed frequencies, namely noise measure, power, gain, and efficiency. We present expected performance data at three frequencies of commercial interest across the 10 to 100 GHz frequency spectrum: 24 GHz, 60 GHz, and 94 GHz. The 24 GHz spectrum is being positioned for wireless LAN applications and is being considered for automobile radar, although most of auto radar work has been done in the 60 and 77 GHz spectrums. The 60 GHz frequencies, long used by the military for secure satellite cross links, falls in a region where atmospheric absorption is high, and as a consequence is ideal for short range, "last mile" connectivity in congested areas, where the short range facilitates frequency re-use. Within the near term scope of this roadmap, we expect to see applications opening at 94 GHz for applications such as concealed weapons detection and imaging applications such as all weather aircraft landing systems. Had we included Long Term projections past 2015, we would have incorporated device projections up to 220 GHz for imaging applications that are currently at the research and development stage and even up to frequencies in the sub-THz region. The spectrum from 100 to 1000 GHz holds promise for many applications in the areas of medical imaging, spectroscopy, and security. The millimeter wave technology requirements section summaries the diverse technology choices for each of the three above frequencies.

Reviewing the tables shows that no one material or device technology has the monopoly at any frequency, and it quickly becomes obvious that the user has many choices. We have made no attempt to select a preferred component for any particular application, as the choice can be driven by many factors, not the least of which is cost. Other factors are

integration level, reliability heritage, operating voltage, and of course, performance, which is the focus of the roadmap. The following are observations regarding the obsolescence and preferences for certain technologies:

- GaAs MESFET has been dropped from the millimeter wave tables for 2007; although high voltage GaAs MESFET may have a role under 10 GHz, we see no new designs forthcoming in millimeter waves due to superior performance along with cost and reliability parity of GaAs PHEMT technologies.
- Likewise, low noise PHEMTs are likely to give way to InP HEMTs and GaAs MHEMTs by the end of this decade.
- Millimeter-wave power devices will fall into two regions: low power [a few to 10s of Watts] dominated by GaAs PHEMT and MHEMT, and high power [10s to 100s of Watts] dominated by GaN.
- GaN may also have a niche in the low noise area for applications requiring high robustness and linearity. GaN noise measure is comparable to PHEMT, and because limiters can be eliminated from the front end of receivers, they will offer distinct advantages in system noise figure.
- InP and SiGe HBTs will continue to compete for applications. SiGe offers clear cost and integration level advantages, while, for equivalent lithography InP will offer up to 4× improvement in performance.

We have also included RF CMOS in the Millimeter Wave section for 2007. The low values of maximum allowed voltage of HP CMOS limits its usefulness in driving power. Therefore, power and efficiency are not considered in the table. The already low and shrinking supply voltage and correspondingly low maximum-allowed voltage of the HP CMOS roadmap will drive innovative design techniques and new circuit topologies. To address designs in the higher millimeter wave frequency range, minimum gate length transistors will likely be used to provide the device maximum bandwidth. The voltage necessary to draw significant power out of the device may cause degradation of key performance parameters (e.g., V_{TH} , g_m, I_{DS}) due to hot carrier injection and other mechanisms and thereby may limit the effective lifetime. Utilizing CMOS for millimeter wave applications may require compromises among maximum operating frequency, maximum available power and acceptable device performances degradation.

Table RFAMS7 Millimeter Wave 10 GHz–100 GHz Technology Requirements

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*26*	*25*
Device Technology—FET									
GaAs PHEMT (low noise)									
Gate length (nm)	**100**								
F_t (GHz)	**150**								
Breakdown (volts)	**12**								
I_{max} (mA/mm)	**700**								
G_m (S/mm)	**0.55**								
NFmin (dB) at 26 GHz	**0.8**								
Associated Gain at 26 GHz	**10.8**								
NFmin (dB) at 94 GHz	**2.5**								
Associated Gain at 94 GHz	**3.6**								
GaAs PHEMT (power)									
Gate length (nm)	**150**		**100**						
F_{max} (GHz)	**150**		**200**						
Breakdown (volts)	**12**		**9**						
I_{max} (ma/mm)	**700**		**800**						
G_m (S/mm)	**0.5**		**0.7**						
P_{out} at 24 GHz and peak efficiency (mW/mm)	**650**		**650**						
Peak efficiency at 24 GHz (%)	**45**		**50**						
Gain at 24 GHz, at P_{1dB} (dB)	**11**		**13**						
GaAs PHEMT (power)									
Gate length (nm)	**100**		**70**						
F_{max} (GHz)	**200**		**250**						
Breakdown (volts)	**8**		**8**						
I_{max} (ma/mm)	**800**		**850**						
G_m (S/mm)	**0.65**		**0.75**	**0.8**					
P_{out} at 60 GHz and peak efficiency (mW/mm)	**550**								
Peak efficiency at 60 GHz (%)	**30**		**35**	**40**					
Gain at 60 GHz, at P_{1dB} (dB)	**7**		**8**	**9**					
P_{out} at 94 GHz and peak efficiency (mW/mm)	**350**		**350**	**350**					
Peak efficiency at 94 GHz (%)	**20**		**25**	**30**					
Gain at 94 GHz, at P_{1dB} (dB)	**5**		**6**	**7**					

Table RFAMS7 Millimeter Wave 10 GHz–100 GHz Technology Requirements

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*26*	*25*
InP HEMT (low noise)									
Gate length (nm)	**100**	**70**		**50**		**35**		**25**	
F_t (GHz)	**200**	**250**		**350**		**420**		**500**	
Breakdown (volts)	**4**	**3**		**2.5**		**2**		**1.5**	
I_{max} (ma/mm)	**500**	**600**		**550**		**500**			
G_m (S/mm)	**1.1**	**1.5**		**1.8**		**2**		**2.2**	
Fmin (dB) at 24 GHz	**0.5**	**0.4**		**0.3**		**0.3**		**0.25**	
Associated Gain (dB) at 24 GHz	**15**	**16**		**17**		**18**		**20**	
Fmin (dB) at 60 GHz	**1**	**0.8**		**0.6**		**0.6**		**0.5**	
Associated Gain (dB) at 60 GHz	**11**	**12**		**13**		**14**		**16**	
Fmin (dB) at 94 GHz	**1.5**	**1.3**		**1.1**		**1**		**0.9**	
Associated Gain (dB) at 94 GHz	**8**	**9**		**11**		**12**		**14**	
InP HEMT (power)									
Gate length (nm)	**100**		**70**			**50**			
F_{max} (GHz)	**250**		**400**			**450**			
Breakdown (volts)	**4**		**3**			**2.5**			
I_{max} (ma/mm)	**500**		**600**			**600**			
G_m (S/mm)	**1.1**		**1.5**			**1.7**			
P_{out} at 24 GHz and peak efficiency (mW/mm)	**450**								
Peak efficiency at 24 GHz (%)	**50**								
Gain at 24 GHz, at P_{1dB} (dB)	**14**								
P_{out} at 60 GHz and peak efficiency (mW/mm)	**300**		**400**						
Peak efficiency at 60 GHz (%)	**40**	**45**	**50**						
Gain at 60 GHz, at P_{1dB} (dB)	**10**		**14**						
P_{out} at 94 GHz and peak efficiency (mW/mm)	**150**	**160**	**200**						
Peak efficiency at 94 GHz (%)	**30**	**35**	**40**						
Gain at 94 GHz, at P_{1dB} (dB)	**7**		**10**						
GaAs MHEMT (low noise)—Ka through W-Band									
Gate length (nm)	**100**		**70**			**50**			**35**
F_t (GHz)	**200**		**250**			**350**			**420**
Channel In content (%)	**60**		**70**						**70**
Offstate Breakdown (volts)	**6**		**4**			**3**			**2.5**
I_{max} (ma/mm)	**900**		**900**			**950**			**950**
G_m (S/mm)	**1.2**		**1.4**			**1.5**			**1.8**
Fmin (dB) at 24 GHz	**0.5**		**0.4**			**0.3**			**0.2**
Associated Gain (dB) at 24GHz	**15**		**16**			**17**			**18**
Fmin (dB) at 60 GHz	**1**		**0.7**			**0.6**			**0.4**
Associated Gain (dB) at 60GHz	**10**		**12**			**14**			**15**
Fmin (dB) at 94 GHz	**1.5**		**1.2**			**1**			**0.8**
Associated Gain (dB) at 94GHz	**8**		**10**			**12**			**13**

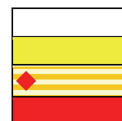
Table RFAMS7 Millimeter Wave 10 GHz–100 GHz Technology Requirements

<table>
<tr><td>Year of Production</td><td>2007</td><td>2008</td><td>2009</td><td>2010</td><td>2011</td><td>2012</td><td>2013</td><td>2014</td><td>2015</td></tr>
<tr><td>DRAM ½ Pitch (nm) (contacted)</td><td>65</td><td>57</td><td>50</td><td>45</td><td>40</td><td>36</td><td>32</td><td>26</td><td>25</td></tr>
<tr><td colspan="10">GaAs MHEMT (Power) -Ka band</td></tr>
<tr><td>Gate length (nm)</td><td colspan="2">150</td><td colspan="3">100</td><td colspan="4">70</td></tr>
<tr><td>Channel In content (%)</td><td colspan="9">35</td></tr>
<tr><td>F_{max} (GHz)</td><td colspan="2">200</td><td colspan="3">250</td><td colspan="4">300</td></tr>
<tr><td>Offstate Breakdown (volts)</td><td colspan="2">8</td><td colspan="3">10</td><td colspan="4">9</td></tr>
<tr><td>I_{max} (ma/mm)</td><td colspan="2">760</td><td colspan="3">850</td><td colspan="4">900</td></tr>
<tr><td>G_m (S/mm)</td><td colspan="2">0.85</td><td colspan="3">1</td><td colspan="4">1.2</td></tr>
<tr><td>P_{out} at 24 GHz and peak efficiency (mW/mm)</td><td colspan="2">800</td><td colspan="3">850</td><td colspan="4">900</td></tr>
<tr><td>Peak efficiency at 24 GHz (%)</td><td colspan="2">45</td><td colspan="3">50</td><td colspan="4">55</td></tr>
<tr><td>Gain at 24 GHz, at P_{1dB} (dB)</td><td colspan="2">12</td><td colspan="3">14</td><td colspan="4">15</td></tr>
<tr><td colspan="10">GaAs MHEMT (Power)</td></tr>
<tr><td>Gate length (nm)</td><td colspan="2">100</td><td colspan="3">70</td><td colspan="4">50</td></tr>
<tr><td>Channel In content (%)</td><td colspan="2">53</td><td colspan="3">43</td><td colspan="4">35</td></tr>
<tr><td>F_{max} (GHz)</td><td colspan="2">300</td><td colspan="3">300</td><td colspan="4">325</td></tr>
<tr><td>Offstate Breakdown (volts)</td><td colspan="2">7</td><td colspan="7">9</td></tr>
<tr><td>I_{max} (ma/mm)</td><td colspan="2">900</td><td colspan="3">900</td><td colspan="4">950</td></tr>
<tr><td>G_m (S/mm)</td><td colspan="2">1.2</td><td colspan="3">1.4</td><td colspan="4">1.5</td></tr>
<tr><td>P_{out} at 60 GHz and peak efficiency (mW/mm)</td><td colspan="2">500</td><td colspan="3">550</td><td colspan="4">600</td></tr>
<tr><td>Peak efficiency at 60 GHz (%)</td><td colspan="2">40</td><td colspan="3">45</td><td colspan="4">55</td></tr>
<tr><td>Gain at 60 GHz, at P_{1dB} (dB)</td><td colspan="2">8</td><td colspan="3">9</td><td colspan="4">10</td></tr>
<tr><td>P_{out} at 94 GHz and peak efficiency (mW/mm)</td><td colspan="2">225</td><td colspan="3">300</td><td colspan="4">350</td></tr>
<tr><td>Peak efficiency at 94 GHz (%)</td><td colspan="2">30</td><td colspan="3">35</td><td colspan="4">45</td></tr>
<tr><td>Gain at 94 GHz, at P_{1dB} (dB)</td><td colspan="2">6</td><td colspan="3">7</td><td colspan="4">8</td></tr>
<tr><td colspan="10">GaN HEMT (low noise)</td></tr>
<tr><td>Gate Length (nm)</td><td></td><td></td><td>150</td><td colspan="2">100</td><td colspan="2">70</td><td colspan="2">50</td></tr>
<tr><td>F_t (GHz)</td><td></td><td></td><td>120</td><td colspan="2">160</td><td colspan="2">200</td><td colspan="2">240</td></tr>
<tr><td>Breakdown (volts)</td><td></td><td></td><td>40</td><td colspan="2">35</td><td colspan="2">30</td><td colspan="2">25</td></tr>
<tr><td>I_{max} (ma/mm)</td><td></td><td></td><td>1000</td><td>1200</td><td>1300</td><td colspan="4">1400</td></tr>
<tr><td>G_m (S/mm)</td><td></td><td></td><td>0.4</td><td>0.5</td><td>0.55</td><td colspan="2">0.6</td><td colspan="2">0.65</td></tr>
<tr><td>Fmin (dB) at 24 GHz</td><td></td><td></td><td>1.2</td><td colspan="2">1</td><td colspan="2">0.8</td><td colspan="2">0.6</td></tr>
<tr><td>Associated Gain at 24 GHz</td><td></td><td></td><td>10</td><td colspan="2">12</td><td colspan="2">13</td><td colspan="2">14</td></tr>
<tr><td colspan="10">GaN HEMT (power)</td></tr>
<tr><td>Gate Length (nm)</td><td></td><td></td><td></td><td colspan="6">150</td></tr>
<tr><td>F_t (GHz)</td><td></td><td></td><td></td><td colspan="6">150</td></tr>
<tr><td>Breakdown (volts)</td><td></td><td></td><td></td><td>60</td><td colspan="5">80</td></tr>
<tr><td>I_{max} (ma/mm)</td><td></td><td></td><td></td><td colspan="2">1200</td><td colspan="4">1400</td></tr>
<tr><td>G_m (S/mm)</td><td></td><td></td><td></td><td colspan="2">0.5
0.5</td><td colspan="4">0.6</td></tr>
<tr><td>P_{out} at 24 GHz and peak efficiency (mW/mm)</td><td></td><td></td><td></td><td>5000</td><td>6000</td><td>7000</td><td colspan="3">8000</td></tr>
<tr><td>Peak efficiency at 24 GHz (%)</td><td></td><td></td><td></td><td>35</td><td>40</td><td>42.5</td><td colspan="3">45</td></tr>
<tr><td>Gain at 24 GHz, at P_{1dB} (dB)</td><td></td><td></td><td></td><td colspan="2">10</td><td colspan="4">12</td></tr>
</table>

Table RFAMS7 Millimeter Wave 10 GHz–100 GHz Technology Requirements

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*26*	*25*
GaN HEMT (power)									
Gate length (nm)				**100**		**70**			**50**
F_{max} (GHz)				**200**		**240**			**280**
Breakdown (volts)				**40**	**60**	**40**	**60**	**60**	**40**
I_{max} (ma/mm)				**1200**		**1500**			
G_m (S/mm)				**0.55**		**0.65**			
P_{out} at 60 GHz and peak efficiency (mW/mm)				**4000**	**4500**	**5000**			**4500**
Peak efficiency at 60 GHz (%)				**30**		**35**			**40**
Gain at 60 GHz, at P_{1dB} (dB)				**8**	**8.5**	**9**	**9.5**		**10**
P_{out} at 94 GHz and peak efficiency (mW/mm)				**2500**	**3000**	**3500**	**4000**		**3500**
Peak efficiency at 94 GHz (%)				**20**	**25**	**30**			**35**
Gain at 94 GHz, at P_{1dB} (dB)				**6**	**6.5**	**7**	**7.5**		**8**
Device Technology—RF CMOS	-								
CMOS NFET [1 HP CMOS lag 2 yrs]	-								
V_{dd}: Power Supply Voltage (V)	**1.1**			**1**			**0.95**	**0.9**	**0.9**
EOT: Equivalent Oxide Thickness (Å) [13]	**12**	**11**		**9**	**7.5**	**6.5**	**5.5**	**5**	**6**
L_g: Physical L_{gate} for High Performance logic (nm)	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
Peak F_t (GHz)	**280**	**320**	**360**	**400**	**440**	**490**	**550**	**630**	**670**
Peak F_{max} (GHz)	**340**	**390**	**440**	**510**	**560**	**630**	**710**	**820**	**880**
NF_{min} (dB) at 24GHz	**2**	**1.8**	**1.6**	**1.4**	**1.3**	**1.2**	**1.1**	**1**	**0.9**
NF_{min} (dB) at 60GHz	**5.1**	**4.5**	**4.0**	**3.6**	**3.3**	**3.0**	**2.7**	**2.4**	**2.3**
Device Technology—HBT									
InP HBT									
Emitter width (nm)	**1**	**0.5**	**0.5**	**0.25**			**0.13**		
Peak F_t (GHz)	**150**	**320**		**400**			**560**		
Peak F_{max} (GHz)	**200**	**320**		**560**			**800**		
BV_{ceo}	**8**	**5**		**4**			**3**		
J_c at Peak F_t (mA/μm^2)	**1**	**5**		**10**			**20**		
SiGe HBT									
Emitter width (nm)	**130**	**120**	**100**			**90**			**80**
Peak F_t (GHz) [V_{bc}=1V]	**250**	**275**	**300**	**320**	**340**	**360**	**380**	**395**	**415**
Peak F_{max} (GHz)	**280**	**305**	**330**	**350**	**370**	**390**	**410**	**425**	**445**
Nfmin (dB) at 60GHz	**3.0**	**2.5**	**2.2**	**1.9**	**1.7**	**1.5**	**1.4**	**1.3**	**1.2**
BV_{ceo}	**1.8**	**1.7**	**1.65**	**1.6**	**1.55**	**1.5**	**1.45**	**1.4**	**1.35**
J_c at Peak F_t (mA/μm^2)	**13**	**15**	**17**	**18**	**19**	**21**	**22**	**23**	**24**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



POTENTIAL SOLUTIONS

The 2007 potential solutions tables are divided into two main figures: one covering the 0.8 GHz–10 GHz applications and one covering 10 GHz–100 GHz millimeter wave applications.

RF AND AMS CMOS

The solutions for mixed-signal applications differ from those already given for memory and logic applications discussed in sections of the *Process Integration, Devices, and Structures (PIDS) Chapter*. Successful mixed-signal technologies will leverage the baseline digital platform while integrating value-added features and functions. Key ingredients to successful mixed-signal integration are the addition of special higher-voltage analog precision transistors, high quality passive elements, adequate signal isolation, and compatible active devices.

Increased CMOS digital performance results in an aggressive roadmap for NF, $F_{t,}$ and F_{max} improvements. In addition to the obvious benefits of increased performance with scaling, technology changes may improve other device characteristics important to RF and analog circuit functions. Although thermal and floating-body effects and high-resistive substrate connections pose challenges, routine production of SOI microprocessors, high performance I/O interfaces, and high frequency phase-locked loop circuits demonstrate the potential for use in other analog applications. The introduction of metal gates may reduce threshold mismatch due to variations in gate doping and increase F_{max} due to decreased gate resistance. The introduction of channel strain to increase device current should enable improvements in precision analog and RF driver performance with little or no degradation in other characteristics. Fully-depleted, dual-gate SOI has low channel doping relative to conventional CMOS structures and so may have reduced mismatch. In addition, this structure will offer reduced drain conductance with an attendant increase in voltage-gain and F_{max}. The multiple threshold voltages that enable optimization of digital power-delay will also offer design options for mixed-signal and RF applications.

The introduction of metal gate electrodes, high permittivity gate dielectrics, and fully depleted, dual-gate SOI will pose additional challenges for mixed-signal applications. With the use of these technology elements, heretofore unimportant physical mechanisms may emerge as limiting factors of performance and will require reconsideration of physical and manufacturing practices.

The mixed-signal supply voltage continues to lag that of high-performance digital by two or more generations. A combination of multiple gate oxide thickness, multiple thresholds, and DC-DC conversion is needed to support the increased mixed-signal requirements. The added process complexity will be in contradiction to desired low cost. Design solutions in active threshold regulation, substrate biasing, and novel architectures will be required to extend the trend for lower supply voltages to mixed-signal applications. An alternative to full integration is the SiP that combines circuits made with different technologies and optimized for the desired functions.

Good matching characteristics are critical for mixed-signal devices including analog to digital converters (ADCs) and for successful design of digital latches and static memory elements. We expect that metal gate electrodes will incrementally improve transistor matching. Active circuit compensation techniques will also compensate for the degradation of matching characteristics with device scaling.

Present scaling trends will result in substantially degraded voltage-gain even at relatively long channel lengths due to the dominant effect that pocket implants have on the variation of device threshold with drain bias. This will slow the increase in F_{max} and require additional power dissipation in analog circuits. This trend can be slowed by the introduction of asymmetric devices with no pocket implant at the drain end. In addition, the RF roadmap will drive the need for integration of asymmetrical devices (drain extensions) to increase the voltage handling capability of CMOS drivers and power management devices and possibly for the use of laterally diffused channels to improve performance of high voltage devices (LDMOS).

Increasing integration levels drive the requirement for improved signal isolation and better simulation capability of cross-talk between circuit blocks. The use of high-resistivity silicon substrates will be required in the most demanding applications.

RF AND AMS BIPOLAR DEVICES

Potential solutions for continuing to improve the F_t /F_{max} of bipolar transistors include lithography advancements which enable more narrow emitter widths for improving F_{max} and reducing the unit length current at peak F_t. The improved F_{max} and reduced unit length current at peak F_t can be traded-off for more aggressive vertical profiles (thinner base width and higher collector doping concentration) to improve F_t while remaining within reliability limits for current handling in the

metal interconnects. The improved F_t and F_{max} will also improve the noise figure at high frequency to address millimeter wave requirements.

Control of the vertical profile can present a limit to this approach and potential solutions can include the introduction of new techniques such as atomic-layer-epitaxy or alternative emitter construction. Potentially, new materials could help improve the transit time and/or control of the base width as the introduction of Ge or Carbon did in the recent past.

Parasitic losses can further limit performance gains and potential solutions here include use of selective epitaxy as well as use of innovative architectures that minimize the interaction between the extrinsic and intrinsic regions of devices.

ON-CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

ON-CHIP PASSIVES

The trend of moving discrete passive elements from board level to chip level will continue. Solutions for achieving discrete-equivalent precision on-chip passive components are expected. Alternatively, some passives may be integrated into the printed board or package as a method of cost reduction and simplification. New high-κ dielectrics can be used either to reduce integrated capacitor area or to keep the integrated capacitor area acceptable for new emerging analog and RF circuit functions. The high-κ dielectrics can significantly increase the capacitance density of the MIM capacitor, MOS capacitor, and MOS varactor. The continued improvement and performance verification in linearity and matching of metal-oxide-metal (MOM) capacitor will make it an attractive low cost option for future analog and RF circuits.

Higher quality and higher density inductors can enable new functionality and circuit topology integrated on-chip and represents a significant challenge for analog and RF integrated circuits. Potential solutions for higher quality and higher density inductors include the use of thicker layers of Cu and thicker top dielectrics and the integration of magnetic materials with on-chip inductors. These may co-exist with inductors integrated in the package for the most demanding applications. Integrated resistors need low parasitic capacitance and high temperature linearity, which can be fulfilled by innovative approaches in fabrication of the integrated resistors.

Further research is needed on MOS capacitors and MOS varactors processed with high-κ dielectrics. These are coupled to the availability of high-κ dielectrics, respectively, for analog high precision transistors and high-speed RF transistors. The impact on the VCO phase noise of the high-κ dielectric, which typically has a much higher trap density, needs sufficient research.

In order to achieve high capacitance density for RF MIM capacitors, various high-κ dielectrics are being explored. This includes Ta_2O_5, HfO_2 and other high-κ materials.

The key challenge is to keep the leakage current and voltage linearity low as the film thickness is reduced. One way to solve this tradeoff is to use multi-layered structures where the capacitance density and voltage linearity can be separately optimized. Whether such solutions are production worthy is yet to be seen.

When feature size is scaled down and when the stacking structure or the high-κ dielectric MIM is excluded, the unit capacitance of the inter-digitated, lateral MOM capacitor can be close to or exceed that of the standard MIM capacitor. Compared with the MIM capacitor, there are no additional processing steps and cost for the inter-digitated MOM capacitor. Therefore, it is recognized as a capacitor option, especially for low-cost applications. There are tradeoffs observed between the unit capacitance and the parasitic coupling with the Si substrate. Moreover, the mismatching performance of the inter-digitated MOM capacitor can't be over-emphasized. However, the mismatching performance of the inter-digitated MOM capacitor can be competitive to that of the MIM capacitor by using proper structure designs.

Above-passivation inductors offer high Q-factors and resonance frequencies, but require special processing. Technical feasibility has been demonstrated. Some companies have this available as a production process. The choice whether to use above-passivation inductors depends on the limited access today to such technology and the economics. The latter is assessed on a case-by-case basis. Improvements in inductance density are difficult to realize. Solutions of stacking inductors have been proposed, but add significantly to the cost and jeopardize the resonance frequency due to the high capacitive coupling between the stacked inductors. The use of magnetic materials has received some attention in the literature, such as the use of magnetic shields. However, the research in this area is not yet complete.

Increasing CMOS complexity makes it more difficult to produce stable, highly manufacturable front-end-of-line (FEOL) resistors. One solution to this problem is to provide high-resistance BEOL resistors comparable to the common p-type polysilicon resistors in the FEOL. Due to thermal affects, this can be a problem because thermal control of these devices is paramount in the BEOL to minimize electromigration. This problem needs to be addressed with new materials that provide not only good resistor parametrics for RF and analog circuits but good thermal control at high currents. This is a good area for R&D on RF and analog technologies.

Embedded Passives

Embedded passives, including Integrated Passives Devices (IPD), provide off-chip and inter-chip solutions for passive networks in circuit design. This technology is not only complementary to on-chip passives, but also provides packaging and interconnection solutions for the system. Process technologies for manufacturing passive components in the substrate, especially for organic PCBs, are divided in two major categories, lamination and print. For the printing process, general screen printing is the most cost effective but less accurate; new process technology such as ink-jet print provides solution for improved process tolerance.

In general, even though the design, material, and process of organic embedded passives are different from silicon based technology, many concepts are similar. The organic PCB manufacturer should learn from the semiconductor manufacturer process methodologies to improve tolerance and quality.

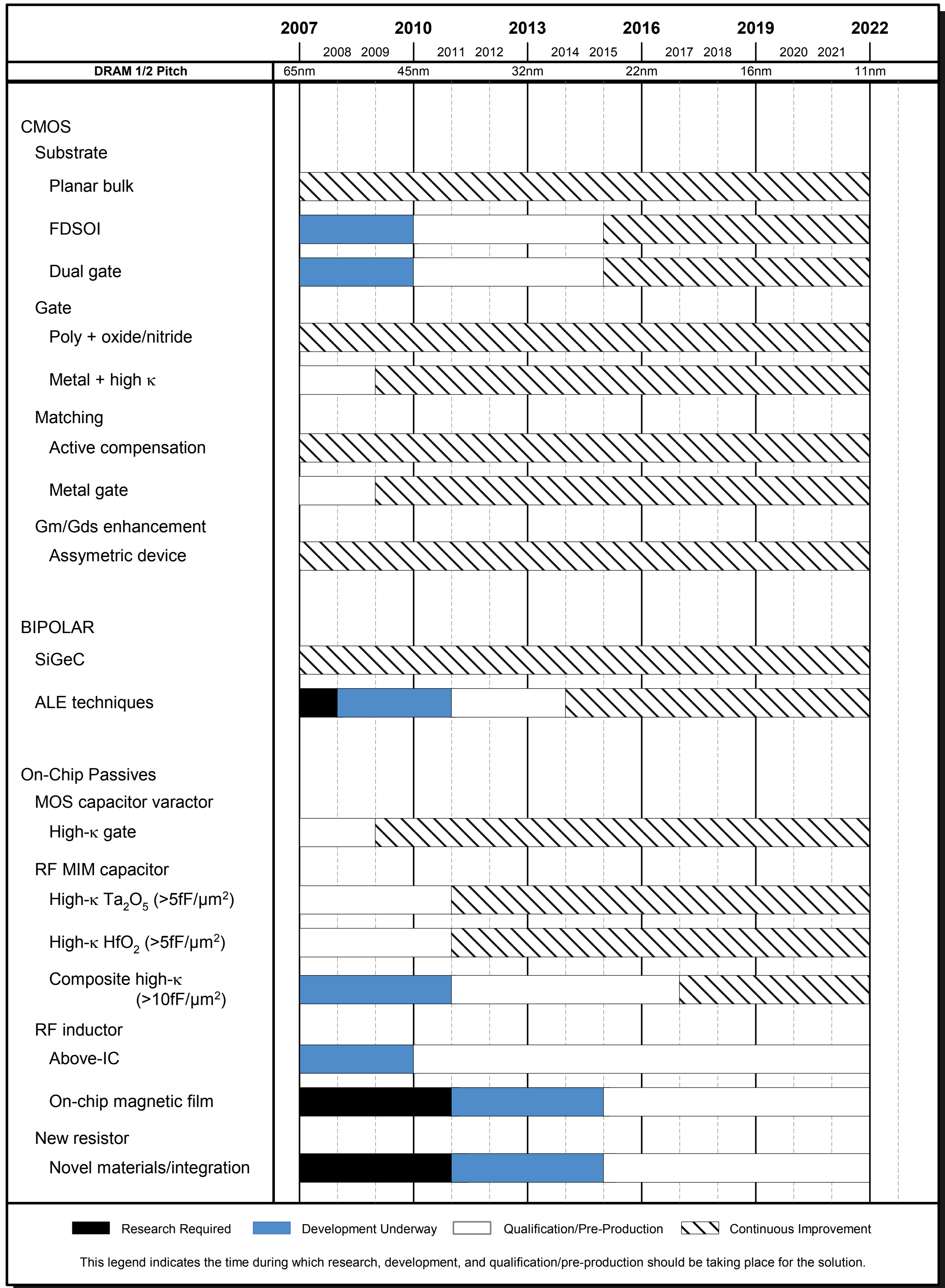
POWER AMPLIFIERS

HANDSET POWER AMPLIFIERS

Integrated HBT-HEMT technologies will address several of the issues that power amplifier designers will face in the long and short term. The integration of the FET with the HBT allows more complex bias circuits to be designed and integrated with the power chain. Such FET-HBT circuits also will allow integration stage by-passing switches to be place directly on the PA die and will contribute to improved mid-power efficiency. While these technologies are available now on a limited basis, manufacturing challenges will need to be addressed before these solutions become pervasive. The reduction of the end-of-life battery voltage will drive several possible solutions that depend on the type of PA being designed and the, as yet, undisclosed customer expectations on performance. Several technologies [MEMs, tunable varactors (using materials such as barium strontium titantate), or high-Q varactor networks] for varying or switching the load to the PA exist. These technologies will play significant roles in addressing the challenging end-of-life battery voltage issue. Such tunable networks will be required to improve performance over the entire PA operating range and which one(s) become the “right” solution(s) will depend heavily on cost structure and integrability into power amplifier modules (PAMs).

BASE STATION AMPLIFIERS

GaN technology appears to offer a technology solution to many of the challenges facing Si LDMOS technology. First GaN is a wide bandgap semiconductor which enables higher breakdown voltages which can be taken advantage of in numerous applications. Second the epitaxial material structure of the GaN device enables a very high current density which when coupled with a high operating voltage achieves an RF power density approximately five times that of Si LDMOS. This higher power density enables a substantial reduction in die size for a given power level which makes achieving wider bandwidth amplifiers possible. The lower parasitic capacitances of the smaller die should also enable utilization of the more efficient classes of amplifiers: Class D, Class E, and Class S. Finally high performance GaN technology utilizes a SiC substrate with its superior thermal conductivity. This keeps device channel temperatures lower and enables the high power density of the technology.



Bipolar use mainly in transceiver; CMOS use in transceiver and AMS; Meeting passive roadmap density and leakage w/Cu backend

Figure RFAMS2 8–10 GHz Potential Solutions

MILLIMETER WAVE

Compound semiconductors take advantage of the advances in lithography and processing equipment that are available in the silicon industry. In order to accomplish this, wafer diameters need to be within one or two generations of the silicon industry. Six-inch semi-insulating GaAs wafers are in production now while InP wafers seem stalled at four inches for the foreseeable future. Silicon carbide semi-insulating substrates, the basis for GaN HEMTs, is at three inches, although the optical industry, which utilizes conducting substrates, will drive the technology to four inches soon. The III–V industry needs to continually push to larger wafer sizes to keep pace with the silicon equipment infrastructure.

While significant advances are being made in optical lithography tools, the cost of masks is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beam is a solution to the mask cost, but wafer through-put, which is measured in hours per III-V wafer as compared to silicon wafers per hour, needs to be increased with high current electron sources and fast alignment systems.

Uniformity, reproducibility and yield metrics for compound semiconductors still lag behind Si-based technologies. This is not surprising, given the much higher investment in infrastructure and research for silicon, as well as the extremely large disparity in production volume between the two. Nevertheless, as production volume in a particular compound technology rises, unit costs are found to decrease on a learning curve not unlike that of silicon.

Substrate quality is still problematic for the emerging wide bandgap devices, although quality has improved significantly over the past several years. Research on GaN templates is continuing, but in the interim, SiC substrates will become more viable as their defect density decreases. If SiGe is to challenge other technologies for the millimeter wave spectrum, then high resistivity low-loss silicon needs to be addressed.

Thermal dissipation is the major challenge for wide-bandgap III-V power devices. While GaN and SiC substrates have higher thermal conductance values compared to GaAs and InP, the 5× to 10× higher power densities typically present in these wide bandgap semiconductors somewhat offsets the advantage in higher thermal conductance. These circumstances make thermal dissipation a critical device design aspect. Proven techniques include thin [0.002-inch 0.05 mm] wafers, thermal shunts, and bathtub vias. These techniques and more innovative solutions such as diamond composites need to be applied to the wide bandgap devices.

High-voltage breakdown is desirable for both mixed-signal and high-power devices. As dimensions decrease for higher frequency performance, the operating voltage suffers. This is particularly troublesome for mixed-signal devices that require more headroom for the analog functions than for the digital functions. In this regard, InP HBTs offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe will be orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs.

For power FETs, gate recessing has been used successfully to achieve higher breakdown voltages, but this has yet to be applied to GaN. Instead, use of field plates to tailor the electric field on the drain side of the gate has been shown to be effective in achieving high breakdown voltages, although this can compromise high frequency performance. Continued improvement of passivation and hot carrier effects is also needed.

Finally, high frequency performance in III-Vs is driven as much by epitaxy (vertical scaling) as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by properly engineering the epitaxial layer stack and continued improvement in all of the III-V devices can be expected through bandgap engineering.

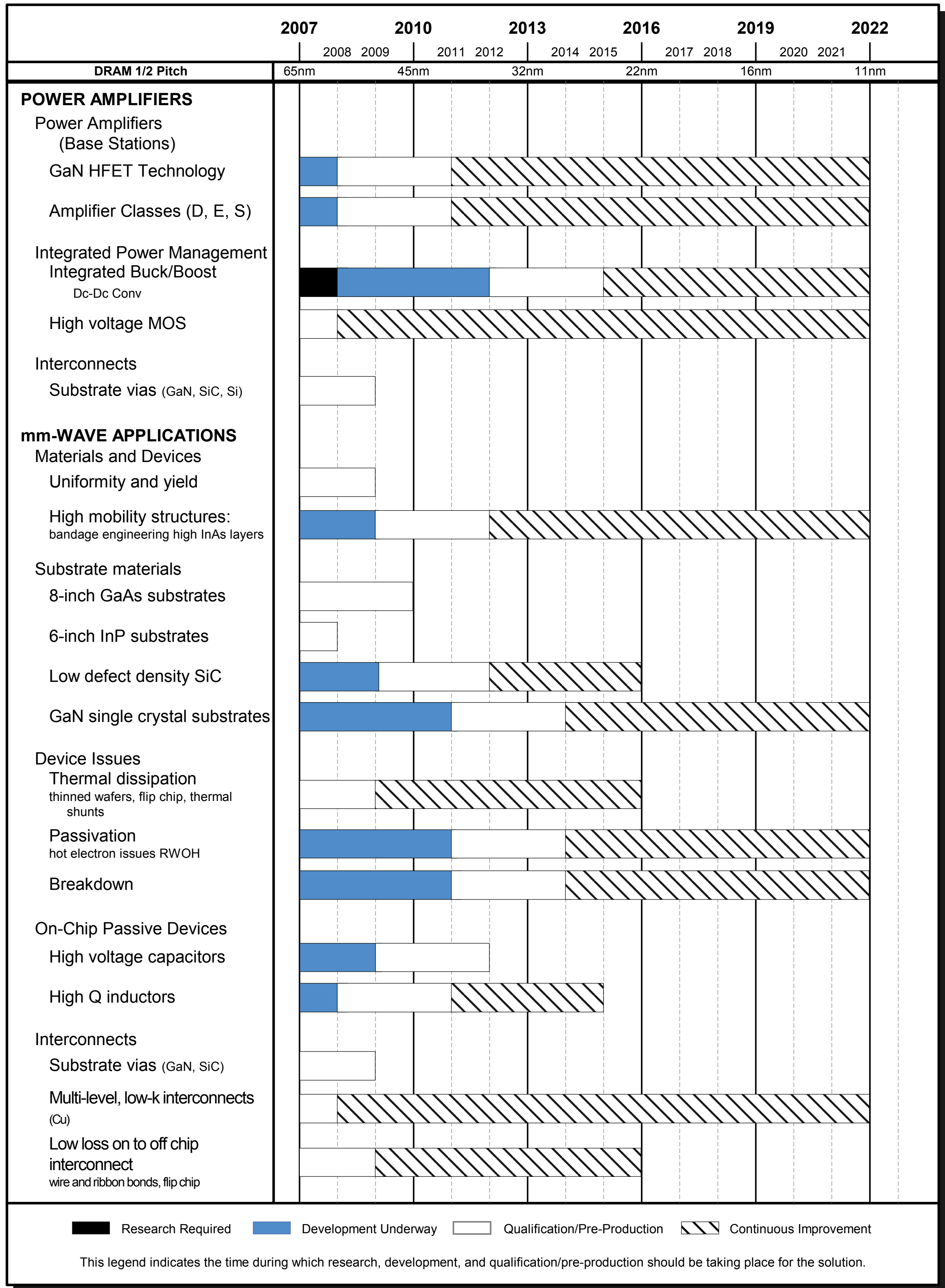


Figure RFAMS3 10–100 GHz Potential Solutions

MORE THAN MOORE

Wireless communications bands and services are proliferating. Cellular technology standards such as global system for mobile communications (GSM), code division multiple access (CDMA), enhanced data rates for GSM evolution (EDGE), and wideband CDMA (WCDMA) are being developed for long-range voice, data, and video transfer. In addition to these public mobile services, many private systems such as IEEE 802.11 WLAN and Bluetooth are also becoming very popular. All these services have different carrier frequencies, channel bandwidths, and modulation schemes. These differences have motivated the industry to look for multi-band, multi-mode devices to enable ubiquitous connectivity.

Although it is possible to combine some of these bands and modes in a device using conventional systems, the best solution is the system called software defined radio (SDR), which can change its radio functions by swapping software instead of replacing hardware. SDR uses a single radio to cover any communication channel in a wide frequency spectrum with any modulation and bandwidth, thus providing multi-band, multi-mode operation and reconfigurability.

To achieve the required flexibility, the boundary of digital processing should be moved as close as possible to the antenna. The exact point where the conversion between digital and analog signals occurs depends on the system architecture. The requirement of supporting multiple frequency bands complicates the design of the RF front end and the A/D and D/A converters. The RF front end should be adjustable for different carrier frequencies, bandwidths, and other requirements such as sensitivity set by the different standards. It requires a wideband LNA that covers the entire frequency range of interest.

The requirement for A/D and D/A converters also depends on the architecture being used. The original concept of SDR by Mitola in 1995 required the digitizing of all possible RF signals concurrently and such digitizing would require a 12 GHz, 12-bit ADC dissipating 500W, which is not unrealistic for mobile equipment. Recent architecture proposals that handle one channel at a time resulted in more tractable, low-power ADC requirements. The digital signal processor (DSP) and digital to analog converter (DAC) requirements are thought to be met by the state-of-the-art, deep submicron CMOS technology. The realization of such a solution is driven by collaboration between the system architect, converter design, and CMOS roadmap.

Another realization of a multi-standard is to support a hybrid solution with a wideband amplifier and integrated low-cost switching and filtering network. Such networks drive the needs for a RFMEMS roadmap and an associated embedded passive roadmap to support an integrated package module solution. The embedded laminate passives requirements were discussed in the above Passives Section.

RF MEMS FOR WIRELESS APPLICATIONS

One of the emerging technologies to address needs in the consumer markets for wireless communication is micro-electrical mechanical systems (MEMS). MEMS have been around for a long time, e.g., used in millimeter wave communications for antenna tuning, and are better know in the sensors and transducer application markets. Two examples of MEMS in high-volume manufacturing are the Texas Instruments' DLP™ technology for cinema projection and airbag sensors (accelerometers, produced by such companies as Analog Devices and Bosch) used in safety equipment in every car built today. The unifying feature between all MEMS technologies are moving parts, however, the MEMS manufacturing technologies and approaches to provide solutions by MEMS are extremely diverse.

The 2007 RFMEMS roadmap focus is on four MEMS technologies—bulk acoustic wave devices, resonator devices, metal contact switches, and capacitive contact switches. The most mature technology of the four examples is the bulk acoustic wave (BAW) filter used today in most cell phones. Refer to Table RFAMS8. BAW devices feature a vibrating (piezoelectric) material and are implemented as discrete components—die attached to the board for handset filters and tuning. The widespread use of BAW filters in wireless applications and the MEMS packaging required to encapsulate the free surface of the BAW helps categorize the BAW product as MEMS and not transducer technology. BAW filter roadmap challenges are in cost reduction (footprint, thickness, packaging), in higher performance (e.g., with higher frequency precision and lower signal loss), and in integration with the wireless chip.

Next in the table are resonator devices for timing chip applications. These devices are relatively new, but leverage technology used in sensor markets for airbags and gyroscopes. One large market is quartz oscillator replacement using silicon based MEMS devices which allow a silicon-like economy of scale. In addition to cost and fit/form improvement, performance may be on par with some quartz devices and thus replacement will be a near term goal. In the medium to long term, resonators may be integrated with CMOS and new functionality due to the need for multiple frequencies on a given chip, tunability, and on-chip integration could be achieved at highly competitive prices.

The two switch applications given in Table RFAMS8 are capacitive contact and metal contact switches. The capacitive switch, which mechanically toggles a circuit or load line between two states of capacitance, has the promise to drastically reduce leakage current and improve the Q factor of switches served today, for example, by VCOs and solid state circuitry. The main advantage is that in the off state the plates of the capacitor are physically separated. The metal contact switch also has two physically separated plates and when they are closed form an Ohmic contact similar to a wall switch in the home. Among the four classes of devices in this year's 2007 MEMS Roadmap, the metal contact switch has the most challenges for integration, primarily due to reliability concerns of the switch contact interfaces that require stable performance over billions of cycles. In addition, size, packaging and cost per function for integration in high volume applications will be a major challenge, but may provide the highest performance pay-off.

Finally, two other MEMS devices were contemplated but left out of the 2007 version of the wireless roadmap. These were MEMS gyroscopes and MEMS microphones. These products do exist today, but may not be in-line with the goals of the 2007 Wireless roadmap. They will be considered for inclusion in future roadmaps.

The RFMEMS requirement table (Table RFAMS8) includes four categories—Design Tools, Packaging, Performance Driver, and Cost Driver—in which the four MEMS devices mentioned above are reviewed.

The first section, Design Tools, addresses common design tool concerns for implementation of MEMS features in a wireless product design flow. This section defines the need and likely timing of design tool availability such that the full advantage of the MEMS manufacturing technologies can be realized. The relative immaturity of MEMS specific tool integration into existing design flow is considered both a limitation on MEMS use as well as an opportunity for tool vendors.

In the next three sections, Packaging, Performance, and Cost, key manufacturing limitations to introduction in the marketplace are considered. Packaging of MEMS is critical to yield, reliability, and cost of MEMS. Packaging requirements include the need to reliably, hermetically enclose a cavity in which the moving parts (MEMS) operate. As wireless MEMS today are mostly discrete components added to a board, an obvious future path is integration of features with the VLSI integrated circuit. Two stages of integration are contemplated in the table:"above IC" also known as post processing after standard wafer fabrication, and "embedded," where the MEMS features have been created within the standard wafer fabrication layers or process.

Performance of MEMS devices is described in the third portion of the table. We expect that MEMS performance is likely the main driver for including MEMS in wireless products. If it were not, then these MEMS potential solutions would not be sought. In some cases, the performance metric listed in the table may represent old demonstrations but contemplated here in a cost and fit/form/function that is usable by the consumer wireless industry. One example would be metal contact switches that exist today with high performance and reliability, but are too large and too costly for consumer wireless product inclusion.

The last section of the table considers the cost drivers for introduction of MEMS into high volume wireless applications. Package, test, and reliability are common themes for areas requiring significant improvement. In addition, the on-chip integration approaches of "above IC" and "embedded" are clear ways to reduce bill of materials (BoM), as with system SoC, that reduces chip count, but is further out in time.

Table RFAMS8 RF and Analog Mixed-Signal RFMEMS

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Design Tools							
BAW	**(0) Separate tools**	**(1) IRFM, (2) CM**	**(3) DF**		**DF + MEMS TCAD**		
Resonator	**(0) Separate tools**	**(1) IRFM, (2) CM**	**(3) DF**				
Switch—capacitive contact	**(0) Separate tools, (2) CM**		**(1) IRFM**	**(3) DF**			
Switch—metal contact	**(0) Separate tools, (2) CM**		**(1) IRFM**	**(3) DF**			
All MEMS devices		**(4) MEMS TCAD**	**(4) MEMS TCAD**				
Packaging							
BAW	**Die stacking.**	**Wafer level package. Micro cavity package.**			**Above IC integration**		
Resonator		**Stacked die**		**Embedded integration with IC**			
Switch—capacitive contact		**Above IC integration**			**Embedded integration with IC**		
Switch—metal contact		**Above IC integration**			**Embedded integration with IC**		
Performance Driver							
BAW	**F= 900MHz to 2.5GHz. Size and cost; TCF= -20 ppm/K; K2*Q=100**	**F= 900MHz to 5GHz. Testability improved. TCF= -5ppm; K2*Q=150**		**Coupled Resonator Filter (CRF) ≥ increase functionality (e.g., impedance match).**		**F= 900MHz to 10GHz. Built In Self Test (BIST) structure. Tunable filter? TCF= -1ppm; K2*Q=200**	
Resonator	**Real time clock (32 kHz)**		**Clock oscillator (10–100MHz) multi-frequency per die.**		**Nano resonator for filter function (800MHz–2.5GHz)**		
Switch—capacitive contact t		**Cellular frontend (tuning): 20:1 tuning ratio, 40V actuation**			**Cellular frontend (tuning): 30:1 tuning ratio, low-voltage actuation**		
Switch—metal contact		**Cellular frontend (tuning, T/R): insertion loss <0.3dB, lifetime >1e10 cycles**			**Cellular frontend (tuning, T/R): insertion loss <0.2dB, lifetime >1e11 cycles**		
Cost Driver							
BAW		**Die size / package**			**Integration with semiconductor die**		
Resonator	**MEMS processing cost**		**Packaging**	**Integration with semiconductor die**			
Switch—capacitive contact		**Processing cost. Die size / microcavity package. Test.**			**Integration with semiconductor die**		
Switch—metal contact		**Process cost. Reliability / size / microcavity package. Test.**			**Integration with semiconductor die**		

Notes for Table RFAMS8:

(0) Separate Tools—Mechanical and RF simulation tools not integrated. Manual integration with package and IC.

(1) IRFM—integrated RF and mechanical 3D simulation tools

(2) CM—physically based compact models i.e. simplified versions of IRFM

(3) DF—Design flow e.g. circuit level simulation, that includes IRFM

(4) MEMS TCAD—3D process sequence simulation tool to simulate deposition, roughness, thermal, underetch, etc…

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