INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

YIELD ENHANCEMENT

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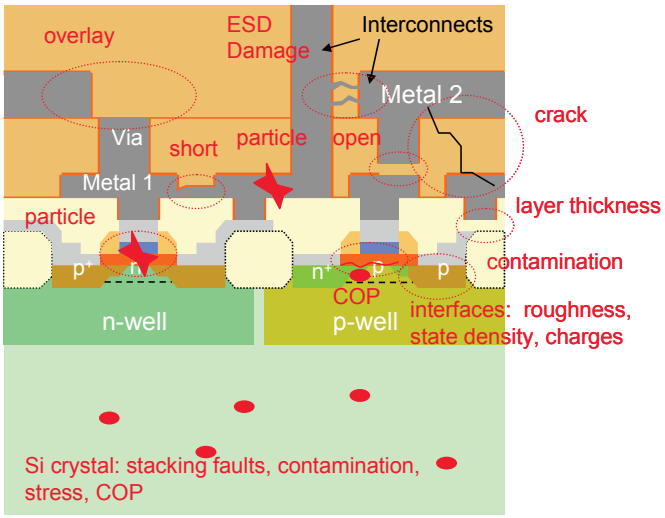
YIELD ENHANCEMENT

SCOPE

Yield in most industries has been defined as the number of products that can be sold divided by the number of products that can be potentially made. In the semiconductor industry, yield is represented by the functionality and reliability of integrated circuits produced on the wafer surfaces. The scope of this chapter is limited to the yield of front end processing. The YE chapter does not discuss manufacture line yield, assembly/packaging yield, and final test yield. Yield Enhancement (YE) for manufacturing of integrated devices addresses the improvement from research and development yield to mature yield. The YE chapter displays the current and future requirements for high yielding manufacturing of DRAM, MPU, and Flash. Furthermore, it has the objective to identify red bricks for manufacturing, and to discuss potential solutions.



During the manufacturing of integrated circuits yield loss is caused for example by defects, faults, process variations, and design. During processes as implantation, etching, deposition, planarization, cleaning, lithography, etc. failures responsible for yield loss are observed. Several examples of contaminations and mechanisms responsible for yield loss are listed in the following: a) Airborne Molecular Contamination (AMC) or particles of organic or inorganic matter caused by the environment or by the tools; b) process induced defects as scratches, cracks, and particles, overlay faults, and stress; c) process variations resulting, e.g., in differing doping profiles or layer thicknesses; d) the deviation from design, due to pattern transfer from the mask to the wafer, results in deviations and variations of layout and critical dimensions; and e) diffusion of atoms through layers and in the semiconductor bulk material.

The determination of defects and yield, and an appropriate yield to defect correlation are essential for yield enhancement. This correlation is of major importance, because not all defects change device properties or cause failure of devices or integrated circuits. Therefore, the yield enhancement chapter addresses not only the identification of tolerable contamination limits for processes and media, but also the tolerable budgets for particulate contamination of tools. The specification of tools for defect detection and classification of defects for root cause analysis addresses the technology requirements for detection and characterization of faults and failures.

The YE chapter has three focus topics: 'Yield Model and Defect Budget', 'Defect Detection and Characterization', and 'Wafer Environment Contamination Control'. These three topics crosscut front end process technology, interconnect processes, lithography, metrology, design, process integration, test, and facility infrastructures. Yield learning is discussed without identification of red bricks for manufacturing or potential solutions.

Yield Model and Defect Budget—The defect budget table has the objective to give tool suppliers control sizes at measurable defect sizes. At present, defect budget calculations use data from particle per wafer test surveys performed at integrated device manufacturers approx. 6 years ago. Due to the lack of current data, it was not possible to provide defect budget tables specifically addressing Flash production issues. The data for DRAM is assumed to be applicable as data for Flash, too. This defect budget data is the only publicly available source for integrated device manufacturers and suppliers to benchmark processes and to design semiconductor manufacturing equipment.

Defect Detection and Characterization—Physical device dimensions and corresponding defect dimensions continue shrinking, posing new challenges to detection and tolerable contamination. The wafer edges were identified to show significant impact on yield as well as process variations and design. Development of defect detection, defect review, and classification technologies showing highest sensitivity at high throughput is crucial for cost efficient manufacturing. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and work-in-progress data, will have to be developed to enhance root cause analysis and therefore enable rapid yield learning.

Wafer Environment Contamination Control—Order-of-magnitude improvements in process critical fluid and gas impurity levels are not considered to be necessary in the foreseeable future. New materials and their precursors, however, introduce challenges that require continuous study. Clarification of potential contamination from point-of-supply to point-of-process will define control systems necessary for delivered purity. There are several locations in the pathway from the original delivery package, i.e., the Point of Supply (POS) of a liquid or gas to the location where that material contacts the wafer, i.e., the Point of Process (POP), for ascertaining purity. This has led to a considerable amount of confusion and ambiguity in discussing the quality of process fluids, including the data found in Table YE9. Table YE1 summarizes the major fluid handling and/or measurement nodes found along the typical systems supplying process fluid. This table is an effort to create a common language for the discussion of attributes and requirements at these different node points. Further information regarding pathway nodes can be found in the supplementary materials and references, such as the Semiconductor Equipment and Materials International (SEMI) Standards.

Table YE1 Definitions for the Different Interface Points

	POS *Delivery Point of Gas/Chemical Supplier*	*POD* *Outlet of Central Facility System*	*POC* *Submain or VMB/VMP Take off Valve*	*POE* *Entry to Equipment or Sub Equipment*	*POU* *Entry to the Process Chamber*	*POP* *Contact with Wafer*
Interfaces	*SEMI Standards Focus Area*	*ITRS Factory Integration Facilities Group Focus Area*		*ITRS Factory Integration Equipment Group Focus Area*		*ITRS Front End Processes, Lithography, Interconnect TWG Focus Area*
Ultrapure water	Raw water	Outlet of final filtration in UPW plant	Outlet of submain take off valve	Inlet of wet bench or subequipment	Inlet of wet bench bath, spray nozzle, or connection point to piping, which is also used for other chemicals	Wafer in production
Process chemicals	Chemical drum/tote/bulk supply	Outlet of final filtration of chemical distribution unit	Outlet of VMB valve	Inlet of wet bench or intermediate tank	Inlet of wet bench bath or spray nozzle	Wafer in production
Specialty gases	Gas cylinder or bulk specialty gas systems	Outlet of final filtration of gas cabinet	Outlet of VMB valve	Inlet of equipment	Inlet of chamber (outlet of MFC)	Wafer in production
Bulk gases	Bulk gas delivered on site or gas generator	Outlet of final filtration/purification	Outlet of submain take off valve or VMB valve	Inlet of equipment/ subequipment	Inlet of chamber (outlet of MFC)	Wafer in production
Cleanroom and AMC	Outside air	Outlet of make-up air handling unit	Outlet of filters in cleanroom ceiling	Inlet to mini-environment or sub equipment for AMC, outlet of the tool filter for particles	Gas/air in vicinity to wafer/substrate	Wafer/substrate in production (AMC/ SMC)

POD—point of delivery POC—point of connection POE—point of entry POU—point of use VMB— valve manifold box VMP— valve manifold post UPW—ultra pure water MFC—mass flow controller AMC—airborne molecular contamination SMC—surface molecular contamination

DIFFICULT CHALLENGES

The difficult challenges for the Yield Enhancement chapter are summarized in Table YE2. The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership, and throughput were identified by the community as the most important challenge for yield enhancement. Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes defined by technology generations. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects. At the same time, a low Cost of Ownership (CoO) of the tools demands for high throughput of the inspection. This is in conflict with the issue of improving the signal-to-noise ratio. The key of successful inspection results are both a high sensitivity and a high capture rate for Defects of Interest (DOI).

The wafer edge and bevel control have a top priority on the list of key challenges. Defects and process problems around wafer edge and wafer bevel were identified to impact yield. It is a key challenge to find the appropriate inspection of wafer edge, bevel, and apex on the wafer front and backside. Defect inspection concepts or technologies are either under development or have to be further improved within the next few years.

Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

It is a challenge to effectively identify Systematic Mechanisms Limited Yield (SMLY). The tackling through logic diagnosis capability designed into products and systematically incorporated in the test flow is crucial. The irregularity of features makes logic areas very sensitive to SMLY such as patterning marginalities across the lithographic process window. Before reaching random-defect limited yields, the SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different Automatic Test Pattern Generation (ATPG) flows to accommodate, Automatic Test Equipment (ATE) architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die, and statistical aggregation of diagnosis results for building a layout-dependent systematic yield model.

The use of Scanning Electron Microscope (SEM) Energy Dispersive X-ray (EDX) for in-line chemical analysis has inherent limitations that are magnified, as defects of interest become smaller than 100 nm. Sampling volume is the primary limitation, followed by insufficient bonding information and possible e-beam damage. So tools/techniques are needed for elemental analysis in-line. The focus of required developments is on light elements and small amount of samples, as the? need to analyze smaller particle increases with shrinking geometries. This challenge is a crosscut of yield enhancement and metrology issues.

Table YE2 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Detection of multiple killer defect types / signal to noise ratio – The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership and throughput is required. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection particles at critical size may not exist. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Filtering and use of Automatic Defect Classification (ADC) is a potential solution for reduction of noise. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Wafer edge and bevel control and inspection — Defects and process problems around wafer edge and wafer bevel are identified to cause yield loss.	Find a for production suitable inspection of wafer edge, bevel and apex on the wafer front and backside.
Process stability versus absolute contamination level including the correlation to yield — Test structures, methods, and data are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect. Definition of maximum process variation (control limits).
Linking systematic yield loss to layout attributes — The irregularity of features makes logic areas very sensitive to Systematic Mechanisms Limited Yield (SMLY) such as patterning marginalities across the lithographic process window.	SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis run time per die. d) Statistical aggregation of diagnosis results for building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
High aspect ratio inspection (HARI) — The requirement for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost. Sensitivity requirements are leading to a dramatic increase of defect counts. The major challenge is to find the yield relevant defect types under the vast amount of defects.	Poor transmission of energy into bottom of via and back out to detection system. Rapid detection of defects at ½× Ground Rule (GR) associated with high-aspect-ratio contacts, vias, and trenches, and especially defects near or at the bottoms of these features Large number of contacts and vias per wafer
Difficult Challenges < 22 nm	*Summary of Issues*
In-line defect characterization and analysis — Alternatives to Energy Dispersive X-ray (EDX) analysis systems are required for in-line defect characterization and analysis for defects smaller 100 nm [1]. The focus has to be on light elements, small amount of samples due to particle size following the miniaturization, and microanalysis.	The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Development of test structures for new technology generations Address complex integration issues Model ultra-thin film integrity issues Improve scaling methods for front-end processes including increased transistor packing density

[1] Cross-link to Metrology chapter

YIELD LEARNING

INTRODUCTION

Yield learning is defined as the collection and application of process and wafer knowledge to improve device yield through the identification and resolution of systematic and random manufacturing events. Currently, yield learning is not described by technology requirements and potential solutions.

The semiconductor industry operates in an environment of exponentially decaying product prices, which put semiconductor manufacturers under time-to-market pressure. Profitability is derived from an early and successful yield ramp. The sooner a semiconductor manufacturer generates high yield, the earlier the manufacturer ramps to volume production, and the more profitable the semiconductor manufacturer's integrated circuit venture is likely to be. Improving the systematic component of yield, which frequently constrains yield in the early stages of manufacturing, can enhance profitability by enabling production at a point in time when chip prices are very high. Yield learning in the early stages of manufacturing may thus differ significantly from yield learning in the later stages of manufacturing. Beside this, any transition from one technology generation to the next is accompanied by a decrease in initial yield. Along with a technology generation change, for example, new materials or litho processes have to be introduced. These changes have to be implemented in parallel with new technology generations. Monitoring capabilities, inspection, metrology to properly cover the issues of latest technology generations cause enormous expenses and require concentrated research and development.

The key requirements for achieving highly sophisticated yield ramps include the detection of ever-shrinking, yield-detracting defects of interest, timely identification of root causes with growing data volume, chip complexity, process complexity, and improving the yield learning rate per each cycle of learning. With increasing process complexity and longer cycle times, tools and methods are needed to increase the number of yield learning cycles for each technology generation. Also, with continuous move to smaller features and longer processes, larger wafers, and new materials, numerous tools and methods are required to understand the entire yield detracting interactions.

DATA MANAGEMENT AND ADVANCED PROCESS CONTROL

Yield Management in a factory is going to be more closely coupled to data management. The rapid identification of defect and fault sources through integrated data management is the essence of rapid yield learning. Learning must proceed at an accelerated rate to maintain the yield ramp from introduction to maturity within the expected timeline, despite the growth in circuit complexity and the larger amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. This is getting significant importance now and in the future. In advanced manufacturing, any data generated could potentially hold the key to understanding and solving a yield issue that is identified at wafer sort, and needs to be recorded in an accessible way for the yield engineers, if required. Accessing the raw data in such a way as to generate meaningful correlations and results, is going to be a critical requirement for manufacturing. Data storage, and consequently the user interfaces to access this data, cannot be handled as an afterthought, if these factories are to be successful during the start up.

How the data from all generating sources of the factory is collected, stored, compiled, and accessed, is going to be crucial. In the face of this increased complexity, strategies and software methods for integrated data management have been identified as critical for maintaining productivity. Integrated device manufacturing must comprehend integrated circuit design, visible and non-visual defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the integrated device manufacturing system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. Integrated device manufacturing will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as Automatic Defect Classification (ADC) and Spatial Signature Analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information.

Implemented Advanced Process Control (APC) and Fault Detection and Classification (FDC) solutions will be of increasing importance. However, these control solutions will require tremendous data transport and data processing systems to support a full-scale implementation. Managing this, which must all be done in real time to benefit the factory, is a monumental undertaking. Maintaining standards, and open access systems allowing the best internal and external solutions to work together, is a must.

Down stream, or rather offline analysis of all the factories' data will also require new approaches, in addition to the existing ones, to fully grasp all information that can be correlated to yield. The greatest challenge to a comprehensive data management system required for yield learning is the ability to deal with and integrate data streams that are continuous, periodic, sporadic, and interval-based so they can all be linked through some common coupling system or user interface and be resolved by engineers. Keeping data aligned down to the wafer level or possibly to the die level, requires automated data matching techniques. It is also critical to have all data sources open and accessible by multiple user interfaces in order to maximize the effectiveness of yield engineering resources in finding problems. The best-of-breed data systems going forward will allow internal as well as multiple third party software solutions and Graphical User Interfaces (GUIs) to access the raw data formats, giving engineers the greatest flexibility in identifying and solving yield limiting issues. Barriers such as these must be eliminated.

The current practice in Data Management System (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient integrated device manufacturing is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect and fault sourcing capabilities, methods must be established for integrating workflow information (WIP) such as data determined with the DMS, particularly in commercial DMS systems. This will be important when addressing issues of advanced process and tool control beyond simple tool shutdown, e.g., lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time based data generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time based data that can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

FOUNDRY SPECIFIC YIELD LEARNING

Yield learning in a foundry differs substantially from yield learning in a fabrication facility that produces a few high-volume products. The high-volume producer will be constrained by batch yield in the early stages of manufacturing. Line yield will be the limiting factor once batch yield is high and volume production has begun. By contrast, a foundry may introduce a plethora of low-volume products into a relatively mature process on a routine basis. On occasion, one lot of wafers may provide a lifetime inventory of a particular design, which sells into a very short market window. A few chips of the design must exit the fabrication facility by a specific date. Due to this it is more important to get a initially defect free design of the integrated circuit, to get a initially flawless masks; and to obtain immediately a rapid cycle time through the line combined with a high line yield instead of a high batch yield.

DEFECTS

The various types of defects are described in the following.

Visible Defects—Tools are needed to detect, review, classify, analyze, and source continuously shrinking visible defects.

Non-visual Defects—Defects that cause electrical failure, but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-visual defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance or timing; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-visual defects) will become increasingly challenging. Techniques need to be developed that rapidly isolate failures and partition them into those caused by visible defects, non-visual defects, and parametric issues.

Parametric Defects—As minimum feature size decreases, so does the systematic mechanism limited yield (SMLY or Y_s). A major contributor to the Y_s component of yield is parametric variation within a wafer and wafer-to-wafer. Parametric

defects have traditionally been referred to as 'non-visual defects'. However, parametric defects require separation from the "non-visual defects" for rapid sourcing.

Electrical Faults—As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the pattern number of a wafer times the number of process steps, forming a defect sourcing complexity factor. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity. Moreover, the soft failures caused by sporadic cross-chip timing variation will require innovative new approaches to identify the root causes since these type of failures reside between a hard spot defect failure and consistent systematic failure issue.

NEEDED RESEARCH

The technology requirements and potential solutions described in 2007 call for continued cooperation between all stakeholders. For example, tool defect data is needed from semiconductor manufacturers and equipment manufacturers to specify design processes and the required equipment. A challenge for the future will be the detection of smallest defects at high throughput. Currently, there are no solutions known. This situation is also observed for control of critical dimensions with respect to the expected scaling down progress. As e-beam inspection is too slow, the development of scatterometry or other optical methodologies seems more promising. Furthermore, the future transition of metrology tools to inspection tools has to be performed as the yield issues get more and more complex related to the small feature sizes at atomic scale. 2007 the importance of flatness control of surfaces was recognized during cross technical working group discussions. The problem is solved for bare wafer inspection but not for pattern wafer inspection. Enormous R&D efforts are required to obtain solutions for the above mentioned red bricks within the next years.

In order to maintain manufacturing costs while improving yield, contamination control must focus on impact at the point of process. Innovative ideas, such as local removal of undesirable contamination from a re-usable process gas or fluid, must be examined. For new thin-film materials, understanding of purity requirements for deposition chemicals is needed.

Performance analysis indicates replacements for SEM/EDX that are also activated by e-beam illumination. Auger-electron spectroscopy can be used in the short-term to augment and replace SEM/EDX analysis because Auger-electron generation can only escape a target particle from a depth of approximately 3 nm or less. This property of Auger electrons specifically avoids a large sampling volume.

In the next two to three years, SEM/EDX can be further improved by more versatile e-beam acceleration control and X-ray detection methods. More sensitive detection methods include micro-calorimetry and WDS.

For elemental and bonding analysis of particles that are 60 nm diameter and below, Scanning Transmission Electron Microscopy (STEM) / Electron Energy Loss Spectroscopy (EELS) holds good promise for performance in the next 3 to 5 years. STEM/EELS has the capabilities to simultaneously capture elemental analysis while imaging the atomic structure of the constituents of a particle. Automated sample preparation must be improved and accelerated to achieve timely ultra-thin samples of 50-100 nm thickness. Aberrations of incoming and transmitted e-beams must be mitigated to enable the identification of constituent elements and compounds by the sizing of these constituents from images alone.

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

The overall die yield of an IC process can be described as a product of material-defect limited yield (Y_M), systematic mechanism limited yield (SMLY - Y_S) and random-defect limited yield (Y_R) (see Equation 1). Y_M separates yield degradation caused by defects embedded in a starting material from Y_S and/or Y_R during wafer fabrication. Further information about Y_M is described in FEP chapter. In most cases, Y_M is negligible. Y_S requires problem specific modeling and general formula to describe Y_S is currently unknown. A negative binomial yield model is adopted to calculate Y_R in YE chapter. A is the area of the device, D_0 is the electrical fault density, and α is the cluster factor. Parameters required to calculate D_0 are defined in Table YE3.

$$Y_{Die} = Y_M * Y_S * Y_R = Y_M * Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha} \quad (1)$$

$$PWP_n = PWP_{n-1} \times \frac{F_n}{F_{n-1} \left(\frac{S_{n-1}}{S_n} \right)^2} \quad (2)$$

Yield Model and Defect Budget technology references in Table YE4 and YE5 show maximum acceptable particle counts with equal or larger than critical defect size to achieve targeted yield in YE3. The random defect targets in Table YE4 and YE5 are based on predefined technology generations, using data collected by SEMATECH member companies on 164 tools, which are divided into 30 generic tool categories. Even with targets for both memory and logic products, rarely do actual user circuit line widths and areas match the ITRS technology assumptions. Although based on results of old studies (1997, 1999, and 2000) of Particles per Wafer Pass (PWP) levels at SEMATECH member companies, they are still useful as a reference for investigating defect reduction target toward new technology generation or discussing difference between several specific processes. In the Equation 2, PWP is the particles per wafer pass defect density per square meter, F is the average faults per mask level (determined by the random electrical fault density (D_0) divided by number of masks at a given technology generation), S is the minimum critical defect size, and n refers to the technology generation. This PWP equation simulates increase of critical area led by Moore's Law and shows PWP requirement of next technology generation. These targets were extrapolated from median PWP value per generic process tool type and then scaled to an MPU/ DRAM -generic process-flow, respectively. Note that the defect budget targets for all process steps include wafer-handling defectivity of the process tool and such embedded particle counts is automatically extrapolated with the other particle counts. A 10% wafer per lot sampling rate for inspection and measurement was assumed. Each entry in the PWP section of Table YE4 and YE5 refers to a generic tool type used in the process flow.

Table YE3 states the yield and the product maturity assumptions that were used in calculating electrical fault density values and PWP defect budget target values for MPUs /DRAMs/Flashs, respectively. These assumptions for the most part are as defined in the 2007 *Overall Roadmap Technology Characteristics* (ORTC). Cluster parameter value of 2 permits slight non-uniformity of fault distribution on wafers. YE4 presents the random PWP defect budget targets necessary to meet the stated assumptions for a cost-performance MPU as defined in the *ORTC Tables 1g and 1h*. This MPU is assumed to have a small L1 cache, but the device consists primarily of logic transistor functionality. With respect to MPUs, this analysis assumes that the process/design improvement target factor (*ORTC Tables 1g and 1h*) for each technology generation is met. Similarly, Table YE5 presents the random PWP budget targets necessary to meet the yield assumptions stated in Table YE3 for DRAMs/Flashs. The electrical fault density that is used to calculate faults per mask level (which is used as input to the PWP extrapolation equation) is based on only the periphery (logic/decoder) area of the chip. This periphery area can be calculated from cell array area at production defined in Table 1c and d. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM/Flash can implement redundancy to attain the overall yield target of 85%. DRAM/Flash chip size is enlarged at the timing of the new generation product introduction, and it shrinks during the period of the same generation product manufacturing as ORTC Tables 1c and d show. So, D_0 is calculated by adopting appropriate target yield value for each chip size to avoid unmeaning fluctuation of D_0 and PWP.

Besides continuous improvement in tool cleanliness, there are at least three other major challenges that must be addressed going forward in order to achieve acceptable yields:

1. The issues of particles and defects which are located not only at the front surface of a wafer but also at wafer bevel/edge portion and backside surface needs to be addressed.
2. With Systematic Mechanisms Limited Yield (SMLY) dominating the rate of yield learning, a concerted effort is required to understand, model, and eliminate SMLY detractors.
3. New methodology including APC should be evaluated the possibility of becoming a new variation/defect source.

Table YE3 Defect Budget Technology Requirement Assumptions

Product	*MPU*	*DRAM*	*Flash*
Yield Ramp Phase	*Volume Production*	*Volume Production*	*Volume Production*
$Y_{OVERALL}$	**75%**	**85%**	**85%**
Y_{RANDOM}	**83%**	**89.50%**	**89.50%**
$Y_{SYSTEMATIC}$	**90%**	**95%**	**95%**
$Y_{MATERIAL}$	**>99%**	**>99%**	**>99%**
Chip Size	**140mm^2**	**93mm^2**	**144mm^2**
Cluster Parameter	**2**	**2**	**2**

The current Defect Budgets tables are based on the survey that was carried out seven year ago, so that the color tiling is not done in this 2007 revision. It is believed that the defect budgets should be re-calculated by using the latest data that will be corrected through a new survey and procedure by next revision. The Yield Enhancement ITWG will survey semiconductor manufacturing companies for defect control limits of semiconductor manufacturing equipments.

Table YE4a Yield Model and Defect Budget MPU Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted) [A]	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Critical Defect Size (nm)	**34**	**29.5**	**26**	**22.5**	**20**	**18**	**16**	**14**	**12.5**
Chip Size (mm2) [B]	**140**	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**
Overall Electrical D0 (faults/m2) at Critical Defect Size Or Greater [C]	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**
Random Electrical D0 (faults/m2) [D]	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
Number of Mask Levels [E]	**33**	**35**	**35**	**35**	**35**	**35**	**37**	**37**	**37**
Random Faults/Mask	**42**	**40**	**40**	**40**	**40**	**40**	**38**	**38**	**38**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m2) for Generic Tool Type Scaled to 34 nm Critical Defect Size or Greater									
CMP clean	**343**	**256**	**204**	**162**	**128**	**102**	**76**	**61**	**48**
CMP insulator	**840**	**629**	**499**	**396**	**314**	**250**	**187**	**149**	**118**
CMP metal	**952**	**713**	**566**	**449**	**356**	**283**	**212**	**169**	**134**
Coat/develop/bake	**149**	**112**	**89**	**70**	**56**	**44**	**33**	**26**	**21**
CVD insulator	**744**	**557**	**442**	**351**	**279**	**221**	**166**	**132**	**105**
CVD oxide mask	**986**	**738**	**586**	**465**	**369**	**293**	**220**	**174**	**139**
Dielectric track	**235**	**176**	**140**	**111**	**88**	**70**	**52**	**42**	**33**
Furnace CVD	**421**	**315**	**250**	**198**	**157**	**125**	**94**	**74**	**59**
Furnace fast ramp	**380**	**285**	**226**	**179**	**142**	**113**	**85**	**67**	**53**
Furnace oxide/anneal	**245**	**183**	**145**	**115**	**92**	**73**	**55**	**43**	**34**
Implant high current	**329**	**246**	**195**	**155**	**123**	**98**	**73**	**58**	**46**
Implant low/medium current	**299**	**224**	**178**	**141**	**112**	**89**	**67**	**53**	**42**
Inspect PLY	**306**	**229**	**182**	**144**	**114**	**91**	**68**	**54**	**43**
Inspect visual	**328**	**246**	**195**	**155**	**123**	**97**	**73**	**58**	**46**
Lithography cell	**253**	**190**	**150**	**119**	**95**	**75**	**56**	**45**	**36**
Lithography stepper	**240**	**180**	**143**	**113**	**90**	**71**	**54**	**43**	**34**
Measure CD	**286**	**214**	**170**	**135**	**107**	**85**	**64**	**51**	**40**
Measure film	**245**	**183**	**145**	**115**	**92**	**73**	**55**	**43**	**34**
Measure overlay	**227**	**170**	**135**	**107**	**85**	**67**	**51**	**40**	**32**
Metal CVD	**449**	**336**	**267**	**212**	**168**	**133**	**100**	**79**	**63**
Metal electroplate	**230**	**172**	**137**	**109**	**86**	**68**	**51**	**41**	**32**
Metal etch	**1012**	**758**	**601**	**477**	**379**	**301**	**226**	**179**	**142**
Metal PVD	**512**	**384**	**304**	**242**	**192**	**152**	**114**	**91**	**72**
Plasma etch	**919**	**688**	**546**	**433**	**344**	**273**	**205**	**163**	**129**
Plasma strip	**419**	**314**	**249**	**198**	**157**	**125**	**93**	**74**	**59**
RTP CVD	**272**	**204**	**162**	**128**	**102**	**81**	**61**	**48**	**38**
RTP oxide/anneal	**178**	**133**	**106**	**84**	**67**	**53**	**40**	**32**	**25**
Test	**69**	**52**	**41**	**33**	**26**	**21**	**15**	**12**	**10**
Vapor phase clean	**634**	**474**	**376**	**299**	**237**	**188**	**141**	**112**	**89**
Wafer handling	**28**	**21**	**17**	**13**	**10**	**8**	**6**	**5**	**4**
Wet bench	**411**	**307**	**244**	**194**	**154**	**122**	**92**	**73**	**58**

Table YE4b Yield Model and Defect Budget MPU Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted) [A]	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5*	*4.5*
Critical Defect Size (nm)	**11.5**	**10**	**9**	**8**	**7**	**6.5**	**5.5**
Chip Size (mm2) [B]	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Overall Electrical D0 (faults/m2) at Critical Defect Size Or Greater [C]	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**	**2210**
Random Electrical D0 (faults/m2) [D]	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
Number of Mask Levels [E]	**37**	**39**	**39**	**39**	**39**	**39**	**39**
Random Faults/Mask	**38**	**36**	**36**	**36**	**36**	**36**	**36**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m2) for Generic Tool Type Scaled to 34 nm Critical Defect Size or Greater							
CMP clean	**38**	**29**	**23**	**18**	**14**	**11**	**9**
CMP insulator	**94**	**71**	**56**	**44**	**35**	**28**	**22**
CMP metal	**106**	**80**	**63**	**50**	**40**	**32**	**25**
Coat/develop/bake	**17**	**13**	**10**	**8**	**6**	**5**	**4**
CVD insulator	**83**	**63**	**50**	**39**	**31**	**25**	**20**
CVD oxide mask	**110**	**83**	**66**	**52**	**41**	**33**	**26**
Dielectric track	**26**	**20**	**16**	**12**	**10**	**8**	**6**
Furnace CVD	**47**	**35**	**28**	**22**	**18**	**14**	**11**
Furnace fast ramp	**42**	**32**	**25**	**20**	**16**	**13**	**10**
Furnace oxide/anneal	**27**	**21**	**16**	**13**	**10**	**8**	**6**
Implant high current	**37**	**28**	**22**	**17**	**14**	**11**	**9**
Implant low/medium current	**33**	**25**	**20**	**16**	**13**	**10**	**8**
Inspect PLY	**34**	**26**	**20**	**16**	**13**	**10**	**8**
Inspect visual	**37**	**28**	**22**	**17**	**14**	**11**	**9**
Lithography cell	**28**	**21**	**17**	**13**	**11**	**8**	**7**
Lithography stepper	**27**	**20**	**16**	**13**	**10**	**8**	**6**
Measure CD	**32**	**24**	**19**	**15**	**12**	**10**	**8**
Measure film	**27**	**21**	**16**	**13**	**10**	**8**	**6**
Measure overlay	**25**	**19**	**15**	**12**	**10**	**8**	**6**
Metal CVD	**50**	**38**	**30**	**24**	**19**	**15**	**12**
Metal electroplate	**26**	**19**	**15**	**12**	**10**	**8**	**6**
Metal etch	**113**	**85**	**67**	**53**	**42**	**34**	**27**
Metal PVD	**57**	**43**	**34**	**27**	**22**	**17**	**14**
Plasma etch	**102**	**77**	**61**	**49**	**39**	**31**	**24**
Plasma strip	**47**	**35**	**28**	**22**	**18**	**14**	**11**
RTP CVD	**30**	**23**	**18**	**14**	**11**	**9**	**7**
RTP oxide/anneal	**20**	**15**	**12**	**9**	**7**	**6**	**5**
Test	**8**	**6**	**5**	**4**	**3**	**2**	**2**
Vapor phase clean	**71**	**53**	**42**	**33**	**27**	**21**	**17**
Wafer handling	**3**	**2**	**2**	**1**	**1**	**1**	**1**
Wet bench	**46**	**34**	**27**	**22**	**17**	**14**	**11**

Notes for Tables YE4a and b:
[A] As defined in the ORTC Tables 1a and 1b.
[B] As defined in the ORTC Tables 1g and 1h.
[C] Based on assumption of 75% overall volume production yield.
[D] As shown in the ORTC Tables 5a and 5b. Based on assumption of 83% Random Defect Limited Yield (RDLY).
[E] As shown in the ORTC Tables 5a and 5b.

Table YE5a Yield Model and Defect Budget DRAM/Flash Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
Critical Defect Size (nm)	**34**	**29.5**	**26**	**22.5**	**20**	**18**	**16**	**14**	**12.5**
DRAM Product Table									
Chip Size (mm^2) [B]	**93**	**74**	**59**	**93**	**74**	**59**	**93**	**74**	**59**
Cell Array Area (%) at Production [B]	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Non-core Area (mm^2)	**41**	**33**	**26**	**41**	**33**	**26**	**41**	**33**	**26**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**
Random Electrical D_0 (faults/m^2) [D]	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**
Number of Mask Levels [E]	**24**	**24**	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**116**	**116**	**107**	**107**	**107**	**107**	**107**	**107**	**107**
DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to -40 nm Critical Defect Size or Greater									
CMP clean	**1329**	**1056**	**773**	**614**	**487**	**387**	**307**	**244**	**193**
CMP insulator	**1027**	**815**	**597**	**474**	**376**	**299**	**237**	**188**	**149**
CMP metal	**1579**	**1254**	**919**	**729**	**579**	**459**	**365**	**289**	**230**
Coat/develop/bake	**409**	**325**	**238**	**189**	**150**	**119**	**94**	**75**	**59**
CVD insulator	**1139**	**904**	**662**	**526**	**417**	**331**	**263**	**209**	**166**
CVD oxide mask	**1400**	**1112**	**815**	**647**	**513**	**407**	**323**	**257**	**204**
Dielectric track	**574**	**456**	**334**	**265**	**210**	**167**	**132**	**105**	**83**
Furnace CVD	**785**	**624**	**457**	**363**	**288**	**228**	**181**	**144**	**114**
Furnace fast ramp	**740**	**587**	**430**	**341**	**271**	**215**	**171**	**136**	**108**
Furnace oxide/anneal	**591**	**469**	**344**	**273**	**217**	**172**	**136**	**108**	**86**
Implant high current	**688**	**546**	**400**	**317**	**252**	**200**	**159**	**126**	**100**
Implant low/medium current	**655**	**520**	**381**	**303**	**240**	**191**	**151**	**120**	**95**
Inspect PLY	**898**	**713**	**522**	**415**	**329**	**261**	**207**	**165**	**131**
Inspect visual	**926**	**736**	**539**	**428**	**339**	**270**	**214**	**170**	**135**
Lithography cell	**768**	**610**	**447**	**355**	**281**	**223**	**177**	**141**	**112**
Lithography stepper	**510**	**405**	**297**	**235**	**187**	**148**	**118**	**93**	**74**
Measure CD	**767**	**609**	**446**	**354**	**281**	**223**	**177**	**140**	**112**
Measure film	**721**	**572**	**419**	**333**	**264**	**210**	**166**	**132**	**105**
Measure overlay	**701**	**557**	**408**	**324**	**257**	**204**	**162**	**128**	**102**
Metal CVD	**722**	**573**	**420**	**333**	**265**	**210**	**167**	**132**	**105**
Metal electroplate	**548**	**435**	**319**	**253**	**201**	**159**	**127**	**100**	**80**
Metal etch	**1334**	**1060**	**776**	**616**	**489**	**388**	**308**	**245**	**194**
Metal PVD	**793**	**629**	**461**	**366**	**290**	**231**	**183**	**145**	**115**
Plasma etch	**1414**	**1123**	**823**	**653**	**518**	**411**	**326**	**259**	**206**
Plasma strip	**1083**	**860**	**630**	**500**	**397**	**315**	**250**	**198**	**158**
RTP CVD	**706**	**561**	**411**	**326**	**259**	**205**	**163**	**129**	**103**
RTP oxide/anneal	**516**	**410**	**300**	**238**	**189**	**150**	**119**	**95**	**75**
Test	**100**	**80**	**58**	**46**	**37**	**29**	**23**	**18**	**15**
Vapor phase clean	**1503**	**1193**	**874**	**694**	**551**	**437**	**347**	**275**	**219**
Wafer handling	**42**	**33**	**24**	**19**	**15**	**12**	**10**	**8**	**6**
Wet bench	**1073**	**852**	**624**	**495**	**393**	**312**	**248**	**197**	**156**

Table YE5a Yield Model and Defect Budget DRAM/Flash Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
Critical Defect Size (nm)	**34**	**29.5**	**26**	**22.5**	**20**	**18**	**16**	**14**	**12.5**
Flash Product Table									
Chip Size (mm^2) [B]	**143.96**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**
Cell Array Area (%) at Production [B]	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**
Non-core Area (mm^2)	**46**	**32**	**26**	**41**	**32**	**26**	**41**	**32**	**26**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**
Random Electrical D_0 (faults/m2) [D]	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**
Number of Mask Levels [E]	**24**	**24**	**24**	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**104**	**104**	**104**	**96**	**96**	**96**	**96**	**96**	**96**

Table YE5b Yield Model and Defect Budget DRAM/Flash Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
Critical Defect Size (nm)	**11.5**	**10**	**9**	**8**	**7**	**6.5**	**5.5**
DRAM Product Table							
Chip Size (mm^2) [B]	**93**	**74**	**59**	**93**	**74**	**59**	**93**
Cell Array Area (%) at Production [B]	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Non-core Area (mm^2)	**41**	**33**	**26**	**41**	**33**	**26**	**41**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**	**4145**
Random Electrical D_0 (faults/m^2) [D]	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**	**2793**
Number of Mask Levels [E]	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**107**	**107**	**107**	**107**	**107**	**107**	**107**
DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to -40 nm Critical Defect Size or Greater							
CMP clean	**153**	**122**	**97**	**77**	**61**	**48**	**38**
CMP insulator	**119**	**94**	**75**	**59**	**47**	**37**	**30**
CMP metal	**182**	**145**	**115**	**91**	**72**	**57**	**46**
Coat/develop/bake	**47**	**37**	**30**	**24**	**19**	**15**	**12**
CVD insulator	**131**	**104**	**83**	**66**	**52**	**41**	**33**
CVD oxide mask	**162**	**128**	**102**	**81**	**64**	**51**	**40**
Dielectric track	**66**	**53**	**42**	**33**	**26**	**21**	**17**
Furnace CVD	**91**	**72**	**57**	**45**	**36**	**29**	**23**
Furnace fast ramp	**85**	**68**	**54**	**43**	**34**	**27**	**21**
Furnace oxide/anneal	**68**	**54**	**43**	**34**	**27**	**22**	**17**
Implant high current	**79**	**63**	**50**	**40**	**31**	**25**	**20**
Implant low/medium current	**76**	**60**	**48**	**38**	**30**	**24**	**19**
Inspect PLY	**104**	**82**	**65**	**52**	**41**	**33**	**26**
Inspect visual	**107**	**85**	**67**	**53**	**42**	**34**	**27**
Lithography cell	**89**	**70**	**56**	**44**	**35**	**28**	**22**
Lithography stepper	**59**	**47**	**37**	**29**	**23**	**19**	**15**
Measure CD	**88**	**70**	**56**	**44**	**35**	**28**	**22**

Table YE5b Yield Model and Defect Budget DRAM/Flash Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
Critical Defect Size (nm)	**11.5**	**10**	**9**	**8**	**7**	**6.5**	**5.5**
DRAM Product Table							
Measure film	**83**	**66**	**52**	**42**	**33**	**26**	**21**
Measure overlay	**81**	**64**	**51**	**40**	**32**	**26**	**20**
Metal CVD	**83**	**66**	**53**	**42**	**33**	**26**	**21**
Metal electroplate	**63**	**50**	**40**	**32**	**25**	**20**	**16**
Metal etch	**154**	**122**	**97**	**77**	**61**	**49**	**39**
Metal PVD	**91**	**73**	**58**	**46**	**36**	**29**	**23**
Plasma etch	**163**	**130**	**103**	**82**	**65**	**51**	**41**
Plasma strip	**125**	**99**	**79**	**62**	**50**	**39**	**31**
RTP CVD	**81**	**65**	**51**	**41**	**32**	**26**	**20**
RTP oxide/anneal	**60**	**47**	**38**	**30**	**24**	**19**	**15**
Test	**12**	**9**	**7**	**6**	**5**	**4**	**3**
Vapor phase clean	**173**	**138**	**109**	**87**	**69**	**55**	**43**
Wafer handling	**5**	**4**	**3**	**2**	**2**	**2**	**1**
Wet bench	**124**	**98**	**78**	**62**	**49**	**39**	**31**
Flash Product Table							
Chip Size (mm2) [B]	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**
Cell Array Area (%) at Production [B]	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**
Non-core Area (mm2)	**41**	**32**	**26**	**41**	**32**	**26**	**41**
Overall Electrical D0 (faults/m2) at critical defect size or greater [C]	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**	**3716**
Random Electrical D0 (faults/m2) [D]	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**	**2503**
Number of Mask Levels [E]	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**96**	**96**	**96**	**96**	**96**	**96**	**96**

Notes for Tables YE5a and b:
[A] As defined in the ORTC Tables 1a and 1b.
[B] As defined in the ORTC Tables 1c and 1d.
[C] Based on assumption of 89.5% (RDLY).
[D] As shown in the ORTC Tables 5a and 5b. Based on assumption of 89.5% RDLY.
[E] As shown in the ORTC Tables 5a and 5b.

DEFECT DETECTION AND CHARACTERIZATION

The ability to detect in-line yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production-process research and development, yield ramp, and volume production — broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabrication facilities begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the integrated device manufacturers just in time for each phase of the process cycle. Tools that meet the requirements for process research and development are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate yield ramp must be available several months before production begins. Finally, the ability to monitor excursions at a technology generation is needed when the product hits high yield levels.

Technology requirements are presented by three tables covering the needs for: a) patterned wafer - and e-beam inspection; b) unpatterned wafer inspection, macro and bevel inspection and defect review; and c) ADC. The complexity of processes and integration schemes for manufacturing of integrated devices requires intense defect inspection for process and tool monitoring. Unpatterned wafer inspection is extensively used for tool qualification. Both defect inspections use subsequent defect review for root cause analysis, posing challenging requirements to the accuracy of defect coordinates. Furthermore, the cleanliness of inspection tools is of increasing importance. Due to the observed impact of defects on wafer bevel and edge on yield, backside and bevel wafer inspection needs a defect review possibility in order to be used to the full extent. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is inspected on e-beam tools which find their application also in detection of small defects.

One of the major challenges is to get to the defect of interest. Therefore, the signal-to-noise ratio is an important criterion for all inspection tools. The more nuisance defects are captured the less valuable the results are as defects of interest might not be recognized even after intense review. Furthermore, an efficient separation of DOI from noise will enable an increased throughput of the subsequent review.

The inspection of bevel, apex, and wafer edge on the top and bottom on multilayer product wafers becomes a big challenge as increasingly more defects or process problems have their origin in those areas of the wafer. Important criteria, besides coverage of all areas, sensitivity, and speed, are the ADC and the optical review capability on the tool as well as a standard result file allowing SEM review.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside inspection requirements are based on the Lithography chapter technology requirements table, and also ask for specification of tool cleanliness of the inspection tools themselves, this was introduced

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers, defects that can not be detected with conventional optical technologies, is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and the back end of the process. Macro defects impacting large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved matching the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology generation.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The cost of the investment, fab space occupied, and the throughput of defect detection tools are major contributors to their cost of ownership (CoC). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table YE6, YE7, and YE8 have been stipulated on the basis of detecting accurately sized PolyStyrene Latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pits pattern flaws, surface roughness, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

Table YE6a Defect Inspection on Pattern Wafer Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*									
Process R&D at 300 cm^2/hr (0,4 "300 mm wafer"/hr)	27	22.5	20	18	16	14	12.5	11	10
Process R&D at 300 cm2/hr with 50 % Capture rate [Q]	16.2	13.5	12	10.8	9.6	8.4	7.5	6.6	6
Yield ramp at 1200 cm^2/hr (1,7 "300 mm wafer"/hr)	43.2	36	32	28.8	25.6	22.4	20	17.6	16
Volume production at 3000 cm^2/hr (4,3 "300 mm wafer"/hr)	54	45	40	36	32	28	25	22	20
Speed [wafer/hrs]at volume production (1xDR) on Brigthfield tools [R]	4	4	5	5	5	6	6	6	7
Tool matching (% variation tool to tool) [C]	10	10	5	5	5	5	5	5	5
Defect coordinate precision [µm] note	2.275	1.995	1.75	1.575	1.4	1.225	1.12	0.98	0.875
Defect coordinate precision [µm] note	1.89	1.575	1.4	1.26	1.12	0.98	0.875	0.77	0.7
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	2	2
Cost of ownership ($/$cm^2$)	0.08	0.08	0.08	0.08	0.08	0.08	0.08	0.08	0.08
*E-beam inspection Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[D, E]*									
Sensitivity for voltage contrast application without speed requirement (nm)	65	57	50	45	40	35	32	28	25
Sensitivity for physical defect detection (nm)	27	22.5	20	18	16	14	12.5	11	10
speed for voltage contrast applications	50	100	100	100	300	300	300	300	500
Speed for physical defect detection	10	50	50	50	50	50	50	100	100
CoO HARI ($/$cm^2$)	0.388	0.388	0.388	0.388	0.388	0.388	0.388	0.388	0.388
Backside cleaniness for inspection tools									
Critical Defect Size (µm) for large defects	50	20	20	20	10	10	10	10	10
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for large defects	<1	<1	<1	<1	<1	<1	<1	<1	<1
Critical Defect Size (nm) for total defects	325	285	250	225	200	175	160	140	125
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for total defects	3500	2500	2500	2500	2500	2500	2500	2500	2500

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table YE6b Defect Inspection on Pattern Wafer Technology Requirements —Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*							
Process R&D at 300 cm^2/hr (0,4 "300 mm wafer"/hr)	9	8	7	6.5	5.5	5	4.5
Process R&D at 300 cm2/hr with 50 % Capture rate [Q]	5.4	4.8	4.2	3.9	3.3	3	2.7
Yield ramp at 1200 cm^2/hr (1,7 "300 mm wafer"/hr)	14.4	12.8	11.2	10.4	8.8	8	7.2
Volume production at 3000 cm^2/hr (4,3 "300 mm wafer"/hr)	18	16	14	13	11	10	9
Speed [wafer/hrs]at volume production (1xDR) on Brigthfield tools [R]	7	7	7	7	7	7	7
Tool matching (% variation tool to tool) [C]	5	5	5	5	5	5	5
Defect coordinate precision [µm] note	0.77	0.7	0.63	0.56	0.49	0.455	0.385
Defect coordinate precision [µm] note	0.7	0.63	0.56	0.49	0.455	0.35	0.315
Wafer edge exclusion (mm)	2	2	2	2	2	2	2
Cost of ownership ($/$cm^2$)	0.08	0.08	0.08	0.08	0.08	0.08	0.08
*E-beam inspection Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[D, E]*							
Sensitivity for voltage contrast application without speed requirement (nm)	22	20	18	16	14	13	11
Sensitivity for physical defect detection (nm)	10	9	8	7	6.5	5	4.5
speed for voltage contrast applications	500	500	500	500	500	500	500
Speed for physical defect detection	100	100	100	100	100	100	100
CoO HARI ($/$cm^2$)	0.388	0.388	0.388	0.388	0.388	0.388	0.388
Backside cleaniness for inspection tools							
Critical Defect Size (µm) for large defects	10	10	10	10	10	10	10
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for large defects	<1	<1	<1	<1	<1	<1	<1
Critical Defect Size (nm) for total defects	110	100	100	100	100	100	100
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for total defects	2500	2500	2500	2500	2500	2500	2500

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

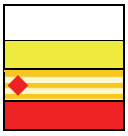


Table YE7a Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements —Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*									
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]									
Films (like Poly Si and metal films)	64.8	54	48	43.2	38.4	33.6	30	26.4	24
Bare silicon	28.5	25.5	20	18	16	14	12.5	11	10
Throughput at highest sensitivity for all layers [wfr/hrs]	60	70	70	80	80	90	90	100	100
Wafer backside (defect size, nm) [H]	325	285	250	225	200	175	160	140	125
CoO ($/cm^2)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.004
Wafer edge exclusion (mm)	2	2	2	2	2	2	2	2	2
Wafer inspection on multilayer product wafer of top and bottom bevel, APEX and 3 mm wafer edge exclusion[U]									
PSL spheres at 90% capture rate, Equivalent sensitivity (nm) [N, O]									
Sensitivity [nm] without speed requirement at 50 % capture rate	325	225	200	180	160	140	125	110	100
Sensitivity[nm] at 100 wafer/hrs	2000	2000	1250	1125	1000	875	800	700	625
Defect classes, ADC [P]	5	5	10	10	10	10	10	10	10
Toolmatching (%variation tool to tool)	10%	10%	10%	10%	10%	5%	5%	5%	5%
CoO [$/300 mm wafer]	1	0.9	0.8	0.8	0.8	0.8	0.8	0.8	0.7
*Macro Inspection on product wafer, PSL Spheres * at 90% Capture, Equivalent Sensitivity (µm)*									
Sensitivity [µm]	5	5	3	3	3	3	2	2	2
speed [w/hrs] at sensitivity	150	150	150	170	170	170	170	200	200
ADC: nr of defect types automated classified	3	3	5	5	10	10	10	10	10
Tool matching (% variation tool to tool) [C]	10	10	10	10	10	10	10	10	10
Backside cleaniness for inspection tools									
Critical Defect Size (µm) for large defects	50	20	20	20	10	10	10	10	10
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for large defects	<1	<1	<1	<1	<1	<1	<1	<1	<1
Critical Defect Size (nm) for total defects	325	285	250	225	200	175	160	140	125
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for total defects	3500	2500	2500	2500	2500	2500	2500	2500	2500

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

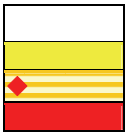


Table YE7b Defect Inspection on Unpatterned Wafers: Macro and Bevel Inspection Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*							
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]							
Films (like Poly Si and metal films)	21.6	19.2	16.8	15.6	13.2	12	10.8
Bare silicon	10	9	8	7	6.5	5	4.5
Throughput at highest sensitivity for all layers [wfr/hrs]	110	110	120	120	130	130	130
Wafer backside (defect size, nm) [H]	110	100	90	80	70	65	55
CoO ($/cm^2)	0.004	0.004	0.004	0.004	0.004	0.004	0.004
Wafer edge exclusion (mm)	2	2	2	2	2	2	2
Wafer inspection on multilayer product wafer of top and bottom bevel, APEX and 3 mm wafer edge exclusion[U]							
PSL spheres at 90% capture rate, Equivalent sensitivity (nm) [N, O]							
Sensitivity [nm] without speed requirement at 50 % capture rate	90	80	70	65	55	50	45
Sensitivity[nm] at 100 wafer/hrs	550	500	450	400	350	300	250
Defect classes, ADC [P]	10	10	10	10	10	10	10
Toolmatching (%variation tool to tool)	5%	5%	5%	5%	5%	5%	5%
CoO [$/300 mm wafer]	0.7	0.7	0.7	0.7	0.7	0.7	0.7
*Macro Inspection on product wafer, PSL Spheres * at 90% Capture, Equivalent Sensitivity (µm)*							
Sensitivity [µm]	1	1	1	1	1	1	1
speed [w/hrs] at sensitivity	200	200	200	200	200	200	200
ADC: nr of defect types automated classified	10	10	10	10	10	10	10
Tool matching (% variation tool to tool) [C]	10	10	10	10	10	10	10
Backside cleaniness for inspection tools							
Critical Defect Size (µm) for large defects	10	10	10	10	10	10	10
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for large defects	<1	<1	<1	<1	<1	<1	<1
Critical Defect Size (nm) for total defects	110	100	100	100	100	100	100
Backside Particle per Wafer pass (PWP) Budget (defects/m^2) for total defects	2500	2500	2500	2500	2500	2500	2500

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

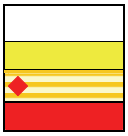


Table YE8a Defect Review and Automated Defect Classification Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*35*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
Defect Review (Patterned Wafer)									
Coordinate accuracy (nm) at resolution [J]	650	570	500	450	400	350	320	280	250
Redetection: minimum defect size (nm) [S]	26	22.8	20	18	16	14	12.8	11.2	10
Number of defect types [L]	10	10	10	10	10	10	10	10	10
Speed (defects/hours) w ADC [T]	720	720	720	720	720	720	720	720	720
Speed w/elemental (defects/hours)	360	360	360	360	360	360	360	360	360
Number of defect types (inline ADC) [M]	10	10	10	10	10	10	10	10	10

Table YE8b Defect Review and Automated Defect Classification Technology Requirements—Long-term Years

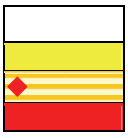
Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
Defect Review (Patterned Wafer)							
Coordinate accuracy (nm) at resolution [J]	220	200	180	160	140	130	110
Redetection: minimum defect size (nm) [S]	8.8	8	7.2	6.4	5.6	5.2	4.4
Number of defect types [L]	10	10	10	10	10	10	10
Speed (defects/hours) w ADC [T]	720	720	720	720	720	720	720
Speed w/elemental (defects/hours)	360	360	360	360	360	360	360
Number of defect types (inline ADC) [M]	10	10	10	10	10	10	10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Tables YE6, YE7, YE8 a and b:

[A] Patterned wafer scan speed is required to be at least 300 cm^2 /hour for process R&D mode, 1,200 cm^2 /hour for yield ramp mode, and, at least, 3,000 cm^2 /hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement.

[B] Patterned wafer nuisance defect rate shall be lower than 5% in all process phases. False counts in the R&D phase less than 5%, and less than 1% in the yield ramp and volume production phase. Nuisance is defined as an event indicated and a defect is present, just not the type of interest. These maybe significant and could be studied at a later date. The defect classifier must consider the defect type and assign significance. False is defined at an event is indicated, but no defect can be seen using the review optics path of the detection tool, which supports recipe setup validation.)

[C] Metric % variation tool-to-tool in number of non-matching defects/total number of defects from standard tool.

Procedure: Recipe sensitivity set on first (standard) tool with false <5. Transfer this recipe without changes and perform ten runs with a wafer containing a minimum of 30 defects.

[D] High Aspect Ration is defined as for contacts 15:1.

[E] HARI defects are already considered "killers" at any process stage, but defined at the contact/via levels for full feature size capture. Hence, minimum defect sensitivity was stipulated as 1.0× technology generation at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more is the model to be detected. If in the future, detection tools can determine size, shape, or remaining material on the order of 0.3× technology generation, this will more adequately match known experience for resistance changes. Scan speed for HARi tools have been broken out into process verification and volume production types. Process verification usually refers to SEM-type tools (but not necessarily in the future) and includes voltage contrast capability. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435.

F] Un-patterned wafer defect detection tools will be required to scan 200 (300 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually.

[G] Must meet haze and crystal originated pit (COP) requirements specified in the Front End Processes chapter Starting Materials section of the Roadmap.

[H] Sensitivity requirement agreed with Lithography TWG. Might need to be revised with implementation of EUV lithography. Optical review capability of backside results is a requirement.

[I] Resolution of defect review is defined as 0.05 × Sensitivity at pattern inspection R&D.

[J] Driver is the defect size.

[K] Assumptions: 5,000 wafer starts per week, defects per wafer based on surface preparation at front end of line (FEOL), leading to defects per hour that need review, 100% ADC.

[L] Defect classifications need to meet: Repeatability 95 %, Accuracy 90 %, Purity 90 %.

[M] Defect classifications need to meet: Repeatability 95 %, Accuracy 80 %, Purity 80 %.

[N] Review capability: optical review capability at the tool but also offline SEM review is necessary.

[O] An industry standard result file is needed also for SEM review capability. Result file containing coordinate and angular information to also allow prior level subtraction, also add images from tool in result file.

[P] The first three ADC classes to start with: chips, surface particle large, surface particle small. The fourth ADC class should be blisters.

[Q] 50 % capture rate is calculated with 10 scans

[R] Speed is considered the time needed for full wafer scan including load and unload

[S] Redetection at minimum defect size at a minimum capture rate of 50 %

[T] Speed is considered the time needed including load and unload for review of 2 wafer / lot and 50 defects / wafer

[U] Inspection of full and partial printed chips, as well as chip free area. A size binning of defects is necessary

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table YE9.

Wafer environment control—The wafer environment control includes the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in PODs/FOUPs. As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to effective wafer and reticle isolation deployment.

Airborne molecular contamination—Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of AMC. Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden. Acid vapors in the air have been linked with the release of boron from HEPA filters and the impact of amines on Deep UltraViolet (DUV) photoresists are well known examples of AMC affecting wafer processing. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation in the cleanroom to measure AMC at the part per trillion level (by volume). Surface Acoustic Wave (SAW) devices and Atmospheric Pressure Ionized Mass Spectroscopy (APIMS) have been used to measure low level AMC, but low cost, routine monitoring may be required as devices approach molecular dimensions, see also *AMC monitoring programs*. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front-end processes. Although numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures, the need for nitrogen purging of wafer environment enclosures is being investigated for critical process steps. Not all process steps will be impacted by AMC. For example, future lithography systems will require vacuum processing and are not expected to impose new AMC control requirements in the cleanroom environment. The potential for AMC to impact new processes should be considered in all process integration studies. A detailed definition of critical impurities is provided in *AMC definitions*.

Temperature and humidity specifications have been added to Table YE9 this year for the most critical applications, e.g. lithography for several reasons.

1) The strictest requirements are driven by the lithography process, which is protected by an environmental chamber. The specifications in the Table YE9 reflect the inlet condition to each individual environmental

chamber. Here especially, the maximum variation over time is important, which the environmental chamber must be able to compensate. At the POP lower specifications down to ± 0.03 K are maintained.

2) But also in the coater/developer track temperature and humidity specifications must be guaranteed to maintain stable conditions for the resist.

3) The temperature variation is also important for the stepper itself, since minor temperature variations can result due to different thermal extension coefficients in misalignments between the stepper foundation/wafer stage and the lense column. Steppers need up to a week to stabilize after a temperature change.

4) Another critical requirement is driven by metrology equipment which depend either on laser beams (the air density depend on temperature and humidity) and by measurements where misalignments are important.

The temperature and humidity stability over different locations within critical areas is less important. Also in other areas temperature and humidity variations shall be controlled to less strict limits since it may have an impact on the surface (native oxide formation) or alignments. Some companies choose not to have different specifications for critical and non-critical areas to allow flexibility in the cleanroom use as well as simplify the temperature and humidity control and the associated segregation.

These specifications are variational specifications and set points can be chosen in a wide range. A recent benchmarking study between fabs has shown values between 19.5 and 24°C for temperature and values between 35% and 48% for the relative humidity. There are different drivers for that. The temperature set point is normally chosen based on comfort level and climatic conditions and the resulting energy consumption. The set point for relative humidity takes into consideration higher electrostatic charges at lower humidity and higher corrosion/native oxide formation at higher relative humidity. Capacity of AMC filters also depends on the humidity.

Another process area with temperature/humidity control as well as AMC control requirements is the location of the lithography excimer lasers, if they are installed in the subfab and not in the main cleanroom.

Process critical materials—Additional experimental investigation is required to support our understanding of impurity specifications in novel materials, such as Cu plating solutions, CMP slurries, or chemical vapor deposition (CVD) precursors to high/low-κ dielectrics and other thin film materials. For many years the critical particle size concept was used to judge whether particles will have an impact on yield or not. This concept has to be rethought since particles do not impact the process yield alone by their physical size but also by their chemical composition. The allowable particle concentration thereby depend also on product parameters such as cell size and have therefore been aligned with the particle concentration on the surface as derived by the FEP surface preparation group calculation model.

Ultrapure water—UPW is generally considered to be 18.2 MegΩ-cm resistivity at 25°C, low ppt in metals, less than 50 ppt in inorganic anions and ammonia, less than 0.2 ppb in organic anions, and below 1 PPB total oxidizable carbon (TOC) and silica (dissolved and colloidal). Particle levels are reduced using the best available ultrafiltration technology. Bacteria are present, on surfaces and to a lesser degree in the bulk fluid, and controlled to very low levels, typically <1 colony forming unit (cfu)/L in the bulk fluid. The 2007 Roadmap values, presented in Table YE9, represent typical UPW quality currently in use to manufacture the most advanced semiconductor devices and have been validated by benchmark surveys. More stringent criteria beyond 2007 are only projected where there is evidence that manufacturing process requirements demand improvements. UPW is generally the cleanest fluid available in the manufacturing process. As such there is not much data to suggest that it is has a significant negative impact on process yields. For this reason the UPW Roadmap is relatively stable over time. The UPW group is evaluating Gibbs Free Energy deposition models to indicate the potential for critical elements to deposit on the wafer under various process conditions. *A discussion of the UPW requirements can be found in the UPW supplemental material online*.

The UPW section of Table YE9 considers some parameters as process variables rather than contaminants. It is clear that the stability of the wafer environment can be as important as the level of contaminants present for some parameters. Some semiconductor manufactures now treat Dissolved Oxygen (DO) in this way, while others still consider it a contaminant Stability of temperature and pressure continue to be important, the former being critically important for immersion lithography.

Contaminant quality levels in UPW must be viewed in the context of where that quality is required and where it is to be measured. Points of measurement are referred to as the POD, POE, and POU. The POD is just after the last treatment step of the UPW system, the POE is at the tool connection point, and the POU is in the tool. Refer to Table YE1 for detailed description of sample locations. The 2007 Roadmap defines UPW quality at the POE in Table YE9. UPW quality can change between these three locations, especially between the POE and POU, and requires particular attention to maintain quality throughout. In addition sampling techniques are critical to ensure accurate analytical results. As UPW specifications shift from the POE to the POU, sampling methods will become more difficult and costly. Most benchmark

data has been collected at POD or POE and is the basis for parameters in Table YE9. A benchmark of POE and POU values was conducted in 2007 however results were not received in time for publishing. These results will be considered for the 2008 update. Where contaminant levels have been extended to POU this has been done based on engineering judgment assuming the semiconductor processing tool is well designed and operated with regard to maintaining fluid purity in accordance with applicable SEMI standards.

Ozonated UPW is not addressed in this Roadmap as it is considered a dilute process chemistry that is generally applied at the process tool. At the time of printing immersion lithography posed no special requirements for UPW other than possible degasification and additional closer temperature control, which would be done at the process tool.

Immersion Lithography processes which use UPW as the lens fluid is very sensitive to temperature and hazing of the lens. Tool manufacturers are interested in minimizing all potential sources of organics. Accelerated hazing tests are being conducted to see if the organic species known and thought to be in UPW can contribute to lens hazing. Results were not available at the time of printing but will be considered in the 2008 update.

UPW recycle—To promote resource optimization UPW use efficiency improvements are typically required. Cost effective technologies, including treatment and analytical methods, are needed to ensure UPW quality is maintained, as more water is recycled back through the system. A well-implemented recycle program has been shown to improve final water quality by using a "cleaner" stream for the feed, in addition to providing other benefits. Further information and requirements can be found in the *Environmental, Safety, and Health* chapter.

UPW measurement methodologies—General test methodologies for monitoring contaminants in UPW are indicated in the Figure YE1 below. Over the past few years the ITRS UPW team has benchmarked many advanced UPW systems to determine water quality. The 2007 benchmark effort includes Non Volatile Residue Monitoring and particles by SEM with a novel sample collection method. Past benchmark efforts have identified the inadequacy of some measurement methodologies to quantify contaminants in UPW. The following analytical methods are not sensitive to present levels of contamination in UPW: resistivity, total oxidizable carbon, inorganic anions, and organic ions, as well as some organic species. Speciation of organics has been limited by these methods. Sensitivity of the following methods is presently adequate: viable bacteria, dissolved gasses, and metals. While particle measurement is generally not adequately sensitive at the critical dimension it may be technically sound to extrapolate particle size and concentration data to the critical dimension. Benchmarking has shown this size distribution to be unique to a particular UPW system and/or measurement technique. Each user of the Roadmap is advised to determine a particle distribution for their fab empirically. Benchmarking has indicated a log: log distribution relationship with slopes from -1 to -5. A more complete treatment of *UPW concerns* is covered in the supplemental material of this chapter online, where also a *conversion tool* can be found.

Parameter	Measured (POD/POC)	Test Method
Resistivity	Online	Electric cell
Viable bacteria	Lab	Incubation
TOC	Online	Conductivity/CO_2
Inorganic anions and NH_4+	Lab	Ion chromatography
Organic ions	Lab	Ion chromatography
Other organics	Lab	Various, e.g., ES TOF, ICP-MS
Reactive silica	Online or lab	Colorimetric
Dissolved N_2	Online	Electric cell
Total silica	Lab	ICP-MS or GFAAS
Particle monitoring	Online	Light scatter
Particle count	Lab	SEM—capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP-MS
Dissolved O_2	Online	Electric cell

ES TOF—Electro spray time of flight ICP-MS—inductively coupled plasma mass spectrometry
GFAAS—graphite furnace atomic absorption spectrometry

Figure YE1 General Test Methodology for Ultrapure Water

UPW and liquid chemicals particle measurement—Problem Definition and Goals: The sensitivity limit of particle counters for UPW and liquid chemicals has not kept pace with decreases in the critical particle size (the size of particles which are thought to be detrimental to wafer yield). Although this concept needs to be discussed again since particles not only impact yield because of their physical dimensions, but even more by the chemical composition, e.g. as spot Fe contamination, the fact remains the same. It is important to measure even smaller particles than we can do today. Measurements of these nanoparticles are made difficult by the low scattering efficiency of them. Low particle concentrations and small sample volumes of current particle monitors can result in large sample-to-sample variability. More sensitive particle measurement methodology with adequate measurement statistics is needed to meet projected purity goals.

The Sensitivity Problem: As of 2007, the highest sensitivity particles counter commercially available for UPW is 0.05 microns and for liquid chemicals is 0.065 microns. Experiments have shown that small particles may even deposit preferentially [M. Knotter] and therefore the impact is increased even further. Past improvements in particle counter sensitivity for UPW have been accomplished by increases in laser power. While improvements in sensitivity for liquid chemical particle counters are viable, further sensitivity improvements for UPW using this approach are unlikely, due to the significant cost implications. In addition, high-cost solutions do not necessarily guarantee a production-worthy metrology tool. High initial expense coupled with increased cost of ownership impact the viability of higher sensitivity instruments. To estimate the concentration of smaller particles currently an extrapolation assumes a $1/d^3$ relationship between particle counts and particle size in liquids. The further away the particle size of interest gets from actual measurement capabilities, the higher the potential for error-error being defined as the difference in the projected value to the true value. Therefore, it is still important for the industry to develop a more sensitive method that can measure particle concentrations at greater sensitivity to validate the particle count versus particle size relationship so that the relationship can continue to be reliably used.

The Measurement Precision Problem: Statistical process control is increasingly being used to monitor the consistency of process parameters. Process variation of fluid purity can be as critical to wafer yield as the absolute purity of the fluids. Therefore, it is important that measurement methods detect sufficient number of events to ensure confidence in measured particle concentrations. Development of other statistically significant particle counting methods or a higher sample volume particle counter is needed to improve confidence in reported particle counts. The sample volume (volume of fluid measured) will determine the number of particle counts that are detected during the sample interval. Refer to Supplemental Information link *Particle monitoring* for more detail.

Although the gas/liquid chemical section of Table YE9 shows an essentially flat purity trend, there is likelihood that specific process steps may require higher purity. Yield improvements may be achieved more by reducing variations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials.

Overview for gases and liquid chemicals— The recommended contaminant values for gases and chemicals in Table YE9 represent typical gas/liquid chemical quality requirements at the point of entry to the process tool (POE) for the more demanding manufacturing processes in the roadmap. In many applications, the requirements for the contaminants in these gases and/or liquid chemicals may be relaxed as dictated by the specific process requirements. On the other hand, some manufacturers have claimed benefits from lower contaminant levels. Considering that a given process can be run successfully within a "window" defined by a range of material purity and also by ranges in other parameters (purging time, etc.), it follows that, in practice, trade-offs exist between imposed purity requirements, process throughput, etc. Pushing a process to the upper limit of its "purity window" may require significant investment of time and effort in optimizing other parameters, and the economics of pursuing that effort will depend on the environment. It may also be that benefits attributed to low contaminant levels are more attributable to the reduction in contaminant variations achieved with high-purity process gases and chemicals. This topic is addressed in more detail below regarding the push for the adoption of statistical process control, SPC, for specifying process fluid purity.

There are three primary sources of process environment contamination: One is the impurities in the process materials as supplied. The second is the delivery system or the process itself. The third is decomposition, which may be caused thermally or by reaction with adventitious contaminants e.g. moisture. These contamination sources are found throughout the pathway from the delivered gas or chemical to the wafer surface. Table YE1 describes the several interfacial points of process materials with equipment found along these paths and associates them with the various TWGs within the ITRS and other organizations such as SEMI that focuses on them. This helps to clarify the relationship of these organizations with the WECC while also removing ambiguity about the definition of various points along the process path.

While purity measurements at the Point of Process, POP (that is, in the processing chamber itself), would provide the most direct correlation between gas or liquid quality and process performance, these measurements are often very difficult

to obtain with the exception of certain fluid properties in wafer immersion baths. Examples include both particulate generation during plasma processes and wafer outgassing. The latter is the most important source of water vapor contamination in many processes, often obscuring moisture contributions from the process fluid. Measurements at the POU provide the most direct information of the quality of process fluids going directly into the process chamber, but these are also not available for many of the common processes.

Because of these difficulties, the values in Table YE9 are intended to represent those at the Point of Entry, POE, defined as the inlet to the process tool as described in Table YE1. There are sufficient measurement data on bulk gases and aqueous fluids to provide guidance with regard to POE impurity levels for many applications, although measurements on these fluids are often performed at the POS, POD, or POC. For these materials, which are relatively unreactive and delivered in large volume, the extrapolation to POE is generally very reasonable. In the case of Specialty Gases and other reactive process fluids, such extrapolation is more delicate because delivered volumes are smaller, increasing sensitivity to contamination effects, and degradation in the distribution system related to materials of construction, atmospheric contamination, thermal degradation, etc. is more likely. These factors are minimized with normal best construction and operations practices, and therefore the best guidance available is often regarding POS specification and to a lesser extent POD or POC measurements, which are interpreted as equivalent to POE. In summary, while the intention is to recommend POE purity levels for all gases and liquids, in practice, the supporting data has more often been collected at POS, POD, or POC.

The targeted levels can be reached either by bulk delivery of a fluid with requisite purity or through use of a local purification/filtration. Care should be taken, at a minimum, to maintain the quality of the gas coming from the source, ensuring that contamination is not added downstream of the POS, as may occur due to particle generation at components, moisture out gassing, byproduct generation due to incompatible materials, etc. Particle filtration as close to the POU as possible is generally advisable for gases. For the most critical applications a local purifier may be used to enhance or ensure ultimate purity at the POU. In those cases, the prevailing approach is to seek POC levels that are adequate for the process and to view the purifier as "insurance." The challenge to the purifier is minimal, and long purifier lifetimes can normally be expected.

Specific purity challenges will be discussed below, but generally there is little objective evidence to suggest that the purity levels listed in Table YE9 are not suitable for multiple generations of semiconductor manufacturing. Yield improvements are expected to be achieved by reducing variations in purity. Statistical process control (SPC) on incoming materials will reduce variation at the POS. Inconsistencies at the POU may remain due to variations in downstream contributions, e.g. when the flow in a distribution system is decreased, moisture contamination due to out gassing tends to increase. Elimination of these variations may require purification at the appropriate point (e.g. POU purification, POUP).

The major bulk gases are listed separately in Table YE9. The 2007 roadmap had indicated an increase in purity requirements post 45 nm. This type of improvement might be anticipated, based upon historical trends as design rules tightened, but there is again little objective evidence to support the need for improvements across the range of bulk gases. Informal poling of several large semiconductor manufacturing organizations suggests that an increase above current purity requirements for the majority of bulk gases is not necessary to meet post 45 nm design rule manufacturing. For very special applications where extraordinarily higher purities are critical, special purity grades or additional purification will be required. As exemplified above, downstream POUP might also be utilized as an additional means of removing variability in POS gases. Therefore, Table YE9 has been modified from 2005 to remove many of the step improvements scheduled for future manufacturing nodes except where specific information has been identified to justify the change.

The situation is similar for many of the Specialty Gases, although several additional categories of applications have been added to better identify needs for specific processes, e.g., etch, deposition, doping and laser applications. Like the Bulk gases, the values in Table YE9 have been left at current levels, unless an objective justification for increased purity can be identified. Although changes to the current table YE9 values for gases are small, the introduction of so many new materials and the process innovations required to meet future design rules, e.g., atomic layer deposition, will require close monitoring. More details with regard to bulk and specialty gases are provided in the *Gas supplemental documents*.

The 2005 roadmap identified the growing need for statistical process control for process gases and liquids. Several companies have begun requesting materials with specifications related to the statistical control of variability of the materials, but there are no standards accepted across the industry that define the SPC process. Currently there is a Semi sponsored task force, composed of representatives from the end user and supplier communities that is creating a common set of characteristics for defining "in control" specifications for gases and liquids.

The promise of providing "in control" process fluids is anticipated to improve process yields by either minimizing the overall variability of the manufacturing process or in simply reducing the likelihood of a process crash resulting from large variations in material quality that would still nominally have met a more standard specification.

An informal survey of several large semiconductor manufacturing companies on their implementation of statistical process control requirements for their bulk and specialty gas purchases indicates that SPC processes are already being applied to many of the materials utilized in manufacturing, or will be shortly. However, the criteria that form the basis of "in control" varies substantially. Survey responses suggest that customer expectation is that the application of process control for the preparation of POS materials will improve their semiconductor manufacturing process stability and are critical for high yield manufacturing. Initial implementation, will likely focus on specialty gases that exhibit the greatest potential for causing semiconductor process variability, e.g., anhydrous HCl but will be used on new and existing products for both memory and microprocessors.

Liquid chemicals—Table YE9 summarizes the purity requirements for liquid chemicals delivered to process tools. Pre-diffusion cleaning requirements drive the most aggressive impurity levels. Liquid particle level targets are shown to become purer each technology generation. These target values are derived from the purity requirements on a wafer as calculated by the FEP surface preparation group assuming a linear relationship between the concentration in the liquid and on the wafer. Particle counters currently are capable of measuring only to 65 nm for liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes, but this will be influenced by the level of filtration utilized. Another measurement challenge for several chemicals is the differentiation between particles and bubbles, which is currently not possible.

The ability to accurately analyze organic, anion, and cation contamination in process chemicals is becoming more critical to successful wafer processing. In the supplementary materials an *ion table* and a *mixing calculation* is provided which shows for which chemicals which ions are important and in which chemicals they could actually occur/have been observed. With the increased use of CMP and plating chemicals, there must be a better understanding of purity requirements for the delivered chemicals. Table YE9 contains information only for very few CVD/ALD precursors. The variety of layers and the respective contaminants is enormous. Therefore, a link to the *precursor table* is provided in the supplementary materials online. The precursor table provides information by application as to which precursors are potential candidates at different technology generations, and the nature of contamination that can be expected. A major challenge is the development of accelerated yield learning for critical processes that introduce new precursors that will only be used for one or two generations.

Bulk/specialty gases—There were only a few changes to the bulk gas purity requirements. The measurement of organic refractory components at <0.1 ppb is a detect ability challenge for both nitrogen and helium used in lithography applications. The roadmap indicates these areas as orange from 2007 to 2010 because this is at the limit of detection for current analytical methods.

In addition, changes were made to better delineate the need to control Ar as an impurity. The N_2 specification was changed to eliminate Ar as a critical impurity, although it was left in the O_2 specification. Even so, the 50 ppbv limit given in 2005 was raised to an Ar limit of <1000 ppbv. The ongoing requirement in O_2 derives from the potential for uncontrolled Ar impurities to impact plasma etching processes, although typical Ar specifications for O_2 used for etching is more consistent with the <1000 ppbv level.

For some processes, such as advanced lithography, very small quantities of "high molecular weight/high boiling point" (e.g., C_6-C_{30}) hydrocarbons are detrimental because of increased adherence to the exposed surfaces, and potential for photochemical degradation to leave non-volatile residues on lenses, masks, mirrors, etc. However, any organics, even ones with retention times less than C_6 are considered detrimental if they can result in refractory deposits. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities. In order to detect such species with ultimate sensitivity, it is necessary to directly detect the relevant species and calibrate the analyzer with the appropriate standard. The methods used are analogous to those for AMC, such as TD gas chromatography (GC)/mass spectroscopy (MS) (TD = thermal desorption) or TD GC/FID, or ion mobility spectroscopy (IMS). Even these approaches may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks. For methods using adsorbent traps, it is very important to determine the trap efficiency. Using APIMS to provide real time measurement of individual hydrocarbons is possible, in principle, but calibration is difficult, because larger hydrocarbons are collisionally dissociated in the ionization process.

A compromise approach that has gained some acceptance is to use TD GC/MS and sum all peaks corresponding to C6 and higher. The instrument is usually calibrated with a multi-component standard and results are reported "hexadecane".

While the quantization provided by this method is approximate, and some species may be overlooked, it does at least emphasize the heavier hydrocarbons while providing a straightforward calibration.

Applications for both O_2 and H_2 generally tolerate higher levels of N_2 contamination than other contaminants and the table reflects this observation. Requirements for critical clean dry air (CDA), lithography purge gases, and supercritical CO_2 supply are included. Whereas critical CDA may not always be conveniently or cheaply available, there is no technological barrier to its production. Analytical methods are usually the same as used for airborne molecular contamination in clean room air, such as bubbling through ultra pure water (for metals, sulfates, amines, etc.) or trapping on an adsorbent trap for organics. In each case, the sampler concentrates impurities so that requisite sensitivities are achieved when the sample is introduced to the analyzer (ICP-MS or ion chromatography for aqueous samples, GC-MS for desorption of organics). Such methods are time consuming by nature, and direct methods would be preferred if available. However, there is no apparent pressing need for real-time analysis. For SO_2 there are convenient on line methods, e.g., UV fluorescence.

For specialty gases, contaminant values in etchants, dopants, and deposition gases have been expanded in Table YE9. to reflect the increase number of different materials in use, and to better delineate the processes they are used for. Particulate contamination is omitted, since online monitoring of particle concentrations is not commonly practiced and the efficacy of POU particle filters is well established. Whereas there is evidence that the most demanding applications, such as low temperature epi and its cleaning gases, will continue to benefit from improvements in purity as deposition temperatures are lowered, this is expected to be reflected in wider use of the best available purity rather than substantial improvements of those levels.

Tighter control over the variation in purity in both bulk and specialty gases is anticipated to be more important than improvement in absolute purity levels. However, the often more chemically reactive specialty gases present a more formidal challenge for maintaining of POS purity levels throughout the delivery to the point of process. Selected specialty gases, e.g. HCl are also expected to be among the first targeted for statistical process control at the POS.

Novel materials—More detailed consideration of the impurity levels found in the growing number of novel materials used in processing will be increasingly important. Requisite purity levels for critical materials such as novel metal oxides, CMP slurries, low/high k dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied, and many of these materials have not been called out in Table YE9. An early attempt to start to catalogue and characterize the properties of the thin film precursors utilized in semiconductor processing is found in the supplementary material for this chapter. (provide link)

Deposition precursors for thin film materials are often sensitive to moisture, air and high temperatures. Control over the delivery process from the POS to the reaction chamber is critical to high yielding performance. The use of very high purity carrier and purge gases in these systems are often required to prevent decomposition that can contribute detrimental molecular and particulate impurities. Traditionally bulk purifiers were used in the bulk gas delivery systems to remove particles and other homogeneous chemical contaminations like oxygen, or moisture present in the supply gases. However, with the development and commercial availability of point-of-use (POU) purifiers, there is a strong interest from end users to utilize point-of-use (POU) purifiers particularly for specialty gases needed for critical process steps with very critical level of contamination control. These point-of-use purifiers (POU) are highly effective to remove chemical contaminants to extreme low level (~ ppt), easy to use, easy to replace, with low cost-of-ownership. The capability of placing those point-of-use (POU) purifiers very close to inlet of process chamber, assures least travel path (less contamination) for process gases after chemical purification and filtration.

Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements. Additional detail on the variety of thin film precursors under consideration can be found in Liquid Chemicals section of Table YE9 and the supplementary *precursor table*.

Table YE9a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Wafer Environment Control such as Cleanroom, SMIF POD, FOUP, etc….not necessarily the cleanroom itself but wafer environment.									
Number of particles ($/m^3$) [1] [2]	ISO CL 2	ISO CL 2	ISO CL 2	ISO CL1	ISO CL1	ISO CL1	ISO CL1	ISO CL1	ISO CL1
Airborne Molecular Contaminants in Gas Phase (pptV V for Volume)) [3, 7, 12, 13, 14, 15, 33].									
Lithography (cleanroom ambient) [23]									
Total Inorganic Acids	5000	5000	5000	5000	5000	5000	5000	5000	5000
Total Organic Acids [30]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Total bases	50,000	50,000	50,000	50,000	50,000	50,000	50,000	50,000	50,000
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane) [31]	26000	26000	26000	26000	26000	26000	26000	26000	26000
Refractory compounds (organics containing S, P, Si)	100	100	100	100	100	100	100	100	100
SMC (surface molecular condensable) refractory compounds on wafers, ng/cm^2/day [12]	2	2	2	2	2	2	2	2	2
Gate/Furnace area wafer environment (cleanroom/POD/FOUP ambient)									
Total metals [8]	1	1	1	0.5	0.5	0.5	0.5	0.5	0.5
Dopants [4] (front end of line only)	10	10	10	10	10	10	10	10	10
SMC (surface molecular condensable) organics on wafers, ng/cm^2/day [12]	2	2	2	0.5	0.5	0.5	0.5	0.5	0.5
Salicidation Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total Inorganic Acids	100	100	100	10	10	10	10	10	10
Total Organic Acids [30]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Exposed Copper Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total Inorganic Acids	500	500	500	500	500	500	500	500	500
Total Organic Acids [30]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Total other corrosive species [32]	1000	1000	1000	1000	1000	1000	1000	1000	1000
H_2S	1000	1000	1000	1000	1000	1000	1000	1000	1000
Total sulphur compounds	10000	10000	10000	10000	10000	10000	10000	10000	10000
Exposed Aluminum Wafer Environment (Cleanroom/POD/FOUP ambient)									
Total Inorganic Acids	500	500	500	500	500	500	500	500	500
Total Organic Acids [30]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Total other corrosive species [32]	1000	1000	1000	1000	1000	1000	1000	1000	1000
Reticle Exposure (Cleanroom/POD/Box ambient)									
Total Inorganic Acids	500	500	500	TBD	TBD	TBD	TBD	TBD	TBD
Total Organic Acids [30]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Total Bases	2500	2500	2500	TBD	TBD	TBD	TBD	TBD	TBD
SMC (surface molecular condensable) organics on wafers, ng/cm^2/week [12]	2	2	2	0.5	0.5	0.5	0.5	0.5	0.5
Critical areas (Litho, Metrology)									
Temperature range in ±K at POE [37]	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Maximum short term temperature variation at POE in ±K/5 min [37]	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Table YE9a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

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MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Maximum long term temperature variation in ±K/hour at POE [37]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Humidity range in ± % r.H. at POE [37]	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Maximum short term humidity variation in ±r.H./5 min at POE [37]	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Non-critical areas (others than Litho, Metrology)									
Temperature range on ±K at POE [37]	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**
Humidity range in ± % r.H. at POE [37]	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Process Critical Materials [5, 7]									
Ultrapure Water [29]									
Resistivity at 25°C (MOhm-cm)	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**
Total oxidizable carbon (ppb) [22]	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Bacteria (CFU/liter) [38]	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Total silica (ppb) as SiO_2 [18]	**<0.5**	**<0.5**	**<0.5**	**<0.5**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Number of particles > 0.05 µm (/ml) [26]	**< 0.9**	**< 0.9**	**< 0.3**	**< 0.3**	**< 0.3**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.1**
Dissolved oxygen (ppb) (contaminant based) [16] POE	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Dissolved nitrogen (ppm) [10]	**8–12**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**
Critical metals (ppt, each) [6]	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**
Other critical ions (ppt each) [24]	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Temperature stability (K)	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**
Temperature gradient in K/10 minutes [22] for immersion photolithography	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
Liquid Chemicals									
49% HF: number of particles/ml >0.065µm [1] [11]	**< 10**	**< 4**	**< 4**	**< 4**	**< 3**	**< 3**	**< 3**	**< 1**	**< 1**
37% HCl: number of particles/ml >0.065µm [1] [11]	**< 10**	**< 4**	**< 4**	**< 4**	**< 3**	**< 3**	**< 3**	**< 1**	**< 1**
30% H_2O_2: number of particles/ml >0.065µm [1] [11]	**< 1000**	**< 400**	**< 400**	**< 400**	**< 300**	**< 300**	**< 300**	**< 100**	**< 100**
29% NH_4OH: number of particles/ml >0.065µm [1] [11]	**< 1000**	**< 400**	**< 400**	**< 400**	**< 300**	**< 300**	**< 300**	**< 100**	**< 100**
100% IPA: number of particles/ml >0.065µm [1] [11]	**< 1000**	**< 400**	**< 400**	**< 400**	**< 300**	**< 300**	**< 300**	**< 100**	**< 100**
49% HF: Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Pd, Pt, Ru) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**
49% HF: Cl (ppt)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
30% H_2O_2: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**
30% H_2O_2: SiO_2 (ppt) [27]	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
29% NH_4OH: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**
100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Ca (ppt, each) [28]	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**	**150**
100% IPA: Cl (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**

Table YE9a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

Year of Production	***2007***	***2008***	***2009***	***2010***	***2011***	***2012***	***2013***	***2014***	***2015***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
100% IPA: Br (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**
100% IPA: F (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**
49% HF: All other metals not listed in row above (ppt, each) [20]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
30% H_2O_2: All other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
29% NH_4OH: all other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
100% IPA: all other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**	**500**
30% H_2O_2: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
100% IPA – Specific organic acids: formate, acetate, citrate, proprionate, oxalate (ppt, each)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
IPA: High molecular weight organics (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30%H_2O_2: resin byproducts (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: K, Ni, Cu, Cr, Co, (ppt, each)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
96% H_2SO_4: K, Ni, Cu, Cr, Co, (ppt, each)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
37% HCl: all other metals not listed in row above (ppt, each) [20]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
96% H_2SO_4: all other metals not listed in row above (ppt, each) [20]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
BEOL solvents, strippers K, Li, Na, (ppt, each)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
CMP slurries: scratching particles (/ml > key particle size) [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: particles>critical size (/ml) [1] [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: elements TBD (ppt, each) [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [1] [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., Trimethylsilane, Tetramethylsilane) [25]									
Metals except B, Au, Ag (ppb, each)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
B, Au, Ag (ppb, each)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
H_2O (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
CO, CO_2 (ppm)	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
Non-methane hydrocarbons C_2-C_4 (ppm)	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**
Nitrogen (ppm)	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**
Ar+O_2 (ppm)	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
Chloride (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
CVD Precursors (e.g., Trimethylaluminum) [25]									
Metals each element (ppb)	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**
O_2 (ppm)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Silicon (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**

Table YE9a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Hydrocarbons (ppm)	<5	<5	<5	<5	<5	<5	<5	<5	<5
Bulk Gases (Contaminants, ppbv) [5]									
N_2 (O_2, H_2, H_2O, CO, CO_2, THC) [34]	<5	<5	<5	<5	<5	<5	<5	<5	<5
O_2 (N_2)	<50	<50	<50	<50	<50	<50	<50	<50	<50
O_2 (Ar)	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
O_2 (H_2, H_2O, CO, CO_2, THC)	<10	<10	<10	<10	<10	<10	<10	<10	<10
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC) [34]	<5	<5	<5	<5	<5	<5	<5	<5	<5
H_2 (N_2)	<50	<50	<50	<50	<50	<50	<50	<50	<50
H_2 (O_2, H_2O, CO, CO_2, THC)	<10	<10	<10	<10	<10	<10	<10	<10	<10
He (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	<10	<10	<10	<10	<10	<10	<10	<10	<10
CO_2 (N_2, CO, H_2O, O_2, THC) [35]	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
Lithography Purge Gases									
Critical clean dry air (H_2O)	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000	<1000
Critical clean dry air (H_2, CO)	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000
Critical clean dry air (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	< 3	< 3	< 3	< 3	< 3	< 3	< 3	< 3	< 3
Critical clean dry air (total base as NH_3) (ppb)	< 1	< 1	< 1	< 1	< 1	< 1	< 1	< 1	< 1
Critical clean dry air (NH_3 (as NH_3)) (ppb)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
Critical clean dry air (total acid including SO_2 (as SO_4)) (ppb)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
Critical clean dry air (SO_4 (as SO_4)) (ppb)	< 0.03	< 0.03	< 0.03	< 0.03	< 0.03	< 0.03	< 0.03	< 0.03	< 0.03
Critical clean dry air (Each refractory compound (Organics containing S, P, Si)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
Lithography nitrogen tool/maintenance purging gas supply (H_2O, O_2, CO_2) (ppb)	<500	<500	<500	<500	<500	<500	<500	<500	<500
Lithography nitrogen tool/maintenance purging gas supply (CO) (ppb)	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000
Lithography nitrogen tool/maintenance purging gas supply (H_2) (ppb)	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000	<2000
Lithography nitrogen tool/maintenance purging gas supply (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	< 3	< 3	< 3	< 3	< 3	< 3	< 3	< 3	< 3
Lithography nitrogen tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	< 0.15	< 0.15	< 0.15	< 0.15	< 0.15	< 0.15	< 0.15	< 0.15	< 0.15
Lithography nitrogen tool/maintenance purging gas supply (total acid (as SO_4) including SO_2) (ppb)	< 0.025	< 0.025	< 0.025	< 0.025	< 0.025	< 0.025	< 0.025	< 0.025	< 0.025
Lithography nitrogen tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppb)	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1

Table YE9a Technology Requirements for Wafer Environmental Contamination Control—Near-term Years

Year of Production	***2007***	***2008***	***2009***	***2010***	***2011***	***2012***	***2013***	***2014***	***2015***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Lithography helium tool/maintenance purging gas supply (H_2O) (ppb)	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**
Lithography helium tool/maintenance purging gas supply (O_2, CO_2) (ppb)	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**
Lithography helium tool/maintenance purging gas supply (CO, H_2) (ppb)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**
Lithography helium tool/maintenance purging gas supply (organics(molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**
Lithography helium tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography helium tool/maintenance purging gas supply (total acid including SO_2 (as SO_4)) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography helium tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppb)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
Number of particles > critical size (/M^3) [1]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
Specialty Gases									
Etchants (Corrosive, e.g., BCl_3, Cl_2, HBr)									
O_2, H_2O (ppbv)	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Critical specified metals/total metals (ppbw) [19]	**<10/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Etchants (Non-corrosive, e.g., C_5F_8, C_4F_8, C_4F_6, CH_2F_2)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Etchants (e.g., Xe)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Deposition gases (e.g., SiH_4, $(CH_3)_3SiH$)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<10/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Deposition gases (e.g., NH_3)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases (e.g., N_2O, NO)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases (e.g., WF_6)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**

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Year of Production	***2007***	***2008***	***2009***	***2010***	***2011***	***2012***	***2013***	***2014***	***2015***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Printed Gate Length (nm)	*42*	*38*	*34*	*30*	*27*	*24*	*21*	*19*	*17*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases—electrical dopants (e.g. AsH_3, PH_3, B_2H_6)									
O_2, H_2 (ppb [36]	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Mixing tolerance for mixtures (relative variance)	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**
Deposition gases—GeH_4									
O_2, H_2O (ppbv)	**<500**	**<500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Mixing tolerance for mixtures	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**
Implant gases—AsH_3, PH_3, BF_3									
O_2, H_2O (ppbv)	**<500**	**<500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Laser gases—Litho, (e.g., F_2/Kr/Ne)									
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Mixing tolerance for F_2 (relative variance)	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**
Other constituents (ppbv)	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**

Table YE9b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	***2016***	***2017***	***2018***	***2019***	***2020***	***2021***	***2022***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm)	*15*	*13*	*12*	*11*	*9*	*8*	*8*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Wafer Environment Control such as Cleanroom, SMIF POD, FOUP, etc…not necessarily the cleanroom itself but wafer environment.							
Number of particles (/m^3) [1] [2]	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**
Airborne Molecular Contaminants in Gas Phase (pptV V for Volume)) [3, 7, 12, 13, 14, 15, 33].							
Lithography (cleanroom ambient) [23]							
Total Inorganic Acids	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
Total Organic Acids [30]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total bases	**50,000**	**50,000**	**50,000**	**50,000**	**50,000**	**50000**	**50000**
Condensable organics (w/ GCMS retention times ≥ benzene, calibrated to hexadecane) [31]	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**	**26000**
Refractory compounds (organics containing S, P, Si)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
SMC (surface molecular condensable) refractory compounds on wafers, ng/cm^2/day [12]	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Gate/Furnace area wafer environment (cleanroom/POD/FOUP ambient)							
Total metals [8]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Dopants [4] (front end of line only)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/day [12]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Salicidation Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total Inorganic Acids	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Total Organic Acids [30]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Exposed Copper Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total Inorganic Acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Total Organic Acids [30]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total other corrosive species [32]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
H_2S	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
Total sulphur compounds	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
Exposed Aluminum Wafer Environment (Cleanroom/POD/FOUP ambient)							
Total Inorganic Acids	**500**	**500**	**500**	**500**	**500**	**500**	**500**
Total Organic Acids [30]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total other corrosive species [32]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
Reticle Exposure (Cleanroom/POD/Box ambient)							
Total Inorganic Acids	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total Organic Acids [30]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Total Bases	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
SMC (surface molecular condensable) organics on wafers, ng/cm^2/week [12]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Critical areas (Litho, Metrology)							
Temperature range in ±K at POE [37]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Maximum short term temperature variation at POE in ±K/5 min [37]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Maximum long term temperature variation in ±K/hour at POE [37]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Humidity range in ± % r.H. at POE [37]	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Table YE9b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	***2016***	***2017***	***2018***	***2019***	***2020***	***2021***	***2022***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm)	*15*	*13*	*12*	*11*	*9*	*8*	*8*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Maximum short term humidity variation in ±r.H./5 min at POE [37]	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Non-critical areas (others than Litho, Metrology)							
Temperature range on ±K at POE [37]	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**	**2.0**
Humidity range in ± % r.H. at POE [37]	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Process Critical Materials [5, 7]							
Ultrapure Water [29]							
Resistivity at 25°C (MOhm-cm)	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**
Total oxidizable carbon (ppb) [22]	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Bacteria (CFU/liter) [38]	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Total silica (ppb) as SiO_2 [18]	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**	**<0.3**
Number of particles > 0.05 µm (/ml) [26]	**< 0.1**	**< 0.1**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**
Dissolved oxygen (ppb) (contaminant based) [16] POE	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Dissolved nitrogen (ppm) [10]	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**	**8–18**
Critical metals (ppt, each) [6]	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**	**<1.0**
Other critical ions (ppt each) [24]	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Temperature stability (K)	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**	**± 1**
Temperature gradient in K/10 minutes [22] for immersion photolithography	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
Liquid Chemicals							
49% HF: number of particles/ml >0.065µm [1] [11]	**< 1**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
37% HCl: number of particles/ml >0.065µm [1] [11]	**< 1**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
30% H_2O_2: number of particles/ml >0.065µm [1] [11]	**< 100**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**
29% NH_4OH: number of particles/ml >0.065µm [1] [11]	**< 100**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**
100% IPA: number of particles/ml >0.065µm [1] [11]	**< 100**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**	**< 50**
49% HF: Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Pd, Pt, Ru) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**
49% HF: Cl (ppt)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
30% H_2O_2: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Ag, Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**
30% H_2O_2: SiO_2 (ppt) [27]	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**	**5000**
29% NH_4OH: Al, Na, K, Fe, Ni, Cu, Cr, Co, Ca, (Au, Ba, Cd, Mg, Mn, Mo, Pb, Pd, Pt, Ru, Sn, Ti, V, W, Zn) (ppt, each) [21]	**150**	**150**	**150**	**150**	**150**	**150**	**150**
100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Ca (ppt, each) [28]	**150**	**150**	**150**	**150**	**150**	**150**	**150**
100% IPA: Cl (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**
100% IPA: Br (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**
100% IPA: F (ppt) [28]	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**	**100000**
49% HF: All other metals not listed in row above (ppt, each) [20]	**500**	**500**	**500**	**500**	**500**	**500**	**500**
30% H_2O_2: All other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**
29% NH_4OH: all other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**

Table YE9b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	***2016***	***2017***	***2018***	***2019***	***2020***	***2021***	***2022***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm)	*15*	*13*	*12*	*11*	*9*	*8*	*8*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
100% IPA: all other metals not listed in row above (ppt, each) [21]	**500**	**500**	**500**	**500**	**500**	**500**	**500**
30% H_2O_2: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
100% IPA—Specific organic acids: formate, acetate, citrate, proprionate, oxalate (ppt, each)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
IPA: High molecular weight organics (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30%H_2O_2: resin byproducts (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: K, Ni, Cu, Cr, Co, (ppt, each)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
96% H_2SO_4: K, Ni, Cu, Cr, Co, (ppt, each)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**
37% HCl: all other metals not listed in row above (ppt, each) [20]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
96% H_2SO_4: all other metals not listed in row above (ppt, each) [20]	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
BEOL solvents, strippers K, Li, Na, (ppt, each)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
CMP slurries: scratching particles (/ml > key particle size) [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: particles>critical size (/ml) [1] [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Post-CMP clean chemicals: elements TBD (ppt, each) [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [1] [9] [17]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., Trimethylsilane, Tetramethylsilane) [25]							
Metals except B, Au, Ag (ppb, each)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
B, Au, Ag (ppb, each)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
H_2O (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
CO, CO_2 (ppm)	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
Non-methane hydrocarbons C_2-C_4 (ppm)	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**	**< 4**
Nitrogen (ppm)	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**	**< 2**
Ar+O_2 (ppm)	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**
Chloride (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
CVD Precursors (e.g., Trimethylaluminum) [25]							
Metals each element (ppb)	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**
O_2 (ppm)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Silicon (ppm)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Hydrocarbons (ppm)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
Bulk Gases (Contaminants, ppbv) [5]							
N_2 (O_2, H_2, H_2O, CO, CO_2, THC) [34]	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
O_2 (N2)	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
O_2 (Ar)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
O_2 (H_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC) [34]	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
H_2 (N_2)	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
H_2 (O_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**

Table YE9b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	***2016***	***2017***	***2018***	***2019***	***2020***	***2021***	***2022***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm)	*15*	*13*	*12*	*11*	*9*	*8*	*8*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
He (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
CO_2 (N_2, CO, H_2O, O_2, THC) [35]	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Lithography Purge Gases							
Critical clean dry air (H_2O)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Critical clean dry air (H_2, CO)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Critical clean dry air (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**
Critical clean dry air (total base as NH_3) (ppb)	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**<1**	**<1**
Critical clean dry air (NH_3 (as NH_3)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**<0.1**	**<0.1**
Critical clean dry air (total acid including SO_2 (as SO_4)) (ppb)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**<0.1**	**<0.1**
Critical clean dry air (SO_4 (as SO_4)) (ppb)	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**< 0.03**	**<0.03**	**<0.03**
Critical clean dry air (Each refractory compound (0rganics containing S, P, Si)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**<0.1**	**<0.1**
Lithography nitrogen tool/maintenance purging gas supply (H_2O, O_2, CO_2) (ppb)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
Lithography nitrogen tool/maintenance purging gas supply (CO) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (H_2) (ppb)	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**	**<2000**
Lithography nitrogen tool/maintenance purging gas supply (organics (molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**
Lithography nitrogen tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**<0.15**	**<0.15**
Lithography nitrogen tool/maintenance purging gas supply (total acid (as SO_4) including SO_2) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**<0.025**	**<0.025**
Lithography nitrogen tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppb)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
Lithography helium tool/maintenance purging gas supply (H_2O) (ppb)	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**	**<3500**
Lithography helium tool/maintenance purging gas supply (O_2, CO_2) (ppb)	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**	**<4000**
Lithography helium tool/maintenance purging gas supply (CO, H_2) (ppb)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**
Lithography helium tool/maintenance purging gas supply (organics(molecular weight > benzene) normalized to hexadecane equivalent) (ppb)	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**	**< 3**
Lithography helium tool/maintenance purging gas supply (total base (as NH_3)) (ppb)	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**	**< 0.15**
Lithography helium tool/maintenance purging gas supply (total acid including SO_2 (as SO_4)) (ppb)	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**	**< 0.025**
Lithography helium tool/maintenance purging gas supply (refractory compounds (organics containing S, P, Si, etc.) normalized to hexadecane equivalent) (ppb)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
Number of particles > critical size (/M_3) [1]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Table YE9b Technology Requirements for Wafer Environmental Contamination Control—Long-term Years

Year of Production	***2016***	***2017***	***2018***	***2019***	***2020***	***2021***	***2022***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
DRAM ½ Pitch (nm) (contacted)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*23*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Printed Gate Length (nm)	*15*	*13*	*12*	*11*	*9*	*8*	*8*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Specialty Gases							
Etchants (Corrosive, e.g., BCl_3, Cl_2, HBr)							
O_2, H_2O (ppbv)	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Etchants (Non-corrosive, e.g., C_5F_8, C_4F_8, C_4F_6, CH_2F_2)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Etchants (e.g., Xe)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Deposition gases (e.g., SiH_4, $(CH_3)_3SiH$)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Deposition gases (e.g,. NH_3)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases (e.g., N_2O, NO)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases (e.g., WF_6)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Critical specified metals/total metals (ppbw) [19]	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**	**<1/1000**
Deposition gases—electrical dopants (e.g. AsH_3, PH_3, B_2H_6)							
O_2, H_2 (ppb [36]	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Mixing tolerance for mixtures (relative variance)	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**
Deposition gases—GeH_4							
O_2, H_2O (ppbv)	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Mixing tolerance for mixtures	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**	**±1%**
Implant gases—AsH_3, PH_3, BF_3							
O_2, H_2O (ppbv)	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**	**< 500**
Other dopants (ppbv)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Laser gases—Litho, (e.g. F_2/Kr/Ne)							
O_2, H_2O (ppbv)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**
Mixing tolerance for F_2 (relative variance)	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**
Other constituents (ppbv)	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**	**< 25000**

Notes for Tables YE9a and b:

*[1] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles. Because of instrumentation limitations, particle densities at the critical dimension for < 90 nm will need to be estimated from measured densities of larger particles and an assumed particle size distribution or determined empirically and extrapolated. The particle size distribution will depend on the fluid (e.g. water, clean room air, gases), f(x)=K*1/X^n (where n=2.2 for air/gases, n varies significantly for liquids from 1 to 4, empirical determination is recommended)[1], [2]*

[2] Airborne particle requirements are based on ISO 14644-1 at "at rest".[3]

[3] Ion/species indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography projections is defined by lithography tool suppliers. Metals and organics scale as defined in the surface preparation roadmap for metallics and organics. Values listed in table are based on experience, however, all airborne molecular contaminants can be calculated as S=E(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1), N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second). The following sticking coefficients have been proposed; SO4 = 1x10^{-5}, NH3 = 1x10^{-6}, Cu = 2x10^{-5}. The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination.*

[4] Includes P, B, As, Sb

[5] Contaminant targets apply up to POE (point-of-entry). POE is defined as the entry point to the equipment or subequipment, see also the text. Benchmark data has been collected both at Point of Delivery (POD) or Point of Entry (POE), which typically show only minor differences.

[6] Critical metals and ions may include: Al, As, Ba, Ca, Co, Cu, Cr, Fe, K, Li, Mg, Mn, Na, Ni, Pb, Sn, Ti, Zn. Three different case studies were reviewed where the levels of Ca, Fe, and Ni in the UPW resulted in levels of problem densities (atoms/sq cm) on the wafer. These were reduced to acceptable levels by reducing the level of these elements in the UPW to levels well below 10 ppt. In only one case does the data exist that showed success by obtaining values below 0.5 ppt. These results drive the 1.0 ~ 0.5 ppt values.

[7] Units on all contaminants in WECC Table are often given as ppb (or ppm or ppt, we use ppb here solely for demonstration purposes). The reader should be aware that these units of parts per billion (ppb) may be ppb by mass, volume, or molar ratios. Where not designated, the following guidelines apply: Chemicals and UPW are typically ppb by mass, gases and clean room are typically ppb by volume. In the case of the fluid acting as an ideal gas, ppb by volume is equal to ppb molar. The notable exception to the above is metals in gases that are ppb by mass.

Some parameters in the tables may be considered process variables rather than contaminants in the classical meaning. They are marked by an asterix. The limits are sometimes fluent.

[8] Detection of metals at the levels indicated will be dependent on sampling time and flow rate. Sticking Coefficients vary widely for metals. It is generally believed that Cu has a sticking coefficient 10x of other metals, and therefore the guideline for Cu could be lower.

[9] Key particle size for scratching particles depends on mean particle size of slurry. Target level will be specific to slurry and wafer geometry sensitivity.

[10] The Dissolved Nitrogen range is solely for the physical process needs of megasonics cleaning. Processes without megasonics cleaning can ignore the line item. The concentration is process specific and needs to be determined by the end user. Factors to consider include UPW temperature, partial pressure in the gas phase and megasonic energy input at the tool. Other gases, such as oxygen and hydrogen, may be used with different optimum levels. Process enhancements through chemistry associated with the other gases or other chemicals are outside of the scope of this chapter.

[11] As of the current year's update the finest sensitivity liquid particle sensor for chemicals is 0.065 µm. Values obtained by these particle counters are not directly comparable to the roadmap values and need to be normalized to critical particle size values in the roadmap using the equation and methods of Footnote A above. Interim solution to higher sensitivity particle counter is to collect data over longer time period to provide greater precision in the data near the threshold sensitivity of the counter. Most benchmark data has been collected at Point of Delivery (POD) or Point of Entry (POE) and is the basis for parameters.

[12] SMC Organics: Single wafer shall be oxidized to make organic-free, then wafer shall be exposed for 24 hours and top side analyzed by TD-GC-MS with 400°C thermal desorption, and quantitation based on hexadecane external standard. TIC response factor per SEMI MF 1982-1103 (formerly ASTM 1982-99).[4] Limits determined by above method are a guideline for many organics. Note higher limits can be used for process wafers oxidized or cleaned prior to subsequent process step. Processes such as gate oxide formation, or polysilicon deposition, may be more sensitive to organics, especially high boilers such as DOP. Silicon nitride nucleation may also be more sensitive than above for some processes. Please note dopants requirement is covered in earlier section. Contamination levels are time based, and samples should be exposed for a weeks time for better sensitivity; ng/cm2/week. Total contamination level on reticles that cause problems also vary with energy exposure. These guidelines subject to change with new data currently being generated.

[13] SMC Dopants: Single wafer is first stripped with HF to yield dopant-free surface and than exposed for 24 hours. Topside of wafer is analyzed by methods known to give reliable recovery of boron. This is a guideline for dopants based on sampling in operating running fabs. Lower specifications may be required for key FEPs, especially for smaller geometries, lower thermal budgets, and for lightly-doped devices. If wafers are stripped with HF or BOE immediately prior to next thermal process, then steps may become less sensitive to surface molecular dopants, and higher limits apply. Note that BEPs tend to be orders of magnitude less sensitive to dopants than FEPs.

[14] SMC Metals: Single wafer known to meet the ITRS FEP spec of 1E10 atoms/cm^2, from the Starting Materials table, is exposed to a clean environment for 24 hours. Subsequent analysis of top surface by VPD-ICP-MS or VPD-GFAA. Lower specifications may be required for key FEPs, especially for smaller geometries. If wafers are cleaned prior to the next thermal process, then air exposure during earlier steps may be less of an issue. Note that majority of environmental metallic contaminants are particles, not molecular. If total particles on wafers are kept in spec than majority of metals, most metals from the environment should be within specifications. Back-end processes (BEPs) tend to be less sensitive to metals that FEPs provided not particles. Specs of twice the incoming wafer specs are readily achievable and readily measurable in case of wafers exposed for 24 hours.

[15] SMC General: A 24-hour exposure will accentuate the contamination per wafer as wafers are often exposed too much shorter times in actual processing. The above SMC (surface molecular contamination) limits are preliminary, and no single value applies to all process steps or types of organics, dopants or metals. The SMC limits can vary substantially from process to process, and local air purification or purges may be needed to control contaminant levels.

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[1] *Cooper, D. W., "Comparing Three Environmental Particle Size Distributions," Journal of the IES, Jan/Feb 1001, 21-24*

[2] *Pui, D. Y. H. and Liu, B.Y.H., "Advances in Instrumentation for Atmospheric Aerosol Measurement," TSI Journal of Particle Instrumentation, Vol 4. (2) Jul-Dec 1989, 3-2.*

[3] *ISO 14644-1 Cleanrooms and Associated Controlled Environments-Part 1: Classification of Air Cleanliness.*

[4] *SEMI MF1982-1103 (previously ASTMF 1982-99e1), Standard Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography, SEMI.*

[16] Dissolved oxygen (DO) has an effect on pre-gate oxide cleaning and the etch rate of non H-passivated SiO2 and copper structures. The level in the table is that of the most stringent. It is expected that slightly higher levels within the same order of magnitude would not have any significant effect on manufacturing processes. If the water for a specific processes need to remain at low oxygen concentrations lower levels of dissolved oxygen could provide somewhat larger process time windows before critical concentration levels are reached. It is known that some fabs consider DO a process variable and operate at DO levels 3 orders of magnitude higher than stated in the table. Corrosion rates as a function of DO are not a linear relationship for all materials, specifically copper etch rates are near a maximum at 300 ppb DO.
[17] Uncertain at this time what target levels might be set given the variety of chemistries used in the industry and unknown sensitivity of the wafer to particles or ionic contamination in the chemical. This parameter is identified as a potentially critical one that should be considered and work is ongoing to define the correct levels.
[18] Total Silica in UPW is a source of wafer water spots. Silica dissolved from the wafer surface, and later deposited back, is also a significant source for water spotting. The values in the table are based on concentrations found in typical fabricators manufacturing 90 nm geometry devices. As device geometries shrink lower silica concentration requirements are expected. Research is needed to develop a clear correlation between UPW concentrations and water spots. Boron and Reactive Silica have been removed from the table as UPW operational parameters, values of 50ppt and 300ppt respectively. These two species remain valuable indicators of ion exchange resin removal capacity as they are the first two anions to leak from a mixed bed. They have been removed from the table as they are not process critical at typical UPW system concentrations.
[19] The list of critical metals (e.g., Al, Ca, Cu, Fe, Mg, Ni, K, Si, Na) varies from process to process depending on the impact on electrical parameters such as gate oxide integrity or minority carrier lifetime as well as mobility of the metal in the substrate. The metals listed in note [G] for liquid process chemicals are of concern but the issues around metals in specialty gases are primarily around the potential for corrosion to add metal particles to the gas flow (e.g., Fe, Ni Co, P). The potential for volatile species containing metals must be considered for each specialty gas but are generally not present in the bulk gases.
[20] The following is a complete list of metal ions of concern in certain liquid chemicals: Ag, Al, As, Au, Ba, Ca, Cd, Co, Cr, Cu, Fe, K, Li, Mg, Mn, Mo, Na, Ni, P, Pb, Pd, Pt, Ru, Sb, Sn, Sr, Ti, V, W, Zn.
[21] Elements listed that are not in parentheses may cause high or some risk to device quality and may often be present in process chemicals. Elements listed that are in parentheses may cause high risk to device quality but are not typically present in process chemicals.
[22] Immersion photolithography tool manufacturers have asked for TOC levels ranging from less than 0.5 to less than 1.0 ppb in UPW. Some manufacturers are supplying ancillary UPW processing equipment to achieve these targets. The concern is hazing of tool lenses. At this time no data has been presented to support the source of haze generating organics to be the UPW. Other sources of organics are the photoresists and topping chemistries. This temperature stability requirement is for immersion photolithography tools, using UPW as an immersion fluid, and based upon utility requirements projected by some tool manufacturers in 2005. It represents the maximum rate of change of the temperature of the cold UPW supplied to the tool in order for the tool to maintain process required temperature stability.
[23] The photolithography AMC guidelines are for tools with ArF lasers only, and are based on inputs from the photolithography tool supplier. All photolithography tools should have chemical filters on the makeup air to the internals of the tools. These filters have a finite lifetime, which is dependent on the contaminant loading. Providing a chemically cleaner environment will extend the life of these filters.
[24] Other critical ions may include inorganic ions such as Fluoride, Chloride, Nitrate, Nitrite, Phosphate, Bromide, Sulfate as well as ammonium. However no reference was currently found that these ions in typical concentrations found in ultrapure water up to 50 ppt have any impact on the process. Also for organic anions such as acetate, formate, propionate, citrate, and oxalate no harmful levels have been established up to now.
[25] The variety of CVD and ALD precursors is continuously increasing as well as their applications. The contaminant types and levels vary widely due to the different chemical behavior. An overview about typical precursors is therefore given in attachment Precursor table.
[26] Particle values for 2006 are based upon 2005 UPW benchmark studies of leading fabs manufacturing/developing 45 nm to 130 nm products measuring particles with optical lasers and Scanning Electron Microscopy (SEM). The values are dependent on the methods used for measurement. Values are based on the most widely used method of measurement namely, optical laser monitoring from various instrument manufacturers. Current optical laser technology is limited to particles >0.05 um, and incapable of detecting particles at critical size based on ½ design rule. Although a correlation between wafer surface counts and UPW particles has not been established a conservative position has been agreed upon which supports the Front End Process ITRS Roadmap for wafer surface counts. It is believed that particle chemical composition plays an increasing role with regard to the contamination effect.
Dialog with the Surface Prep/FEP subcommittee has resulted in a reduction of the suggested maximum particle levels from the previous year. Although a correlation between wafer surface counts and UPW particles has not been established a conservative position has been agreed upon which supports the Front End Process ITRS Roadmap for wafer surface counts. Note that current optical laser technology is limited to particles >0.05 um, and is incapable of detecting particles at the critical size based on ½ design rule.
[27] It needs to be considered that the total H2O2 anion concentration will impact the life time of the solution. Also the fluoride in the ppm range of the total chemical mixture can etch the wafer.
[28] Concentrations higher than 100 ppb could cause corrosion especially in back end of line processes.
[29] The ultrapure water parameters provided in this table are applicable for the most critical process unless otherwise identified by additional footnotes. Further information can be found in the Supplementary tables
[30] Typical Organic Acids found in cleanroom environments that may be of concern include Acetate, Citrate, Formate, Glycolate, Lactate, Oxalate, and Proprionate. Others may also be of concern. These acids can be a significant load on acid removal filters.
[31] Ideally, continuous monitoring using online instrumentation would be preferred when practical since this can give both long term averages and catch excursions. When online monitoring is not available, an average grab sample for at least 4 hours, and not more than 24 hours is recommended, to get an average, increase sensitivity of the analysis, and avoid short term transient effects
[32] Other corrosive species include contaminants such as chlorine. Humidity is also of major concern, as it exacerbates corrosion. The humidity should be kept as low as possible in corrosive environments.
*[33] Calculations for expressing ng/L into ppt are; [(ng/(L of Air) * (24.4 L of Air)/mol Air / MW(ng/nmol)) * *1000picomol/nmol] = picomol/mol of Air = ppt molar and/or ppt volume.*
[34] For certain processes such as sputtering POE purifiers may be required for N2 and Ar
[35] CO2 here is assumed to be used for wet cleaning and other equipment, not for super critical CO2 applications or dry etching.
[36] Epi – need to purify @ 45 nm; currently must add purifiers from B2H6/Germane/PH3/AsH3 - need 100 ppb
[37] The variation is defined at one location over time in at rest conditions. As reference point for the POE a location is chosen 0.3 m below the ceiling panels. Common sense requires that sensitive equipment are not installed heat sources within the cleanroom, since they may impact the temperature control between the reference point and the actual inlet to the mini-environment/tool filter.
[38] Bacteria level in clean UPW system is typically zero, therefore the target level of bacteria is less than 1 CFU/L. It should be noted that the that commonly used method of bacteria cultivation has it's limitations and slightly higher than 1 readings may be result of the sample contamination (see more details in the supplimental materials). See also Supplementary materials.

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

Very small particles will request study of thermophoresis and/or Van Der Waals force to understand behavior in the near future. Currently yield society does not have enough experience about particles between molecular and optically visible particles. Research into precise yield model assisted by TCAD is becoming important because SMLY issues tend to restrict yield ramping rate and attainment level. Ever increasing NRE also requests understanding of SMLY and its effective implementation to product. Parametric limited yield issues including line edge roughness and design to process mismatch also tend to limit yield. This will require research into new characterization devices and statistical methods to organize measured data. Figure YE2 illustrates a few potential solutions that may help address the technology requirements for future yield modeling.

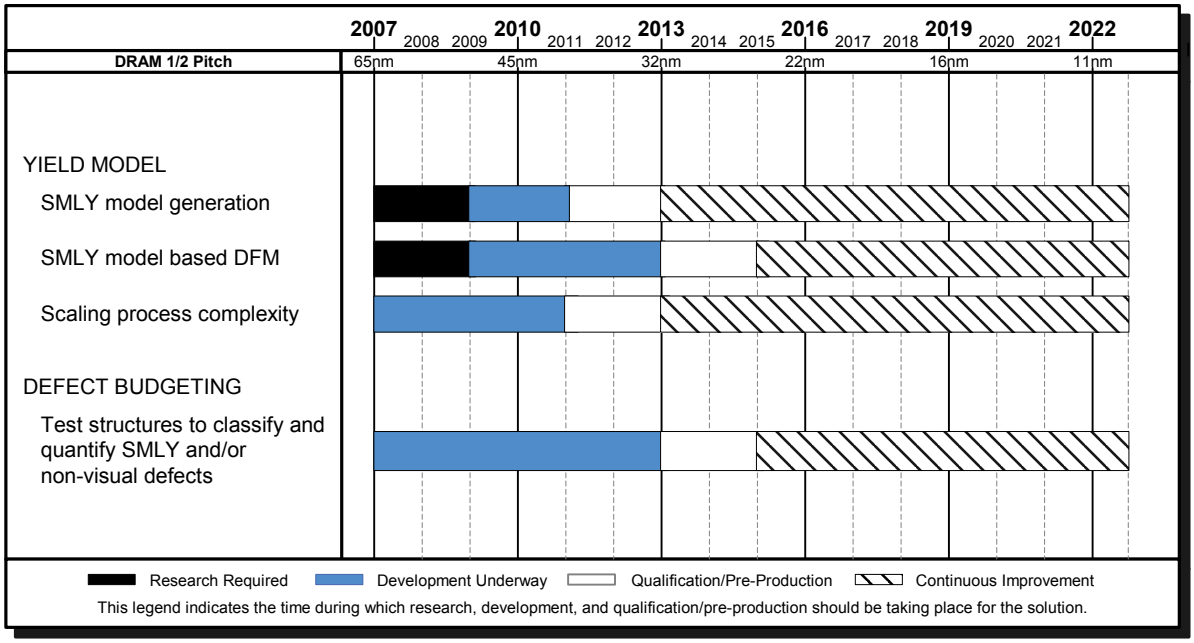

Figure YE2 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION AND CHARACTERIZATION

Considerable research and development is now necessary to meet the technology requirements for advanced defect detection tools. The research and development should focus on methods to filter out the defects of interest automatically. Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. Arrayed detection schemes for parallel data acquisition from a larger area of the wafer need to be explored.

There is a lack of suitable component technologies for developing novel detection systems. Significant advancement associated with shorter wavelengths, continuous-wave lasers, detectors with higher quantum efficiency and higher acquisition speed, suitable low-loss and low-aberration lenses, waveplates and polarizers, and robust mechanical and acousto-optic scanners are needed now to continue the economical development of optical techniques.

Wafer edge and bevel inspection need further research in order to meet sensitivity and speed requirements, furthermore methods have to be developed to filter out the defect of interest and classify the defects automatically. Also a review capability of the whole edge and bevel area is requested to allow further analysis of the defects and their causes.

The benefit of e-beam inspection are highly dependant on the speed improvements and the possibility to filter out the defects of interest.

Potential solutions must comprehend the need for greater amounts of defect-related data, e.g., composition, shape, defect classification, and rapid decision-making. ADC, spatial signature analysis, adaptive sampling, yield-impact assessment, and other algorithmic techniques still need to be improved significantly in order to be used to its full capability. Defect

detection and characterization equipment must produce more defect descriptive information for these techniques to analyze. The challenge of improved sensitivity to smaller defect sizes has moved characterization platforms in-line to provide higher resolution. This also applies to defect review including in-line EDX analysis. The trade-off between associated throughput and the provided information is crucial. Thereby, defect detection is evolving closer to the defect source. Development to integrate defect detection into process equipment must progress at faster pace to implement automated process control.

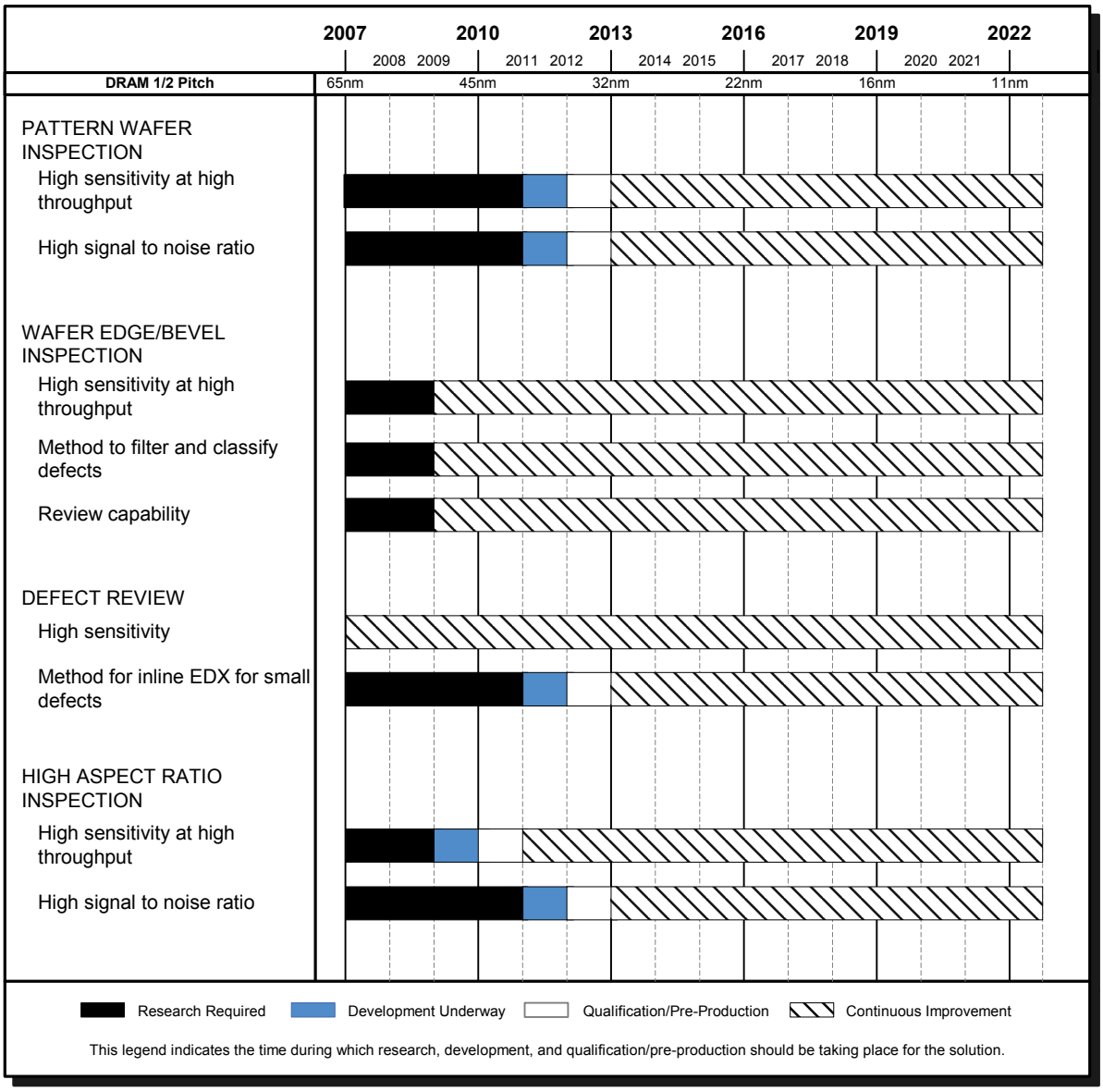

Figure YE3 Defect Detection and Characterization Potential Solutions

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and continue to enable cost-effective high volume manufacturing for device dimensions below 90 nm. Refer to Figure YE4. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning

chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Process critical materials—Figure YE4 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities.

In order to accelerate yield enhancement for processes that incorporate new materials, it is very desirable that development studies include purity data as much as is practical. Studies of new materials (e.g., for gate dielectrics) are initially concerned with basic process performance, and later with integration issues. During those stages of development contamination is a relatively minor concern. However, if no information is collected, later yield enhancement efforts proceed with inadequate technical basis. Collecting and reporting both environmental and material contamination data whenever practical will lead to long-term benefits.

UPW—UPW systems meeting specifications do not appear to be large defect drivers for current device geometries. Based on this the Roadmap does not predict that significant changes are required for future geometries. As a Roadmap priority, specific defect mechanisms related to UPW are required to drive significant changes. The current focus is to understand the impact of the tool upon water quality, specifically particles, bacteria, and dissolved gasses, as well as to identify species that are suspected to be in UPW but are below the detection limit of available measurement methods. Improved measurement methodologies are required for organics, and organic ions to specify low-level contaminants in UPW. Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water.

Chemicals—Figure YE4 shows various technological areas that may be required to enhance and measure the purity of delivered chemicals to the wafer manufacturing process.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low outgassing, and non-absorbing materials development are key to effective wafer isolation deployment.

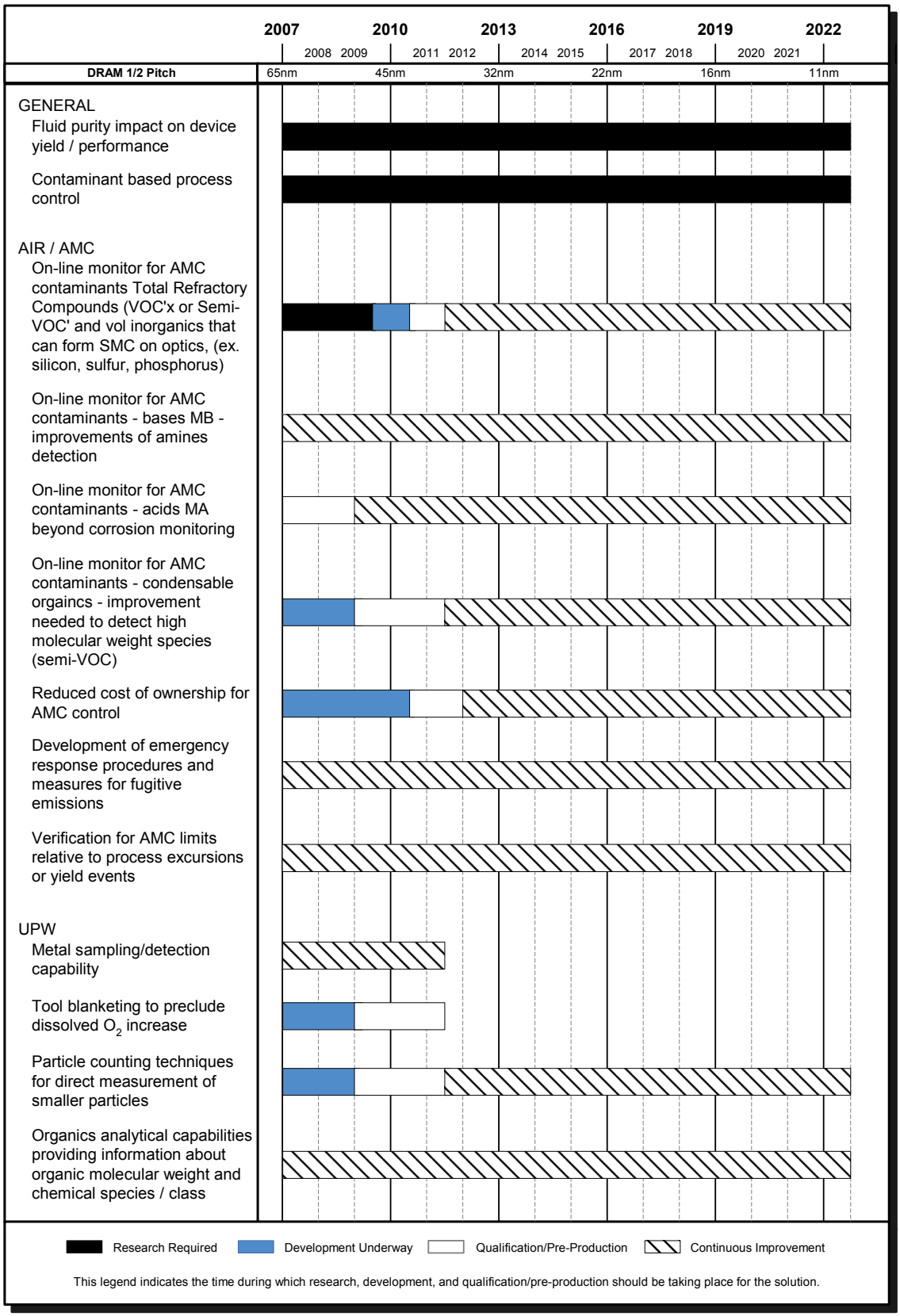

Figure YE4 Wafer Environmental and Contamination Control Potential Solutions

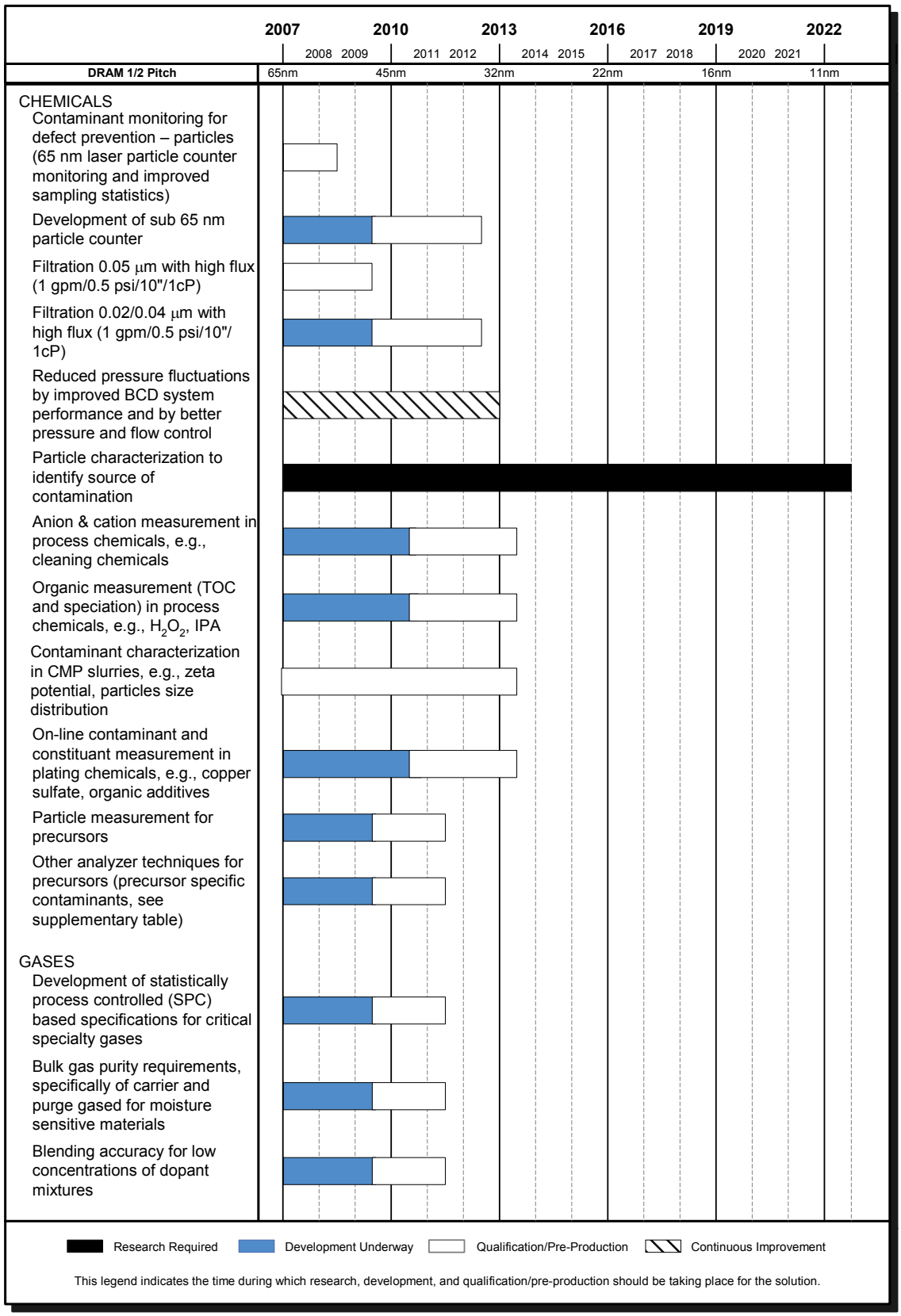

Figure YE4 Wafer Environmental and Contamination Control Potential Solutions (continued)