INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

ASSEMBLY AND PACKAGING

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ASSEMBLY AND PACKAGING

1. SCOPE

This chapter addresses the near term assembly and packaging roadmap requirements and introduces many new requirements and potential solutions to meet market needs in the longer term. Assembly and Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability.

Today assembly and packaging is a limiting factor in both cost and performance for electronic systems. This is stimulating an acceleration of innovation. Design concepts, packaging architectures, materials, manufacturing processes and systems integration technologies are all changing rapidly. This accelerated pace of innovation has resulted in development of several new technologies and both expansion and acceleration of others introduced in prior years. Wireless and mixed signal devices, bio-chips, optoelectronics, and MEMS are placing new requirements on packaging and assembly as these diverse components are introduced as elements for System-in-Package (SiP) architectures.

The electronics industry is nearing the limits of traditional CMOS scaling. The continued growth of the industry, driven by a continuous reduction in cost per function, will require new devices types, new package architectures and new materials. There will be a gap between the time CMOS scaling can no longer maintain progress at the Moore's Law rate and the time a new generation of device architectures and electronic material will support a continued drop in cost per function. As traditional Moore's law scaling becomes more difficult, innovation in assembly and packaging enabling functional diversification and allowing scaling in the third dimension must take up the slack.

Assembly and Packaging provides a mechanism for cost effective incorporation of functional diversification through System-in-Package technology. This technology enables the continued increase in functional density and decrease in cost per function required to maintain the progress in cost and performance for electronics. This will provide the principle mechanism for delivering cost effective functional diversification and thereby, equivalent scaling, to maintain the pace of progress.

New architectures including printed electronic circuits, thinned wafers and both active and passive embedded devices are emerging as solutions to market requirements. The materials and equipment used in assembly and packaging are also changing rapidly to meet the requirements of these new architectures and the changing environmental regulatory requirements.

This chapter is organized in eight major sections:

Difficult Challenges
Single Chip Packaging
Wafer Level Packaging
System Level Integration in Package (SiP)
3D Integration
Packaging for Specialized Functions
Advanced Packaging Elements
Environmental Issues

Wherever possible we have aligned the ITRS Assembly and Packaging chapter with other industry roadmap organizations including iNEMI, JISSO and IPC.

2. DIFFICULT CHALLENGES

There are a few key limitations faced by the Semiconductor industry in the near term that will involve most, if not all, of the Technical Working Groups (TWGs) that must be overcome. These are:

- Manage the power and thermal dissipation requirements by reduction of power requirements and improving the heat dissipation capability of the packages.

- Increasing the physical density of bandwidth in order to make use of the enormous gains in the physical density of processor power.
- Support the growing functional diversity requirements driven by More than Moore technologies.
- Support the reliability, power integrity and thermal management challenges of 3D integration.
- Drive down cost in assembly and packaging to reduce the impact of packaging cost not scaling to match device cost.
- Reduce time to market and by co-design and simulation that includes electrical, thermal, mechanical and in some cases chemical requirements fror the device, package and system.

The difficult challenges identified for the Packaging and Assembly Roadmap are presented in Table AP1. The challenges arising from the list above provide more specific granularity for these issues. Difficult challenges for geometries greater than 16 nm are presented in the table below. There has been a rapid pace of change in materials, processes and architectures to meet these challenges in the last few years and this progress continues. To maintain the rate of progress the difficult challenges in the table below must be overcome.

Table AP1: Assembly and Packaging Difficult Challenges

Difficult Challenges ≥16 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	– Direct wire bond and bump to Cu for very fine pitch due to thin wire limits)
	– Dicing for ultra low k dielectric (Includes k<2.5eff and air gaps)
	– Improved fracture toughness of dielectrics
	– Interfacial adhesion
	– Mechanical reliability for chip-package interconnect (requires co-design due to chip-package interaction)
	– Methodologies for measurement of critical properties needed.
	– Probe damage for copper/ultra low κ
Wafer level packaging	– I/O pitch for small die with high pin count
	– Solder joint reliability for tight pitch-low stand-off interconnect
	– Compact ESD structures
	– CTE mismatch compensation for large die and fanout die
Coordinated design tools and simulators to address chip, package, and substrate co-design	– Mix signal co-design and simulation environment
	– Rapid turn around modeling and simulation
	– Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis
	– Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching)
	– System level co-design is needed now.
	– EDA for “native” area array is required to meet the Roadmap projections.
	– Models for reliability prediction
Interposers and Embedded components	– CTE mismatch for large interposers
	– Defect density at very thin interfaces
	– Low cost embedded passives: R, L, C
	– Embedded active devices
	– Quality levels required not attainable on chip
	– Electrical and optical interface integration
	– Wafer level embedded components

Thinned die packaging	– Handling technologies for thin wafers (particularly for bumped wafers)
	– Impact of different carrier materials (organics, silicon, ceramics, glass, laminate core)
	– Establish new process flows
	– Reliability
	– Testability

The challenges for geometries below 16 nm include the items listed below. These challenges reflect the fundamental changes associated with continued scaling. The challenges are complex and will require substantial innovation.

Table AP1: Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≤ 16 nm	*Summary of Issues*
Close gap between chip and substrate, Improved Organic substrates	– Increased wireability at low cost
	– Improved impedance control and lower dielectric loss to support higher frequency applications
	– Improved planarity and low warpage at higher process temperatures
	– Low-moisture absorption
	– Increased via density in substrate core
	– Silicon I/O density increasing faster than the package substrate technology
High current density packages	– Low resistance contacts
	– Electromigration
Flexible system packaging	– Conformal low cost organic substrates
	– Small and thin die assembly
	– Handling in low cost operation
3D assembly and packaging	– Thermal management
	– Design and simulation tools
	– Wafer to wafer bonding
	– Through wafer via structure and via fill process
	– Singulation of TSV wafers/die
	– Test access for individual wafer/die
	– Cost of TSV
	– Bumpless interconnect architecture
Package cost does not follow the die cost reduction curve	– Margin in packaging is inadequate to support investment required to reduce cost
	– Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	– Electromigration at high current density for interconnect (die, package).
	– Thermal dissipation
	– Improved current density capabilities
	– Higher operating temperature
High frequency die	– Substrate wiring density to support >20 lines/mm
	– Lower loss dielectrics
	– "Hot spot" thermal management
	– Package substrates with lines and spaces below 10 microns.

System-level design capability to integrated chips, passives, and substrates	– Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult.
	– Complex standards for information types and management of information quality along with a structure for moving this information will be required.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	– Organic device packaging requirements not yet defined (will chips grow their own packages)
	– Biological interfaces will require new interface types
Power Integrity	– Power supply quality
	– Power delivery in stacked die
	– Reducing power supply voltage with high device switcihng currents

3. SINGLE CHIP PACKAGING

OVERALL REQUIREMENTS

Electronics and electronic products are being deeply woven into the fabric of our society. Without electronics, cars and trains will not move, planes would not fly, and certainly home appliances and home entertainment systems, and personal mobile devices (cell phones, smart phone, tablets), laptops and desktops and others would not function. From communications, commerce, transportation, energy, environment medical and health, electronics has provided the tools for operations, global productivity, innovation, improvement and sustaining of the standards of living for people everywhere.

The ubiquitous electronic components continue to find applications in traditional markets for data processing, communication networks and computing, military and aerospace as well as new applications in personal communication such as smart phones and PDA, game consoles, home and home entertainment, medical and health care, energy and environment, automotive, and security systems. New device categories such as light emitting diodes, photonic devices, MEMs and other sensors add families of integrated circuits for packaging and assembly into electronic components. The advent of cloud computing coincide with double digit growth in bandwidth requirements accentuate the demand for high performance network systems and servers which provide the backbone structures to global internet traffic and data flow.

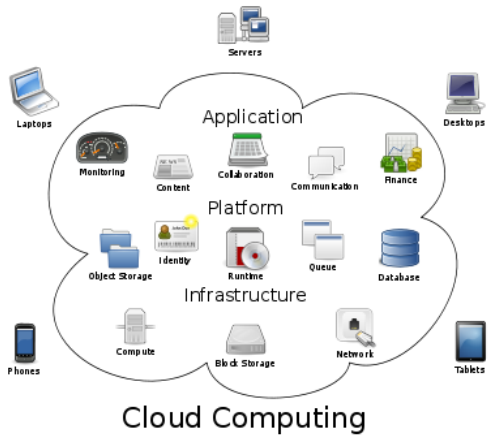


Figure AP1: Hardware Components of Cloud Computing

The dynamics of market requirements and new device types led to requirements for new packaging technologies and new packaging architecture. In this chapter the packaging and assembly technology requirements are divided into devices serving five different market segments:

- Low cost low end: Low end consumer electronics and memory, e.g. electronics in household appliances, toys, MP3, DVD players, portable hard drive products, electronic books, and cell phones.
- Mobile Products: Smart phones, high end cell phones, portable personal devices, portable video systems.

- Cost Performance: PC, notebook, tablets, and high-end electronic books, Blade server and processors, game consoles, and small business routers and servers.
- High End: High performance servers, routers and network systems and computers.
- Harsh Environment: Automotive, aerospace, and military systems.

There will be gray areas between the five market segments. While the very low end cell phone belongs to the low end market, it is, by definition, part of the mobile market. And the game consoles performance rival those of blade servers. Tablets and electronic readers are duplicating functions in market competition. The market momentum for mobile video entertainment is elevating the speed and bandwidth for mobile products and drive the speed, bandwidth and capacity of network system infrastructure, and server farms. The advent of cloud computing connects mobile intelligence platforms with fixed network infrastructure and database, blurring the boundary between the market segments in functions, form factors and price points.

For each of the five market segments, their technology requirements, cost per pin, die size, power, package pin count, operating characteristics, and environments, have been addressed in Table AP2. Where solutions are not proven or unknown, they will be color coded to show the solution status. In many cases the reason for the color is not that the parameter cannot be met, but that the cost of implementation would be beyond the cost targets for that specific product segment.

Table AP2: Single-chip Package Technology Requirements

The technology requirement for the Cost Performance Market has been the leader for package technology innovations in the past decade with the drive for performance in notebooks, game consoles, routers, and servers as the technology nodes advances while keeping cost at bay. The leading package technologies are flip chip ball grid array organic packages with large die and high density. The issues have been performance, heat dissipation, reliability and cost.

The dramatic rise of the mobile market with smart phones, tablets, portable personal devices, and portable entertainment systems has brought up a different set of technology challenges in form factors (height and size) and weight, functional diversification such as RF and video, system integration, reliability, time to market, and cost. The packaging community has responded with wafer level packaging, new generations of flip chip CSPs, various forms of SiP including 3D stacked die and stacked packages, fine pitch surface mount, silicon and glass interposers (2.5D) and 3D IC. They illustrate the dynamic nature of the Packaging and Assembly world in "More Moore" and "More than Moore". The dramatic escalation and gyration in the price of gold works against consumer market expectations for cost reduction. It has given great impetus to the conversion from gold wire bond to copper wire bond. As the experience in conversion from lead solder materials to non-lead solder materials, the replacement of gold wire by copper wire in fine pitch wire-bonding lead to a very significant set challenges in new assembly process development, a whole set of material changes and equipment infrastructure. In Cu wirebond the industry is seeing major challenges in what commonly perceived as "mature" technology with well-established manufacturing infrastructures. For flip chip technologies the transition from lead based solder to lead free solder, and the implementation of low-κ d e-low-κ and ultra low-κ dielectric and finer bond pad pitch adds a new set of challenges to the packaging technologists. With flip chip moving towards cu pillar bumping for reasons of finer pitch and lower cost solutions, one would find that new materials set and different assembly process and equipment would be required. In wafer level packaging WLCSP is the fastest growing packaging type driven by the mobile phone market. This packaging technology is being re-invented to expand its application space in response to market demand for minimum package thickness and small form factor.

ELECTRICAL REQUIREMENTS

Manufacturing tolerances have a major impact on the performance of electrical designs. The manufacturing tolerance roadmap reflected by the tables, for via diameter, via alignment, metal thickness, line width and dielectric thickness must be aligned with the electrical requirements. The major issues defining requirements for single chip packages are discussed below.

CROSS TALK

Circuit speed and density continue their improvements from one CMOS generation to the next. Faster circuits translate into shorter clock cycles and increased density gives rise to more closely spaced parallel threads. These

device advancements demand increased package I/O at ever-increasing speed. These advanced circuits require packages that minimize device, package, and system noise.

A major noise source is crosstalk between parallel signal lines. Crosstalk noise is roughly proportional to the ratio of dielectric thickness to edge spacing between adjacent signal lines. For a given signal line width and spacing, a lower dielectric constant medium requires a thinner dielectric to obtain the same characteristic impedance, resulting in smaller crosstalk noise. Cross talk issues are also associated with fine pitch bonding wires and fine pitch vias.

POWER INTEGRITY

Power integrity issues are becoming more critical for high-speed integrated circuits as frequency and increases and operating voltage decreases. Discrete decoupling capacitors are extensively used today to damp AC noise. The Equivalent Series Inductance (ESL) associated with discrete capacitors is the major factor limiting performance at high frequency. Embedded planar capacitors and on-die decoupling cells are used to reduce high-frequency noise due to high ESL in discrete capacitors. The cost and complexity of on-die decoupling will be an increasing problem. Due to resonance between package and die and package and PCB, it is difficult to control power distribution impedance over a wide frequency range. This results in a packaging related bottle-neck in high-speed power delivery system design and new technology is required.

THERMAL REQUIREMENTS

Temperature control is critical for the both operating performance and long term reliability of single chip packages. The high junction-to-ambient thermal resistance resulting from an air-cooled heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of this roadmap. Today, a massive heat sink, which may be larger than the chip by orders of magnitude, is attached to a silicon chip through a heat spreader and variety of thermal interface materials (TIM). Not only does this insert a large thermal resistance between the chip and the ambient, it also limits the chip packing density in electronic products thereby increasing wiring length, which contributes to higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses. The ITRS projected power density and junction-to-ambient thermal resistance for high-performance chips at the 14 nm generation are >100 W/cm^2 and <0.2°C/W, respectively. The main bottlenecks in reducing the junction-to-ambient thermal resistance are the thermal resistances of the thermal interface material (TIM) and the heat sink. There is a need for TIMs that provide the highest possible thermal conductivity, are mechanical stable during chip operation, have good adhesion, and conform to fill the gaps between two rough surfaces. To address this need, new TIMs are being explored. The integration of carbon nanotubes (CNTs), which exhibit very high thermal conductivity, within a TIM's matrix is being investigated. More details may be found in the Emerging Materials chapter. The die stacking 3D and interposer (2.5D) package architecture give challenges thermal solutions in limited space for thermally designed package solutions. There has been a commonly held assumption that mobile devices, powered by batteries would not require thermal management solutions. With stacked POP design packages and 3D architecture, thermal design will be an important technical challenge.

HOT SPOTS

Hot spot thermal management generally dictates the thermal solution of the component. Even when the total power of a component is unchanged, hot spot power density increase could limit the device performance. While this is a critical issue for SiP it is also important for single chip devices such as SoC circuits, high power lasers and diodes, RF devices and other high power devices that have portions of the die generating thermal loads substantially higher than the die average.

New liquid and phase change (liquid to gas) active heat sinks are in limited use today and are addressed in more detail in the System in Package section of this chapter. They hold the promise of decreased thermal resistance and improved heat spreading capability to address the effect of hot spots.

MECHANICAL REQUIREMENTS

The constant drive for increased functionality and flexibility in the end product will be the key driver for the electronic industry in future. With shorter design turns and faster time to market, there is little room for error during the design, development, and validation phases. The continued geometric scaling of integrated circuits and the introduction of low-κ and e-low-k dielectric film materials raise serious concerns about mechanical stress damage in the dielectric layers due to thermo-mechanical stresses in the combined package device structure. Chip package interaction (CPI) has become a major area for trade off between die designers and packaging engineers. Legislative

requirements for lead free and halogen free materials in electronic products introduced higher temperature stresses and new packaging materials and materials interfaces into the package. New package types including stacked die packages, Package on Packages (PoPs), Package in Packages (PiPs), and wafer level packages have brought forth new failure mechanisms. This is especially true for 3D TSV and interposer based packaging architectures.

Consumers in the mobile market demand more functions and faster performance in thin handheld size package. Stacked die and stacked packages are by its very nature "thickness challenged". The drive for reducing package thickness across the different package types poses challenges in architecture, materials and design innovations.

The packaging industry will face the challenge of integrating multiple device technologies such as digital, RF and MEMS, optoelectronics, displays and others on the same packaging platform. Expanding consumer markets introduced new paradigms in reliability requirements. For example drop tests, in various forms, are being added to components to be used in cell phones and other portable electronic products. To ensure reliability of the end products, it is imperative to have focused R&D efforts in mechanical and thermal modeling and simulation tools.

MECHANICAL MODELING AND SIMULATION

Electronic packages represent a classic case of convergence of multi-scale, multi-physics, multi materials, and multi-materials interface systems. The length scale varies from nm to cm, a wide range of materials with mechanical properties from stiff and brittle inorganics like Si, glass and other dielectrics with property modifications such as micro-pores to achieve low-κ, to softer materials like solders or polymers and polymer composites with very non-linear time and temperature dependent material behaviour are combined. Material response varies from elastic to non-linear in time-temperature dependent characteristics. It is critically important to have practical and usable tools for predictive thermal mechanical and dynamic modeling of electronic packaging structures to assist packaging engineers in predicting failure modes and elucidate the failure mechanisms in the development stages. This would enable trade-offs in design, materials and manufacturing processes, and ultimately in feature, performance, cost, and time to market. Such predictive modeling tools would need to be integrated into device package co-design environments. Coupled analysis for thermal, electrical, hydrothermal, and mechanical characteristics is also needed.

Accurate experimental techniques to observe and experimentally measure mechanical deformation such as package and die warpage will be very important to observe the package deformation phenomena and to quantitatively verify the physical models. Warpage has been typically defined as the largest value of non-planarity. For full understanding of package deformation full field warpage including z and x-y deformation will be highly desirable.

To complement mechanical analysis and modeling efforts, it is necessary to develop accurate materials properties data over a range of loading and environmental conditions. Characterization of interface properties such as polymer/metal and polymer/polymer interface fracture toughness and micromechanical properties is required. A key challenge in this area is associated with the small dimensions. Bulk properties are often not usable for thin material layers. Interface effects, grain size and pre-stresses due to process or adjacent materials become very important. Metrologies are needed that can handle thin films of sub-micron thickness to measure both bulk and interfacial response. Properties of materials such as intermetallics formed from solder under bump metallurgy (UBM) metals interaction which grow and evolve over time and temperature will be required. Physical failure mechanisms such as electromigration, thermal migration in combination with mechanical stresses need to be understood and modeled for practical life assessment.

There is also a need to develop metrologies that can be used to efficiently measure either stress or strain under both thermal and mechanical loading conditions in thin films (for example in layers within Silicon) in packaged form. For example, interferometry-based techniques with sub-micron resolution are required whereas the current state of art methods have spatial resolution of 1 to 2 μm. Efforts are needed in extending other known techniques such as digital image correlations, micro-Raman spectroscopy, and PZT sensors to sub-micron length scales.

COST

The continuous reduction in cost per function has been the key to growth of the electronics industry. This has been achieved historically through scaling of the wafer fabrication processes and improvements in design. The cost of assembly and packaging has not kept pace with the cost reduction in wafer fabrication and today packaging costs often exceed silicon IC fabrication cost. The cost reduction challenge is made more difficult by several factors increasing cost of packaging. Cost of packaging materials such as bonding wire, molding compound, substrate,

leadframe, contributes substantially to the cost of the package. The cost of gold wire is a substantial portion of the package cost. With the dramatic escalation of gold price, maintenance of package cost requires game changing strategies such as the high level of momentum shifting to copper wire from gold wire. Reducing cost is a important motivation for innovations from flip chip CSP to WLCSP.

Lead-free solder materials, halogen free molding compounds, low-κ dielectrics, and high-κ dielectrics are more costly than the materials they replace. Higher processing temperatures and a wider range of environmental temperature associated with portable consumer electronics require new, more expensive, substrate and interconnect technology. The increasing power density and decreasing junction temperature require more efficient thermal management. The details of the chip to package substrate technology are covered in Table AP3 and the specific issues associated with package warpage during processing are covered in Table AP4. The changes in substrate to board pitch are covered in Table AP5.

New technology is required to meet the demand for more cost effective packaging. Wafer-level packaging and systems in a package (SiP) are among the innovative approaches to reduce cost and achieve advantages of scaling similar to the front end processes.

Table AP3: Chip-to-package Substrate Technology Requirement

Table AP4: Package Warpage at Peak Processing Temperature

Table AP5: Substrate to Board Pitch

RELIABILITY

Rapid innovation in packaging is evident from the introduction of new package formats including area array packages (flip chip BGA and flip chip CSP); leadless packages, direct chip attach, wafer level packaging (WLP), wirebond die stacking, flip chip Cu Pillar and FC-wirebond hybrid, PoP, PiP and other forms of 3D package integration. With 3D TSV and Silicon or Glass Interposers, new failure mechanisms and package risks needs to be identified. In addition there are new packaging requirements emerging such as Cu/E low-κ materials, interconnects to address the need for flexibility and expanding heat and speed requirements. The introduction of low-κ and e-low-κ materials makes the low κ layer in the chip susceptible to mechanical stresses in the combined chip package structure. New environmental constraints such as Pb-free and halogen-free requirements enforced by law, and use of electronics in extreme environments also force rapid changes. The introduction of these new materials and package architectures are posing new reliability challenges. For example in the flip chip package the interaction of the stiffer Pb free solder bump to the mechanically weaker low k dielectric requires chip and design and materials selection to address reliability risks in chip to packaging interaction (CPI). This comes at a time when there must be substantially higher reliability on a per transistor basis to meet market requirements. Many of the reliability issues involve the Chip to Package Substrate Technology which is covered in Table AP3.

Some new package designs, materials, and technologies will not be capable of the reliability required in all market applications. More in-depth knowledge of failure mechanisms coupled with knowledge of end product use conditions will be required to bring reliable new package technologies into the market-place. For example mobile products have drop test requirements for dynamic mechanical integrity in drop impact environments.

There are many factors that determine the reliability of electronic components. The factors that must be considered are similar for all systems but the relative importance changes for consumer products. Consumer products have higher thermal cycle count due to the use pattern of consumer electronics and greater mechanical stress due to vibrations and dropping for the same reason. Typical package failure modes are presented in Table AP6.

Table AP6: Package Failure Modes

The storage and use environments also have a wider range than components not used in consumer applications. Meeting the reliability requirements for future components will require tools and procedures that are not yet available. These include:

- Failure classification standards
- Identification of failure mechanisms
- Improved failure analysis techniques

- Electrical/thermal/mechanical simulation
- Lifetime models with defined acceleration factor
- Test vehicles for specific reliability characterization
- Early warning structures

As described earlier, the use of low-κ ILD to reduce on-chip interconnect parasitic capacitance has exacerbated the difficultly of maintaining high thermomechanical reliability of die assembled on organic substrates in flip chip packages. Due to the fragile nature of low-κ ILDs in the die and their relatively poor adhesion to the surrounding materials, it is becoming progressively critical to minimize stresses imparted on the chip during thermal cycling and wafer-level probing. The large CTE mismatch between the silicon die (3 ppm/°C) and the organic substrate (17 ppm/°C) have been shown to be destructive for ILD materials and their interfaces. This issue has motivated the investigation of new I/O interconnect technologies that minimize mechanical stresses on the chip. The pending replacement of lower modulus lead solder bump material by lead free solder bump material or copper pillar makes the problem more difficult. To this end, the device and package communities must collaborate together to address the chip package interaction issue in the design of UBM structure, solder bump or Cu pillar, underfill materials, and surface finishes. In addition, the use of solder bumps augmented with mechanically flexible electrical leads to replace underfill is a potential solution.

In addition to compliant/flexible interconnects, thin solder interconnects and micro-bumps (diameter: <20 µm) as well as Cu pillar bump structures (Figures AP2 and AP3) are used to improve interconnect reliability. The selection of the type will depend on die sizes, thickness and interconnect density.

Moving forward reliability considerations of dies with TSV and microbumps will pose significant challenges to the chip and package designers and their reliability counterparts. This will be addressed in future editions for the roadmap.

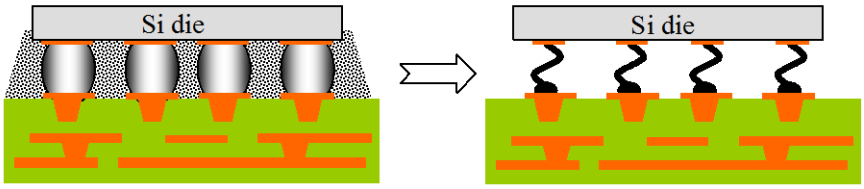
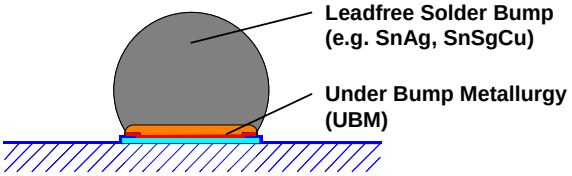
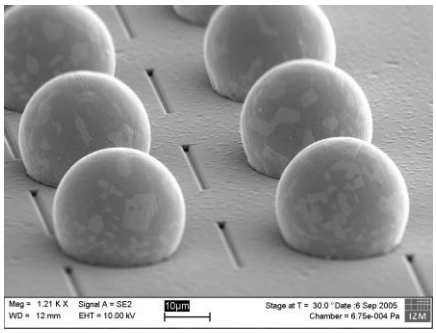


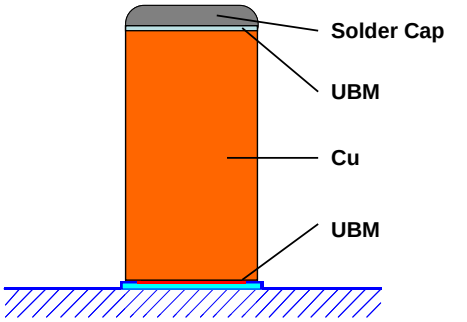
Figure AP2: The Use of Compliant/Flexible I/O Can Potentially Eliminate the Need for Underfill



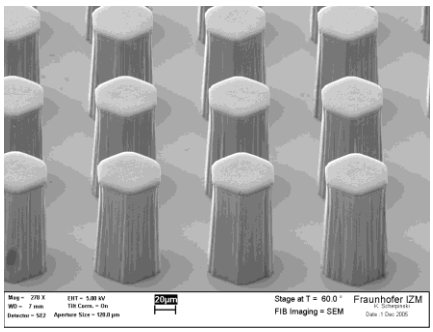
Schematic construction of a solder bump



SnAg microbump (20 µm diameter)



Schematic construction of a HAR (High Aspect Ratio) Cu pillar bump with solder cap



Cu pillar bump (height: 80 µm)

Figure AP3: Micro Bump and Pillar Bump Structures for High Reliable Chip-to-Substrate Interconnects

CHIP TO PACKAGE SUBSTRATE

There are several factors that drive the selection of the appropriate chip to package substrate technology. The issues are addressed in Table AP3 Chip-to-package Substrate Technology, Table AP4 Package Warpage at Peak Processing Temperature, and Table AP5 Substrate Board Pitch. The specific technologies are discussed in the sections below.

INTERCONNECT TECHNOLOGIES FOR SINGLE CHIP PACKAGE

Single Chip package is till the volume leader, and wirebond and flip Chip continue to be the two basic interconnect technology for the semiconductor packaging industry. Today in IC packaging (excluding LEDs, MEMs and discretes) wirebond serves as the basic interconnect technology for 87% of the unit in production and flip chip interconnect serves as the basic interconnect technology for 12% of the units in production. In terms of package value the ratio is about 70% and 20%. There has been major and significant innovations in both interconnect technologies in the last few years in response to dynamic market requirements and technology node advancement.

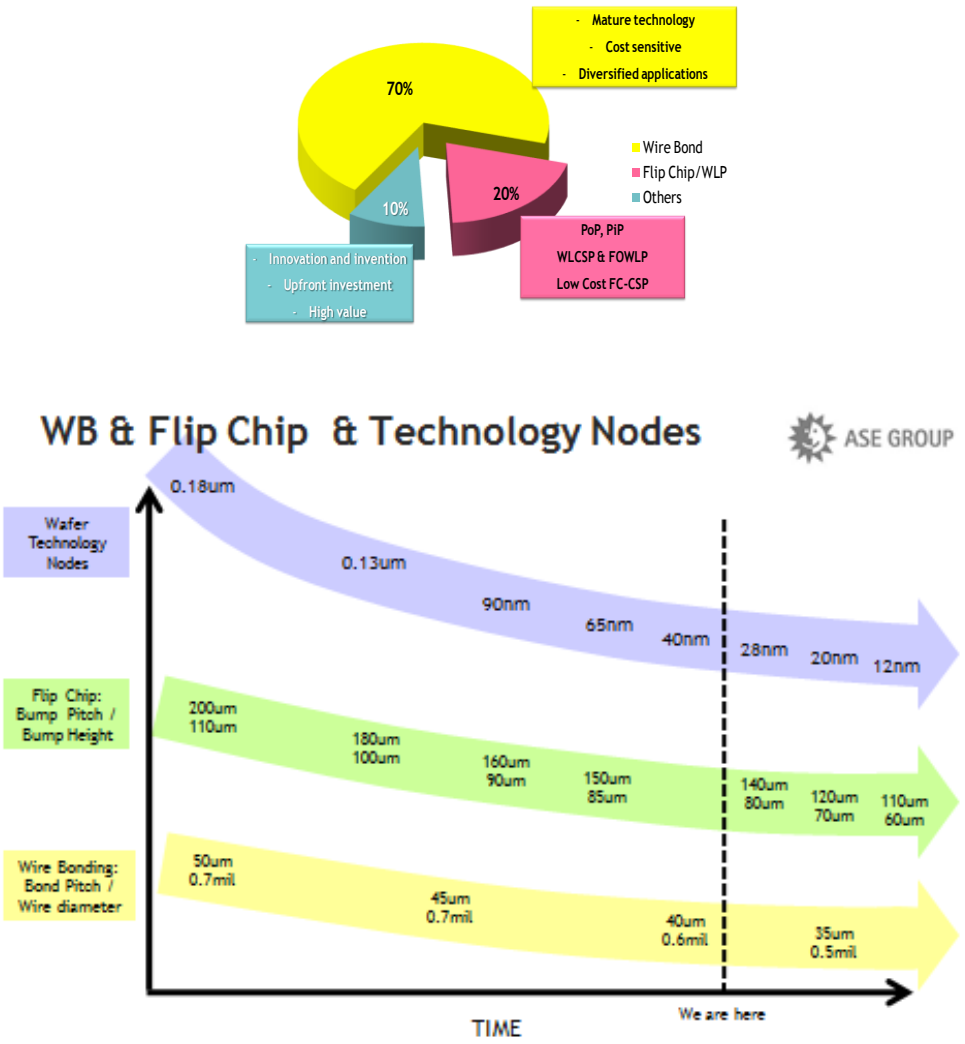


Figure AP4: Wirebond and Flip Chip Pitch versus Technology Nodes

WIRE BONDING

Wire bonding has been the workhorse of the semiconductor industry. It is the dominant method for interconnecting to semiconductor device. IC devices, wire bonded to various forms of lead frames and organic substrates and molded in epoxy molding compounds have been the standard of the industry for years. Despite repeated predictions that wire bond technology has reached its practical physical limit, wire bond technology continues to re-invent itself with new innovative concepts and technology improvements. Today it has been estimated that 70% and more of the world semiconductor components are packaged in wirebond.

In the last few years year the replacement of gold with copper wire in fine pitch wirbond packages has moved into mainstream. A majority of new wirebond packages will be using Cu wire and PdCu wire. And momentum is building to convert Au to Cu (including Pd Cu) in existing packaged components. The implementation of Cu wirebond requires changes of almost the entire packaging materials set, and assembly manufacturing equipment infrastructure. In other words the industry has completely re-invented the wirebond technology in bonding wires, in wire bonders, in molding compounds, and in the manufacturing infrastructure. The implementation for Cu Wire is remarkable in the rapid market acceptance to a major high volume manufacturing technology change.

Replacement of Au wire by Cu is being implemented across both generic package types, e.g. leadframe and PBGA. At the same time the introduction of advanced nodes and low κ materials will demand finer diameter wires for Au as well as Cu below the 18 um being practiced today. While copper wirebond has been in use for power devices with

50 micron diameter wires and low IO counts, fine pitch Cu wirebond is a recent development. Fine pitch applications with Cu wire diameters at 25 micron and below requires improvements in understanding of wire properties, IMC formation and evolution, wire bonding processes and equipment development and control for wire oxidation.

Pd coated wire has been introduced to eliminate the need for forming gas in production.

Multi-tier wire bonding has provided good practical solutions to meet increased IO requirements. Wire bonded stacked die packaging, typically with two to five vertically stacked dies with a leadframe, laminate substrate or flex circuit base has proven to be particularly versatile method for multi-chip or SiP in the mobile market. While the majority is for various memory to memory combinations, a significant proportion involves memory stacked with logic devices. The developments that enabled die stacking package include wafer thinning, low profile wire bonding, mold compound flow and filler size, and wafer level test for known good die. Shown below is example of stacked die Cu Wirebond structure with 15 µm Cu wire.

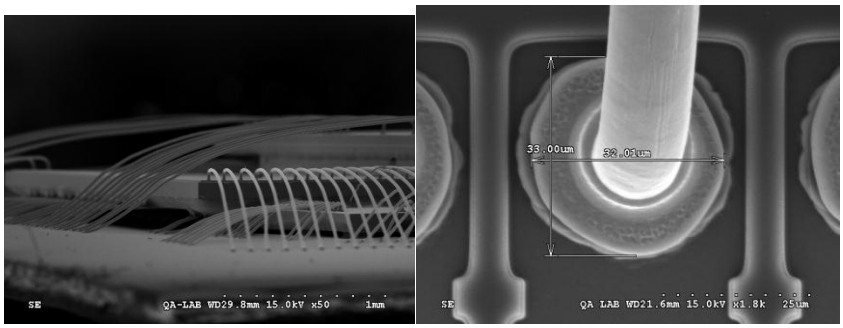


Figure AP5: Example of 15 µm Cu Wire Bond with Die Stacking

In order to meet thinner and more densely integrated package requirements lower profile wire bond loops are necessary. Innovations such as forward bond loops with 50 µm loop height are in production. Other innovations such as die to die bonding and cascade bonding are shown in Figure AP6. While many of these developments have been in production for Au wires, it is expected that these capabilities would be extend Cu wirebond in time.

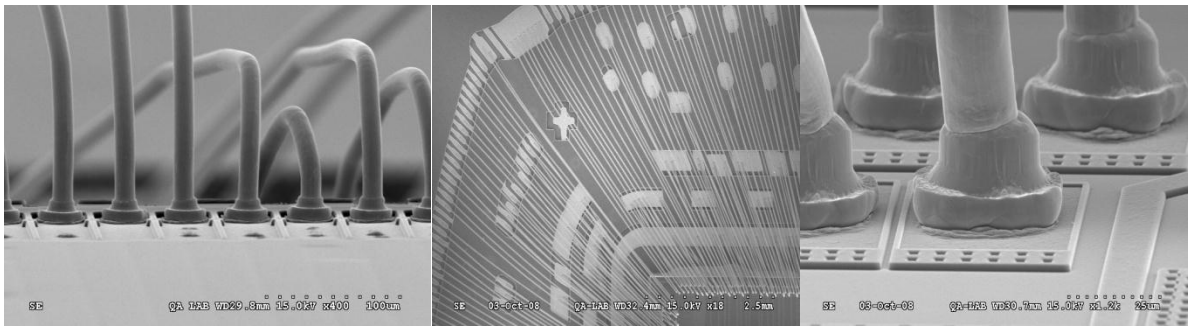


Figure AP6: Example of Multi-Tier Cu Wire Bonding with 847 Lead PBGA

Some of the technology issues being addressed are bonding overhang die and wire bonding on both sides of the lead frame shown in Figures AP7 and AP8.

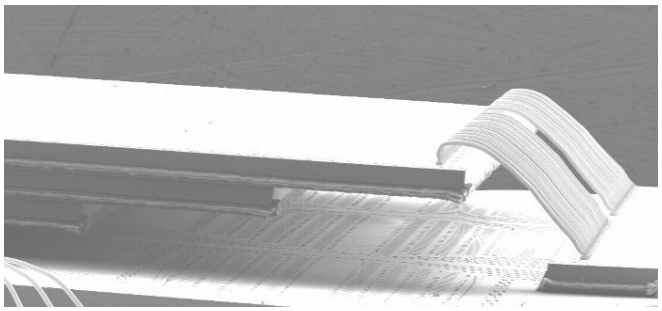


Figure AP7: Bonding Overhang Die

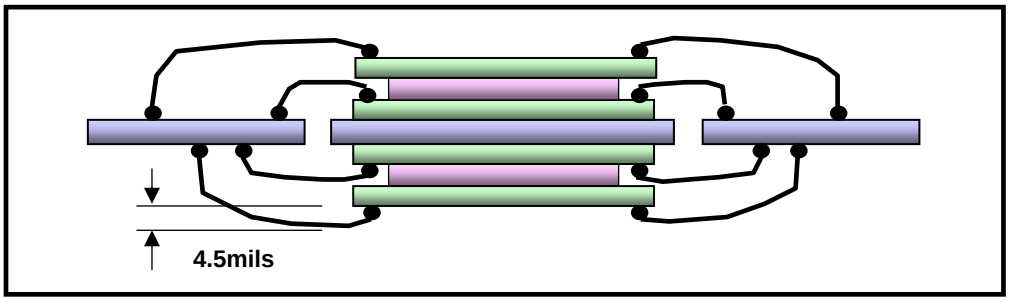


Figure AP8: Wire Bond on Both Sides of Lead Frame Substrate

There is a well-established global infrastructure and supply chain for wire bonded and molded packages from design practices and tools, materials, manufacturing processes, and equipment. The industry has been developing faster wire bonders, larger format substrate assembly, and more efficient molding processes to address the market demand for efficiency and cost saving. The next few years will see significant innovations in design, process, materials and equipment for the implementation of Cu wirebond. As the wafer technology approaches 45 nm node and below, the bonding wire diameter will be reduced correspondingly to 20 nm and below. In the long term such cost improvements efforts may be approaching their practical limits and are of diminishing returns.

FLIP CHIP

Flip chip and wire bond are the two standard processes to connect die to a substrate. Flip chip PBGA processes evolve from technologies originally developed for multi-chip applications on ceramic modules with high lead solder bumps. It has become the standard die interconnect solution for organic substrates for microprocessors and graphics processors in the cost performance and high end markets. The key elements are: wafer bumping (UBM and bump metallurgy), underfill, TIM, and build-up substrates. For these applications flip chip pitch, lower than 150 μm, has been limited by availability of high-volume cost-effective substrates and high-volume defect-free underfill processes, with higher Pb-free temperature, higher Tj, and increased current density, there are requirements to improve underfills, UBM structure, high lead solder, eutectic and lead free alternatives, and TIM materials in order to meet the demands of future technology nodes and market applications. Plated wafer bumping including copper pillar wafer bumping is being introduced in microprocessor applications and will be expanded to broader applications. The advantages are in finer pitch, lead free and electrical/thermal performance.

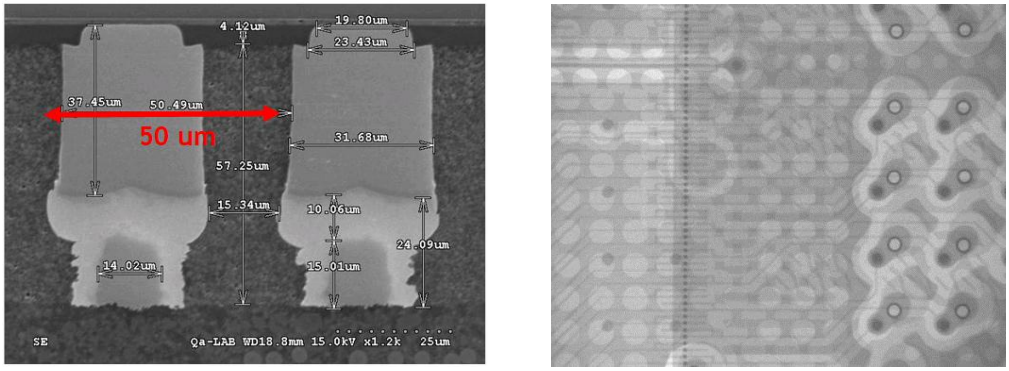


Figure AP9: Examples of Copper Pillar Bumps (a) and Assembled Copper Pillar (b) X-Ray

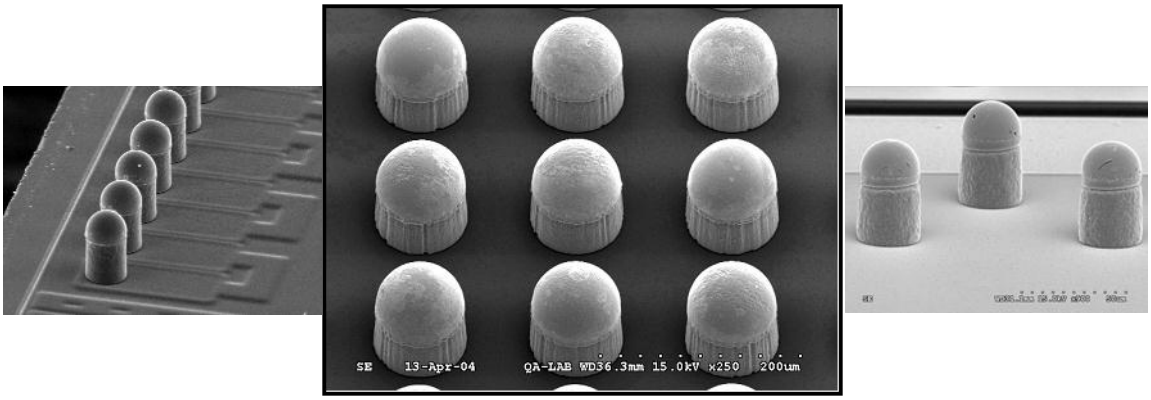


Figure AP10: Example of Copper Pillars with Solder Tips Single Line 50 µm Pitch (staggered (100 µm)

For applications beyond the microprocessor, graphics and game processors, flip chip FC CSP packages have been developed for applications with smaller die, lower IO array pitch and low profile small package format requirements. Primary driver has been the mobile market application, and drop test is an important requirement. Laminate substrate and 1+2+1 buildup substrates are used to meet cost targets. To save cost of redistribution process the bond pads would remain in peripheral single line or staggered. These flip chip CSP packages may have multiple dies side-by-side or they may be stacked onto other flip chip and wire bond packages. Analog and RF ICs have different electrical requirements than digital only applications. The industry has developed several package variations to meet different application requirements, In addition to the classical capillary underfill process, they include molded underfill and underfill plus molding processes. The large format molded underfill process provides significant cost saving. Potential solutions include redesigned UBM, copper pillar or flexible interconnect, fluxless reflow and PoP and PiP package structures. There is a movement for a new generation of flip chip structures, materials, manufacturing processes and equipment sets to serve the industry for the More than Moore era. A good example is the flip chip CSP package with copper pillar bump, bond on lead assembly process, molded underfill with low cost laminate substrate in large format.

MOLDING

Conventional bottom-gate molding has been a highly successful workhorse for the industry. For some complex stack dice and complex SiP package there is risk for excessive wire sweep and yield loss. Recent industry adoption in top center mold gate (TCMG) process provides a radial mold compound flow from a top gate that minimizes wire sweep

and filler separation that can occur as the fine pitch bond wires filter out part of the fillers as the compound moves between them.

Also compression molding is entering the mainstream. The liquid mold compound is dispensed onto the substrate before it is placed into the mold die. No gate is needed and the mold flow speed is minimized preventing wire sweep. Lower cost powder molding compound developed for compression molding process is coming on board.

Thin packages are prone to warpage, and chips with low-κ dielectrics are more sensitive to stress. In both cases, low modulus molding compounds are in development to minimize the problems.

A novel approach to reduce or eliminate the occurrences of wire shorts in molding is the use of coated wire. Coated wire has been in development for some years and has achieved some level of technical success. However the high cost of coated wire has limited its application and prevented its broad proliferation into the industry.

PACKAGE SUBSTRATE TO BOARD INTERCONNECT

LEAD FRAMES

Lead frame carriers have thrived for their low cost and good reliability for more than 30 years. They are expected to continue to thrive with innovations in package design and processes. New material related challenges appeared because environmental and health regulatory requirements demand the elimination of Pb. The move from Pb to Sn led to the challenge of tin whiskers. For improved reliability and low-cost new plating materials are required, e.g., based on NiPd, Cu, lead-free solder alloys. Other challenges include improved heat dissipation and higher interconnect density including increased pin count capability for platforms such as QFN and QFP. Innovations in advanced multi-row QFN has extended the I/O and performance for QFN packages.

HIGH DENSITY CONNECTIONS

The density of connections between the package substrate and the system printed circuit board continues to increase and the size of devices for a given functionality and the number of contacts required continues to increase. The Roadmap for chip to package substrate pitch is found in Table AP3.

The increase in pin count is driven by the requirement to maintain power integrity and the increasing width of the data communication. Ensuring power integrity in an environment where operating voltage is decreasing and the number and speed of the transistors is increasing requires a larger number of contacts to handle the larger current spikes without fluctuations in power or ground. The slow improvement in board line width and spacing would provide some board routing density increase, but there is better opportunity for this density increase by reducing BGA pad pitch on board and package.

The greatest contact density in conventional packages will be available for the fine pitch ball grid array (FBGA) packages which are projected to reach 100 µm area array pitch in 2014. The higher density and resulting smaller pads bring issues related to joint reliability and package ball co-planarity requirement. The joint reliability needs to be achieved through innovations in pad design, innovations in solder metallurgy and surface finishes, and in some cases use of board level underfill. The co-planarity issue needs to be addressed through improvements in substrate material and design, better understanding of package behavior at high temperature, and working with process flow to do key co-planarity sensitive operations prior to solder ball attach. The package to printed circuit board pitch for existing package types is presented in Table AP5. Greater contact density will be in use for die-to-system substrate and die-to-die interconnect architectures using TSV structures.

PACKAGE SUBSTRATES

Package substrates are both the most expensive element of packages as well as the factor limiting package performance. Innovation in package substrate technology is required to meet the cost and performance projections of the Roadmap. The substrate properties required to meet each market demand are shown in Tables AP7 through AP12.

FOR LOW-COST APPLICATIONS—LAMINATE FOR PBGA

PBGA is a relatively large-size package and mostly used for low-cost applications, demanding substrates in low cost, high volume production, and are mostly two- or four-metal layer laminates. Table AP7 shows the roadmap of laminate for low-cost applications. Their roadmaps tend to be moderate based on the traditional manufacturing

processes with critical cost constraints. Increasing strip sizes are the trend of package substrates to provide higher productivity in package assembly and materials utilization. Assembly equipment must meet the increasing strip sizes, e.g., molding press must be designed to have larger die-set bases with higher clamping pressures. Equipment suppliers need the guidelines for increasing strip sizes, although they differ among package manufacturers. Lowering material costs is another challenge. The core material of the substrate, high Tg FR4, dominates the physical property of package substrate; thus, package manufacturers are accustomed to specify the product number of core material for their substrates. Standardizing the properties of core materials and substrate frame size is necessary to accelerate the market competition. In terms of quality requirements, package warpage during reflow is a significant problem for this package due to its large body size. One of the approaches to reduce package warpage during reflow is matching the properties of the substrate and molding compound. Lower CTE and higher fracture modulus of the substrate will mostly mitigate the warpage.

Table AP7: Package Substrates:Low Cost (PBGA)

HAND-HELD APPLICATIONS—FINE LAMINATE FOR FBGA

Handhelds are driving ever thinner substrates and finer patterns with laminate (See Table AP8). These requirements result can drive smaller panel sizes in substrate manufacturing processes for accurate alignment and finer pattern as one solution. Total thickness has been reduced to 100 µm based on 60 µm cores in high volume manufacturing. 50 µm cores and 35 µm prepregs are available but cost is still high and improvements in handling equipment are needed to take these materials to high volume. Below 35 µm thickness, new high performance low cost material is required to meet the market needs.

Table AP8: Package Substrates: Hand-held (FBGA)

MOBILE APPLICATIONS—BUILD-UP SUBSTRATE FOR SiP

Mobile packages with wire bonded die are utilizing high density substrates with blind vias in laminate, essentially a build-up technology using prepreg instead of unreinforced resin. To achieve finer resolution (See Table AP9), glass cloth with more uniform glass fiber density or glass mats will have to be developed while overall thickness of the resultant prepreg has to be reduced below 40 µm. Thereafter, film forming resin systems with wire bonding resilience after lamination will have to be developed. In general, the lack of the latter type of materials is impeding the improvement of resolution of lines and spaces. The pattern formation itself is shifting from a subtractive process to pattern plating.

Table AP9: Package Substrates: Mobile Products (SiP, PoP)

Mounting flip chip die and wirebond die on the same package, either side by side or stacked, provide challenges for substrate surface finish. A number of finishes can coexist: organic solder preservative (OSP), immersion tin or pre-solder with electroplated nickel/gold versus electroless nickel immersion gold (ENIG) with electroplated nickel/gold. Each case requires a carefully tuned assembly and substrate manufacturing process to be successful in high volume. Hence, the search for a universal surface finish has been reinvigorated and electroless nickel electroless palladium immersion gold (ENEPIG) seems to be the most likely candidate. This surface can be wire bonded, flip chip soldered as well surface mount soldered. The cost of this universal finish seems to be competitive with mixed finishes.

COST PERFORMANCE APPLICATIONS—BUILD-UP SUBSTRATE FOR FCBGA

The advent of organic substrates changed the structure of flip chip packages to through-hole technology based on printed wiring boards in contrast to the stacked-via approach of ceramics. The invention of build-up technology introduced redistribution layers over cores. While the build-up layers employed fine line technology and blind vias, the cores essentially continued to use printed wiring board technology albeit with shrinking hole diameters.

As copper thickness shrinks in traces and plated through holes, these features become susceptible to thermal expansion in the z-direction. Hence, CTE in z-direction must be reduced to 20 ppm/degree for core materials (See Table AP10). The typical approach is to add filler to the resin system which typically degrades other material properties or introduces process disadvantages.

Table AP10: Package Substrates: Cost performance (CPU, GPU, Game Processor)

Adhesion of copper traces has been primarily by physical adhesion: rough, dendritic copper anchored in the resin. This anchoring treatment results in larger surface roughness, exacerbating conductor loss. The latest developments

are primers which are applied with the help of Cu foil and will provide chemical adhesion to the electroless Cu of pattern plated Cu. The primer provides a smooth surface and chemical adhesion thereby enabling much tighter trace pitches. Instead of primers, adhesion promoters based on porphyrene chemistry may be used to provide adhesion to electroless Cu or smooth Cu foil. Soldermask is emerging as another challenge for flip chip substrates. Planarity and thickness need to be controlled more tightly in the future. Dry film materials can achieve the requirements but cost is still too high for wide spread implementation.

HIGH PERFORMANCE—LOW K DIELECTRIC SUBSTRATE FOR FCBGA

High-speed transmission characteristics drive the demand for ever decreasing dielectric constant and low loss materials. Incremental materials improvements enable κ~3.4 today (See Table AP11). Materials are available with κ down to 2.8 but are still far too expensive for broad market application. There is no cost effective solution available for κ~2.5 and below. For such low κ, new reinforcement materials need to be developed. Thermoplastic resins with high heat resistance based on olefine systems seem feasible as well as new materials discussed in the Emerging Research Materials chapter of this Roadmap. These include the development of porous systems. Dielectric loss needs to be reduced by one order of magnitude. While PTFE and some cyanate resins achieve this, cost effective solutions are not yet available.

Table AP11: Package Substrates: High Performance (High End)

The next step in the evolution of substrates was to develop high density cores where via diameters were reduced to the scale of blind vias, i.e., 50 µm. The initial applications were based on PTFE dielectrics with metal alloy cores to manage package stresses. The full advantage of the dense core technology will be realized when lines and spaces are reduced to less than 25 µm. Thin photo resists (<15 µm) and high adhesion, low profile copper foils are essential to achieve such resolution.

In parallel, coreless substrate technologies are being developed. One of the more common approaches is to form vias in a sheet of dielectric material and fill the vias with metal paste to form the basic building block. A second building block is formed by laminating copper foil on both sides of the basic building block. Subsequent circuitization completes this second building block. By laminating the appropriate selection of building blocks, a raw substrate is formed which only needs external finishing. Variations of this process are to form the building blocks on carrier sheets as single layers of circuitry which are the transferred by lamination to the composite stack. In either case, the dielectric materials have little or no reinforcing material. Control of dimensional stability during processing will be essential. While different coreless technologies with proprietary designs and processes are emerging, significant market development is required to broaden the supply base, ensure stable quality and force cost reduction. Currently, coreless substrates are not in high volume production applications because these substrates have a tendency to warp during assembly. High volume assembly requires greater substrate stiffness with improved tolerance for warpage. The environmentally driven modifications to improve temperature robustness for lead-free assembly and to achieve halogen-free flame retardation are nearing completion for their first generation.

The primary advantages of Low Temperature Co-fired Ceramics (LTCC) over conventional Al2O3 ceramics for high performance applications are a significantly lowered dielectric constant, Dk, and conductor resistivity. In addition, the thermal coefficient expansion (TCE) of LTCC substrates more closely matches silicon than organic substrate materials. The combination of low dielectric constant, Dk, low dissipation factor, Df, high electrical conductivity, and matched Si/substrate TCE make LTCC an attractive material for high power, large die, high performance applications (See Table AP12). Future development challenges include establishment of finer pitch metallization printing and high-productivity laser vias to improve routing density. Laser vias also allow for lower-cost, quick-turn prototyping, compared to conventional mechanical via punching. The ball diameter will continue to decrease as the interconnect pitch reduces as shown in Figure AP11 below. This will cause additional challenges for production processes and reliability.

Table AP12: Package Substrates: High Performance (LTCC)

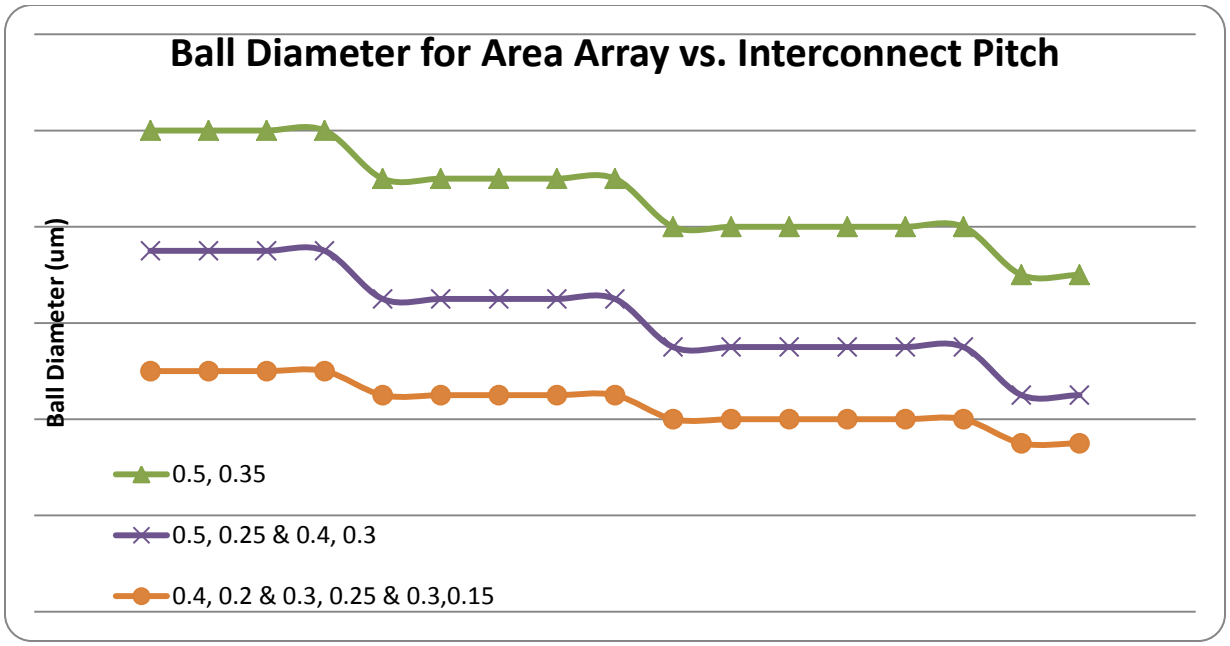


Figure AP11: Ball Diameter versus Pitch for Area Array Interconnect

4. WAFER LEVEL PACKAGING

Wafer level packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at the wafer level. The original WLP definition required that all package IO terminals be continuously located within the chip outline (fan-in design) producing a true chip size package. This definition described a Wafer Level Chip Scale Package, or WLCSP, with the processing of a complete silicon wafer. From a systems perspective, under this definition, the limitation on WLP was how many I/O could be placed under the chip and still have a board design that can be routed. WLP can provide a solution when requirements for a continued decrease in size, increase in IC operating frequency and demand for cost reduction are not met by traditional packaging e.g. wire bonding or flip chip bonding.

However, there are products coming to market that do not fall under this earlier definition of WLP. These new packages have been described as "Fan-out" WLP. They are processed by placing individual sawn die into a polymer matrix or silicon carrier that has the same form factor as the original silicon wafer. These "Reconstituted" artificial wafers are then processed through all of the same processes that are used for "real" silicon wafers, and finally sawn into separate packages. The die are spaced in the polymer matrix such that there is a perimeter of polymer surrounding each placed die. This are can be used during redistribution (RDL) to "fan out" the RDL to an area larger than the original die. This allows a standard WLP solder ball pitch to be used for die that are too small in area to allow this I/O pattern without "growing" the die to a larger size. With the implementation of this technology, it is no longer only intact silicon wafers that can be processed as a "WLP", but hybrid silicon/polymer matrices in wafer form that also can be now classified as WLP products.

WLP technology includes wafer level chip size packages (WLCSP), Fan-out wafer level packages, wafer capping and thin film capping on a MEMS, wafer level packages with Through Silicon Vias (TSVs), wafer level packages with Integrated Passive Devices (IPD), and wafer level substrates featuring fine traces and embedded integrated passives. There are wafer to wafer stacking technologies that will support stacked die WLP for future products to reduce cost. While many of these technologies are still in the developmental stage they represent solutions to cost, power level reduction, performance and size challenges for consumer products in the future.

Wafer Level CSP was the first generation of a wafer level package product to be introduced into the market place. Today WLP technology (fan-in WLP) with and without redistribution layers (RDL) are used for a large variety of products. WLPs with fan-in design today are typically for low I/O count and small die sizes, although the I/O count for today's products exceed 150. They are mainly being used in portable consumer markets where small size,

thickness, weight, and electrical performance are additional advantages to cost. Major trends include work for cost efficient rerouting with multi-layer RDL and improved design and simulation tools for WLP technologies.

With the introduction of TSVs, IPDs, Fan-out, and MEMs packaging technologies, WLP products can be used in a much broader range of applications, with higher I/O counts, and greater functional complexity. These packaging technologies open new opportunities for WLPs in the packaging field.

WLP now incorporates many different structures to meet specific application targets. A variety of WLP types are shown in Figure AP12 below. Table AP13 presents the technology requirements.

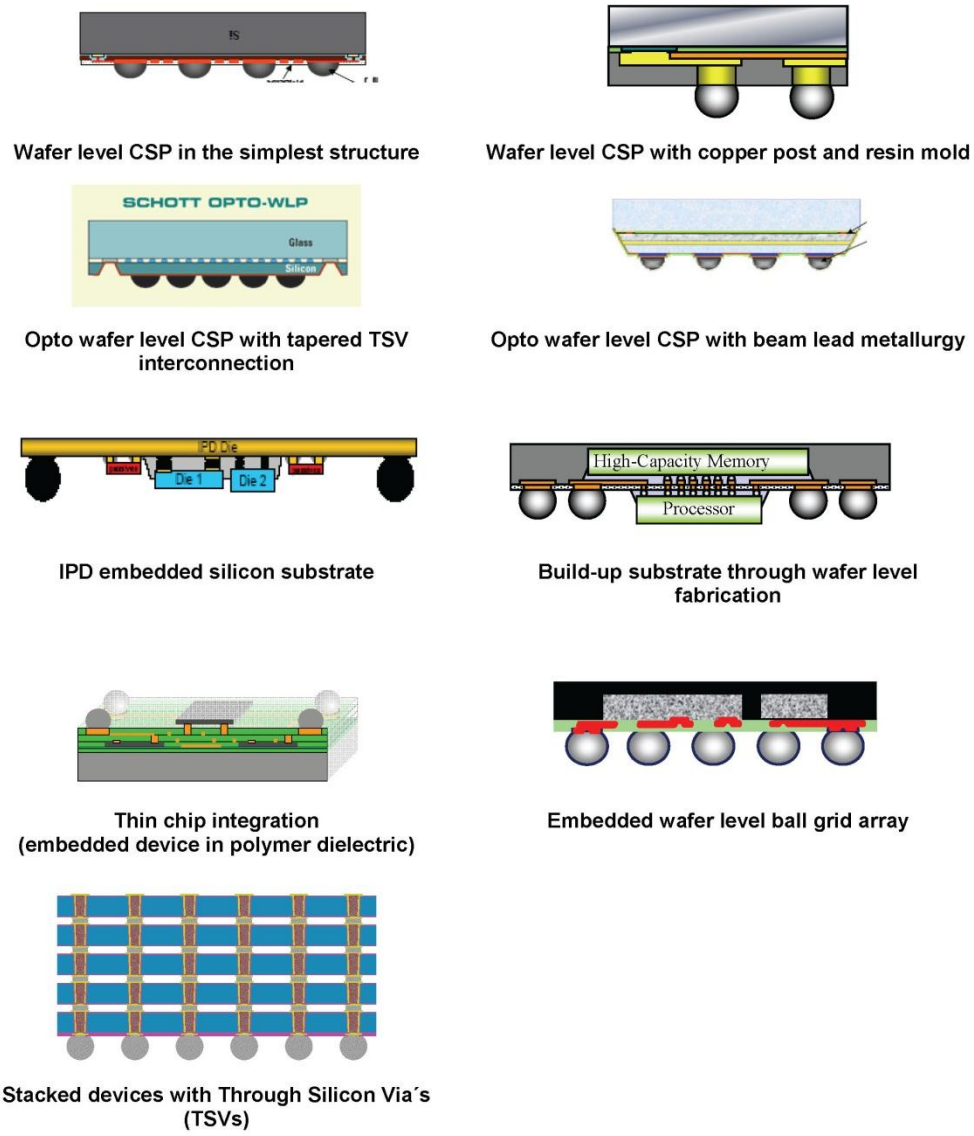


Figure AP12: Examples of Wafer Level Packaging Types

Table AP13: Wafer Level Packaging

The manufacturing process technology and high volume infrastructure enabling wide spread implementation of Wafer Level CSP in the market place have been based upon the adoption and implementation of established flip chip wafer bumping (under bump metallurgy, solder bumping, repassivation, redistribution, wafer inspection, wafer

probing) processes and equipment in the merchant market. The infrastructure has been developed to serve the high volume needs of flip chip packaging in the high performance and cost performance markets.

In contrast to flip chip assembly, WLP assembly typically does not require underfill. For solder joining, solder balls are typically used with a diameter larger than 250 µm. However, for specific applications where low package height is required, smaller solder balls can be used for lower stand-off heights. The smallest pitches used in the market are 0.4 mm and 0.3 mm is sampling. For standard WLP under-fill may be used to meet specific reliability requirements such as drop test.

The traditional drop ball WLCSP designs and processes are being further developed with modifications to the stress absorbing layers, underfill in board level assembly, and stress absorbing bump structures to allow for larger die applications. Thicker copper trace redistribution features have been introduced for higher reliability, higher power and lower signal loss applications. These trends will continue and WLP is adopted for larger and higher power die in the future.

The processes developed for copper redistribution layers are being introduced and extended to the fabrication of copper studs and passive components such as inductors, to be followed by capacitors and resistors (see section on passive devices). The combination of these components will lead to capabilities for the fabrication of filters and other sub-system circuit elements. Integration of these components into WLP-SiP packages constitutes a next step towards 3D wafer integration.

Memory devices are being used in portable consumer products such as cell phones and PDAs in increasing quantities. WLP offers advantages in these applications, due to inherent lower cost, improved electrical performance, and lower power requirements. Key enabling technologies to take full advantage of WLP for these applications will be the development of cost effective wafer level test and burn-in.

5. WAFER LEVEL PACKAGE DEVELOPMENTS AND TRENDS

Today, WLP developments are motivated by the recognition that wafer level processing technology, i.e., parallel processing on the wafer, opens additional alternatives to traditional packaging and assembly. WLP includes not only processing on active devices, but also processing of silicon dice with integrated passives, other substrates such as glass leading to wafer level substrates, and artificially reconstituted polymer wafers with embedded die.

For package substrates, fine design rules and the capability of creating integrated passive devices are attractive features. Dielectrics and traces are built on silicon substrate by wafer process technology and the following assembly is performed on the wafer level substrate. Some wafer level substrates are not made of silicon but dielectric layers and traces built up on a wafer, which will be removed during the manufacturing process.

Currently, different technologies at wafer level are in development to satisfy the need to increase performance and functionality while reducing size, power, and the cost of the system. This development leads to more complex packages for both single and multi-die Wafer Level Packages.

The wafer level CSP may incorporate copper post terminals with thicker resin coat providing a package that is more durable to the rough handling and more tolerant of CTE mismatch. This package is used for a variety of the applications from power amplifier to CPU with the ball pitches as fine as 0.20 mm.

The wafer level CSP specialized for image sensing is a glass-sealed optical wafer level CSP. Die are sandwiched or laminated on the circuit side by clear glass and terminals are routed to the reverse side of the die via TSVs or beam-lead metallurgy extending to the side of the die.

Low cure temperature polymers, with cure temperatures below 200 Celsius are being developed to allow the implementation of embedded flash into WLPs, insuring the integrity of the memory states during standard WLP processing. These lower cure polymers are also needed for fan-out packaging, as the mold compound used to reconstitute the wafers are typically epoxy based systems with relatively low Tg's. They also serve the special needs of WLP with TSV and IPD processing.

FUTURE TRENDS FOR WAFER LEVEL PACKAGING

Developments needed to meet the future requirements of wafer level packaging include:

- Continued reduction of processing temperatures, particularly for dielectric curing
- Wafer-level substrates with passives in silicon or passives in RDL
- Integrating passive structures into the RDL by thin film dielectric deposition
- Embedded active and passive devices
- Wafer-level assembly—die to wafer—of Si (memory, MPU), MEMS, III/V (InP, GaAs, GaN etc.) and SiGe devices at wafer level
- Integrated shielding (RF and power)
- Functional layers integration (actuators, sensors, antennas)
- Through-silicon-via (TSV) formation and metallization, wafer thinning and adjusted bonding technologies for stacked dies on wafer (see Interposer and 3D Integration sections)
- Optical chip to chip interconnects
- TSVs on WLP to allow double-sided connectivity, including Package on Package (POP) applications for WLPs
- Continued development of WLP for mechanical MEMS, in addition to the current optical MEMS applications

The development of wafer level packaging (WLP) is proceeding in several directions:

- Processes for larger die and higher functionality application based on RDLs (fan-in)
- Fan-out approaches (see various Embedded Wafer Level Package approaches)
- Higher complexity applications such as System in Package (SiP) with chip to wafer, 3D configurations and passive device integration. This includes face-down and face up approaches on active Si devices, carriers with passives, etc.
- New applications such as multiple IC stacks (memories, processor-ASIC-memories, MEMS); based on through silicon via (TSV) technology
- Wafer to wafer stacks
- These WLP technologies are driven by market demand for higher integration density and system capability (See SiP section)

DIFFICULT CHALLENGES FOR WLP

Wafer level Packages are expected to have better reliability even for larger die with small ball pitch. The physical structure and the materials used are being refined to satisfy the requirements of specific applications. This is a particular challenge for MEMS devices.

Key challenges include:

- Board level reliability especially for large die
- Testing of wafer level stacked packages and new 3D architectures with multiple die
- Vias through chip (WLP) and package (for embedded wafer level architectures)
- Thin package profile using very thin silicon die for extremely thin applications
- Mechanical tolerances required for chip alignment to small pads
- Contacts on small pads
- High reliability (electromigration, drop test)
- Topology of multilayer RDLs
- Combination of different materials—dielectrics, conductors—with mismatch in CTE, adherence, stress…
- Topology for thick metals for high current

- Reduction of metal roughness for RF (skin effect)
- Cross talk on chip because of small vertical distance
- Yield and defect repair possibilities for embedded WLP products

EXAMPLES FOR EMERGING WAFER LEVEL PACKAGE TECHNOLOGIES

WAFER LEVEL THROUGH SILICON VIA (TSV) FOR 3D INTEGRATION

The realization of vertical interconnected devices/chips using through silicon vias is one of the key emerging trends in wafer level packaging. This technology offers significant advantages in terms of electrical performances, e.g., signal transmission, interconnect density and reduced power consumption as well as form factor, heterogeneous integration, and manufacturing cost reduction. Today, new approaches are in development to incorporate TSVs into the Front End (FE)-CMOS process or as a post-CMOS process with VIA first or VIA last process (see Figure AP13). The key technical parameters for stacked die architectures using TSV are presented in Table AP14.

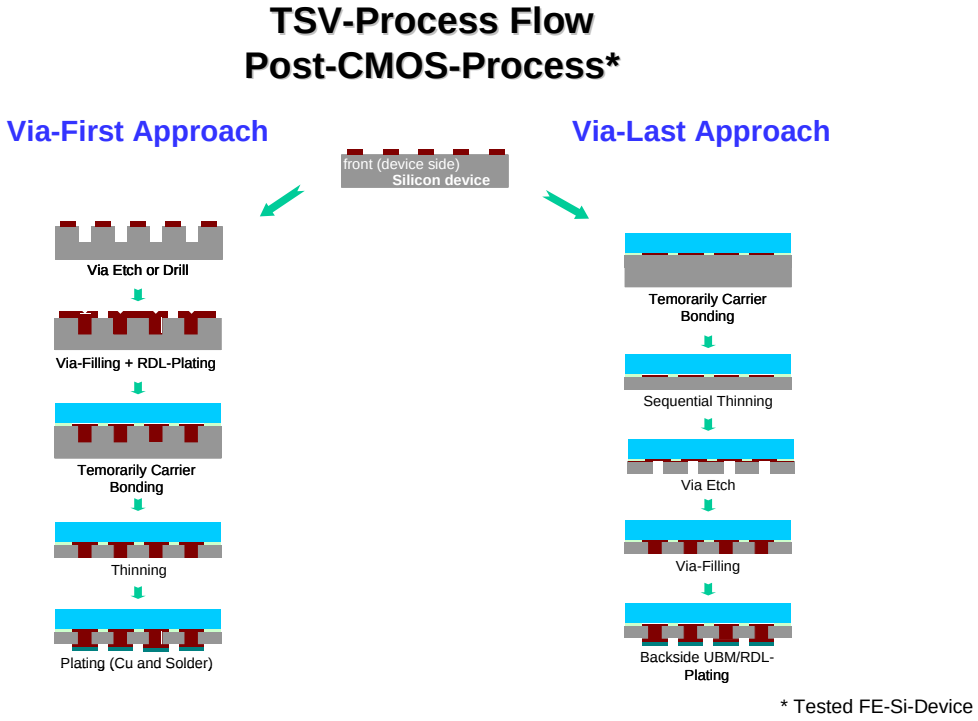


Figure AP13: Basic Process Flow Via-first versus Via Last

Table AP14: Key Technical Parameters for Stacking Architectures

The implementation of TSVs into the front-end processes will be covered by the Interconnect chapter of this Roadmap; here some aspects from the assembly and packaging view point will be discussed. The basic processes for the TSV formation are via etching (DRIE, laser), insulation, and metallization, which are well known from front-end processing. Additional processes which are required for the stack formation are wafer thinning, deposition of redistribution layer (RDL) and under-bump formation, wafer level bonding processes (die-to-wafer or wafer-to-wafer, e.g., micro bump soldering or Solid Liquid Interdiffusion (SOLID), as well as final encapsulation. Today the TSV process is demonstrated at the R&D level and only a few companies are running on the product level. The transition from R&D demonstrations to high-volume processes requires viable business models, the development of an equipment infrastructure, and the existence of viable costs for competitive applications.

Key technical challenges for the TSV approach are:

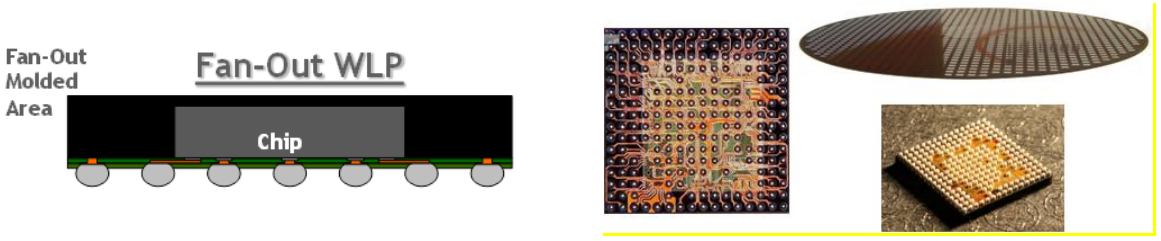
- High density and high aspect ratio via etching
- Low temperature processes for passivation and metallization

- High speed via filling (e.g., electroplating (Cu), CVD (Cu, W)
- Thinned wafer/device handling
- High speed and precise wafer level alignment and assembly processes (die-to-wafer and wafer-to-wafer)
- Testing and methodology
- Competitive cost

The first applications of TSV are used for CMOS image sensors and are in production today. Stacked die approaches for memory devices are in development and are projected to be in high volume production by the end 2012. Future applications for stacked die with TSV will include mixed architectures like analog, logic, processor, memory, and sensors.

FAN OUT WLP USING RECONFIGURED WAFER LEVEL TECHNOLOGIES

New package developments that have begun production and in consumer products are fan out or embedded wafer level package technologies. These technologies allow higher integration density and fan-out solutions using WLP technologies. For this new approach the chips are reconstituted and embedded in an epoxy compound to rebuild an artificial wafer. A thin film redistribution layer is applied (see Figure AP14) instead of a laminate substrate, which is typical for classical BGAs. Laminate substrates are reaching their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layers opens new opportunities for SiP. The possibility to integrate passives, like inductors, capacitors or even active devices into the mold compound or various thin film layers opens additional design possibilities for new SiP. There are other approaches that incorporate a copper pillar over ball integrated arrays. Special difficult challenges for these types of embedded wafer level packages are their implementation in the packaging industry infrastructure from design to manufacturing, and surface mount assembly to the board and board level reliability. These packaging technologies will require closer cooperation between the die design and packaging engineering groups to insure the manufacturability of the entire die/package structure. This will minimize the packaging cost and maximize the manufacturing yields.



(a) (b)

Graphic courtesy of ASE Graphic courtesy of Infineon

Figure AP14: Example of a Side-by-Side Solution of a Fan-Out WLP

6. SYSTEM LEVEL INTEGRATION IN PACKAGE

Predictions that Moore's Law has reached it limits have been heard for years and have proven to be premature. We are now nearing the basic physical limits to CMOS scaling and the continuation of the price elastic growth of the industry cannot continue based on Moore's law scaling alone. This will require "More than Moore" through the tighter integration of system level components at the package level. In the past scaling geometries enabled improved performance, less power, smaller size, and lower cost. Today scaling alone does not ensure improvement of all four items. The technical requirements for SiP are presented in Table AP15**.** The primary mechanism to deliver "More than Moore" will come from integration of multiple circuit types through SoC and SiP technology (see Figure 15). The most important as the electronics industry becomes ever more dominated by the consumer will be System in Package. This will allow the efficient use of three dimensions through innovation in packaging and interconnect technology. The result will support continued increase in functional density and decrease in cost per function as the industry begins to reach the limit of conventional CMOS scaling.

Table AP15: System in Package Requirements

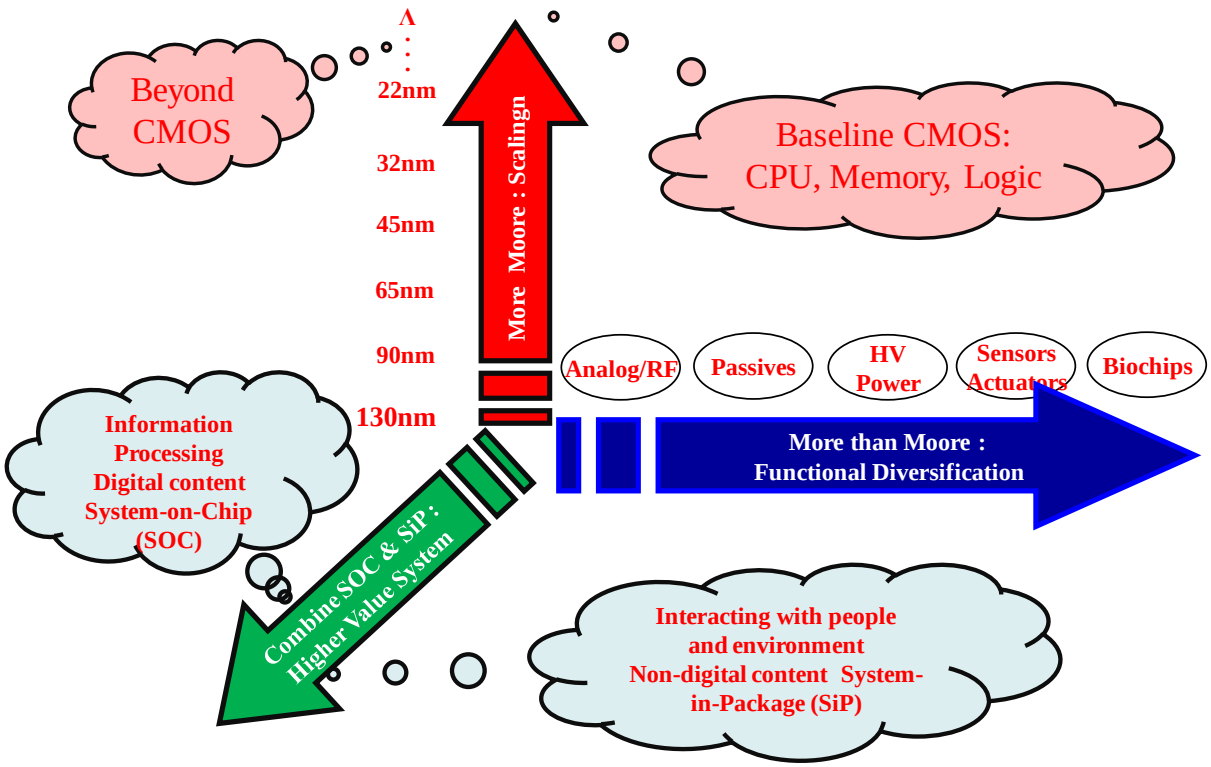


Figure AP15: Higher Value Added System by Combining More Moore and More than Moore

System in Package (SiP) technology is rapidly evolved from specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications. Numerous concepts for 3D SiP packaging are now emerging driven largely by the demands of portable consumer products.

DEFINITION OF SIP

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit, which provides multiple functions associated with a system or sub-system. AN SiP may optionally contain passives, MEMS, optical components, and other packages and devices.

There are many types of SiP packages. They are divided into horizontal placement, stacked structures, and embedded structures. Examples of the major categories are shown in Figure AP16 below.

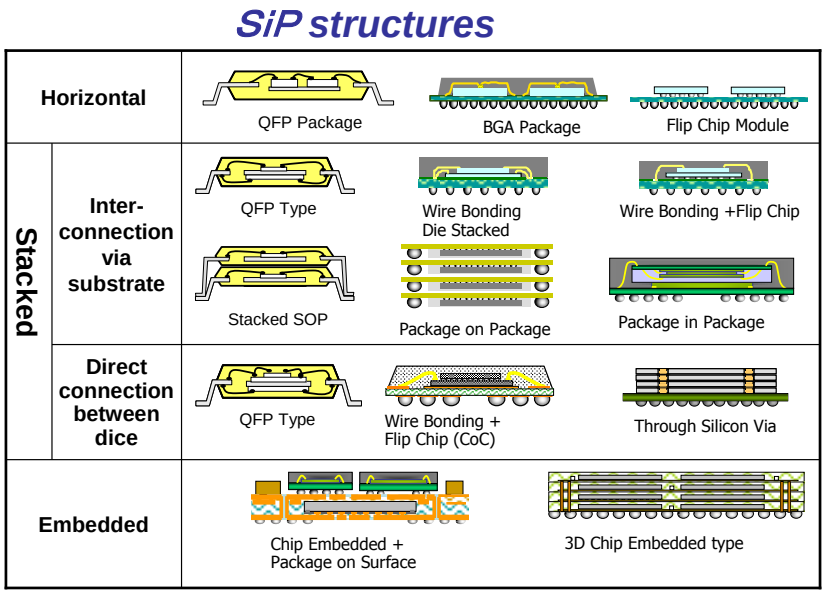


Figure AP16: Categories of SiP

SiP versus SoC

The benefits of "More than Moore" can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future. The pros and cons of each architecture are outlined in the Table AP16.

Table AP16: Comparison of SoC and SiP Architecture

SiP-Level System Design versus Board-Level System Design

Besides the comparison with SoC, SiP is often compared with monolithic packages for the selection of packages to a new product. SiP is sometimes considered more costly than the corresponding combination of monolithic packages. It is sometimes true when only the packaging costs are compared. But the total cost of the system building and the accompanying advantages must be taken into account. SiP offers customers benefits of smaller footprint of devices and fewer number of connecting traces between devices, which results in lower number of PCB layers. Also shorter signal paths in SiP reduce electromagnetic emission and cross talk. These features were demonstrated by an experiment with the system composed of microprocessor and DDR memories (See Figure 17). Board-level system design was made of monolithic packages and built on a PCB, while SiP-level system design was embedded in SiP. Comparing with the board-level system design, the SiP-level system design reduced footprint by 80%, electromagnetic emission by -20 dB/uV and number of PCB layers from 6 to 4 layers.

These benefits can often offer SiP-level system design lower total cost in addition to the higher quality of reduced noise and electromagnetic emission. Thus, optimum system solution often can only achieved by close collaboration and understanding between semiconductor/package/system suppliers.

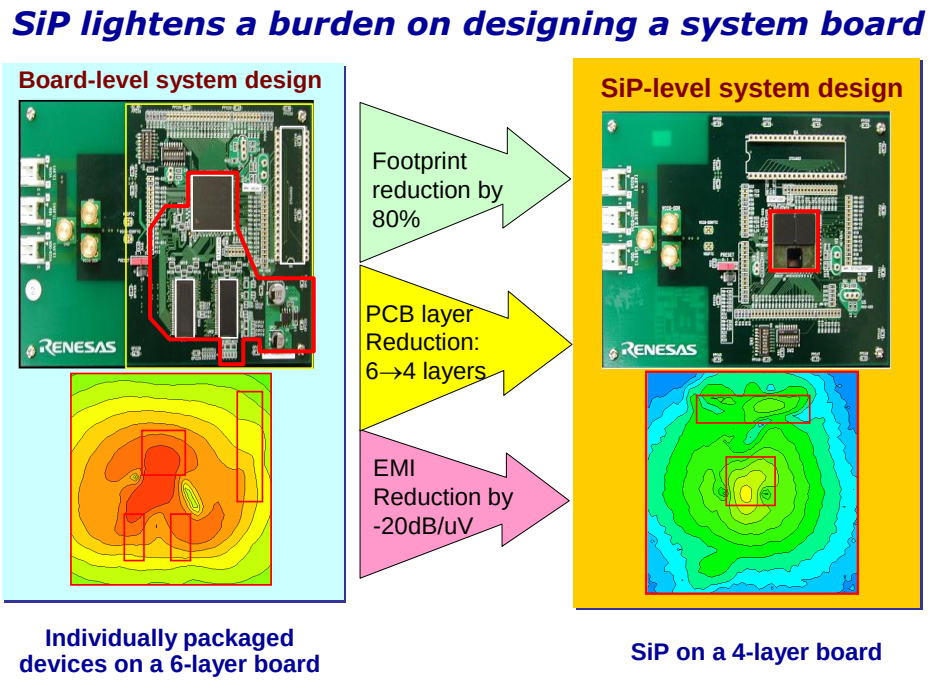


Figure AP17: SiP Design Improves Footprint, Reduces PCB Layers Reduction and Improves Performance

DIFFICULT CHALLENGES FOR SIP

System integration is aimed at higher performance, miniaturization, heterogeneous integration, and eventual cost reduction at the package level. For those purposes structures have diversified. Many critical technology challenges must be solved to achieve the ultimate performance goals and other benefits of SiP. The difficult challenges for SiP are presented in Table AP17.

Table AP17: Difficult Challenges for SiP

THERMAL MANAGEMENT

Today we encounter hot spots in integrated circuits which have circuit elements of different thermal density in the same IC. This presents a problem for package design but it has known solutions (see further in this chapter: Single chip packaging). The problem is becoming more difficult as the industry introduces new generations of microprocessors with many cores and incorporates core hopping to address local heating problems. This presents significant hot spot problems exacerbated by the fact that we now have no way to know where the hot spot will be located since it will move during operation. Finally we may have circuits included in a SiP with different maximum junction temperature. The challenges associated with these issues are discussed elsewhere in this chapter. The specific requirements to provide a cost effective mechanism to manage junction temperature while minimizing test time remains a major challenge for testing complex SiP devices.

THERMAL CHALLENGE OF HOT SPOTS IN SIP

The heat generation from an IC is highly non-uniform with areas of very high local heat fluxes at few locations on the die. Future trends show an increase in thermal design power and an increase in both average power density and local power density (also known as "hot spots"). Hot spot thermal management would limit the thermal solution of the component. Even when the total power of the component remains within design specification, the hot spot power density increase could limit the device performance and reliability.

For a SiP, thermal management must take account of the hot spot thermal dissipation within the die as well as within the package. Higher power dissipation with suboptimal placement of heat sources increases the risk of "hot spots" in 2D/3D integrated circuits. Also, difficulty in removing heat from the interspersed chips with a relatively poorly

conducting thermal interfaces in 3D die stacking (e.g. thermal impedance of C4 attach/underfill for flip-chip package, thermal resistance of chip attach material for low density wire-bond package) signify the cooling challenge of hot spots in SiP.

Cooling Solution Design Requirements for SiP

For the side-by-side configuration in SiP, the challenge over the single chip packaging with individual heat sink is the need to deal with the thermal cross-talks between devices as well as increased total power. For example, devices will heat each other inside a package, so that even the low power device can possibly get hot, if its neighboring devices dissipate excessive heat. The cooling solution design for SiP addresses all the devices in the package.

Different devices inside the same package may have different Tj_max specifications. For example, the typical Tj_max for microprocessor is about 100°C, while the typical Tj_max for memory device is about 85°C. The cooling solution design for SiP needs to accommodate different Tj_max specifications of all the devices.

For stacked die configuration and for embedded device configurations, the decreased volume and available exposed surface provide significant challenges. For low profile packages with 3D die stacking, various package and system level thermal solutions should be considered. The hot devices need to be located with due consideration for various primary heat flow paths as shown below in Figure 18.

Hot spot on top has a relative smaller heat resistance to top side; but in general the heat resistance chip-(chip-to-chip, etc.)-substrate-system (chassis) is in the range of one magnitude smaller than natural convection including heat path to the top). An opportunity to improve the heat path to the top with double side cooling and an applied heat sink on top will influence system design, system cost and potentially system reliability.

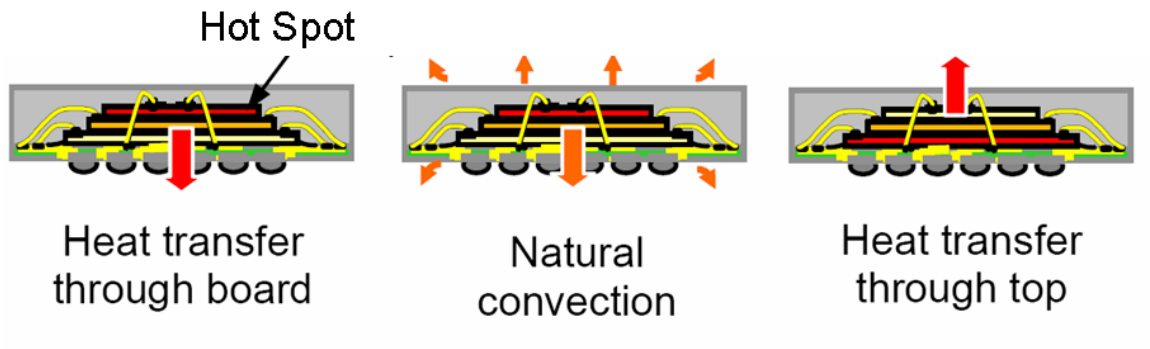


Figure AP18: Location of High Power Die versus Primary Heat Flow Path

The hot spot generally occurs farthest from the primary surface used for heat dissipation. The higher power devices need to place closest to the primary heat dissipating surface. Technology improvement to the primary heat flow paths needs to continue. For top side heat flow path, use of higher conductive molding compound, embedded heat spreaders and improved package to casing thermal interface material are potential thermal management options. For bottom side, i.e. board side, heat flow path, thermal performance enhancement options include use of thermally conductive under-fill between package and board, dummy solder balls between package and board, embedded heat spreader within the package substrate, and high conductive die attach between die and die to substrate. System level enhancement options include use of thermally conductive enclosure, venting grill, and active air moving device close to the device.

Thermal Challenges of Processor and Memory Die SiP

In packaging a multichip module with one high power process and several low power memory chips, the preferred technique has been to locate the module lid precisely above the processor chip, permitting use of a thin layer of thermal interface material (TIM). The inevitable variations in chip heights and planarity of memory chips are accommodated by use of gap-pad (conductive elastomeric) TIM which results in significantly higher thermal resistance than that of the processor. Since the processor power density is typically several times that of the memory dice, resulting junction temperatures of all chips are similar.

For 3D stacked die configuration with TSV interconnects, the processor die is preferred to be placed at the bottom in 3D die stacking to make it closer to the substrate due to IO signal performance and power delivery efficiency, but cooling performance from the high power process will be the bottleneck. If the processor die is placed on the top, TSV requirements in both counts and size would cause significant mechanical concerns (e.g., crack, stress) for the memory dice at the bottom.

THERMAL MANAGEMENT OF 3D TECHNOLOGY WITH TSV INTERCONNECT

3D technology with TSV interconnect can be used to enhance communication between ICs (larger bandwidth, lower latency, and lower energy per bit) [1–4] but it also presents some challenges. Aside from issues relating to manufacturing, power delivery [5] and cooling [6–9] of a stack of logic chips becomes more complex as compared to the single chip case. Challenges in power delivery include issues that relate to reducing power supply noise and losses in the power delivery network (as well as issues relating to electromigration). The continued reduction in supply voltage (although slower in the future) and timing margins causes the tolerated peak noise in high performance circuit to also decrease. This problem becomes worse as current consumption of microprocessors increase and circuits switch faster. Furthermore, power delivery becomes even more exacerbated when logic chips are stacked as the total current that needs to be delivered to the stack increases. Solutions to the power delivery problem will involve, among other things, co-design and optimization of both on-chip (for example, on-chip decoupling capacitors) and off-chip resources for power delivery including the number of power/ground pads and through-silicon vias. Trade-offs and analysis of the interaction of these is important to the understanding how to best minimize power supply noise in 3D stack.

Cooling represents another challenge for 3D logic ICs. Historically, in order to maintain constant junction temperature with increasing power dissipation, the size of the heat sink used to cool a microprocessor has been increasing (along with improved heat spreaders and thermal interface material (TIM)), and thus imposing limits on system size, chip packing efficiency, and interconnect length between chips. The cooling of hot-spots (power density up to 500 W/cm2) greatly exacerbates the complexity of cooling and it is becoming increasing challenging to meet thermal performance needs of chips. Challenges in cooling become magnified in 3D chips because it requires: 1) "paving" a path for heat flow from within the stack to the periphery of the stack (i.e., the thermal resistance to the ambient for chips within the stack increases compared to a single chip), and 2) methods of removing the increased power density to the ambient once the heat is "routed" to the periphery of the stack (usually the top of the stack). The low thermal conductivity of the on-chip interlayer interconnect dielectric increases the challenges to the former. Many researchers have proposed the use of "thermal TSVs" to enable "routing" of the heat to the top of the stack where it can be extracted to the ambient. However, such an approach may require a prohibitively large number of vias (especially with stack count increase). Another approach that is being explored by a number of researchers it the use of inter-layer microfluidic liquid cooling using micro-channels or micro pin fin array [3, 8, 9] as illustrated in the figure below (see Figure 19).

In order to achieve high heat transfer, low thermal resistance, and low pressure drop, a relatively tall micro-channel heat sink is typically needed (~250 μm, for example). As a result, this necessitates a "thick" silicon wafer and is different from other 3D integration technologies, which seek to polish the silicon wafer to as small a thickness as possible before wafer handling and mechanical strength become limiters [3, 8]. As a result, this presents interesting set of constraints on the fabrication and integration of E-TSVs, which had been demonstrated recently. Ultimately, the number of electrical TSVs that can be placed will impact the connectivity between tiers in a stack, including power delivery.

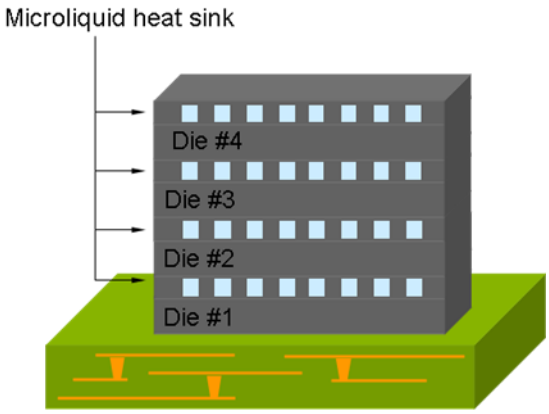


Figure AP19: Interposer Based Microliquid Heat Sink for Stacked Die

POWER DELIVERY/POWER INTEGRITY

The power level of high end microprocessors places very stringent requirements on power integrity as the power density increases and the operating voltage decreases. The power integrity and product cost requirements cannot be met for high performance devices without chip/package/system co-design. (See section on The Need for Co-Design Tools below) The voltage level for 45 nm and 28 nm chips are in the sub one volt range resulting in reduced noise margin. Even with low resistive losses, the higher current transients due to multiple cores on the chip requires lower interconnect inductance and more decoupling capacitance on the substrate. The capacitor path requires multiple thin dielectric layers to meet the target impedance of the power delivery system. For multi-chip packages, placement of the various chips and decoupling capacitors is crucial and requires system level simulations. New materials will also be needed with higher dielectric constant and lower leakage currents to deliver the high capacitance density required ensuring power integrity at low cost.

Power delivery for multi-chip packages is also getting complicated due to multiple power supplies for different types of circuits such as core, memory, back-biasing, etc. Due to the test and system requirements, noise margins for the various power supplies are also different. Managing multiple power supplies requires more layers in the package which may restrict the use of some package technologies.

TESTING OF SIP

The complexity of SiP based products continues to increase and, with that, test becomes a more difficult problem. The challenges are many and they include:

- test access
- contacting for testing thinned wafers and/or thinned die
- thermal management during test
- testing mechanical and thermal characteristics in addition to electrical test

TEST ACCESS

If we assume that we begin the assembly and packaging process with known good die (KGD) the test problem is limited to confirming the assembly process and testing the performance of the on-package interconnect. If SiP is to meet its potential the off-chip drivers will be similar to the core transistors and only the off-package drivers will require more power. The SiP will not deliver all the test points to package pins for these more complex packages. There are several potential solutions including the incorporation of a “BIST” chip on-package that can have access to device pins that are not delivered to package pins. In some cases the more cost effective solution may be to test the SiP functionally without retesting the KGD post assembly if yields are high.

CONTACTS

The continued reduction in geometries is approaching a terminal density that cannot be met with even the leading edge of conventional MEMS contactors. Several solutions are being evaluated including capacitive coupling which

will suffice for digital signals but cannot provide power delivery or appropriate contact for analog signals. RF contactors have also been proposed and may offer a solution for some contact challenges. None of these proposed solutions has been proven to meet the requirements.

The test contactor required to deliver KGD for thinned wafers/die may be an even more difficult problem. The competition between ensuring power integrity when contacting these thinned die and damage to the die associated with the contactor force and potential pad damage.

These challenges and others may prevent the industry from delivering KGD for thinned wafers as we approach devices with a billion transistors and more. The concept of "probably good die" with redundancy in the SiP is being explored as a potential approach for ensuring the quality of complex SiP products.

MECHANICAL AND THERMAL TESTING

The thermal cycles and specific use cases for many consumer products impose mechanical stresses that require test to ensure reliability of the products. The "drop test" approaches that have been used for cell phones and some other consumer products need to be replaced by new approaches that test a wider range of stresses including those associated with the thermal cycles experienced in the use cases. In addition we need tests that fit in a production flow without excessive test time or test cost. This remains a challenge not yet met.

COST OF TEST

These test challenges must be met with low cost. Most SiP are today are used in consumer electronics. These markets are very price sensitive and any SiP for the consumer market with excessive test cost will not be successful. The major elements of conventional test cost are applications programming, test time, cost of ATE equipment, and cost of probe cards. Complex SiPs may require both conventional test and BIST testing to accomplish adequate testing. This is due to test access limitations in high component density, the very high speed of RF and digital communications circuits, and the requirement to test system level characteristics.

We have introduced some of the details for test challenges that are specifically relevant to assembly and packaging. The Test Chapter of the ITRS should be reviewed for a more complete description of test challenges.

SiP FOR TERA-SCALE COMPUTING

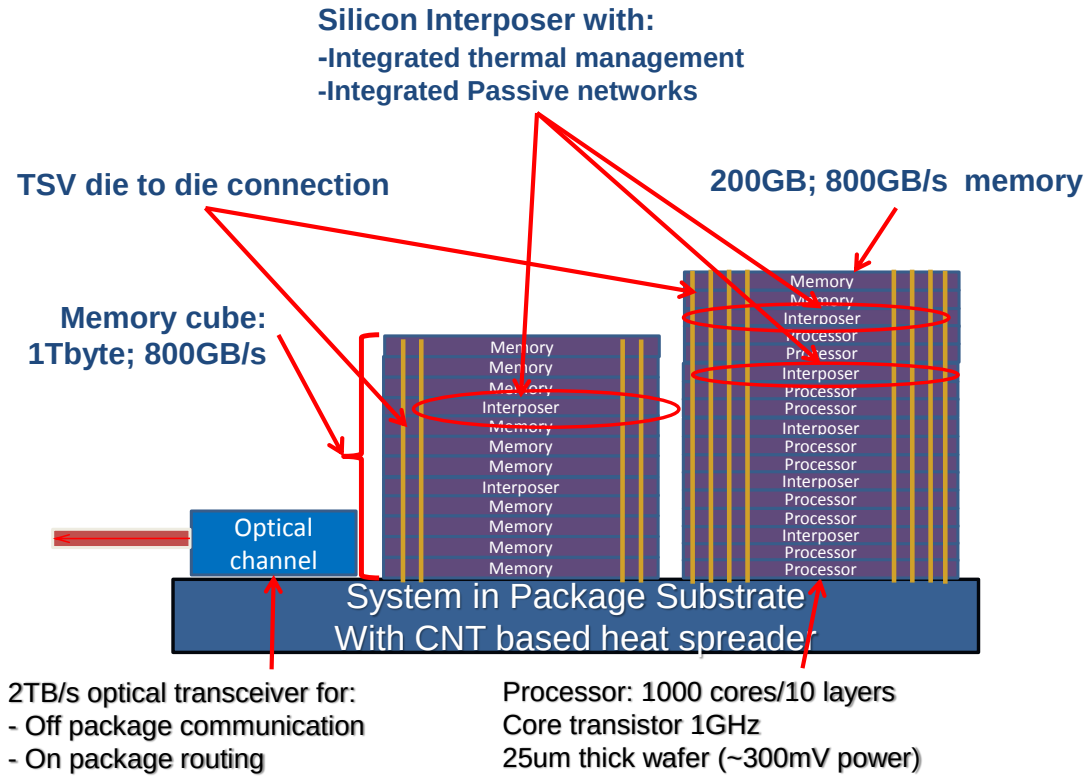


Figure AP20: Current Vision for Packaging of 3D-SiP

The major challenges for digital systems today are power requirement and integrity, thermal management and the limitations in physical density of bandwidth. These challenges become more difficult in 3D-TSV SiP architectures. In this section we will only address the packaging issues related to these challenges. Other work to reduce power requirements such as new transistor materials and architectures to reduce leakage currents are addressed in other chapters of the Roadmap.

The total power requirement can be reduced by dropping the operating voltage, reducing the interconnect distance, reducing the capacitance and reducing the operating frequency. Each of these approaches is incorporated into the vision presented in Figure 20.

- Stacking the circuits in layers will reduce the interconnect length by approximately the square root of the number of layers. Today a majority of the power is associated with the interconnect so 4 layers may approach a reduction in power requirement by a factor of 2. (this depends on the % of power in the metal 1 and metal 2 layers which is more than that of the global interconnect)
- The frequency capability of the logic transistors exceed the frequency used so a reduction in operating voltage can be realized without compromise in performance. The power consumption is proportional to the square of the voltage so a reduction to half can reduce power requirement by four. This is very effective if the power integrity can ensure keeping the transistors above the voltage threshold.
- Reducing the frequency results in major reductions in power. Stacking the die enables a much larger number of cores and, to first order, an increase by an order of magnitude in the number of cores can deliver similar computing power when the frequency is reduced by an order of magnitude.
- Reducing the capacitance will require new material for interlayer dielectric. Today the state of the art is k_{eff} of about 2.6. Material currently in qualification can drop this number to below 2.0. This provides both a performance improvement and reduction of power required.

Power integrity is much more difficult when the voltage is near the low voltage threshold and the potential exists for billions of transistors to switch essentially simultaneously. When these transistors are stacked the inductance in the wiring between the power source and the transistors must be decoupled as close as possible to the transistors. The incorporation of interposers in the stack with very large capacitors can accomplish this task. This will also require new materials since the dielectric constant of approximately 4.0 used for on chip/on package capacitors today is too low to provide the required capacitance. New materials in qualification may increase this number to 100 or greater.

The thermal density is increased and the surface area to exhaust the heat is reduced with 3D integration. The steps defined above to reduce power requirements will help but the stacked die architectures for logic devices will require heat removal from inside the stack. In the vision of Figure 19 this is provided by microfluidics incorporated into the interposers inside the stack.

As the density and performance of the logic circuits are increased and the physical area available to address the resulting increase in demand for bandwidth is reduced new approaches are necessary. There have been proposals to bring photonic data transmission to the IC. These proposals may address the bandwidth but the wavelength employed for photonic data transmission is many times larger than the transistors. In addition, using an indirect band gap material requires more energy than a direct band gap material for converting data from electrical to optical and back. The solution is to bring photonics to a direct bandgap semiconductor circuit in an SiP package and convert to a very wide electrical bus on the package.

The implementation of all elements of the vision in Figure 20 will enable a tera-scale computing in a package the size of a modern smart phone. Until the energy requirement is further reduced there will still need to be additional space for dispersing the heat that is removed from the stack.

DIVERSIFICATION AND MANAGEMENT OF COMPLEXITY

In today's SiP many new processes and materials are introduced. Examples are redistribution layers, which push development of new dielectrics. RDL are on WLP and eWLP. Mold compound are investigated and new developments e.g. towards specialist functions and requirements take place. We need to select package type related to applications. Different reliability constraints from applications require different package solutions. All these examples demonstrate the diversification we have. The management of the complexity of all the different materials and processes to make the right choice is an extreme challenge. Target is reliable supply chain.

THE NEED FOR COHERENT CHIP-PACKAGE-SYSTEM CODESIGN

Chip-package-system co-design methodology is a vital enabler for integrating SoCs, other die, MEMS devices and passive components efficiently into System-in-Package. Chip-package-board design collaboration is essential to reduce cycle time and cost and to optimize performance for stacked die, PoP, PiP, and 3D packaging in general. A more detailed overview is available in the paper titled "The Next Step in Assembly and Packaging: Systems Level Integration."

Failure to identify and meet essential system-level requirements and to apply lessons-learned, will result in lower-than-expected performance. Understanding design trade-offs and the performing critical system-level analysis is essential to produce designs that can meet the desired cost and performance targets. Incomplete feasibility studies and failure to capture some key interaction at the system level can result in extra iterations before the package design is finalized. It is important to identify essential system-level requirements and to apply lessons-learned for good optimal design. Without the benefit of co-design and simulation, there is risk that a device will be late to market with an expensive, overly conservative package.

Some key challenges in 3D packaging are design for manufacturability, design for low cost, reducing design time, design for reliability, complex wire bond and/or flip chip rules checking, chip design flexibility trade-offs. Also critical is interface/alignment with tools and flows such as those provided by EDA design software tools, IDM specific design flow and tools, and alignment with substrate suppliers and assembly sites. Implementing co-design methodology requires iterative design reviews; collaboration between chip, package and system design; application development; electrical, thermal, and mechanical modeling; simulation, and high-density substrate design teams. A suggested design flow is shown in Figure 21 below.

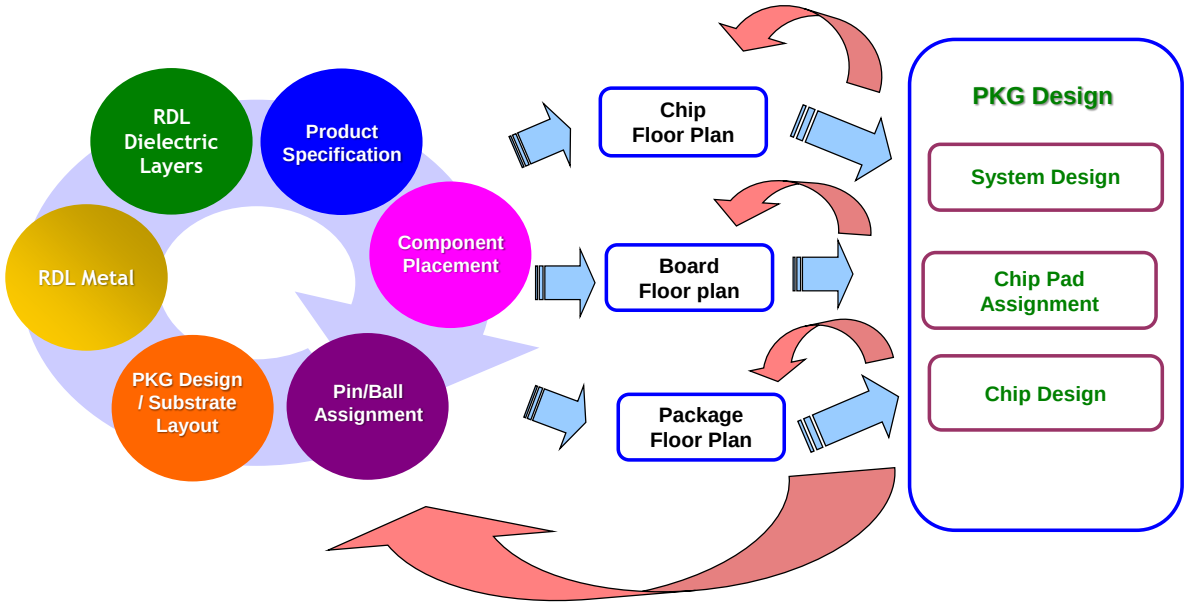


Figure AP21: Chip-Package-System Co-Design Flow

Below a design methodology that has been worked out by the EU CATRENE project CoSiP is presented. A backbone based on XML for data transfer has been introduced as shown in Figure AP22 below.

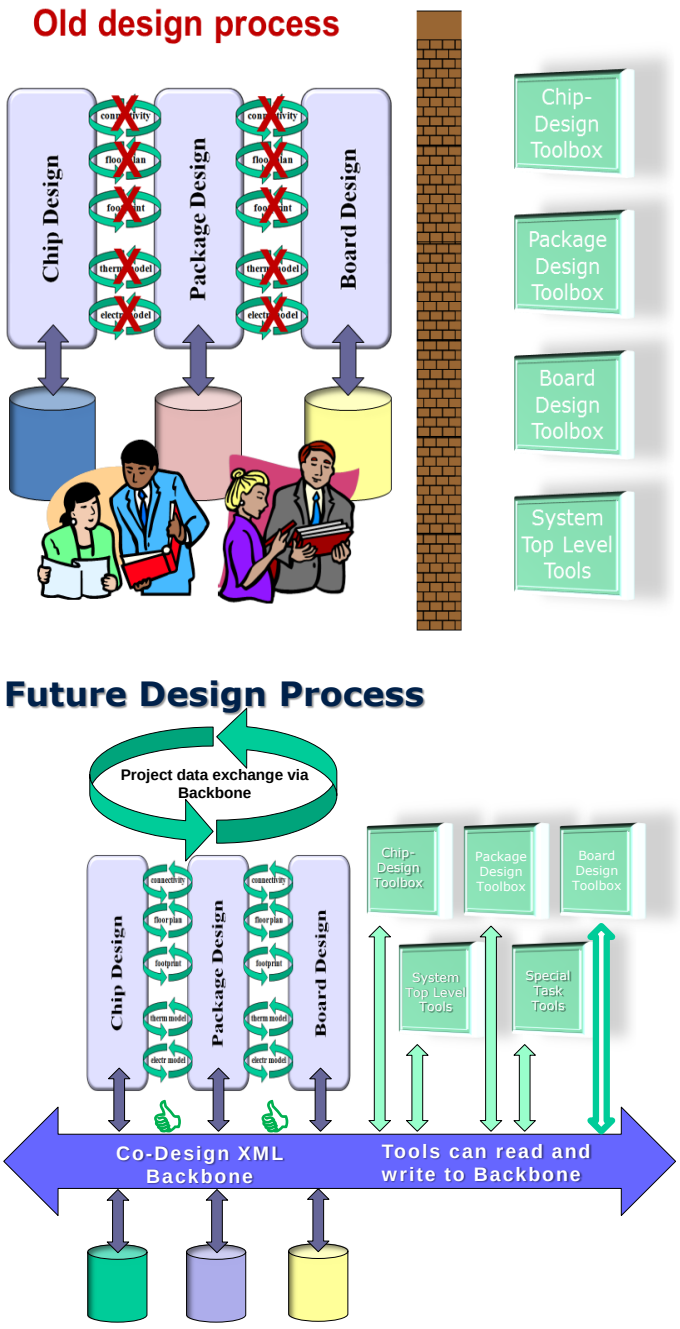


Figure AP22: Past and Future Design Process for 3D SiP

In the past chip, package, and board designers worked independently (top figure). Chip-Package-System co-design methodology is required that allows data exchange. A solution is the introduction of a backbone based on XML.

COLLABORATION, COST AND TIME TO MARKET

Expert users of each tool environment chip/package/system must collaborate to optimize the design. Thus, for the future, appropriate user interfaces are required. Co-design can improve performance while reducing costs and cycle time dramatically—often by 2X. Without the benefit of extraordinary collaboration within the design team, the package is almost impossible to optimize at the system level. The cost trade-offs are not clear, system level performance impacts are uncertain, and changes are cumbersome to implement. To avoid this, designers often use overly conservative design margins and assumptions that lead to higher package costs. Without co-design analysis

tools that function across design environments, "what-if" analyses are difficult and time-consuming, leading to longer design cycle times.

IMPORTANCE OF RELIABILITY FOR SiP

Effective co-design should comprehend the interaction between functional, physical, thermal, mechanical, electrical design, and reliability. Many of the trade-offs between design areas and reliability that are evident in conventional packaging become more complex for SiP configurations. Thus, it is not good practice, especially in SiPs, to run the electrical, mechanical, thermal and reliability design portions separately. Because of the complexity of sub-component interactions, there is not a universal or specific list of parameters to design for reliability. In general, one needs to examine the sub-component interactions, design goals, trade-offs, design rules, specifications, and existing design for reliability practices in order to select the appropriate design for reliability guidelines.

NEED FOR A SYSTEMATIC APPROACH

Package design requirements and changes originate from many different functional areas and usually end up being applied in stages. A potential solution would be for the chip-package co-design to borrow methods and tools from modern systems design. This approach can head off constant iteration and other challenges. One way to reduce iterations is to use "look-ahead" test and modeling vehicles (virtual prototyping) to support system-level reliability and manufacturability testing, as well as system-level electrical and thermal modeling. Look-ahead vehicles come in two forms: an actual mechanical vehicle for reliability and manufacturability testing, and a paper design vehicle for feasibility, thermal and electrical modeling analysis. These vehicles require a certain discipline and commitment. This approach could help to answer many general design questions early in the process, and at a fraction of the cost of using production test vehicles.

NEED FOR CO-DESIGN TOOL DEVELOPMENT

SoC and SiP package design requires 3D capable thermal, electrical, and mechanical modeling tools that allow integration and analysis of chip, package and system level requirements, and interactions. We also need electronic design automation (EDA) tools for powerful chip-package-system design and routing capability, built-in checks, standards and reporting features like design rule checks (DRC), standard net list syntax, and connectivity reports.

Custom automation tools can provide fast and efficient communication and verification of design data between different design environments. Spreadsheets are a common platform for these automation tools since they are available in almost all design environments and readily scale to handle large volumes of data. These tools have three primary uses: 1) convert data to pictures, 2) convert data to standard formats, and 3) compare the standard format datasets. This type of automation is essential on typical SoC designs to reduce the time spent manipulating relatively large datasets, and to reduce possible manual errors in handling large amounts of raw data.

The development of chip-package-system co-design methods and tools is an ongoing process. A comprehensive, user-friendly, and tightly integrated tool(s) that can seamlessly span all the different design environments is not yet available. Nevertheless, existing chip-package co-design tools, with the right methodology and custom-developed internal tools can provide useful benefits including reduced package costs, and design and verification cycle time.

GENERIC CHIP-PACKAGE-SYSTEM CO-DESIGN TOOL DEVELOPMENT REQUIREMENTS

- Improve design cycle time, accuracy and design-for-manufacturability
- Align with critical tools, import/export data formats, flows and rules such as: IDM's internal tools die design tools, suppliers, assembly sites, electrical constraints and modeling tools
- Reduce iterations, less manual/more automated checking, capture complex design rules and enable more chip-package-system trade-off capabilities
- Forward-looking: better methods, more complexity, collaboration, and technology combinations
- Easier verification: Substrate, substrate plus die, manufacturability, electrical, functional, thermal, and mechanical verification. Import/export to IDMs internal tools
- Easier and more rapid feasibility analysis
- Collaboration with die and system design teams. Unified data formats, chip plus package plus system verification tools, etc.
- Comprehend the interaction and I/O planning of multiple functions within a single package (also passives)

- Great complexity—amount of design data, multiple layers, elaborate patterns, multiple net lists
- Complicated electrical constraints (long traces/wires, crossing traces/wires…). Enhanced constrain management
- Allow minor tweaks in IC or package design without leading to significant cycle time hit
- Need faster design iterations in early phase to avoid more costly design iterations in the later phase
- Capture complex mechanical, wire bond and flip chip bond assembly-rule constraints driven by smaller and thinner packages
- Better design for manufacturability and cost analysis. More and easier to use manufacturability constraints
- Real-time chip-package-system design trade-offs
- Interface and alignment with internal tools and flows
- Shortening design cycle of complex designs
- Cost-weighting of constraints
- More flexibility to handle frequent design changes
- Flexibility of design flow, user-defined design starting point from chip or from system
- Tighter integration with chip, system and manufacturability design teams
- System-level electrical modeling, including high-speed applications
- Complexity drives verification tools that work across different design environments
- Tight collaboration with suppliers, support, development, production, and customers to enable better methods and tools for complex package co-design
- More powerful user-friendly scripting capabilities
- Common, technology independent database to enable reuse

CO-SIMULATION OF RF, ANALOG/MIXED SIGNAL, DSP, EM, AND DIGITAL

SiPs that combine RF, analog/mixed signal, DSP, EM, and digital bring not only design and manufacturing challenges but also simulation challenges. Usually different functions of an IC require a different simulation technology. For instance, frequency domain simulations such as Harmonic Balance are adequate simulation technologies for RF circuit designs; whereas time domain simulations are typically used to predict nonlinearity and VHDL or C based system simulation for digital applications. It is important to understand the system's behavior with packages and interconnect parasitics. Simulation and Modeling of Embedded Passives and Integrated Passive Devices in SiP applications need to be considered. Embedded passives are used to replace traditional surface mount parts.

7. 3D INTEGRATION

SCOPE

We are rapidly approaching the limits of Moore's Law scaling and the effort to continue the pace of progress has been focused on two technical directions. Functional diversification which is referred to as "more than Moore" is one direction and for packaging it is the driving force behind system in a package (SiP). The second is the use of the third dimension and wafer thinning technologies to increase the functional density for a given node. This section addresses the requirements, difficult challenges and potential solutions to continue the pace of progress in performance, functional density and cost through use of the third dimension. There are several driving forces for 3D integration. The potential benefits include higher performance, reduced power requirement, smaller size and eventually lower cost than conventional 2D packaging. Some of the basic driving forces for 3D integration are presented Figure AP23 below.

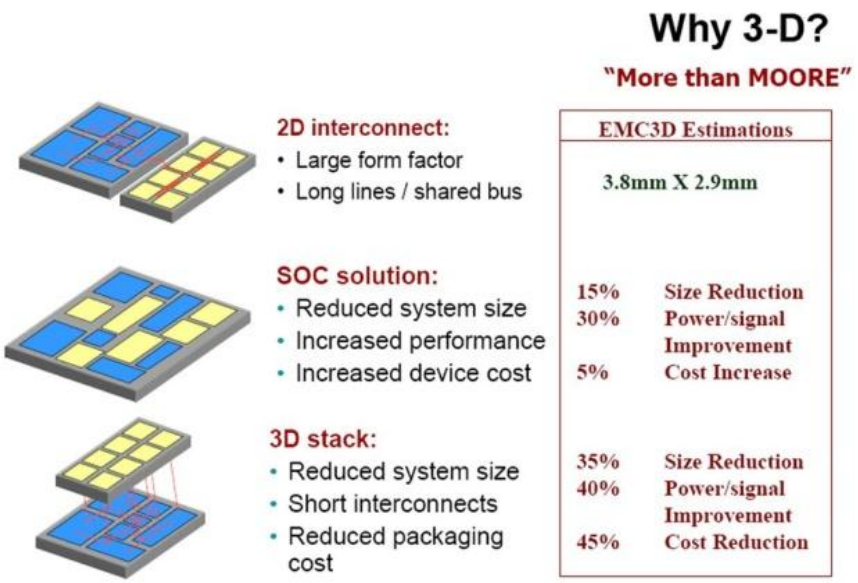


Figure AP23: Driving Forces for 3D Integration

There have been several 3D integration techniques and associated challenges presented in the Wafer Level Packaging and System-in-a-Package sections above. The issues specifically related to TSV are presented in Tables AP13, AP14 and AP18 with TSV related materials issues in Table AP19. There is a separate section below that addresses the thinning processes required for 3D integration. Many difficult challenges remain related to cost, reliability, alignment accuracy for D2D, D2W and W2W, and bonding techniques but rapid progress is being made by industry Consortia such as EMC-3D and others and volume production of TSV based product has already commenced.

Table AP18: Key Technical Parameters for Interposers

Table AP19: Materials Challenges

DIFFICULT CHALLENGES

Many examples exist for 3D integration as illustrated in Figure 24 below. Most, however, have not yet achieved product status due to difficult challenges that are not yet resolved. The primary result is cost of these products compared to alternatives using conventional 2D packaging. Many of these technologies have not yet come down the learning curve. As production volume increases cost will decrease such that 3D packaging will become the standard for portable consumer products.

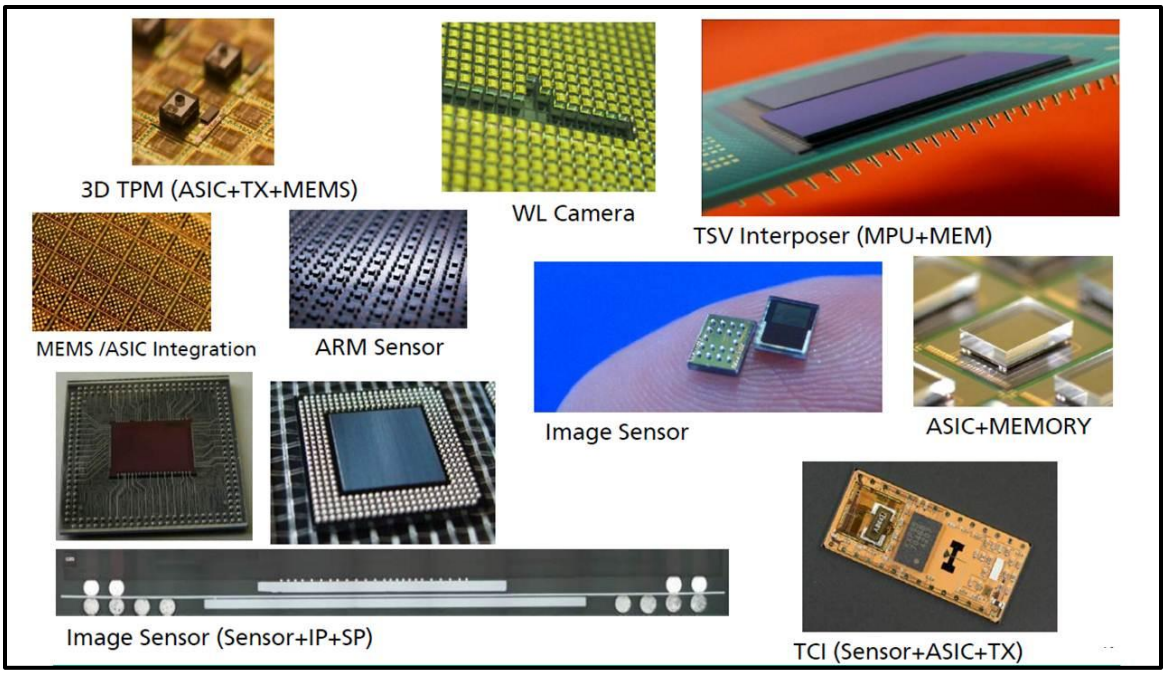


Figure AP24: Examples of 3D SiP Integration

Source: Fraunhofer IZM

There are many difficult challenges for 3D integration. Test access, thermal management, power delivery and power integrity, among other things, will require significant innovation to meet the Roadmap requirements. The difficult challenges and potential solutions are listed in Table AP20. Some of these issues are discussed in more detail in the text of this section.

Table AP20: Difficult Challenges and Potential Solutions for 3D Integration

TECHNOLOGY REQUIREMENTS

The major new packaging technologies for 3D integration are:

- TSV formation for via middle and via last
- Wafer thinning
- Handling of thinned wafers and thinned die
- Bonding and interconnect (at low temperature)
- Package substrates with high wiring density
- Formation of package enclosures (particularly for MEMS and Photonics elements)

There are solutions or potential solutions for all of these technology requirements and many are already in production use. In most areas there are competing technologies and the development continues for higher yield, lower cost solutions.

INTERPOSERS

The introduction of interposers for advanced packaging, first introduced as a product by Xilinx, is now in use for 2.5D integration. The benefits of higher bandwidth, lower power and reduced latency are compelling and several other products are in development using this technology. The full benefits of 3D are even more compelling. They include enabling heterogeneous integration, reduced size, increased performance, lower power requirement and reduced latency. The key technical parameters for interposers are in Table AP18. The table addresses both base silicon interposers used for 2.5D architectures and intermediate silicon interposers used for use in a 3D stack. While

silicon is the material of choice today, work is underway to use glass, ceramics or polymers for interposer material. Each approach has some potential advantages but for now we have addressed only silicon and glass.

2.5D ISSUES

The introduction of product with using 2.5D interposers used a TSV interposer to connect multiple chips side by side and provide high bandwidth connections between the die, RDL to map the die geometries to the printed circuit board geometries and TSVs to connect the top and bottoms layers of the interposer. This is illustrated in Figure 25 below.

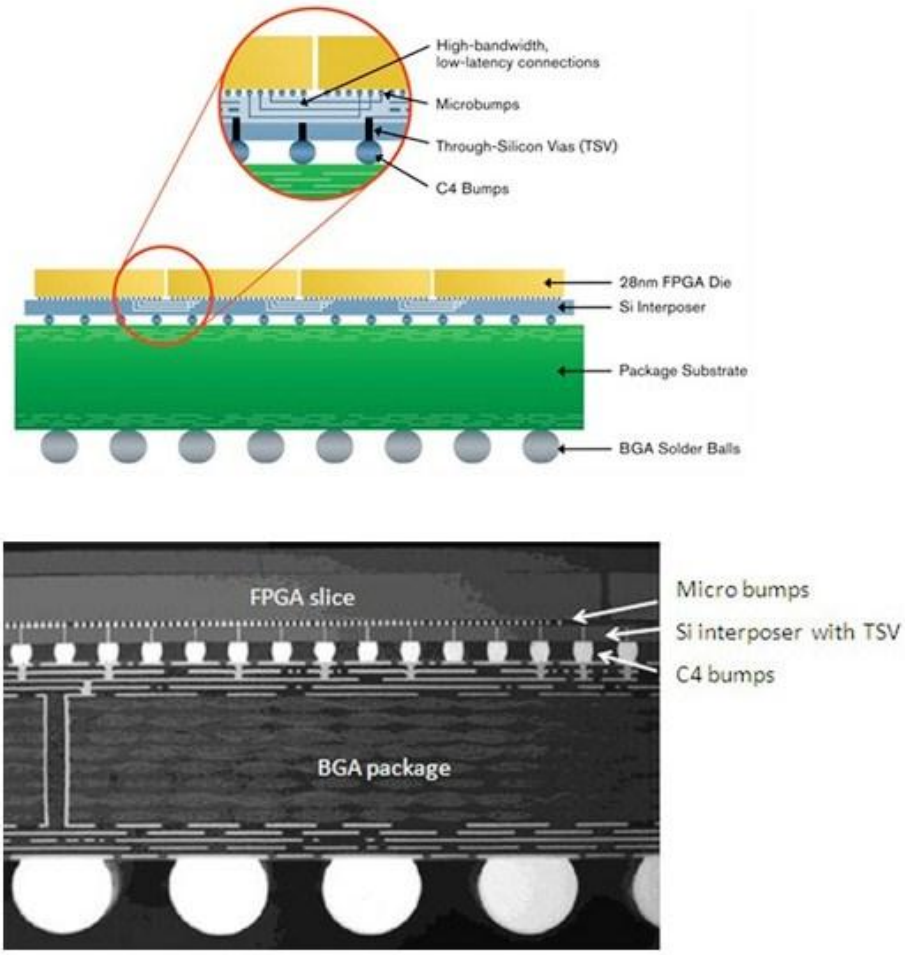


Figure AP25: 2.5D Interposer for Xilinx FPGA

3D ISSUES

Intermediate interposers must perform the functions of the base interposer with the probability of requiring redistribution wiring to match the geometries of the die connected above with the geometries of the die connected below the interposer. The coming increase in the number of die in the stack and increased heterogeneous integration will require the interposer to take on more complex functions. The interposer represents potential solutions for many of the difficult challenges. (See SiP section of this chapter.)

- Thermal management can be addressed by incorporating microfluidic channels into the interposer to circulate cooling liquids.
- Integrated passives may be fabricated on the interposer to provide decoupling capacitors, inductors and resistors.

- A relay matrix may be fabricated on the interposer to allow TSV connections to be switched. This can support test access as well as switching in of redundant components in the stack in the event a failure is detected.
- BIST and BOST engines can be located on the interposer to provide for continuous test while running. Sharing these engines through relay switching may enable sharing this resource.

3D INTEGRATION DEFINITION OF TERMS

The definitions of terms for elements of 3D integration used in this section are illustrated in Figure 26 below.

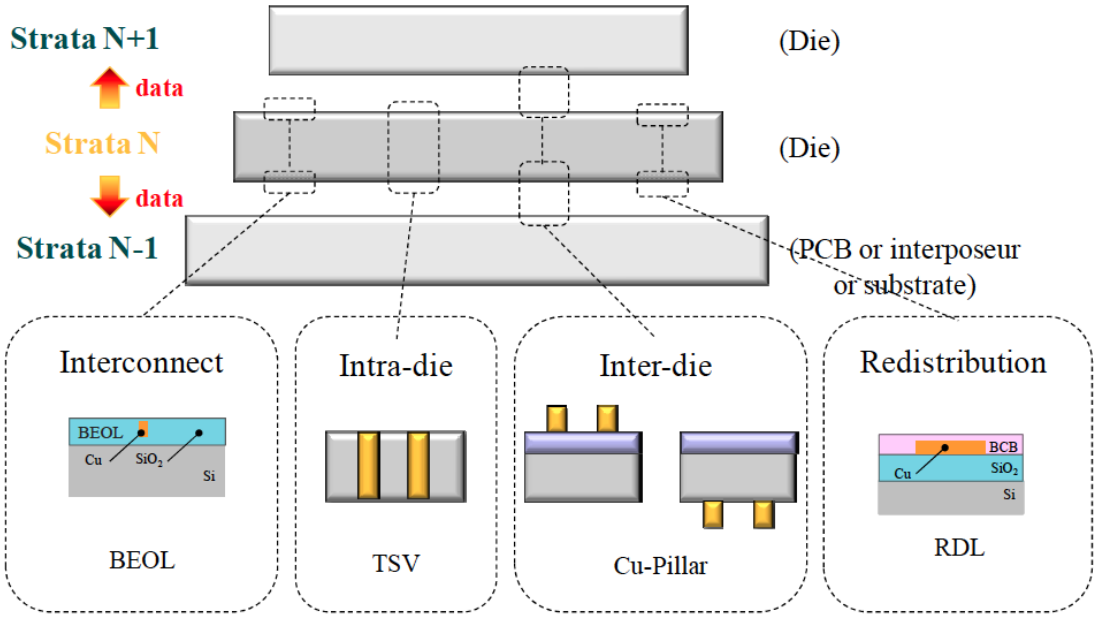


Figure AP26: A Schematic of 3D Integration

Source: IEEE ECTC

An example of process flow and equipment requirements is presented in Figure 27 below.

PROCESSES FOR 3D-TSV INTEGRATION

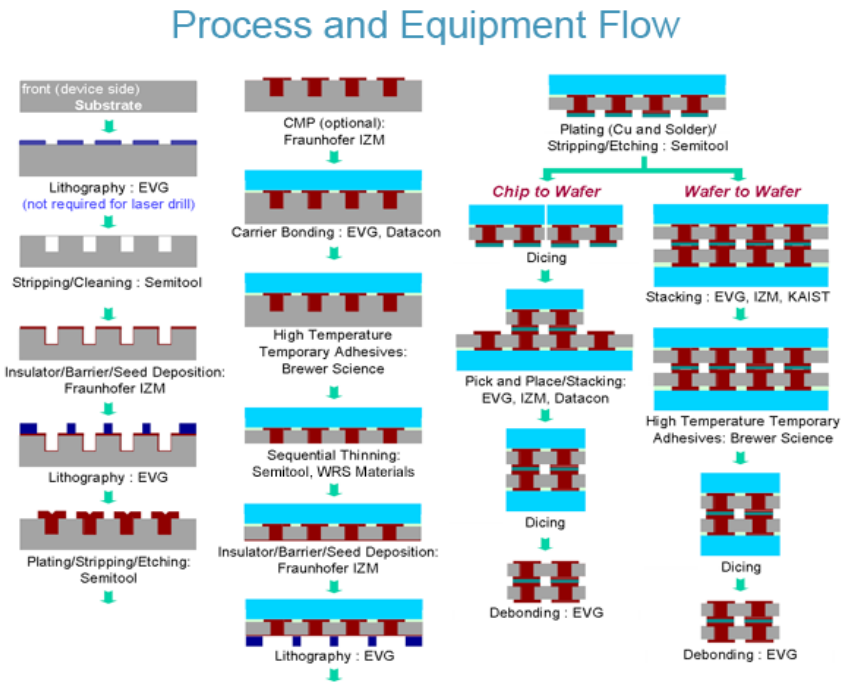


Figure AP27: Example of Process Flow and Equipment for 3D Integration

Source: EMC-3D

WAFER/DEVICE STACKING

The key technical parameters for stacking architectures are summarized on Table AP14. A variety of options have been proposed for the actual stacking of die, and packaging of the stacks. The relative merits of die-to-die (D2D), wafer-to-wafer (W2) and die-to-wafer (D2W) stacking, with the process requirements of high assembly yield, and low complexity and cost will initially point to die-to-die and die-to-wafer stacking until progress on standards and alignment accuracy allow wafer-to-wafer to be adopted. The choice will be determined based on application and economic grounds.

For die-to-die and die-to wafer stacking, the industry is focused on micro-pillar or micro-bump interconnect methods. The advantages include high through put if mass reflow process can be used and compatibility with the conventional flip chip interconnect methods.

For wafer-to-wafer stacking, the industry is currently focused on two bonding methods: metal-to-metal, which uses the preferred foundry-based TSV technology and has the advantage of simultaneously forming the mechanical and electrical bonds, and oxide bonding. Current copper-copper thermocompression bonding is very slow (~8 bonds/hr in a four-chamber tool) as opposed to oxide bonding, which requires via-last processing but is capable of performing 25 bonds/hr in a single-chamber tool. With a high alignment accuracy of better than 1 μm, which is expected to be in the sub-0.5 μm range within the next two years, interconnect pitches of 6–10 μm can enable high interconnect densities of ~1–3 million interconnects/cm^2. For the next 2–3 years, alignment capability will not be the bottleneck.

Oxide diffusion bonding is 3× faster than copper bonding. However, the electrical interconnect is formed after the bonding, thus requiring an extra process step and potentially a level of complexity. Still, from a throughput point of view, it is more attractive than copper diffusion bond processing. The challenge is not feasibility or equipment technology at this point it is cost.

In addition to the bonding techniques needed and various wafer/device stacking configurations, the stacking sequence and the coupling with the TSV revealing (or protrusion) and packaging assembly processes are also critical to achieving high assembly yield. Tezzaron has pioneered wafer-to-wafer bonding with the tungsten (W) TSV to

serve as the "Super Contact". By firstly using a face-to-face, copper-to-copper bonding, and then followed by the TSV revealing and consequently face-to-back bonding, the 3D wafer stacking is achieved without using a supporting wafer [10]. For 3D heterogeneous integration, like integrating a CPU or GPU with a 3D stacked, high bandwidth memory cube on a silicon interposer or directly on top of the processer, it is required that the Known-Good-Die-Stacks (KGDS) are made available to the final module integrator. To make and deliver the KGDS, die stacking on a carrier wafer and then following by reconfiguration and probing processes are developed. Over-molding of the memory die stacks while still on the carrier wafer is also developed to improve the mechanical integrity of the 3D die stacks and test access ability [11].

Similarly, for the completed 3D IC stacking and packaging assembly flow, Chip-on-Chip-First (CoC-First), Chip-on-Substrate-First (CoS-First) and Chip-on-Wafer-First (CoW-First) processes are evaluated and developed. Each has its own advantages and disadvantages. From providing a completed end-to-end, turnkey solution perspective, the CoW-First process has been adopted by one of the major wafer foundry supplier [12].

TSV INTERCONNECT METHODS

The process technology for TSV formation is fairly well established. They are now manufactured in high volume for camera modules and they are in production for 2.5D interposers with other applications in development. There are a variety of interconnect methods for different applications that are addresses in Table AP21.

Table AP21: TSV Interconnect Methods

EMERGING INTER-DIE INTERCONNECT

A stacking solution with high throughput and high reliability is needed to meet the cost performance requirements of the markets. One potential solution is to use the speed of oxide bonding (or some equivalent direct interconnect bonding process), which uses foundry-based vias forming metal-to-metal bonds.

One such technology is Direct Bond Interconnect (DBI) covalent bonding technology, which enables room-temperature W2W or D2W bonding. With DBI, nickel can be used to interconnect to copper, tungsten or aluminum TSVs, while providing for adequate planarity of the oxide/metal interface to achieve a strong, reliable bond. The direct bond interconnect process flow, one of the promising options for 3D integration, offers high throughput and low process temperature as illustrated in Figure 28 below. Table AP21 summarizes selected properties of the bonding processes for 3D TSV interconnect methods.

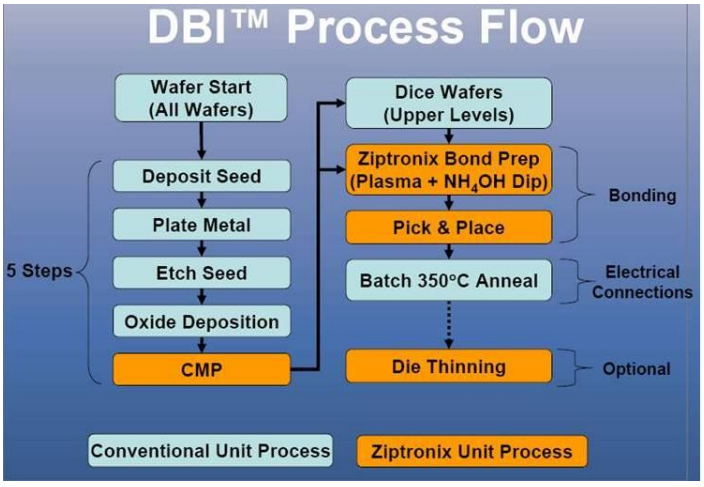


Figure AP28: Direct Bond Interconnect Process Flow

Source: Ziptronix

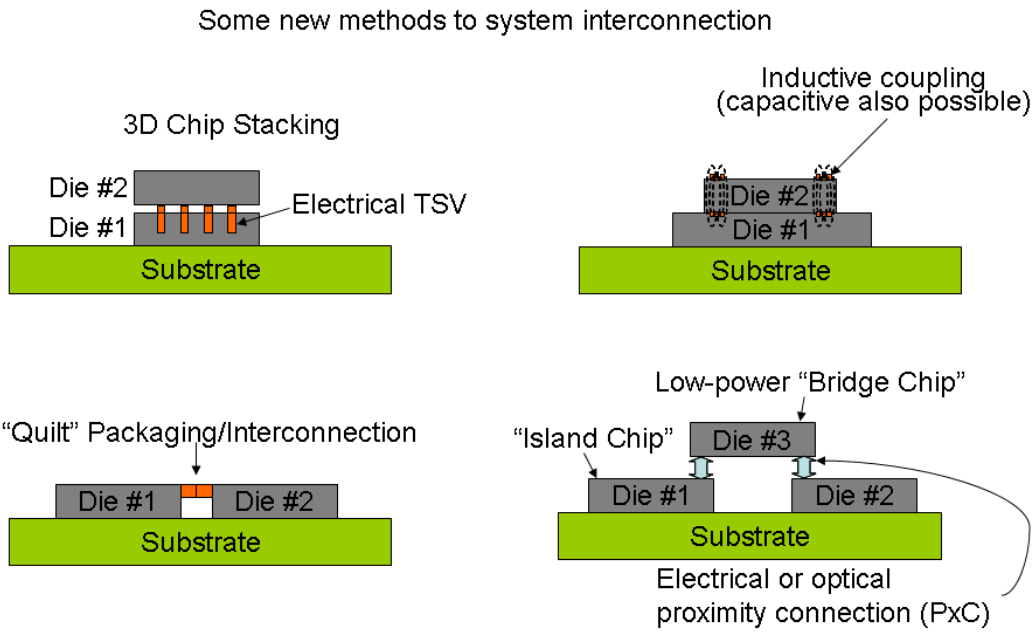


Figure AP29: Methods of System Interconnect for 3D Integration

Three-dimensional chip stacking can be accomplished in a number of way, but in general, require through silicon vias to enable vertical electrical interconnection. In some proposed 3D stacking methodologies, electrical TSVs are not used. Rather, inductors are integrated in each of the stacked dice, possibly using semiconductor BEOL processing, and used for inductive wireless communication [13–14]. Capacitive coupling has also been demonstrated for 3D stacked die [15]. It requires the die be face-to-face bonded and have at most a small gap between the chips (i.e., a short distance between the electrodes) in order to maximize transmitted voltage. Inductive coupling can overcome this limitation as it can provide communication through the silicon substrate (thus face-up-to-face-up bonding is possible, for example). However, as the communication distance between the inductors increases, the diameter of the coil has to increase for a given transmitted voltage, and the spacing between coils may increase to avoid coupled noise. Using inductive coupling, 19.2 Gbps/channel at an energy efficiency of 1 pJ/b has been demonstrated [13]. Power can be delivered using wire bonds as well as using inductive coupling [16].

Quilt packaging is based on the fabrication of microscale nodules on the periphery of each chip to enable direct die-to-die edge interconnection [17–18]. This enables one to bypass the package based interconnects and provide, in principal, a seamless electrical die-to-die interconnection. The microscale nodules can be bonded using a number of processes including solder.

Yet another method to system interconnection is depicted in the figure above [19–21]. Proximity Communication (PxC) technology enables die to be tiled and interconnected in a face-to-face topology. The interconnection between the tiled face-to-face formed dice can be achieved using capacitive or optical coupling. When capacitive coupling is used, each electrode of the capacitor is formed on either of the dice, while when optical coupling is used, two mirrors (or grating couplers), one on each chips, are aligned to provide vertical interconnection between optical waveguides. Low power silicon-photonic communication was demonstrated using this technology.

3D Integration of Logic and Memory

While multi-core, and eventually many-core, processors will provide a means for improving processor performance and power efficiency, the demand for off-chip bandwidth will greatly increase as the number of cores increases [22–25]. In an effort to address this ever increasing demand for off-chip bandwidth, a number of innovations in off-chip interconnection and system integration are being pursued by industry and academia.

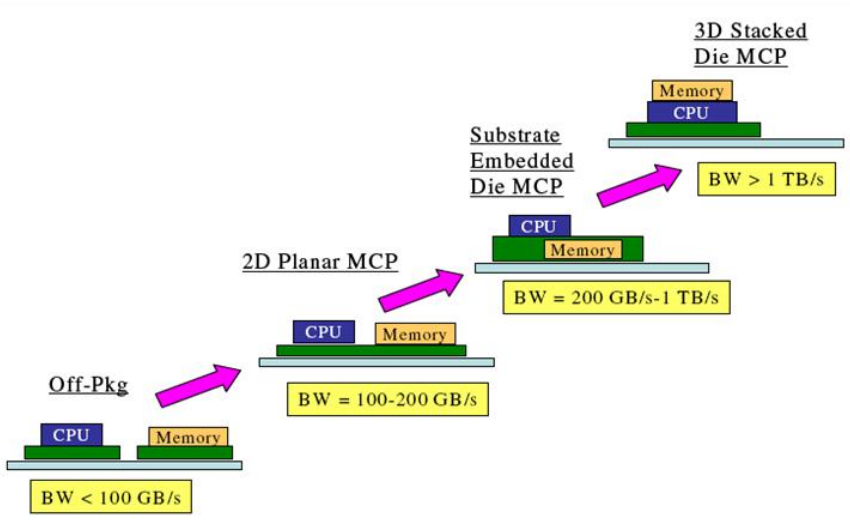


Figure AP30: Roadmap for Package Transitions Addressing the Memory Bandwidth Challenge

Source: Intel Technology Journal Vol. 11, pp. 197–205, 2007

Latency, bandwidth (bandwidth density), power dissipation (or energy in pJ/bit), Bit Error Rate (BER) and cost of the overall off-chip network (which includes the drivers and receivers) are metrics that must be optimized. This will involve the migration to and/or integration with optical interconnects, 3D integration using through-silicon-vias (TSVs), capacitive and inductive signal I/Os, and other innovations in packaging and system integration. Some of these are illustrated in Figure 30. While each of these methods of interconnection has advantages and disadvantages, they each are intended to greatly improve off-chip signal connectivity in a system.

POWER INTEGRITY

The issue of power integrity for 3D-SiP packages becomes more challenging as the number of transistors rises and the operating voltages decreases. This is addressed in further in this chapter.

THERMAL MANAGEMENT

While three-dimensional ICs provide low-energy and large bandwidth density signaling, thermal challenges in 3D can be significant and require careful design. In a single chip, heat can be readily accessed and removed from the back side (bulk silicon side) of the die. In 3D, when chips are stacked, there is no direct access to the back side of the chips in the stack nor a method of spreading the heat laterally from the stack. Thus, because of the increased power density after die stacking, high thermal resistance path for the embedded chips in the stack due to various low-thermal conductivity materials in the stack, maintaining all die in the stack at acceptable junction temperature may be difficult. The challenges in cooling are increased due to the fact that power dissipation is non-uniform across a die leading to the formation of hot spots. In one study, it was shown that increasing TSV density in the region of hot spots can reduce peak temperature [26]. Increasing the thermal conductivity of the chip to chip interfaces within the stack would be beneficial in 3D thermal management. For that, metal bumps for thermal conduction purposes and high conductivity underfill material are some of the important considerations. For high power applications, improving the thermal conductivity path may not be sufficient, which has caused researchers to explore embedded thermal cooling technologies within the stack. For example, the use of embedded microfluidic heat sinks within the chips in the stack has been demonstrated in both academia and industry [27–28]. In one study, liquid cooling of a two tier 100W/cm^2/tier chips shows junction temperature of less than 50°C per tier [27]. However, one of the challenges with embedded microfluidic cooling in a stack of chips is the need to integrate TSVs within the relatively thicker silicon layers (silicon layer may increase due to the thermal resistance and pressure drop design requirements of the microfluidic heat sink). Recently, 10-micron diameter TSVs have been integrated in a micropin fin silicon heat sink for 3D ICs [29].

TEST FOR 3D INTEGRATION

Test access for 3D package architectures is sometimes not available with current technology. New methods to ensure functionality and reliability will be required. The solution will require access points to be designed into the package design at the die stack level. The inclusion of built in self-test (BIST) and built off chip self-test (BOST) elements will also need to be incorporated into the package.

The test requirement is dramatically increased by the fact that transistors at the smallest nodes will wear out. The Roadmap projects transistor count in the hundreds of billions for complex 3D SiP packages and even a very slow wear out rate may prevent the adequate reliability. This requires not only ensuring proper function when a package is initially completed but also some mechanism of continuous testing and self-repairs. Package designs will have to incorporate test elements to ensure reliability of complex systems over their design life.

RELIABILITY IN 3D INTEGRATION

3D chip stacks will experience the same environmental, mechanical and electrical stresses as in single chips during operations. However, in the 3D chip stack, there are extra silicon layers, called strata, and TSVs, which add more structures and complexity to the system (Figure AP28). The additional level of electrical interconnections introduces new failure opportunities and mechanisms for the 3D system. For example, mechanical stress, which modulates device mobility and Vt, can have negative impact on the performance of certain field-effect transistors (FETs). Similarly, the combined use of ELK dielectrics in BEOL with harder interconnect materials used in packaging (such as Cu pillars or Pb-free interconnects) is exacerbating Chip-Package Interactions (CPI) that cause delaminating, cracking and or fracturing of various materials that often limit yield and reliability for advanced packages. The increased power density and thermal gradient in vertical and horizontal directions related to TSVs and stacking of thin dice can also create unique reliability issues. It's very important to identify, evaluate and understand the reliability implications associated with 3D integration [30].

To manage the stresses in the 3D system, a Design-for-Manufacturing and Design-for-Reliability methodology needs to be implemented. Design rules that include properly defined TSV keep out zones and thermal-aware design flow should be part of the design environment for the 3D design tools.

To improve the yield and reliability of the 3D chip stacks, Built-in Self-Test (BIST), redundant interconnect structures and In-field repair mechanisms at the transistor and interconnect (including TSV) levels are needed. For example, a simple but effective solution is to add redundant TSVs which can be used to replace failed TSVs. This idea has been realized in 3D DRAM designs [31].

8. PACKAGING FOR SPECIALIZED FUNCTIONS

OPTOELECTRONIC PACKAGING FOR DATA TRANSMISSION

SCOPE

This section covers semiconductor packaging topics related to the use of photons to transmit data over distances of 100s of km down to mm on-chip.

OPTICAL DATA TRANSMISSION

The packaging methods for telecommunications applications, meaning distances over 10 Km at data rates usually over 1 Gb/s, are well established and generally follow the Telcordia, or less demanding Ethernet and CATV standards. The major packaging issues relate to:

- reducing cost
- implementing data rates of 400 Gb/s and higher
- provisioning and building out dense wavelength division multiplexing technology
- reducing the energy per bit transmitted
- saving space
- eliminating heat
- providing alignment at low cost

- supporting photonic integrated circuits (active) and planar lightwave circuits (passive)
- supporting multiple optical lanes per port to raise data densities

Table AP22 lists the challenges for optical packaging.

Table AP22: Difficult Challenges for Optical Packaging

Electronic vs Optical Data Transmission

Main Potential Benefits of Optical Technology

- **utilizes less energy per bit to transmit data over distances as short as 1 meter(pJ/bit)**
- **bandwidth of 10s of Gb/s, even Terabits/s**
- **data density of 10s of Terabits/mm².**

Implications of Optical Wavelength

The wavelength of light used is ~ 1 micron. While that is quite small it is relatively large compared to the 45nm features common in semiconductor devices. A key result is that utilizing photons to transmit data on-chip, or to process data logically, requires much more space than doing so utilizing electronic methods.

Figure AP31: Electronic vs. Optical Data Transmission

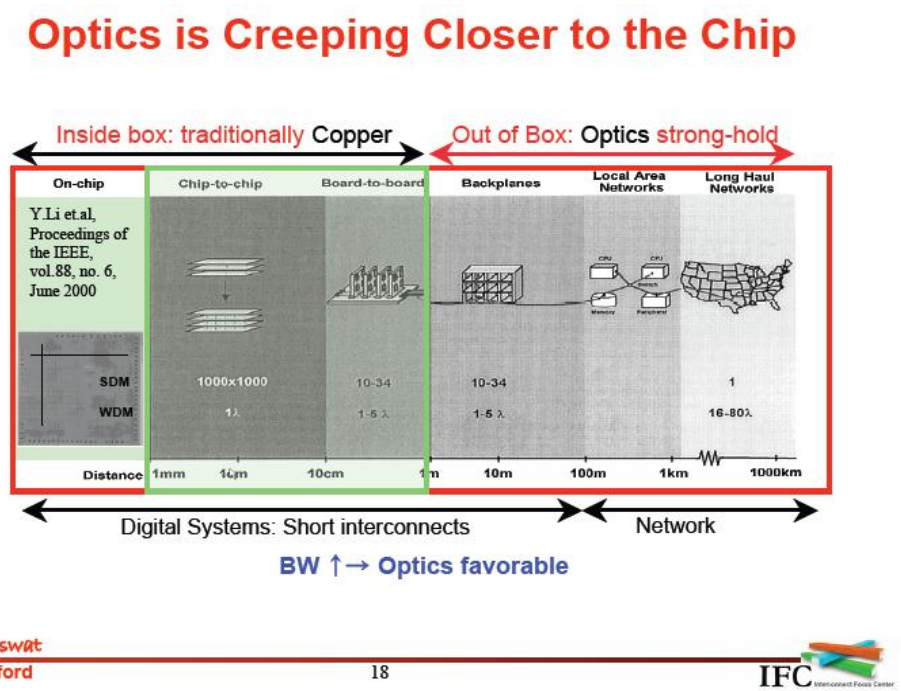


Figure AP32: Overview of the Role of Optical Data Transmission versus Electrical Methods Illustrating Optical Methods Moving Down to the Meter Distance as Data Rates Increase into the Gb/s Range

The graphic above provides a good overview of the current and potential applications of optical data transmission technology. In summary, optical methods have replaced electrical transmission for distances greater than a few kilometers, are widely used in application down to 1 meter, and are being explored for high density, on-to and off-of chip, data transmission. (Emerging high end microprocessors require data rates of ~ 5 Tera bits/sec, both on-to and off-of chip. See Table AP23, row 6.) In general, as data rates go higher, optical methods become more attractive at shorter distances. Table AP24 lists the optical packaging potential solutions.

Table AP23: Technology Requirements for Optical Packaging

Table AP24: Potential Solutions for Optical Packaging

TELECOMMUNICATIONS DEVICE PACKAGING

The graphic below shows a photonic integrated circuit (PIC) from Infinera that integrates many optical functions on one semiconductor chip of III-V material and combines that in a package with conventional CMOS devices. The fiber out of the package interfaces to the laser through an optical chain but does have the important and expensive requirement for sub-micron alignment in at least 2 dimensions.

This hermetic package, with a fiber pigtail, is typical of conventional Telecommunications single mode devices. Telecommunications is starting to replace fiber pigtails that must be spliced with optical connectors that are easier to handle, maintain and manufacture.

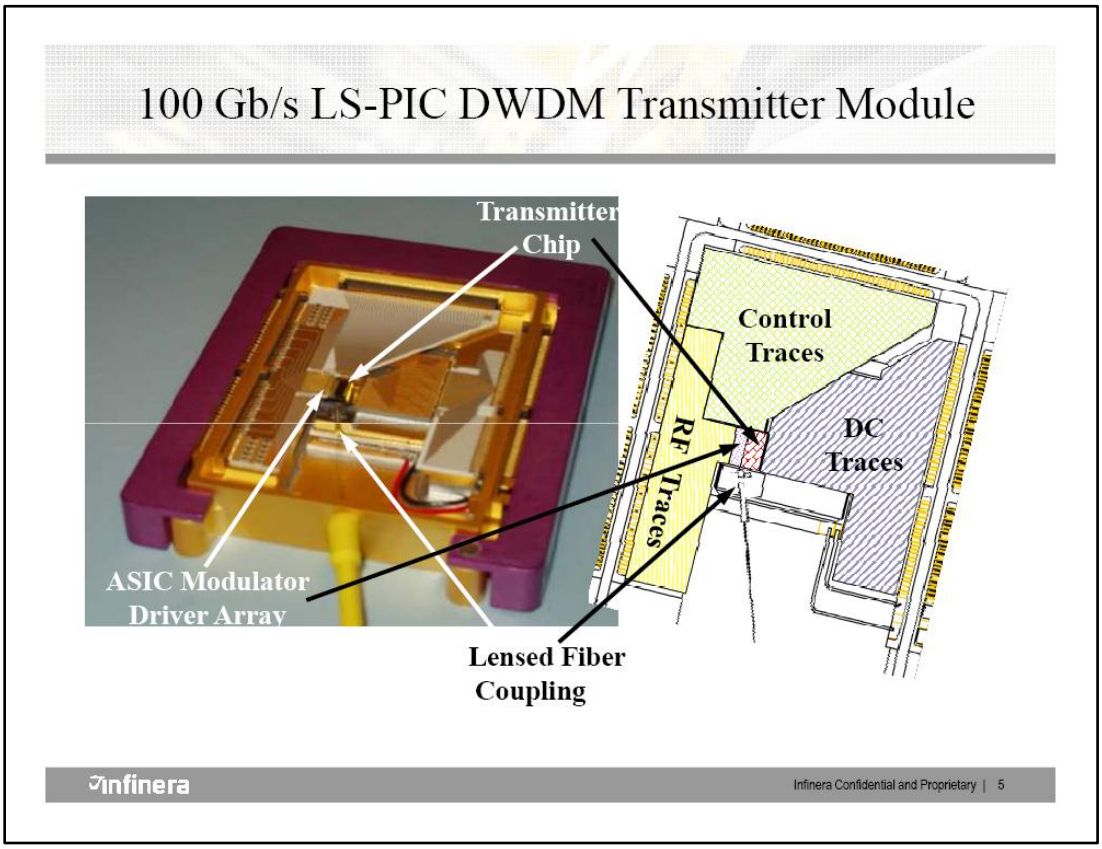


Figure AP33: A telecommunications Transmitter Module from Infinera

PHOTONIC INTEGRATED CIRCUIT PACKAGING

Increasingly important optical electronic manufacturing processes are those used to build Planar Lightwave Circuits (PLC) and Photonic Integrated Circuits (PIC). As data rates increase, and more optical wavelengths are transmitted through one fiber, the role of PICs included in System in Package configurations is likely to increase. The graphic

below illustrates a Photonic Integrated circuit (PIC), in this case a modulator. The PIC concept is being explored and implemented when multiple optical functions are needed for an application.

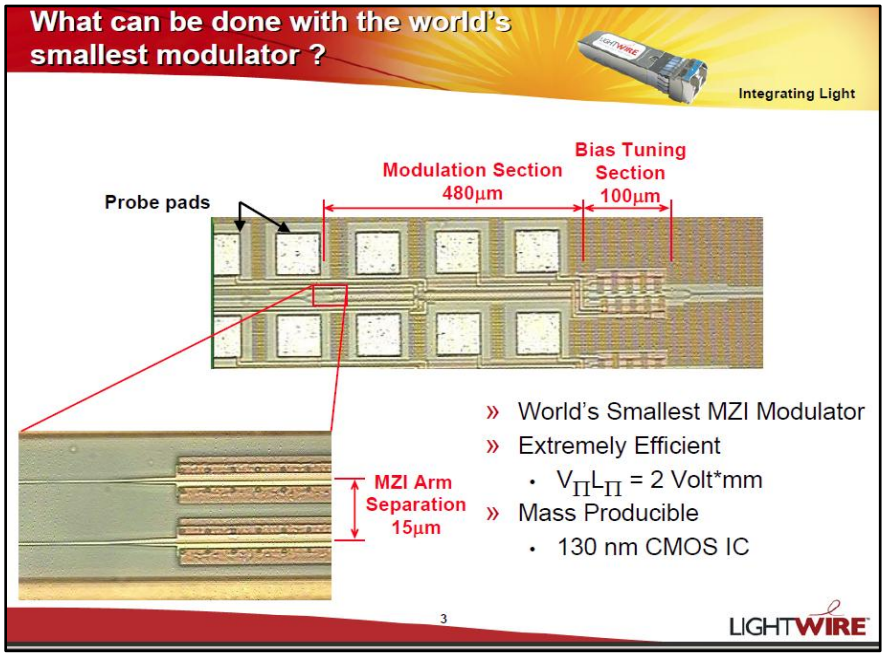


Figure AP34: Even the World's Smallest Modulator is Large vs. Transistors

The modulator illustrated above is fabricated on a conventional silicon substrate in a manner that is compatible with CMOS fabrication technology. That is a desirable combination because of the reduced costs resulting from utilizing CMOS technology.

The packaging issues for PICs are similar to those for telecommunications devices because PICs usually utilize single mode technology that requires sub-micron alignment and often hermetic packaging to retain that alignment over time.

PICs differ from PLCs, discussed below, because PICs include active optical devices such as lasers, photodetectors, modulators, and optical semiconductor amplifiers (OSA). The active functionality is achieved by utilizing III-V semiconductors such as InP or GaAs. PICs are fabricated utilizing semiconductor manufacturing methods of diffusion, sputtering, lithographic patterning, etc. Even though a PIC fab is expensive to build, PIC foundry services are widely available.

Silicon used for making integrated circuits, especially CMOS devices that are the backbone of the electronics industry, are not suitable for PICs because they will not lase or amplify light. That is an unfortunate character of the base material. Much effort is going into developing technology that is compatible with CMOS device fabrication to provide active optical functions such as lasing.

PLANAR LIGHTWAVE PACKAGING

PLCs are passive structures made on silicon, glass or polymer substrates utilizing some patterning method to define the waveguides. Splitters, multiplexers, demultiplexers, Bragg gratings, etc, can all be fabricated as PLCs. PLCs are an important component of many optical products discussed in this chapter. Multiple processes from multiple vendors are available and used to fabricate PLCs. PLC often have active devices such as lasers or photodetectors mounted on them and usually have to interface to optical fibers or other waveguides.

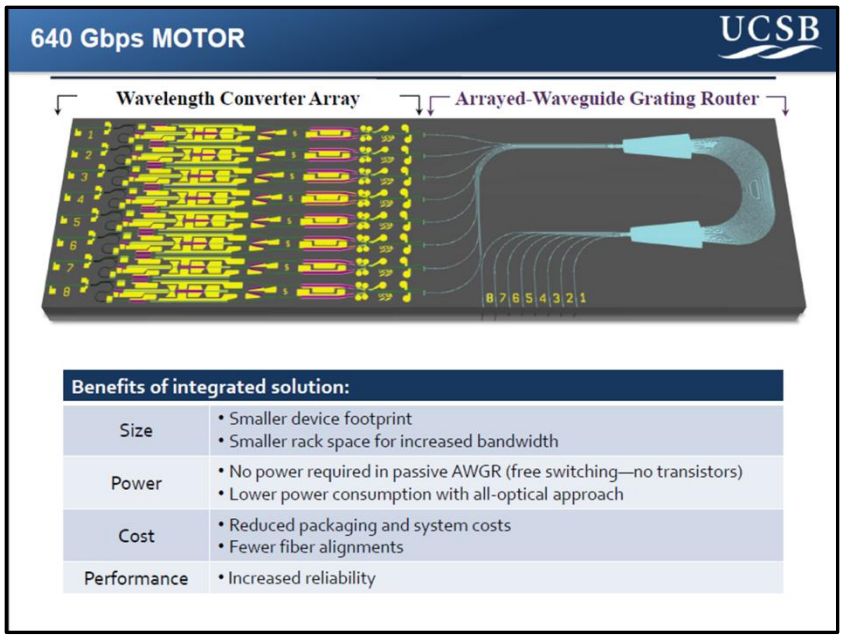


Figure AP35: A Planar Lightwave Circuit, a Passive Device that Requires No Power

Some of the PLC materials are quite stable (glass with waveguides made by diffusing a compound into the glass to raise the index of refraction, for example), and do not require hermetic packaging. Nonetheless, the other devices and materials they are combined with are frequently not as robust, hence hermetic packaging is still frequently used with these structures.

Whether non-hermetic packaging can eventually be used in at least some telecommunications applications is unclear.

LOCAL AREA NETWORK (LAN) TRANSCEIVER PACKAGING

The packaging issues for the standardized, well established local area network (LAN) applications over distances of 10 meters to 10 Km, are largely cost reduction driven. At the same time, the data rates and data density (amount of data transmitted per unit of rack face, for example) continue to increase. These applications often use multimode technology, connectors with 2 fibers, one to transmit and one to receive, and increasingly use plastic optical fiber. These methods eliminate sub-micron alignment and minimize assembly and field installation issues. They are, however, limited in the data rate × distance capability to ~ 1 kilometer × 1 Giga bit per second by mode dispersion.

The graphic below shows a series of packaging solutions that have been implemented over the years to serve this market. The graphic highlights the continuing reduction in size and increasing data rates that have been achieved and continue. Approximately 100 million transceivers of all sorts are built each year. The continually increasing volumes have enabled cost reduction.

The interior structure of these transceivers incorporates:

- A conventional PCB with small SMT parts and an electrical connector
- A few CMOS chips to provide various functions
- A laser and a photodetector
- 2 halves of an optical connector
- 2 optical chains that interfaces between the connectors and the laser and photodetector
- A case capable of dissipating ~1 to 10 watts of heat

The components are assembled using conventional SMT, direct chip attach such as flip-chip, and combine those methods with careful mounting and alignment of optical components, particularly lenses, mirrors, splitters, connector ferrules and heat sinks.

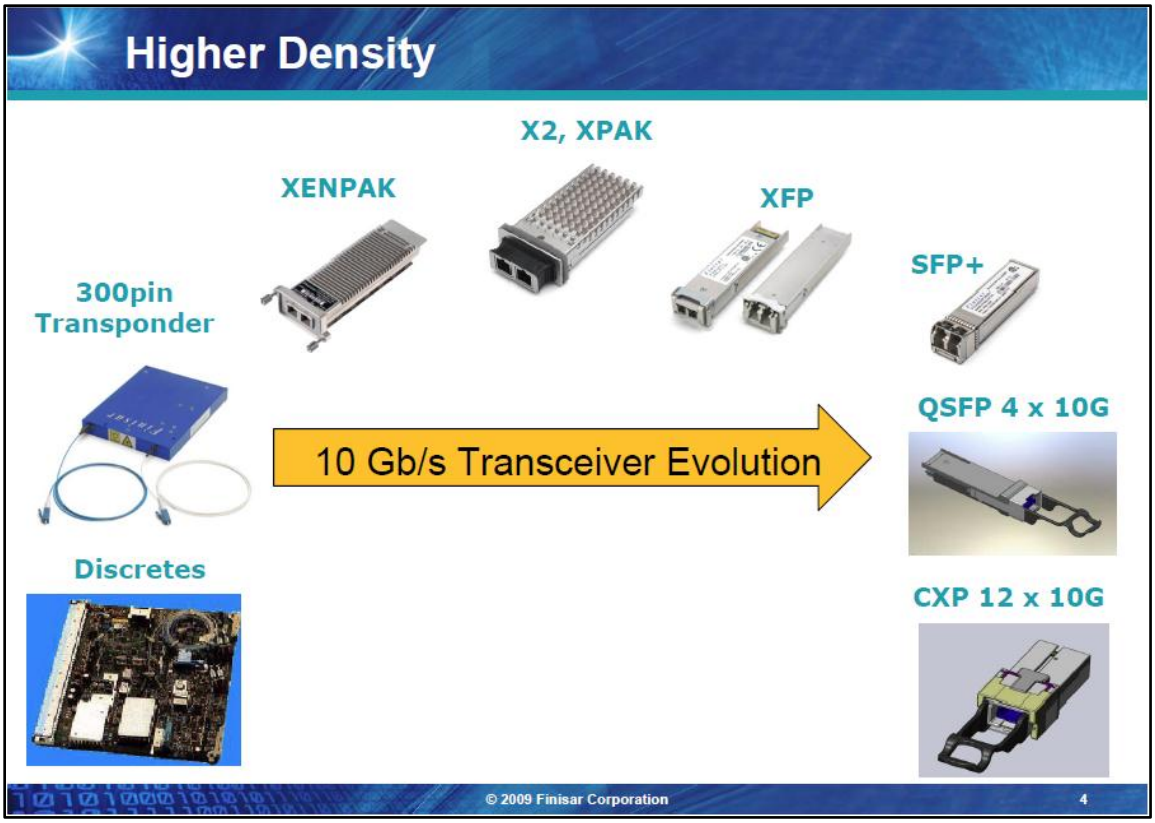


Figure AP36: The Evolution of Optical Transceivers Over the Last 30 Years

The graphic below illustrates the increasing data densities in recent years. With data densities and total data transmitted growing at least as fast as Moore's Law (doubling every 2 years), demand for greater LAN component packaging densities will continue to increase. The cost of many LAN transceivers is low partially due to the Multi Supplier Agreements (MSA) that the industry has developed. These agreements standardize form factors and the data protocol but leave the method of achieving those requirements to each manufacturer.

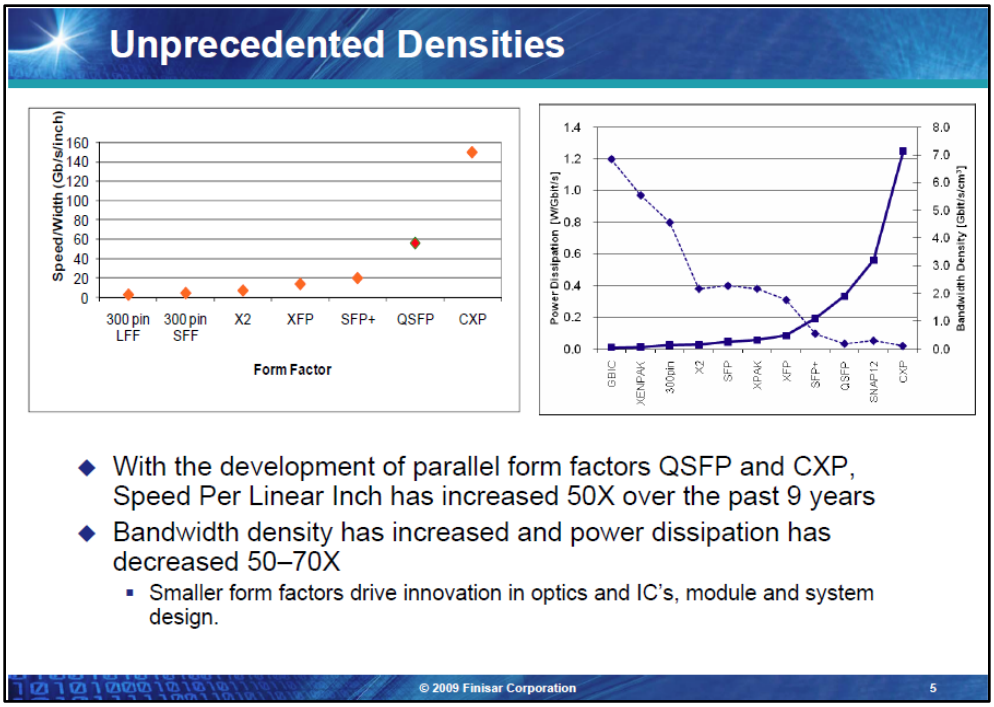


Figure AP37: The Evolution of Rack Density on the Left in Gb/s/inch and Power in Watts/Gb/s or the Right as the Transceiver Form Factor Changed

ACTIVE OPTICAL CABLE PACKAGING

The Active Optical Cable (AOC) shown to the right is an example of one of the newest optical devices that requires packaging. An AOC transmits from one point to another using optical methods but the interfaces to the end points between which the data is transmitted are electrical. Thus, the "electrical connectors" at the ends of the cable contain electrical to optical and optical to electrical converters. Data is transmitted through the fiber using optical protocols. Electrical power to make the convresons and manage the process is scavaged from the electrical ports. AOC typically transmit data at 5 to 10 Gb/s through multiple multimode fibers. Most arre duplex but utililze separate fibers to transmit data in each direction. The main benefit they provide is transmitting data with ~ 75% less power (typically 8 to 25 pJ per bit) and requiring ~75% less space than the coper they replace.

Figure AP38: A Luxtera Active Optical

The packaging issues for AOCs are similar to those for LAN transceivers, mainly because AOCs actually replace those tranceivers in many applications.

THE AVAGO MICROPOD

The Micropod optical cable system, was developed by IBM, Avago and Molex to transmit data distance of 10 cm to several meters in supercomputers. The Micropod shown in the illustration below, measures 7.8 mm × 8.2 mm, has 96 balls, and 12 multimode optical fibers that interface to either VCSELs in a Tx Micropod, or a photodetector in an Rx Micropod. Data is transmitted at 850 nm at 10 Gb/s through all 12 fibers and requires ~ 25 pJ/bit transmitted.

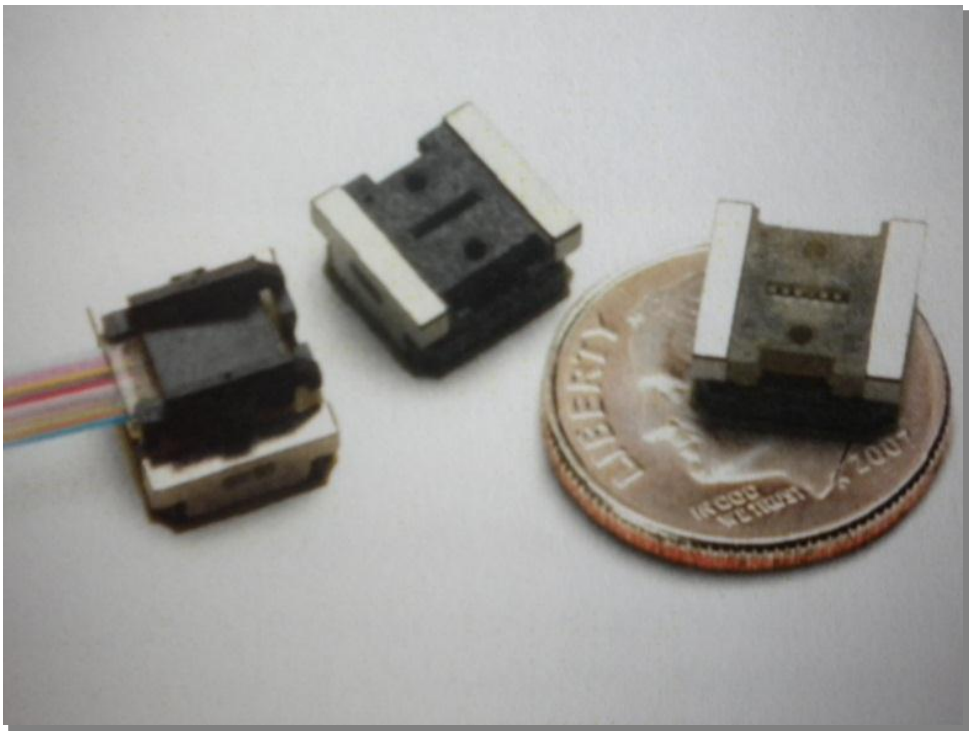


Figure AP39: The Micropod Optical Cable System

The Micropod is not an AOC because it has optical connectors at each end of the fiber that not only enable the usual "make and break" function but turn the light 90 degrees from the "horizontal" to the vertical" to interface with the VCSELs and photodetector arrays.

The manufacturing capabilities needed for the electronics portion of optical data communication products are well known. Developing products that can be manufactured at the lowest cost is complex due to the need to combine optical methods, with their high tolerances and larger numbers of materials, with conventional semiconductor packaging and electronic components. Success requires building a design and manufacturing team that is able to integrate all of the requirements, including the optical components, in a robust, reliable product and then developing a supply chain to provide the components, subassemblies and final assembly.

Design complexity, meaning multiple parts that must be tooled and then assembled, is a major reason that OE devices are costly to manufacture. The Avago MicroPOD, shown in a blow-up on the right is an example of an OE product designed for automatic assembly. This sketch shows 18 parts and does not include one half of the optical connector or the ribbon fiber. The complexity results when optical technology is combined with electronic technology.

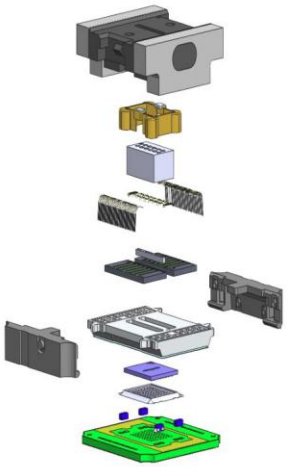


Figure AP40: The Avago MicroPOD

PLASTIC OPTICAL FIBER DEVICE PACKAGING

Plastic optical fiber (POF) for applications less than 100 meters is growing in importance for transportation, meaning mostly automotive but also aircraft and military use. As with AOCs, this packaging technology is undergoing rapid cost reduction with the goal of achieving < $1/Gb/s.

The graphic below illustrates some of the highlights associated with POF. POF offers important advantages in weight, EMI reduction, and cost, especially when data must be transmitted relatively short distances, such as 10 meters, and must be transmitted between many points.

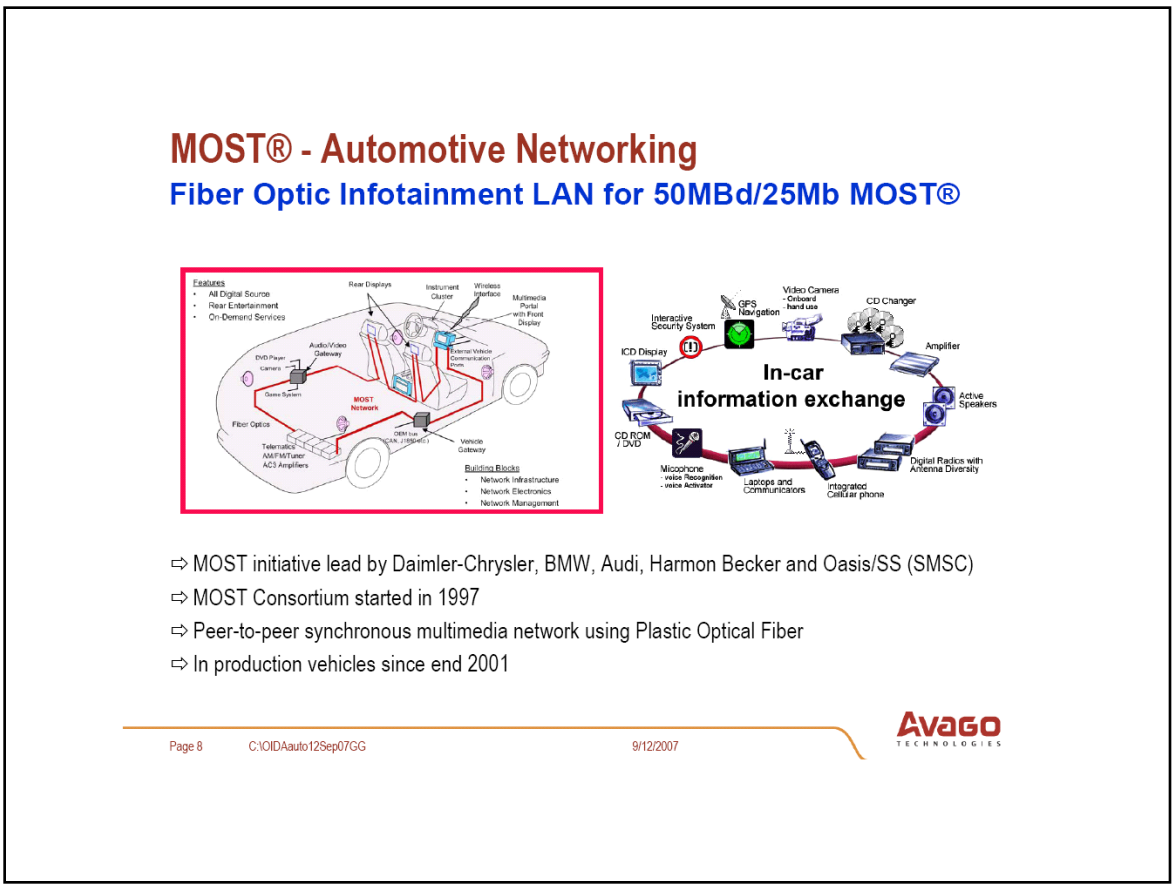


Figure AP41: The Use of Plastic Optical Fiber (POF) in Automotive Applications

The cost of terminating mm POF is quite low. The graphic below illustrates a typical automotive connector. POF can be terminated to this transmitter by simply cutting it with a simple tool at 90 degrees to the main axis and pushing it into the connector receptacle. The Rx termination is similar.

Packaging of the transmitters and receivers for POF is conventional. The modulated light source, modulating and managing electronics are mounted on a substrate, typically a small circuit board, using conventional assembly methods. Alignment of the female optical connector to the optical source or detector is relatively easy due to the 50 micron size of the multimode fiber core.

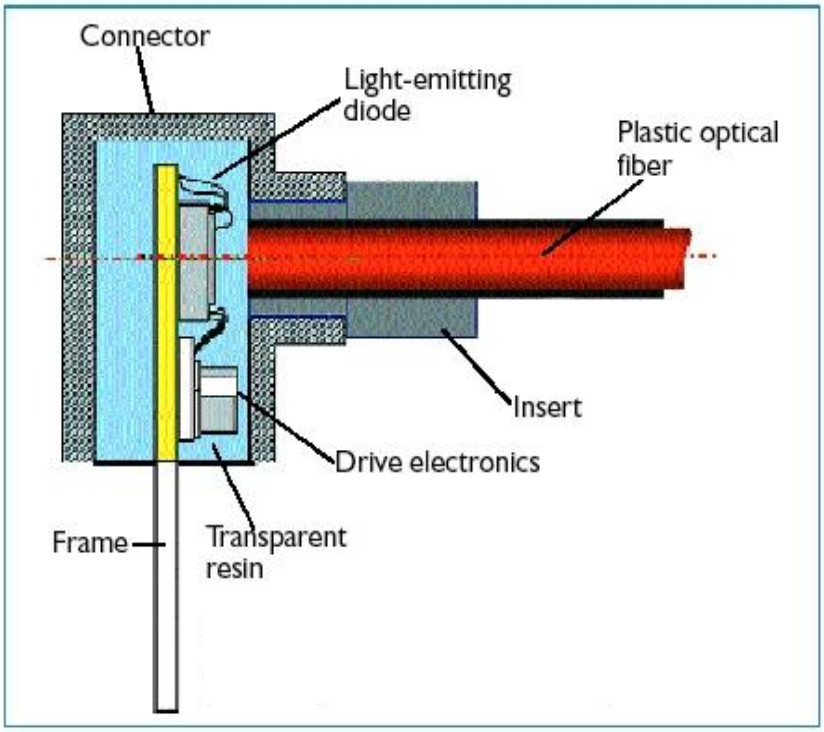


Figure AP42: Connector, Light Source, and Plastic Optical Fiber are Easily Interfaced

HIGH DATA DENSITY OPTICAL DEVICE PACKAGING

Interest is growing in utilizing optical methods to transmit data into and out of semiconductor packages. Interest is driven by the very high IO data density that can be achieved with optical methods and by the relatively small amount of power lost with increasing distance compared to electrical methods.

The methods of packaging optical technology for distances < 1 meter are the subject of continuing R&D by many organizations. These assemblies fall within the System-in-Package class of assemblies described in other sub-sections of this Chapter. The drivers for these applications are increasing data rates and power reduction, ideally without cost increases.

The major issues include:

- the limit of electronic methods (the general opinion is that electrical methods are viable up to 18 Gb/s over distances of up to 1 meter if signal conditioning and detection, SERDES, are used) methods to implement optics in backplanes
- methods to implement on-to and off-of chip data transfer
- the impact of through silicon vias (TSVs) and the option of stacking chips made with different technologies.

The following graphic from Reflex Photonics illustrate methods of implementing optical IO. The graphic utilizes electrical connections on the substrate to take data electrically to the 4 edge modules near the corners where data undergoes E to O or O to E conversion. This implementation utilizes optical ribbon fiber connectors on the four corners to interface to optical ribbonfiber. The package also has conventional BGA balls to bring power and signals into the chip through the substrate in the conventional manner.

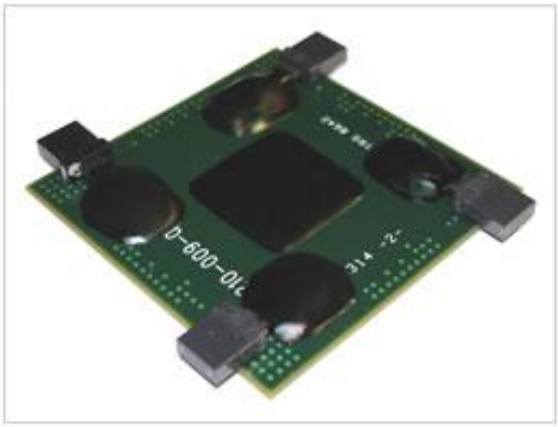
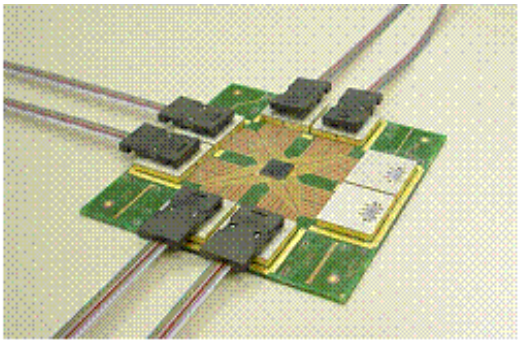


Figure AP43: Gb/s Data Rates On-to and Off-of Chip Using Optically Connectorized Chip Packaging per Reflex Photonics

Packaging this device requires utilizing conventional BGA methods but adds the complexity of incorporating 4 optical transceivers. These transceivers are built utilizing methods similar to those described above for LAN transceivers.

The graphic below illustrates several concepts that are being explored to provide greater IO data density and provide high bandwidth between packages that are within 10 cm of each other. These utilize a substrate that has optical waveguides added to a conventional circuit board. Incorporating waveguides in circuit boards has been widely explored. Several methods of building these dual purpose boards are available and are in production for specialized applications.



OE module (fibre pigtailed/optical connector)

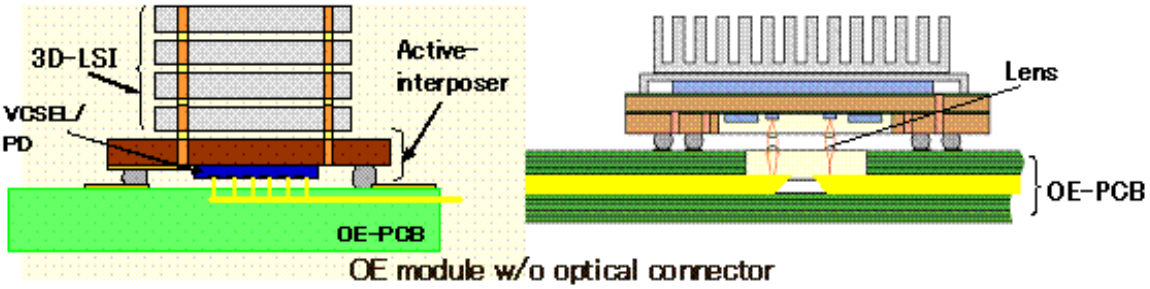


Figure AP44: An Optical Wiring Board Based on the Work of Mr. Takahara of NTT

Presented at IEC/TC86/TC91/JWG9 at Locarno, Switzerland on 2009-04-22.

The assembly process for the type of semiconductor packaging above is illustrated in the process flow graphic below. Much of this looks like conventional assembly. However, for optical devices, a few unique requirements often arise. These include:

- Minimizing dirt and dust that interfere with light transmission and result in light loss
- Unusually tight assembly tolerances. (Multimode require ±5 microns; Single Mod requires ±0.1 microns.)
- Non-planar assembly meaning precisely fixing parts in the 3rd dimension
- Long term stability to temperature and humidity cycling and mechanical stress
- Stable optical adhesives to avoid loss of transparency due to aging
- Control of heat whose source varies over time and even location within a package.

The graphic below illustrates the process used to build a specific product.

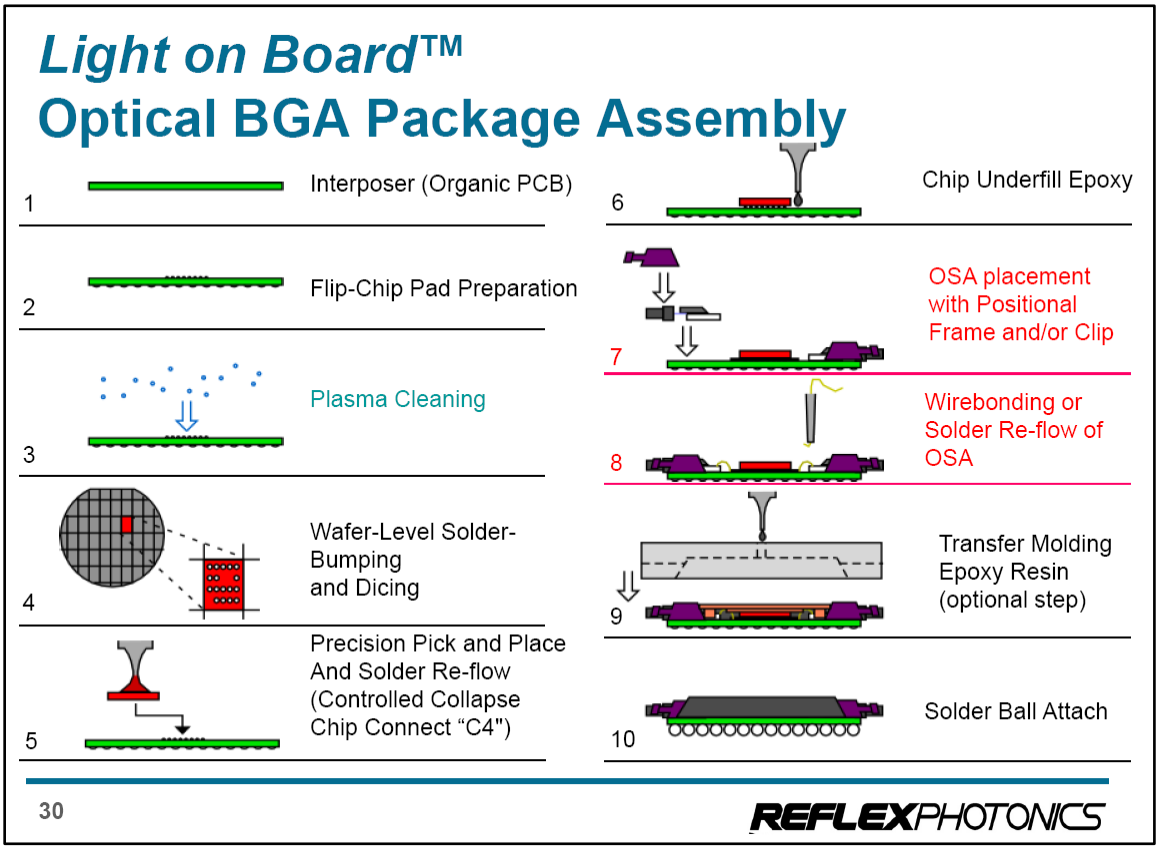


Figure AP45: Manufacturing Process for an Optical Product

PACKAGING PHOTONIC STRUCTURES ON-CHIP?

The final potential data transmission packaging issues relate to optics-on-chip where the motivation is achieving the data rates required, especially to interface multicore processors to memory, and in principal, to reduce power requirements. A consensus has not emerged regarding the role of optics, if any, in this application. Not only are packaging issues being re-evaluated, but system architecture and physical structures as well. One view is that electronic methods will not be needed or cost effect especially if through silicon vias (TSV) come into wide used. Another view is that TSVs will enable optical methods by enabling an optics layer in a multi-die stack to provide on-to and off-of chip optical methods and potentially to replace copper for some global interconnect.

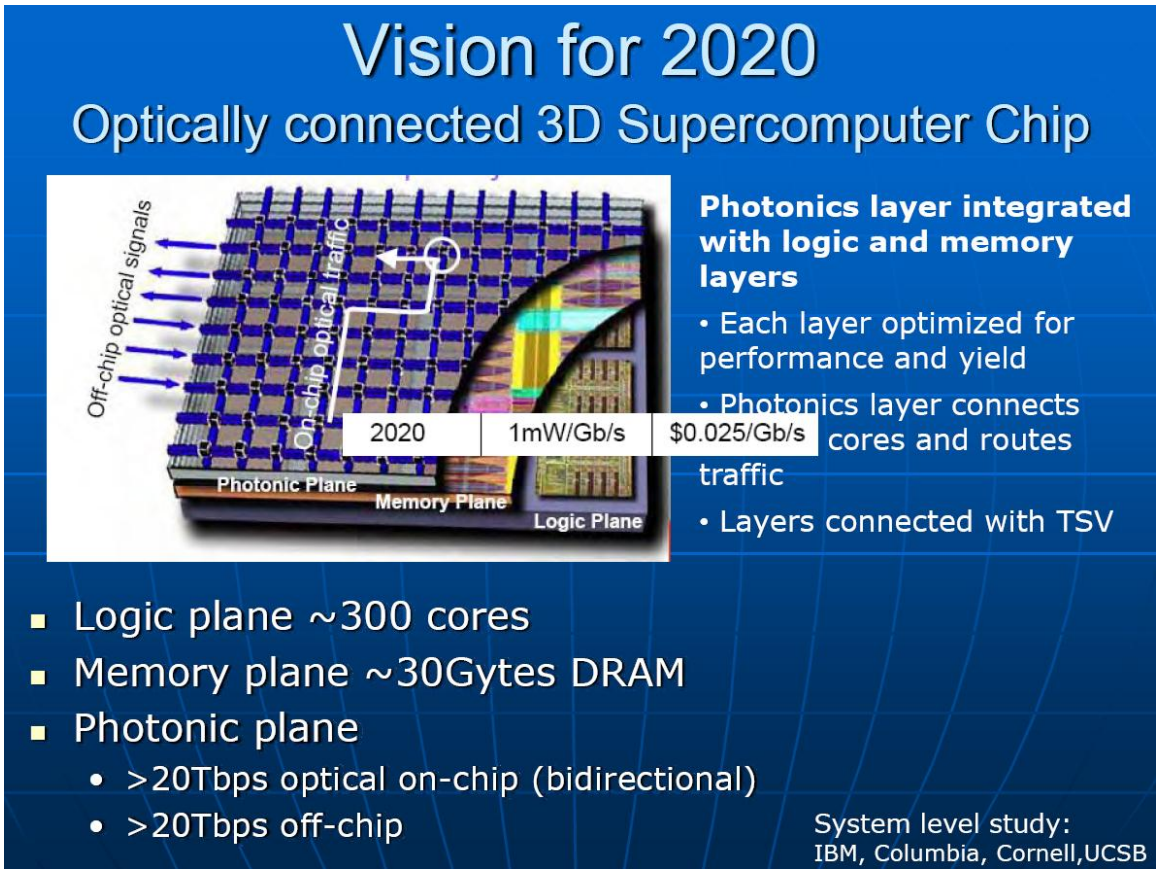


Figure AP46: A Vision of 2020 Projected Needs with On-Chip Optical Data Transmission Using TSVs and Specialized Chip Layers

SUMMARY OF OPTICAL DATA TRANSMISSION NEEDS

The data transmission applications above generally require 3 classes of optical transceivers:

1. Telecommunications transceivers for distances greater than 1 km are all single mode, generally at data rates over 1 Gb/s. The primary need is for low attenuation over 100's of kilometers that can only be achieved with single mode technology even though that technology is expensive to implement due to the tight tolerances that must be maintained over extended periods in a variety of unpredictable environments.
2. Transceivers for LANs and data transfer over distances of 1 meter to 1 km incorporate a mix of single mode and multimode methods with multi mode dominating, especially at the shorter distances. The multimode group might be split further into POF and glass fiber based methods. Much innovation is currently taking place for products in this regime. Even though multimode attenuation rates are greater than those of single mode technology, multimode is effective for this application because the component costs, assembly tolerances and field installation and maintenance costs are lower than those of single mode technology.
3. Methods to implement optical data transmission for distances less than 1 meter are not well established and are the subject of continuing discussion.

The Difficult challenges, technology requirements and potential solutions for optical packaging are presented in Tables AP22, AP23, and AP24 respectively.

PACKAGING FOR MEMS

MicroElectroMechanical Systems (MEMS) began to appear in the 1970s, initially for pressure sensors. Through the 1980's and 1990's there were many processes developed and a wide variety of MEMS devices including pressure sensors, microphones, accelerometers, ink jet printers, and eventually bio-MEMS devices. (see MEMS chapter)

MEMs devices are packaged in an unusually wide variety of ways due to the great variation in requirements. These requirements, and the resulting package solutions, go well beyond those of microelectronic packaging and result in an unusual variety of packages.

Examples include MEMs packages for the following:

- Devices, such as transmit/receive switches, must exclude moisture to prevent deterioration or corrosion and might require an inert atmosphere to remain stable
- Pressure sensors must be open to atmospheric pressure but not be susceptible to moisture damage
- Optical devices, such as camera modules, must exclude particles, must not have organics that can condense on optical surfaces over time, require optical windows and must maintain optical chain alignment over the product life.
- Devices requiring controlled atmosphere; vacuum, inert gas, etc.
- Devices that analyze fluids require containment of those liquids and must not leak
- Devices requiring ESD protection greater than that required by CMOS devices

The commercial success of many of MEMS devices was limited by the lack of robust packaging technology. Initially, the typical approach to MEMS packaging was to use the technologies that had been developed for integrated circuits and other electronic devices. This ignored the critical differences between these MEMS devices and solid state electronics resulting in packaging solutions that were not reliable and not suitable for the many use case environments such as automotive and consumer electronics.

One key technology used to reduce cost and improve performance of MEMS devices is the integration of MEMS with standard semiconductor devices which provide drive, control, and signal processing functions in a single package. This approach enables increased integration and reduction in cost. This may be enabled for many MEMS device types through a low cost wafer level package which can provide cavities. Technologies which enable the decoupling of package stress through the bump or die attach to the MEMS structure are also a critical challenge for MEMS in wafer level packages.

The approach consisting to introduce the cap at the wafer level (called Wafer Level Caps) is today in production. This technique requires further steps (wire bonding, overmolding, BGA). WLC caps are done for absolute pressure sensors, inertial sensors or capacitive sensors. Thin film encapsulation at the wafer level scale could be employed for RF MEMS and inertial MEMS (no contact with environment, specific pressure on cavity). Bonding technologies are developed with intermediate layer (glass frit, adhesive, metal) or without intermediate layer (anodic, direct or fusion bonding). The main technical challenge on WLC is to shift high vacuum and hermetic packaging for resonators and accelerometers sensors in order to increase the sensibility.

Wafer level packaging approach where the wafer encapsulation is doing with interconnections and bumps. The developments for WLP MEMS focus on developing capping technologies with through silicon vias, redistributive die layers and bumping steps. It's clearly the way to the 3D integration. Wafer level packaging has just starting in production last year for inertial MEMS and Si microphones.

These differences that presented difficult challenges for packaging included:

- Mechanical fragility of the unpackaged devices
- Stress management, particularly for sensors
- Access to the environment outside the package (microphones, pressure sensors, microfluidics, etc.)
  - Acoustical signals
  - Light input for sensors and light output for digital light processing
  - Liquids (printers and pressure sensors)
- Protection of package contents from
  - Mechanical shock
  - Vibration
  - Electromagnetic interference

  - Chemically harsh environments
  - Light reaching the interior of the package
- Thermal management, particularly in SiP packages with component
  - "hot spots"

Several MEMS devices are now manufactured in volume and the packaging requirements are the limiting cost factor for most of them. Packaging costs account for between 50 and 80% of the cost of typical MEMS devices. The Roadmap does not yet address MEMS packaging in detail and there are no tables addressing MEMS packaging requirements in this edition of the ITRS Roadmap. The work is now underway in collaboration with the MEMS technical working group to address the Roadmap for the difficult challenges and potential solutions for MEMS packaging. The initial focus will be on a limited number of MEMS categories that are already used in high volume. They are pressure sensors, accelerometers, Microfluidics and relays.

SEMICONDUCTOR PACKAGING FOR AUTOMOTIVE APPLICATIONS

AUTOMOTIVE ELECTRONICS

The current revolution in automotive technology has been driven by two motivations; maximizing comfort and fun, and eliminating accidents and eco-hazards. The recent resource-conservation movement has promoted applications of electronics technology to improve fuel economy. Many mechanical parts have been replaced by semiconductor devices, microelectromechanical systems (MEMS) and electric motors to make vehicles safer, more comfortable and more eco-friendly. The typical number of electronic control units (ECUs), MEMS and electric motors used in a vehicle has grown to between 100 and 130 pieces today and is still rising. The downward trend in MEMS cost has also boosted the adoption of MEMS for vehicles.

These replacement of mechanical parts with electronic devices is taking place in all parts of vehicle, such as the power train including the engine, transmission and battery controls; networking including controller area network and local interconnect network; information and entertainment system including global positioning system-based navigation and mobile communication; body and security system including a cipher door lock, power window, air conditioning and intelligent beam; and safety system including predictive and proactive mechanisms, avalanche airbag safety system, stability controls and driver-face monitoring.

Consequently, the number of electrical and electronic devices used in a car has been increasing, boosting the percentage of material cost for electronics. Small cars generally spend 15% of material costs on electrical and electronic devices and consume 0.21 of a silicon wafer with a diameter of 150 mm. Luxury cars spend 28% and consume 0.48 of a wafer, and hybrid electric vehicles (HEV) spend 47% and consume as much as 0.96 of a wafer. Regulations against CO_2 emission are accelerating the move to electric motor driven vehicles and raising the consumption of silicon. The amount of silicon consumed for a vehicle is significant when compared with a typical personal computer, where today only 0.12 of a wafer is consumed.

GLOBAL WARMING

Concerns for global warming have driven European Automobile Manufacturers' Association to introduce self-regulation against CO_2 emissions, with which the Japanese and Korea Automobile Manufacturers Associations have aligned. EU set a target as low as 120 g/km as a criteria of CO_2 emission for any vehicles by 2015, a tough challenge for the vehicles solely powered by fossil fuel. Thus, a concerted effort by scientists and technologists is underway to replace or supplement fossil fuels with renewable energy sources to reduce CO_2 emissions.

Gas engines have energy efficiencies of 27% to 34% with significant dependence on the rate of revolution (RPM) whereas electric motors have energy efficiencies of 90% to 94% with less dependence on RPM. Energy efficiencies of vehicles are measured by well-to-wheel energy consumption, how much energy is consumed after mining until transformation to driving energy. Battery electric vehicles (BEVs) are the least energy-consuming vehicle on the premise of electricity generated from 29% compressed natural gas, 29% nuclear power, 25% coal, 8% petroleum, and 8% hydroelectric power (based on the status in Japan, 2009), although changes of resource mixture may change the position of the BEV.

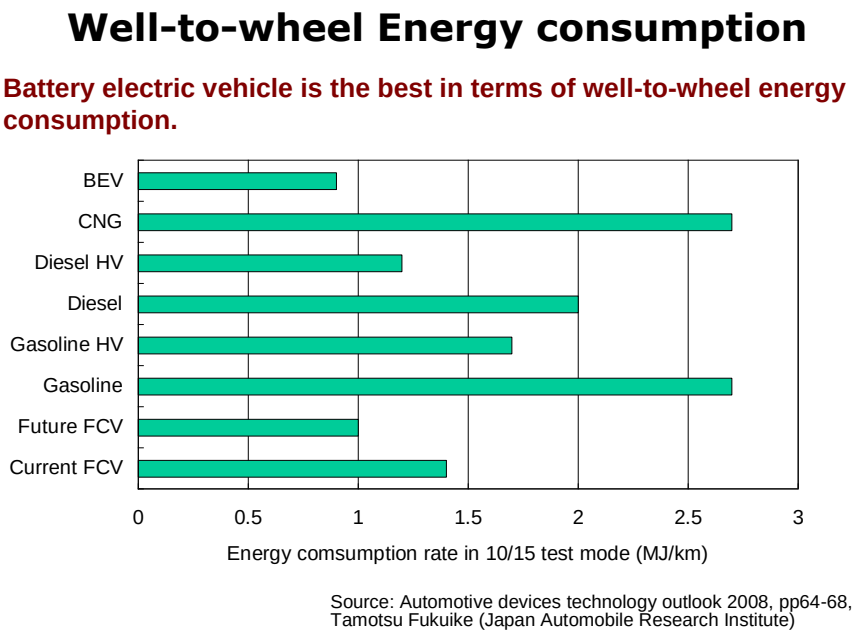


Figure AP47: Automotive Energy Consumption

One of the key advantages of fossil fuel is high energy-storage density, about 100 times higher than batteries, and the consequent long driving distances. For these reasons, BEV has been used for short-distance commuters covering 120 to 160 km. This driving-distance range is determined by the daily driving distances and how much customers are willing to spend for their cars. To increase use of BEVs across the country, it is essential to increase the energy density of the battery, deploy an ample number of charging stations and develop snap charging methods. Batteries for BEVs need higher energy densities to drive farther and longer life time even under the extreme conditions of charge and discharge cycles to reduce cost.

Beyond the range of short-distance commuters, hybrid electric vehicles (HEVs) and plug-in HEVs (PHEVs) are suitable for universal use as passenger cars. The high energy-storing density feature of fossil fuel compensates the low energy-storing density of battery and extends the driving distances. At the same time, high energy efficiencies of electric motors save energy and reduce CO_2 emission, which is especially noticeable in a low revolution rate (RPM) range, i.e. when a vehicle starts moving. Batteries for HEVs are, unlike those for BEVs, used in moderate conditions, being kept around 50% state-of-charge relying on an electric generator available anytime to prevent an excessively discharged condition. Batteries for HEV must have higher power densities to provide for heavier passenger cars with powerful driving force rather than high energy densities. As a result, the effort for battery development splits into two directions; power density oriented development for HEV applications and energy density oriented development for BEV applications.

Heavier, larger vehicles, such as buses and trucks, can afford the cost of fuel cell batteries with a compressed hydrogen cylinder to drive with the least CO_2 emission.

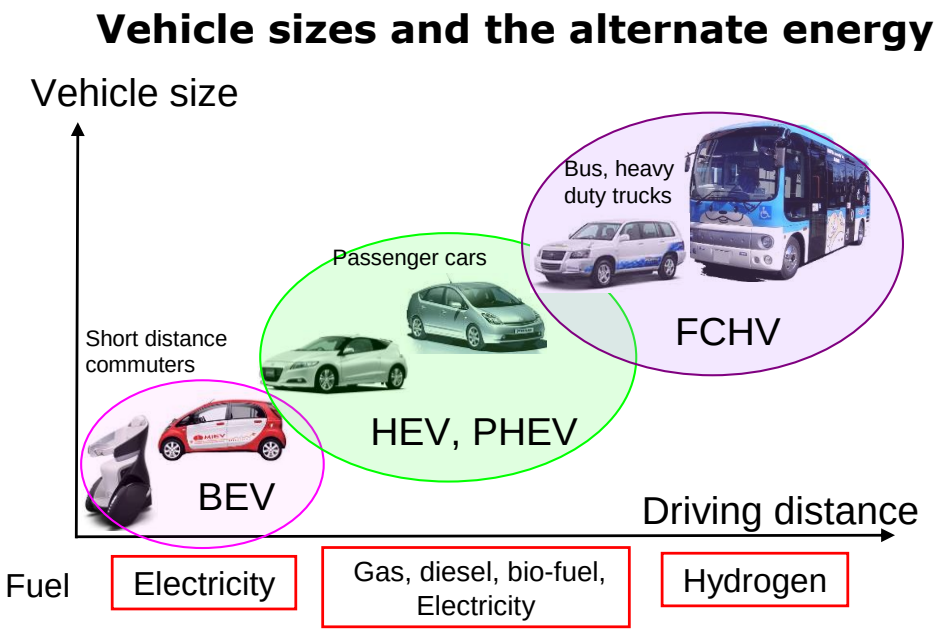


Figure AP48: Alternative Energy Vehicle Characteristics

Regarding the increasing number of ECUs, each part of vehicle is equipped with a dedicated ECU for better control, but presently the network system is growing to connect all parts over a vehicle. This trend supports the idea of consolidating these dedicated ECUs into a smaller number of commodity ECUs, along with advancing performance of ECUs. Another recent requirement for the network is transmitting large amount of video-image data from an image sensor to a processor. For such applications a fast-signal network, plastic optical cables, being immune to electric magnetic interference and affordable, are expected to replace heavy metal harnesses (see the optoelectronics section of this chapter). In addition to the networking in a vehicle presently, all vehicles are going to be connected in the future to form a traffic information network or "probe car" system. In such a system each interconnected vehicle functions as a sensor to collect data at its location and send it to a traffic system, such as break-activation signals for traffic congestion information, wiper operation for precipitation information, and tire-pressure sensor detections for road surface conditions. The traffic system can then broadcast driving suggestions for approaching road and traffic conditions.

Although a quantitative roadmap for automotive electronics is not easy to describe, collecting information from various sources and the analysis of that information led to the table below. Key indexes include gas mileage and performance of power devices, batteries, capacitor packs, electric motors, networks, sensors and ECUs. Better gas mileage is a basic requirement for vehicles to reduce CO_2 emission. Once gas engines hit the theoretical limit of gas mileage, HEVs and BEVs will be essential to continue support for the requirement to increase mileage.

Roadmap of automotive electronics

Category	Characteristics	Unit	2010	2012	2014	2016	2018	2020
Mileage	Medium car at JC08 mode	km/litter	15.5	16	16.5	17	17.5	18
Power device	Inverter power density	W/cm3	2	6	10	16	23	30
	Specific on-resistance at breakdown voltage of 1.2kV	mΩcm2 @1.2kV	40 MOSFET IGBT	25 MOSFET IGBT	5 SiC/GaN	4 SiC/ GaN	3 SiC/ GaN	3 SiC/GaN
	Drain current density	A/cm2	200	300	500	500	500	600
	Die size Si SiC/GaN	mm sq.	144 -	169 -	169 36	169 49	196 64	196 81
Battery for HEV (high power)	Energy density	Wh/kg	60	80	100	110	120	130
	Power density	kW/kg	2.8	3.4	3.8	4.2	4.4	4.5
Battery for BEV (High energy)	Energy density	Wh/kg	100	150	200	230	240	250
	Power density	kW/kg	1	1.2	1.3	1.4	1.45	1.5
Capacitor	**Capacity of capacitor pack**	F	170	200	220	234	247	260
Motor	**power**	kW	60	62	62	62	62	62
Network	Power train, body (CAN→Flex Ray)	Mbps	10	10	10	10	10	10
	Media, information	Mbps	50	150	200	220	240	262
Sensor	Number of sensors	pcs	125	130	135	138	146	150
ECU	Number of ECUs	pcs	130	140	140	130	110	100

Figure AP49: Roadmap of Automotive Electronics

PACKAGING TECHNOLOGY DEVELOPMENT

From the roadmap of automotive electronics above, the requirements for semiconductor packages are elicited for each part (See Figure 50 below). Main requirements include small footprint, high-temperature durability, low electrical resistivity, low thermal resistivity, effective cooling systems, EMI immunity, higher data rate, and system integration of sensors, processors and actuators.

Requirements to packages for vehicles

Category	Trend	Requirements to packages
Power train - Combustion	•ECU-built in engine •Fuel-saving vehicle management	•High-temperature durable packaging
Power train -Motor	•High power, fast switching devices •Intelligent battery management:	•Lower Ron •Low Rth, cooling system •Management chip built-in cell
Network	•X-by-wire; FlexRay (10Mbps) •Longer harness (50km now) •Reducing number of MCUs by networking •Plastic optical fiber	•Integration with network chip •Low impedance •EM immunity design •Higher-pin count packages •Smaller, cheaper EO devices
Information/ entertainment	•Probe-car infrastructure •Traffic information infrastructure	•Higher data rate •Multiple communication path to outside sources
Body and security	•Integration of MEMS sensor, actuator, interface chip, etc.	•Inverter-embedded motor •Integration
Safety	•Sensors and real-time processing •Monitoring a driver and lanes •Man-machine interface to inform the risk to the driver •Predictive safety mechanism	•module self-generating electricity •High speed package •mm-wave devices •Sensor/CPU/actuator integrated module

Figure AP50: Requirements to Packages for Vehicles

For body applications, only niche spaces are available for electronic devices, therefore packages should have small footprints with high board-level reliability. Low cost small packages such as QFNs with enhanced board-level

reliability will be used for this need. Area-array QFNs, offering larger pin counts, are also under evaluation as a potential solution to meet the requirements of manufacturability and reliability. Side-by-side placement of die has been used for automotive SiPs, but the demand for smaller footprints will lead the SiP to 3D configurations in the future. Thus, failure analysis methodology for 3D configurations must be established to facilitate the application of 3D packaging in a vehicle.

For a conventional gas engine, mounting an ECU directly on the engine is an attracting solution to reduce space and the number of harnesses. The ECU must be durable at extreme-temperature excursions and vibrations generated by the engine. The temperature attached to the engine is said 155°C and is projected to grow 170°C in 2017; the corresponding junction temperature is 175°C now and will be 200°C in 2017. Package materials, wire bonding materials, and solder joint reliability have been reviewed and developed to withstand such harsh conditions. Traditional pad metallization of a die has been Al, which forms Au-Al intermetallic compound (IMC) by bonding Au wires. Exposing ECUs at higher temperature such as 175°C accelerates the growth of IMC to cause Kirkendall voids, which often result in open failures in the market. To impede the IMC growth, over-pad metallization (OPM) has been developed and applied to the devices for high temperature applications. Cu wire bonding on Al pads is expected to be the useful means to eliminate OPM and cut its manufacturing cost. Qualification and adoption of Cu wire bonding for automotive applications may need at least two more years. Key parameters for automotive electronics are contained in Table AP25.

Table AP25: Key Parameters for Automotive Electronics

The HEV also needs more powerful inverters to provide higher power for driving the electric motor. Electric current through power devices generates heat in proportion to the conduction loss. The heat must be dissipated outside package mainly via die-bond material that has mostly been Pb-rich solder featuring high thermal conductance and ductility. This provides a means to compensate for the mismatch of coefficient of temperature expansion (CTEs) between a semiconductor die and the die-bond base during extreme power cycles. Replacing Pb-rich solder with Pb-free material with compatible properties and cost is under evaluation but also a difficult challenge.

Primary requirements for power devices are higher blocking voltages and lower on-resistances. Introduction of wide-band gap semiconductors including SiC and GaN have made significant progress in these properties. Experimental results demonstrated that SiC-MOSFET was functional at the junction temperature of 300°C, although the existing package material and surrounding organic materials could hardly withstand such a temperature.

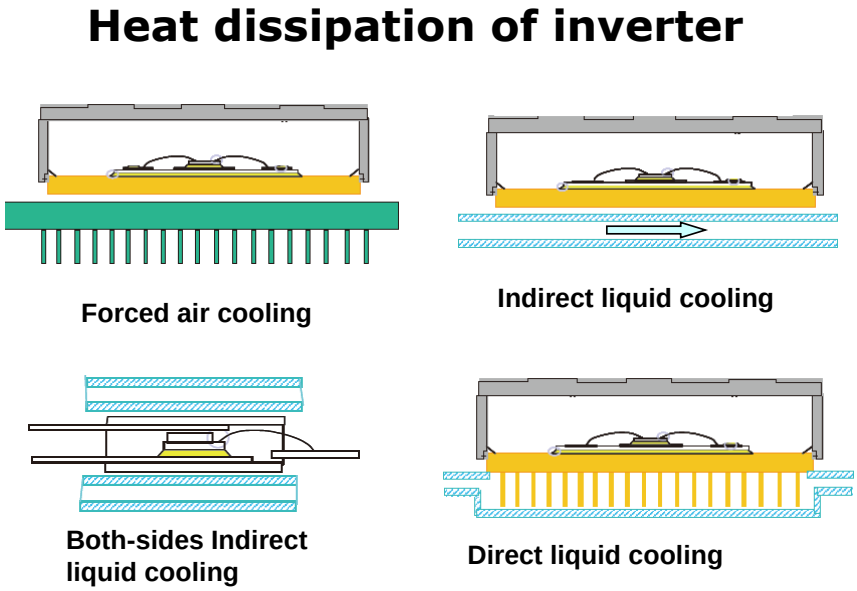


Figure AP51: Thermal Management for the Inverter Electronics

In addition to the thermal challenges, interconnection resistance to the device must be lowered to the hundreds of micro-ohms level to be aligned with the low on-resistance of SiC and GaN. Al/Cu ribbon bonding and Cu clips are currently used for low electric resistance interconnection. Extremely low resistance interconnection configuration is achieved by having solderable metallization on both top and bottom surfaces of the die which can be "sandwiched" by Cu plates with solder to form terminals.

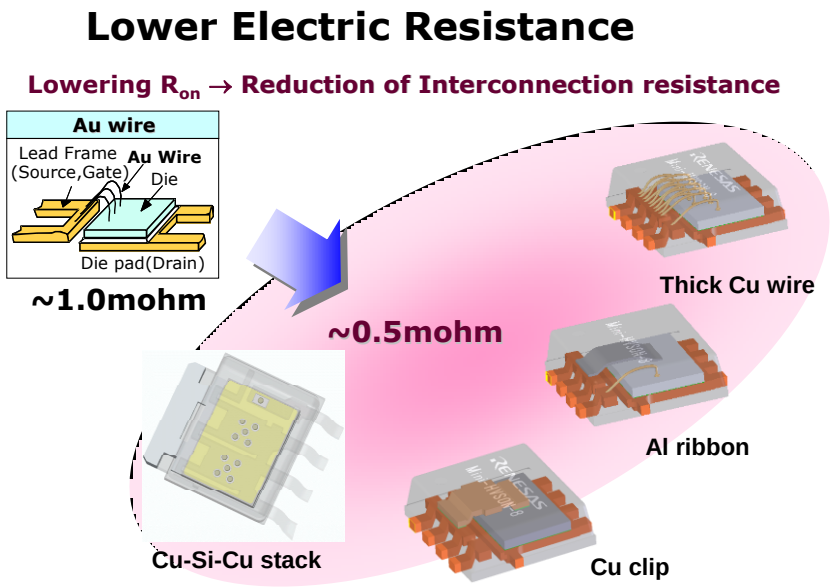


Figure AP52: Techniques for Reducing Interconnect Resistance in Automotive Electronics

For safety purposes, capturing images of traffic lanes, other cars and the driver's face, processing these image data and actuating an alarm to the driver, if needed, has been developed. Relatively high speed, high pin count packages must be used to support the required real-time processing performance.

Man-machine interfaces to inform the driver of potential risks will also be an important part of future safety features—it should not impede driving but make sure to inform the drivers. Device technologies and their packaging must provide the solutions for such risk preventative methods as well.

MEDICAL AND BIO CHIP PACKAGING

The requirements of medical electronics are often best met with SiP solutions. This is particularly true for implantable and wearable devices such as biosensors, hearing aids, pacemakers, implantable cardioverter defibrillators and similar products. Additional implantable electronic and electromechanical systems are being developed and qualified at a rapid pace. The emerging applications range from drug delivery through integration of biomaterials with integrated circuits for neurostimulation. Future products will incorporate telemetry for real time data monitoring which incorporate RF circuitry and antenna structures that are biocompatible. The requirements for SiP based medical products are similar to those of SiP based products for other applications with two important exceptions. First the reliability required for medical SiP based products is at the highest possible level since a failure may be fatal for the user. Second the environmental requirements of the package have to include exposure to body fluids. There are several areas where additional development is needed for medical SiP. Among those are:

- Low power, biocompatible radios with a signal that can reliably penetrate the human body and package to reach a remote receiver. This receiver is most likely worn by the user.
- Reduced power consumption through improved interconnect
- Power scavenging from the user's body temperature (up to 30 micro Watts/cm^2) or motion (up to 10 micro Watts/cm^2) to extend battery life of implantable products. This will require research and development of biocompatible MEMS SiP components

- Biological and silicon integration such as neurons grown on silicon. This allows silicon to monitor brain waves to detect seizures and provide counteracting neurostimulus.
- Reliable interoperability of wireless telemetry for medical devices in a world where RF devices operating across a number of frequencies have become ubiquitous.

One common method used in biomedical devices is to illuminate a sample with a suitable light source, then look for the presence, absence, or difference in intensity between two or more wavelengths with photo detectors that may require narrow band optical filters.

Many of the biomedical devices incorporating this sensor concept are disposable products made to detect pregnancy, glucose levels, blood oxygen levels, CO or NOx levels in the air, etc. Thus, they must be rugged, small, required minimal amounts of power to operate on batteries and be manufactured for low cost.

The packaging issues with these products are:

- Mechanical design, especially of the optical elements, to
- ensure optical alignment is achieved initially
- ensure alignment is retained for the life of the product
- protect the optical chain integrity over the lifetime of the device
- Materials selection, especially adhesives
- Protection of the optical system and related electronics from external light and EMI effects
- Protection of the device from the environment including from fluids that are samples either to be evaluated or used in the detection process.
- Selection of the processes and assembly methods for the optical alignment.

SOLAR CELL PACKAGING

The rapid growth of the solar power has generated a need to address the unique packaging requirements for packaging solar cells and solar cell arrays. Solar cell modules face temperature extremes and must have a very long life compared to almost any other packaging requirement. The current state of the art for the photovoltaic modules used in solar cell arrays is:

- Semiconductor thickness 180 µm
- Soldered with high-throughput tabber-stringer
- Vacuum lamination
- EVA as encapsulant
- Guaranteed lifetime of 25 years

The continued expansion of solar power and the changes anticipated in the solar cells will require focus on additional parameters to meet the packaging requirements. Table AP26 presents the key parameters for packaging of multiple-sun solar cells. These new requirements include:

- Low-stress interconnection for very thin solar cells (between 100 and 150 µm thick)
- High throughput lamination technology
- Pb-free soldering solutions
- 30 years lifetime
- Design for easy recycling at end of life

Table AP26: Multiple-Sun Photovoltaic Cell Packaging Issues

9. ADVANCED PACKAGING PROCESSES

SCOPE

The consumer driven market demand for products that are smaller, higher performance, lighter weight and have lower power requirements cannot be met without new materials and processes for packaging the devices used in these products. The innovations in processing include embedded devices (both active and passive), through silicon vias, wafer thinning as well as new methods of attaching the components of the package and the package contents to each other. This section addresses some of the most important of these emerging processes for packaging.

EMBEDDED AND INTEGRATED ACTIVE AND PASSIVE DEVICES

Integrated passive devices (IPD) are subcomponents, which exclusively contain passive components. They contain all three types of passives (R, L, and C) as well as only two or one type or any combination. The elements can be connected to each other in order to realize certain network, matching or filter functions or stand for their own to realize only single resistive, inductive, or capacitive functions.

The introduction of new materials like thin oxides or filled polymers as dielectric extends the value range for capacitors to maximum values in the micro farad range. Besides standard redistribution wiring systems it is also possible to realize ground planes and transmission lines to create impedance controlled RF-signal transmission.

The use of wafer level thin film processes (polymer-metal-oxide) technology offers the possibility to manufacture application specific WL-IPDs with passives in the following value ranges:

- Resistors: 10 Ohm–150 kOhm (e.g., NiCr 100 Ohm/sq; TaN 25 Ohm/sq.)
- Inductors: 1 nH–80 nH (Q: 30–150)
- Capacitors: (3–6) pF/ mm² (er=2.65, e.g., polymer BCB)
- Capacitors: (1–3) nF/ mm²(er=23, e.g., Ta_2O_5)

With this value range nearly 70 % of capacitors and 95% of resistors and nearly all inductors of the required passive elements for a wireless cellular can be realized, which demonstrate the large potential for system miniaturization.

WL-IPDs are designed as flip chip mountable as well as wire bondable components by using different thin film substrates like silicon, alumina, or glass. Figure AP53 shows an example of an integrated passive device as a CSP with 2X low-pass filter with 3X inductors 3.9 nH, 2X capacitors 1.8 pF realized with a multi-layer polymer-metal (Cu) redistribution layer on Pyrex.

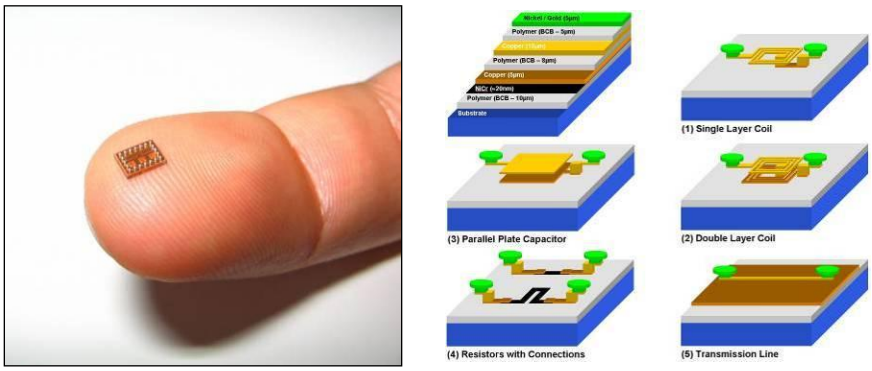


Figure AP53: CSP with Integrated Passive Devices and Thin-film Build-Up Passive Elements

Today's bottleneck for the realization of integrated passive devices are capacitors, In combination with high aspect ratio deep reactive ion etching (DRI) in silicon deep trench capacitors with an value of (20–30 nF /cm^2) can be realized. This very promising technology is currently in development by several companies with focus to wafer level System in Package approaches. With respect to cost and form factor, larger passive devices are implemented as SMD devices on top or embedded into substrates for System in Package approaches.

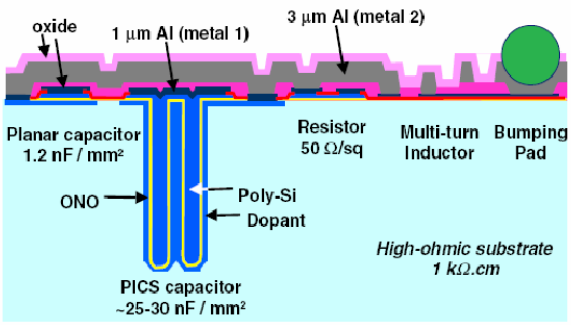


Figure AP54: PICS Substrate with High Density "Trench" MOS Capacitors, Planar MIM, Multi-Turn Inductors, and Poly-Si Resistors

APPLICATIONS FOR EMBEDDED ACTIVE AND PASSIVE DEVICES

Current applications on embedded active devices are cellular phone related products e.g., TV tuner, finger print ID sensor. Cellular phone and semiconductor manufacturers are expecting next generation products on embedded active devices for communication modules e.g., GPS and wireless LAN with passive devices on surface which use the space "liberated" by embedding active devices. In addition, power supply units with embedded actives and surface mounted passives have also strong demands from market place. Also, image sensors such as CMOS sensor and strobe light for cellular phone camera will adopt embedded active devices with surface mount passives for reducing form factor. In the very near future, ASICs and graphic processor with stacked memory devices as well as DSC will use embedded active and passive devices.

At this time, two different types of active device are common for embedded applications. One is wafer level package with thinned embedded active devices without copper post for enhanced mechanical strength which are directly interconnected by thin film RDLs, and the other is flip chip with stud bump or copper posts embedded in organic laminates substrates. Figure AP55 represents a schematic overview.

For the economical production of embedded active and passive devices in organic substrates, a chip bonder compatible with printed circuit board work panel size is required. The major issues for embedded technologies are test, yield and quality assurance. Test standards and the implementation of a responsible supply chain are needed for market adoption of embedded active and passive devices.

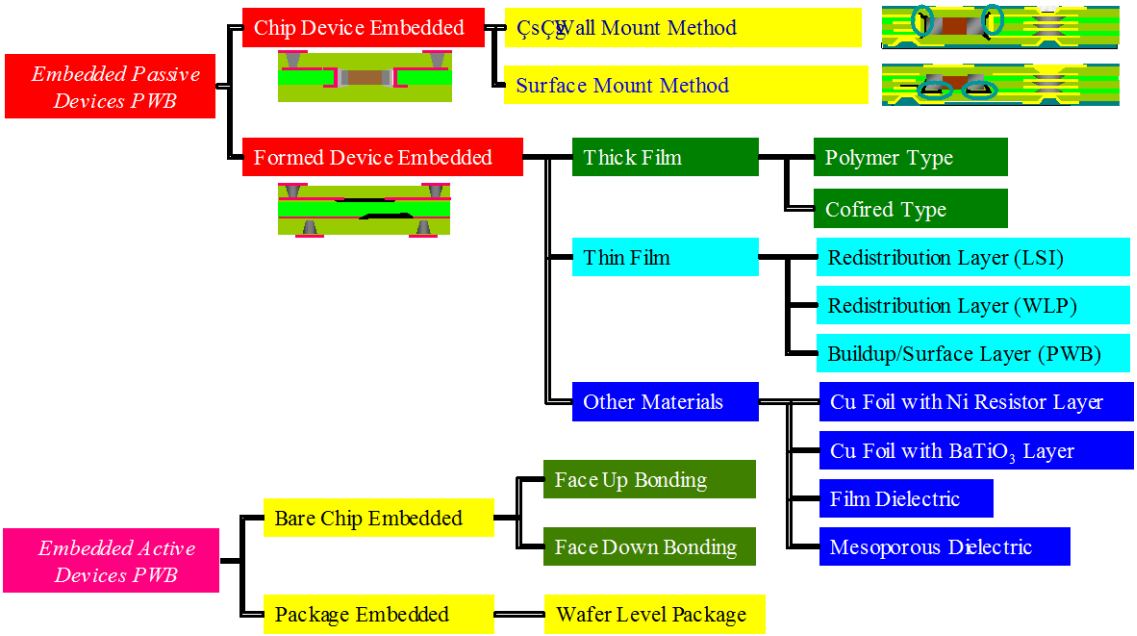


Figure AP55: Overview of Embedded Active Devices and Passive Devices

WAFER THINNING AND SINGULATION

Wafer thinning is a key enabler for thin packages, stacked die packages and, most recently, packages with through silicon vias (TSV). While wafer singulation typically follows wafer thinning, several new process combinations are possible to accommodate packages which have multiple die and wafer based processes. These are described in Figures AP56, AP57 and AP58 below.

WAFER THINNING

In 2009, thinned wafers of 50–75 µm are common. The roadmap for wafer thinning is shown in Tables AP27 and AP28. Wafers are typically processed by mechanical grinding with a resin bonded abrasive wheel, followed by chemical mechanical polishing (CMP). Dry and wet etch methods are also available, but are less economical. Prototypes of 5 µm thickness, after careful processing, have been reported, but the infrastructure for such thin wafers is limited. The major technical challenge in wafer thinning is to retain wafer and die strength. Two prominent failure mechanisms and their mitigation are described below.

Table AP27: Thinned Silicon Wafer Thickness

Table AP28: Challenges and Potential Solutions in Thinning Si Wafers

First, mechanical grinding generates defects on the wafer surface. These defects may propagate as cracks during wafer handling and assembly operations, possibly leading to failures after assembly and environmental exposure. Stress relief by polishing, commonly by CMP, removes the defect layer and thereby strengthens the wafers.

Second, during thinning, the wafer rim progressively changes shape from a round profile to a sharp edge. Edge defects may initiate cracks during handling, leading to wafer breakage. The thinnest wafers have the sharpest edge and therefore are most susceptible to damage. New techniques have been developed to avoid edge cracking. A first technique is to cut the wafer circumference to remove the sharp edge. A second method is to grind the wafer over a region which does not include the wafer rim. The intact wafer rim supports the wafer during subsequent handling. A third method is to employ a carrier which supports the wafer though the processing after thinning, such as in the double sided processing required for TSV. A fourth option is to perform dicing before grinding (DBG), described as a singulation technique below.

Bumped wafers are thinned by mechanical grinding. The wafer is partially immersed in an adhesive material during processing. Dry etching may be used to remove top layer defect. As the bump side of the wafer is not protected, however, CMP is typically not used. Alternatively, wafers may be bumped after thinning by using special handling equipment or a sacrificial carrier.

WAFER SINGULATION

Sawing by a resin bonded diamond blade is the most common singulation method. However, the blade sawing process creates defects at the die edge. So called *chip-outs* may propagate as cracks during assembly and environmental exposure and may result in full die cracks. Chip-outs become more severe with thinner wafers and narrow scribe lines, and are typically reduced by optimizing the dicing blade and process parameter. Nevertheless, a residual amount of defects persist, especially for low-κ wafer fabrication technologies. To arrest crack propagation, wafers are designed with seal rings at the die periphery. In recent years, laser based techniques provide a way to significantly reduce chip-outs. The two most common techniques are full laser cutting and laser grooving on both side of the scribe line which is followed by a mechanical saw cut to remove the remaining material.

Dicing before grinding (DBG) is another way to reduce wafer defects while mitigating wafer edge and surface defects in thin wafers. In DBG, the wafer is "pre-cut" by either etch or sawing, followed by wafer thinning to complete the wafer singulation process. Several process options are reported elsewhere [SiP Whitepaper p. 98, Shinya Taku, et al. ECTC 2006].

Recently, a new technique has been developed where a laser beam is focused at the wafer center, rather than the surface as in laser grooving. The localized heat converts the crystalline silicon at the wafer center into polycrystalline silicon which has more volume and, in turn, creates a localized compressive stress. The silicon is then cleaved by stretching the wafer film frame, leading to a clear separation into individual dice along the laser scan lines. The technique has been shown to reproducibly singulate dice with scribe lines below 16 µm, leading to very optically smooth surfaces without chip-out. By contrast, the scribe line region in conventional is typically 60–100 µm in width. The proposed applications for the new technique for 1) die where very little or no chip-out is

allowed, such as automotive, wafer level packaging, or wafer with low-κ dielectric which are susceptible to chip out, 2) small die where a very narrow scribe line will allow a greater number of dice per wafer and 3) wafers with multiple die of different size or non-rectangular die shapes.

PROCESS FLOWS ASSOCIATED WITH WAFER THINNING AND SINGULATION

As noted above, there is additional complexity to the process flows for packages with multiple die (System-in-Package) and wafer based processing. Figures AP56–58 divide these process flows into three categories and show examples of the flows for wafer thinning and singulation in the context of each category. For simplicity, the use of a sacrificial carrier(s) is not shown explicitly in the figures. The three categories are:

1. Single die flows – process of thinning and singulation for a single die; may have multiple die in a package by stacking single die or side-by-side format.
2. Heterogeneous die flows/die on wafer – one or more dice are thinned and singulated before bonding to a thinned wafer which is, in turn, singulated.
3. Homogeneous die flows/wafer bonding – thinning and stacking of wafers prior to singulation.

Following the final singulation, the single die or die stacks are processed further using common interconnection technologies such as wirebond, flip chip and ball attach.

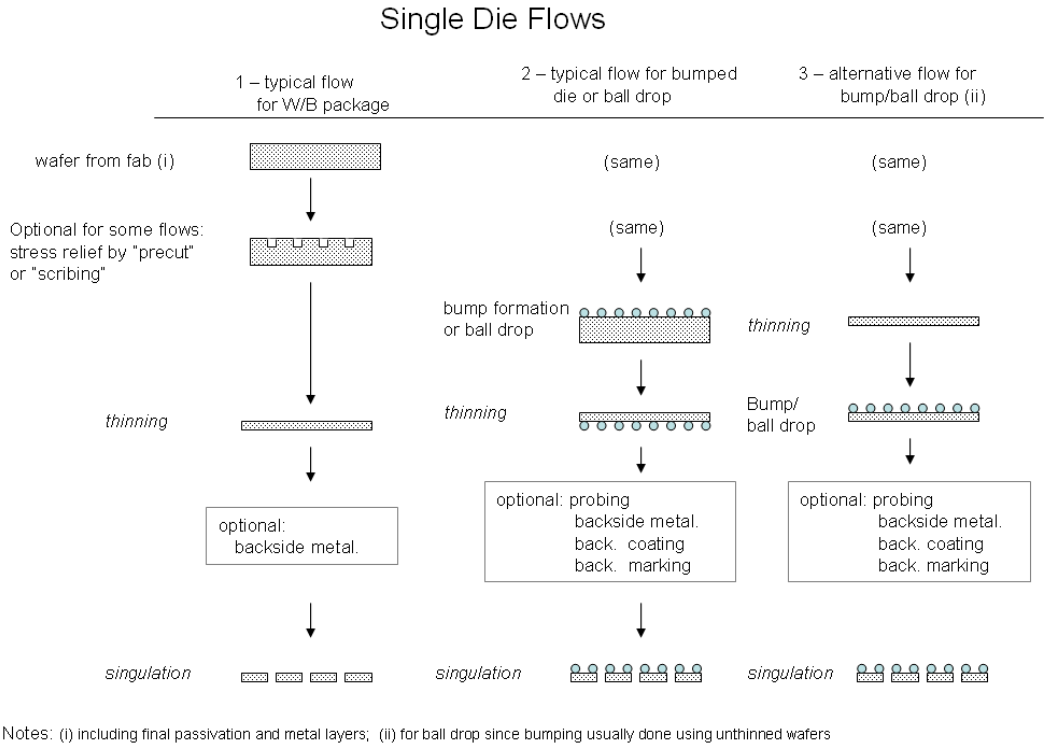


Figure AP56: Extract of Thinning and Singulation Process Flow for Single Die Package

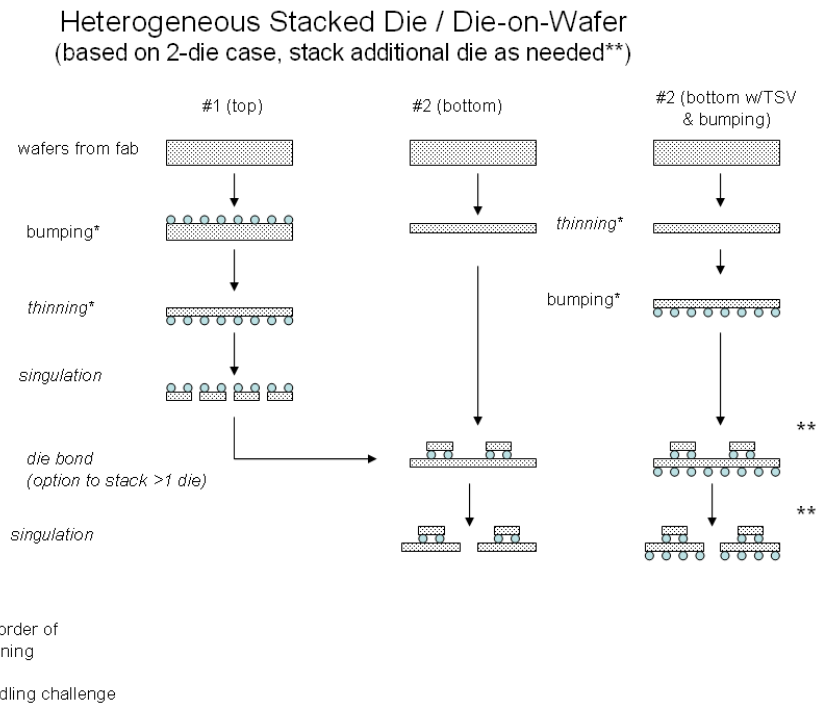


Figure AP57: Extract of Thinning and Singulation Process Flow for Packages Using Die on Wafer Process

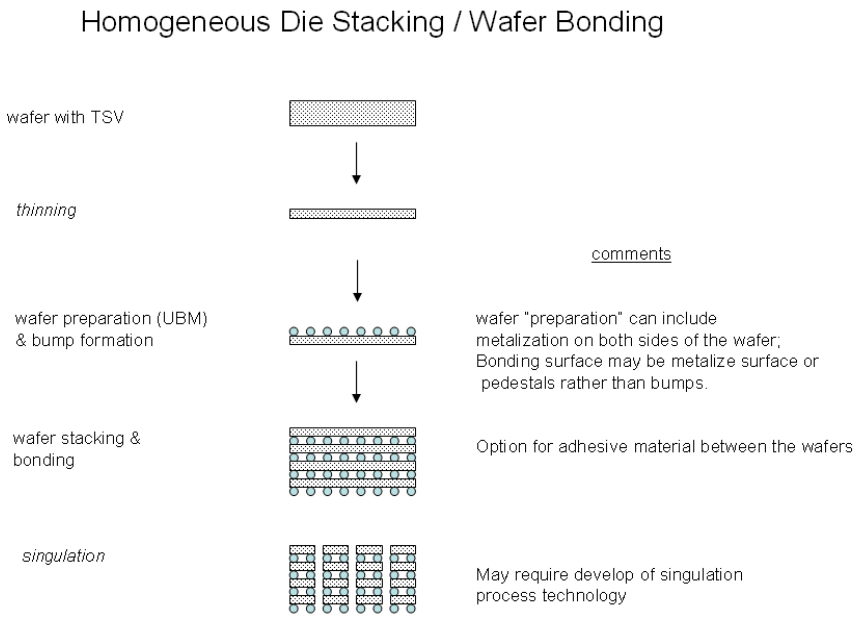


Figure AP58: Extract of Thinning and Singulation Process Flow for Packages Using Bonded Wafers

10. PACKAGING MATERIALS REQUIREMENTS

SCOPE

Packaging materials are at the heart of Assembly and Packaging Technology. Packaging material contributes significantly to the packaged device performance, reliability, and workability as well as to the total cost of the package. With the advent of the "More Moore" and "More than Moore" initiatives, the challenges for packaging materials have broadened from requirements for traditional packages for future generations of devices as well as for new package types such as the SiP package families, wafer level packaging, IPDs, TSVs and for applications in RF, MEMs, and optoelectronics.

The Assembly and Packaging industry has been in the midst of a sea change in materials. The bill of materials in today's packages may not be the same tomorrow. Furthermore, these changes are expected to accelerate in pace and scope in the coming years. Much of the near-term new materials introduction is driven by environmental regulatory compliance requirements including Pb-Free and RoHS compliance (European Union Directive for Reduction of Hazardous Substances). The migration to "green" materials that are lead-free and halogen-free compatible are in full swing. Industry has been adopting "green" materials for the new products packages when they transition to new packaging materials to meet RoHS requirements. Materials for the traditional wire bond and flip chip packages including molding compound, die attach materials, underfill materials, thermal interface materials (TIM), and package substrates, will have to be improved to meet lead-free, halogen-free, and low-κ/ULK requirements.

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly advanced next generation devices. While wirebond and flip chip remain the two basic interconnect methodologies, the introduction of low-κ dielectric materials, increasing power density and hand held consumer products, imposes additional requirements to traditional materials applications. For example, with the mechanically weak low-κ and the still weaker ultra low-κ dielectrics in the device, comprehensive design of

underfill materials properties compatible with the bump materials properties are crucial in addressing the risk for interface stress damage to the dielectric layer. With the increasing thermal output and uneven temperature distribution of many IC device applications, thermal interface materials represent an important opportunity for innovation. The drive for miniaturization through die stacking, package stacking, and low profile packages requires improvements in molding compounds, underfill materials and die attach materials originally developed for traditional single chip packages.

The developments of potential solutions, such as SiP, wafer level packaging, embedded die and passives, and TSV, will call for innovations in design of materials and materials processing innovations beyond what is available today. Wafer level packaging will require materials with improved or different properties as it evolves to meet new packaging applications. Different metallization systems for both redistribution traces and under bump metallization, as well as new dielectric polymers, are needed to meet the ever changing reliability requirements for portable electronic devices. The development of fan-out WLP and embedded passives/actives will require new low-temperature embedding polymers and low-temperature cure redistribution layer polymers. TSVs will benefit from new dielectric insulators and conductive via filling media for improved low cost manufacturability. Integrated passive devices (IPDs) will also require better materials, with improved electrical properties, for both resistive and capacitive devices. The difficult materials challenges are summarized in Table AP19.

11. ENVIRONMENTAL ISSUES

Environmental issues are gaining more attention with expanding restraint on the use of chemical substances in legislation and additional regulatory actions as new materials are developed and the health and safety issues associated with materials currently in use are better understood. The environmental protection laws originated in Europe have been affecting the legislation in other industry countries, thus resulting in the establishment of similar laws in these countries (see Figure AP59). These laws have constrained packaging engineers from adopting restricted substances. One of leading actions in electronics industry has been lead-free conversion and halogen free packages. Today, most of packages used in consumer market do not use lead-contained materials except die-attach materials for power devices and some flip-chip bumps. The deployment of lead-free material in consumer market is now affecting other market segments for fear of phasing out conventional lead-contained materials and possible increases in cost. Even heavy duty-industry sectors have started to find a replacement for the conventional lead-contained devices. As in the lead-free requirement, halogen-free packages would require halogen-free retardants for molding resin or solder resist for a package substrate.

The regulation, REACH, gives greater responsibility to industry to manage the risks from chemicals and to provide safety information for these substances. Manufacturers and importers will be required to gather information on the properties of their chemical substances, which will allow their safe handling, and to register the information in a central database. It requires complete chemical database on the manufacturer's side through the entire supply chain from the raw material to the final products. A leading example of the activities that integrate the chemical information through supply chains is "Joint Article Management Promotion Consortium (JAMP)" in Japan, which attempts to manage seamless information transfer of restricted substances through whole global supply chain and promote cross-industrial activities to facilitate disclosure and conveyance of information on chemicals contained in the products. This type of consortium will be helpful globally as industry works to comply with the evolving tighter environmental regulations.

There are several existing environmental regulations as listed below and the introduction of new materials is likely to result in new regulations. The current consideration of additional regulations for nano-materials could be a major impediment to the incorporation of these new into electronic packaging.

ELV	Directive on end-of life vehicles
RoHS	Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment
WEEE	Directive on waste electrical and electronic equipment
EuP	Directive on the eco-design of Energy-using Products
REACH	Registration, Evaluation and Authorization of Chemicals
SB20	Electronic Waste Recycling Act in California, US
J-Moss	The marking of presence of the specific chemical substances for electrical and electronic equipment

Figure AP59: Current Environmental Regulations

12. PACKAGING GAPS AND TECHNOLOGY NEEDS

The pace of change demands addressing a continuous flow of unmet technology needs that result in "gaps" in our capability that must be addressed. In a joint effort with INEMI we have initiated an activity to identify these gaps and update the list annually. The summary of this work is presented in Table AP29. The table is arranged with a near term horizon of 5 years and a longer term section. The objective is to focus the investment of the industry on these areas to close the gaps before they impact the pace of progress.

Table AP29: Packaging/Gaps/Technology Needs Summary

13. INDUSTRY CONSORTIA

The pace of progress in Assembly and Packaging is accelerated by cooperation among industry, government and research in research and development to meet the difficult challenges. There are consortia around the world where the investments of multiple interested parties are combined to increase the resources and focus the investment. Table AP30 provides a list of Consortia and Research Institutes in Packaging Technology.

Table AP30: Consortia and Research Institutes in Packaging Technology

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