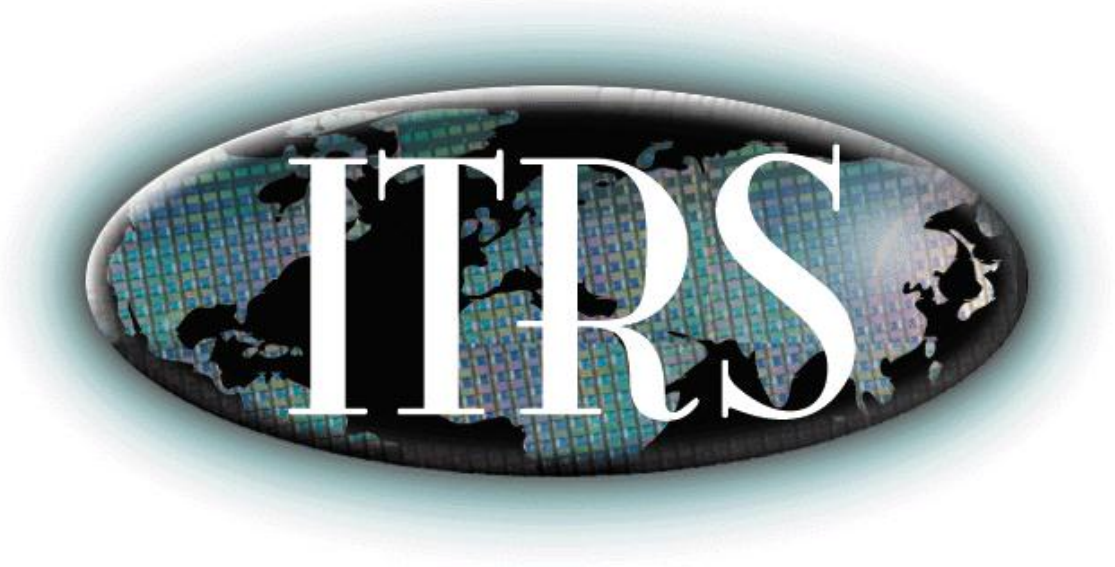

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

EMERGING RESEARCH DEVICES

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EMERGING RESEARCH DEVICES

1. SCOPE

Continued dimensional and functional scaling[1] of CMOS is driving information processing[2] technology into a broadening spectrum of new applications. Many of these applications are enabled by performance gains and/or increased complexity realized by scaling. Because dimensional scaling of CMOS eventually will approach fundamental limits, several new alternative information processing devices and microarchitectures for existing or new functions are being explored to sustain the historical integrated circuit scaling cadence and reduction of cost/function into future decades. This is driving interest in new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions (a.k.a. "More than Moore"), and new paradigms for systems architecture. This chapter, therefore, provides an ITRS perspective on emerging research device technologies and serves as a bridge between CMOS and the realm of nanoelectronics beyond the end of CMOS dimensional and equivalent functional scaling. (Material challenges related to emerging research devices are addressed in a complementary chapter entitled *Emerging Research Materials)*

An overarching goal of this chapter is to survey, assess and catalog viable new information processing devices and systems architectures for their long-range potential, technological maturity, and to identify the scientific/technological challenges gating their acceptance by the semiconductor industry as having acceptable risk for further development. A new goal is to pursue long term alternative solutions to technologies addressed in More-than-Moore (MtM) ITRS entries, currently for wireless devices and, in the future, for power devices, image sensors, etc.

This is accomplished by addressing two technology-defining domains: 1) extending the functionality of the CMOS platform via heterogeneous integration of new technologies, and 2) stimulating invention of a new information processing paradigm. The relationship between these domains is schematically illustrated in Figure ERD1. The expansion of the CMOS platform by conventional dimensional and functional scaling is often called "More Moore". The CMOS platform can be further extended by the "More-than-Moore" approach which is a new subject included in this chapter. On the other hand, new information processing devices and architectures are often called "Beyond CMOS" technologies and have been the main subjects of this chapter. The heterogeneous integration of "Beyond CMOS", as well as "More-than-Moore", into "More Moore" will extend the CMOS platform functionality to form ultimate "Extended CMOS".

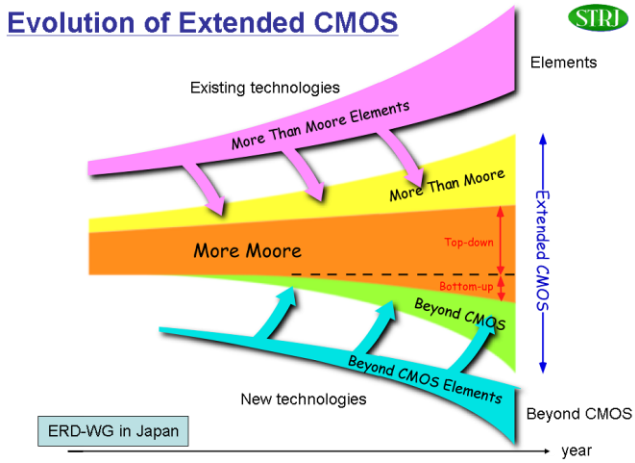


Figure ERD1 Relationship among More Moore, More-than-Moore, and Beyond CMOS.

The chapter is intended to provide an objective, informative resource for the constituent nanoelectronics communities pursuing: 1) research, 2) tool development, 3) funding support, and 4) investment, each directed to developing a new

[1] *Functional Scaling: Suppose that a system has been realized to execute a specific function in a given, currently available, technology. We say that system has been functionally scaled if the system is realized in an alternate technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost, and does not degrade in any of the other metrics.*

[2] *Information processing refers to the input, transmission, storage, manipulation or processing, and output of data. The scope of the ERD Chapter is restricted to data or information manipulation, transmission, and storage.*

information processing technology. These communities include university, research institute, and industrial research laboratories; tool suppliers; research funding agencies; and the semiconductor industry. The potential and maturity of each emerging research device and architecture technology are reviewed and assessed to identify the most important scientific and technological challenges that must be overcome for a candidate device or architecture to become a viable approach.

The scope is expanded to include a major new section on devices required for heterogeneous integration to realize a specific system function in a "More-than-Moore" application. In addition, the Memory Device Section is expanded to include two new subsections: one on Storage Class Memory (to include Solid State Drive Memory) and another on the "Select Device/Diode" required for a crossbar memory application. Finally, the "Benchmarking" subsection is expanded and moved from the Architecture Section to the Critical Assessment Section to provide a balanced assessment of these emerging new device technologies. A brief section also is included to propose a set of fundamental principles that will likely govern successful extension of information processing technology substantially beyond that attainable solely with ultimately scaled CMOS.

A section introduced in the 2009 edition that highlights "Carbon-based Nanoelectronics" as a rapidly emerging information processing technology is expanded to highlight two rapidly emerging memory technologies: Spin Transfer Torque Magnetostatic RAM (STT-MRAM), and Redox Resistive RAM. These three technologies exhibit substantial potential such that they will likely be ready for manufacture within a five – ten year period. Highlighting also suggests that a technology is an attractive candidate for accelerated development.

The chapter is divided into five sections: 1) memory devices, 2) information processing or logic devices, 3) More-than-Moore device technologies, 4) emerging research information processing architectures, and 5) a critical assessment of each technology entry. Some detail is provided for each entry regarding operation principles, advantages, technical challenges, maturity, and current and projected performance. Also included is a device and architectural focus combining emerging research devices offering specialized, unique functions as heterogeneous core processors integrated with a CMOS platform technology. This represents the nearer term focus of the chapter, with the longer term focus remaining on discovery of an alternate information processing technology to eventually replace digital CMOS.

As in previous editions, the chapter includes "transition tables." The purpose of these transition tables is twofold. The first is to track technologies that have appeared in or have been removed from the 2009 tables and so provide a very brief explanation of the reason for this change. The second is to identify technologies that are considered important but do not meet the criteria for full inclusion into the more detailed tables. These may be expected to become more or less visible in future editions of the roadmap and hence the name.

2. DIFFICULT CHALLENGES

2.1. INTRODUCTION

The semiconductor industry is facing three classes of difficult challenges related to extending integrated circuit technology to new applications and to beyond the end of CMOS dimensional scaling. One class relates to propelling CMOS beyond its ultimately density and functionality by integrating, for example, a new high speed, dense and low power memory technology onto the CMOS platform. Another class is to invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless and eventually in power devices, image sensors, etc. The third class is to extend information processing substantially beyond that attainable by CMOS using an innovative combination of new devices, interconnect and architectural approaches for extending CMOS and, eventually, inventing a new information processing platform technology. These difficult challenges, all addressing the long term period of 2018 – 2026, are presented in Table ERD1.

Table ERD1 Emerging Research Devices Difficult Challenges

Difficult Challenges – 2018– 2026	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile, and non-volatile memory technologies to replace SRAM and / or FLASH for manufacture by 2018.	SRAM and FLASH scaling in 2D will reach definite limits within the next several years (see PIDS Difficult Challenges). These limits are driving the need for new memory technologies to replace SRAM and possibly FLASH memories by 2018. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond 2018 - 2026	Develop 2nd generation new materials to replace silicon (or InGaAs, Ge) as an alternate channel and source/drain to increase the saturation velocity and to further reduce Vdd and power dissipation in MOSFETs while minimizing leakage currents for technology scaled to 2018 and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in this development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A new information processing technology must also be compatible with a systems architecture that can fully utilize the new device. A new non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for a new systems architecture. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials Reliability issues should be identified & addressed early in the technology development
Invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless/analog and eventually in power devices, MEMS, image sensors, etc.	The industry is now faced with the increasing importance of a new trend, "More than Moore" (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment.

2.2. DEVICE TECHNOLOGIES

Difficult challenges gating development of emerging research devices are divided into those related to memory technologies, those related to information processing or logic devices, and those related to heterogeneous integration of multi-functional components (a.k.a. More-than-Moore (MtM) or Functional Diversification. (Refer to Table ERD1.) One challenge is the need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with CMOS process flow scaled beyond the present limits of SRAM and FLASH. This would provide a memory device fabrication technology required for both stand-alone and embedded memory applications. The ability of an MPU to execute programs is limited by interaction between the processor and the memory, and scaling does not automatically solve this problem. The current evolutionary solution is to increase MPU cache memory, thereby increasing the floor space that SRAM occupies on an MPU chip. This trend eventually leads to a decrease of the net

information throughput. In addition to auxiliary circuitry to maintain stored data, volatility of semiconductor memory requires external storage media with slow access (e.g., magnetic hard drives, optical CD, etc.). Therefore, development of *electrically accessible non-volatile* memory with *high speed* and *high density* would initiate a revolution in computer architecture, referred to as "Storage Class Memory" or SCM. This development would provide a significant increase in information throughput beyond the traditional benefits of scaling when fully realized for nanoscale CMOS devices.

A related challenge is to sustain scaling of CMOS logic technology beyond 2018. One approach to continuing performance gains as CMOS scaling matures in the next decade is to replace the strained silicon MOSFET channel (and the source/drain) with an alternate material offering a higher potential quasi-ballistic-carrier velocity and higher mobility than strained silicon. Candidate materials include strained Ge, SiGe, a variety of III-V compound semiconductors, and graphene. Introduction of non-silicon materials into the channel and source/drain regions of an otherwise silicon MOSFET (i.e., onto a silicon substrate) is fraught with several very difficult challenges. These challenges include heterogeneous fabrication of high-quality (i.e., defect free) channel and source/drain materials on non-lattice matched silicon, minimization of band-to-band tunneling in narrow bandgap channel materials, elimination of Fermi level pinning in the channel/gate dielectric interface, and fabrication of high-κ gate dielectrics on the passivated channel materials. Additional challenges are to sustain the required reduction in leakage currents and power dissipation in these ultimately scaled CMOS gates and to introduce these new materials into the MOSFET while simultaneously minimizing the increasing variations in critical dimensions and statistical fluctuations in the channel (source/drain) doping concentrations.

The industry is now addressing the increasing importance of a new trend, "More than Moore" (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". This chapter includes for the first time significant parts of the "More-than-Moore" domain; initial coverage in 2011 will encompass wireless technologies. Traditionally, the ITRS has taken a "technology push" approach for roadmapping "More Moore", assuming the validity of Moore's law. In the absence of such a law, a different methodology will be developed and used to identify and guide roadmap efforts in the MtM-domain.

A longer-term challenge is invention and reduction to practice of a manufacturable information processing technology addressing "beyond CMOS" applications. For example, emerging research devices might be used to realize special purpose processor cores that could be integrated with multiple CMOS CPU cores to obtain performance advantages. These new special purpose cores may provide a particular system function much more efficiently than a digital CMOS block, or they may offer a uniquely new function not available in a CMOS-based approach. Solutions to this challenge beyond the end of CMOS scaling also may lead to new opportunities for such an emerging research device technology to eventually replace the CMOS gate as a new information processing primitive element. A new information processing technology must also be compatible with a systems architecture that can fully utilize the new device. A non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for a new systems architecture.

2.3. MATERIALS TECHNOLOGIES

The most difficult challenge for Emerging Research Materials is to deliver materials with controlled properties that will enable operation of emerging research devices in high density at the nanometer scale. To improve control of material properties for high density devices, research on materials synthesis must be integrated with work on new and improved metrology and modeling. These important objectives are addressed in the companion chapter entitled Emerging Research Materials.

3. NANO-INFORMATION PROCESSING TAXONOMY

Information processing to accomplish a specific system function, in general, requires several different interactive layers of technology. The objective of this section is to carefully delineate a taxonomy of these layers to further distinguish the scope of this chapter from that of the Emerging Research Materials chapter and the Design chapter.

One comprehensive top-down list of these layers begins with the required application or system function, leading to system architecture, micro- or nano-architecture, circuits, devices, and materials. As shown in Figure ERD2 below, a different bottom-up representation of this hierarchy begins with the lowest physical layer represented by a computational state variable and ends with the highest layer represented by the architecture. In this more schematic representation, focused on generic information processing at the device/circuit level, a fundamental unit of information (e.g., a bit) is represented by a computational state variable, for example, the position of a bead in the ancient Abacus calculator or the charge or voltage state of a node capacitance in CMOS logic. A device provides the physical means of representing and manipulating a computational state variable among its two or more allowed discrete states. Eventually, device concepts

may transition from simple binary switches to devices with more complex information processing functionality perhaps with multiple fan-in and fan-out. The device is a physical structure resulting from the assemblage of a variety of materials possessing certain desired properties obtained through exercising a set of fabrication processes. An important layer, therefore, encompasses the various materials and processes necessary to fabricate the required device structure, which is the domain of the ERM chapter. The data representation is how the computational state variable is encoded by the assemblage of devices to process the bits or data. Two of the most common examples of data representation are binary digital and continuous or analog signaling. This layer is within the scope of the ERD chapter. The architecture plane encompasses three subclasses of this Taxonomy: 1) nano-architecture or the physical arrangement or assemblage of devices to form higher level functional primitives to represent and execute a computational model, 2) the computational model that describes the algorithm by which information is processed using the primitives, e.g., logic, arithmetic, memory, cellular nonlinear network (CNN); and 3) the system-level architecture that describes the conceptual structure and functional behavior of the system exercising the computational model. Subclass 1) is within the scope of the ERD chapter, and subclasses 2) and 3) above are within the scope of the Design chapter.

The elements shown in the red-lined yellow boxes represent the current CMOS platform technology that is based on electronic charge as a binary computational state variable. This state variable serves as the foundation for the von Neumann computational system architecture. Analog data representation also is included in the current CMOS platform technology. The other entries grouped in these five categories summarize individual approaches that, combined in some yet to be determined highly innovative fashion, may provide a new highly scalable information processing paradigm.

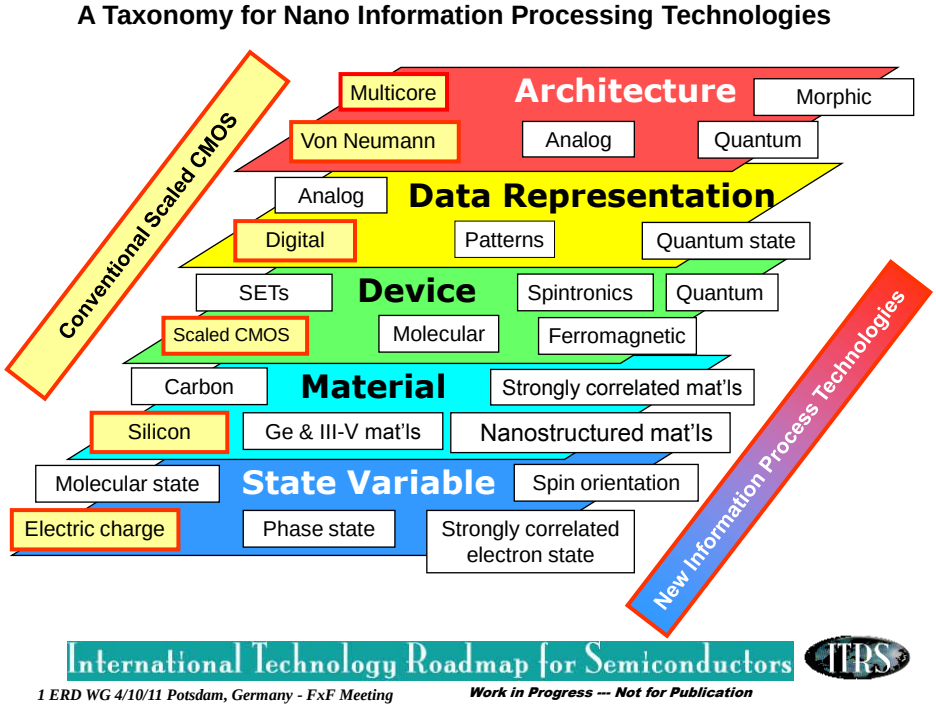


Figure ERD2 *A Taxonomy for Emerging Research Information Processing Devices (The technology entries are representative but not comprehensive.)*

4. EMERGING RESEARCH DEVICES

4.1. MEMORY TAXONOMY AND DEVICES

The emerging research memory technologies tabulated in this section are a representative sample of published research efforts (circa 2009 – 2011) selected to describe some attractive alternative approaches[3]. In addition, the scope of this section is expanded to include two new subsections: one addressing the "Select Device" required for a crossbar memory application and another treating "Storage Class Memory" (to include Solid State Drive Memory).

Table ERD2 is an organization or taxonomy of the existing and emerging memory technologies into four categories. A strong theme is the need to monolithically integrate each of these memory options onto a CMOS technology platform in a seamless manner. Fabrication technologies are sought that are modifications of or additions to a CMOS platform technology. A goal is to provide the end user with a device that behaves similar to the familiar silicon memory chip.

Table ERD2 Memory Taxonomy

Because each of these new approaches attempts to mimic and improve on the capabilities of a present day memory technology, key performance parameters are provided in Table ERD3 for existing baseline and prototypical memory technologies. These parameters provide relevant benchmarks against which the current and projected performance of each new research memory technology may be compared.

Table ERD3 Current Baseline and Prototypical Memory Technologies

The emerging research memory technology entries in the current version of the roadmap differ in several respects from the 2009 edition. These changes in technology entries in this section are captured in the Transition Table for emerging research memory devices (Table ERD4). The changes are: 1) *STT-MRAM* is taken out of Table ERD5 (this technology entry is now addressed in the PIDS chapter); 2) *FeFET* memory is replaced with *Emerging Ferroelectric* memory, 3) *Nanothermal* and *Nanoionic* memories are now merged in *Redox* memory, 4) *Electronic Effects Memory* is taken out of Table ERD5, and lastly 5) A new entry for *Mott* memory is added. The reasons and motivations for these changes are given in Table ERD4.

Table ERD4 Transition Table for Emerging Research Memory Devices

Table ERD5 Emerging Research Memory Devices—Demonstrated and Projected Parameters

This memory portion of this section is organized around a set of six technology entries shown in the column headers of Table ERD5. These entries were selected using a systematic survey of the literature to determine the areas of greatest worldwide research activity. Each technology entry listed has several sub-categories of devices that are grouped together to simplify the discussion. Key parameters associated with the technologies are listed in the table. For each parameter, three values for performance are given: 1) minimum performance, satisfactory for practical application, 2) theoretically predicted performance values based on calculations and early experimental demonstrations, 3) up-to-date experimental values of these performance parameters reported in the cited technical references.

The last row in Table ERD5 contains the number of papers on the particular device technology published in the last two years. It is meant to be a gauge of the amount of research activity currently taking place in the research community and it is a primary metric that determines which of the candidate devices are included in this table. The tables have been extensively footnoted and details may be found in the indicated references. The text associated with the table gives a brief summary of the operating principles of each device and as well as significant scientific and technological issues, not captured in the table, but which must be resolved to demonstrate feasibility.

The purpose of many memory systems is to store massive amount of data, and therefore *memory capacity* (or *memory density*) is one of the most important system parameters. In a typical memory system, the memory cells are connected to

[3] Including a particular approach in this section does not in any way constitute advocacy or endorsement. Conversely, not including a particular concept in this section does not in any way constitute rejection of that approach. This listing does point out that existing research efforts are exploring a variety of basic memory mechanisms.

form a two-dimensional array, and it is essential to consider the performance of memory cells in the context of their array architecture. A memory cell in array can be viewed as being composed of two fundamental components: the '*Storage node'* and the *'Selector',* which allows a given memory cell in an array to be addressed for read or write. Both components impact scaling limits for memory. For several advanced concepts of resistance-based memories, the storage node can in principle be scaled down below 10 nm[1], and the memory density will be limited by the select device. Thus the select device represents a serious bottleneck for ReRAM scaling to 10 nm and beyond. Planar transistors (e.g. FET or BJT) are typically used as select devices. In two-dimensional layout using in-plane select FETs the cell layout area is A_{cell}=(6-8)F^2. In order to reach the highest possible 2-D memory density of 4F^2, a vertical select transistor can be used. Table ERD6 shows several examples of vertical transistor approaches currently being pursued for select devices. Another approach to obtaining a select device with a small footprint is a two-terminal nonlinear device, e.g. a diode, either as a separate device or intrinsic to a nonlinear resistive memory element. Table ERD7 displays benchmark parameters required for a 2-terminal select device and Table ERD8 summarizes the operating parameters for several candidate 2-terminal select devices.

Table ERD6 Experimental Demonstrations of Vertical Transistors In Memory Arrays

Table ERD7 Benchmark Select Device Parameters

Table ERD8 Experimentally Demonstrated 2-Terminal Select Devices

Storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost per bit of conventional hard-disk magnetic storage. Such a device requires a nonvolatile memory technology that can be manufactured at a very low cost per bit. The potential of prototypical and emerging research memory devices for SCM applications is assessed in the context of existing commercialized storage technologies, namely the magnetic hard disk drives (HDD) and nonvolatile semiconductor flash memory. Table ERD9 lists a representative set of *target* specifications for SCM devices and systems compared with benchmark parameters of existing technologies (HDD, NAND Flash, and DRAM). To be successful, SCM should offer a combination of the reliability, fast access, and endurance of a solid-state memory, together with the low-cost archival capabilities and vast capacity of a magnetic hard disk drive. Table ERD10 shows the potential of *prototypical* memory technologies (Table ERD3) and the current emerging research memory entries (Table ERD5) for storage-class memory applications based on the above parameters.

Table ERD9 Target device and System Specifications for SCM

Table ERD10 Potential of the Current Prototypical and Emerging Research Memory Candidates for SCM Applications

4.1.1. MEMORY TAXONOMY

Table ERD2 provides a simple way to categorize memory technologies. In this scheme, equivalent functional elements that make up a cell are identified. For example, the familiar DRAM cell that consists of an access transistor and a capacitor storage node is labeled as a 1T1C technology. Other technologies, such as STT-MRAM where data is stored as the spin state in a magnetic material, can be represented as a 1T1R technology. Here the resistance "R" indicates that the cell readout is accomplished by sensing the current through the cell. The utility of this form of classification reflects the trend to simplify cells (i.e., reduce cell area) by reducing the number of equivalent elements to a minimum. Thus, early in the development of a given technology it is common to see multi-transistor multi-x (x equals capacitor or resistor) cells. As learning progresses, the structures are scaled down to a producible 1T1x form. The near ideal arrangement is to incorporate the data storage element directly into the transistor structure such that a 1T cell is achieved. In ultra-dense nanoelectronic memory arrays, instead of the transistor "T", a two terminal non-linear diode-like element may be used with a resistive memory element. Such structure is represented as 1D1R technology.

An important property that differentiates emerging research memory technologies is whether data can be retained when power is not present. Nonvolatile memory offers essential use advantages, and the degree to which non-volatility exists is measured in terms of the length of time that data can be expected to be retained. Volatile memories also have a

characteristic retention time that can vary from milliseconds to (for practical purposes) the length of time that power remains on.

4.1.2. MEMORY DEVICES

4.1.2.1. Ferroelectric Memory

Emerging Ferroelectric Memory consists of two exploratory classes: 1) Ferroelectric FET and 2) Ferroelectric polarization ReRAM. (This entry should not be confused with the conventional ferroelectric capacitor-based memory (FeRAM or FRAM), which is addressed in tables in PIDS and Table ERD3.

4.1.2.1.1. Ferroelectric FET

The Ferroelectric FET (FeFET)[2] memory is a 1T memory device where a ferroelectric capacitor is integrated into the gate stack of a FET. The ferroelectric polarization directly affects charges in the channel and leads to a defined shift of the output characteristics of the FET. A typical FeFET memory element uses inorganic complex oxides or fluorides, such as $PbZr_xTi_{1-x}O_3$, $SrBa_2Ta_2O_9$, $BiMgF_4$, in the gate stack of a silicon FET. A serious difficulty with these materials is interdiffusion and chemical reaction between the stack interfaces at the high deposition temperatures and high oxygen concentrations needed for deposition of the ferroelectric films on a Si substrate[2,3]. In order to avoid the diffusion problem, an insulating buffer layer is inserted between a ferroelectric film and the Si substrate[2], hence, the resulting gate structure consists of a metal-ferroelectric-insulator-semiconductor (MFIS) gate stack. Using an organic ferroelectric film (for example polyvinylidene fluoride - PVDF) as a gate dielectric allows for elimination of the buffer layer, due to lower crystallization temperature of organic materials, and therefore suppression of the diffusion[2,3]. The major challenge of the FeFET memory is the short retention time (typically ~days to ~months), which is the result of two fundamental mechanisms, namely the finite depolarization field present in the stack and the charge injection in the stack due to ferroelectric polarization and a subsequent charge trapping[4,5]. Proposed approaches to increase retention time include improvements of the quality of the FE layer and its interface with the FET structure, e.g. by using all-oxide heteroepitaxial structures[6]. As an ideal case, the use a perfect, single crystal single-domain ferroelectric has been discussed[4,5].

Short retention of the FeFET memory raises question of its potential for application as nonvolatile memory, e.g. for the S-SCM technologies [see the SCM section 4.1.4 below]. On the other hand, DRAM-like applications are envisioned[5] and the FeFET memory may have a potential for M-SCM, if scalability below 50 nm can be demonstrated. Currently, new materials for the FeFET stacks are being actively investigated, such as organic ferroelectrics[3,7], nanotubes[8], nanowires[9], and graphene[10]. The FeFET memory scaling is projected to end approximately with the 22 nm generation, because the insulation layer becomes too thin and the properties of the ferroelectric with respect to thickness dependence of the coercive field will not allow further reduction[11].

4.1.2.1.2. Ferroelectric Polarization ReRAM

The *ferroelectric polarization ReRAM* is based on a M-FE-M structure where changing ferroelectric polarization can modify the charge injection/transport properties of FE films. The correlations between the resistance change and the ferroelectric switching are explained in terms of different mechanisms, such as modulation of the Schottky barrier[12], FE tunnel junctions[13], and polarization-induced lattice strains[14]. A serious challenge for practical ferroelectric ReRAM is typically low ferroresistive current (most ferroelectrics are insulating wide bandgap materials)[15]. In order to obtain sufficiently high currents needed for the stable detection of the memory state, thin ferroelectric layers are required[15], which constitutes a significant practical issue.

4.1.2.2. Nanoelectromechanical memory (NEMM)

The NEMM is based on a bi-stable nano-electromechanical switch (NEMS). In this concept, mechanical digital signals are represented by displacements of solid nanoelements (e.g. nanowires, nanorods, or nanoparticles), which result in closing or opening of an electrical circuit. Several different modifications of suspended-beam/cantilever NEMMs are currently being explored using different materials including Si[16], Ge[17], TiN[18] CNT[19], and others. A difficult challenge of the cantilever NEMM is scalabily: the cantilever spring constant and therefore the pull-in voltage are increasing as the beam's length decreases. NEMM scaling analysis[20] suggests that it might be difficult to achieve low-voltage (~1 V) operation for the beam length less than 50 nm. Vertically oriented cantilever switches could reduce the NEMM area footprint[16]. In addition, nanoelectromechanical torsion switches has recently been demonstrated[21,22], which are claimed to have better scaling properties[22].

There are also proposals for hybrid NEMS/floating gate memory devices to improve the write/erase characteristics. In these devices, either floating gate[23] or control gate[24] are made as a suspended bridge or cantilever[25], separated from the other by an air gap. The suspended bridge electrode can move within the gap under applied voltage, thus changing the separation between the control and floating gates, e.g. smaller for the fast write/erase and larger for longer retention time for the storage mode.

Limited endurance is a serious issue of experimentally demonstrated NEMM devices, as they often fail after ~100 switching cycles[17,18,19,26].

4.1.2.3. Redox Memory

The redox-based nanoionic memory operation is based on a *change in resistance* of a MIM structure caused by ion (cation or anion) migration combined with redox processes involving the electrode material or the insulator material, or both[27,28]. Three classes of electrically induced phenomena have been identified that involve chemical effects, i. e. effects which relate to redox processes in the MIM cell. In these three ReRAM classes, there is a competition between thermal and electrochemical driving forces involved in the switching mechanism. Firstly, the bipolar electrochemical metallization mechanism or memory effect (ECM), relies on an electrochemically active electrode metal such as Ag, the drift of the highly mobile Ag^+ cations in the ion conducting ´I´ layer, their discharge at the (inert) counter electrode leading to a growth of Ag dendrites. These dendrites form a highly conductive filament connecting the metal electrodes resulting in the ON state of the cell[29]. Upon reversal of polarity of the applied voltage, an electrochemical dissolution of these filaments takes place, resetting the system into the high-resistance OFF state. Second, the valence change mechanism or memory effect (VCM) occurs in specific transition metal oxides and is triggered by a migration of anions, such as oxygen anions (which are typically described by the motion of the corresponding vacancies, i. e. oxygen vacancies). A subsequent change of the stoichiometry leads to a redox reaction expressed by a valence change of the cation sublattice and a change in the electronic conductivity. This bipolar memory switching is induced by voltage pulses, where the polarity of the pulse determines the direction of the change, i.e. reduction or oxidation. A third class relies on a unipolar thermo-chemical mechanism or memory effect (TCM, often called fuse-antifuse memory) which leads to a change of the stoichiometry due to a current induced increase of the temperature[30].

The material class for redox memory is comprised of oxides, higher chalcogenides (including glasses), semiconductors, as well as organic compounds including polymers. In some cases, a formation process is required before the bi-stable switching can be started[28]. Often, the conduction is of filamentary nature. If this effect can be controlled, memories based on this bi-stable switching process can be scaled to very small feature sizes. The switching speed is limited by the ion transport. If the active distance, which is relevant for the redox controlled bi-stable switching, is small (in the < 10 nm regime) the switching time can be as low as a few nanoseconds. Many details of the mechanism of the reported phenomena are still unknown. Developing an understanding of the physical mechanisms governing switching of the redox memory is a key challenge for this technology. Nevertheless, recent experimental demonstrations of scalability, retention and endurance are encouraging[31,32]

4.1.2.4. Mott Memory

In the Mott memory, charge injection induces a transition from strongly correlated to weakly correlated electrons, resulting in an insulator-metal transition (IMT) or *Mott* transition. Electronic switches and memory elements based on the Mott transition (sometimes referred as CeRAM – correlated electron random access memory) has been explored using several materials systems, such as VO_2[33], $SmNiO_3$[34], NiO[35,36,37] and others. It is argued that the switching mechanism is activated by a critical electron population described by the Mott-Hubbard model[35,36]. Recently, a reversible and nonvolatile resistive switching has been reported for a class of Mott insulators AM_4X_8 (A=Ga, Ge; M=V, Nb, Ta; X=S, Se), and their potential for memory devices has been discussed[38].

A critical issue for this type of device is the sensitivity of the behavior of correlated electrons to small changes in parameters, including charge density, strain, disorder, and local chemical composition. Thus, precise control of the physical and chemical structure of the material and interfaces is crucial. For IMT in NiO, it was found that fine tuning of electronic phase transition is possible by $Ni(CO)_4$ doping[36,37]. Such doping stabilizes the oxygen vacancies resulting in a pure Mott transition system[37].

More recently, a new metal-insulator transition effect has been explored which is based on formation of a quasi two-dimensional electron gas (2DEG) at the interface between two complex oxides[39,40,41,42]. For example, room-temperature switching of 2DEG nanowires $LaAlO_3/SrTiO_3$ grown on Si substrate has been demonstrated and the opportunities for nanoscale memory devices discussed[42]

4.1.2.5. Macromolecular Memory

Macromolecular memory, also referred to as *polymer* or *organic* resistive memory, consists of a memory element, which is a film of organic material sandwiched between two metal electrodes[43,44]. The organic film is typically relatively thick (~many monolayers). Reduced fabrication cost is often considered as the primary driver for this type of memory, while extreme scaling is de-emphasized[44]. The memory operation mechanisms are still unclear. Some research suggests that the changes in resistance could be due to intrinsic molecular mechanisms[44], charge trapping[45, 46], or redox/ionic mechanisms[44].

Example material systems for macromolecular memory devices include different polymers and small-molecule organic compounds, e.g. polyimides[47], polyfluorenes[48], PMMA[49](PMMA=poly(methylmethacrylate)), TCNQ (TCNQ=7,7,8,8-tetracyano-p-quinodimethane) [50]. The active organic insulator layer in the macromolecular memory often contains embedded conductive components, such as metal nanoparticles[46], ultrathin graphite layers[49] etc. The role of these conductive components remains unclear.

Small macromolecular resistive memory arrays have been demonstrated[51,52,53], including a 3D-stack of three active layers[54].

4.1.2.6. Molecular Memory

Molecular memory is a broad term encompassing different proposals for using individual molecules or small clusters of molecules as building blocks of memory cells. In the molecular memory, data are stored by applying an external voltage that causes a transition of the molecule into one of two possible conduction states. Data is read by measuring resistance changes in the molecular cell. The concept emphasizes extreme scaling; in principle, one bit of information can be stored in the space of a single molecule[55]. Computing with molecules as circuit building blocks is an exciting concept with several desirable advantages over conventional circuit elements. Because of their small size, very dense circuits could be built, and bottom-up self-assembly of molecules in complex structures could be applied to augment top-down lithography fabrication techniques. As all molecules of one type are identical, molecular switches should have identical characteristics, thus reducing the problem of variability of components. However, the success of molecular electronics depends on our understanding of the phenomena accompanying molecular switching, where currently many questions remain. Early experiments on the reversible change in electrical conductance generated considerable interest[56,57]. However, further studies revealed several serious challenges for single/few molecule devices due to extreme sensitivity of the device characteristics to the exterior parameters such as contacts, reproducible nanogap, environment etc. Also, there are multiple mechanisms contributing to the electrical characteristics of the molecular devices, e.g. the conductivity switching as an intrinsic behavior of molecular switches may often be masked by other effects, such as e.g., in some cases, formation of metal filaments along the molecule attached between two metal electrodes[58]. In other cases, intrinsic molecular switching has been reported, and a 160-kbit molecular memory has been fabricated[59]. Molecular memory is viewed as a long term research goal. The knowledge base for molecular electronics needs further fundamental work, which is currently under way[60,61].

4.1.3. Memory Select Device

The purpose of many memory systems is to store massive amounts of data, and, therefore, *memory capacity* (or *memory density*) is one of the most important system parameters. Thus in a typical memory system, the memory devices (cells) are connected to form an array, and it is essential to consider the performance of memory devices in the context of their array architecture. A memory cell in array can be viewed as being composed of two fundamental components: the '*Storage node'*, which is usually characterized by the physics of operation of different memory devices, and the *'Selector',* which allows a given memory cell in an array to be addressed for read or write. Both components impact scaling limits for memory. It should be noted that for several advanced concepts of resistance-based memories, the storage node could in principle be scaled down below 10 nm[62], and the memory density will be limited by the select device. Thus the select device represents a serious bottleneck for ReRAM scaling to 10 nm and beyond. The select device is a non-linear element, which can operate as a switch. Typical examples are transistors (e.g. FET or BJT) or 2-terminal devices, e.g. diodes. Up to now, a planar FET is commonly used as the select device in practical memory arrays, such as DRAM or flash. In a two-dimensional layout using in-plane select FETs, the cell layout area is A_{cell}=(6-8)F^2. In order to reach the highest possible 2-D memory density of 4F^2, a vertical select transistor needs to be used; this approach is currently being pursued.

4.1.3.1. Vertical Transistors

Several examples of experimental demonstrations of vertical select transistors used in memory arrays are presented in Table ERD6. While a vertical select transistor allows for the highest planar array density ($4F^2$), this technology is more difficult to integrate into stacked 3D memory, than the conventional $8F^2$ technology using planar FETs. For example, to avoid thermal stress on the memory elements on the existing layers, the processing temperature of the vertical transistor as selection devices in 3D stacks must be low. Also, making contact to the third terminal (gate) of vertical FET constitutes an additional integration challenge, which usually results in cells size larger than $4F^2$[63]; although true $4F^2$ arrays can, in principle, be implemented with 3-terminal select devices[64].

4.1.3.2. Two-terminal select devices (resistance-based memories)

In order to achieve the highest planar array density of $4F^2$, without considerable constraints associated with vertical select FETs, passive memory arrays with two-terminal select device are currently being investigated[65,66]. Two-terminal devices with nonlinear behavior (e.g. diodes) can be integrated with resistive storage nodes in a cross-bar array. General requirements for such two-terminal switches are sufficient ON currents at proper bias to support read and write operations and sufficient ON/OFF ratio to enable selection. The minimum ON current required for fast read operation is ~ 1μA (Table ERD7). The required ON/OFF ratio depends on the size of the memory block, $m \times m$: for example using a standard scheme of array biasing the required ON/OFF ratio should be in the range of 10^7-10^8 for m=10^3-10^4, in order to minimize the 'sneak' currents[67]. These specifications are quite challenging, and the experimental scaled select devices have yet to meet them. Thus, select devices are becoming a critical part of emerging memory and there is a need for detailed analysis on the performance requirement. It should be noted that resistance based memories could target different applications, which may impact requirements for the select device. Currently two approaches to integrating the select device with storage node are being pursued. The first approach is to use an external select device in series with the storage node, e.g. integrated in a multilayer stack. The second approach is to use a storage element with inherent nonlinear (e.g. rectifying) properties.

4.1.3.2.1. Diode-type select devices

The simplest realizations of two-terminal memory select devices use semiconductor diode structures, such as a *pn*-junction diode, Schottky diode, or heterojunction diode. Such devices are suitable for a unipolar memory cell. For bipolar memory cells, selectors with two-way switching are needed. Proposed examples include Zener diodes[68], BARITT diodes[69], reverse breakdown Schottky diode[70], and c*omplementary resistive switches*[71,72]. In the latter approach, the memory cell is composed of two identical non-volatile ReRAM switches connected back-to-back (for example in the Pt/GeSe/Cu/GeSe/Pt structure[71]; or vertically integrated in a Pt/SiO_2/Cu/SiO_2/Pt structure[72]). In such a configuration, one of the switches will always be at the high-resistance state so the sneak current can be suppressed at low bias. The read operation however is destructive, and the cell state needs to be recovered by re-programming the disturbed switch back to HRS afterwards. It should be noted that several read modes have been suggested which can be adapted to specific applications. Representative data on the experimental device parameters of diode type select devices used in memory arrays are shown in Table ERD8.

4.1.3.2.2. Resistive-Switch-type select devices

The category of "switch-based selector" refers to recent innovative device concepts that exhibit resistive switching behavior. In fact, in some of these concepts, the device structure/physics of operation is similar to the structure of the storage node. In other words, a modified memory element could act as a select device. The main difference between the two is that a 'nonvolatile' switch is required for the storage node, while for the select device, depending on the approaches, non-volatility may not be necessary and can sometimes be detrimental. A brief description of several proposed select devices is given below.

4.1.3.2.2.1. MIT switch

This device is based on the Metal-Insulator Transition, such as Mott transition, and exhibits a low resistance above a critical electric field (threshold voltage). The select device will exhibit a high-resistance state if the voltage is below a hold voltage. To achieve reliable read the select device needs to be volatile to ensure rapid transition from the low-resistance state to high-resistance state at low bias. If the electronic conditions that triggered Mott transition can relax within the memory device operation time scale, the Mott transition device is essentially a volatile resistive switch, which can be utilized as a select device. A VO_2-based device has been demonstrated as a select device for NiO_x RRAM element[73]. However, the switching mechanism is not clear and the feasibility of the Mott-transition switch as select devices still needs further research. It should be also noted that VO_2 undergoes a phase transition to the metal state at temperature around 68°C, and thus its operation as MIT switch is restricted to temperatures below 68°C. This limits

practical applications of VO_2 in memory devices as current specifications require operational temperature of 85°C. Suitable Mott materials with higher transition temperatures need to be investigated. Recently, metal insulator transitions at ~ 130°C and electrically driven MIT switching were observed in thin films of $SmNiO_3$ [74].

4.1.3.2.2.2. Threshold switch

This type of select device is based on the threshold-switching effect observed in thin-film based MIM structures, where the threshold switching is caused by electronic charge injection. Operation of the threshold switch is thus governed by an electronic switching process. Significant resistance reduction can occur at a threshold voltage and this low-resistance state quickly recovers to the original high-resistance state when the applied voltage falls below a holding voltage. One example is the threshold switching which occurs before the structural change in phase change materials[75].

4.1.3.2.2.3. MIEC switch

This type of select device is based on the exponential I-V characteristics observed in materials that conduct both ions and electronic charges – so called mixed ionic and electronic conduction materials (MIEC). The resistive switching mechanism of MIEC switch is similar to the ionic memories. With appropriate control, the resistive switching in MIEC devices is volatile and provides device selection functions[76].

4.1.3.2.3. Summary – 2 Terminal Switches

As follows from Table ERD8, the required device characteristics have not yet been demonstrated and remain a significant scientific and technical challenge. For scaled two-terminal select devices two fundamental challenges are *contact resistance*[77] and *lateral depletion effects*[78,79]. Very high concentration of dopants is needed to minimize both effects. However, high dopant concentrations result in increased reverse bias currents in classical diode structures and therefore in reduced I_{on}/I_{off} ratio. For switch-type select devices the main challenges are identifying the right material and the switching mechanism to achieve the required drive current density, I_{on}/I_{off} ratio, and reliability.

4.1.4. Storage Class Memory

Storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost of conventional hard-disk magnetic storage[80,81]. Such a device requires a nonvolatile memory technology that could be manufactured at a very low cost per bit. The potential of prototypical and emerging research memory devices for SCM applications is assessed in the context of existing commercialized storage technologies, namely the magnetic hard disk drives (HDD) and nonvolatile semiconductor flash memory.

4.1.4.1. Hard-disk drives

Conventionally, magnetic hard-disk drives are used for nonvolatile data storage. The cost of HDD storage (in $/GB) is extremely low and continues to decrease. Although the bandwidth with which contiguous data can be streamed is high, the poor random access time of HDDs limits the number of I/O requests per second (IOPs). Also, HDDs have relatively high energy consumption, large form factor, and limited reliability.

4.1.4.2. Flash solid-state drives

Nonvolatile semiconductor memory in the form of NAND flash has recently become an alternative storage technology, which has faster access times, smaller size and potentially lower energy consumption, as compared to HDD. The NAND-based solid state drive (SSD) market has flourished recently. However, there are several serious limitations of NAND flash for storage applications, such as poor endurance (10^4 – 10^5 erase cycles), modest retention (typically 10 years on a new device, but only 1 year at the end of rated endurance lifetime), long erase time (~ms), and high operating voltage (~15V). Another difficult challenge of NAND flash SSD is due to its page/block-based architecture, which doesn't allow for a direct overwrite of data, thus requiring sophisticated garbage collection and bulk erase procedures, which takes extra memory space, limits performance and accelerates the wearing out of memory cells. Therefore, computation-intensive algorithms for garbage collection, wear leveling and error correction are needed for SSD operation. As result, a SSD, in addition to its flash memory, also includes a processor, RAM, peripheral logic etc[82].

While, flash memory technology continues to have opportunity for further scaling, the scaling doesn't improve the basic performance characteristics, such as read, write and erase latencies, which have been nearly constant for over a decade[83]. Recent introduction of multi-level cell (MLC) flash devices extends the flash memory capacity by a factor of two, or potentially in the future, by as much as eight times. However, both extreme scaling and use of MLC result in the degradation of retention time and endurance, two parameters critical for storage applications; therefore the promise of

significant density improvement beyond today's flash devices is limited. This outlook has provided opportunities for prototypical and emerging research memory technologies to enter the non-volatile solid state memory space.

4.1.4.3. Prototypical and emerging research memory technologies for SCM applications

As the scalability of flash is approaching its limit, emerging technologies for non-volatile memories need to be investigated for a potential "take over" of the scaling roadmap for flash. In principle, such new SCM technology could engender two entirely new and distinct levels within the memory and storage hierarchy, differentiated from each other by access time and located below off-chip DRAM and above mechanical storage.

The first new level, identified as S-type storage-class memory (S-SCM), would serve as a high-performance solid-state drive, accessed by the system I/O controller much like an HDD. S-SCM would need to provide at least the same data retention as flash, allowing S-SCM modules to be stored offline, while offering new direct overwrite and random access capabilities (which can lead to improved performance and simpler systems) that NAND flash devices cannot provide. However, it would be absolutely critical that the device cost *at introduction* for S-SCM be no more than 1.5-2x higher than NAND flash, in order to guarantee large unit volumes and justify the capital investment in an unproven new technology. If the cost per bit could be driven low enough through ultrahigh memory density, ultimately such an S-SCM device could potentially replace magnetic hard-disk drives in enterprise storage server systems, as well as in mobile computers.

The second new level within the memory and storage hierarchy, termed M-type storage-class memory (M-SCM), should offer a read/write latency of less than 100 ns. These specifications would allow it to remain synchronous with a memory system, allowing direct connection from a memory controller and bypassing the inefficiencies of access through the I/O controller. The role of M-SCM would be to augment a small amount of DRAM to provide the same overall system performance as a DRAM-only system, while providing moderate retention, lower power-per-GB and lower cost-per-GB than DRAM. Again, as with S-SCM, the cost target is critical. It would be desirable to have cross-use of the same technology in either embedded applications or as a standalone S-SCM, in order to spread out the development risk of a M-SCM technology. The retention requirements for M-SCM are less stringent, since the role of non-volatility might be primarily to provide full recovery from crashes or short-term power outages.

Particularly critical for M-SCM will be device endurance, since the time available for wear-leveling, error-correction, and other similar techniques is limited. The volatile portion of the memory hierarchy will have effectively infinite endurance compared to any of the non-volatile memory candidates that could become an M-SCM. Even if device endurance can be pushed well over 10^9 cycles, it is quite likely that the role of M-SCM will need to be carefully engineered within a cascaded-cache or other Hybrid Memory approach[84]. That said, M-SCM offers a host of new opportunities to system designers, opening up the possibility of programming with truly persistent data, committing critical transactions to M-SCM rather than to HDD, and performing commit-in-place database operations.

The density and cost requirements of SCM transcend what may be achieved through the straightforward scaling application of Moore's Law. Additional techniques will be needed to achieve the ultrahigh memory densities and extremely low cost demanded by SCM, either by using: (1) 3-D integration of multiple layers of memory, currently implemented commercially for write-once solid-state memory[85], and/or (2) Multiple bits per cell (MLC) techniques.

The goal of SCM development is to create compact, robust storage (and memory) systems with greatly improved cost/performance ratios relative to other technologies. The defining requirements for all SCM technologies are non-volatility (ranging from 1 week to 10 years), very low latencies (ranging from hundreds of nanoseconds up to tens of microseconds), physical durability during practical use, and most important, ultra-low cost per bit.

Table ERD9 lists a representative set of *target* specifications for SCM devices and systems compared with benchmark parameters of existing technologies (HDD and NAND Flash). To be successful, SCM should offer a combination of the reliability, fast access, and endurance of a solid-state memory, together with the low-cost archival capabilities and vast capacity of a magnetic hard disk drive.

In view of the current market success of SSD, while there is only a limited potential for further improvements in flash storage devices, it appears that storage applications could be the primary driver for the new memory technologies, as they may help to overcome the fundamental shortcomings of flash technology. Necessary attributes of a memory device for the storage-class memory applications (mainly driven by the requirement to *minimize the cost per bit*) are:

- Scalability

- Multilevel Cell (however MLC vs. extreme scaling dilemma should be noted)
- 3D integration
- Fabrication costs
- Endurance (for M-SCM)
- Retention (for S-SCM)

Table ERD10 shows the potential of the *prototypical* memory (Table ERD3) and the current emerging research memory entries (Table ERD5) for storage-class memory applications based on the above parameters. A likely introduction of these new memory devices to the market is by the *hybrid* solid-state discs, where the new memory technology complements the traditional flash memory to boost the SSD performance. Experimental implementations of FeRAM/flash[86] and PCRAM/flash[87] have recently been explored. It was shown that the PCRAM/Flash hybrid improves SSD operations by decreasing the energy consumption and increasing the lifetime of flash memory[87].

4.1.4.4. Memory Interfaces

Since SCM is a system level approach to fill the memory gap, not only development of the memory technology itself, but dedicated interface and architecture for each technologies are necessary to be examined, in order to make use of the potential, and/or to back up the weakness of the memories. For example, performance of flash SSD is strongly limited by their interface performance. The standard SATA (Serial Advanced Technology Attachment) interface, which is a commonly used interface for SSD, was originally designed for HDD, and is not optimized for flash SSD[88]. There are several approaches to employ novel interface or architecture to take advantage of the flash SSD performance[88,89,90]. In considering new SCM candidates, one should explore new memory interface solutions at a system level.

4.1.1.5 Architectural Implications

In addition to storage applications, successful implementation of SCM could also affect developments in new chip architectures. For example, advances in SCM could drive the emerging data-centric chip architectures, the *Nanostores*[91], which could be an important direction for the future of information processing. A detailed discussion of the architectural implications of SCM in the context of different applications can be found in the *Emerging Research Architectures* Section 5.

4.2. LOGIC AND ALTERNATIVE INFORMATION PROCESSING DEVICES

A primary goal of this chapter is to survey, assess and catalog viable new information processing devices and systems architectures for their long-range potential and technological maturity. The purpose of this section is to focus on the devices themselves. The organization of the section is unchanged from the 2009 edition. It contains a transition table, Table ERD11, that provides the disposition of technologies transitioned into and out of Table ERD12 from 2009 to 2011. It also gives a preview of new technologies that may be included in the 2013 edition. The section divides 18 Technology Entries into three separate tables. These tables are labeled: ERD12a MOSFET: Extending MOSFETs to the End of the Roadmap"; ERD12b"Charge based Beyond CMOS: Non-Conventional FETs and other Charge-based Information Carrier Devices", and ERD12c; "Non-FET, Non Charge-based 'Beyond CMOS' Devices" respectively. The titles of the three tables are suggestive of their contents. The first table contains extensions and enhancements to current MOSFETs. They are all charge based and utilize a basic MOSFET functionality. ERD12b entries all involve electron transport but the switching function is inherently different from the MOSFET functionality and involves effects such as quantum mechanical tunneling and Coulomb blockade. Entries in ERD12c involve information carriers other than electronic charge and utilize effects such as spin wave interference and magnetic exchange coupling. The entries in ERD12a, ERD12b and ERD12c have a progressively longer horizon in terms of the date of possible introduction. The contents of ERD12c are heavily influenced by the U.S. based Nanoelectronics Research Initiative which has chosen to focus on devices using computational state variables other than electronic charge. This has resulted in a collection of novel devices based on spin waves, spin diffusion, ferroelectric ordering and even excitonic Bose Einstein condensates. They all show promise for various special purpose functionalities and offer potential for new applications which have not yet been conceived.

Table ERD11 Transition Table for Emerging Research Logic Devices

Table ERD12a MOSFETS: Extending MOSFETs to the End of the Roadmap

Table ERD12b Charge based Beyond CMOS: Non-Conventional FETs and other Charge-based Information Carrier Devices

Table ERD12c Alternative Information Processing Devices

4.2.4. LOGIC DEVICES

4.2.4.4. MOSFET: Extending MOSFETs to the End of the Roadmap

4.2.4.4.1. Carbon Nanotube FETs

The most often mentioned advantages of Carbon Nanotube FETs are the high mobility of charge carriers and the potential to minimize the subthreshold slope (i.e., minimize the short channel effects) by a surround gate geometry. However, there are multiple challenges to achieving this, including: 1) the ability to control bandgap energy, 2) positioning of the nanotubes in required locations and directions, 3) control of the number of nanotube walls, 4) control of charge carrier type and concentration, 5) deposition of a gate dielectric, and 6) formation of low resistance electrical contacts.

In the past two years, significant advances have been made in fabricating and characterizing CNT FETs. They include 1) maintaining their performance as their channel length was scaled down to 15 nm without observing the short channel effect[92]; 2)fabricating a 15-nm device showing a transconductance of 40 μS for a single channel; 3) fabricating a FET with an extrinsic f_T of 15 GHz and an intrinsic f_T of 80 GHz[93]; 4) fabricating a n-type FET with Y contacts and projected 2.06 ps gate delay[94]; and 5)fabricating a CMOS inverter with a noise margin of 0.67 V at V_{DD} of 2 V using fully CMOS compatible materials[95].

In addition, continuous progress has been achieved for the remaining challenges including sorting carbon nanotubes with chemical techniques to achieve a distribution of nanotubes with controlled bandgap energy and improving the purity of single chiral semiconducting nanotubes to ~99%[96]. This is still however, many orders of magnitude less than would be required for fabrication of VLSI. Dense and highly-aligned semiconducting nanotubes have been grown on quartz substrates, and transferred to silicon wafers. However, the purity of the semiconductor nanotubes is~ 95 %, and the growth mechanism is not well understood[97]. The Langmuir -Blodgett method and the evaporating-droplet method have been proposed as alternative technologies to achieve highly-dense and aligned semiconducting nanotubes. However, a technology to remove dispersants is needed to form a good contact and to reduce unintentional doping. A technique for controlling carrier type and concentration has been proposed using interface charges incorporated in a high-k gate insulator[98]. The reliability, controllability, and the carrier trapping effect need to be understood. A uniform 5-nm-thick high-k gate insulator has been realized on a nanotube using Y_2O_3[99] but the reproducibility and the interface traps need to be better understood. Good contacts have been formed for both p-type and n-type FETs,[100] but CMOS compatible material is needed for n-type FETs. Even though significant progress has been made, the ultimate goal of depositing dense, aligned, and only semiconducting nanotubes as a high mobility channel replacement material on a silicon wafer remains elusive, as does fabricating nanotube circuits in an otherwise conventional CMOS process flow.

4.2.4.4.2. Graphene Nanoribbon FETs

Graphene materials offer the potential of extremely high carrier mobilities that can exceed that of CNTs, and also offer the promise of patterning graphene nanoribbons using conventional top down processes. Work on graphene field effect transistors (FETs), is proceeding at a rapid pace but is still at an early stage. Beginning with the first description of the electric field effect in graphene in 2004[101], graphene FETs using bottom gating[102], top-gating [103,104,105] dual-gating [106,107], and side-gating [108] have now been demonstrated using exfoliated [109,110] epitaxial [111,112,113] and CVD-grown graphene [114,115].

Research on graphene FETs started with use of exfoliated graphene to form a transistor channel. Recently, there have been many studies using epitaxial graphene on SiC substrates and CVD-grown graphene. Exfoliated graphene still offers the highest mobility[116,117,118] but is not manufacturable. Back-gated graphene FETs with SiO_2 dielectric were typically shown to have field-effect mobilities up to around 10,000 $cm^2/V\ s$[119] (note that although back-gating is not desirable for FET-based circuitry, this mobility value does act as a useful comparison to top-gate mobility values). It has been

predicted that the room-temperature mobility of graphene on SiO_2 is limited to ~40,000 cm^2/Vs due to scattering by surface phonons at the SiO_2 substrate[120] . In fact, the highest field effect mobilities were obtained using suspended graphene. Values as high as 120,000 cm^2/Vs and 1,000,000 cm^2/Vs at 240K and liquid-helium temperatures, respectively[121,122,123] have been measured. Recently, boron nitride, an inert and flat material, was used as a substrate for a graphene channel[124,125], and it was shown that the field effect mobility of such devices can exceed 100,000 cm^2/Vs at room temperature. Epitaxial graphene on SiC has exhibited carrier mobilities as high as 15,000 cm^2/Vs and 250,000 cm^2/Vs at room and liquid helium temperatures respectively[126,127]. On the other hand CVD graphene has shown carrier mobilities as high as 10,000 cm^2/Vs at room temperature[128].

As for top-gated graphene-channel transistors, field-effect mobilities are in general lower than those shown above, because the deposition of gate dielectric can degrade the electrical properties of graphene[129]. In order to avoid such degradation, a buffer layer is often used between graphene and high-k materials[130,131]. It was also shown that SiO_2 layer formed by vacuum evaporation did not degrade graphene channel so much, and field-effect mobilities as high as 5,400 cm^2/Vs were achieved for top-gated transistors[132]. In another case, naturally-oxidized thin aluminum layer was used as a seeding layer of Al_2O_3 by atomic layer deposition and field effect mobilities as high as 8600 cm^2/Vs were achieved[133]. The highest field effect mobility of top-gated graphene transistors was obtained using Al_2O_3 nanowire as gate dielectric, which was as high as 23,600 cm^2/Vs[134]. The highest field-effect mobilities of top-gated transistors using epitaxial graphene and CVD-graphene were 5,400 cm^2/Vs and 4,000 cm^2/Vs, respectively[135,136]. In all the cases mentioned here, the mobilities of electrons and holes are similar.

Predictions of high current densities, extraordinarily high mobilities, and superior FET performance[137,138] with the goal of compatibility with CMOS process and temperature range, continue to drive the rapid pace of innovation in graphene FETs. This innovation, accompanied by evidence of tunable I_{on}/I_{off} via bandgap energy[139,140] and advancement in CVD technology for synthesizing large-area graphene[141,142,143] is likely to bring rapid advances in this area over the next few years, hence ERD's identification of graphene as a possible solution for extending CMOS to the end of the Roadmap.

An important limitation of graphene for digital applications is its zero bandgap energy which in turn will result in a very small I_{on}/I_{off} ratio. As mentioned above, however, several methods to open a bandgap have been proposed. One is to build devices with graphene nanoribbons[144,145,146,147,148]. Carrier transport through a nanoribbon was first demonstrated using nanoribbons fabricated by a top-down approach[149]. Nanoribbons were then made by several other methods[150,151,152,153]. Specifically, it was recently demonstrated that graphene nanoribbon with a precisely-controlled uniform width can be synthesized by a bottom-up approach using precursor monomers[154]. Devices using nanoribbons with a 2-nm width made by sonication of exfoliated graphite in a chemical solution showed an on-off ratio of 10^7, with a field effect mobilitiy of ~200 cm^2/Vs[155]. The relatively low mobility was considered to be caused by scattering at the edges of nanoribbons. In fact, recent theoretical studies showed that obtaining smooth edges is essential to obtain good electrical properties[156]. In addition, recent experimental studies suggest that transport in graphene nanoribbon is greatly affected by defects at the edges and charged impurities[157,158,159]. More efforts are required to realize graphene nanoribbon transistors for CMOS.

An important application space for graphene may be RF with discrete elements and high linearity requirements. There have been many studies aiming at such high-frequency applications[160,161,162]. A cut-off frequency of 300 GHz has been obtained by self-aligned processes using exfoliated graphene and core-shell nanowire as a gate stack[163]. Unity current gain cut-off frequencies as high as 170 GHz and 155 GHz have also been obtained for devices using epitaxial[164] and CVD[165] graphene, respectively. Achieving a high maximum frequency of oscillation is the next important step for realizing RF applications.

4.2.4.4.3. Nanowire Field-Effect Transistors (NWFETs)

Nanowire field-effect transistors are structures in which the conventional planar MOSFET channel is replaced with a semiconducting nanowire. Such nanowires have been demonstrated with diameters as small as 0.5 nm[166]. They may be composed of a wide variety of materials, including silicon, germanium, various III-V compound semiconductors (GaN, AlN, InN, GaP, InP, GaAs, InAs), II-VI materials (CdSe, ZnSe, CdS, ZnS), as well as semiconducting oxides (In_2O_3, ZnO, TiO_2), etc.[167] Importantly, at low diameters, these nanowires exhibit quantum confinement behavior, i.e, 1-D conduction, that may permit the reduction of short channel effects and other limitations to the scaling of planar MOSFETs.

Important progress has been made in the fabrication of semiconducting nanowires for use as FET channels, for which there are two principal methods. The first method is nanoimprint lithography, by which semiconducting channels are formed through a printing or stamping process[168]. The second is catalyzed chemical vapor deposition[169,170]. In particular, the vapor-liquid-solid (VLS) growth mechanism has been used to demonstrate a variety of nanowires, including core-shell and core-multishell heterostructures[171,172]. Heterogeneous composite nanowire structures have been configured in

both core-shell and longitudinally segmented configurations using group IV and compound materials. The longitudinally segmented configurations are grown epitaxially so that the material interfaces are perpendicular to the axis of the nanowire. This allows significant lattice mismatches without significant defects. Vertical transistors have been fabricated in this manner using Si[173], InAs[174,175] and ZnO[176] , with quite good characteristics. Core-shell gate-all-around configurations[177] display excellent gate control and few short channel effects.

Circuit and system functionality of nanowire devices have been demonstrated, including individual CMOS logic gates[178], a PMOS ring oscillator exhibiting ~12 MHz operation[179] , and extended, programmable arrays (a.k.a. "tiles") of nonvolatile nanowires that were used to demonstrate full-adder, full-subtractor, multiplexer, demultiplexer, and clocked D-latch operations[180] . The measured operating speed of these various nanowire test circuits was limited by off-chip interconnect capacitance and thus did not achieve the THz operation that is predicted to be the intrinsic capability of nanowire devices[181].

4.2.4.4.4. N-type III-V channel replacement devices

Use of III-V compound semiconductors as *n*-type channel replacement materials has attracted great attention because of their excellent bulk electron mobilities (μ_e) of 33000 $cm^2V^{-1}s^{-1}$ (InAs) and 80000 $cm^2V^{-1}s^{-1}$ (InSb) respectively. In addition, Sb-based III-V compound semiconductors exhibit hole mobilities (μ_h) of 1250 $cm^2V^{-1}s^{-1}$ (InSb) and 850 $cm^2V^{-1}s^{-1}$ (GaSb), significantly greater than bulk Si μ_h of 500 $cm^2V^{-1}s^{-1}$. InAs has been studied as *n*-type channel replacement materials in several types of structures such as HEMT[182]and nanowire[183,184,185] device structures. The operation of a short-channel device with gate length (L_g) of 30nm has been demonstrated with f_t of 601GHz and f_{max} of 609GHz. Since Sb-based compound semiconductors show high μ_e as well as high μ_h, these are potential CMOS channel replacement materials. $InAs_{0.8}Sb_{0.2}$ quantum-well field-effect transistor have shown high μ_e of 3900-5600 $cm^2V^{-1}s^{-1}$ [186]. InSb quantum well transistors with L_g of 85nm shows f_t of 305 GHz[187] . A unity power gain cut-off frequency f_{max} of 500GHz has been also demonstrated[188]. As a p-channel replacement material, AlSb/InGaSb heterostructure FETs (HFETs) show hole mobility of μ_h 1500$cm^2V^{-1}s^{-1}$ [189] . HFETs with L_g of 0.2μm show f_t of 19GHz and f_{max} of 34GHz[190]. The mobility of buried-channel and surface-channel $In_{0.35}Ga_{0.65}Sb$ pFETs have been evaluated to be 910$cm^2V^{-1}s^{-1}$ and 620$cm^2V^{-1}s^{-1}$, respectively [191]. It has been demonstrated that the strain is quite effective to enhance hole mobility of III-V compounds[192,193,194,195]. $In_{0.41}Ga_{0.59}Sb$ shows piezoresistance coefficient of 1.5x higher than that of Si[196]. The piezoresistance coefficient of p-GaSb shows more than 2x higher than that of Si[197] . Compressively strained InSb quantum well pFETs with L_g of 40nm shows f_t of 140GHz with the power supply voltage of 0.5[198] V. Therefore, III-V compound semiconductor n-channel MOSFETs are considered viable candidates to extend CMOS to the end of the Roadmap. The major challenges facing high volume production of III-V devices include the need for high quality, low EOT gate dielectrics, damage-free low resistivity junctions, and hetero-integration on a VLSI compatible silicon substrates.

4.2.4.4.5. n-type Ge channel replacement devices

Initially, Germanium attracted great attention as a potential channel replacement material because of its excellent bulk electron mobility of 3900 $cm^2V^{-1}s^{-1}$; 2.7x higher than the comparable parameter in bulk Si. However in practice, the actual electron mobility (μ_e) of *n*-type Ge in MOSFETs was much worse than μ_e of n-type Si FET applications and hence looked less promising as a channel replacement material. It has been concluded that the high interface state density (D_{it}) near the conduction band edge is one of the key issues resulting in low μ_e of *n*-type Ge MOSFETs[199] . Therefore, the key to enhancing the mobility is the improvement of Ge/dielectric interface quality. Recently, high-temperature oxidation[200] , high pressure oxidation[201], and ozone oxidation[202], of Ge have been successfully adopted to form good quality Ge oxide and Ge/oxide interface. As a result, excellent μ_e of *n*-type Ge MOSFETs has been recently obtained[203,204,205,206,207]. In addition, optimization of the surface/directional crystal orientation offers another path for improving performance of Ge n-channel MOSFETs and has been pursued by fabricating Ge n-channel MOSFETs on Ge substrates with various surface orientations. Those fabricated on the (111) surface have shown the best peak μ_e of 1920 $cm^2V^{-1}s^{-1}$, [208], which is approximately 2x higher than the bulk Si universal peak mobility. Strain engineering of Ge n-channel MOSFETs has also been studied as a performance booster technology[209,210] and its effectiveness has been demonstrated at a small strain level of approximately 0.1%. Contact performance is impacted by the formation of Ge n+/p junction diodes caused by the low activation of dopants. Laser annealing[211], Sb doping[212], [213], [214], and vapor phase doping[215,216] have been demonstrated as effective methods to achieve high dopant activation of as large as $1x10^{20}cm^{-3}$ [217] . Ohmic contacts to n-Ge are difficult, due to the Fermi level pinning around the valence band edge in Ge/metal contacts. However, progress on high dopant activation technologies serves to mitigate this problem. In order to scale the equivalent oxide thickness (EOT), several gate stack structures using a high-k gate dielectric have been investigated. These include use of a Ge nitride interfacial layer with HfO_2[218], use of a Ge oxide interfacial layer with Y_2O_3[219], and a SiO_2 interfacial layer with Al_2O_3[220]. Although

the operation of short-channel Ge *p*-channel MOSFETs with gate lengths of less than 80nm has been reported, operation of short-channel Ge *n*-type MOSFETs has not yet been demonstrated.

Key research needs required for n-channel Ge devices include resolving whether the low electron saturation velocity in Ge will limit the short channel performance of n-channel Ge MOSFETs relative to Si n-channel MOSFETs. Specifically, the effect of strain greater than 1% should be clarified to show its potential to outperform strained Si n-channel MOSFETs. In summary, even though additional progress is required in reducing EOT, continuing gate-length scaling to and below 20nm, and development of lower-resistivity diffusion layers with lower-resistivity metal contacts, Ge n-channel MOSFETs are good potential candidates to extend CMOS to the end of the Roadmap.

4.2.4.4.6. Tunnel FETs

Tunnel FETs are gated reverse-biased p-i-n junctions that are expected to have $I_{on} - I_{off}$ transitions much more abrupt than conventional MOSFETs, whose 60mV/dec subthreshold swing limit at room temperature is set by the thermal injection of carriers from the source to the channel[221,222,223]. By lowering the subthreshold swing below 60mV/decade, the Tunnel FET can operate at much lower V_{DD} and, thereby, operate with substantially lower power dissipation. At low gate bias, the width of the energy barrier between the intrinsic region and the p^+ region is wider than the minimum for significant band-to-band tunneling probability, and the device is in the OFF-state. As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow. Band-to-band tunneling (BTBT) is a quantum-mechanical phenomenon, providing a much more abrupt transition between $I_{on} - I_{off}$ states of a three terminal switch compared to the 60mV/decade MOSFET limit and a non-constant subthreshold swing with smallest values at low current levels. Tunnel FETs are actively investigated due to their potential for low standby leakage current and as enablers of future logic circuits operating with a supply voltage less than 0.5V thus saving many decades of I_{off}. Recent reports suggest that Tunnel FETs could be also considered as promising candidates for the high performance switch, by using appropriate heterostructure architectures[224] and/or exploiting low band-gap materials such as III-V compound semiconductors, Ge, SiGe, or graphene. Tunnel FETs are expected to match the speed performance of CMOS (in terms of equivalent CV/I metrics) at the same supply voltage but with[225] lower I_{on}.

Many detailed device simulations have predicted that BTBT FETs could produce subthreshold swings below the thermal limit in devices based on conventional semiconductor materials such as silicon[226] or SiGe[227], carbon-nanotube (CNT)[228] or graphene based transistors[229]. Since the tunneling current is determined by the bandgap and effective mass of the material, the silicon TFET seems limited by its low on-state current density and, probably, only high amounts of strain at the tunneling junction (>3GPa) can improve their behavior[230].

Subthreshold swings of less than 60mV/dec have been measured for several different fabricated Tunnel FETs. The first reported results were for a carbon nanotube Tunnel FET[231] whose swing was 40mV/dec over a limited range of small currents. In 2008, two separate Tunnel FETs in the Si/Ge system exhibited a point swing (a subthreshold swing in a small gate voltage range) of 50mV/dec[232] and 42mV/dec[233]. Silicided source devices with 46mV/dec[234,235] with high I_{on}/I_{off} (>10^7 for 0.5V operation) for moderate I_{on}~100μA/μm at V_{DS}=1V have been reported. In 2009, long channel VLS grown silicon nanowire Tunnel FETs[236] were reported with high-k dielectric, I_{on}/I_{off} of the order of 10^7 and an average subthreshold swing over two decades of 120mV/dec at V_{DS}=0.5V. Performance improvements in 25nm narrow fin-like device architectures have been shown[237], with a point slope of 46 mV/dec at low biases and an I_{on}/I_{off} of 10^6 at a supply voltage of 1.2 V (I_{on}=46μA/μm and I_{off} of 5pA/μm) with a MuGFET technology using a high-k dielectric and a metal gate inserted gate stack. All these advanced studies tend to show that a high performance tunnel FET cannot be achieved with all-silicon architectures and would require the use of Ge or III-V material systems on silicon platforms.

Key challenges for tunnel FETs include optimization of the device architecture for high I_{on} combined with an average subthreshold swing lower than 60mV/decade over at least four decades of current. The engineering of the source tunneling region (junction abruptness, bandgap energy, carrier effective mass) and enhancement of gate control on internal electric field are of major importance for achieving an experimental tunnel FET device, matching the predictions made by numerical simulations. In this respect, tunnel FETs can benefit from heterostructures needing low bandgap materials on advanced silicon platforms, which defines a clear technological challenge. Critical research is needed concerning demonstration of staggered–bandgap heterostructure tunnel FETs exploiting narrow bandgap materials on silicon substrates[238] with sub-0.5V power supply and I_{on} performance enabling operation at switching speed on the order of GHz. Significant progress in the future design of integrated circuits based on tunnel FETs or their co-design with CMOS requires the development of specific compact models.

4.2.4.5. Charge based Beyond CMOS: Non-Conventional FETs and other Charge-based information carrier devices

4.2.4.5.1. Spin FET and Spin MOSFET Transistors

Spin-transistors are classified as "Non-Conventional Charge-based Extended CMOS Devices". They exhibit transistor behavior with the functionalities of a magnetoresistive device. The important features of spin-transistors are variable current drivability controlled by the magnetization configuration of the ferromagnetic electrodes (or the spin direction of the carriers) and nonvolatile information storage using the magnetization configuration. These features are very useful and suitable ffunctionalities for highly energy-efficient, low-power circuit architectures that are inaccessible to ordinary CMOS circuits. Field-effect spin-transistors can be divided into two categories, i.e., spin-FET and spin-MOSFET. Although these device structures are similar, their operating principles are quite different[239,240].

The operation of spin-MOSFETs has not yet been experimentally verified[4] [241,242]. However, there has been important progress for spin dynamics in Si channels and for half-metallic ferromagnetic source and drain of spin-MOSFETs. A relatively long spin lifetime in heavily doped Si was observed even at 300K[243] by a detection technique using spin accumulation phenomenon in a ferromagnet-Si tunnel junction interface. However, questions have been raised regarding the evaluation of spin lifetime using spin accumulation methods. Electrical spin injection for Si channels was also demonstrated up to 500k by a similar method[244].

For half-metallic ferromagnetics, there have been major breakthroughs since the previous 2009 ITRS edition. In particular, the application to magnetic tunnel junctions (MTJs) of half-metallic full-Heusler alloy electrodes has progressed greatly. Very high tunneling magnetoresistance (TMR) ratios were observed even at room temperature in such MTJs[245,246]. Current-induced magnetization (spin transfer torque) switching was also confirmed in magnetoresistive devices with full-Heusler alloy electrodes[247]. Moreover, very high quality full-Heusler alloy thin films have been formed by a RTA technique compatible with CMOS technology[248]. These results are promising for spin-MOSFETs using half-metallic ferromagnetic material for the source and drain. Other types of ferromagnetic source/drain (spin-injector/detector) structures using ordinary ferromagnetic material were also investigated [249,250,251,252].Electrical spin injection, transport, and detection for Si channels have been verified using specific devices, as mentioned above. The half-metallic ferromaget technologies have also been progressed dramatically. In order to demonstrate the potential of spin-MOSFETs, it is important to realize highly efficient spin injector/detector structures matched to spin-MOSFETs through uniting these technologies. It should be noted that spin-MOSFETs require the ferromagnetic source/drain (spin-injector/detector) that not only exhibits a significant magneto-resistance but also satisfies a high device performance as a MOSFET.

An alternative approach for realizing spin-MOSFETs has been proposed[253,254]. A pseudo-spin-MOSFET is a circuit for reproducing the functions of spin-MOSFETs using an ordinary MOSFET and a MTJ that is connected to the MOSFET with a negative feedback configuration. The pseudo-spin-MOSFET can accurately reproduce the spin-transistor behaviors such as variable current drivability. Nonvolatile logic circuits using pseudo-spin-MOSFETs, which are suitable for power-gating systems with low static energy, have been proposed[255,256,257,258].

Recently, experimental demonstration of Datta–Das spin-FET (the original type of spin-FET[259],[260]) was reported[261]. Oscillatory spin signals controlled by a gate voltage were observed implying spin precession of spin-polarized carriers in the channel. However, the origin of the observed spin signals is not yet clear[262,263,264].

4.2.4.5.2. Impact Ionization MOS (IMOS)

Impact ionization based FETs, called IMOS[265,266,267] have been proposed as candidates to achieve an $I_{on} - I_{off}$ current transition steeper that the 60mV/dec limit of MOSFET at room temperature. As for Tunnel FET, the main goal is to achieve a scalable switch that can operate at a voltage supply much lower than CMOS, and thereby lower power dissipation. The IMOS device consists of a gated p-i-n structure operated in the reverse-bias regime, with the gate partially overlapping the intrinsic region. The placement of the gate region with respect to the n+ and p+ regions determines the polarity of the IMOS device (N-IMOS or P-IMOS), which means that complementary devices can be easily be designed and fabricated. In fact, the attractiveness of IMOS was motivated by its potential co-integration with silicon CMOS. The co-integration of Tunnel FETs and IMOS devices with sub-100nm channel length on CMOS-compatible platforms was demonstrated[268] .

[4] *Although an experimental demonstration of a spin-MOSFET was reported, the authors later denied their result. See references 241 and 242.*

The principle of IMOS consists in the control of the impact ionization onset in the gated p-i-n structure. At low values of the gate voltage there is no inversion region under the gate: the effective channel length is the length of the entire intrinsic region and the off current is limited by the reverse leakage current of the p-i-n diode, which can be kept very low. When the gate voltage is increased an inversion region is created and the effective channel length is reduced. At higher V_G an increasing fraction of V_D falls across the impact ionization i-region outside the gate, and the lateral electric field increases; therefore, V_G modulates the avalanche breakdown voltage of the device. IMOS is used in the avalanche mode following the impact ionization regime in order to obtain a very steep increase of current via carrier multiplication. However, avalanche charge multiplication is an intrinsically slow and statistical process with a stochastic nature that could inject additional variability into IMOS device design[269] . Therefore, there is a fundamental limitation on the transient speed of the IMOS because of *carrier multiplication delay* (CMD), which was confirmed recently[270]. Subthreshold slopes of 5mV/dec or less, in combination with Ion > 1mA/μm have been reported in various IMOS embodiments[271,272,273,274,275,276,277] .The smallest experimental value of the subthreshold slope was of 2mV/dec [278] but the voltage applied to the source was V_S=17V. In addition[279] an IMOS with elevated SiGe impact-ionization region for bandgap engineering achieved a swing of 3.2 mV/dec with a source voltage of 8V. It was also suggested that IMOS devices can potentially reduce CMOS inverter switching current by 75% and to improve the static noise margin of 6T SRAM cells by 22% [280].

On the other hand, the high electric field needed to produce impact ionization[281] limits the scaling of the supply voltage to values higher than the bandgap of some materials that would otherwise be good channel replacement candidates. For silicon, the smallest functional device demonstrated 5.3V avalanche breakdown in a 40nm device but with a large leakage current[282]. Practically feasible breakdown voltages in silicon IMOS seems to saturate at short device lengths (below 100nm) and cannot fall under about 4.5 V[283]. Materials with lower bandgap energy than silicon, e.g. Ge and SiGe, have been proposed to build IMOS devices requiring lower voltage supply[284,285,286]. In general, even if IMOS does not suffer from a low on-current common to Tunnel FETs, it has an intrinsic limitation in voltage supply scaling, which is crucial for power consumption reduction. Increased drivability due to higher impact ionization generation rates and reduced breakdown voltages would make the device more scalable and would allow use of germanium in which impact ionization is higher than in silicon. Another intrinsic limitation of IMOS is related to the fact that impact ionization generates hot carriers which induce increased trapping in the gate dielectric[287], and makes IMOS very susceptible to hot carrier degradation. The majority of the IMOS experimental reports deal with devices that cannot be switched more than a few hundreds of times without a degradation of the threshold voltage. Despite some proposed solutions (such as the reduction of the gate oxide thickness, which seems to improve the reliability[288]) to avoid degradation of IMOS characteristics due to highly energetic carriers, the hot carrier issue in IMOS was never satisfactorily addressed. In conclusion, voltage scaling and hot carrier issue can be considered as the main showstopper for IMOS and, consequently, less effort has been paid in the last few years by the research community to IMOS compared to emerging Tunnel FET device architecture. Recently, it was suggested that both IMOS and Tunnel FET can still benefit from a vertical device integration compared to the lateral architectures.

4.2.4.5.3. Negative gate capacitance FET

Based on the energy landscapes of ferroelectric capacitors, it has been suggested[289] that by replacing the standard insulator of a MOSFET gate stack with a ferroelectric insulator of appropriate thickness it should be possible to implement a step-up voltage transformer that will amplify the gate voltage, thus leading to values of S lower than 60 mV/decade and enabling low voltage/low power operation; this device is called a negative gate capacitance FET. The main advantage of such a device[290] is that it involves no change in the basic physics of the FET thus does not affect its current drive or impose other restrictions; thus, high I_{on} levels, similar to advanced CMOS would be achievable with lower voltages. An experimental attempt to demonstrate small swing Fe-FET, based on a P(VDF-TrFE)/SiO_2 organic ferroelectric gate stack was reported at IEDM 2008[291]. However, this particular experiment demonstrated <60 mV/decade only at very low currents (~1nA) that could be prone to noise. A second demonstration[292] was reported at IEDM 2010. This experiment showed <60 mV/decade subthreshold swing at much higher current levels (~50nA) and over a range of few decades of current. In addition, careful measurements were done to properly characterize the noise levels (found to be around ~10pA range). This experiment thus established the proof of concept of <60mV/decade operation using the principle of negative capacitance. In addition, recent demonstration[293] of capacitance enhancement in a series combination of a ferroelectric and dielectric capacitor, composed of single crystalline oxides grown epitaxially, also demonstrates a number of predictions of negative capacitance theory.

The major challenge concerns identification of appropriate materials (ferroelectrics and/or oxides) that can provide the best swing with minimal hysteresis. It was theoretically shown[294,295] that if the negative capacitance can be properly matched with the device capacitance, a very steep swing can be achieved without any significant hysteresis. However,

due to the fact that capacitance varies significantly with voltage for a MOSFET, matching capacitance over a large range of voltage may prove to be challenging. Extremely thin body double gate structures may prove to be useful for this. A second significant challenge comes from the integration of high quality single crystalline ferroelectric oxides on Si. Although, negative gate capacitance FET with organic ferroelectric such as, P(VDF-TrFE)/SiO2 gate stack already has been demonstrated, crystalline oxides are more attractive due to their well-behaved and sharp hysteresis and better dynamic response. One possible pathway could be to use Strontium Titanate (STO) on Si as a template to grow single crystalline ferroelectric materials like PZT on Si. In principle, the scalability of the device should be similar to the one of a MOSFET. However, no study on scalability has been performed as yet.

4.2.4.5.4. NEMS Switch

Micro/Nano-Electro-Mechanical (M/NEM) Switches (or relays) are devices where the operation is based on the displacement of a solid beam under the influence of electrostatic force in order to create a conducting path between two electrodes. M/NEM relays feature two key properties for logic computation which are unavailable in MOSFETs: *zero leakage* and *zero subthreshold swing*[296,297]. The first property indicates zero standby energy dissipation, while the second suggests the potential to scale V_{DD} aggressively (without degrading the on-current to off-current ratio) and hence reduce significantly the dynamic energy consumption as well. Moreover, features such as electromechanical hysteresis and sticking induced by surface forces make NEM relays attractive for non-volatile memory applications[298]. Additional motivations for NEM logic include high-temperature and radiation-hard operation[299] and the possibility of using cheap substrates such as plastic or glass for their fabrication. M/NEM relays can be processed at low temperatures, allowing their co-integration with CMOS. Possible applications of a hybrid NEMS-CMOS technology consist of power gating high-performance CMOS circuits[300] and configuration of CMOS FPGAs[301] using NEM relays. The most recent overview [302] of developments in electrostatic micro-relay design and process technology, suggest that M/NEM switches are attractive for ultra-low-power digital logic applications.

As for MOSFETs, performance of M/NEM switches is improved by constant-field scaling, which increases speed while decreasing dynamic energy dissipation and area[303]. The ultimate device density achievable with NEM switches in principle may be competitive with CMOS due to the simplicity of their structure. The main advantage of M/NEM switches in terms of scaling resides in their *improved energy efficiency* as well as in their potential for 3-D integration, both of which may allow increased functional density for a given substrate real-estate[304]. This is especially true for memory applications[305] where hysteresis and sticking lead to an even better functional density.

M/NEM switches can be fabricated by top-down approaches using conventional lithography techniques or bottom-up approaches using carbon nanotubes or nanowire beams. There are many successful demonstrations using top-down approaches at the micron scale with reliable operation up to 10^8 cycles[306]. In M/NEM switch fabrication, the most critical process step is the beam release (gap formation), which is realized by the etching of a sacrificial material, such as oxide, polyimide, or silicon.

The smallest actuation gap demonstrated so far for a functional NEM structure fabricated using a top-down approach is 15nm[307] . The device consists of a vertically actuated 2-terminal NEM switch featuring a 35-nm-thick TiN cantilever beam that is 300 nm long and 200 nm wide. The pull-in voltage is approximately 13 V. As expected, the off-state current is virtually zero and the sub-threshold swing is practically zero. An endurance of several hundred switching cycles in air ambient is reported. The smallest actuation gap demonstrated to date for a carbon nanotube-based structure fabricated using a bottom-up approach is 40-60nm[308]. Two and three-terminal relays based on LPCVD-grown Si nanowires with ~100nm diameter were also demonstrated[309]. Pull-in voltage was 3.8 V for the 2-terminal NEM switch featuring a 200nm gap, while leakage was virtually zero.

The main advantage of M/NEM relays is their zero off-state leakage and potential for low dynamic energy dissipation, which can be reduced down to the aJ range. Their main weakness is switching speed: a realistic lower limit for the delay related to beam movement from the off position to the on position is ~1ns[310].

Many issues remain to be solved in order to apply M/NEM relays to logic applications. The most important issue is nanoscale contact reliability, since logic circuits would require the relays to operate correctly over ~10^{16} "hot switching" cycles where the drain voltage is as high as the gate voltage. High impact velocity at the end of pull-in and the resultant "tip bouncing" (which also increases the effective switching delay) can aggravate the problem[311] . Another significant issue for NEM relays is the presence of surface forces (van der Waals or Casimir) that can cause sticking if the restoring elastic force is not sufficiently high. Stiction is typically overcome by stiffening the beam at the expense of increasing the pull-in voltage and thus these surface forces often set the minimum energy required to switch a M/NEM relay. In order to minimize stiction and maintain clean contact spots, M/NEM relays should be hermetically sealed.

There are several factors which will eventually impact the dimensional scaling of M/NEM relays. At gaps of a few nm, the subthreshold swing is already expected to degrade due to the onset of tunneling current before the unstable beam position is reached at ~2/3 of the nominal gap. With sufficiently small dimensions and gaps, the effect of Brownian beam motion may become significant; however, stiffening of the beam (*e.g.* by changing the beam material) can allow for further scaling. In relays with gaps near the limit set by tunneling (~2 nm), the long turn-off settling time could cause a significant risk for "short-circuit" current.

Mechanical switches are a relatively mature technology at the micron scale[312,313] and have been shown to be scalable to the nanometer scale[314] .

In conclusion, M/NEM switch technology is an interesting candidate for LSTP applications because M/NEM switches exhibit virtually zero leakage. If the influence of surface forces can be reduced, the steep subthreshold swing of the NEM relay can be exploited to significantly decrease V_{DD} and hence the active power as well. In this context, controlling and minimizing surface forces as well as improving contact reliability are the key requirements and warrant fundamental research. Recent demonstrations of functional relay logic circuits[315] with more than 10x improvement in energy efficiency compared with conventional technology suggests a possible resurgence of mechanical computing for energy-efficient electronics.

4.2.4.5.5. Atomic Switch

The atomic switch is classified as an electrochemical switch using the diffusion of metal cations and their reduction/oxidation processes to form/dissolve a metallic conductive path[316], similar to Resistance Random Access Memories (ReRAMs) in which oxygen vacancies are controlled to make a conductive path[317]. The difference appears in their respective electrode materials. The atomic switch has a reversible electrode for introducing metal atoms (cations) into the ionic conductive materials[318], and is both experimentally[319] and theoretically[320] confirmed. On the other hand, both electrodes of ReRAMs are inert and use oxygen vacancies to enable formation of a conductive path.

The atomic switch was initially developed as a two-terminal device using sulfide[321,322,323,324,325] materials that was embedded in a crossbar architecture[326] with scalability down to 20 nm[327,328]. Later, an atomic switch using fully CMOS compatible materials was developed to enable the formation of these devices in the metal layers of CMOS devices[329,330,331,332,333,334,335]. This configuration resulted in the development of new type of programmable logic device[336,337].

One advance in this field was development of three-terminal atomic switches[338,339], characterized by high I_{on}/I_{off} ratio, low ON-resistance, nonvolatility, and low power consumption. Several operating mechanisms have been proposed, including gate-controlled formation and annihilation of a metal filament[340], and gate-controlled nucleation of a metal cluster[341]. The latter mechanism can be utilized for volatile operation by controlling the metal cation density to be less than that required for nucleation of stable clusters.

The long retention time of the metal filament has been confirmed[342]. Switching time is of the order of ns[343,344] and the switching repetition of 10^{11} times have been confirmed by the two-terminal atomic switches[345] . High I_{on}/I_{off} ratio (10^8) and low power consumption (pW) have been demonstrated using the three-terminal atomic switches[346].

Switching speed, cyclic endurance, uniformities of the switching bias voltage and resistances both for the on-state and the off-state should be improved for general usage as a logic device. Although basic phenomena in their switching have been reported[347], establishment of the device physics still seems to be the most important and urgent issue. In addition, development of the architecture for nonvolatile devices is desired same as with other nonvolatile logic devices.

4.2.4.5.6 MOTT FET

Mott field-effect transistor (Mott FET) utilizes a phase change in a correlated electron system induced by a gate as the fundamental switching paradigm[348,349]. Mott FETs could have a similar structure as conventional semiconductor FET, with the semiconductor channel materials being replaced by correlated electron materials. Correlated electron materials can undergo Mott insulator-to-metal phase transitions under an applied electric field. Besides electric field excitation, the Mott phase transition can also be triggered by photo- and thermal-excitations for potential optical and thermal switches. The Mott FET structure has been explored with cuprate oxide channel materials[350] Among several correlated materials that could be explored as channel materials for Mott FET, vanadium dioxide (VO_2) has attracted much attention recently due the sharp metal-insulator transition temperature (nearly five orders in single crystals) and above room temperature transition at ~340 K[351]. The phase transition time constant in VO_2 materials is in sub-picosecond range determined by optical pump-probe methods[352]. Elementary device simulations indicate that the VO_2-channel-based Mott FET lower bound switching time is of the order of 0.5 ps at a power dissipation of 0.1 μW[353]. VO_2 Mott channels have been

experimentally studied recently with thin film devices and the field effect has been demonstrated in preliminary device structures[354,355,356]. Experimental challenges with correlated electron oxide Mott FETs include fundamental understanding of gate oxide-functional oxide interfaces and local bandstructure changes in the presence of electric fields. Understanding the electronic arrest mechanisms while de-coupling from structural Peierls distortions is of interest. While the electric field-induced transitions are typically explored with Mott FET, nanoscale thermal switches with Mott materials could also be of substantial interest. Recent simulation studies of "ON and "OFF" times for nanoscale two-terminal VO_2 switches indicate possibility of sub-ns switching speeds in ultra-thin device elements in the vicinity of room temperature and could also be of interest to Mott memory[357]. One can in a broader sense visualize such correlated electron systems as 'threshold materials' wherein the conducting state can be rapidly switched by a slight external perturbation, and hence lead to potential applications in electron devices. Electronically driven transitions in perovksite-structured oxides such as rare-earth nickelates with minimal lattice distortions would also be of relevance in this regard.[358,359]

4.2.5. ALTERNATIVE INFORMATION PROCESSING DEVICES

4.2.5.4. Non-FET, Non Charge-based "Beyond CMOS" Devices

4.2.5.4.1. Spin Wave Device

Spin Wave Devices (SWD*)* are a type of magnetic logic exploiting collective spin oscillation (spin waves) for information transmission and processing. The primary expected advantages of SWDs are (i) the ability to utilize phase in addition to amplitude for building logic devices with a fewer number of elements than required for transistor-based approach; (ii) non-volatile magnetic logic circuits, and (iii) parallel data processing on multiple frequencies at the same device structure by exploiting each frequency as a distinct information channel. SWDs consist of two major components: magneto-electric (ME) cells and magnetic waveguides (spin wave buses)[360]. The ME cell is a multi-functional element (e.g. multiferroic) used for spin wave excitation, detection, and information storage. Input data are received in the form of voltage pulses applied to the input ME cells to generate spin wave signals. The excited spin waves are of the same amplitude, while logic 0 and 1 are encoded into the initial phase (0 or π). Next, spin waves propagate through the spin wave buses and interfere at the points of junction constructively or destructively, depending on the relative phase. The amplitude of the propagating wave is amplified by the ME cells via magneto-electric coupling[361]. The result of computation can be stored in the magnetization or converted into the voltage pulse by the output ME cells.

During the past five years, several prototype devices exploiting spin wave interference (but without ME cells) have been experimentally demonstrated[362,363]. The prototypes operate at room temperature and at GHz frequency. Currently, the major work is focused on the integration of spin wave buses with ME cells and the demonstration of non-volatile magnonic logic. Among a number of technical challenges, the most critical ones are associated with the development of multiferroic elements with strong magneto-electric coupling and GHz frequency operation.

4.2.5.4.2. Nanomagnetic Logic

Nanomagnetic Logic consists of fringing field interactions between magnetic islands that are used to perform Boolean logic operations[364]. Binary information is represented via magnetization state. Nanomagnet logic (NML) also appears to be scalable to the ultimate limit of using individual atomic spins[365]. Presently, five fundamental tenets[366] that a device must satisfy for use in a digital system have been experimentally demonstrated for NML: a device should enable a functionally complete logic set[367 368,369], have non-linear response characteristics[370], the output of one device must drive another, power amplification (or gain) is needed (see fanout[371]), and dataflow directionality must be well defined[372].

A clock modulates the energy barriers between magnetization states in an NML circuit[373]. Nearly all fabricated NML circuit ensembles have been "clocked" with an external magnetic field. Recently, experimental demonstrations of individual island switching[374], as well as the re-evaluation of NML lines and gates with CMOS compatible clock structures[375] have been reported (fields are generated with a metal line clad with ferromagnetic material[376]). Multiferroic materials[377,378] are also being investigated, and could represent an electric field based approach to clocking.

To interface with transistor-based circuitry, a magnetic-electrical interface is needed. Two designs where fringing fields from an NML device are used to set the state of the free layer in a magnetic tunnel junction have been proposed[379]. These designs (and variants thereof) are (a) active experimental targets, and (b) could be repurposed for input (spin transfer torque would *set* the state of the free layer). A simple biasing line[380] and multiferroic materials are alternative input mechanisms.

Research has begun to consider how NML ensembles might behave given the effects of thermal noise, clock field misalignment, lithographic variations in individual islands, and combinations thereof. Notably, work from 2008 suggests that in a soliton operating mode, dipole-to-dipole coupling could be insufficient to prevent thermal noise from inducing

premature/random switching[381]. It has been suggested that devices with a magnetocrystalline biaxial anisotropy be used to introduce a local minimum in the energy landscape of an individual magnetic island, and further promote hard axis stability of an ensemble[382]. Alternatively, adiabatic switching[383] and/or field gradients could potentially mitigate the effects of premature switching. Simulations suggest that NML circuits could tolerate some field misalignment[384,385]. Whether or not a circuit ultimately exhibits reliable and deterministic switching is very much a function of how it is clocked – and requires much additional study.

In CMOS systems, the ability to route signals in multiple layers of metal is essential for creating local interconnections between individual logic gates and/or functional units. Because information is moved via fringing field interactions in NML, any type of wire crossing would presumably need to occur "in-plane." Simulations of candidate designs have been successfully performed[386]. In principle, signals could be routed in multiple planes, or converted to the electrical domain for intermediate and/or global communication. As larger, n-bit systems evolve, this topic requires more study.

4.2.5.4.3. Excitonic Field Effect Transistor

The Excitonic field-effect transistor (ExFET) as currently envisioned allows for an ultra-steep inverse subthreshold slope (S) by the creation of an energy gap through the gate controlled formation of an excitonic insulating state. While in the on-state, charge is the relevant state variable as in a conventional FET, the state variable characterizing the device off-state is an excitonic insulator that is formed through the interaction between two oppositely doped parallel segments of a device channel as schematically depicted in Figure ERD3 Coulomb interaction between electrons in the n-type branch and holes in the p-type branch allows condensation of the system into an excitonic phase under certain gate voltage conditions. This in turn opens an energy gap in the single particle excitation spectrum. Recombination of electrons and holes is suppressed through the spatial separation of charges with opposite polarity. Since the gate field is used to create a previously non-existent energy gap to suppress current flow from source to drain, the above limitation of S no longer applies and low-power device operation becomes feasible. The device switches as a function of V_{gs} from a highly conductive state into the off-state once the conditions for the formation of an insulating excitonic phase are satisfied.

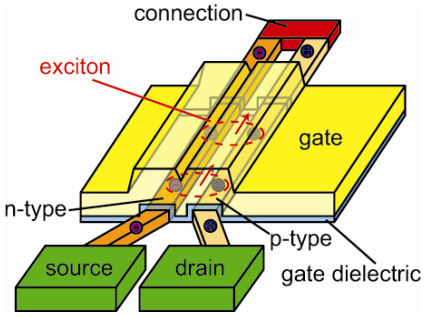


Figure ERD3 Schematic layout of the excitonic field-effect transistor (ExFET).

In the 1970s, so-called direct excitons were theoretically discussed in the context of bulk (3D) materials forming an insulating state[387,388,389,390,391,392]. It was not until 1988 that an excitonic insulator was experimentally verified [393,394,395,396,397]. Typical excitonic binding energies in these systems are of the order of several meV[398]. Exciton formation between spatially separated electrons and holes was predicted in 1985[399]. Optical experiments were used to prove the existence of an excitonic state in these two-dimensional (2D) systems[400,401,402], and theoretical work predicts a phase transition to an excitonic insulator[403], or a crystalline state[404]. Indirect exciton formation was also predicted for one-dimensional (1D) nanowires[405]. In 1D systems – as carbon nanotubes – excitonic binding energies of the order of several 100meV have in fact been experimentally verified supporting the notion of room-temperature operation of the proposed ExFET[406,407].

4.2.5.4.4. BiSFET

The bilayer pseudo-spin field effect transistor (BiSFET) is a recently proposed concept for an ultra-low-power and fast transistor[408] based on the possibility of a room temperature exciton (paired electron and hole) superfluid condensate in two oppositely charged (n-type and p-type) layers of graphene separated by a thin dielectric.[409] In the detailed analysis, electron occupation of the top layer or bottom layer can be treated much like spin up or down, that is as a pseudospin, and the collective effects considered here are analogous to collective spin effects in a ferromagnet. What separates this graphene system from that of adjacent III/V semiconductor quantum wells where ultra-low temperatures and high magnetic fields are required to observe such condensates[410,411,412,413] is a synergy of favorable graphene properties: atomically thin layers, symmetric electron and hole band structures, low density of states and zero bandgap energy.

The condensate allows an enhanced interlayer current between the separately contacted graphene layers to flow up to some critical current, beyond which the condensate collapses, producing a negative differential characteristic with respect to the interlayer source-to-drain voltage.[414,415,416] This critical interlayer current can be reduced via a gate-induced charge imbalance.[417,418,419] The resulting device output characteristics are qualitatively similar to those of gated resonant tunneling diodes (RTDs). However, the conductance is intrinsically maximized at a zero source-to-drain voltage and, crucially, the source-to-drain voltage associated with the critical current can be smaller than the thermal voltage k_BT/q,

allowing for very low voltage—perhaps on the scale of k_BT/q—and low power operation. Prototype inverters, based on a simple BiSFET device model and simulated with SPICE, have exhibited switching energies per device of approximately 10 zeptojoules (10^{-20} J).[420,421] And because it remains charge based, even if dependent on collective pseudospin effects internally, there is no need to convert between state variables for use with conventional CMOS.

However, because the BiSFET output characteristics are much different than those of MOSFETs, logic circuits must work in a different manner, more akin to that proposed for the afore-mentioned gated RTDs[422] than to CMOS, including the use of a four-phase clocked power supply. Nevertheless, highly energy efficient circuits have so far been simulated for all basic logic functions[423] through ripple-carriers adders[424] at a 100 GHz clock frequency.

The BiSFET, however, remains only a concept based on novel predicted physics within a novel material system. And fabrication of BiSFETs with the necessary degree of control of graphene, dielectric and surface quality, of work functions, and of lithography, etc. imposes numerous challenges. Issues relating to BiSFET fabrication, some of them unique to this system and others common to other graphene techanologies, as well as theory are currently being addressed.[425]

4.2.5.4.5. Spin Torque Majority Logic Gate

Spin torque nano-oscillators (STNOs) are nanomagnetic voltage-controlled oscillators operating in the microwave frequency range. The oscillators make use of the spin transfer torque effect in nanoscale all-metallic spin valves and magnetic tunnel junctions[426]. Direct voltage applied to a STNO generates spin transfer torque and induces auto-oscillatory precession of the magnetic moment of the spin valve free layer. Precessing magnetization generates alternating voltage in the microwave frequency range due to either giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) effects[427]. The frequency of the precessing magnetization is tunable by the applied dc voltage due to strong non-linearity of the STNO. When several STNOs share a common extended free layer, spin waves propagating in the free layer provide coupling between the STNOs, which can give rise to frequency and phase locking of the STNO dynamics[428,429]. In this phase locking regime, each STNO generates microwave radiation with the same frequency and phase. The frequency band of phase locking can be very large in STNOs due to their strong nonlinearity[430].

A majority logic gate based on phase locking of STNOs consists of a common free-layer metallic ferromagnetic nanowire on a metallic nonmagnetic bottom lead with several GMR or TMR junctions patterned on top of the free layer[431]. One of these junctions can serve as the gate output while the rest of the junctions are the gate inputs. All inputs are dc current-biased at a current level above the critical current for magnetization self-oscillations. To each input, signals of two frequencies f_1 and f_2 can be applied. Due to injection locking and spin wave interaction in the common free layer, the entire free layer precesses at either f_1 or f_2, depending on the input signal frequency applied to the majority of the inputs. Therefore, the output frequency of this logic gate is determined by the frequency applied to the majority of the input gates, and the device operates as a majority logic gate with the signal frequency as the state variable.

Another type of spin torque majority logic gate is based on spin torque switching[432] in a multi-terminal magnetic tunnel junction. Spin torque from direct current can result in switching of the direction of magnetization of the free ferromagnetic layer of the tunnel junction, which results in switching of the tunnel junction resistance between high (free layer antiparallel to the pinned layer) and low (free layer parallel to the pinned layer) resistance states. This type of majority logic gate is a five-terminal device with three inputs, one output and a common ground[433]. The three inputs and the output are nanoscale magnetic tunnel junctions making contact to a grounded ferromagnetic free layer shared by all the inputs and the output. The output of the majority gate assumes the logic state ("0" low resistance state or "1" high resistance state) dictated by the polarity of the voltage applied between the majority of the three inputs and the ground. Magnetization of the common free layer is switched by spin torque to a state determined by the polarity of the majority (at least 2 out of 3) of currents passed between the inputs and the ground. The stack of layers in STMG with in-plane magnetization is similar to that in a typical magnetic tunnel junction[434], although the inputs are represented by separate nanopillars electrically isolated from each other. Spin Torque majority gate devices are intrinsically non volatile and offer performance advantages relative to conventional CMOS in low duty factor and normally off applications. A key challenge is to reduce the current required to induce magnetic switching.

4.2.5.4.6. All Spin Logic

The recently proposed concept of all spin logic (ASL)[435] uses magnets to represent non-volatile binary data while the communication between magnets is achieved using spin currents in spin coherent channels with the energy coming from the power supply. The ASL concept is based on key scientific advancements of the last decade [436,437,438,439,440,441,442,443]. These advancements have blurred the distinction between spintronics and magnetics, creating the possibility of a device capable of providing a low power alternative to charge-based information processing. In particular, the two key recent

advances are (1) the demonstration of spin injection into metals[444,445,446] and semiconductors[447,448,449,450] from magnetic contacts and (2) the switching of a second magnet by the injected spins [451,452]. These demonstrations suggest an all-spin approach to information processing. Magnets inject spins and spins turn magnets (digital bits) forming a closed "ecosystem" which takes advantage of both analog (spin currents) and digital (bistable magnets) properties without the need to convert to charge. It has been shown that ASL can potentially reduce the switching energy-delay product[453] by a significant amount, but there are major challenges to be overcome. One is the room temperature demonstration of switching in multi-magnet networks interacting via spin currents. The other is the introduction of high anisotropy magnetic materials [454] into relevant experiments which can improve energy-delay. Issues such as current density and proper choice of channel materials also have to be carefully considered. The analog nature of ASL communication can be efficiently coupled with median function[455] to develop an architecture called Functionality Enhanced ASL (FEASL) to realize low-power, lower delay and lower area circuits. FEASL is especially suited for adder and multiplier circuits which are an integral part of arithmetic logic units (ALU). Moreover, it should be mentioned that ASL could also provide a natural implementation for biomimetic systems with architectures that are radically different from the standard von – Neumann architecture.

4.3 MORE-THAN-MOORE DEVICES

4.2.5.4.7. Introduction

In recent years in this "Emerging Research Devices" chapter, the ITRS focused on "information manipulation, transmission, and memory" (*i.e.*, the "More Moore" domain) with the charter "to survey, assess, and catalog viable emerging research devices for their long-range potential, technological maturity, and to identify the scientific/technological challenges" of getting them accepted by the semiconductor industry. The figures of merit of such devices are expected to surpass substantially the ones of existing technologies. Over time the list of potential candidates evolves either when a device is mature enough to transition to more industrial development or to less attention, in acknowledging lack of significant progress towards potential displacement of a more standard technology. Owing to the growing attention on the "More-than-Moore" domain, the charter of the ERD chapter is extended to the non-digital domain.

Most of the published nano-enabled devices pertain to the fields of photonics, energy, (bio)chemical sensors and to the RF domain. Considering the need of benchmarking these emerging devices with existing non-digital technologies already addressed by the ITRS, the first step of this extension is focused on RF emerging devices which could eventually transition to the "RF and A/MS Technologies" chapter. Further extensions to other non-digital emerging devices will be made according to the development of such topics in the other ITRS chapters.

The approach chosen follows the methodology outlined in the ITRS "More-than-Moore" White Paper [5] (see Figure ERD4 below). A generic high-level function in wireless communications is the RF front-end block which translates the incoming modulated electromagnetic wave into a digital stream of information: this function can be partitioned into generic lower-level functions like antenna, switch, filter, local oscillator, mixer, etc. which in turn could use generic devices like RF transistors, mechanical filters, etc. It should be stressed that a single device can fulfill higher-level functions. That is why it is important to start from the functional analysis and not try to replace existing devices tuned to a very specific underlying architecture.

[5] *http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf*

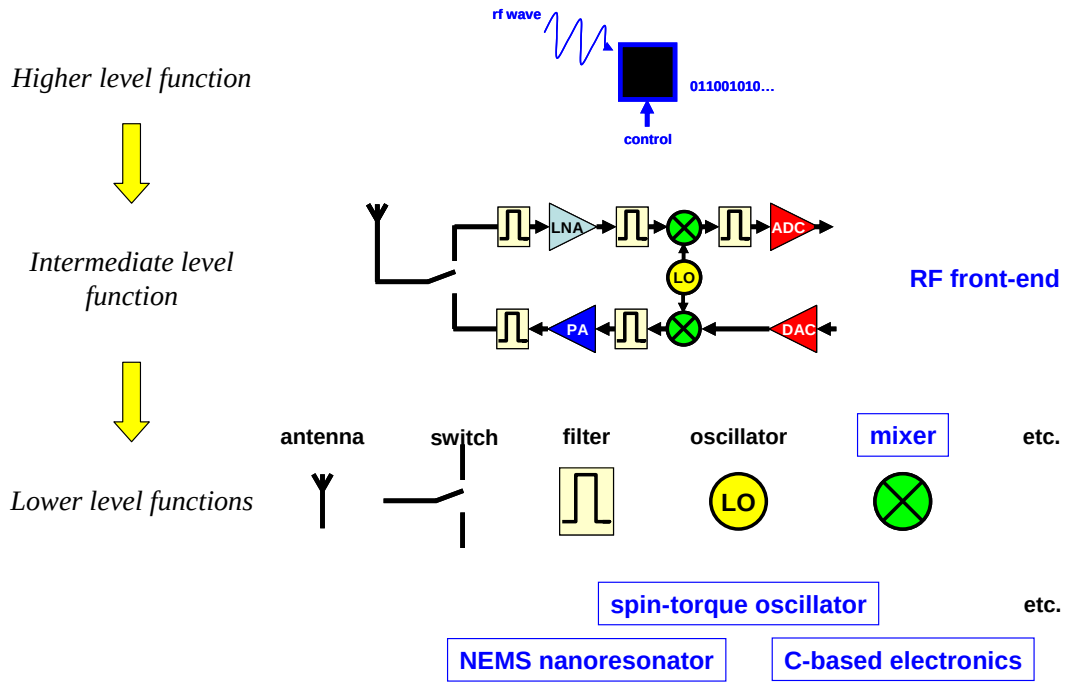


Figure ERD4 A Taxonomy for Emerging Research Information Processing Devices (The technology entries are representative but not comprehensive.)

In this first attempt to address the wide field of "More-than-Moore" emerging RF devices, this section is focused on a few devices and functional blocks. Carbon-based RF transistors – and more specifically graphene-based RF transistors – will be considered first as potential replacement of existing RF transistors. Then some functional blocks using emerging research devices will be explored, namely oscillators using spin transfer torque, mechanical resonators, and mixers. In assessing these devices, only few reliable data are available to benchmark them with respect to more classical solutions: the semiconductor community is highly encouraged to refer to the relevant figures of merit and measurement methodologies as detailed in the "RF and A/MS Technologies" chapter.

4.3.1. GRAPHENE RF TRANSISTORS

Owing to the potentially very high carrier velocity of graphene, RF transistors using this material possibly can reach very high unity current gain cutoff frequency, f_T: graphene RF transistors have been reported with higher f_T and lower f_{Max} than Si transistor at the same gate length. The maximum cutoff frequency reported for graphene is 300 GHz using Co_2Si-nanowire gate and an exfoliated graphene.[456] A f_T of 240 GHz was reported using wafer scale epitaxial graphene[457] and a f_T of 200 GHz was reported using a CVD-grown graphene layer[458]

To obtain higher f_T, the device configuration needs to be optimized. The source and drain of the graphene transistor are usually defined by depositing a metal film, which can induce parasitic capacitances: in top-gate configuration, where source, drain and gate are on the same side of graphene channel, gate-source or gate-drain capacitances can be large, which results in a reduced f_T. However, in back-gate configuration, where the gate is on the opposite side of the graphene layer than the source and drain, the gate-source or gate-drain capacitances could be lower even for an overlapped situation (L_{gs}<0). CVD graphene can be fabricated easily on the back-gate configuration; epitaxial graphene could not. Methods to fabricate a local embedded back gate on a SiC wafer are, however, suggested, although high growth temperature could make it difficult[459]

Since the cutoff frequency is inversely proportional to the channel length, the limit of f_T in graphene transistor has not been fully assessed by the reported wafer scale devices. Using a nanowire gate instead of a patterned metal, f_T was

estimated down to a 45 nm channel length based on transition time. High Fermi velocity of carriers in graphene, resulting in high drift velocity (~ 4 x 10^7 cm/s) in a channel, makes 1THz f_T achievable for a sub-70 nm channel length device[460]. This is greater than sub-30 nm channel length of HEMT and Si RF transistors[461].

The unity power gain frequency or maximum frequency of oscillation, f_{Max}, which is around 10-50 GHz even for devices with f_T of 200 GHz, could be increased by improving the device structure and reducing the parasitics. This is a field which is presently less investigated than the intrinsic properties of graphene.

4.3.2. SPIN TORQUE OSCILLATORS

Spin transfer torque in metallic spin-valves and magnetic tunnel junctions using nano-sized magnetic multilayer structures can drive uniform precession of the free layer magnetization under external magnetic field conditions[462,463]. When combined with the giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) effect, this precession produces voltage responses that make those magnetic multilayers high frequency spin torque oscillators. The oscillation frequency in a spin torque oscillator can be tuned by adjusting the electric current or the external magnetic field. Due to its high compactness, extremely wide tunability, and compatibility with standard CMOS process, spin torque oscillator has the potential to be an agile RF oscillator[464,465]

Currently, oscillation frequencies ranging from several hundred MHz to tens of GHz have been demonstrated depending on the magnetic structures, magnetic field and input current levels[466] . The output power in spin torque oscillators based on metallic spin valve structures is about several hundred pW and it was improved up to about tens of nW in MTJ based spin torque oscillators[467,468]. Despite these experimental advancements in spin torque oscillators, there are several challenges to be overcome for the practical application of spin torque oscillator. These challenges include 1) auto-oscillation structures, 2) increase of output power, and 3) high spectral purity (low phase noise).

Auto-oscillation structures are required to eliminate the need for an external magnetic field that is used in most recent experimental demonstrations. Spin torque oscillator structures with a perpendicular polarizer and a planar free layer[469], vortex magnetization state in free layer[470], and wavy angular dependence of spin torque[471] have been suggested.

For the spin torque oscillator to be useful, the output power of RF oscillation should be improved above a few microwatts. Although achieving higher magnetoresistance (MR) ratios through high spin polarization of magnetic layers or large precession angle of free layers could be a first approach for higher output power, phase locking of many weakly coupled oscillators is further needed for a sufficient increase of the output power. Many theoretical predictions and experimental demonstrations of synchronization of electrically connected spin torque oscillators have been reported so far[472,473,474].

Among the remaining challenges, obtaining spectral purity that is compatible to the levels of existing current oscillator devices may be the biggest obstacle for the spin torque oscillators to be applied in the telecommunication field. Issues in the spin torque oscillation linewidth are reportedly coming from the lack of temporal coherence[475] and from the non-linearity of the oscillation frequency[476,477]. The adoption of PLL circuits and synchronization of several spin torque oscillators can be one of the solutions for the higher spectral purity.

4.3.3. NEMS Resonators

There is an increasing interest to miniaturize and integrate the off-chip RF components, especially the quartz crystal used in the reference oscillator whose quality factor Q (>10^4-10^5) and temperature stability (better than 1 ppm/°C) are difficult to achieve with integrated devices. The quality factors of integrated LC-tank circuits are limited by the poor quality factor values of integrated inductors and capacitors (from 10's to 100's). As a consequence, the most promising solutions to miniaturize reference oscillators with uncompromised quality factors[478] are related to the classes of vibrating devices.

Among the most promising of these vibrating structures are the *capacitively transduced micro- and nano-electro-mechanical (M/NEM) resonators*. In recent years tremendous progress has been achieved in the frequency x quality factor product, the main figure of merit for MEM/NEM resonators. The general trend of increasing their resonance frequency to values exceeding the GHz domain pushed such resonators towards very small, very stiff and low mass NEM systems. However, their ability to conserve a high-Q at low dimensions is questionable when the main energy dissipation mechanisms are the gas friction, the clamping and surface losses[479]. Another important issue is how the (in)stabilities of these resonators scale with dimensions as the effects of fluctuations in numbers of photons, phonons, electrons and adsorbed molecules can significantly affect the noise characteristics[480]

4.3.3.1. NEM resonators based on silicon nanowires, carbon nanotubes and graphene

At micrometer scale, recent successful demonstrations of very high frequency resonators are the extensional wine-glass resonators with frequencies ranging from 400 MHz to 1.5 GHz (and Q > 3700)[481] and the dielectrically actuated and piezoresistively sensed 4.41 GHz silicon bar resonator exploiting internal dielectric actuation[482]. Piezoresitive sensing[483] of capacitively actuated resonator exceeding 4GHz with Q>8000 and using the 9th harmonic longitudinal model was implemented.

Very high frequency (VHF) NEM resonators were described using platinum nanowires, resonating at frequencies higher than 100MHz and with a quality factor of 8500 at 4K[484]. The same group later reported[485,486] VHF NEM resonators based upon single-crystal Si nanowires.

Carbon nanotubes attracted major interest for building NEM resonators, due to their high stiffness (Young's Elastic Modulus, E, near 1Tpa), low density, defect-free structure and ultra-small cross section. Resonator responses have been[487] reported varying from 3 to 200MHz with voltage-tunable characteristics, in CNTs with 1-4nm in diameter, suspended over a trench. The NEM resonator with resonance frequencies up to ≈ 4 GHz were reported with a similar CNT device loaded in an abacus style with inertial metal clamps, yielding very short effective beam lengths[488,489].

One issue of such small vibrating SiNWs and CNTs is the early onset, at very low applied power, of non-linearities characterized by frequency bistability arising from the effect of tension built-up in the wire at large vibration amplitudes.

Recently, graphene material attracted further attention for its extremely high strength, stiffness, and thermal conductivity along the basal plane. In Ref.[490] exfoliated graphene sheets are suspended to form two-dimensional NEM resonators with resonance frequencies from 1MHz to 170MHz.

4.3.3.2. NEM resonators based on resonant gate or vibrating body transistors

The capacitively transduced signals of MEM resonators are very small and the impedance matching can be limiting. The movable gate and body FET transistor structures can operate as M/NEM resonators, with the main difference that the output is the drain current of the transistor, offering the possibility of building active resonators.

Resonant gate transistors were reported with out-of-plane AlSi resonant gate MOSFETs[491,492]and with in-plane resonant silicon gate transistors[493]. Aggressively scaled versions of the in-plane resonant gate transistors have been reported[494] based on Silicon-On-Nothing technology to achieve sub-100nm gaps and 400nm-thick single crystal resonators with a front-end process. The lateral MOS transistor could suffer from poor carrier mobility due to the roughness of the vertically etched sidewalls and have shown very little gain, but can be integrated with advanced CMOS[495] to minimize the influence of parasitic capacitances.

An alternative resonant transistor, called Vibrating-Body FET (VB-FET) has been proposed[496,497]; the movable body modulates both the inversion or accumulation charge in the lateral channels and the piezoreistance of the structure (carrier mobility and mass). Silicon nanowires show an unusually large piezoreistance effect compared with bulk Si. An outstanding gain of more than +30dB for the output signal was obtained in micrometer scale double-gate VB-FET when the output is taken from the transistor drain. Moreover, the device motional resistance is reduced from 16kΩ to below 100Ω, which enables excellent conditions for 50Ω matching in RF applications.

Another active resonator has been proposed[498] by using the mechanical strain rather than an electric field to modulate the conductivity of the silicon. This resonator can provide a gain higher than unity at 15MHz, similarly to the VB-FET.

4.3.4. RF MIXERS

An RF mixer is an important building block of the RF front end and many emerging solutions seek attention[499]

Resonant tunneling diodes were explored for decades. Owing to their negative differential resistance and fast response, they had some potential in the RF domain, and subharmonic mixers were demonstrated[500,501]. The potential advantages of such an approach are a wide range of operating temperature, frequencies ranging up to 10 THz, and a reduced noise figure due to RTD shot noise suppression. While this field wasn't very active in the recent years it could regain interest due to the increased demand for THZ applications and the coming integration of III-V materials on Si.

For the same reason single electron transistors were considered with resonant frequencies in the range 1 – 10 GHz. A SET-based mixer with fully tunable band selection from 0 to 300 MHz was demonstrated but at cryogenic temperature[502,503].

Recently the ambipolar I-V characteristic of the graphene transistor which mimics the response of full-wave rectifier has been used to demonstrate a frequency-doubler circuit[504,505].

Finally the nonlinear I-V characteristic of a carbon nanotube can be used to demodulate AM signal. However the demonstrations were limited to <100 kHz due to the external bias circuitry and to <2 GHz due to intrinsic parasitics (chip bond pads, etc.)[506,507].

5. EMERGING RESEARCH ARCHITECTURES

The objective of the ERA section is to identify possible applications for emerging research memory and logic devices. This is a difficult challenge because in many cases, circuit-level models and/or architecture-level models for these devices and their interconnect systems either do not exist or they are very primitive. Moreover, the envisioned applications for these new devices can take many forms; i.e., i) as a drop-in replacement for conventional circuits, ii) as supplemental devices that complement and coexist with CMOS devices, or iii) as devices whose unusual properties can provide unique functionality for selected information processing applications. With this in mind, this section has been organized to reflect the potential application space for emerging research devices from an architecture perspective. Section 5.1 is focused on the application of emerging devices in conventional computing. Section 5.2 addresses evolved architectures that still exploit conventional computation paradigms. Section 5.3 is focused on utilizing emerging devices in "morphic" computing paradigms, i.e. computing not based on conventional approaches but approaches that are inspired by other paradigms, such as neuromorphic computing.

5.1. EMERGING MEMORY ARCHITECTURES IN "CONVENTIONAL" COMPUTING

5.1.1. INTRODUCTION

In traditional computing, SRAM is used to build caches, while DRAM is designed to refill a uniprocessor cache as fast as possible. Furthermore, the entire system image is stored in a non-volatile medium, traditionally a hard drive, and swapped to and from memory as needed. Solid State non-volatile storage (flash) has enabled cost effective small disk-drive replacements especially for portable applications. Some ASICs employ SRAM as local, fast managed store, and occasionally use Content Addressable Memories (CAM). FPGAs use SRAM to build look up tables for small logic and to program look-up tables.

However, this situation is changing rapidly. With continued scaling, application needs are also scaling, as well as evolving, and are rapidly exhausting the capabilities of the traditional memory hierarchy. Simultaneously, new memory technologies create opportunities to solve these problems and create new memory hierarchies. The main objective of this section is to explore this landscape.

5.1.2. CHALLENGES IN MEMORY SYSTEMS

Table ERD13 presents a summary of memory needs by application space. The table is organized as a cross-matrix of application drivers indexed against desired memory properties. It is not indexed by year but is meant to be read in the context of computing in the 2012 – 2020 timeframe. Before proceeding, a discussion of memory properties follows:

- Size. The size of the potential working memory space, given in Bytes. The size is important to understand the cost and power ramifications.
- Speed. Read and write access times are important, but this row presents any "unusual" requirements.
- Power Consumption. The overall average and peak power consumption of the memory system is important in sizing system power delivery and cooling.
- Power Proportionality. Many computer systems are not running at peak load continuously. This row addresses the potential need for the memory system power to be proportional to actual load.
- Persistence. There is often a need for the memory state to persist when the system is turned off, or the power supply quickly moved. Persistence can also be useful for achieving power proportionality.
- Associativity. Some applications benefit from having associative memories, i.e. content addressability.

- Cost. While cost effectiveness is obvious, are there any specific cost considerations?

The application spaces summarized are as follows:

- Multicore. This column represents continued scaling of today's multicore computers aimed at personal and departmental needs.
- Data. Data based processing supports primarily cloud based services, especially analytic services that span multiple computers or locations. Examples include searching, cloud storage, and the provision of complex data-driven services. This sector is fast growing and evolving rapidly.
- Exascale. The next generation of scientific super computers will be operating in the ExaFlop and ExaByte range. (Exa = 10^{18}.) While the codes for scientific computing are fairly well established, the demand for computation is very large.
- Mobile. The fastest growing consumer computer segment is in mobile devices. These are tending towards being multicore systems with complex operating environments.
- ASIC. Specific applications, such as networking and signal processing continue to require evolved memories.

The needs of these applications, and how they potentially relate to emerging memory devices, are discussed in the next few paragraphs.

5.1.2.1 Multicore Computing for Personal and Departmental Use.

The issues in multicore computing are generally well understood, and are largely continuations of existing trends, and thus won't be discussed here. As the number of cores and simultaneous threads grow, the need for additional support for multi-threading will continue. If DRAM scaling ends as anticipated, a DRAM replacement would be valuable. This replacement would need to achieve DRAM read and write speeds (< 100 ns), while having high write endurance (beyond 10^{15} cycles.) Persistence would be valuable for the purposes of reducing the power overhead of memory refresh, or permitting instant powering down and up (e.g. as in Ref.[508]).

5.1.2.2 Research Database Computing in the Cloud.

Database computing has several characteristics that make it clearly distinctive from personal, departmental and supercomputing. These characteristics are well explained in references [Ref.[509]] and [Ref.[510]], and will only be summarized here. The potential for emerging research memories to replace or supplement existing memory technologies is very high and has lead to several proposed emerging architectures, referred to as Storage Class Memory (SCM)[511] or Nanostores[512] . Database computing takes many forms and is evolving rapidly. Some common memory requirement characteristics include the following:

- Scale. The total memory required for a particular application can easily be in the PetaByte (10^{15} B) range and is growing rapidly.
- Residence. Many applications benefit from a large portion of database permanently residing in DRAM. For example, it is widely reported that Google keeps all of its indexing data in DRAM while Facebook keeps 75% of its non-image data in DRAM.
- Data Access Patterns. Data access patterns can vary substantially across the industry. While some companies continue to use relational databases, others have switched to flat databases that must be separately indexed to create connections amongst entries. In general, database accesses tend to be fairly atomic (i.e. small – maybe a few Bytes), and can be widely distributed across the entire database. This is true for both reads and writes, and the relative ratio of reads and writes varies widely by application. Low-cost associative memories could potentially provide benefit in some database types, though this potential is little explored.
- Cost of Ownership. It is useful to consider the total cost of ownership and not overly focus on the specific contributors. The current cost-to-purchase trends are that High Density Disk (HDD) costs roughly an order of magnitude less per bit than flash memory, which in-turn costs almost an order of magnitude more per bit than DRAM[513] . Few cost models exist for emerging memories but it is anticipated that ReRAM and emerging multi-bit vertical flash structures will further close the cost gap with HDD. However, for read intensive applications, it is important to realize that NVRAM will consume considerably less power than HDD, and take up considerably less floorspace. In [Ref.[514]] the authors predict that a ~2020 data center main storage system, performing at 8.4 G-SIO/s will consume 93 MW, if built with HDD, and only 4 kW if built with emerging memories, while

consuming 98,568 sq.ft. of disk space if built with HDD, and only 12 sq.ft. if built with emerging memory devices. Given the cost of energy, this differential can easily shift the total cost advantage to emerging memory, away from HDD, even if a cost per bit differential still exists.

- Power proportionality. Roughly one-third of the power in a large computer system is consumed in the memory sub-system [515]. A substantial amount of this is refresh power, required by the non-volatile nature of DRAM. As a result, modern data servers consume considerable power even when operating at low utilization rates. For example, Google [516] reports that servers are typically operating at over 50% of their peak power consumption even at very low utilization rates. The requirement for fast transition to operation precludes using a hibernate mode. A persistent memory that did not require constant refresh would be valuable.

  These requirements have led to considerable early investigation into new memory architectures, exploiting emerging memory devices, often in conjunction with DRAM and HDDs in novel architectures. These new memory systems are often referred to as Storage Class Memories (SCM). These can be further differentiated as whether they are intended to be close to the CPU, or to largely supplement the hard-drives [517]. The key characteristics are summarized in Table ERD14.

Storage Class Memory architectures that are intended to replace or merge with DRAM, and be close to the CPU, are referred to as M-type or Memory-type SCM (M-SCM). Thus, the properties of this memory will have many similarities to DRAM, including its interfaces, architecture, endurance, and read and write speed. Since write endurance of an emerging research memory is likely to be inferior to DRAM, considerable scope exists for architectural innovation. Examples of problems that will require architectural innovation include the integration of multiple memory technologies to optimize performance and power while maximizing lifetime, advanced load leveling that preserves the word level interface (since load leveling is usually done at the block level), and error correction suited for the likely error pattern. The memory management system is still to be worked out. For example, is the DRAM simply treated as an L4 cache for the persistent memory or is it directly managed? The interface is likely to be a word addressable bus, treating the entire memory system as one flat address space. Note, that flash, or evolved flash, is unlikely to have sufficient write endurance for this application. Cell level requirements are explored in detail in Section 4.1 of this chapter.

S (Storage) type SCMs are intended to replace or supplement hard-disk drive as main storage. Their main advantage will be speed, avoiding the seek time penalty of main drives. However, to succeed, their total cost of ownership needs to approach that of HDDs. Research issues include whether the SCM serves as a disk cache, or is directly managed; how load leveling is implemented while retaining a sufficiently fast and flexible interface; how error correction is implemented, and what is the optimal mix of technologies. Some open questions are the storage management, interface and architectural integration. For example, is it treated like a fast disk drive, or as a managed extension of main memory, preserving an addressable interface. Also, are pages preserved and how are they managed? It is likely that Virtual Memory won't be optimal in this type of storage system. Note that flash is a possible contender for S-SCM.

While Ref.[518] does not use the terminology "SCM", the author defines three possible architectures, two of which are broadly similar to M-SCM and S-SCM. However, the author does point to a third possibility – a 3D stacked node that incorporates computing cores, caches, DRAMs and emerging nano-memories into a monolithic stack.

5.1.2.3 Mobile Wireless Computing.

Mobile devices are the fastest growing consumer computing sector and they have their own unique memory requirements. Traditionally, mobile devices have emphasized simple CPUs with most of the storage using NAND flash, but they are fast evolving into complex multi-core devices running applications similar to that of laptop computers, but with limited power and cost budgets. With block-based wear leveling management, and erase before write, NAND flash is not well suited to being high in the memory hierarchy for advanced mobile devices. For example, integrating PRAM (Phase change RAM) into the mobile environment, together with a redesigned memory management controller, can deliver a six times improvement in speed and also extends the memory lifetime six times[519]. There is considerable opportunity to improve the price-performance of mobile wireless computing by rethinking the memory architecture with emerging memory devices within them.[520]

5.1.2.4 Application Specific Computing.

ASIC memory architectures are also likely to evolve as emerging memory devices become broadly available. For example, persistent STT-RAM leads to opportunities for aggressive power management, as does other persistent memory

technologies. The potential for lower-cost associative memories could be interesting in networking and neuromorphic applications.

Table ERD13 Anticipated Important Properties of Emerging Memories as driven by Application Need

Table ERD14 Likely desirable properties of M (Memory) type and S (Storage) type Storage Class Memories

5.2. EVOLVED ARCHITECTURES EXPLOITING EMERGING RESEARCH MEMORY DEVICES

Emerging non-volatile memory devices are becoming accepted to implement logic functions. The potential density of nano memory devices makes this option particularly attractive. A common approach is to investigate the potential for emerging memory devices to replace functions within FPGAs. Field Programmable Gate Array architectures rely on numerous small SRAMs to act as Look Up Tables (LUTs) for small combinational logic functions (typically a few inputs and 2 outputs) and to program the pass gates used in the interconnect Programmable Switch Matrices (PSM) used for interconnect. Replacing these SRAMs with NV memories has been suggested numerous times and was even once implemented in a commercial product using Floating Gate FETS. Recently researchers have suggested using STT-RAM, ReRAM or Nanocrystal Floating Gate FETs instead [e.g. Ref.[521]]. Typically, these substitutions reduce the 6T SRAM cell to one or two devices when used in the LUT and are used instead of the SRAM cell and pass gate in the PSM. This decreases the size of each, leading typically to a 2-3x improvement in the performance/power ratio at any particular CMOS node. Additional advantage can be obtained by using an NVRAM technology with high cycle endurance, such as STT-RAM, to implement reconfigurable dynamic logic[522]. Another interesting direction is to use emerging memories to build high density associative memories[523]. The high power and low density of SRAM based associative memories limits their employability today.

An open question is how to better leverage emerging devices to obtain improvements larger than 2-3x. Directions being pursued include using nano crossbars as programmable logic arrays, merging such arrays with CMOS (CMOL – a neuromorphic architecture – see Section 5.3.1 below), reconfigurable computing using nano memories, and associative memories or content addressable memories (discussed above).

Table ERD15 Current Research Directions for Employing Emerging Research Memory Devices to Enhance Logic

5.3. MORPHIC ARCHITECTURES

Biological systems give us examples of amorphous, unstructured, devices capable of noise- and fault-tolerant information processing. They excel in massively parallel spatial problems, as opposed to digital processors, which are rather weak in that area. The *morphic* architecture was thus introduced in the ERA section of ITRS 2007, to refer to biologically-inspired architectures that embody a new kind of computation paradigm in which adaptation plays a key role to effectively address the particulars of problems[524]. This subsection focuses on recent progress of two morphic architectures that offer opportunities for emerging research devices: neuromorphic architectures and cellular automaton architectures.

5.3.1. NEUROMORPHIC ARCHITECTURES

The term "neuromorphic" was introduced by Carver Mead in the late 1980s, to describe VLSI systems containing electronic analog circuits that mimic neuro-biological architectures in the nervous system[525]. Traditional neurocomputers employ components that are biologically rather implausible, like static threshold elements that represent neurons, whereas neuromorphic architectures are closer to biology. An example of a neuromorphic VLSI system is the silicon retina[526] that is modeled after the neuronal structures of the vertebrate retina.

The appeal of neuromorphic architectures lies in i) their potential to achieve (human-like) intelligence based on unreliable devices typically found in neuronal tissue, ii) their strategies to deal with anomalies, emphasizing not only tolerance to noise and faults, but also the active exploitation of noise to increase the effectiveness of operations, and iii) their potential for low-power operation. Traditional von Neumann machines are less suitable with regard to item i), since for this type of tasks they require a machine complexity (the number of gates and computational power), that tends to increase exponentially with the complexity of the environment (the size of the input). Neuromorphic systems, on the other hand, exhibit a more gradual increase of their machine complexity with respect to the environmental complexity[527]. Therefore,

at the level of human-like computing tasks, neuromorphic machines have the potential to be superior to von Neumann machines. Points ii) and iii) are strongly related to each other in von Neumann machines, since tolerance to noise runs counter to lowering power supply voltage and bias currents. Neuromorphic architectures, on the other hand, suffer much less from this trade-off. Unlike von Neumann machines, which can correct bit-errors only to a certain extent through the use of error-control techniques, neuromorphic machines tend to keep working even under high error rates.

Like the areas of the human brain, neuromorphic machines (VLSIs) are application-specific. Significant performance benefits can be achieved by employing them as supplemental CMOS, as an addition to a von Neumann system, which provides universal computation ability. Neuromorphic systems thus have a diversified functionality, and consequently can be categorized as more-than-Moore candidates. Table ERD16 shows trends in the development of neuromorphic systems and their applications. The application category "Information processing" is only a single item in the table, which understates the potentially large benefits in terms of machine complexity of human-like information processing, since functionalities like prediction, associative memory, and inference offer new opportunities left unexplored by von Neumann architectures. The ERA section of ITRS 2009, for example, introduced an inference engine based on Bayesian neural networks[528], and in 2010 Lyric Semiconductor introduced NAND gates where the input probabilities are combined using Bayesian logic rather than the binary logic of conventional processors. Lyric Error Correction (LEC) uses this probabilistic logic to perform error detection and correction with about 3 percent of the circuitry and 8 percent of the power that would be needed for the equivalent conventional error correction scheme[529].

Table ERD16 Applications and Development of Neuromorphic System

ITRS 2007 (ERA section) did not address neuromorphic "Intelligent sensors", since they were considered ancillary to the central focus on information processing of ITRS at the time. However, intelligent sensors were revived in the table, because there exist vast opportunities for high performance architectures that combine them with emerging research devices. So far CMOS implementations (in the items titled: "Vision" and "Others"; see Table ERD16) and SET implementations (in the item titled "Vision") have been proposed.

Another approach to build neuromorphic systems is inspired by biochemical reactions in living organisms. Reaction-diffusion computers, for example, are based on a biochemical reaction[530], and they are able to efficiently solve combinatorial problems through the use of natural parallelism. Electronic implementations of this type of information processing require strong nonlinear I-V characteristics to mimic the chemical reactions involved, and there exist many opportunities for emerging research devices in this respect.

On the technology side, one of the key issues for neuromorphic systems is how neuronal elements are implemented. An important consideration in this respect is the level of abstraction of a biological neuron, which can range from (almost) physically representative to a very simple model, such as an integrate-and-fire neuron. Depending on the technology used (SET neurons, RTD, memristors, etc.), this level may vary, and opportunities for emerging research devices exist in this respect. Another important issue is how non-volatile analog synapses are implemented. Many attempts have been made to design analog synaptic devices based on existing flash-memory technologies, but they have experienced difficulties in designing appropriate controllers for electron injection and ejection as well as increasing the limit on the number of rewriting times. Memristive devices (e.g., resistive RAMs and atomic switches) offer a promising alternative for the implementation of non-volatile analog synapses. They are applied in the CMOL architecture, which combines memristive nano-junctions with CMOS neurons and their associated controllers. In ITRS 2007, CMOL (CrossNets) was introduced in terms of nanogrids of (ideally) single molecules fabricated on top of a traditional CMOS layer, but the concept has since been expanded to use a nanowire-crossbar add-on as well as memristive (two-terminal) crosspoint devices like nanowire resistive RAMs[531]. The CMOL architecture may be further expanded to include multiple stacks of CMOS layers and crossbar layers. This may result in the implementation of large-scale multi-layer neural networks, which have thus far evaded direct implementations by CMOS devices only. However, while CMOL remains an interesting concept it has yet to be reduced to practice or even demonstrated.

A final important issue is noise tolerance and noise utilization in neural systems and their possible application in electronics. Noise and fluctuations are usually considered obstacles in the operation of both analog and digital circuits and systems, and most strategies to deal with them focus on suppression. Neural systems, on the other hand, tend to employ strategies in which the properties of noise are exploited to improve the efficiency of operations. This concept may be especially useful in the design computing systems with noise-sensitive devices (e.g., extremely low-power devices like SET and subthreshold analog CMOS devices).

Table ERD17 Noise-Driven Neural Processing and its Possible Applications

Table ERD17 shows examples of noise-driven neural processing and their possible applications in electronics. *Stochastic resonance (SR)* is a phenomenon where a static or dynamic threshold system responds stochastically to a subthreshold or suprathreshold input with the help of noise. In biological systems SR is utilized to detect weak signals under a noisy environment. Stochastic resonance for some emerging research devices (a SET network and GaAs nanowire FETs) has been demonstrated. Stochastic resonance can be observed in many bi-stable systems, and will be utilized to facilitate the state transitions in emerging logic (bi-stable) memory devices. *Noise-driven fast signal transmission* is observed in neural networks for the vestibulo ocular reflex, where signals are transmitted with an increased rate over a neuronal path when non-identical neurons and dynamic noise are introduced. Implementation in terms of a SET circuit has demonstrated that when several non-identical pulse-density modulators were used as noisy neurons, performances on input-output fidelity of the population increased significantly as compared to that of a single neuron circuit. *Phase synchronization among isolated neurons* can be utilized for skew-free clock distribution where independent oscillators are implemented on a chip as distributed clock sources, while the oscillators are synchronized by a common temporal noise. Noise in *synaptic depression* can be used to facilitate the operation of a neuromorphic burst-signal detector, where the output range of the detector is significantly increased by noise. *Noise-shaping in inhibitory neural networks* has been demonstrated in subthreshold CMOS, where static and dynamic noises can be used constructively if one could not remove a certain level of noise or device mismatches. The circuits exploit properties of device mismatches and external (temporal) noise to perform noise-shaping 1-bit AD conversion (pulse-density modulation).

5.3.2. CELLULAR-AUTOMATA ARCHITECTURES

A *Cellular Automaton* is an array of cells, organized in a regular grid. Each cell can be in one of a finite number of *states* from a predefined state set, which is usually a set of integers. The state of each cell is updated according to *transition rules*, which determine the cell's next state from its current state as well as from the states of the neighboring cells. The neighbors of a cell are usually the cells directly adjacent in orthogonal directions of a cell, like the north, south, east, and west neighbor in the case of a two-dimensional grid (*von Neumann neighborhood*), but other neighborhoods have also been demonstrated. The functionality of each cell is defined by the transition rules of the cellular automaton. The transition rules are usually the same for all cells, but heterogeneous sets of rules have also been considered, as well as programmable rules. A cell can typically be expressed in terms of a *Finite Automaton*, which is a model in computer science well-known for its simple but effective structure.

Cellular automata were initially proposed by von Neumann in the 1940's as a model of self-reproduction, but most of the interest they have attracted since then has been motivated by their ability to conduct computation in a distributed way. Though cellular automata have the name of their inventor in common with von Neumann architectures, they represent a radically different concept of computation.

The appeal of cellular automata as emerging research architectures lies in a number of factors. First, their regular structure has the potential for manufacturing methods that can deliver huge numbers of cells in a cost-effective way. Candidates in this respect are bottom-up manufacturing methods, such as those based on molecular self-assembly. Second, regularity also facilitates reuse of logic designs. The design of a cell is relatively simple as compared to that of a microprocessor unit, so design efforts are greatly reduced for cellular automata. Third, errors are more easily managed in the regular structures of cellular automata, since a unified approach for all cells can be followed. Fourth, wire lengths between cells are short, or wires are completely unnecessary if cells can interact with their neighboring cells through some physical mechanism. Fifth, cells can be used for multiple purposes, from logic or memory to the transfer of data. This makes cellular automata configurable in a flexible way. Sixth, cellular automata are massively parallel, offering a huge computational power for applications of which the "logical structure" fits the topology of the grid of cells.

Cellular automata may be less suitable for certain application due to the following factors. First, there is a relatively large overhead in terms of hardware. Cells tend to require a certain minimal level of complexity in order to be useful for computation[532]. In practice this means that they are configurable for logic, memory, or data transfer. The density of such functionality per unit of area tends to be lower than that of more conventional architectures. A large hardware overhead may be acceptable, though, if cells are available in huge numbers at a low cost, especially if the cellular automaton can be mapped efficiently onto a certain application. Second, input and output of data to cells may be difficult. The use of the border cells of a grid for input and output is infeasible in case of huge numbers of cells, because it fails to employ all cells in parallel. Parallel input and output to cells through optical means or by wires addressing individual cells like in memory have more potential in this context. Third, it is difficult to configure cells into various patterns of states. Such configuration and reconfiguration functionality is required to give the cellular automaton its functionality for a certain

computational task. Here similar solutions as those for the input and output of data need to be employed to access cells in parallel.

There are two approaches for implementing cellular automata in hardware: fine-grained and tiny-grained. Systems that are coarser grained are considered outside the class of cellular automata, since they are associated with multi-core architectures. Fine-grained cellular automata have cells that can be configured each as one or a few logic gates, or as a simple hub for data transfer. A cell typically contains a limited amount of memory in the order of 10 to 100 Bytes. Cells are usually addressed on an individual basis for input and output, or for configuration. Typically, the transition rules governing the functionality of a cell are changed during configuration. An example of a fine-grained approach is the Cell Matrix[533], which is a model capable of universal computation. Fine-grained cellular automata have a good degree of control over configuration and computation, but it comes at the price of relatively complex cells, limiting the use of cost-effective manufacturing methods that can exploit the regularity of these architectures.

The other approach to cellular automata is tiny-grained. Cells in this model have extremely simple functionality, in the order of a few states per cell and a limited number of (fixed) transition rules. The small number of states translates into memory requirements of only a few bits per cell, whereas the non-programmable nature of the transition rules drastically reduces the complexity of cells. The simple nature of rules poses no problems if the rules are designed to cover the functionality intended for the cellular automaton. An example of a tiny-grained approach has been proposed in Ref.[534], which is capable of universal computation as well as the correction of errors. Tiny-grained cellular automata have the potential of straightforward realizations of cells on nanometer scales. The challenge is to design models with as few states and transition rules per cell as possible. The theoretical minimum is two states and one transition rule. In synchronously timed models this has been approached by the *Game-of-Life* cellular automaton (two states, two rules), and in asynchronously timed models (no clock) by the *Brownian Cellular Automata*[535] (three states, three rules). Both models are universal. The number of states and rules should be considered only as rough yardsticks, since ultimately the most important measure is the efficiency at which cells can be realized in a technology.

Most hardware realizations of cellular automata to date are application specific. In this context cellular automata are used as part of a larger system to conduct a specific set of operations with great efficiency. Applications typically have a structure that can be mapped efficiently onto the hardware, and the approach followed is generally tiny-grained, since cells are optimized for one or a few simple operations. Image processing applications are the most common in such hardware realizations[536,537,538], since they can be mapped with great efficiency onto two-dimensional cellular automata. Though the focus in the past was mostly on operations like filtering, thinning, skeletonizing, and edge detection, recent applications of cellular automata include the watermarking of images with digital image copyright[539,540]. Cellular automata have also been used for the implementation of a Dictionary Search Processor[541], memory controllers[542], and the generation of test patterns for Built-In Self-Test (BIST) of VLSI chips[543,544]. An overview of application-specific cellular automata is given in Ref.[545].

It is expected that the role of cellular automata in architectures will gradually increase with technological progress, from being merely used as dedicated sub-processor to the main part of the architecture. At that point cellular automata need a capacity that their application-specific cousins lack: computation universality, i.e., the ability to carry out the same class of computations as do our current computers. This term is mostly used in a theoretical context, to prove equivalence to a universal Turing machine. The extreme inefficiency of Turing machines carries with it the misunderstanding that cellular automata proven to be universal are inefficient; but this is often far from the truth. A general approach to carry out operations efficiently on a cellular automaton is to configure it as a logic circuit. Cells will then be used as logic gates or for transferring data between logic gates. In fine-grained cellular automata, a cell is typically sufficiently complex such as to be able to function as one or a few gates. In tiny-grained cellular automata, on the other hand, clusters of cells need to work together in order to obtain logic gate functionality. A cluster typically consists of up to 10 cells, its size depending on the functionality covered. This may seem a large overhead, but cells tend to be much less complex than in fine-grained cellular automata, making this approach feasible. Furthermore, cells used merely to transfer data – and this is the majority of the cells – see much less of their hardware unused when carrying out this simple task.

Cellular automata have seen only limited attempts at realizations at nanometer scales. *Molecule Cascades*[546] use CO molecules on a Cu(111) grid to conduct simple logic operations. The CO molecules jump from grid point to grid point, triggering each other sequentially, like dominos. This process is quite slow and error-prone, though there appears to be potential for improvement. The mechanical nature of the operations, though, means that this cellular automaton is unlikely to reach competitive speeds. Another attempt uses layers of organic molecules on a gold grid[547]. Interactions between molecules take place via the tunneling of electrons between them. The rules that have been identified as governing those interactions appear to be influenced by the local presence of excess electrons in the grid. This may limit

the control over the operation of the cellular automaton, but it also carries the promise of efficient ways to configure the grid.

5.3.3. TAXONOMY OF COMPUTATIONAL ABILITY OF ARCHITECTURES

Whereas von Neumann architectures generally refer to the use of memory resources separated from computational resources to store data and programs, there is an increasing need for taxonomy of those architectures that are based on different concepts.

The term "More-Neumann" refers to those architectures that differ from the classical von Neumann architecture only in terms of numbers. While the stored memory concept is still followed in More-Neumann architectures, a certain level of parallelism is assumed, like in multi-core systems.

"More-than-Neumann" refers to architectures that do not suffer from the von Neumann bottleneck between computation and memory resources, i.e., these resources are integrated to a high degree. These architectures tend to have a highly distributed character in which small elements have extremely limited memory and computation resources to the extent that each element individually is "Less-than-Neumann" (i.e., incapable of being used as a full-fledged von Neumann architecture), yet the *combination* of these elements lifts them to a higher level of competence. In More-than-Neumann architectures *reorganization* or *reconfiguration* usually plays the role that programmability has in von Neumann architectures. Programming a More-than-Neumann architecture thus involves an appropriate organization or configuration of the individual elements in order to make them perform a certain function. This reorganization may take the form of setting / adjusting the memories of the individual elements, but it may also involve a reconfiguration of interconnections between the elements. In the context of neuromorphic architectures the elements take the form of neurons and synaptic connections between them. Synapses can be adjusted based on a learning process, while in some architectures new synaptic connections can be created and old ones destroyed. In the case of cellular automata, the elements are the cells, and their functionality is changed by setting their memory states to appropriate values. More-than-Neumann architectures are typically capable of high performance on certain classes of problems, but much less so on other problems (or may be even unable to handle other problems). Neuromorphic architectures have their strengths in problems that involve learning, classification, and recognition, but they will do less well on traditional computing problems. Cellular automata are strong in applications that demand a regular structure of logic or data and a huge degree of parallelism.

"Beyond-Neumann" refers to architectures that can solve certain computational problems fundamentally faster than would be possible on the architectures outlined above. Problems such as these typically require computation times that are exponential as measured in terms of their input. The fundamental limits that restrict the computational power of architectures ranging from von Neumann to More-than-Neumann are exceeded in Beyond-Neumann architectures through adopting novel operating principles. Schemes that use analogue values instead of digital (neuromorphic architectures, dynamic systems, etc.), that use superposition of bit values (quantum computing schemes), or that use an analogue timing scheme (asynchronous architectures) are prime candidates for this category. The flow of information in an architecture may also characterize it as Beyond-Neumann. While Turing machines embody the traditional Input-Processing-Output flow, modern computers (even von Neumann ones) are used in a more interactive mode with humans, like in gaming, or with other computers, when connected in networks. Biological brains have a somewhat related concept of input and output, but different in its implementation: their processing of information appears to be an autonomous process, that may (or may not) be modulated by the input signals in the environment[548]. This allows biological organisms to flexibly select important signals from the environment, while ignoring irrelevant ones. Underneath these lies an impressive neural machinery, yet to be uncovered, that can solve problems with unrivaled efficiency. Many of the above elements (analogue-valued signals, asynchronous timing in combination with selective synchronization, and chaotic dynamics) are thought to play an important role in neural information processing. While Beyond-Neumann architectures are promising in principle, it needs to be emphasized that currently no practical implementations of them have been reported.

6. EMERGING MEMORY AND LOGIC DEVICES—A CRITICAL ASSESSMENT

6.1 INTRODUCTION

The purpose of this section is to assess the potential of each emerging research technology entry considered in this chapter to perform its intended memory or information processing function benchmarked against current memory or CMOS technologies, all at their full maturity. These targeted functions are: 1) eventually replace CMOS with a highly scalable, high performance, low power, information processing device technology, or 2) provide a memory or storage technology capable of scaling either volatile and/or nonvolatile memory technology beyond the 15nm generation.

Two independent methods are used to perform this assessment. In one method, referred to as "Quantitative Logic Benchmarking", each emerging logic device is evaluated by its operation in three conventional Boolean Logic circuits: a unity gain inverter; a 2-input NAND gate; and a 32-bit shift register. Metrics evaluated are: speed, areal footprint, and power dissipation, each normalized to the performance projected for two 15nm CMOS applications (high performance and low power).

The second method, referred to as "Survey-Based Benchmarking", is to conduct a survey of the ERD working group to evaluate each technology entry against eight evaluation criteria normalized to high-performance CMOS at full maturity for logic or to the memory technology targeted for replacement. An important issue regarding emerging charge-based nanoelectronic switch elements is related to the fundamental limits to the scaling of these new devices, and how they compare with CMOS technology at its projected end of scaling. An analysis [549]concludes that the fundamental limit of scaling an electronic charge-based switch is only a factor of 3× smaller than the physical gate length of a silicon MOSFET in 2024. Furthermore, the density of these switches is limited by maximum allowable power dissipation of approximately 100W/cm^2, and not by their size. The conclusion of this work is that MOSFET technology scaled to its practical limit in terms of size and power density will asymptotically reach the theoretical limits of scaling for charge-based devices.

Most of the proposed beyond-CMOS replacement devices are very different from their CMOS counterparts, and often pass computational state variables (or tokens) other than charge. Alternative state variables include collective or single spins, excitons, plasmons, photons, magnetic domains, qubits, and even material domains (e.g. ferromagnetic). With the multiplicity of programs characterizing the physics of proposed new structures, it is necessary to find ways to benchmark the technologies effectively. This requires a combination of existing benchmarks used for CMOS and new benchmarks which take into account the idiosyncrasies of the new device behavior. Even more challenging is to extend this process to consider new circuits and architectures beyond the Boolean architecture used by CMOS today, which may enable these devices to complete transactions more effectively.

6.2 QUANTITATIVE LOGIC BENCHMARKING FOR BEYOND CMOS TECHNOLOGIES

The first method for benchmarking emerging information processing devices, as indicated above, is based on their quantitative evaluation in conventional circuits mentioned in Section 6.1 above. The Nanoelectronics Research Initiative (http://nri.src.org) has been benchmarking several diverse beyond-CMOS technologies over the past two years, trying to balance the need for quantitative metrics to assess a new device concept's potential with the need to allow device research to progress in new directions which might not lend themselves to existing metrics. Several of the more promising NRI devices have been described in detail in the Logic and Emerging Information Processing Device Section 4.2 [14], and the intermediate results on the benchmarking efforts were outlined in a recent IEEE Proceedings article[550] While this effort is still very much a work in progress – and no concrete decisions have been made on which devices should be chosen or eliminated as candidates for significantly extending or augmenting the roadmap as CMOS scaling slows – this section summarizes some of the data and insights gained from the exercise thus far. It should be noted that NRI is continuing to refine the benchmark data within the program, with updated results being generated in the second half of 2011. This data (potentially to be published in 2012) may alter some of the conclusions here and the outlook on some of these devices, but the overall message on the challenge of finding a beyond CMOS device which can compete well across the full spectrum of benchmarks of interest remains.

6.2.1 ARCHITECTURAL REQUIREMENTS FOR A COMPETITIVE LOGIC DEVICE

The circuit designer and architect depend on the logic switch to exhibit specific desired characteristics in order to insure successful realization of a wide range of applications. These characteristics, outlined in Ref. [551],which have since been supplemented in the literature, include:

- Inversion and Flexibility (can form an infinite number of logic functions)
- Isolation (output does not affect input)
- Logic gain (output may drive more than one following gate and provides a High I_{on}/I_{off} Ratio)
- Logical completeness (the device is capable of realizing any arbitrary logic function)
- Self Restoring / Stable (Signal quality restored in each gate)
- Low cost Manufacturability (Robust evaluate physics, acceptable process tolerance)
- Reliability (Aging, wear-out, radiation immunity)
- Performance (transaction throughput improvement)
- "Span of Control" is an important means of connecting device performance and area to communication performance, relating time to space. The metric measures how other devices may be contacted within a characteristic delay of the switch, and is dependent not only on switch delay, but switch area as well as communication speed [552] Successful architectures also need effective fan-out.

Devices with intrinsic properties supporting the above features will be adopted more readily by the industry. Moreover, devices which enable architectures that address emerging concerns such as computational efficiency, complexity management, self-organized reliability and serviceability, and intrinsic cyber-security[553] are particularly valuable.

6.2.2 QUANTITATIVE RESULTS

Preliminary analyses sponsored by SRC/NRI[554] surveyed the potential logic opportunities afforded by 16 emerging research switches using a variety of information tokens and communication transport mechanisms. Specifically, the projected effectiveness of these devices used in a number of logic gate configurations was evaluated, and normalized to CMOS at the 15nm generation as captured by the ITRS. The initial work has focused on "standard" Boolean logic architecture, since the CMOS equivalent is readily available for comparison. It should also be noted that the majority of this data is based on simulations only, since many of these structures have not yet been built, so it should be considered only a "snapshot in time" of any given device's potential, as the research on all of them is at a very early stage and hence the data is evolving

At a high level, the data from this study corroborates qualitative insights from earlier works, suggesting that many new logic switch structures are superior to CMOS in energy and area, but inferior to CMOS in delay, as shown in the plot of median data for the device (Figure ERD5). This is perhaps not surprising; the primary goal for nanoelectronics and NRI is to find a lower power device [555] since power density is a primary concern for future CMOS scaling, and power and speed are a common trade-off. Looking at the energy-delay characteristics for a NAND2 circuit specifically (Figure ERD6), one observes that several of the devices are significantly lower power (even lower than a low voltage version of CMOS), while maintaining a reasonable delay.

Moving beyond the logic gate, it is important to understand the potential impact of the transport delay for the different information tokens these devices employ. As shown in Figure ERD7, communication with many of the non-charge tokens can be significantly slower than moving charge, although this may be balanced in some cases with significantly lower energy for transport. Moreover, the combination of the new balance between switch speed, switch area, and interconnect speed can lead to advantages in the span of control for a given technology (Figure ERD 8). Finally, for some of the technologies, such as nanomagnetic logic, there is no strong distinction between the switch and the interconnect, indicating the need for additional thinking on the appropriate architecture to exploit some of these attributes.

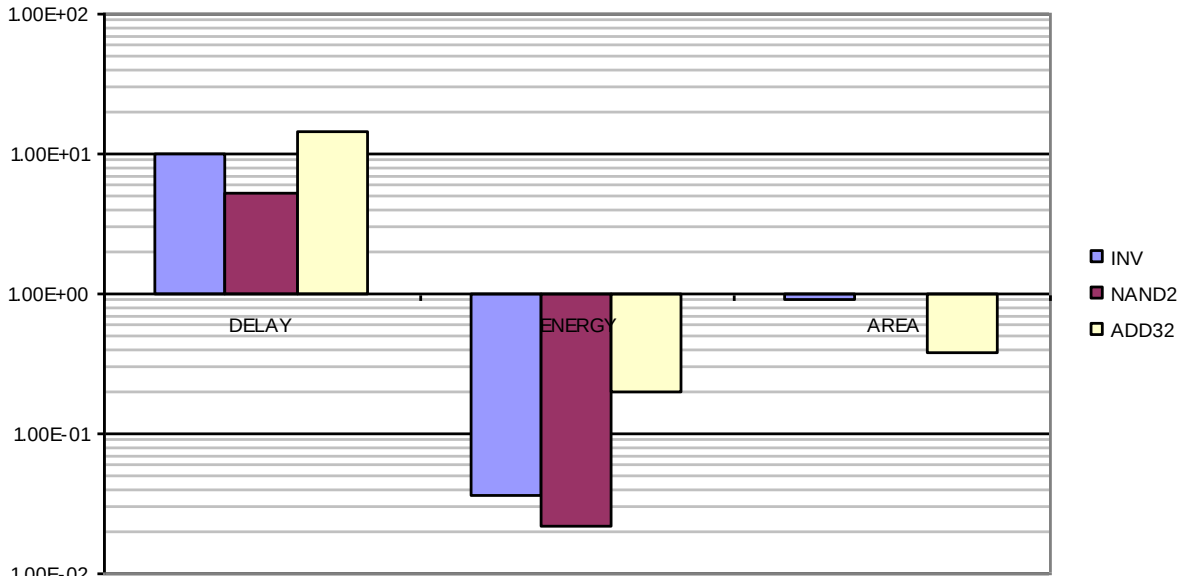


Figure ERD5 Median delay, energy, and area of proposed devices, normalized to ITRS 15-nm CMOS. (Based on principal investigators' data; from Rev. [556]

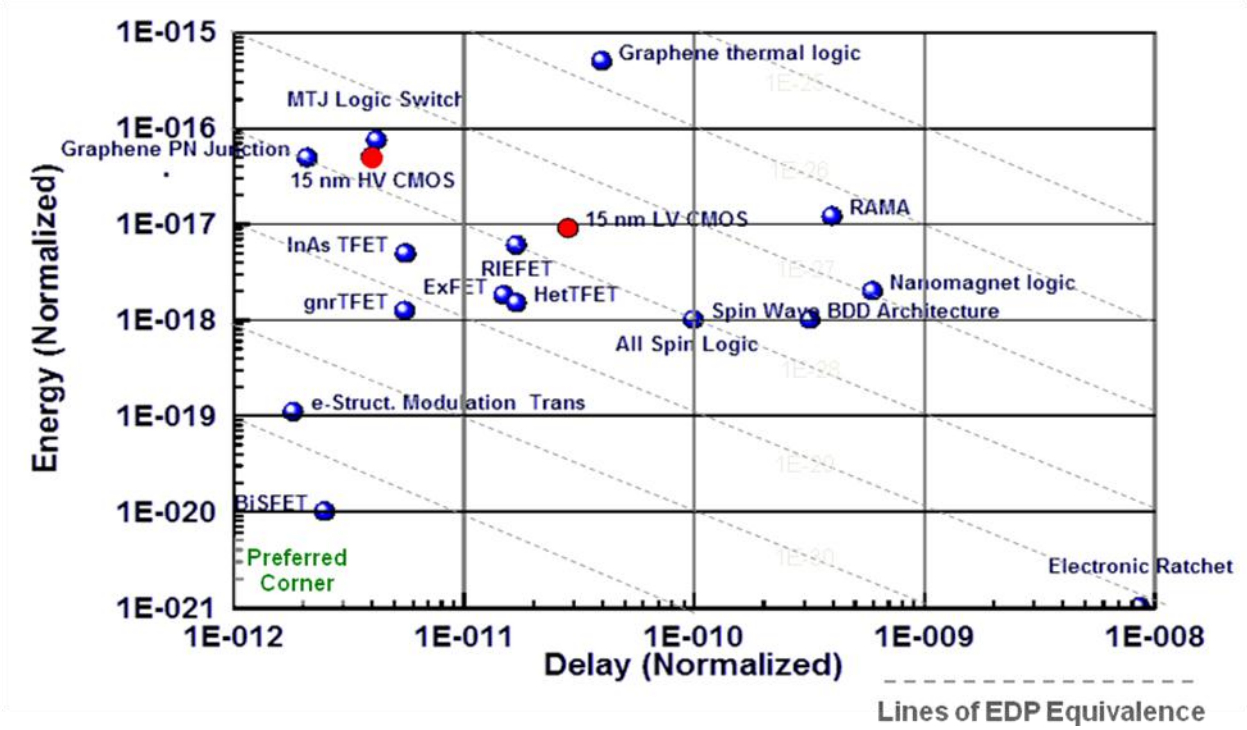


Figure ERD6 Energy versus delay of a NAND2 gate in various post-CMOS technologies. Projections for both high-performance and low-power 15nm CMOS are included as reference. All values are a snapshot in time, and will change as work continues. (Based on principal investigators' data; from Ref. [557] *)*

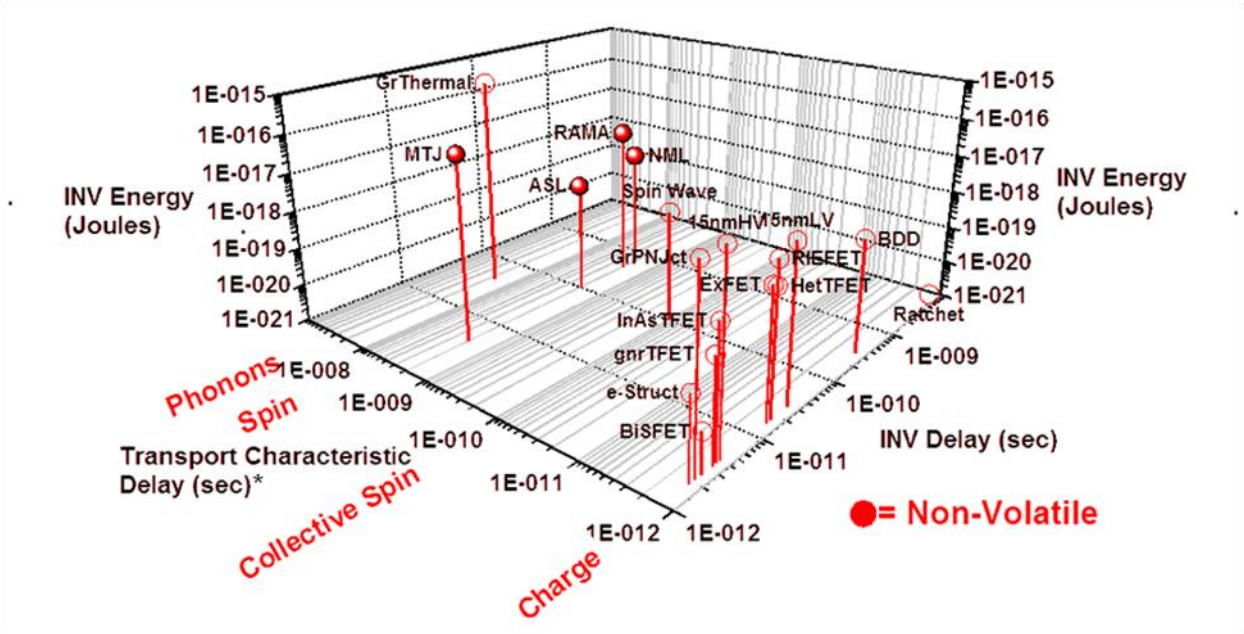


*Figure ERD7 Inverter energy and delay and interconnect delay (*characteristic of transport over 10um) for various beyond-CMOS technologies. Projections for both high-performance and low-power 15nm CMOS included as reference. Solid dots indicate the switch is intrinsically non-volatile. All values are a snapshot in time, and will change as work continues. (Based on principal investigators' data)*

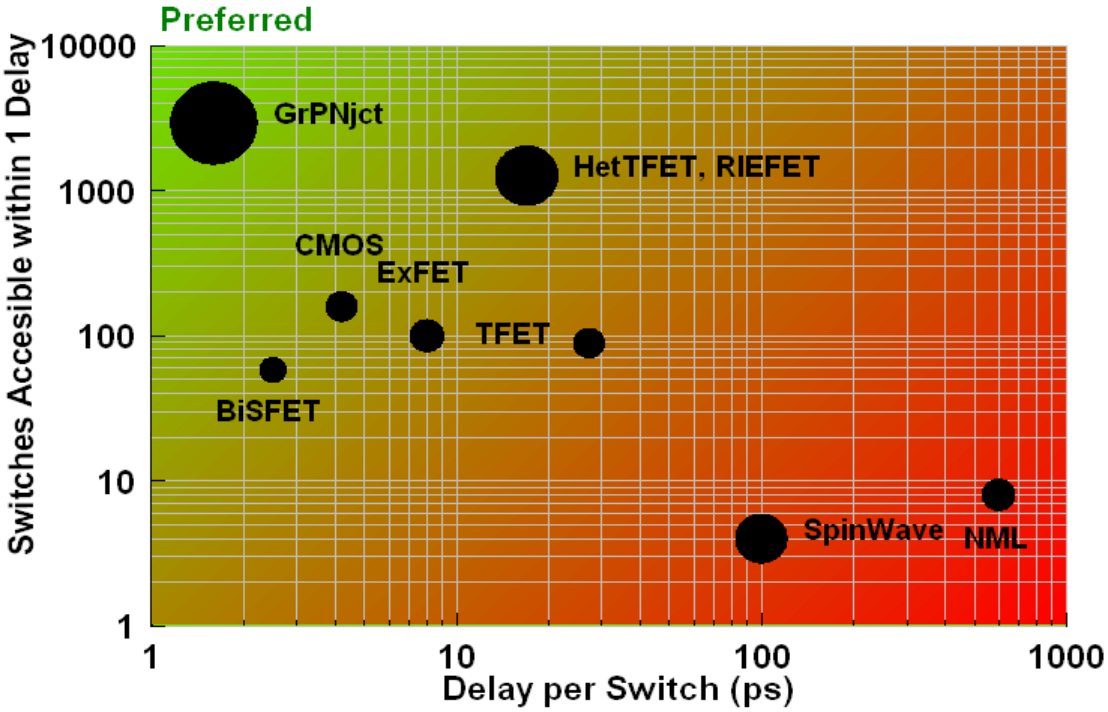


Figure ERD8 Transport impact on switch delay, size, and area of control. Circle size is logarithmically proportional to physically accessible area in one delay. Projections for 15nm CMOS included as reference. (Based on principal investigators' data; from Ref. [558])

In fact at the architecture level, the ability to speculate on how these devices will perform is still in its infancy. While the ultimate goal is to compare at a very high level – e.g. how many MIPs can be produced for 100mW in 1 mm^2? – the current work must extrapolate from only very primitive gate structures. One initial attempt to start this process has been to look at the relative "logical effort" [559] for these technologies, a figure of merit which ties fundamental technology to a resulting logic transaction. As seen in Figure ERD 9, several of the devices appear to offer advantage over CMOS in logical effort, particular for more complex functions which increases the urgency of doing more joint device – architecture co-design for these emerging technologies.

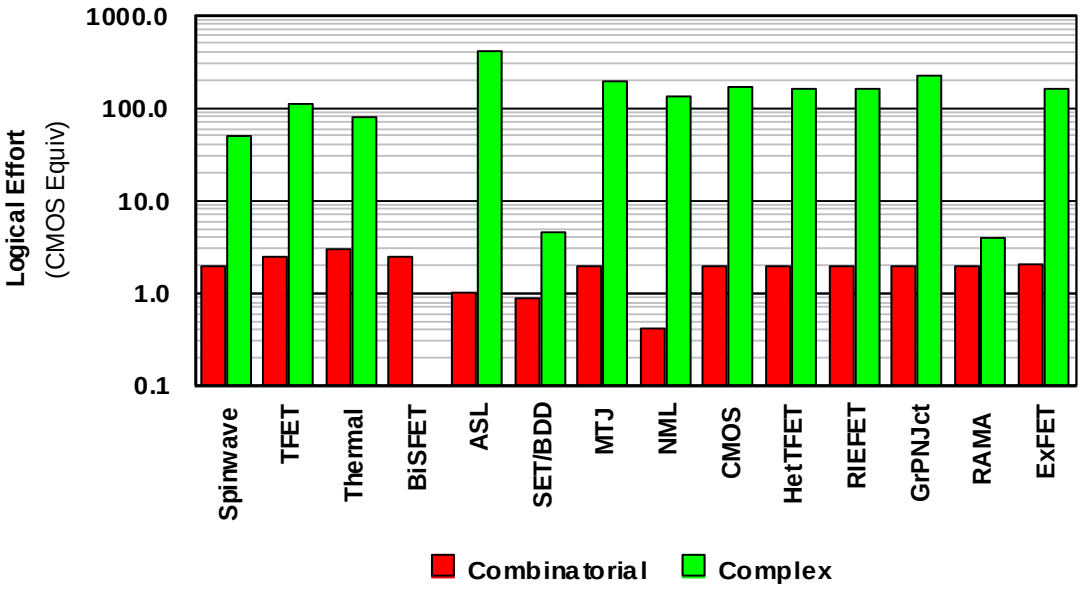


Figure ERD9 Estimated logical effort – a measure of the relative "expense" required to perform a given logic function – for new switches in both simple combinatorial and complex circuits (lower values are preferred). Projections for 15nm CMOS included as reference. (Based on principal investigators' data)

6.2.3 OBSERVATIONS

A number of common themes have emerged from the results of this work and in the observations made during recent studies of beyond-CMOS replacement switches [560, 561]. A few noteworthy concepts:

1) The low voltage energy-delay tradeoff conundrum will continue to be a challenge for all devices. Getting to low voltage must remain a priority for achieving low power, but new approaches to getting throughput with 'slow' devices must be developed.
2) Most of the architectures that have been considered to date in the context of new devices utilize binary logic to implement von Neumann computing structures. In this area, CMOS implementations are difficult to supplant because they are very competitive across the spectrum of energy, delay and area – not surprising since these architectures have evolved over several decades to exploit the properties and limitations of CMOS most effectively. Novel electron-based devices – which can include devices that take advantage of collective and non-equilibrium effects – appear to be the best candidates as a drop-in replacement for CMOS for binary logic applications.
3) As the behavior of other emerging research devices becomes better understood, work on novel architectures that leverage these features will be increasingly important. A device that may not be competitive at doing a simple NAND function may have advantages in doing a complex adder or multiplier instead. Understanding the right building blocks for each device to maximize throughput of the system will be critical. This may be best accomplished by thinking about the high-level metric a system or core is designed to achieve (e.g. computation, pattern recognition, FFT, etc.) and finding the best match between the device and circuit for maximizing this metric.
4) Increasing functional integration and on-chip switch count will continue to grow. To that end, in any logic architectural alternative, both flexible rich logic circuit libraries and reconfigurability will be required for new switch implementations.

5) Patterning, precision layer deposition, material purity, dopant placement, and alignment precision critical to CMOS will continue to be important in the realization of architectures using these new switches.
6) Assessment of novel architectures using new switches must also include the transport mechanism for the information tokens. Fundamental relationships connecting information generation with information communication spatially and temporally will dictate CMOS' successor.

Based on the current data and observations, it is clear that CMOS will remain the primary basis for IC chips for the coming decade. While it is unlikely that any of the current emerging devices could entirely replace CMOS, several do seem to offer advantages, such as ultra-low power or non-volatility (Figure ERD 7), which could be utilized to augment CMOS or to enable better performance in specific application spaces. One potential area for entry is that of special purpose cores or accelerators that could off-load specific computations from the primary general purpose processor and provide overall improvement in system performance. This is particularly attractive given the move to multi-core chips: while most are homogeneous today, if scaling slows in delivering the historically expected performance improvements in future generations, heterogeneous multi-core chips may be a more attractive option. These would include specific, custom-designed cores dedicated to accelerate high-value functions, such as accelerators already widely-used today in CMOS (e.g. Encryption/Decryption, Compression/Decompression, Floating Point Units, Digital Signal Processors, etc.), as well as potentially new, higher-level functions (e.g. voice recognition). While integrating dissimilar technologies and materials is a big challenge, advances in packaging and 3D integration may make this more feasible over time, but the performance improvement would need to be large to balance this effort.

As a general rule, an accelerator is considered as an adjunct to the core processors if replacing its software implementation improves overall core processor throughput by approximately ten percent; an accelerator using a non-CMOS technology would likely need to offer an order of magnitude performance improvement relative to its CMOS implementation to be considered worthwhile. That is a high bar, but there may be instances where the unique characteristics of emerging devices, combined with a complementary architecture, could be used to advantage in implementing a particular function. At the same time, the changing landscape of electronics (moving from uniform, general purpose computing devices to a spectrum of devices with varying purposes, power constraints, and environments spanning servers in data centers to smart phones to embedded sensors) and the changing landscape of workloads and processing needs (Big Data, unstructured information, real-time computing, 3D rich graphics) are increasing the need for new computing solutions. One of the primary goals then for future beyond-CMOS work should be to focus on specific emerging functions and optimize between the device and architecture to achieve solutions that can break through the current power/performance limits.

6.3 SURVEY-BASED BENCHMARKING OF BEYOND CMOS MEMORY & LOGIC TECHNOLOGIES

6.3.1 OVERALL TECHNOLOGY REQUIREMENTS AND RELEVANCE CRITERIA

The second method for benchmarking emerging memory and information processing devices is based on a survey of the Emerging Research Devices Work Group. Some emerging nanoscale devices discussed in this chapter are charge-based structures proposed to extend CMOS to the end of the current roadmap. Other emerging devices offer new computational state variables and will likely require new fabrication technologies. A set of relevance or evaluation criteria, defined below, are used to parameterize the extent to which proposed "CMOS Extension" and "Beyond CMOS" technologies are applicable to memory or information processing applications. The Relevance Criteria are: 1) Scalability, 2) Speed, 3) Energy Efficiency, 4) Gain (Logic) or ON/OFF Ratio (Memory), 5) Operational Reliability, 6) Operational Temperature, 7) CMOS Technological Compatibility, and 8) CMOS Architectural Compatibility. Definitions of the evaluation criteria follow:

[1] Scalability—First and foremost the major incentive for developing and investing in a new information processing technology is to discover and exploit a new domain for scaling information processing functional density and throughput per Joule substantially beyond that attainable by ultimately-scaled CMOS. Silicon-based CMOS has provided several decades of scaling of MOSFET densities. The goal of a new information processing technology is to replicate this success by providing additional decades of functional and information throughput rate scaling using a new technology. In other words, it should be possible to articulate a Moore's law for the proposed technology over additional decades.

[2] Speed— A future information processing technology must continue to provide (at least) incremental improvements in speed beyond that attainable by ultimately scaled CMOS technology. In addition, nanodevices that implement both logic and memory functions in the same device would revolutionize circuit and nanoarchitecture implementations.

[3] Energy Efficiency—Energy efficiency has become the limiting factor of any beyond CMOS device using electronic charge or electric current as a computational state variable. It also appears that it will be a dominant criterion in

determining the ultimate applicability of alternate state variable devices. Clock speed versus density trade-offs for electron transport devices will dictate that for future technology generations, clock speed will need to be decreased for very high densities or conversely, density will need to be decreased for very high clock speeds. Nanoscale electron transport devices will best suit implementations that rely on the efficient use of multi-core processing to minimize energy dissipation.

[4A]I_{on}/I_{off} Ratio (Memory Devices)—The I_{on}/I_{off} ratio of a memory device is the ratio of the resistance of a memory storage element in the I_{on} state to its resistance in the I_{off} *state*. For non-volatile memories, the I_{on}/I_{off} ratio represents the ratio between the read current of a selected memory cell to the leakage current of an unselected cell. In cross-point memories, a very large I_{on}/I_{off} ratio is required to minimize power dissipation and maintain adequate read signal margin.

[4B] Gain (Logic Devices)—The gain of nanodevices is an important limitation for presently used combinatorial logic where gate fan-outs require significant drive current and low voltages make gates more noise sensitive. New logic and low-fan-out circuit approaches will be needed to use most of these nanodevices for computing applications. Signal regeneration for large circuits of nanodevices may need to be accomplished by integration with CMOS.

[5] Operational Reliability—Operational reliability is the ability of the memory and logic devices to operate reliably within their operational error tolerance given in their performance specifications. The error rate of all nanoscale devices and circuits is a major concern. These errors arise from the difficulty of providing highly precise dimensional control needed to fabricate the devices and also from interference from the local environment. Large-scale and powerful error detection and correction schemes will need to be a central theme of any architecture and implementations that use nanoscale devices.

[6] Operational Temperature—Nanodevices must be able to operate close to a room temperature environment for most practical applications with sufficient tolerance for higher temperature (e.g., 100^{o}C) operation internal to the device structure.

[7] CMOS Technological Compatibility—The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principal economic benefit of such an approach is it allows the industry to fully apply previous technology investments to future products. Any alternative technology as a goal should utilize the tremendous investment in infrastructure to the highest degree possible. Furthermore, in the near-term, integratability of nanodevices with silicon CMOS is a requirement due to the need for signal restoration for many logic implementations and to be compatible with the established technology and market base. This integration will be necessary at all levels from design tools and circuits to process technology.

[8] CMOS Architectural Compatibility—This criterion is motivated by the same set of concerns that motivate the CMOS technological compatibility, namely the ability to utilize the existing CMOS infrastructure. Architectural compatibly is defined in terms of the logic system and the data representation used by the alternative technology. CMOS utilizes Boolean logic and a binary data representation and ideally, an alternative technology would need to do so as well.

6.4 Potential Performance Assessment for Emerging Memory and Logic Devices

6.4.1 Methodology

Each CMOS extension and beyond-CMOS emerging research nanoscale memory and logic device technology is evaluated against each Relevance Criterion according to a single factor. For logic, this factor relates to the *projected potential performance* of a nanoscale device technology, assuming its successful development to maturity, *compared to that for silicon CMOS scaled to the end of the Roadmap*. For memory, this factor relates the *projected potential performance* of each nanoscale memory device technology, assuming its successful development to maturity, *compared to that for ultimately scaled current silicon memory technology which the new memory would displace*. Performance potential for each criterion is assigned a value from 1–3, with "3" substantially exceeding ultimately-scaled CMOS, and "1" substantially inferior to CMOS or, again, a comparable existing memory technology. These numbers are more precisely defined in that charts below. This evaluation is determined by a survey of the ERD Working Group members composed of individuals representing a broad range of technical backgrounds and expertise.

Logic—Individual Potential for Emerging Research Logic Devices Related to each Technology Relevance Criterion

Score	
3	Substantially exceeds ultimately scaled CMOS digital information processing technology (Relevance Criteria 1 – 5) 6) *or* is compatible with CMOS operating temperature 7) *or* is monolithically integrable with CMOS wafer technology 8) *or* is compatible with CMOS wafer technology (i.e., *Substantially Better than Silicon CMOS Digital Information Processing Technology*)
2	Comparable to ultimately scaled CMOS digital information processing technology (Relevance Criteria 1 – 5) 6) *or* requires a very aggressive forced air cooling technology 7) *or* is functionally integrable (easily) with CMOS wafer technology 8) *or* can be integrated with CMOS architecture with some difficulty (i.e., *Comparable to Silicon CMOS Digital Information Processing Technology*)
1	Substantially (2×) inferior to ultimately scaled CMOS digital information processing technology (Relevance Criteria 1 – 5) 6) *or* requires very aggressive liquid cooling technology 7) *or* is not integrable with CMOS wafer technology 8) *or* can not be integrated with CMOS architecture (i.e., *Substantially Worse than Silicon CMOS Digital Information Processing Technology*)

Memory—Individual Potential for Emerging Research Memory Devices Related to each Technology Relevance Criterion

Score	
3	Substantially exceeds the appropriate ultimately scaled Baseline Memory Technology (Relevance Criteria 1 – 5) 6) *or* is compatible with CMOS operating temperature 7) *or* is monolithically integrable with CMOS wafer technology 8) *or* is compatible with CMOS wafer technology (i.e., *Substantially Better than* ultimately scaled *Silicon Baseline Memory Technology*)
2	Comparable to the appropriate ultimately scaled Baseline Memory Technology (Relevance Criteria 1 – 5) 6) *or* requires a very aggressive forced air cooling technology 7) *or* is functionally integrable (easily) with CMOS wafer technology 8) *or* can be integrated with CMOS architecture with some difficulty (i.e., *Comparable to Silicon* ultimately scaled *Baseline Memory Technology*)
1	Substantially (2×) inferior to the appropriate ultimately scaled Baseline Memory Technology (Relevance Criteria 1 – 5) 6) *or* requires very aggressive liquid cooling technology 7) *or* is not integrable with CMOS wafer technology 8) *or* can not be integrated with CMOS architecture (i.e., *Substantially Worse than* ultimately scaled *Silicon Baseline Memory Technology*)

Overall Potential Assessment (OPA) = Potential Summed over the Eight Relevance Criteria for each Technology Entry

Maximum Overall Potential Assessment (OPA) = 24

Minimum Overall Potential Assessment (OPA) = 8

Overall Potential Assessment for Technology Entries

Potential for the Technology Entry is projected to be significantly better than silicon CMOS or baseline memory (compared using the Technology Relevance Criteria) (OPA ≥20)	***Potential***
Potential for the Technology Entry is projected to be slightly better than silicon CMOS or baseline memory (compared using the Technology Relevance Criteria) (OPA >16–20)	***Potential***
Potential for the Technology Entry is projected to be significantly (2x) less than silicon CMOS or baseline memory (compared using the Technology Relevance Criteria) (OPA < 16)	***Potential***

6.4.2 RESULTS

Tables ERD18 – ERD21 summarize the results of the critical review. The color scale is defined in the table above entitled "Overall Potential Assessment for Technology Entries." The color represents the overall assessment for each emerging research memory and logic technology. White indicates the ERD Working Group's judgment of a relatively high potential for a fully matured research device technology to excel compared to ultimately-scaled CMOS for logic or compared to the current memory technology to be replaced. Conversely, magenta indicates a relatively low potential. Green provides additional granularity from a moderately high potential to a lower assessment for potential. On a scale of 1–3, the numbers given in each box are the average of the responses for that technology/relevance criterion received from members of the ERD Working Group. The Overall Potential Assessment (OPA) is given in the left cell that defines the Technology Entry evaluated. The error bars indicate the average response ± the standard deviation. Assignment of the relative ratings for each Technology Entry for memory and for logic is the collective judgment of the ERD Working Group and is intended to be a guideline, but not proscriptive. These ratings taken together with the numerical tables and descriptive text are intended to provide the reader with ERD Working Group's perspective on each Technology Entry following two years of conducting several workshops, reviewing the literature, and engaging in lively discussions within the Working Group. This evaluation is illustrated in further detail for each Memory Technology in Figures ERD10a through ERD10f and for each Logic Technology in Figures ERD11a through ERD11f, ERD12a through ERD12g, and ERD13a through ERD13f.

Table ERD18 Potential Evaluation for Emerging Reseach Memory Devices

Table ERD19 Potential Evaluation - Extending MOSFETS to the end of the Roadmap

Table ERD20 Potential Evaluation - Non-conventional FETs and other Charge-based Devices

Table ERD21 Potential Evaluation: Non-FET, Non-Charge-Based "Beyond CMOS" Devices

The results displayed in the Memory and Logic Critical Review Tables ERD18 and ERD21 are interpreted briefly below beginning with the highest rated technology entry and ending with the lowest rated entry. The discussions are centered on the Technology Entries having a higher potential.

6.4.2.1 Emerging Research Memory Technologies

Each of the emerging research memory technology entries, assessed in Table ERD18, has some potential of becoming a viable, manufacturable memory. However, each has one or more challenges gating fulfillment of their potential. (Detailed discussion of these gating challenges is found in the section on Emerging Research Memory technologies. Section 4.1)

Redox Resistive Memory encompasses three different but related technologies: Electrochemical (a.k.a Conducting Bridge) technology, Thermochemical (a.k.a. Fuse/Antifuse memory and Nanothermal) technology, and Valence Change

memory. Their relationship is through mutual dependence on a chemical reduction/oxidation switching process. Redox memory is highlighted by the ERD work group (see Section 6.5.2.2 below) to offer an attractive means for scaling memory technology to and beyond the 15nm generation. Two areas of concern related to the Thermochemical component are the energy efficiency and the operational reliability. The energy efficiency challenge is related to the switching current and therefore the write energy needed to obtain the ON (set) and OFF (reset) states. The concern for operational reliability is related to the state-change mechanism of this category depending principally upon thermally activated processes. A related issue is to clarify and understand the possible role of other physical processes, e.g., electrochemical effects, in changing the resistive state of the fuse/antifuse technology. The Valence Change Memory (formerly Nanoionic memory) is another broad category of memory technology, in which the resistance switching mechanism is thought to depend principally on ionic (cation or anion) transport in either an insulator or an electrolytic ion conductor. In the first case of transport in an insulator, electronic conduction is through mixed valence metallic (cation) states in filaments formed by oxygen vacancies; in the second case, electronic conduction is along metallic filaments formed in the electrolyte. While this category is thought to be promising, two areas of concern are raised. The more serious challenge is the Operational Reliability followed by a slight concern regarding a potentially low I_{on}/I_{off} ratio. The concern with Operational Reliability is related to an inability to obtain complete reversibility of ionic drift processes exacerbated by possible thermal processes as well. As shown in Figure ERD10a, the critical evaluation of Redox did not change appreciably from 2009.

Ferroelectric memory now includes two ferroelectric memory categories: the Ferroelectric FET memory and a Ferroelectric Schottky barrier structure. In the first case, a ferroelectric dielectric forms the gate insulator of an FET, and in the second case, the device is controlled by ferroelectric Schottky barrier. In 2009, the Ferroelectric FET memory was encumbered by concerns in four areas: Operational Reliability, I_{on}/I_{off} Ratio and, to a lesser extent, Performance, and Energy Efficiency. Operational Reliability of the FeFET RAM is limited by the time dependant remnant polarization of the ferroelectric gate dielectric, particularly governed by the dielectric-semiconductor interface, which changes the threshold voltage in time. Also, the FeFET memory element may not be scalable beyond the 22nm generation. Figure ERD10b shows that evaluation for I_{on}/I_{off} ratios and energy efficiency increased in 2011, suggesting that Ferroelectric memory remains a viable contender, perhaps for m-Storage Class Memory.

Evaluation of the NEM memory structure improved in 2011, however, scalability remains as a difficult challenge of the suspended-beam Nanomechanical Memory (NEMM) structure. According to a recent study, it might be difficult to achieve low-voltage (~1 V) operation for the beam length less than 50 nm. Consequently, the NEMM may not be competitive in the long term. (Figure ERD10c)

Although the Mott Memory is seen to have some potential, three important challenges are identified: Scalability, Operational Reliability, and I_{on}/I_{off} Ratio. Evaluation of this memory category declined considerably (> 1.5 in Overall Potential Assessment or OPA) from the 2007 evaluation to 2009 and declined an additional 0.7 in 2011, as shown in Figure ERD10d.

Neither of the last two memory technologies evaluated, Macromolecular Memory and Molecular Memory, is considered to have long range potential for high-performance computing due to low expectations for Speed, Operational Reliability, and I_{on}/I_{off} Ratio.

6.4.2.2 Emerging Research Logic Technologies

The results for Emerging Research Logic and Alternative Information Processing technologies are displayed in Table ERD 19-21 and Figures ERD11a–11f, ERD12a-12g, and ERD13a-13f. While the color coding highlights eight information processing or logic technologies as being most promising, the top five are clustered within one Overall Potential Assessment (OPA) point (OPA = 17.9 to 18.9). These top four, (NW-FETs, CNT-FETs, Ge & III-V (GaPSb and GaInSb)) p-channel MOSFETs, InP and Ge n-channel MOSFETs) are all electron charge-based FET structures targeting extension of CMOS to the end of the current Roadmap. This assessment is consistent with the preliminary results of a study discussed in this Section (Section 6.2.2) in which electron charge-based and non-charge based devices are benchmarked using a number of CMOS logic gate configurations. The lower three of this green-colored sub-group (Tunnel MOSFETs, IMOS, and Negative Cg FET) are clustered at a lower point (OPA =16.9 to 16.3). GNR MOSFETs are between these two groups at an OPA of 17.4. The last eleven of the Logic group, colored magenta, are not rated to have a long range potential performance exceeding that for ultimately scaled CMOS.

Nanowire FETs offer an appealing approach to scaling CMOS with attributes similar to CNT FETs, including excellent gate control of the channel minimizing short channel effects. Nanowire FETs also have challenges similar to those for CNTs related to well controlled growth and fabrication as well as parasitic resistances and capacitances. The 2011 and 2009 critical assessments for Nanowire FETs are quite similar and not too different from the 2007 assessment, as shown in Figure ERD11a.

Carbon Nanotube FETs offer high carrier mobility, high quasi-ballistic charge carrier velocity, and a tubular structure ideally suited for minimized short channel effects (i.e., abrupt turnoff of channel current), if a gate-all-around process is developed. Other challenges include the ability to obtain single wall semiconducting nanotubes, control the bandgap energy, control growth of nanotube position/direction, and control the carrier type and density. As shown in Figure ERD11b, the critical assessment of CNTs in 2011 is similar to that of 2009 and 2007, with the exception of CMOS Architectural Compatibility, which increased in 2009.

Semiconductor materials proposed to replace the silicon channel and source/drain in an otherwise silicon MOSFET technology have gained attention for their potential to enable performance scaling of CMOS to the end of the current Roadmap. These materials include carbon nanotubes, germanium, III-V compound semiconductors, and graphene nanoribbons. Carbon nanotubes are discussed above and graphene nanoribbons are discussed below. Germanium and III-V compound semiconductors offer similar advantages and face similar challenges. In particular, a III-V n-channel MOSFET can be integrated with a germanium p-channel MOSFET to maximize high n-channel III-V and p-channel germanium carrier mobilities and carrier velocities. Principal challenges include several material and fabrication process issues discussed in the ERM chapter. Figures ERD11c and ERD11d (Ge and InP n-channel MOSFETs) and (GaInSb and GaPSb p-channel MOSFETs) indicate very similar (rather positive) assessments for these technologies from 2009 to 2011.

While graphene nanoribbon (GNR), used as a channel replacement material, offers an attractive alternative, it faces several important challenges discussed above in the Logic Section (Section 4.2) and in the ERM chapter. Assuming solution to these several materials and process challenges (including development of a viable epitaxial growth technology), GNR may not offer sufficient device gain to be competitive. This assessment is illustrated in Figure ERD11e.

The Tunnel MOSFET offers an appealing concept for substantially lowering the energy dissipated in a switching device by substituting a tunneling process for a thermionic process for injecting charge carriers into the channel of a MOSFET. The major challenge is to simultaneously obtain a sharp subthreshold slope (much less than 60mV/decade) with a high on current, I_{on}. This is discussed in detail above in the Logic Section (Section 4.2) and in the ERM chapter. Further the Tunnel FET may have a problem with Operational Reliability due to high sensitivity of device operation to slight variations of the tunnel structure and the resulting tunnel barrier. This assessment is illustrated in Figure ERD11f.

The IMOS device offers an advantage similar to that of the Tunnel MOSFET, namely to reduce the subthreshold slope, but faces several additional serious concerns related to Scalability, Speed, and Operational Reliability. Assessments illustrating these concerns are given in Figure ERD12a.

The negative Cg MOSFET offers another approach to lowering the energy dissipated in switching a MOSFET, and has overcome a major challenge of identifying a gate dielectric (a ferroelectric and an oxide) that demonstrated a negative capacitance in a MOSFET gate stack. A recent experiment has established proof of concept of <60 mV/decade operation using the principle of negative capacitance[562]. In addition, recent demonstration[563] of capacitance enhancement in a series combination of a ferroelectric and dielectric capacitor, composed of single crystalline oxides grown epitaxially, also demonstrates a number of predictions of negative capacitance theory. The major challenge concerns identification of appropriate materials (ferroelectrics and/or oxides) that can provide the best voltage swing with minimal hysteresis. A second significant challenge comes from the integration of high quality single crystalline ferroelectric oxides on Si. Although, a negative capacitance MOSFET with organic ferroelectric such as polyvinylidene Fluoride (PVDF) already has been demonstrated, crystalline oxides are more attractive due to their well-behaved and sharp hysteresis and better dynamic response. Another important concern, however, is the Operational Reliability as shown in ERD12b.

The Atomic Switch is classified as an electrochemical switch using the diffusion of metal cations and their reduction/oxidation processes to form/dissolve a metallic conductive path. One advance in this field is development of three-terminal atomic switches[564,565], characterized by high I_{on}/I_{off} ratio, low ON-resistance, nonvolatility, and low power consumption. Switching speed, cyclic endurance, uniformities of the switching bias voltage and resistances both for the on-state and the off-state should be improved for general usage as a logic device. Although basic phenomena in their switching have been reported[566], establishment of the device physics still seems to be the most important and urgent issue. In addition, development of the architecture for nonvolatile devices is desired same as with other nonvolatile logic devices. The 2011 assessment shown in Figure ERD12c is similar to that for 2009, except the energy efficiency is lower in the new assessment.

The Mott field-effect transistor (Mott FET) utilizes a phase change in a correlated electron system induced by a gate voltage as the fundamental switching paradigm[567,568]. Mott FETs could have a similar structure as conventional semiconductor FETs, with the semiconductor channel materials being replaced by correlated electron materials.

Correlated electron materials can undergo Mott insulator-to-metal phase transitions under an applied electric field. Besides electric field excitation, the Mott phase transition can also be triggered by photo- and thermal-excitations for potential optical and thermal switches. Challenges with correlated electron oxide Mott FETs include fundamental understanding of gate oxide-functional oxide interfaces and local energy bandstructure changes in the presence of electric fields. Understanding the electronic arrest mechanisms while de-coupling from structural Peierls distortions is of interest. The Mott FET is a new device entry, therefore there is no comparison with previous assessments. (Figure ERD12d)

The Spin Transistor category represents two different device structures. One is the Spin FET and the other is the Spin MOSFET. In both instances the device complements the usual field effect behavior of a MOSFET with additional functionality of magnetoresistive devices. Consequently, the Spin Transistors may enable more complex transfer functions with fewer devices than CMOS is able to provide. Notwithstanding considerable focused research on developing these devices, none have been realized experimentally. Further, there are concerns with the potential Scalability, Gain, Operational Reliability, and CMOS technological compatibility of these devices, as illustrated in Figure ERD12e. The 2011 assessment of the Spin Transistor is similar to the 2009 assessment.

Micro/Nano-Electro-Mechanical (M/NEM) Switches (or relays) are devices in which operation is based on the displacement of a solid beam under the influence of electrostatic force in order to create a conducting path between two electrodes. M/NEM relays feature two key properties for logic computation which are unavailable in MOSFETs: *zero leakage* and *zero subthreshold swing*[569,570]. The first property indicates zero standby energy dissipation, while the second suggests the potential to scale V_{DD} aggressively (without degrading the on-current to off-current ratio) and hence reduce significantly the dynamic energy consumption as well. The performance of M/NEM MOSFETs is improved by constant-field scaling, which increases speed while decreasing dynamic energy dissipation and area[571]. The main advantage of M/NEM switches in terms of scaling resides in their *improved energy efficiency* as well as in their potential for 3-D integration, both of which may allow increased functional density for a given substrate real-estate [572]. This is especially true for memory applications[573]where hysteresis and sticking lead to an even better functional density. Many issues remain to be solved in order to apply M/NEM relays to logic applications. The most important issue is nanoscale contact reliability, since logic circuits would require the relays to operate correctly over ~10^{16} "hot switching" cycles where the drain voltage is as high as the gate voltage. High impact velocity at the end of pull-in and the resultant "tip bouncing" (which also increases the effective switching delay) can aggravate the problem[574] . Another significant issue for NEM relays is the presence of surface forces (van der Waals or Casimir) that can cause sticking if the restoring elastic force is not sufficiently high. Stiction is typically overcome by stiffening the beam at the expense of increasing the pull-in voltage and thus these surface forces often set the minimum energy required to switch a M/NEM relay. In order to minimize stiction and maintain clean contact spots, M/NEM relays should be hermetically sealed. There are several factors which will eventually impact the dimensional scaling of M/NEM relays. At gaps of a few nm, the subthreshold swing is already expected to degrade due to the onset of tunneling current before the unstable beam position is reached at ~2/3 of the nominal gap. With sufficiently small dimensions and gaps, the effect of Brownian beam motion may become significant; however, stiffening of the beam (*e.g.* by changing the beam material) can allow for further scaling. In relays with gaps near the limit set by tunneling (~2 nm), the long turn-off settling time could cause a significant risk for "short-circuit" current. As given in Figure ERD 12f, the M/NEMs device is viewed as having several challenges. These challenges include scaling, speed, and, particularly, Operational Reliability.

The bilayer pseudo-spin field effect transistor (BiSFET) is a recently proposed concept for an ultra-low-power and fast transistor[575] based on the possibility of a room temperature exciton (paired electron and hole) superfluid condensate in two oppositely charged (n-type and p-type) layers of graphene separated by a thin dielectric.[576] In the detailed analysis, electron occupation of the top layer or bottom layer can be treated much like spin up or down, that is as a pseudospin, and the collective effects considered here are analogous to collective spin effects in a ferromagnet. The BiSFET, however, remains only a concept based on novel predicted physics within a novel material system. And fabrication of BiSFETs with the necessary degree of control of graphene, dielectric and surface quality, of work functions, and of lithography, etc. imposes numerous challenges. Issues relating to BiSFET fabrication, some of them unique to this system and others common to other graphene technologies, as well as theory are currently being addressed.[577] (Figure ERD13a)

The last five devices evaluated [i.e., Exciton FET. Spin Torque Majority Gate, All Spin Logic, Spin Wave Devices, and Nanomagnetic Logic] are viewed to be very early in their development or as being limited by important challenges related to their projected Speed, Gain, Operational Reliability, and CMOS technological compatibility, as shown in Figures ERD13b through ERD13f. First, however, many of these proposed information processing device technologies need to be realized and demonstrated experimentally to provide a more concrete and realistic basis for their critical assessment.

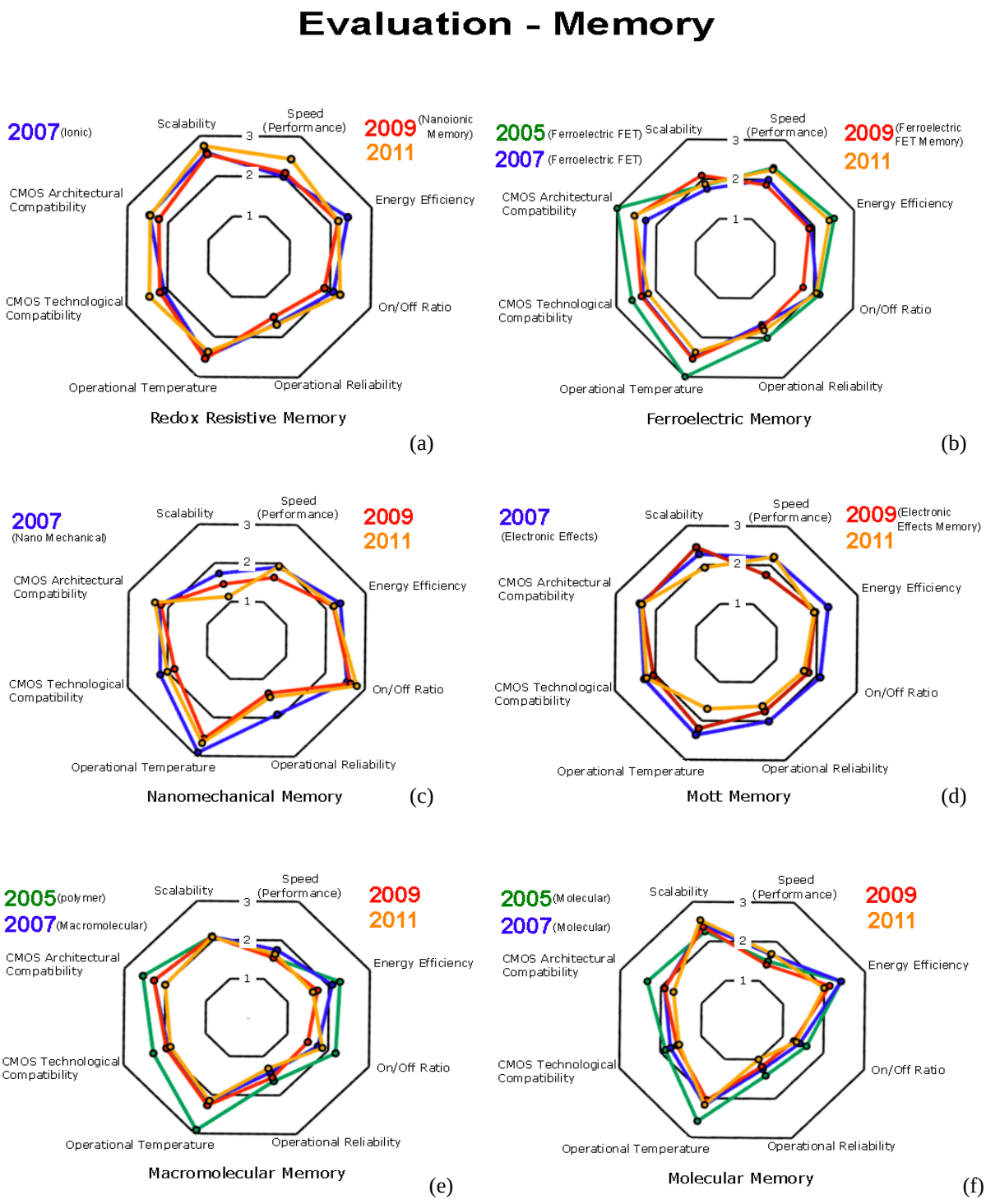
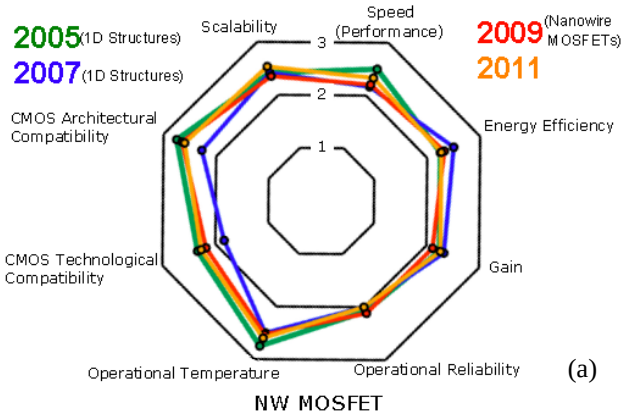
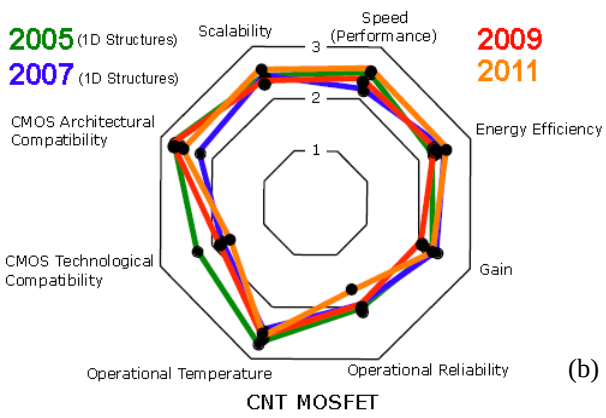


Figure ERD10 a-f Technology Performance Evaluation for a) Redox Resistive Memory, b) Ferroelectric Memory, c) Nanomechanical Memory, d) Mott Memory e) Macromolecular Memory, and f) Molecular Memory.

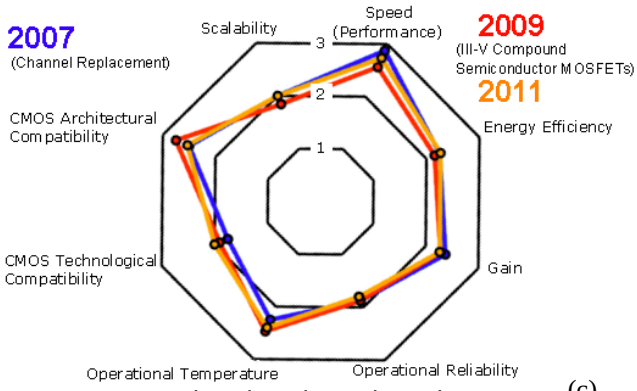
Evaluation – Logic MOSFET



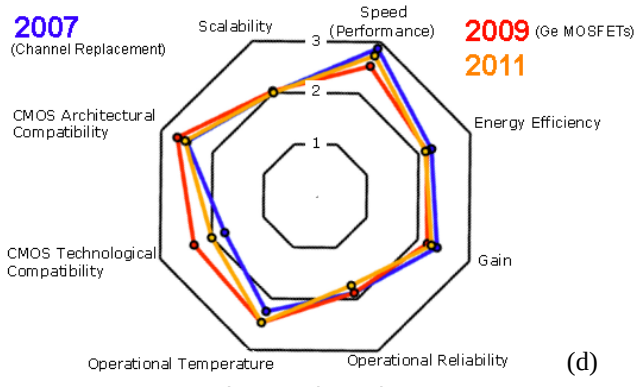
(a) NW MOSFET



(b) CNT MOSFET



GaInSb and GaSbP p-Channel MOSFET (c)



Ge and InP n-Channel MOSFET (d)

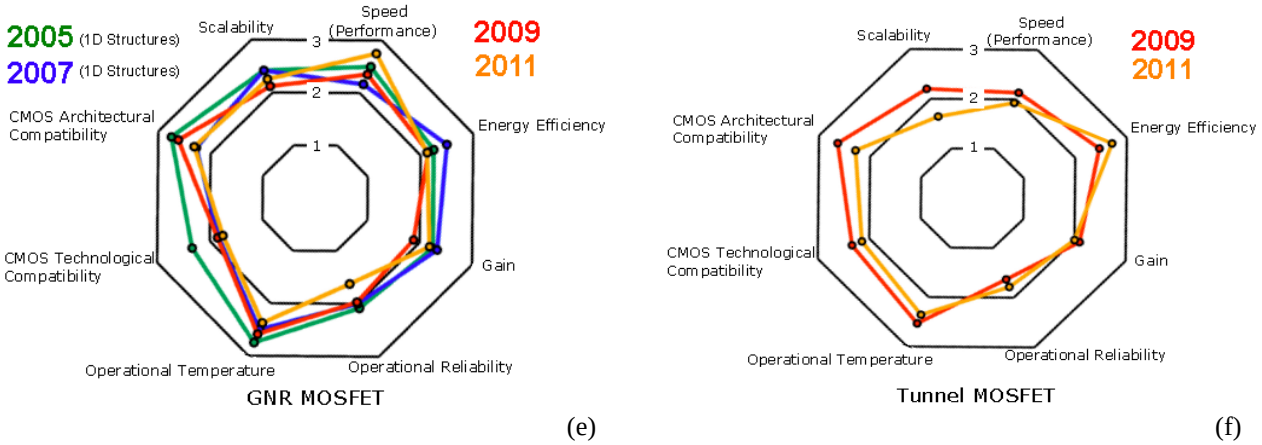


Figure ERD 11 a-f Technology Performance Evaluation for a) Nanowire MOSFETs, b) CNT MOSFETs, c) GaInSb and GaSbP p-channel MOSFETs, d) Ge and InP n-channel MOSFETs, e) GNR MOSFETs, and f) Tunnel MOSFETs

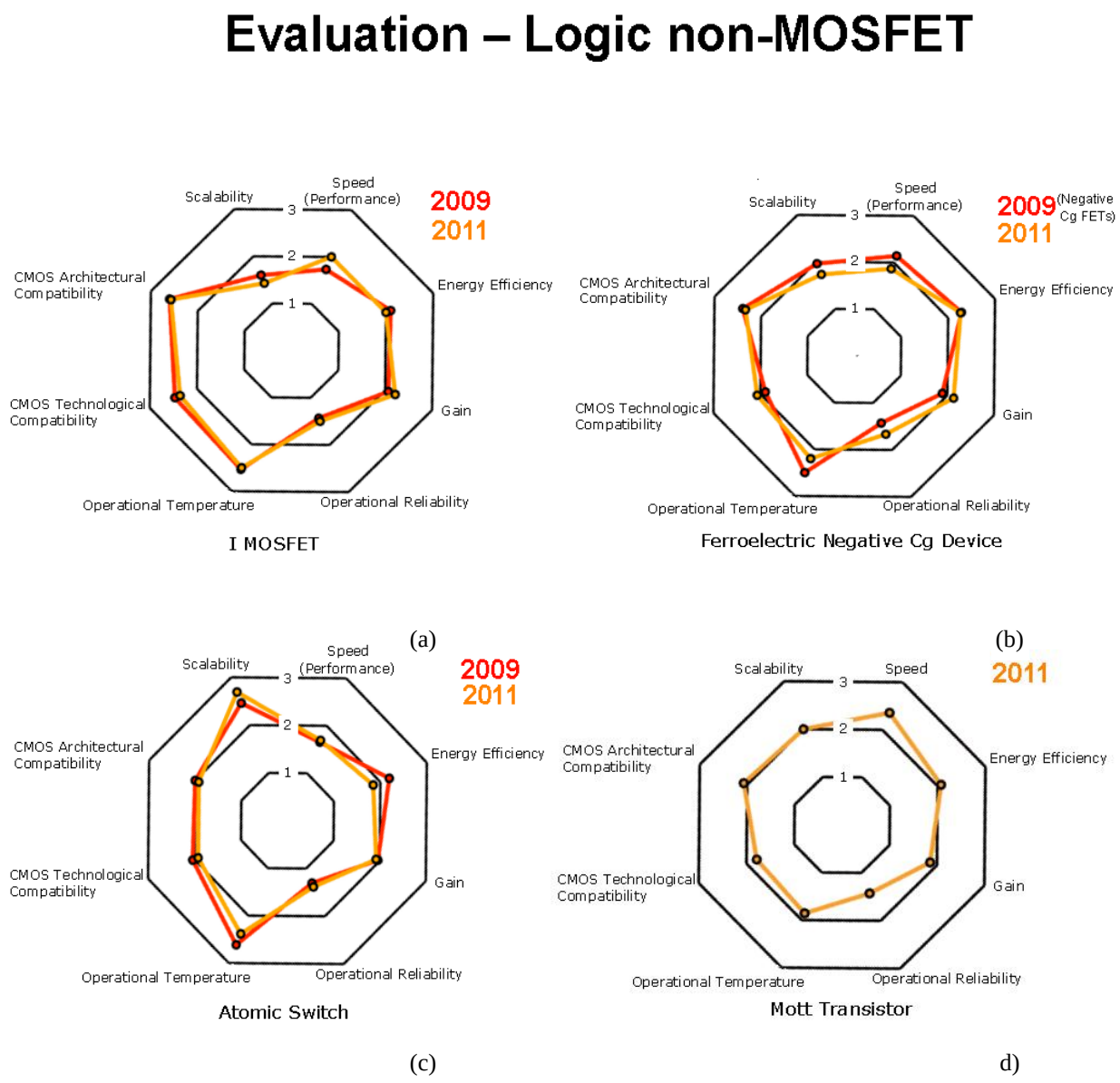
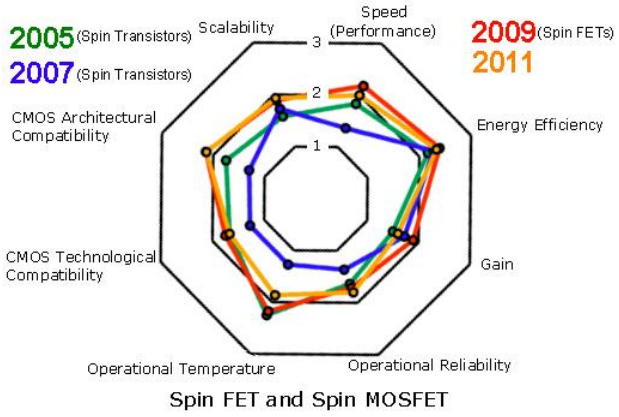
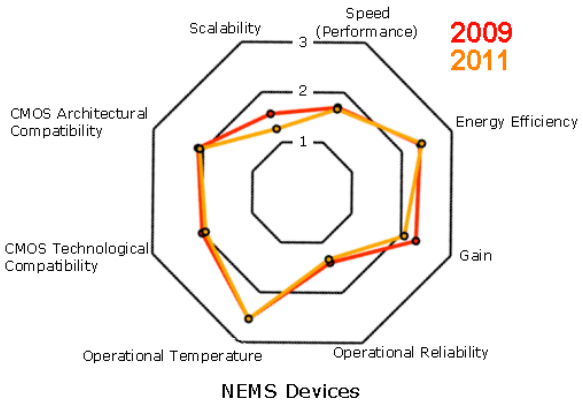


Figure ERD 12a-d Technology Performance Evaluation for a) I MOSFET, b) Ferroelectric Negative Cg MOSFET, c) Atomic Switch, and d) Mott Transistor.

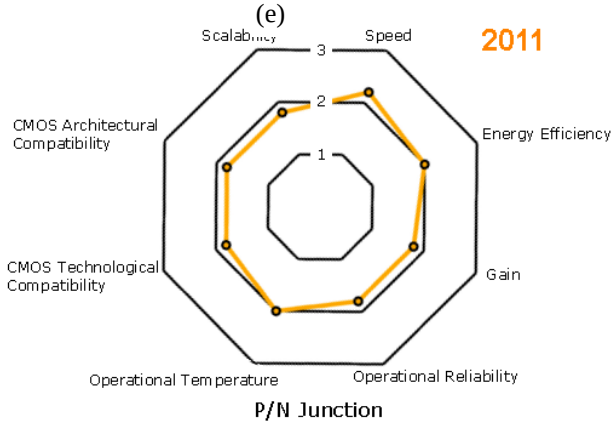
Evaluation – Logic non-MOSFET



(e)



(f)



(g)

Figure ERD 12e-g Technology Performance Evaluation for e) Spin FET and Spin MOSFET, f) NEMS Device, and g) P/N Junction Device.

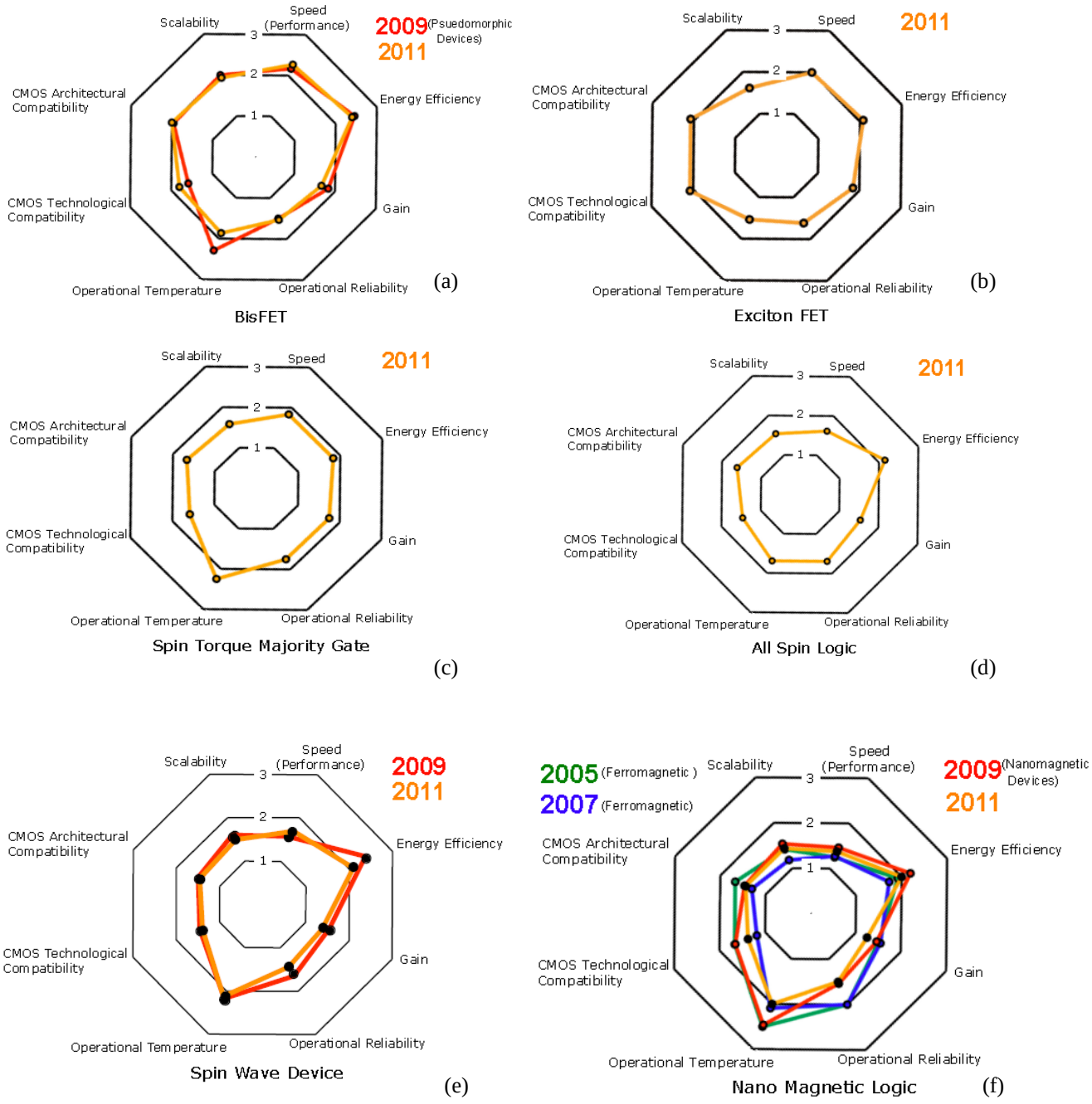


Figure ERD13a-f Technology Performance Evaluation for a) BiSFET, b) Exciton FET, c) Spin Torque Majority Gate, d) All Spin Logic Device, e) Spin Wave Device, and f) Nanomagnetic Logic Device.

6.5 MEMORY AND LOGIC TECHNOLOGIES HIGHLIGHTED FOR ACCELERATED DEVELOPMENT

6.5.1. INTRODUCTION

The ITRS' International Roadmap Committee (IRC), recognizing that it is timely to accelerate development of one or two of the more promising proposals for new well-defined information processing devices, requested the Emerging Research Devices and Emerging Research Materials working groups to recommend one or two of the emerging research memory and information processing device technologies with high potential and sufficient maturity to justify their accelerated development. In response, the ERD/ERM working groups conducted two studies and two related workshops. One was entitled "*Potential & Maturity of Selected Emerging Research Memory Technologies"* and the other "*Maturity Evaluation for Selected beyond CMOS Emerging Technologies.* The objective of these studies was to evaluate nine candidate emerging research memory and seven "beyond CMOS" information processing technologies, followed by near-consensus selection of one or two of each having high potential and sufficient maturity for enabling a paradigm shift in information processing technology. Also, the recommended technologies would need to be manufacturable within 5 – 10 years.

Two candidate memory technologies were recommended: Spin Transfer Torque Magnetostatic RAM (STT-MRAM) and Redox Resistive RAM. The STT-MRAM has been transferred to the PIDS chapter, and the Redox Resistive RAM remains in the ERD and ERM chapters.

The single candidate Information Processing Technology selected was "Carbon-based Nanoelectronics". Focused research necessary to develop either carbon nanotubes or graphene for MOSFETs may provide a technology platform and requisite scientific knowledge base to enable discovery of a new paradigm for processing information for "beyond CMOS."

6.5.2. HIGHLIGHTED EMERGING RESEARCH MEMORY AND LOGIC TECHNOLOGIES

6.5.2.1. STT-MRAM

Spin Transfer Torque memory (STT-MRAM) technology is emerging as a very promising approach to nonvolatile memory applications, motivated by potentially increasing the bit density and lowering the power dissipation beyond that attainable by the magnetostatic RAM or MRAM. Other appealing features making STT-MRAM a particularly attractive non-volatile memory candidate, particularly for embedded applications, include: 1) a simple integration scheme with the backend CMOS process; 2) By adding only 3-4 additional masks, the process requires no front end device integration that interferes with the CMOS devices and no high-voltage devices; 3) The STT – MRAM cell may be integrable with a vertical MOSFET select transistor thereby reducing the footprint of the memory cell from $21F^2$ (current value) to $4F^2$.

While the STT-MRAM offers clear advantages, it also faces several important challenges. First and foremost is the ability to scale STT-MRAM to obtain a competitive cost/bit together with adequate performance parameters. The footprint or cell size of the STT-MRAM is determined by the layout of the select transistor, which, in turn, must be wide enough to provide the required program current. Consequently, the program current, which drives the power dissipation and the dimensional scaling of the STT-MRAM cell, must be reduced to < 50μA (ideally ~10μA) to be competitive as a cost/bit technology. Furthermore, its switching speed is rather slow and its meaningful application to logic that is highly scalable beyond CMOS is seen as very difficult. Another challenge is that the STT-MRAM cell structure requires 10-12 different layers, deposited by physical vapor deposition processes for a thickness of ~ 0 .8 – 2.0nm.

6.5.2.2. REDOX RERAM

Redox ReRAM MIM structures are deceptively simple and, therefore, very appealing for their low cost/bit and their scaling potential. However, their commercialization is facing solution to some important challenges. First and foremost, one needs a better understanding and control of the physical SET/RESET processes through development of accurate, quantitative models. A forming process now needed for many of these technologies should be eliminated, and they need better endurance and data retention time.

The category of "Redox RAM" encompasses a wide variety of MIM structures and materials loosely connected by the fact that they share reduction/oxidation (redox) electrochemistry as an important component of their physical mechanism for changing the resistance state from high to low or the reverse. These redox electrochemical mechanisms can operate in the bulk I-layer, along conducting filaments in the I-layer, and/or at the I-layer/metal contact interfaces in the MIM structure.

Until recently, this category (Redox RAM) was further divided into two subcategories, "Thermochemical Mechanism" (i.e. Fuse/antifuse) and "Nanoionic" (i.e. Valence Change Mechanism and Electrochemical Metallization). The

distinction between these two subcategories was whether the diffusion or drift of O anions, Ag^+ and Cu^+ cations, and Vo oxygen vacancies in the insulator or I-layer is driven by a thermal gradient diffusion mechanism or by an electrostatic drift field driving the ion drift and the redox electrochemistry mechanisms. In many cases both mechanisms are operative and it's just a matter of which is dominant. If the thermal gradient mechanism is dominant, the resistance switching is unipolar. Conversely, if the applied electric field drives the redistribution of charged species, the resistance switching is bipolar. Because this distinction is so subtle and because both mechanisms are likely operative, these two subcategories were combined into the category of "Redox RRAM".

6.5.2.3. HIGHLIGHTED EMERGING LOGIC TECHNOLOGY – CARBON-BASED NANOELECTRONICS

Carbon-based Nanoelectronics has a major advantage in that the science and technologies resulting from accelerated development of CNTs and GNRs for MOSFET applications can provide a substantial basis for exploring and developing new physical phenomena in these materials for "Beyond CMOS" information processing paradigms. The field of Carbon-based Nanoelectronics has bifurcated into two related topics: carbon nanotubes and graphene. Carbon nanotubes, based on one or more layers of sp^2 bonded carbon atoms to form either single-wall or multi-wall cylinders of varying chirality, can be metallic or semiconducting. Exploration of CNTs for MOSFET applications has shown CNTs to have excellent electron transport properties, exhibiting ballistic transport over substantial distances. Using the cylindrical shape of CNTs in a vertical MOSFET format enables the ideal MOSFET structure, a "gate all around" transistor, which provides near ideal gate control of the channel electrostatics. This would minimize short channel effects, e.g. DIBL. CNTs are also amenable to band-to-band-tunneling MOSFETs which could provide subthreshold slopes, S << 60mV/dec, leading to lower dissipated power. The major issue that has challenged CNT MOSFETs for some time is lack of a growth process to control placement, alignment, chirality, conductivity, diameter, single or multiple wall, energy bandgap, etc.

The second field in carbon-based nanoelectronics is based on graphene, a single planar layer of sp^2 bonded carbon atoms. A graphene nanoribbon can be imagined as a CNT cut lengthwise and opened to form a mono-atomic ribbon or sheet of sp^2 bonded carbon atoms. Similar to CNT MOSFETs, a graphene nanoribbon (GNR) MOSFET exhibits ballistic electron transport and excellent MOSFET properties for analog or RF applications. However, while the CNT technology requires multiple CNT MOSFETs connected in parallel to achieve a desired I_{on}, the GNR MOSFET can achieve the required I_{on} by increasing the width of the transistor. Graphene also exhibits some new physical phenomena (e.g. "pseudospin", zero effective mass charge carriers, etc.) that may be exploited to realize a new charge-transport independent paradigm for information processing. Major issues challenging development of graphene are lack of a reasonable process for growing graphene epitaxially over large areas on a suitable substrate and an inability to turnoff the channel of a MOSFET making GNR MOSFETs currently unsuitable for use as digital logic devices.

7. PROCESSING

7.1 INTRODUCTION

In considering the many disparate new approaches proposed to provide order of magnitude scaling of information processing beyond that attainable with ultimately scaled CMOS, the Emerging Research Devices Working Group proposes the following comprehensive set of guiding principles. We believe these "Guiding Principles" provide a useful structure for directing research on any "Beyond CMOS" information processing technology to dramatically enhance scaling of functional density and performance while simultaneously reducing the energy dissipated per functional operation. Further this new technology would need to be realizable using a highly manufacturable fabrication process.

7.2 GRAND CHALLENGES

7.2.1 COMPUTATIONAL STATE VARIABLE(S) OTHER THAN SOLELY ELECTRON CHARGE

These include spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states. The estimated performance comparison of alternative state variable devices to ultimately scaled CMOS should be made as early in a program as possible to down-select and identify key trade-offs.

7.2.2 NON-THERMAL EQUILIBRIUM SYSTEMS

These are systems that are out of equilibrium with the ambient thermal environment for some period of their operation, thereby reducing the perturbations of stored information energy in the system caused by thermal interactions with the environment. The purpose is to allow lower energy computational processing while maintaining information integrity.

7.2.3 NOVEL ENERGY TRANSFER INTERACTIONS

These interactions would provide the interconnect function between communicating information processing elements. Energy transfer mechanisms for device interconnection could be based on short range interactions, including, for example, quantum exchange and double exchange interactions, electron hopping, Förster coupling (dipole–dipole coupling), tunneling and coherent phonons.

7.2.4 NANOSCALE THERMAL MANAGEMENT

This could be accomplished by manipulating lattice phonons for constructive energy transport and heat removal.

7.2.5 SUB-LITHOGRAPHIC MANUFACTURING PROCESS

One example of this principle is directed self-assembly of complex structures composed of nanoscale building blocks. These self-assembly approaches should address non-regular, hierarchically organized structures, be tied to specific device ideas, and be consistent with high volume manufacturing processes.

7.2.6 ALTERNATIVE ARCHITECTURES

In this case, architecture is the functional arrangement on a single chip of interconnected devices that includes embedded computational components. These architectures could utilize, for special purposes, novel devices other than CMOS to perform unique functions.

8 ENDNOTES/REFERENCES

[1] V. V. Zhirnov, R. K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Bräuhaus, C. Schindler and R. Waser, "Memory Devices: Energy-Space-Time Trade-offs", *Proc. IEEE* 98 (2010) 2185-2200

[2] H. Ishiwara, "Current status of ferroelectric-gate Si transistors and challenge to ferroelectric-gate CNT transistors", *Curr. Appl. Phys.* 9 (2009) S2-S6

[3] A. Gerber, M. Fitsilis, R. Waser, T. J. Reece, E. Rije, S. Ducharme, H. Kohlstedt, "Ferroelectric field effect transistors using very thin ferroelectric polyvinylidene fluoride copolymer films as gate dielectrics", *J. Appl. Phys.* 107 (2010) 124119

[4] T. P. Ma, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?", *IEEE Electron. Dev. Lett.* 23 (2002) 386-388

[5] J. Hoffman, X. Pan, J. W. Reiner, F. J. Walker, J. P. Han, C. H. Ahn, and T. P. Ma, "Ferroelectric field-effect transistors for memory applications", *Adv. Mat.* 22 (2010) 2957-2961

[6] Y. Kaneko, H. Tanaka, M. Ueda, Y. Kato, "A dual-channel ferroelectric-gate field-effect transistor enabling NAND-type memory characteristics", *IEEE Trans. Electron. Dev.* 58 (2011) 1311-1318

[7] P. Heremans, G. H. Gelinck, R. Müller, K-J Baeg, D-Y. Kim, Y-Y Noh, "Polymer and organic nonvolatile memory devices", *Chem. Mat.* 23 (2011) 341-358

[8] W. Y. Fu et al. "Intrinsic memory function of carbon nanotube-based ferroelectric field-effect transistor", *Nano Letters* 9 (2009) 921

[9] J. I. Sohn, S. S. Choi, S. M. Morris, JS Bendall, H. J. Coles, W. K. Hong, G. Jo, T. Lee, M. E. Welland, "Novel Nonvolatile Memory with Multibit Storage Based on a ZnO Nanowire Transistor", *Nano Lett.* 10 (2010) 4316-4320

[10] Y. Zheng, G. X. Ni, S. Bae, "Wafer-scale graphene/ferroelectric hybrid devices for low-voltage electronics", *EPL* 93 (2011) 17002

[11] M. Fitsilis, Y. Mustafa, R. Waser, "Scaling the ferroelectric field effect transistor", *Integrated Ferroelectrics* 70 (2005) 29-44

[12] H. Kohlstedt, N. A. Pertsev, J. Rodriguez Contreras, and R. Waser "Theoretical current-voltage characteristics of ferroelectric tunnel junctions", *Phys. Rev. B*, 72 (2005) 125341

[13] P. W. M. Blom, R. M. Wolf, J. F. M. Cillessen, and M. P. C. M. Krijn, "Ferroelectric Schottky Diode", *Phys. Rev. Lett.* 73 (1994) 2107.

[14] E. M. Bourim, S. Park, X. Liu, K. P. Biju, H. Hwang, A. Ignatiev, "Ferroelectric polarization effect on Al-Nb codoped $Pb(Zr_{0.52}Ti_{0.48})O_3/Pr_{0.7}Ca_{0.3}MnO_3$ heterostructure resistive memory", *Electrochem. and Solid-State Lett.* 14 (2011) H225-H228

[15] A. Q. Jiang, C. Wang, K. J. Jin, X. B. Liu, J. F. Scott, C. S. Hwang, T. A. Tang, H. B. Lu, G. Z. Yang, "A resistive memory in semiconductiong $BiFeO_3$ thin-film capacitors", *Adv. Mat.* 23 (2011) 1277-1281

[16] E. J. Ng; J. B. W. Soon; N. Singh; et al., "High density vertical silicon NEM switches with CMOS-compatible fabrication", *Electron. Lett.* 47 (2011) 759-760

[17] J. Andazane et al., "Two-terminal nanoelectromechanical devices based on germanium nanowires", *Nano Lett.* 9 (2009) 1824

[18] K. Lee and W. Y. Choi, "Nanoelectromechanical Memory Cell (T Cell) for Low-Cost Embedded Nonvolatile Memory Applications", *IEEE Trans. Electron Dev.* 58 (2011) 1264-1267

[19] O. Loh; X. Wei; C .Ke; et al. "Robust Carbon-Nanotube-Based Nano-electromechanical Devices: Understanding and Eliminating Prevalent Failure Modes Using Alternative Electrode Materials", *SMALL* 7 (2011) 79-86

[20] W. Y. Choi, T. Osabe and T-S. K. Liu, "Nano-electro-mechanical nonvolatile memory (NEMory) cell design and scaling", *IEEE Trans. Electron Dev.* 55 (2008) 3482-3488

[21] W. Xiang and C. Lee, "Nanoelectromechanical torsion swith of low operation voltage for nonvolatile memory application", *Appl. Phys. Lett.* 96 (2010) 193113

[22] J. Rubin, R. Sundararaman, M. Kim, and S. Tiwari, " A low-voltage torsion nanorelay", *IEEE Electron Dev. Lett.* 32 (2011) 414-416

[23] T. Nagami, Y. Tsuchiya, K. Uchida, H. Mizuta, S. Oda, "Scaling analysis of nanoelectromechanical memory devices", *Jap. J. Appl. Phys.* 49 (2010) 044304

[24] M. A. Garcia-Ramirez, Y. Tsuchiya, H. Mizuta, "Hybrid circuit analysis of a suspended gate silicon nanodot memory (SGSNM) cell, *Microelectronic Eng.* 87 (2010) 1284-1286

[25] S. W. Lee, S. J. Park, E. E. B. Campbell, and Y. W. Park, "A fast and low-power microelectromechanical system-based non-volatile memory device", *Nature Communications* 2 (2011) 220

[26] W. Y. Choi and T-J. K. Liu, "Reliability of nanoelectromechanical nonvolatile memory (NEMory) cells", *IEEE Electron Dev. Lett.* 30 (2009) 269-271

[27] R. Waser, R. Dittman, G. Staikov, and K. Szot, "Redox-based resistive switching memories – nanoionic mechanisms, prospects, and challenges", *Adv. Mat.* 21 (2009) 2632-2663

[28] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides", *Proc. IEEE* 98 (2010) 2237-2251

[29] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki. "Electrochemical metallization memories-fundamentals, applications, prospects", *Nanotechnology*, 22 (2011) 254003/1-22.

[30] D. Ielmini, R. Bruchhaus, and R. Waser, „Thermochemical resistive switching: materials, mechanisms, and scaling projections", *Phase Transitions* 84 (2011) 570-602.

[31] J. Y. Yang, M.-X. Zhang, J. P. Strachen, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, "High switching endurance in TaOx memristive devices", *Appl. Phys. Lett.* 97 (2010) 232102

[32] M-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y-B. Kim, C-J. Kim, D. H. Seo, S. Seo, U-I. Chung, I-K. Yoo, K. Kim, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5-x/TaO2-x bilayer structures", *Nature Mat.* July 2011.

[33] D. Ruzmetov, G. Gopalakrishnan, J. Deng, V. Narayanamurti, S. Ramanathan, "Electrical triggering of metal-insulator transition in nanoscale vanadium oxide junctions", *J. Appl. Phys*. 106 (2009) 083702

[34] S. D. Ha, G. H. Aydogdu, and S. Ramanathan, "Metal-insulator transition and electrically driven memristive characteristics of $SmNiO_3$ thin films", *Appl. Phys Lett*. 98 (2011) 012105

[35] K-H. Xue, C. A. Paz de Araujo, J. Celinska, C. McWilliams, "A non-filamentary model for unipolar switching transition metal oxide resistance random acess memories", *J. Appl. Phys*. 109 (2011) 091602

[36] J. Celinska, C. McWilliams, C. Paz de Araujo, K-H. Xue, "Material and process optimization of correlated electron random access memories", *J. Appl. Phys*. 109 (2011) 091603

[37] C. R. McWilliams, J. Celinska, C. A. Paz de Araujo, K-H. Xue, "Device characterization of correlated electron random access memories", *J. Appl. Phys.*109 (2011) 091608

[38] L. Cario, C. Vaju, B. Corraze, V. Guiot, E. Janod, "Electric-field-induced resistive switching in a family of Mott Insulators: Toward a new class of RRAM memories", *Adv. Mat*. 22 (2010) 5193-5197

[39] A. Ohtomo and H. Y. Hwang, "A high-mobility electron gas at the LaAlO3/SrTiO3 heterointerface", *Nature* 427 (2004) 423-426

[40] S. Thiel, G. Hammerl, A. Schmehl, C. W. Schneider, J. Mannhart, "Tunable quasi-two-dimensional electron gas in oxide heterostructures", *Science* 313 (2006) 1942-626

[41] M. K. Niranjan, Y. Wang, S. S. Jaswal, and E. Y. Tsymbal, "Prediction of a switchable two-dimensional electron gas at ferroelectric oxide interfaces', *Phys. Rev. Lett*. 103 (2009) 016804

[42] J. W. Park, D. F. Bogorin, C. Cen, D. A. Felker, Y. Zhang, C. T. Nelson, C. W. Bark, C. M. Folkman, X. Q. Pan, M. S. Rzchowski, J. Levy, C. B. Eom, "Creation of a two-dimensional electron gas at an oxide interface on silicon", *Nature Communications* 1 (2010) 94

[43] J. C. Scott and L. D. Bozano, "Nonvolatile memory elements based on organic materials", *Adv. Mat.* 19 (2007) 1452-1463

[44] P. Heremans, G. H. Gelinck, R. Müller, K-J. Baeg, D-J. Kim, Y-Y. Noh, " Polymer and organic nonvolatile memory devices, *Chem. Mater*. 23 (2011) 341-358

[45] C-T. Lee, L-Z. Yu, H-C. Chen, "Memory bistable mechanisms of organic memory devices", *Appl. Phys. Lett*. 97 (2010) 043301

[46] D. Prime, S. Paul, P. W. Josephs-Franks, Gold nanoparticle charge trapping and relation to organic polymer memory devices", *Phil. Trans. R. Soc*. A (2009) 4215-4225

[47] S. Park, K. Kim, D. M. Kim, W. Kwon, J. Choi, M. Ree, "High temperature polyimide containing anthracene moiety and its structure, interface, and nonvolatile memory behavior", *ACS Appl. Mat & Interfaces* 3 (2011) 765-773

[48] S-J. Liu, Z-H. Lin, Q. Zhao, Y. Ma, H-F. Shi, M-D. Yi, Q-D. Ling, Q-L. Fan, C-X. Zhu, E-T. Kang, W. Huang, "Flash-memory effect for polyfluorenes with on-chain iridium(III) complexes, *Adv. Funct. Mat*. 21 (2011) 975-985

[49] D. I. Son, J. H. Shim, D. H. Park, J. H. Jung, J. M. Lee, W. I. Park, T. W. Kim, W. K. Choi, "Polymer-ultrathin graphite sheet-polymer composite structured flexible nonvolatile bistable organic memory devices", *Nanotechnology* 22 (2011) 295203

[50] Title: Resistive Electrical Switching of Nonvolatile Memories from Electrodeposited copper tetracyanoquinodimethane (CuTCNQ)

Author(s): Muller R.; Katzenmeyer A.; Rouault O.; et al.

Editor(s): Vincenzini P; Darrigo G

Conference: 3rd International Conference on Smart Materials, Structures and Systems Location: Acireale, ITALY Date: JUN 08-13, 2008

Source: SMART MATERIALS & MICRO/NANOSYSTEMS Book Series: Advances in Science and Technology Volume: 54 Pages: 464-469 Published: 2009

[51] Y. Kuang, R. Huang, Y. Tang, W. Ding, L. Zhang, Y. Wang, "Flexible single-component-polymer resistive memory for ultrafast and highly compatible nonvolatile memory application", IEEE Electron Dev. Lett. 31 (2010) 758-760

[52] X-H. Liu, W-S. Lu, Z-Y. Ji, D-Y. Tu, X-L. Zhu, C-Q. Xie, M. Liu, "Fabrication of a 256-bits organic memory by soft x-ray lithography", Chin. Phys. B 19 (2010) 0572204

[53] J-H. Kim, C-Y. Ahn, J-H. Lee, S-S. Lee, "Operation method verification for two-terminal polymer RAM", *J. Korean Phys. Soc*. 57 (2010) 1816-1819

[54] S. Song, B. Cho, T-W. Kim, Y. Ji, M. Jo, G. Wang, M. Choe, Y. H. Kahng, H. Hwang, and T. Lee, "Three-dimensional integration of organic resistive memory devices", *Adv. Mat*. 22 (2010) 5048-5052

[55] H. Song, M. A. Reed, T. Lee, "Single molecule electronic devices", *Adv. Mat.* 23 (2011) 1583-1608

[56] M. A. Reed, J. Chen, A. M. Rawlett, et al.,Molecular random access memory cell, *Appl. Phys. Lett*. v. 78, no. 23 (2001) 3735-3737

[57] J. M. Tour, L. Cheng, D. P. Nackashi, Y. X. Yao, A. K. Flatt, S. K. St Angelo, T. E. Mallouk, P. D. Franzon, "NanoCell electronic memories", *J. Amer. Chem. Soc*., 125 (2003): 13279-13283

[58] C. N. Lau, D. R. Stewart, R. S. Williams, M. Bockrath, Direct observation of nanoscale switching centers in metal/molecule/metal structures, *NANO LETTERS* 4 (2004): 569-572

[59] J. E. Green, J. W. Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. Delonno, Y. Luo, B. A. Sheriff, K. Xu, Y. Shik Shin, H-R. Tseng, J. F. Stoddart, and J. R. Heath, "A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimetre", *Nature* 445 (2007) 414-417

[60] T. Pro, J. Buckley, K. Huang, A. Calborean, M, Gely, G. Delapierre, G. Ghibaudo, F. Duclairoir, J-C. Marchon, E. Jalaguier, P. Maldivi, B. De Salvo, and S. Deleonibus, "Investigation of Hybrid Molecular/Silicon Memories With Redox-Active Molecules Acting as Storage Media" *IEEE Trans. Nanotechnol*. 8 (2009) 204-212

[61] S. P. Cummings, J. Savchenko, , T. Ren, "Functionalization of flat Si surfaces with inorganic compounds-Towards molecular CMOS hybrid devices", *Coordination Chem. Rev*. 255 (2011) 1587-1602

[62] V. V. Zhirnov, R. K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Bräuhaus, C. Schindler and R. Waser, "Memory Devices: Energy-Space-Time Trade-offs", *Proc. IEEE* 98 (2010) 2185-2200

[63] L. Li, K. Lu, B. Rajendran, T. D. Happ, H-L. Lung, C. Lam, and M. Chan, "Driving Device Comparison for Phase-Change Memory", *IEEE Trans. Electron. Dev*. 58 (2011) 664-671

[64] U. Gruening-von Schwerin, *Patent* DE 10 2006 040238 A1; *US Patent Application* "Integrated circuit having memory cells and method of manufacture", US 2009/012758

[65] H.-S. P. Wong, S. Raoux, S. B. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase Change Memory", *Proc. IEEE* 98 (2010) 2201-2227

[66] C. Kügeler, R. Rosezin, E. Linn, R. Bruchhaus, R. Waser, "Materials, technologies, and circuit concepts for nanocrossbar-based bipolar RRAM, *Appl. Phys*. A (2011) 791-809

[67] G. H. Kim, K. M. Kim, J. Y. Seok, H. J. Lee, D-Y. Cho, J. H. Han, and C. S. Hwang, "A theoretical model for Schottky diodes for excluding the sneak current in cross bar array resistive memory", *Nanotechnology* 21 (2010) 385202

[68] H.Toda, "Three-dimensional programmable resistance memory device with a read/write circuit stacked under a memory cell array", Patent (2009). US7606059

[69] P. Woerlee et al. "Electrical device and method of manufacturing therefore", *Patent Application* (2005).WO 2005/124787 A2

[70] S. C. Puthentheradam, D. K. Schroder, M. N. Kozicki. "Inherent diode isolation in programmable metallization cell resistive memory elements", *Appl. Phys.* A 102 (2011) 817-826

[71] E. Linn, R. Rosezin, C. Kugeler, and R. Waser, Complementary resistive switches for passive nanocrossbar memories, *NATURE MATERIALS* 9 (2010) 403-406

[72] R. Rosezin, E. Linn, L. Nielen, C. Kugeler, R. Bruchhaus, and R. Waser, "Integrated Complementary Resistive Switches for Passive High-Density Nanocross Arrays", *Electron Device Lett*. 32 (2011) 191-193

[73] M. J. Lee et al., "Two Series Oxide Resistors Applicable to High Speed and High Density Nonvolatile Memory," *Adv. Mater*. 19, 3919 (2007)

[74] S. D. Ha, G. H. Aydogdu, and S. Ramanathan, "Metal-insulator transition and electrically driven memristive characteristics of $SmNiO_3$ thin films", *Appl. Phys Lett.* 98 (2011) 012105

[75] D. Kau, et al, "A stackable cross point phase change memory," *2009 IEDM*, 617

[76] K. Gopalakrishnan, et al, "Highly Scalable Novel Access Device based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays," *2010 VLSI Symp.*, 205

[77] Y. Sasago et al. "Cross-point phase change memory with $4F^2$ cell size driven by low-contact resistivity poly-Si diode", *2009 VLSI Symp*., 24-25

[78] B. S. Simpkins, M. A. Mastro, C. R. Eddy, R. E. Pehrsson, "Surface depletion effects in semiconducting nanowires", *J. Appl. Phys*. 103 (2008) 104313

[79] V. V. Zhirnov, R. Meade, R. K. Cavin, G. Sandhu, "Scaling limits of resistive memories ", *Nanotechnology*22 (2011) 254027

[80]G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, ''Overview of Candidate Device Technologies for Storage-Class Memory,'' *IBM J. Res. & Dev*. 52, No. 4/5, 449–464 (2008).

[81]R. F. Freitas and W. W. Wilcke, ''Storage-Class Memory: The Next Storage System Technology,'' *IBM J. Res. & Dev*. 52, No. 4/5, 439–447 (2008).

[82]Y. Deng and J. Zhou, "Architectures and optimization methods of flash memory based storage systems", *J. Syst. Arch.* 57 (2011) 214-227

[83]L. M. Grupp, A. M. Caulfield, J. Coburn, S. Swanson, E. Yaakobi, P. H. Siegel, J. K. Wolf "Characterizing Flash Memory: Anomalies, Observations, and Applications", *MICRO'09*, Dec. 12-16, 2009, New York, NY, USA, p.24-33

[84]M. Franceschini, M. Qureshi, J. Karidis, L. Lastras, A. Bivens, P. Dube, and B. Abali, "Architectural Solutions for Storage-Class Memory in Main Memory," *CMRR Non-volatile Memories Workshop*, April 2010 http://cmrr.ucsd.edu/education/workshops/documents/Franceschini_Michael.pdf

[85] M. Johnson, A. Al-Shamma, D. Bosch, M. Crowley, M. Farmwald, L. Fasoli, A. Ilkbahar, et al., ''512-Mb PROM with a Three-Dimensional Array of Diode/Antifuse Memory Cells'', *IEEE J. Solid-State Circ*. 38, No. 11, 1920–1928 (2003).

[86]J. H. Yoon, E. H. Nam, Y. J. Seong, H. Kim, B. S. Kim, S. L. Min, Y. Cho, "Chameleon: A high performance Flash/FRAM hybrid solid state disk architecture", *IEEE Comp. Arch. Lett.* 7 (2008) 17-20

[87]H. G. Lee, "High-performance NAND and PRAM hybrid starage design for consumer electronics", *IEEE Trans. Consum. Electron.* 56 (2010) 112-118

[88] D. Kim, K. Bang, S-H. Ha, S. Yoon, and E-Y. Chung, "Architecture exploration of high-performance PCs with a solid-state disk", IEEE Trans. Comp. 59 (2010) 879-890

[89]http://www.fusionio.com

[90]*NVM Express Explained* - http://download.intel.com/standards/nvmhci/NVM_Express_Explained.pdf

[91]P. Ranganathan, "From Microprocessors to Nanostores: Rethinking Data-Centric Systems", *COMPUTER* 44 (2011) 39-48

[92] A. D. Franklin and Z. H. Chen, Nature Nanotechnology **5,** 858 (2010)

[93] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, Applied Physics Letters **94,** 243505 (2009)

[94] L. M. Peng, L. Ding, S. Wang, Z. Y. Zhang, Q. S. Zeng, Z. X. Wang, T. Pei, L. J. Yang, X. L. Liang, J. Shen, Q. Chen, R. L. Cui, and Y. Li, Nano Letters **9,** 4209 (2009).

[95] N. Moriyama, Y. Ohno, K. Suzuki, S. Kishimoto, and T. Mizutani, Applied Physics Express **3** (2010).

[96] M. Zheng, L. Zhang, X. M. Tu, K. Welsher, X. R. Wang, and H. J. Dai, Journal of the American Chemical Society **131,** 2454 (2009).

[97] Y. Li, L. Ding, A. Tselev, J. Y. Wang, D. N. Yuan, H. B. Chu, T. P. McNicholas, and J. Liu, Nano Letters **9,** 800 (2009).

[98] N. Moriyama, Y. Ohno, K. Suzuki, S. Kishimoto, and T. Mizutani, Applied Physics Express **3** (2010).

[99] Z. Y. Zhang, Z. X. Wang, H. L. Xu, S. Wang, L. Ding, Q. S. Zeng, L. J. Yang, T. A. Pei, X. L. Liang, M. Gao, and L. M. Peng, Nano Letters **10,** 2024 (2010).

[100] Z. Y. Zhang, S. Wang, Z. X. Wang, L. Ding, T. Pei, Z. D. Hu, X. L. Liang, Q. Chen, Y. Li, and L. M. Peng, Acs Nano **3,** 3781 (2009).

[101] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov: "Electric Field Effect in Atomically Thin Carbon Films", Science, 306, 666 (2004).

[102] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov: "Electric Field Effect in Atomically Thin Carbon Films", Science, 306, 666 (2004).

[103] Gong Gu, Shu Nie, R. M. Feenstra, R. P. Devaty, W. J. Choyke, Winston K. Chan and Michael G. Kane, "Field effect in epitaxial graphene on a silicon carbide substrate," Applied Physics Letters, Vol. 90, 253507, (2007).

[104] Kedzierski, J., Pei-Lan Hsu, Healey, P., Wyatt, P.W., Keast, C.L., Sprinkle, M., Berger, C., de Heer, W.A., "Epitaxial Graphene Transistors on SiC Substrates," IEEE Transactions on Electron Devices, Vol. 55 (8), pp. 2078 - 2085 (Aug. 2008).

[105] Lemme, M.C., Echtermeyer, T.J., Baus, M., Kurz, H., "A Graphene Field-Effect Device," IEEE Electron Device Letters, Vol. 28 (4), pp. 282 - 284 (April 2007).

[106] Seyoung Kim,, Junghyo Nah, Insun Jo, Davood Shahrjerdi, Luigi Colombo, Zhen Yao, Emanuel Tutuc, and Sanjay K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric," Applied Physics Letters, Vol. 94, 062107, (2009).

[107] Naoki Harada, Katsunori Yagi, Shintaro Sato, and Naoki Yokoyama, "A polarity controllable graphene inverter, " Applied Physics Letters, Vol. 96, 012102, (2010)

[108] L. A. Ponomarenko, F. Schedin, M. I. Katsnelson, R. Yang, E. W. Hill, K. S. Novoselov, and A. K. Geim, "Chaotic Dirac billiard in graphene quantum dots," Science, Vol. 320, 356 (2008)

[109] Inanc Meric, Melinda Y. Han, Andrea F. Young, Barbaros Ozyilmaz, Philip Kim, Kenneth L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," Nature Nanotechnology, Vol. 3, 654 - 659 (2008).

[110] Lei Liao, Yung-Chen Lin, Mingqiang Bao, Rui Cheng, Jingwei Bai, Yuan Liu, Yongquan Qu, Kang L. Wang, Yu Huang, and Xiangfeng Duan, "High-speed graphene transistors with a self-aligned nanowire gate." Nature, Vol. 467, 305 (2010)

[111] Gong Gu, Shu Nie, R. M. Feenstra, R. P. Devaty, W. J. Choyke, Winston K. Chan and Michael G. Kane, "Field effect in epitaxial graphene on a silicon carbide substrate," Applied Physics Letters, Vol. 90, 253507, (2007).

[112] Kedzierski, J., Pei-Lan Hsu, Healey, P., Wyatt, P.W., Keast, C.L., Sprinkle, M., Berger, C., de Heer, W.A., "Epitaxial Graphene Transistors on SiC Substrates," IEEE Transactions on Electron Devices, Vol. 55 (8), pp. 2078 - 2085 (Aug. 2008).

[113] Y. Q. Wu, Y.-M. Lin, K. A. Jenkins, J. A. Ot1, C. Dimitrakopoulos, D.B. Farmer, F. Xia, A. Grill, D.A. Antoniadis, and Ph. Avouris, "RF performance of short channel graphene field-effect transistor, " IEEE IEDM Technical Digest 2010, p.226 (2010).

[114] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, *Science*, 324, 1312 (2009).

[115] Yanqing Wu, Yu-ming Lin, Ageeth A. Bol, Keith A. Jenkins, Fengnian Xia, Damon B. Farmer, Yu Zhu, and Phaedon Avouris, Nature 472, 74 (2011)

[116] Xu Du, Ivan Skachko, Anthony Barker, and Eva Y. Andrei, Nature Nanotechnol. 3, 491 (2008)

[117] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, Phys. Rev. Lett. 101, 096802 (2008)

[118] Eduardo V. Castro, H. Ochoa, M. I. Katsnelson, R.V. Gorbachev, D. C. Elias, K. S. Novoselov, A. K. Geim, and F. Guinea, Phys Rev. Lett. 105, 266601 (2010)

[119] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov: "Electric Field Effect in Atomically Thin Carbon Films", Science, 306, 666 (2004).

[120] Jian-Hao Chen, Chaun Jang, Shudong Xiao, Masa Ishigami, Michael S. Fuhrer, Nature Nanotechnol. 3, 206 (2008)

[121] Xu Du, Ivan Skachko, Anthony Barker, and Eva Y. Andrei, Nature Nanotechnol. 3, 491 (2008)

[122] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, Phys. Rev. Lett. 101, 096802 (2008)

[123] Eduardo V. Castro, H. Ochoa, M. I. Katsnelson, R.V. Gorbachev, D. C. Elias, K. S. Novoselov, A. K. Geim, and F. Guinea, Phys Rev. Lett. 105, 266601 (2010).

[124] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, J. Hone, Nature Nanotechnol. 5, 722 (2010)

[125] Alexander S. Mayorov, Roman V. Gorbachev, Sergey V. Morozov, Liam Britnell, Rashid Jalil, Leonid A. Ponomarenko, Peter Blake, Kostya S. Novoselov, Kenji Watanabe,| Takashi Taniguchi, and A. K. Geim, Nano Lett. dx.doi.org/10.1021/nl200758b

[126] Xiaosong Wu, Yike Hu, Ming Ruan, Nerasoa K Madiomanana, John Hankinson, Mike Sprinkle, Claire Berger, and Walt A. de Heer, Appl. Phys. Lett. 95, 223108 (2009)

[127] M. Orlita, C. Faugeras, P. Plochocka, P. Neugebauer, G. Martinez, D. K. Maude, A.-L. Barra, M. Sprinkle, C. Berger, W. A. de Heer, and M. Potemski, Phys. Rev. Lett. 101, 267601 (2008)

[128] X. Li, C. W. Magnuson, A. Venugopal, J. An, J. W. Suk, B. Han, M. Borysiak, W. Cai, A. Velamakanni, Y. Zhu, L. Fu, E. M. Vogel, E. Voelkl, L. Colombo, and Rodney S. Ruoff, *Nano Lett.* **10**, 4328 (2010).

[129] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz: "A Graphene Field Effect Device", IEEE Electron Device Lett. 28, 282 (2007).

[130] J. R. Williams, L. DiCarlo, C. M. Marcus: "Quantum Hall Effect in a Gate-Controlled p-n Junction of Graphene", Sicence 317, 638 (2007).

[131] D. B. Farmer, H.-Y. Chiu, Y.-M. Lin, K. A. Jenkins, F. Xia, and Ph. Avouris: "Utilization of a Buffered Dielectric to Achieve High Field-Effect Carrier Mobility in Graphene Transistors", Nano Lett. 9, 4474 (2009).

[132] Y. Q. Wu, P. D. Ye, M. A. Capano, Y. Xuan, Y. Sui, M. Qi, J. A. Cooper, T. Shen, D. Pandey, G. Prakash, and R. Reifenberger: "Top-gated Graphene Field-effect-transistors Formed by Decomposition of SiC", Appl. Phys. Lett., 92, 092102 (2008).

[133] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, S. K. Banerjee: "Realization of a High Mobility Dual-Gated Graphene Field-Effect Transistor with Al2O3 Dielectric", Appl. Phys. Lett. 94, 062107 (2009).

[134] Lei Liao, Jingwei Bai, Yongquan Qu, Yung-chen Lin, Yujing Li, Yu Huangb, and Xiangfeng Duan, PNAS, 107, 6711 (2010)

[135] Y. Q. Wu, P. D. Ye, M. A. Capano, Y. Xuan, Y. Sui, M. Qi, J. A. Cooper, T. Shen, D. Pandey, G. Prakash, and R. Reifenberger, Appl. Phys. Lett. 92, 092102 (2008)

[136] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, *Science*, 324, 1312 (2009).

[137] Gengchiau Liang, Neophytos Neophytou, Dmitri E. Nikonov and Mark S. Lundstrom, "Performance Projections for Ballistic Graphene Nanoribbon Field-Effect Transistors," IEEE Transactions on Electron Devices, Vol. 54 (4), p. 677 (April 2007).

[138] Grassi, R., Gnudi, A., Gnani, E., Reggiani, S., Baccarani, G., "Graphene nanoribbons FETs for high-performance logic applications: Perspectives and challenges," Proceedings of the 2008 ICSICT Oct 20-23, 2008, pp. 365-368

[139] M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim: "Energy Band-Gap Engineering of Graphene Nanoribbons" Phys. Rev. Lett. 98, 206805 (2007)

[140] X. Li, X. Wang, Li Zhang, S. Lee, and H. Dai: "Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors", Science 319, 1229 (2008).

[141] Xuesong Li, Carl W. Magnuson, Archana Venugopal, Rudolf M. Tromp, James B. Hannon, Eric M. Vogel, Luigi Colombo, and Rodney S. Ruoff, J. Am. Chem. Soc., 133, 2816 (2011).

[142] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, Nature Nanotech., 5, 574 (2010).

[143] Shintaro Sato, Katsunori Yagi, Daiyu Kondo, Kenjiro Hayashia, Ayaka Yamada, Naoki Harada, Naoki Yokoyama, ECS Trans. 35(3), 219 (2011)

[144] M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim: "Energy Band-Gap Engineering of Graphene Nanoribbons" Phys. Rev. Lett. 98, 206805 (2007)

[145] X. Li, X. Wang, Li Zhang, S. Lee, and H. Dai: "Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors", Science 319, 1229 (2008).

[146] L. Jiao, L. Zhang, X. Wang, G. Diankov, and H. Dai: "Narrow Graphene Nanoribbons from Carbon Nanotubes", Nature 458, 877 (2009).

[147] D. V. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, B. K. Price, and J. M. Tour: "Longitudinal Unzipping of Carbon Nanotubes to Form Graphene Nanoribbons", Nature 458, 872 (2009).

[148] J. Campos-Delgado, J. M. Romo-Herrera, X. Jia, D. A. Cullen, H. Muramatsu, Y. A. Kim, T. Hayashi, Z. Ren, D. J. Smith, Y. Okuno, T. Ohba, H. Kanoh, K. Kaneko, M. Endo, H. Terrones, M. S. Dresselhaus, and M. Terrones: "Bulk Production of a New Form of sp2 Carbon: "Crystalline Graphene Nanoribbons", Nano Lett. 8, 2773 (2008).

[149] M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim: "Energy Band-Gap Engineering of Graphene Nanoribbons" Phys. Rev. Lett. 98, 206805 (2007)

[150] X. Li, X. Wang, Li Zhang, S. Lee, and H. Dai: "Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors", Science 319, 1229 (2008).

[151] L. Jiao, L. Zhang, X. Wang, G. Diankov, and H. Dai: "Narrow Graphene Nanoribbons from Carbon Nanotubes", Nature 458, 877 (2009).

[152] D. V. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, B. K. Price, and J. M. Tour: "Longitudinal Unzipping of Carbon Nanotubes to Form Graphene Nanoribbons", Nature 458, 872 (2009).

[153] J. Campos-Delgado, J. M. Romo-Herrera, X. Jia, D. A. Cullen, H. Muramatsu, Y. A. Kim, T. Hayashi, Z. Ren, D. J. Smith, Y. Okuno, T. Ohba, H. Kanoh, K. Kaneko, M. Endo, H. Terrones, M. S. Dresselhaus, and M. Terrones: "Bulk Production of a New Form of sp2 Carbon: "Crystalline Graphene Nanoribbons", Nano Lett. 8, 2773 (2008).

[154] Jinming Cai, Pascal Ruffieux, Rached Jaafar, Marco Bieri, Thomas Braun, Stephan Blankenburg, Matthias Muoth, Ari P. Seitsonen, Moussa Saleh, Xinliang Feng, Klaus Mu¨llen & Roman Fasel, Nature 466, 470 (2010).

[155] X. Li, X. Wang, Li Zhang, S. Lee, and H. Dai: "Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors", Science 319, 1229 (2008)

[156] M.Bresciani, A.Paussa, P.Palestri, D.Esseni, L.Selmi, IEEE IEDM Technical Digest 2010, p.724 (2010).

[157] Melinda Y. Han, Juliana C. Brant, and Philip Kim, Phys. Rev Lett. 104, 056801 (2010)

[158] Patrick Gallagher, Kathryn Todd, and David Goldhaber-Gordon, Phys. Rev. B **81**, 115409 (2010)

[159] Xinglan Liu, Jeroen B. Oostinga, Alberto F. Morpurgo, and Lieven M. K. Vandersypen, Phys. Rev. B 80, 121407(R) (2009)

[160] Yanqing Wu, Yu-ming Lin, Ageeth A. Bol, Keith A. Jenkins, Fengnian Xia, Damon B. Farmer, Yu Zhu, and Phaedon Avouris, Nature 472, 74 (2011)

[161] Y.Q. Wu, Y.-M. Lin, K.A. Jenkins, J.A. Ott, C. Dimitrakopoulos, D.B. Farmer, F. Xia, A. Grill, D.A. Antoniadis, and Ph. Avouris, IEEE IEDM Technical Digest 2010, p.226 (2010).

[162] Lei Liao, Yung-Chen Lin, Mingqiang Bao, Rui Cheng, Jingwei Bai, Yuan Liu, Yongquan Qu, Kang L. Wang, Yu Huang, and Xiangfeng Duan, Nature 467, 305 (2010)

[163] Lei Liao, Yung-Chen Lin, Mingqiang Bao, Rui Cheng, Jingwei Bai, Yuan Liu, Yongquan Qu, Kang L. Wang, Yu Huang, and Xiangfeng Duan, Nature 467, 305 (2010)

[164] Y.Q. Wu, Y.-M. Lin, K.A. Jenkins, J.A. Ott, C. Dimitrakopoulos, D.B. Farmer, F. Xia, A. Grill, D.A. Antoniadis, and Ph. Avouris, IEEE IEDM Technical Digest 2010, p.226 (2010).

[165] Yanqing Wu, Yu-ming Lin, Ageeth A. Bol, Keith A. Jenkins, Fengnian Xia, Damon B. Farmer, Yu Zhu, and Phaedon Avouris, Nature 472, 74 (2011)

[166] Ma, D. D., Lee, C. S., Au, F. C., Tong, S. Y., & Lee, S. T. (2003, Mar. 21). Small-diameter silicon nanowire surfaces. *Science, 299*, 1874-1877.

[167] Yan, H., & Yang, P. (2004). Semiconductor nanowires: functional building blocks for nanotechnology. In P. Yang (Ed.), *The Chemistry of Nanostructured Materials.* River Edge, NJ: World Scientific.

[168] Beckman, R., Johnston-Halperin, E., Luo, Y., Green, J. E., & Hearh, J. R. (2005, Oct. 21). Bridging dimensions: demultiplexing ultrahigh-density nanowire circuits. *Science, 310*(5747), 465-468.

[169] Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J., & Lieber, C. M. (2001, Apr. 9). Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett., 78*(15), 2214-2216.

[170] Wu, Y., & Yang, P. (2000). Germanium nanowire growth via simple vapor transport. *Chem. Mater., 12*, 605-607.

[171] Xiang, J., Lu, W., Hu, Y., Wu, Y., Yan, H., & Lieber, C. M. (2006). Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature, 441*, 489-493.

[172] Lu, W., & Lieber, C. M. (2007, Nov.). Nanoelectronics from the bottom up. *Nature Materials, 6*, 841-850.

[173] Yang, B., Buddharaju, K. D., Teo, S. H., Singh, N., Lo, G. Q., & Kwong, D. L. (2008, Jul.). Vertical silicon-nanowire formation and gate-all-around MOSFET. *IEEE Elect. Dev. Lett., 29*(7), 791-794.

[174] Wernersson, L.-E., Thelander, C., Lind, E., & Samuelson, L. (2010, Dec. 12). III-V nanowires--extending a narrowing road. *Proc. IEEE, 98*(12), 2047-2060.

[175] Autran, J.-L., & Munteanu, D. (2007, Apr.). Beyond silicon bulk MOS transistor: new materials, emerging structures and ultimate devices. *Revue de l'Electricite et de l'Electronique, 4*, 25-37.

[176] Ng, H. T., Han, J., Yamada, T., Nguyen, P., Chen, Y. P., & Meyyappan, M. (2004). Single crystal nanowire vertical surround-gate field-effect transistor. *Nano Lett., 4*(7), 1247-1252.

[177] Yeo, K. H., Suk, S. D., Li, M., Yeoh, Y., Cho, K. H., Hong, K., et al. (2006). Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires. *Proc. Int'l Electron Devices Meeting.*

[178] Sheriff, B. A., Wang, D., Heath, J. R., & Kurtin, J. N. (2008). Complementary symmetry nanowire logic circuits: experimental demonstrations and in silico optimizations. *ACS Nano, 2*(9), 1789-1798.

[179] Friedman, R. S., McAlpine, M. C., Ricketts, D. S., Ham, D., & Lieber, C. M. (2005, Apr.). High-speed integrated nanowire circuits. *Nature, 434*(7037), 1085.

[180] Yan, H., Choe, H. S., Nam, S., Hu, Y., Das, S., Klemic, J. F., et al. (2011, Feb. 10). Programmable nanowire circuits for nanoprocessors. *Nature, 470*, 240-244.

[181] Lu, W., Xie, P., & Lieber, C. M. (2008, Nov.). Nanowire transistor performance limits and applications. *IEEE Trans. Elect. Dev., 55*(11), 2859-2876.

[182] D.-H. Kim and J. A. del Alamo, "30nm E-mode InAs PHEMTs for THz and Future Logic Applications," in *IEDM Tech. Dig.*, p719, 2008.

[183] T. Tanaka, K. Tomioka, S. Hara, J. Motohisa, E. Sano, and T. Fukui, "Vertical Surrounding Gate Transistors Using Single InAs Nanowires Grown on Si Substrates," Appl. Phys. Express, vol. 30, 025003, 2010

[184] Q.-T. Do, K. Blekker, I. Reglin, W. Prost, and E. J. Tegude, "High Transconductance MISFET With a Single InAs Nanowire Cannel," IEEE Electron Dev. Lett., vol. 28, no. 8, p682, 2007.

[185] M. Egard, S. Johannson, A.-C. Johansson, K.-M. Persson, A. W. Dey, B. M. Borg, C. Thelander, L.-E. Wernersson, and E. Lind, "Vertical InAs Nanowire Wrap Gate Transistors with ft > 7 GHz and fmax > 20GHz," Nano Lett., vol. 10, p809, 2010.

[186] A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ramirez, P. Schiffer, T. N. Jackson, S. E. Mohney, J. B. Boos, B. R. Bennett, I. Geppert, M. Eizenberg, and S. Datta, "Advanced Composite High-k Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors," in *IEDM Tech. Dig.*, p134, 2010.

[187] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed Very Low Power Digital Logic Applications," in *IEDM Tech. Dig*, 2005.

[188] T. Ashley, M. T. Emeny, D. G. Hayes, K. P. Hilton, R. Jefferies, J. O. Maclean, S. J. Smith, A. W-H. Tang, D. J. Wallis, and P. J. Webber, "High-Performance InSb Based Quantum Well Field Effect Transistors for Low-Power Dissipation Applications," in *IEDM Tech. Dig.*, p849, 2009.

[189] J. B. Boos, B. R. Bennett, N. A. Papanicolaou, M. G. Ancona, J. G. Champlain, Y.-C. Chou, M. D. Lange, J. M. Yang, R. Bass, D. Park, and B. V Shanabrook, "Sb-based n- and p-channel Heterostructure FETs for High-Speed, Low-Power Applications," IEICE Trans. Electron., vol. E91-C, p1050, 2008.

[190] J. B. Boos, B. R. Bennett, N. A. Papanicolaou, M. G. Ancona, J. G. Champlain, Y.-C. Chou, M. D. Lange, J. M. Yang, R. Bass, D. Park, and B. V Shanabrook, "Sb-based n- and p-channel Heterostructure FETs for High-Speed, Low-Power Applications," IEICE Trans. Electron., vol. E91-C, p1050, 2008

[191] A. Nainani, T. Irisawa, Z. Yuan, Y. Sun, T. Krishnamohan, M. Reason, B. R. Bennett, J. B. Boos, M. G Ancona, Y. Nishi, and K. C. Saraswat, "Development of high-k dielectric for Antimonides and a sub 350oC III-V pMOSFET outperforming Germanium," in *IEDM Tech. Dig.*, p138, 2010.

[192] L. Xia, J. B. Boos, B. R. Bennett, M. G. Ancona, and J. A. del Alamo, "Hole mobility enhancement in InGaSb quantum-well field-effect transistors," *Appl. Phys. Lett.*, vol. 98, 053505, 2011.

[193] A. Nainai, S. Raghunathan, D. Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan, K. Saraswat, "Engineering of Strained III-V Heterostructures for High Hole Mobility," in *IEDM Tech Dig.*, p857, 2009.

[194] A. Nainani, J. Yum, J. Barnett, R. Hill, N. Goel, J. Huang, P. Majhi, R. Jammy, and K. C. Saraswat, "Study of piezoresistance under uniaxial stress for technologically relevant III-V semiconductors using wafer bending experiments," *Appl. Phys. Lett.*, vol. 96, 242110, 2010.

[195] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Widing, and R. Chau, "High-Performance 40nm

Gate Length InSb P-Channel Compressively Strained Quantum Well Field Effect Transistors for Low-Power (Vcc=0.5V) Logic Applications," in *IEDM Tech. Dig.*, p727, 2008

[196] L. Xia, J. B. Boos, B. R. Bennett, M. G. Ancona, and J. A. del Alamo, "Hole mobility enhancement in InGaSb quantum-well field-effect transistors," *Appl. Phys. Lett.*, vol. 98, 053505, 2011.

[197] A. Nainani, J. Yum, J. Barnett, R. Hill, N. Goel, J. Huang, P. Majhi, R. Jammy, and K. C. Saraswat, "Study of piezoresistance under uniaxial stress for technologically relevant III-V semiconductors using wafer bending experiments," *Appl. Phys. Lett.*, vol. 96, 242110, 2010

[198] M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Widing, and R. Chau, "High-Performance 40nm Gate Length InSb P-Channel Compressively Strained Quantum Well Field Effect Transistors for Low-Power (Vcc=0.5V) Logic Applications," in *IEDM Tech. Dig.*, p727, 2008

[199] P. Tsipas and A. Dimoulas, "Modeling of negative chaged states at the Ge surface and interfaces," *Appl. Phys. Lett.*, vol. 94, 012114, 2009.

[200] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Appl. Phys. Lett.*, 93, 032104, 2008.

[201] C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "Ge/GeO2 interface control with high-pressure oxidation for improving electrical characteristics," *Appl. Phys. Express*, vol. 2, 071404, 2009.

[202] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Panetta, H.-S. P. Wong, and K. C. Saraswat, "High-Moblity Ge N-MOSFETs and Mobility Degradation Mechanisms", IEEE Trans. Electron Devices, vol. 59, no. 1, pp. 59–66, 2011.

[203] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Panetta, H.-S. P. Wong, and K. C. Saraswat, "High-Moblity Ge N-MOSFETs and Mobility Degradation Mechanisms", IEEE Trans. Electron Devices, vol. 59, no. 1, pp. 59–66, 2011.

[204] Yen-Chun Fu, William Hsu, Yen-Ting Chen, Huang-Siang Lan, Cheng-Han Lee, Hung-Chih Chang, Hou-Yun Lee, Guang-Li Luo, Chao-Hsin Chien, C. W. Liu, Chenming Hu, and Fu-Liang Yang, "High mobility high on/off ratio C-V dispersion-free Ge n-MOSFETs and their strain response", in *IEDM Tech. Dig.*, 2010, p. 432.

[205] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High-Performance GeO2/Ge nMOSFETs With Source/Drain Junctions Formed by Gas-Phase Doping," *IEEE Electron Device Lett*, vol. 31, no. 10, p. 1092, 2010.

[206] C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, "Ge MOSFETs Performance: Impact of Ge Interface Passivation", in *IEDM Tech. Dig.*, 2010, p. 416.

[207] M. Jamil, J. Oh, M. Ramon, S. Kaur, P. Majhi, E. Tutuc, and S. K. Banerjee, "High-Mobility TaN/Al2O3/Ge(111) n-MOSFETs With RTO-Grown Passivation Layer", *IEEE Electron Device Lett*, vol. 31, no. 11, p. 1208, 2010.

[208] C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, "Ge MOSFETs Performance: Impact of Ge Interface Passivation", in *IEDM Tech. Dig.*, 2010, p. 416

[209] Yen-Chun Fu, William Hsu, Yen-Ting Chen, Huang-Siang Lan, Cheng-Han Lee, Hung-Chih Chang, Hou-Yun Lee, Guang-Li Luo, Chao-Hsin Chien, C. W. Liu, Chenming Hu, and Fu-Liang Yang, "High mobility high on/off ratio C-V dispersion-free Ge n-MOSFETs and their strain response", in *IEDM Tech. Dig.*, 2010, p. 432

[210] W. B. Chen, B. S. Shie, and Albert Chin, "Higher Gate Capacitance Ge n-MOSFETs Using Laser Annealing", *IEEE Electron Device Lett*, vol. 32, no. 4, 2011 p. 449.

[211] M. Jamil, J. Oh, M. Ramon, S. Kaur, P. Majhi, E. Tutuc, and S. K. Banerjee, "High-Mobility TaN/Al2O3/Ge(111) n-MOSFETs With RTO-Grown Passivation Layer", *IEEE Electron Device Lett*, vol. 31, no. 11, p. 1208, 2010.

[212] M. Kobayashi, T. Irisawa, B. M. Kope, Y. Sun, K. Saraswat, H.-S. P. Wong, P. Panetta, Y. Nishi, "High quality GeO2/Ge Interface Formed by SPA Radical Oxidation and Uniaxial Stress Engineering for High Performance Ge NMOSFETs," in *Symp. VLSI Tech.*, p76, 2009.

[213] J. Kim, S. W. Bedell, and D. K. Sadana, "Improved germanium n+/p junction diodes formed by co-implantation of antimony and phosphorus", *Appl. Phys. Lett.*, vol. 98, 082112, 2011

[214] G. Thareja, J. Liang, S. Chopra, B. Adams, N. Patil, S.-L.Cheng , A.Nainani, E. Tasyurek, Y.Kim, S. Moffatt, R. Brennan, J. McVittie, T. Kamins, K. Saraswat and Y. Nishi, "High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond $1x10^{20}$ cm^{-3}, in *IEDM Tech. Dig.*, 2010, pp. 245

[215] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High-Performance GeO2/Ge nMOSFETs With Source/Drain Junctions Formed by Gas-Phase Doping," *IEEE Electron Device Lett*, vol. 31, no. 10, p. 1092, 2010

[216] M. Takenaka, K. Mori, M. Sugiyama, Y. Nakano, and S. Takagi, "Gas Phase Doping of Arsenic into (100), (110), and (111) Germanium Substrates Using a Metal-Organic Source," *Jpn. J. Appl. Phys.*, vol. 50, 010105, 2011.

[217] G. Thareja, J. Liang, S. Chopra, B. Adams, N. Patil, S.-L.Cheng , A.Nainani, E. Tasyurek, Y.Kim, S. Moffatt, R. Brennan, J. McVittie, T. Kamins, K. Saraswat and Y. Nishi, "High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond $1x10^{20}$ cm^{-3}, in *IEDM Tech. Dig.*, 2010, pp. 245.

[218] T. Maeda, Y. Morita and S. Takagi, "Impact of Ge nitride interfacial layers on performance of Metal Gate/High-k Ge-nMISFETs", in *Symp. VLSI Tech.*, 2010, p. 213.

[219] T. Nishimura, C. H. Lee, S. K. Wang, T. Tabata, K. Kita, K. Nagashio, and A. Toriumi, "Electron Mobility in High-k Ge-MISFETs Goes Up to Higher," in *Symp. VLSI Tech.*, 2010, p209

[220] W. B. Chen, C. H. Wu, B. S. Shie, and A. Chin, "Gate-First TaN/La2O3/SiO2/Ge n-MOSFETs Using Laser Annealing," *IEEE Electron Device Lett.*, vol. 31, no. 11, p1184, 2010.

[221] J. Quinn, G. Kawamoto, B. McCombe, "Subband Spectroscopy by Surface Channel Tunneling," Surface Sci, vol. 73, 1978, pp. 190-196

[222] T. Baba, "Proposal for Surface Tunnel Transistors," Jpn. J. Appl. Phys., vol. 31, 1992, pp. L455-L457

[223] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," IEEE Electron Device Lett., vol. 27, no. 4, Apr. 2006, pp. 297–300.

[224] O.M. Nayfeh, C.N. Chleirigh, J. Hennessy, L. Gomez, J.L. Hoyt, D.A. Antoniadis, IEEE Electron Device Letters, Volume 29, Issue 9, Sept. 2008, pp. 1074 – 1077

[225] S.O. Koswatta, M.S. Lundstrom, D.E. Nikonov, "Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs," IEEE Transactions on Electron Devices, Volume 56, Issue 3, March 2009, pp. 456 – 465

[226] K. Boucart, A.M. Ionescu, "Double-Gate Tunnel FET With High-κ Gate Dielectric, " IEEE Transactions on Electron Devices, Volume 54, Issue 7, July 2007, pp. 1725 – 1733

[227] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp+ layer," Jpn. J. Appl. Phys., vol. 43, no. 7A, Jul. 2004, pp. 4073–4078

[228] S.O. Koswatta, M.S. Lundstrom, D.E. Nikonov, "Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs," IEEE Transactions on Electron Devices, Volume 56, Issue 3, March 2009, pp. 456 – 465

[229] G. Fiori, G. Iannaccone, "On the possibility of tunable-gap bilayer graphene FET", IEEE Electron Device Letters, Vol. 30, 2009, pp. 261-264

[230] K. Boucart, W. Riess, A.M. Ionescu, "Lateral Strain Profile as Key Technology Booster for All-Silicon Tunnel FETs," IEEE Electron Device Letters, Vol. 30 , Iss. 6, 2009, pp. 656 – 658

[231] J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," Phys. Rev. Lett., vol. 93, no. 19, 2004, pp. 196805-1-4

[232] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope," in IEDM Tech. Dig., Dec. 15–17, 2008, pp. 947–949

[233] F. Mayer, C. Le Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance," in IEDM Tech. Dig., 2008, pp. 163-166

[234] K. Jeon, W. Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J. King Liu, and C. Hu, "Si tunnel transistors with a novel silicided source and 46mV/dec swing," 2010 Symposium on VLSI Technology (VLSIT), 2010 , pp. 121 – 122

[235] W.-Y. Loh, K. Jeon, C. Y. Kang, J. Oh, P. Patel, C. Smith, J. Barnett, C. Park, T.-J. King Liu, H.-H. Tseng, P. Majhi, R. Jammy, and C. Hu, "Sub-60nm Si tunnel field effect transistors with Ion >100 μA/μm," 2010 Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2010, pp. 162 – 165

[236] W.-Y. Loh, K. Jeon, C. Y. Kang, J. Oh, P. Patel, C. Smith, J. Barnett, C. Park, T.-J. King Liu, H.-H. Tseng, P. Majhi, R. Jammy, and C. Hu, "Sub-60nm Si tunnel field effect transistors with Ion >100 μA/μm," 2010 Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2010, pp. 162 – 165

[237] D. Leonelli, A. Vandooren, R. Rooyackers, S. De Gendt, M.M. Heyns, G. Groeseneken, "Optimization of tunnel FETs: Impact of gate oxide thickness, implantation and annealing conditions," 2010 Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2010, pp. 170 – 173

[238]A.C. Seabaugh, Q. Zhang, Low-Voltage Tunnel Transistors for Beyond CMOS Logic, Proceedings of the IEEE, vol. 98, iss. 12, 2010, pp. 2095 – 2110b

[239] ITRS 2009 edition.

[240] S. Sugahara, and J. Nitta, "Spin-Transistor Electronics:An Overview and Outlook", Proc. IEEE, vol. 98, pp. 2124-2154, 2010.

[241]T. Marukame, T. Inokuchi, M. Ishikawa, H. Sugiyama, Y. Saito, "Read/write operation of spin-based MOSFET using highly spin-polarized ferromagnet/MgO tunnel barrier for reconfigurable logic devices", 2009 IEEE International Electron Devices Meeting, pp. 9.2.1-9.2.4, 2009.

[242] T. Inokuchi, T. Marukame, T. Tanamoto, H. Sugiyama, M. Ishikawa, Y. Saito, "Reconfigurable characteristics of spintronics-based MOSFETs for nonvolatile integrated circuits", 2010 Symp. on VLSI Technology, pp. 119 – 120, 2010.

243 S.P. Dash, S. Sharma, R.S. Patel, M.P. de Jong, R. Jansen, "Electrical creation of spin polarization in silicon at room temperature", Nature, vol. 462, pp. 491-494, 2009.

[244] C.H. Li, O.M.J. van't Erve, B.T. Jonker, "Electrical injection and detection of spin accumulation in silicon at 500 K with magnetic metal/silicon dioxide contacts", Nature Communications, vol. **2**, p. 245, 2011.

245 W. Wang, H. Sukegawa, and K. Inomata, "Temperature dependence of tunneling magnetoresistance in epitaxial magnetic tunnel junctions using a Co2FeAl Heusler alloy electrode", Phys. Rev. B, vol. 82, pp. 092402/1-4, 2010.

246 S. Tsunegi, Y. Sakuraba, M. Oogane, K. Takanashi, Y. Ando, "Large tunnel magnetoresistance in magnetic tunnel junctions using a Co2MnSi Heusler alloy electrode and a MgO barrier", Appl. Phys.Lett., vol 93, pp. 112506/1-3, 2008.

247 H. Sukegawa, S. Kasai, T. Furubayashi, S. Mitani, K. Inomata, "Spin-transfer switching in an epitaxial spin-valve nanopillar with a full-Heusler Co2FeAl0.5Si0.5 alloy", Apple. Phys. Lett., vol. 96, pp. 042508/1-3, 2010

248 Y. Takamura, R. Nakane, S. Sugahara, 'Quantitative analysis of atomic disorders in full-Heusler Co2FSi alloy thin films using x-ray diffraction with Co Kα and Cu Kα sources, J. Appl. Phys., vol. 107, pp. 09B111/1-3, 2010.

249 G. Kioseoglou, A. T. Hanbicki, R. Goswami, O. M. J. van 't Erve, C. H. Li, G. Spanos, P. E. Thompson,and B. T. Jonker, "Electrical spin injection into Si: A comparison between Fe/Si Schottky and Fe/Al2O3 tunnel contacts", Appl. Phys. Lett., vol. 94, pp. 122106/1-3, 2009.

250 A. Kohn, A. Kovács, T. Uhrmann, T. Dimopoulos, and H. Brückl, "Structural and electrical characterization of SiO2 /MgO(001) barriers on Si for a magnetic transistor", Appl. Phys. Lett., vol. 95, pp. 042506/1-3, 2009.

251 A.M. Roy, D.E. Nikonov and K.C. Saraswat, "Conductivity mismatch and voltage dependence of magnetoresistance in a semiconductor spin injection device", J. Appl. Phys., vol. 107, pp. 064504/1-9, 2010.

252 D. Lee, S. Raghunathan, R.J. Wilson, D.E. Nikonov, K. Saraswat, and S.X. Wang, "The influence of Fermi level pinning/depinning on the Schottky barrier height and contact resistance in Ge/CoFeB and Ge/MgO/CoFeB structures", Appl. Phys. Lett., vol. 96, pp. 052514/1-3, 2010.

253 S. Sugahara, and J. Nitta, "Spin-Transistor Electronics:An Overview and Outlook", Proc. IEEE, vol. 98, pp. 2124-2154, 2010.

254 Y. Shuto, R. Nakane, W. Wang, H. Sukegawa, S. Yamamoto, M. Tanaka, K. Inomata, and S. Sugahara, "A New Spin-Functional Metal–Oxide–Semiconductor Field-Effect Transistor Based on Magnetic Tunnel Junction Technology: Pseudo-Spin-MOSFET", Appl. Phys. Express, vol. 3, pp. 013003/1-3, 2010.
255 S. Sugahara, and J. Nitta, "Spin-Transistor Electronics:An Overview and Outlook", Proc. IEEE, vol. 98, pp. 2124-2154, 2010.
256 S. Shuto, S. Yamamoto, and S. Sugahara, "Nonvolatile Static Random Access memory based on spin-transistor architecture", J. Appl. Phys., vol. 105, pp. 07C933/1-3, 2009.
257 S. Yamamoto, and S. Sughara, "Nonvolatile Delay Flip-Flop Based on Spin-Transistor Architecture and Its Power-Gating Applications", Jpn. J. Appl. Phys., vol. 49, pp. 090204/1-3, 2010.
258S. Sugahara, Y. Shuto, and S. Yamamoto, "Nonvolatile Logic Systems Based on CMOS/Spintronics Hybrid Technology: An Overview", Magnetics Japan, Vol. 6, pp. 5-15, 2011.
259ITRS 2009 edition.
260 S. Sugahara, and J. Nitta, "Spin-Transistor Electronics:An Overview and Outlook", Proc. IEEE, vol. 98, pp. 2124-2154, 2010.
261H. C. Koo, J. H. Kwon, J. Eom, J. Chang, S. H. Han, and M. Johnson, "Control of spin precession in a spin-injected field effect transistor", Science, vol. 325, pp. 1515–1518, Sep. 2009.
262] S. Bandyopadhyay, Comment on "Control of Spin Precession in a Spin-Injected Field Effect Transistor", http://arxiv.org/abs/0911.0210.
263A. N. M. Zainuddin, S. Hong, L. Siddiqui, and S. Datta, "Voltage Controlled Spin Precession", http://arxiv.org/abs/1001.1523.
264S. Bandyopadhyay, "Analysis of the Two Dimensional Datta-Das Spin Field Effect Transistor", http://arxiv.org/abs/1001.2705.

[265] K. Gopalakrishnan, P.B. Griffin and J. Plummer, "I-MOS: A Novel Semiconductor Device with a Subthreshold Slope lower than kT/q," IEEE International Electron Devices Meeting, December 2002, pp. 289-292

[266] K. Gopalakrishnan, P. B. Griffin and J. D. Plummer, "Impact Ionization MOS (I-MOS) - Part I: Device and Circuit Simulations," IEEE Transactions on Electron Devices, Vol. 52, Iss. 1, January 2005, pp. 69–76

[267] K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, "Impact Ionization MOS (I-MOS) - Part II: Experimental Results," IEEE Transactions on Electron Devices, 52 (1) pp. 77–84, January 200

[268] W.Y. Choi, J.Y. Song, J.D. Lee, Y.J. Park and B.J. Park, "70-nm Impact-Ionization Metal-Oxide-Semiconductor (I-MOS) Devices Integrated with Tunneling Field-Effect Transistors (TFETs)," IEEE International Electron Devices Meeting, p. 975-978, December 2005

[269] C. Shen, J.-Q. Lin, E.-H. Toh, K.-F. Chang, P. Bai, C.-H. Heng, G. S. Samudra, and Y.-C. Yeo, "On the performance limit of impact ionization transistors," in IEDM Tech. Dig., 2007, pp. 117–120

[270] C. Hyunbo, C. Onal, P.B. Griffin, J.D. Plummer, "Statistical Retardation Delay of I-MOS and Its Measurement Using TDR IEEE Electron Device Letters," Vol. 32, Iss. 2, 2011, pp. 206 – 208

[271]K. Gopalakrishnan, P.B. Griffin and J. Plummer, "I-MOS: A Novel Semiconductor Device with a Subthreshold Slope lower than kT/q," IEEE International Electron Devices Meeting, December 2002, pp. 289-292,.

[272]K. Gopalakrishnan, P. B. Griffin and J. D. Plummer, "Impact Ionization MOS (I-MOS) - Part I: Device and Circuit Simulations," IEEE Transactions on Electron Devices, Vol. 52, Iss. 1, January 2005, pp. 69–76

[273]K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, "Impact Ionization MOS (I-MOS) - Part II: Experimental Results," IEEE Transactions on Electron Devices, 52 (1) pp. 77–84, January 2005

[274]W.Y. Choi, J.Y. Song, J.D. Lee, Y.J. Park and B.J. Park, "70-nm Impact-Ionization Metal-Oxide-Semiconductor (I-MOS) Devices Integrated with Tunneling Field-Effect Transistors (TFETs)," IEEE International Electron Devices Meeting, p. 975-978, December 2005

[275]C. Charbuillet, S. Monfray, S.; Dubois, E.; Bouillon, P.; Judong, F.; Skotnicki, T.; "High Current Drive in Ultra-Short Impact Ionization MOS (I-MOS) Devices," International Electron Device Meeting, 11-13 Dec. 2006

[276]E.-H. Toh; G. H. Wang, L. Chan; G.-Q. Lo; G. Samudra, Y.-C. Yeo; I-MOS Transistor With an Elevated Silicon–Germanium Impact-Ionization Region for Bandgap Engineering, IEEE Electron Device Letters, Vol. 27 , Iss. 12, 2006 , pp. 975 - 977

[277]F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier C. Tabone and S. Deleonibus, "Co-integration of 2mV/dec Subthreshold Slope Impact Ionization MOS (I-MOS) with CMOS," ESSDERC, September 2006

[278]F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier C. Tabone and S. Deleonibus, "Co-integration of 2mV/dec Subthreshold Slope Impact Ionization MOS (I-MOS) with CMOS," ESSDERC, September 2006.

[279]E.-H. Toh; G. H. Wang, L. Chan; G.-Q. Lo; G. Samudra, Y.-C. Yeo; I-MOS Transistor With an Elevated Silicon–Germanium Impact-Ionization Region for Bandgap Engineering, IEEE Electron Device Letters, Vol. 27 , Iss. 12, 2006 , pp. 975 - 977

[280]F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier and S.Deleonibus, "Static and Dynamic TCAD Analysis of IMOS Performance: From the Single Device to the Circuit," IEEE Transaction On Electron Devices, Vol.53, Issue 8, p. 1852-1857, August 2006

[281] A.G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," Physical Review, Vol. 109, N°5, March 1958.

[282]C. Charbuillet, S. Monfray, S.; Dubois, E.; Bouillon, P.; Judong, F.; Skotnicki, T.; "High Current Drive in Ultra-Short Impact Ionization MOS (I-MOS) Devices," International Electron Device Meeting, 11-13 Dec. 2006.

[283] A. Savio, S. Monfray, C. Charbuillet, T. Skotnicki, "On the Limitations of Silicon for I-MOS Integration, IEEE Transactions on Electron Devices, Vol. 56 , Issue: 5, 2009 , pp. 1110 – 1117

[284]A.G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," Physical Review, Vol. 109, N°5, March 1958

[285]E.-H. Toh, G. H. Wang, G.-Q. Lo, N. Balasubramanian, C.-H. Tung, F. Benistant, and L. Chan, "A novel CMOS compatible L-shaped impact ionization MOS (LI-MOS) transistor," in IEDM Tech. Dig., 2005, pp. 951–954

[286]E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, "Reduction of impact-ionization threshold energies for performance enhancement of complementary impact-ionization metal–oxide–semiconductor transistors," Appl. Phys. Lett., vol. 91, no. 15, p. 153 501, Oct. 2007

[287]F. Mayer, C. Le Royer, D. Blachier, L. Clavelier, and S. Deleonibus, "Avalanche Breakdown Due to 3-D Effects in the Impact-Ionization MOS (I-MOS) on SOI: Reliability Issues," IEEE Transaction on Electron Devices, Vol. 55, no. 6, June 2008, pp. 1373-1378

[288]C. Hyunbo, C. Onal, P.B. Griffin, J.D. Plummer, "Statistical Retardation Delay of I-MOS and Its Measurement Using TDR IEEE Electron Device Letters," Vol. 32, Iss. 2, 2011, pp. 206 – 208.

[289] S. Salahuddin and S. Datta, `Use of negative capacitance to provide a subthreshold slope lower than 60 mV/decade,` Nanoletters, vol. 8, No. 2, 2008.

[290] S. Salahuddin and S. Datta," Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?", Proceedings of IEEE Electron Devices Meeting (IEDM), 2008.

[291] G. A. Salvatore, D. Bouvet, A. M. Ionescu, "Demonstration of Subthrehold Swing Smaller Than 60 mV/decade in Fe-FET with P(VDF-TrFE)/SiO2 Gate Stack", IEDM 2008, San Francisco, USA, 15-17 December 2008.

[292] A. Rusu, G. A. Salvatore, D. Jiménez, A. M. Ionescu, "Metal-Ferroelectric-Metal- Oxide-Semiconductor Field Effect Transistor with Sub-60mV/decade Subthreshold Swing and Internal Voltage Amplification", IEDM 2010 , San Francisco, USA, 06-08 December 2010.

[293] Asif Islam Khan, Debanjan Bhowmik, Pu Yu, Sung Joo Kim, Xiaoqing Pan, Ramamoorthy Ramesh, Sayeef Salahuddin,"Experimental Evidence of Ferroelectric Negative Capacitance in Nanoscale Heterostructures," arXiv:1103.4419,2011.

[294] S. Salahuddin and S. Datta, `Use of negative capacitance to provide a subthreshold slope lower than 60 mV/ decade,` Nanoletters, vol. 8, No. 2, 2008.

[295] S. Salahuddin and S. Datta," Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?", Proceedings of IEEE Electron Devices Meeting (IEDM), 2008.

[296] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[297] A.M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M.J. Declercq, P. Renaud, C. Hibert, P. Fluckiger, G.A. Racine, "Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal-over-gate architecture," Proc. of International Symposium on Quality Electronic Design, ISQED 2002, pp. 496 – 501

[298] W. Y. Choi, H. Kam, D. Lee, J. Lai, T.-J. King Liu, "Compact Nano-Electro-Mechanical non-volatile memory (NEMory) for 3D integration," IEEE International Electron Devices Meeting Technical Digest, pp. 603 - 606, 2007.

[299] S.-W. Lee, R. W. Johnstone, A. M. Parameswaran, "MEMS mechanical logic units: characterization and improvements of devices fabricated with MicraGEM and PolyMUMPs," Proc. SPIE, 6037, pp. 1A1-1A10, 2005.

[300]R. S. Chakraborty, S. Narasimhan, S. Bhunia, "Hybridization of CMOS with CNT-based nano-electromechanical switch for low leakage and robust circuit design," IEEE Trans. Circ. and Syst. I, 54(11), pp. 2480-2488, 2007

[301] Y. Zhou, S. Thekkel, S. Bhunia, "Low power FPGA design using hybrid CMOS-NEMS approach," ISLPED Proceedings, pp. 14-19, 2007.

[302] T.-J. King Liu, J. Jeon, R. Nathanael, H. Kam, V. Pott, and E. Alon, "Prospects for MEM-relay logic switch technology," presented at the IEEE International Electron Devices Meeting (San Francisco, California, USA), December 2010.

[303] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[304]S. Fujita, K. Nomura, K. Abe, T. H. Lee, "3-D nanoarchitectures with carbon nanotube mechanical switches for future on-chip network beyond CMOS architecture," IEEE Trans. Circ. and Syst. I, 54(11), pp. 2472-2479, 2007.

[305]W. Y. Choi, H. Kam, D. Lee, J. Lai, T.-J. King Liu, "Compact Nano-Electro-Mechanical non-volatile memory (NEMory) for 3D integration," IEEE International Electron Devices Meeting Technical Digest, pp. 603 - 606, 2007.

[306] G. M. Rebeiz, RF MEMS: Theory, Design and Technology, Wiley, 2003.

[307] W. W. Jang, J. O. Lee, J.-B. Yoon, M.-S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park, W.-S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," Appl. Phys. Lett., 92(10), 103110, 2008

[308]S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amaratunga, D.-J. Kang, D. G. Hasko, J. E. Jung, J. M. Kim, "Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube," Appl. Phys. Lett., 86(8), 083105, 2005.

[309]Q. Li, S.-M. Koo, M. D. Edelstein, J. S. Suehle, C. A. Richter, "Silicon nanowire electromechanical switches for logic device application," Nanotechnology, 18, 315202, 2007.

[310] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[311]K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[312]T.-J. King Liu, J. Jeon, R. Nathanael, H. Kam, V. Pott, and E. Alon, "Prospects for MEM-relay logic switch technology," presented at the IEEE International Electron Devices Meeting (San Francisco, California, USA), December 2010.

[313]V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, T.-J. King Liu; Mechanical Computing Redux: Relays for Integrated Circuit Applications, Proceedings of the IEEE, Volume: 98 , Issue: 12, 2010, pp. 2076 – 2094

[314] W. W. Jang, J. O. Lee, J.-B. Yoon, M.-S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park, W.-S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," Appl. Phys. Lett., 92(10), 103110, 2008

[315]V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, T.-J. King Liu; Mechanical Computing Redux: Relays for Integrated Circuit Applications, Proceedings of the IEEE, Volume: 98 , Issue: 12, 2010, pp. 2076 – 2094.

[316] R. Waser and M. Aono, 'Nanoionics-based resistive switching memories'Nature materials, 6 (2007) 833.

317 H. Akinaga and H. Shima, 'Resistive Random Access Memory (ReRAM) Based on Metal Oxides' Proc. IEEE, 98 (2010) 2237

318 H. Akinaga and H. Shima, 'Resistive Random Access Memory (ReRAM) Based on Metal Oxides' Proc. IEEE, 98 (2010) 2237

319 T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama and M. Aono, Appl. Phys. Lett., 'Nanometer-scale switches using copper sulfide', 82 (2003) 3032

320 Z. Wang, T. Gu, T. Tada and S. Watanabe, 'Excess-silver-induced bridge formation in a silver sulfide atomic switch', Appl. Phys. Lett. 93 (2008) 152106

321 T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama and M. Aono, Appl. Phys. Lett., 'Nanometer-scale switches using copper sulfide', 82 (2003) 3032

322 Z. Wang, T. Gu, T. Tada and S. Watanabe, 'Excess-silver-induced bridge formation in a silver sulfide atomic switch', Appl. Phys. Lett. 93 (2008) 152106

323 M. Kundu, T. Hasegawa, K. Terabe and M. Aono, 'Effect of sulfurization condition on structural and electrical properties of copper sulfide films', J. Appl. Phys., 103 (2008) 073523

[324] M. Kundu, T. Hasegawa, K. Terabe and M. Aono, 'Effect of sulfurization conditions and post deposition annealing treatment on the structural and electrical properties of silver sulfide films', J. Appl. Phys., **99** (2006) 103501.

325 M. M. Masis, S. J. van der Molen, W. T. Fu, M. B. Hesselberth and J. M. van Ruitenbeek, 'Conductance switching in Ag2S devices fabricated by in situ sulfurization', Nanotechnol., 20 (2009) 095710.

326 K. Terabe, T. Hasegawa, T. Nakayama and M. Aono, 'Quantized conductance atomic switch', Nature 433 (2005) 47.

327 K. Szot, W. Speier, G. Bihlmayer and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline SrTiO3," Nature Mater., 5 (2006) 312.

328 Ch. Liang, K. Terabe, T. Hasegawa, R. Negishi, T. Tamura and M. Aono, ''Ionic-Electronic Conductor Nanostructures: Template-Confined Growth and Nonlinear Electrical Transport', Small, 10 (2005) 971.

329T. Sakamoto, K. Lister, N. Banno, T. Hasegawa, K. Terabe, and M. Aono, ''Electronic transport in Ta2O5 resistive switch', Appl. Phys. Lett., 91 092110 (2007).

[330] N. Banno, T. Sakamoto, S. Fujieda and M. Aono, 'On-state reliability of solid-electrolyte switch', *Proc. Int. Reliabil. Phys. Symp*., Phoenix, 2008, p.707.

[331] R. Soni, P. Meuffels, H. Kohlstedt, C. Kugeler and R. Waser, 'Reliability analysis of the low resistance state stability of $Ge_{0.3}Se_{0.7}$ based solid electrolyte nonvolatile memory cell', Appl. Phys. Lett., 94 (2009) 123503.

[332] M. N. Kozicki M. Park and M. Mitkova, 'Nanoscale memory elements based on solid-state electrolytes', IEEE Trans. Nanotechnol., 4 (2005) 331.

[333] C. Schindler, G. Staikov and R. Waser, 'Electrode kinetics of Cu-SiO_2-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories', Appl. Phys. Lett., 94 (2009) 072109.

[334] M. Haemori, T. Nagata and T. Chikyow, 'Impact of Cu electrode on switching behavior in a Cu/HfO_2/Pt structure and resultant Cu ion diffusion', Appl. Phys. Express, 2 (2009) 061401.

[335] Y. Naitoh, Y. Morita, M. Horikawa, H. Suga and T. Shimizu, 'Non-volatile resistive switching using silicon nanogap junction', Appl. Phys. Express, 1 (2008) 103001.

[336] S. Kaeriyama, T. Sakamoto, H. Sunamura, M. Mizuno, H. Kawaura, T. Hasegawa, K. Terabe, T. Nakayama, and M. Aono, 'A nonvolatile programmable solid-electrolyte nanometer switch', *IEEE J. Solid-State Circuits*, **40** 168 (2005).

[337] M. Tada, T. Sakamoto, Y. Tsuji, N. Banno, Y. Saito, Y. Yabe, S. Ishida, M. Terai, S. Kotsuji, N. Iguchi, M. Aono, H. Hada, and N. Kasai, 'Highly Scalable Nonvolatile TiOx/TaSiOy Solid-electrolyte Crossbar Switch Integrated in Local Interconnect for Low Power Reconfigurable Logic', in Tech. Dig. IEEE Int. Electron Device Meeting, pp. 943- (2009).

[338] T. Sakamoto, N. Iguchi and M. Aono, 'Nonvolatile triode switch using electrochemical reaction in copper sulfide', Appl. Phys. Lett., **96** (2010) 252104.

[339] T. Hasegawa, Y. Itoh, H. Tanaka, T. Hino, T. Tsuruoka, K. Terabe, H. Miyazaki, K. Tsukagoshi, T. Ogawa, S. Yamaguchi and M. Aono, 'Volatile/Nonvolatile Dual-Functional Atom Transistor', APEX, **4** (2011) 015204.

[340] T. Sakamoto, N. Iguchi and M. Aono, 'Nonvolatile triode switch using electrochemical reaction in copper sulfide', Appl. Phys. Lett., **96** (2010) 252104.

[341]T. Hasegawa, Y. Itoh, H. Tanaka, T. Hino, T. Tsuruoka, K. Terabe, H. Miyazaki, K. Tsukagoshi, T. Ogawa, S. Yamaguchi and M. Aono, 'Volatile/Nonvolatile Dual-Functional Atom Transistor', APEX, **4** (2011) 015204.

[342] N. Banno, T. Sakamoto, S. Fujieda and M. Aono, 'On-state reliability of solid-electrolyte switch', *Proc. Int. Reliabil. Phys. Symp*., Phoenix, 2008, p.707.

[343] K. Aratani, K. Ohba, T. Mizuguchi, S. Yasuda, T. Shiimoto, T. Tsushima, T. Sone, K. Endo, A. Kouchiyama, S. Sasaki, A. Maesaka, N. Yamada and H. Narisawa, 'A Novel Resistance Memory with High Scalability and Nanosecond', in Tech. Dig. IEEE Int. Electron Device Meeting, pp. 783-786 (2007).

[344]K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, 'Low power and high speed switching of Ti-doped NiO ReRAM under the unipolar voltage source of less than 3V', in Tech. Dig. IEEE Int. Electron Device Meeting, pp. 767–770 (2007).

[345] M. N. Kozicki M. Park and M. Mitkova, 'Nanoscale memory elements based on solid-state electrolytes', IEEE Trans. Nanotechnol., 4 (2005) 331

[346]T. Hasegawa, Y. Itoh, H. Tanaka, T. Hino, T. Tsuruoka, K. Terabe, H. Miyazaki, K. Tsukagoshi, T. Ogawa, S. Yamaguchi and M. Aono, 'Volatile/Nonvolatile Dual-Functional Atom Transistor', APEX, **4** (2011) 015204.

[347]I. Valov, R. Waser, J. R. Jameson and M. N. Kozicki, 'Electrochemical metallization memories-fundamentals, applications, prospects', Nanotechnol., **22** (2011) 254003.

[348] C. Zhou, D. M. Newns, J. A. Misewich and P. C. Pattnaik, Appl Phys Lett **70** (5), 598-600 (1997)

[349] D. M. Newns, J. A. Misewich, C. C. Tsuei, A. Gupta, B. A. Scott and A. Schrott, Appl Phys Lett **73** (6), 780-782 (1998)

[350] D. M. Newns, J. A. Misewich, C. C. Tsuei, A. Gupta, B. A. Scott and A. Schrott, Appl Phys Lett **73** (6), 780-782 (1998)

[351] Z. Yang, C. Ko and S. Ramanathan, Annual Review of Materials Research **41**, 8.1 (2011).

[352] A. Cavalleri, Cs. Toth, C. W. Siders, J. A. Squier, F. Raksi, P. Forget and J. C. Keiffer, Phy. Rev. Lett. 87, 237401 (2001)

[353] S. Hormoz and S. Ramanathan, Solid State Electron **54** (6), 654-659 (2010)

[354] H. T. Kim, B. G. Chae, D. H. Youn, S. L. Maeng, G. Kim, K. Y. Kang and Y. S. Lim, New J Phys **6**, 52 (2004)

[355] G. Stefanovich, A. Pergament and D. Stefanovich, J. Phys: Cond Mat, 12, 8837 (2000)

[356] D. Ruzmetov, G. Gopalakrishnan, C. Ko, V. Narayanamurti and S. Ramanathan, J Appl Phys **107** (11), 114516 (2010)

[357] Y. Zhang and S. Ramanathan, Solid State Electronics, August 2011, pp. 161-164 (2011)

[358] S. D. Ha, G. H. Aydogdu and S. Ramanathan, Appl. Phys. Lett., 98, 012105 (2011)

[359] P. Lacorre, J. B. Torrance, J. Pannetier, A. I. Nazzal, P. W. Wang and T. C. Huang, J. Sol. St. Chem. 91, 225 (1991)

[360] A. Khitun and K. L. Wang, "Non-volatile magnonic logic circuits engineering," *http://arxiv.org/abs/1012.4768*, 2010.

[361]A. Khitun, D. E. Nikonov, and K. L. Wang, "Magnetoelectric spin wave amplifier for spin wave logic circuits," *Journal of Applied Physics*, vol. 106, pp. 123909-7, 2009.

[362]A. Khitun, M. Bao, Y. Wu, J.-Y. Kim, A. Hong, A. Jacob, K. Galatsis, and K. L. Wang, "Logic Devices with Spin Wave Buses - an Approach to Scalable Magneto-Electric Circuitry," *Mater. Res. Soc. Symp. Proceedings*, vol. 1067, pp. B01-04, 2008.

[363]Y. Wu, M. Bao, A. Khitun, J.-Y. Kim, A. Hong, and K. L. Wang, "A Three-Terminal Spin-Wave Device for Logic Applications," *Journal of Nanoelectronics and Optoelectronics*, vol. 4, pp. 394-397, 2009.

[364] Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G. H., & Porod, W. (2006). Majority logic gate for Magnetic Quantum-dot Cellular Automata. *Science, 311*(5758), 205-208.

[365] Nikonov, D. E., Bourianoff, G. I., & Gargini, P. A. (2008). Suitability for Digital Logic and Scaling of Atomistic Magnetic QCA. *Device Research Conference, 2008*, 163-164.

[366] Waser, R. (2003). *Nanoelectronics and information technology: Advanced electronic materials and novel devices*. Weinheim: Wiley-VCH.

[367]Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G. H., & Porod, W. (2006). Majority logic gate for Magnetic Quantum-dot Cellular Automata. *Science, 311*(5758), 205-208

[368]Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G. H., & Porod, W. (2006). Majority logic gate for Magnetic Quantum-dot Cellular Automata. *Science, 311*(5758), 205-208.

[369] Kurtz, S., Varga, E., Niemier, M., Porod, W., Bernstein, G. H., & Hu, X. S. (2011). Two Input, Non-Majority Magnetic Logic Gates: Experimental Demonstration and Future Prospects. *Journal of Physics: Condensed Matter, 23*(5), 053202.

[370] Varga, E., Niemier, M. T., Bernstein, G. H., Porod, W., & Hu, X. S. (2009). Non-volatile and Reprogrammable MQCA-based Majority Gates. *Device Research Conference*, 1-2.

[371] Varga, E., Orlov, A., Niemier, M. T., Hu, X. S., Bernstein, G. H., & Porod, W. (2010). Experimental Demonstration of Fanout for Nanomagnetic Logic. *Nanotechnology, IEEE Transactions on, 9*(6), 668-670.

[372] Alam, M. T., Kurtz, S., Siddiq, M. J., Niemier, M. T., Bernstein, G. H., Hu, X. S., et al. (2011). On-chip Clocking of Nanomagnet Logic Lines and Gates. *submitted to IEEE T. on Nanotechnology.*

[373] Csaba, G., Lugli, P., & Porod, W. (2004). *Power dissipation in nanomagnetic logic devices.* Paper presented at the 2004 4th IEEE Conference on Nanotechnology.

[374] Alam, M. T., Siddiq, M. J., Bernstein, G. H., Niemier, M., Porod, W., & Hu, X. S. (2010). On-Chip Clocking for Nanomagnet Logic Devices. *IEEE Transactions on Nanotechnology, 9*(3), 348-351.

[375]Alam, M. T., Kurtz, S., Siddiq, M. J., Niemier, M. T., Bernstein, G. H., Hu, X. S., et al. (2011). On-chip Clocking of Nanomagnet Logic Lines and Gates. *submitted to IEEE T. on Nanotechnology.*

[376] Niemier, M. T., Hu, X. S., Alam, M., Bernstein, G., Porod, W., Putney, M., et al. (2007). Clocking Structures and Power Analysis for Nanomagnet-Based Logic Devices. *International Symposium on Low Power Electronics and Design (ISLPED)*, 26-31.

[377] Mohammad Salehi, F., & et al. (2011). Magnetization dynamics, Bennett clocking and associated energy dissipation in multiferroic logic. *Nanotechnology, 22*(15), 155201.

[378] Chu, Y. H., Martin, L. W., Holcomb, M. B., Gajek, M., Han, S. J., He, Q., et al. (2008). Electric-field control of local ferromagnetism using a magnetoelectric multiferroic. [Article]. *Nature Materials, 7*(6), 478-482.

[379] Liu, S., Hu, X. S., Nahas, J. J., Niemier, M. T., Porod, W., & Bernstein, G. H. (2010). Magnetic-Electrical Interface for Nanomagnet Logic. *IEEE T. on Nanotechnology, PP*, 1-1.

[380] Niemier, M. T., Bernstein, G. H., Dingler, A., Hu, X. S., Kurtz, S., Liu, S., et al. (2011). Nanomagnet Logic: Progress Toward System-Level Integration. *Journal of Physics - Condensed Matter, under review.*

[381] Carlton, D. B., Emley, N. C., Tuchfeld, E., & Bokor, J. (2008). Simulation Studies of Nanomagnet-Based Logic Architecture. *Nano Letters, 8*(12), 4173-4178.

[382]Carlton, D. B., Emley, N. C., Tuchfeld, E., & Bokor, J. (2008). Simulation Studies of Nanomagnet-Based Logic Architecture. *Nano Letters, 8*(12), 4173-4178

[383]Niemier, M. T., Bernstein, G. H., Dingler, A., Hu, X. S., Kurtz, S., Liu, S., et al. (2011). Nanomagnet Logic: Progress Toward System-Level Integration. *Journal of Physics - Condensed Matter, under review*

[384]Kurtz, S., Varga, E., Niemier, M., Porod, W., Bernstein, G. H., & Hu, X. S. (2011). Two Input, Non-Majority Magnetic Logic Gates: Experimental Demonstration and Future Prospects. *Journal of Physics: Condensed Matter, 23*(5), 053202

[385]Niemier, M. T., Bernstein, G. H., Dingler, A., Hu, X. S., Kurtz, S., Liu, S., et al. (2011). Nanomagnet Logic: Progress Toward System-Level Integration. *Journal of Physics - Condensed Matter, under review.*

[386] Niemier, M., Hu, X. S., Dingler, A., Alam, M. T., Bernstein, G., & Porod, W. (2008). Bridging the Gap between Nanomagnetic Devices and Circuits. *2008 IEEE International Conference on Computer Design*, 506-513.

[387] Cloizeaux, J. (1965). Exciton instability and crystallographic anomalies in semiconductors. *Journal of Physics and Chemistry of Solids, 26*(2), 259-266

[388] Halperin, B. & Rice, T. (1968). Possible Anomalies at a Semimetal-Semiconductor Transistion. *Reviews of Modern Physics, 40*(4), 755-766.

[389] Jérome, D., Rice, T., & Kohn, W. (1967). Excitonic Insulator. *Physical Review, 158*(2), 462-475.

[390] Knox, R. S. (1963). Theory of excitons. *Solid State Physics, suppl. 5* (p. 100). Academic Press New York.

[391]Kohn, W. & Sherrington, D. (1970). Two Kinds of Bosons and Bose Condensates. *Reviews of Modern Physics, 42*(1), 1-11. Emerald Group Publishing Limited.

[392] Mott, N. F. (1961). The transition to the metallic state. *Philosophical Magazine, 6*(62), 287-309. Taylor & Francis.

[393] Bucher, B., Steiner, P., & Wachter, P. (1991). Excitonic insulator phase in TmSe_{0.45}Te_{0.55}. *Physical Review Letters*, *67*(19), 2717-2720

[394]Cercellier, H., Monney, C., Clerc, F., Battaglia, C., Despont, L., Garnier, M. G., et al. (2007). Evidence for an excitonic insulator phase in 1T-TiSe2. *Physical review letters*, *99*(14), 146403

[395]Neuenschwander, J., Wachter, P., Bu¨hrer, W., & Fischer, P. (1988). Electron-hole interaction in TmSe1−xTex under pressure. *Journal of Applied Physics*, *63*(8), 3399

[396]Wachter, P., Jung, A., & Pfuner, F. (2006). Exciton condensation in intermediate valent Sm0.90La0.10S. *Physics Letters A*, *359*(5), 528-533

[397]Wachter, P., Jung, A., & Steiner, P. (1995). Pressure-driven metal-insulator transition in La-doped SmS: Excitonic condensation. *Physical Review B*, *51*(8), 5542

[398]Wannier, G. (1937). The Structure of Electronic Excitation Levels in Insulating Crystals. *Physical Review*, *52*(3), 191-197

[399]Datta, S., Melloch, M., & Gunshor, R. (1985). Possibility of an excitonic ground state in quantum wells. *Physical Review B*, *32*(4), 2607-2609.

[400] Butov, L., Zrenner, A., Abstreiter, G., Böhm, G., & Weimann, G. (1994). Condensation of Indirect Excitons in Coupled AlAs/GaAs Quantum Wells. *Physical Review Letters*, *73*(2), 304-307

[401]Cheng, J. P., Kono, J., McCombe, B., Lo, I., Mitchel, W., & Stutz, C. (1995). Evidence for a stable excitonic ground state in a spatially separated electron-hole system. *Physical review letters*, *74*(3), 450–453.

[402] Fukuzawa, T., Mendez, E., & Hong, J. (1990). Phase transition of an exciton system in GaAs coupled quantum wells. *Physical review letters*, *64*(25), 3066–3069.

[403]Wang, E., Zhou, Y., Ting, C., Zhang, J., Pang, T., & Chen, C. (1995). Excitons in spatially separated electron–hole systems: A quantum Monte Carlo study. *Journal of applied physics*, *78*(12), 7099–7102

[404]**B**erman, O. L. (1998). Quantum crystallization of two-dimensional dipole systems. *Physics of the Solid State*, *40*(7).

[405]Reyes, J., & Castillo-Mussot, M. del. (1998). Wannier-Mott exciton formed by electron and hole separated in parallel quantum wires. *Physical Review B*, *57*(3), 1690.

[406]Perebeinos, V., Tersoff, J., & Avouris, P. (2004). Scaling of Excitons in Carbon Nanotubes. *Physical Review Letters*, *92*(25), 8-11

[407]Spataru, C., Ismail-Beigi, S., Benedict, L., & Louie, S. (2004). Excitonic Effects and Optical Spectra of Single-Walled Carbon Nanotubes. *Physical Review Letters*, *92*(7), 1-4

[408] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," IEEE Electron Device Lett. **30**, 158-160 (2009).

[409] H. Min, R. Bistritzer, J.-J. Su, and A. H. MacDonald, "Room temperature superfluidity in graphene bilayers," Phys. Rev. B **78**, article no. 121401 (2008).

[410] I. B. Spielman, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, "Resonantly enhanced tunneling in a double layer quantum Hall ferromagnet," Phys. Rev. Lett. **84**, 5808-5811 (2000).

[411] J. P. Eisenstein and A. H. MacDonald, "Bose–Einstein condensation of excitons in bilayer electron systems," Nature (London) **432**, 691 (2004).

[412] M. Kellogg, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, "Vanishing Hall resistance at high magnetic field in a double layer two-dimensional electron system," Phys. Rev. Lett.. **93**, article no. 036801 (2004).

[413] E. Tutuc, M. Shayegan, and D. A. Huse, "Counterflow measurements in strongly correlated GaAs hole bilayers: Evidence for electron–hole pairing," Phys. Rev. Lett. **93**, article no 036802 (2004).

[414]S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," IEEE Electron Device Lett. **30**, 158-160 (2009).

[415] J.-J. Su and A. H. MacDonald, "How to make a bilayer exciton condensate flow," Nat. Phys. **4**, 799 (2008).

[416] L. Tiemann, W. Dietsche, M. Hauser, and K. von Klitzing, "Critical tunneling currents in the regime of bilayer excitons," New J. Phys. **10**, 045018 (2008).

[417] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," IEEE Electron Device Lett. **30**, 158-160 (2009).

[418] D. Basu, L. F. Register, Dharmendar Reddy, A. H. MacDonald, and S. K. Banerjee, "Tight-binding study of electron-hole pair condensation in graphene bilayers: Gate control and system-parameter dependence" Phys. Rev. B. **82**, article no. 075409, (2010).

[419] D. Basu, L. F. Register, A. H. MacDonald and S. K. Banerjee, "On the effect of interlayer bare tunneling on electron-hole coherence in graphene bilayers," Phys. Rev. B., in review.

[420] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," IEEE Electron Device Lett. **30**, 158-160 (2009).

[421] D. Reddy, L. F. Register, E. Tutuc, A. H. MacDonald, and S. K. Banerjee, "Bilayer pseudoSpin field effect transistor (BiSFET): A proposed logic device and circuits, Device Research Conference," June 2009, pp. 67-68.; D. Reddy, L. F. Register, E. Tutuc, and S. K. Banerjee, IEEE Trans. Electron Devices **57**, 755-763 (2010).

[422] C. Pacha, K. Goser, A. Brennemann, and W. Prost. "A Threshold Logic Full Adder Based on Resonant Tunneling Transistors," Proceedings of the 24th European Solid-State Circuits Conference ESSCIRC, The Hague, NL, pages 428–431, September 1998.

[423] D. Reddy, L. F. Register, E. Tutuc, A. H. MacDonald, and S. K. Banerjee, "Bilayer pseudoSpin field effect transistor (BiSFET): A proposed logic device and circuits, Device Research Conference," June 2009, pp. 67-68.; D. Reddy, L. F. Register, E. Tutuc, and S. K. Banerjee, IEEE Trans. Electron Devices **57**, 755-763 (2010).

[424] D. Reddy, L. F. Register, and S. K. Banerjee, "Graphene Field Effect Transistors," Journal of Physics D: Applied physics, in review (Invited review article).

[425] http://www.src.org/program/nri/

[426] J. C. Slonczewski, "Current-driven excitation of magnetic multilayers", J. Magn. Magn. Mater. Vol. 159, 1996, p. L1

[427] S. I. Kiselev, J. C. Sankey, I. N. Krivorotov, N. C. Emley, R. J. Schoelkopf, R. A. Buhrman, D. C. Ralph, Nature vol. 425, 2003, p. 380

[428] S. Kaka, M.R. Pufall, W.H. Rippard, T.J. Silva, S.E. Russek, and J.A. Katine, "Mutual phase-locking of microwave spin torque nano-oscillators", Nature vol. 437, 2005, p. 389

[429] F.B. Mancoff, N.D. Rizzo, B.N. Engel, and S. Tehrani, "Phase-locking in double-point-contact spin transfer devices", Nature vol. 437, 2005, 393

[430] Slavin, A., Tiberkevich, V., Nonlinear auto-oscillator theory of microwave generation by spin-polarized current. *IEEE Trans. Magn.* Vol. 45, 2009, p. 1875

[431] C.T. Boone, J. A. Katine, J. R. Childress, V. Tiberkevich, A. Slavin, J. Zhu, X. Cheng, I. N. Krivorotov, "Resonant Nonlinear Damping of Quantized Spin Waves in Ferromagnetic Nanowires: A Spin Torque Ferromagnetic Resonance Study", Phys. Rev. Lett. vol. 103, 2009, p. 167601

[432] D. C. Ralph and M. D. Stiles, "Spin Transfer Torques", J. Magn. Magn. Mater. Vol. 320, 2008, p. 1190

[433] D. E. Nikonov, G. I. Bourianoff, and T. Ghani, "Proposal of a spin torque majority gate logic", arXiv:1006.4663, 2010

[434] J. Z. Sun and D. C. Ralph, "Magnetoresistance and spin-transfer torque in magnetic tunnel junctions", J. Magn. Magn. Mater. Vol. 320, 2008, p. 1227

[435] B. Behin-Aein, D. Datta, S. Salahuddin and S. Datta, *Nature Nanotech*. vol. 5, p.266, (2010).

[436] F.J. Jedeema, A.T. Filip and B.J. Van Wees, *Nature*, vol. 410, p.345, (2001).

[437] F. J. Jedeema, M. S. Nijboer, A. T. Filip and B. J. van Wees, *Phys. Rev. B.*, vol. 67, p. 085319 (2003

[438] B.T. Jonker et al., *Nature Phys.*, vol. 5, p. 817 (2006).

[439] I. Appelbaum, B. Huang and D.J. Monsma, *Nature*, vol. 447, p. 295 (2007).

[440] N. Tombros, et al., *Nature*, 448, p. 571 (2007

[441] Lou, X. et al., *Nature Physics*, vol. 3, p.197 (2007).

[442] T. Yang, K. Kimura and Y. Otani, *Nature Phys.*, vol. 4, p. 851, (2008).

[443] J.Z. Sun et al., *APL*, vol. 95, p.083506, (2009).

[444] F.J. Jedeema, A.T. Filip and B.J. Van Wees, *Nature*, vol. 410, p.345, (2001).

[445] F. J. Jedeema, M. S. Nijboer, A. T. Filip and B. J. van Wees, *Phys. Rev. B.*, vol. 67, p. 085319 (2003).

[446] J.Z. Sun et al., *APL*, vol. 95, p.083506, (2009).

[447] B.T. Jonker et al., *Nature Phys.*, vol. 5, p. 817 (2006).

[448] I. Appelbaum, B. Huang and D.J. Monsma, *Nature*, vol. 447, p. 295 (2007).

[449] N. Tombros, et al., *Nature*, 448, p. 571 (2007).

[450] Lou, X. et al., *Nature Physics*, vol. 3, p.197 (2007).

[451] T. Yang, K. Kimura and Y. Otani, *Nature Phys.*, vol. 4, p. 851, (2008).

[452] J.Z. Sun et al., *APL*, vol. 95, p.083506, (2009).

[453] B. Behin-Aein, A. Sarkar, S. Srinivasan and S. Datta, *APL*, vol. 98, p. 123510, (2011).

[454] D. Weller et al., IEEE Tran. Magn. 36, 10, (2000)

[455] S. B. Akers, Proc. 3rd Ann. Symp. on Switching Circuit Theory and Logical Design, pp. 150, 1962.

[456] L. Liao, Y.-C. Lin, M.Bao, R. Cheng, J.Bai, Y. Liu, Y.Qu, K. L. Wang, Y. Huang, X.Duan, "High-speed graphene transistors with a self-aligned nanowire gate," Nature 467, 305 (2010)

[457] Ph. Avouris, Y.-M. Lin, F. Xia, D.B. Farmer, T. Mueller, C. Dimitrakopoulos, K. Jenkins, A. Grill, "Graphene-Based Fast Electronics and Optoelectronics," IEDM 2010, pp. 552 – 555

[458] J. Lee, H.-J. Chung, J. Lee, H. Shin, J. Heo, H. Yang, S.-H. Lee, J. Shin, S. Seo, U. Chung, I. Yoo, K. Kim, "RF Performance of Pre-Patterned Locally-Embedded-Back-Gate Graphene Device," IEDM 2010, pp. 568 – 571

[459] D.Waldmann, J.Jobst, F. Speck, T.Seyller, M. Krieger, H. B. Weber, "Bottom-gated epitaxial graphene," Nature Mat. 10, 357 – 360 (2011)

[460] L. Liao, J.Bai, R. Cheng, Y.-C. Lin, S. Jiang, Y.Qu, Y. Huang, X.Duan, "Sub-100 nm Channel Length Graphene Transistors," Nano Lett. 10, 3952 (2010)

[461] F.Schwierz, "Graphene Transistors," Nature Nanotechnology 5, 487 (2010)

[462] S. I. Kiselev, J. C. Sankey, I. N. Krivorotov, N. C. Emley, R. J. Schoelkopf, R. A. Buhrman, and D. C. Ralph, "Microwave oscillation of nanomagnet driven by a spin-polarized current", Nature 425, 380 (2003)

[463] W. H. Rippard, M. R. Pufall, S. Kaka, S. E. Russek, and T. J. Silva, "Direct-Current Induced Dynamics in Co90Fe10/Ni80Fe20 Point Contacts", Phys. Rev. Lett. 92, 027701(2004)

[464] J.A. Katine, and Eric E. Fullerton, "Device implications of spin-transfer torques ", J. of magnetism and magnetic materials 320, 1217(2008)

[465] P. Villard, U. Ebels, D. Houssameddine, J. Katine, D. Mauri, B. Delaet, P. Vincent, M.-C. Cyrille, B. Viala, J.-P. Michel, J. Prouvée, and F. Badets, "A GHz Spintronic-Based RF Oscillator", IEEE J. Solid-State Circ. 45, 214(2010)

[466] Y. Guan, D. W. Abraham, M. C. Gaidis, G. Hu, E. J. O'Sullivan, J. J. Nowak, P. L. Trouilloud, D. C. Worledge, and J. Z. Sun, "Field and bias dependence of high-frequency magnetic noise in MgO-based magnetic tunnel junctions", J. Appl. Phys. 105, 07D127(2009)

[467] W. H. Rippard, M. R. Pufall, and S. E. Russek, "Comparison of frequency, linewidth, and output power in measurements of spin-transfer nanocontact oscillators", Phys. Rev. B 74, 224409(2006)

[468] A. M. Deac, A. Fukushima, H. Kubota, H. Maehara, Y. Suzuki, S. Yuasa, Y. Nagamine, K. Tsunekawa, D. Djayaprawira, and N. Watanabe, "Bias-driven high-power microwave emission from MgO-based tunnel magnetoresistance devices", Nature Phys. 4, 803(2008)

[469] D. Houssameddine, U. Ebels, B. Delae, B. Rodmacq, I. Firastau, F. Ponthenier, M. Brunet, C. Thirion, J.-P. Michel, L. Prejbeanu-Buda, M.-C. Cyrille, O. Redon, and B. Dieny, "Spin-torque oscillator using a perpendicular polarizer and a planar free layer", Nature Mat. 6, 447(2007)

[470] V. S. Pribiag, I. N. Krivorotov, G. D. Fuchs, P. M. Braganca, O. Ozatay, J. C. Sankey, D. C. Ralph, and R. A. Buhrman, "Magnetic vortex oscillator driven by d.c. spin-polarized current", Nature Phys. 3, 498(2007)

[471] O. Boulle, V. Cros, J. Grollier, L. G. Pereira, C. Deranlot, F. Petroff, G. Faini, J. Barna, and A. Fert, "Shaped angular dependence of the spin-transfer torque and microwave generation without magnetic field", Nature Phys. 3, 492(2007)

[472] S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, and J. A. Katine, "Mutual phase-locking of microwave spin torque nano-oscillators", Nature 437, 389(2005)

[473] F. B. Mancoff, N. D. Rizzo, B. N. Engel, and S. Tehrani, "Phase-locking in double-point-contact spin-transfer devices", Nature 437, 393(2005)

[474] A. Ruotolo, V. Cros, B. Georges, A. Dussaux, J. Grollier, C. Deranlot, R. Guillemet, K. Bouzehouane, S. Fusil, and A. Fert, "Phase-locking of magnetic vortices mediated by antivortices", Nature Nano. 4, 528(2009)

[475] D. Houssameddine, U. Ebels, B. Dieny, K. Garello, J.-P. Michel, B. Delaet, B. Viala, M.-C. Cyrille, J. A. Katine, and D. Mauri, "Temporal Coherence of MgO Based Magnetic Tunnel Junction Spin Torque Oscillators", Phys. Rev. Lett. 102, 257202 (2009)

[476] A. Slavin, and V. Tiberkevich, "Nonlinear Auto-Oscillator Theory of Microwave Generation by Spin-Polarized Current", IEEE Trans. Mag. 45, 1875(2009)

[477] J.-V. Kim, V. Tiberkevich, and A. N. Slavin, "Generation Linewidth of an Auto-Oscillator with a Nonlinear Frequency Shift: Spin-Torque Nano-Oscillator", Phys. Rev. Lett. 100, 017207(2008)

[478] C.T.C. Nguyen, "MEMS technology for timing and frequency control," IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control 54 (2), 251 (2007)

[479] K. Jensen, H.B. Peng, and A. Zetl, "Limits of Nanomechanical Resonators," Proc. of International Conference on Nanoscience and Nanotechnology ICONN 2006, pp. 68-71

[480] J.R. Vig and Y. Kim, "Noise in Microelectromechanical System Resonators," IEEE Trans. Ultrasonics, Ferroelectrics, and Frequency Control 46 (6), 1558 (1999)

[481] Y. Xie, S.-S. Li, Y.-W. Lin, Z, Ren, and C.T.-C. Nguyen, "UHF Microlectromechanical Extensional Wine-Glass Mode Ring Resonators," IEDM 2003, pp. 953-956

[482] D. Weinstein and S. Bhave, "Piezoresistive Sensing of a Dielectrically Actuated Silicon Bar Resonator," Proc. of Solid-State Sensors, Actuators and Microsystems Workshop 2008, pp. 368-371

[483] D. Weinstein and S. Bhave, "Internal dielectric transduction of a 4.5GHz silicon bar resonator," IEDM 2007, pp. 415-41

[484] A. Hussain, J. Hone, H.W. Postma, X.M.H. Huang, T. Drake, M. Narbic, A Scherer, and M.L. Roukes, "Nanowire–based very-high-frequency electromechanical resonator," Appl. Phys. Lett. 83 (6), 1240 (2003)

[485] X.L. Feng, R. He, P. Yang, and M.L. Roukes, "Very High Frequnecy Silicon Nanowire Electromechanical Resonators," Nano Lett. 7 (7), 1953 (2007)

[486] R. He, X.L. Feng, M.L. Roukes, and P. Yang, "Self-transducing Silicon Nanowire Electromechancial Systems at Room Temperature," Nano Lett. 8 (6), 1756 (2008)

[487] V. Sazonova, Y. Yaish, H. Ustunel, D. Roundy, T.A. Arlas, and P.L. McEuen, "A tunable carbon nanotube electromechanical oscillator," Nature 431, 284 (2004)

[488] H.B. Peng, C.W. Chang, S. Aloni, T.D. Yuzvinsky, and A. Zettl, "Ultrahigh Frequency Nanotube Resonators," Phys. Rev. Lett. 97, 087203 (2006)

[489] H.B. Peng, C.W. Chang, S. Aloni, T.D. Yuzvinsky, and A. Zettl, "Microwave Electromechanical Resonator Consisting of Clamped Carbon Nanotubes in an Abacus Arrangement," Phys. Rev. B76, 035405 (2007)

[490]] J. Scott Bunch, A.M. van der Zande, S.S. Verbridge, I.W. Frank, D.M. Tanenbaum, J.M. Parpia, H.G. Craighead, and P.L. McEuen, "Electromechanical Resonators from Graphene Sheets," Science 315, 490 (2007)

[491] N. Abele, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A.M. Ionescu, "Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor," IEDM 2005, pp. 479 – 481

[492] N. Abele; K. Segueni; K. Boucart; F. Casset; B. Legrand; L. Buchaillot; P. Ancey, and A.M. Ionescu, "Ultra-Low Voltage MEMS Resonator Based on RSG-MOSFET," IEEE MEMS 2006, pp. 882 – 885

[493]] D. Grogg, D. Tsamados, N.D. Badila, and A.M. Ionescu, "Integration of MOSFET Transistors in MEMS Resonators for Improved Output Detection," Transducers 2007, pp. 1709 – 1712

[494] C. Durand, F. Casset, P. Renaux, N. Abele, B. Legrand, D. Renaud, E. Ollier, P. Ancey, A.M. Ionescu, and L. Buchaillot, "In-Plane Silicon-On-Nothing Nanometer-Scale Resonant Suspended Gate MOSFET for In-IC Integration Perspectives," IEEE Elect. Dev. Lett. 29 (5), 494 (2008

[495] E. Colinet, C. Durand, L. Duraffourg, P. Audebert, G. Dumas, F. Casset, E. Ollier, P. Ancey, J.-F. Carpentier, L. Buchaillot, and A.M. Ionescu, "Ultra-Sensitive Capacitive Detection Based on SGMOSFET Compatible With Front-End CMOS Process," IEEE J. Solid-State Circ. 44 (1), 247 (2009)

[496] D. Grogg, H.C. Tekin, N.D. Badila-Ciressan, M. Mazza, D. Tsamados, and A.M. Ionescu, "Laterally vibrating-body double gate MOSFET with improved signal detection," DRC 2008, pp. 155-156

[497] D. Grogg, M. Mazza, D. Tsamados, and A.M. Ionescu, "Multi-gate vibrating-body field effect transistor (VB-FETs)," IEDM 2008, pp. 663 – 666

[498] J.T.M.van Beek, K.L. Phan, G.J.A.M. Verheijden, G.E.J. Koops, C. van der Avoort, J. van Wingerden, D.E. Badaroglu, J.J.M. Bontemps, and R. Puers, "A piezo-resistive resonant MEMS amplifier," IEDM 2008, pp. 667-670

[499] L. Pierantonian and F. Coccetti, "Radio-frequency nanoelectronics: A new paradigm in electronic systems design," 2010 Asia-Pacific Microwave Conference Proceedings (APMC), pp. 1007-1014

[500] N. V. Alkeev, S. V. Averin, A. A. Dorofeev, E 1. Golant, and A. B. Pashkovskii, "New TeraHertz Mixer Based on Resonant-Tunneling Diode," Proc. Int'l Symp. on Phys. and Engr. of Microwaves, Millimeter and Submillimeter Waves (MSMW), Jun. 2007, pp. 192-194 (2007)

[501] I. Magrini and A. C. G. Manes, "A Low Local Oscillator Power K-Band Mixer Based on Tunneling Diodes," Microwave and Opt. Tech. Lett., 51(4), 1140 (2009)

[502] R. Knobel, C. S. Yung, and A. N. Cleland, "Single-electron transistor as a radio-frequency mixer," Appl. Phys. Lett., 81 (3), 532 (2002)

[503] K.-H. Oh, N. Shimizu, N. Kukutsu, Y. Kado, S. Kohjiro, K. Kikuchi, T. Yamada and A. Wakatsuki, "Heterodyne THz-wave receiver with a superconducting tunneling mixer driven by a high sweeping-speed photonics-based THz-wave local oscillator," IEICE Electronics Express, 6(10), 601 (2009)

[504] T. Palacios, A. Hsu, and H. Wang, "Applications of Graphene Devices in RF Communications," IEEE Comm. Mag., 48 (6), 122 (2010)

[505] H. Wang, A. Hsu, J. Wu, K. Jing, and T. Palacios, "Graphene-Based Ambipolar RF Mixers," IEEE Elec. Dev. Lett. 31 (9), 906 (2010)

[506] C. Rutherglen and P. Burke, "Carbon Nanotube Radio," Nano Letters, 7 (11), 3296 (2007

[507] N. Rouhi, D. Jain, and P. J. Burke, "Nanoscale Devices for Large-Scale Applications," IEEE Microwave Mag. 11 (7), 72 (2010)

[508] D. Schinke, N. DiSpigna, M. Shiveshwarkar, P. Franzon, "Computing with Novel Floating-Gate Devices," in IEEE Computer, Vol. 44, No. 2, pp. 29-36.

[509] R.F. Freitas, W.W. Wilcke, "Storage-class memory: The next storage system technology," IBM. J. Res. & Dev. Vol. 52, No. 4/5, July/September 2008, pp. 439-447.

[510] [3] P . Ranganathan, "From Micro-processors to Nanostores: Rethinking Data-Centric Systems", in IEEE Design and Test of Computers, Jan. 2011, pp. 39-48.

[511] R.F. Freitas, W.W. Wilcke, "Storage-class memory: The next storage system technology," IBM. J. Res. & Dev. Vol. 52, No. 4/5, July/September 2008, pp. 439-447.

[512] P . Ranganathan, "From Micro-processors to Nanostores: Rethinking Data-Centric Systems", in IEEE Design and Test of Computers, Jan. 2011, pp. 39-48.

[513] P . Ranganathan, "From Micro-processors to Nanostores: Rethinking Data-Centric Systems", in IEEE Design and Test of Computers, Jan. 2011, pp. 39-48.

[514] R.F. Freitas, W.W. Wilcke, "Storage-class memory: The next storage system technology," IBM. J. Res. & Dev. Vol. 52, No. 4/5, July/September 2008, pp. 439-447.

[515] "Final Report, Exascale Study Group: Technology Challenges in Advanced Exascale Systems" (DARPA), 2007.

[516] L.A. Barroso, and U. Holzle, "The case for Energy-Proportional Computing," *in IEEE Computer*, Vo. 40, No. 12, Dec. 2007, pp. 33-37.

[517] G. Burr, "Storage Class Memory," in CMOS – Emerging Technologies Conference, May 2011. www.cmoset.com

[518] P . Ranganathan, "From Micro-processors to Nanostores: Rethinking Data-Centric Systems", in IEEE Design and Test of Computers, Jan. 2011, pp. 39-48.

[519] H. Lee, "High-Performance NAND and PRAM Hybrid Storage Design for Consumer Electronics", IEEE *Trans.Consumer Electronics, Vol. 56, No. 1, Feb. 2010, pp. 112-118.*

[520] T.M. Coughlin, "New Storage Hierarchy for Consumer Computers," in Proc. 2011 IEEE International Conference on Consumer Electronics, pp. 483-484.

[521] C. Dong, D. Chen, S. Tanachutiwat, and W. Wang, "Performance and Power Evaluation of a 3D CMOS/Nanomaterial Reconfigurable Architecture, "in Proc. ICCAD 2007, pp. 758-764.

[522] S. Paul, S. Chatterjee, S. Mukhopadhyay, and S. Bhunia, "Nanoscale Reconfigurable Computing Using Non-Volatile 2-D STTRAM," in Proc. 2009 IEEE Nano.pp. 880.

[523] C. Dong, D. Chen, S. Tanachutiwat, and W. Wang, "Performance and Power Evaluation of a 3D CMOS/Nanomaterial Reconfigurable Architecture,"in Proc. ICCAD 2007, pp. 758-764.

[524] ITRS 2007 Edition, Emerging Research Devices, Chapter: Emerging Research Architectures, Section: Morphic Computational Architecture

[525] C. Mead, Analog VLSI and Neural System, Addison-Wesley, 1989

[526] http://siliconretina.ini.uzh.ch/wiki/index.php

[527] http://www.facepunch.com/threads/1105228-DARPA-Synapse-phase-2-targets-integrated-neuromorphic-chip

[528] ITRS 2009 Edition, Emerging Research Devices, Chapter: Emerging Research Architectures, Section: Inference Computing

[529] http://arstechnica.com/hardware/news/2010/08/probabilistic-processors-possibly-potent.ars

[530] http://en.wikipedia.org/wiki/Belousov–Zhabotinsky_reaction

[531] K.K. Likharev, "Hybrid CMOS/nanoelectronic circuits: opportunities and challenges," J. Nanoelectronics and Optelectronics, 3(3), 2008, pp. 203-230.

[532] V. Zhirnov, R. Cavin, G. Leeming, K. Galatsis, "An Assessment of Integrated Digital Cellular Automata Architectures", IEEE Computer 41(1), 2008, pp. 38-44.

[533] L. Durbeck and N. Macias, "The Cell Matrix: An Architecture for Nanocomputing", Nanotechnology, 12(3), 2001, pp. 217-230.

[534] F. Peper, J. Lee, F. Abo, T. Isokawa, S. Adachi, N. Matsui, S. Mashiko, "Fault-Tolerance in Nanocomputers: a Cellular Array Approach", IEEE Trans. Nanotechnology, 3(1), 2004, pp. 187-201.

[535] J. Lee and F. Peper, "On Brownian Cellular Automata", Proc. Automata 2008, pp. 278-291.

[536] K. Preston, M.J.B. Duff, S. Levialdi, P.E. Norgren, J.-I. Toriwaki, "Basics of Cellular Logic with Some Applications in Medical Image Processing", Proc. IEEE, 67(5), 1979, pp. 826-856.

[537] T. Sunayama, M. Ikebe, T. Asai, Y. Amemiya, "Cellular vMOS Circuits Performing Edge Detection with Difference-of-Gaussian Filters", Jpn. J. Appl. Phys., Part 1, 39(4B), 2000, pp. 2278-2286.

[538] T. Asai, T. Sunayama, Y. Amemiya, M. Ikebe, "A vMOS Vision Chip Based on Cellular-Automaton Processing", Jpn. J. Appl. Phys., Part 1, 40(4B), 2001, pp. 2585-2592.

[539] V.H. Mankar, T.S. Das, S.K. Sarkar, "Cellular Automata Based Robust Watermarking Architecture towards the VLSI Realization", Proc. World Acad. of Sc., Eng., and Techn., 25, 2007, pp. 20-29.

[540] J. Shin, S. Yoon, D.S. Park, "Contents-based digital image protection using 2-D cellular automata transforms", IEICE Electronics Express, 7(11), 2010, pp. 772-778.

[541] M. Motomura, H. Yamada, T. Enomoto, "A 2K-Word Dictionary Search Processor (DISP) LSI with an Approximate Word Search Capability", IEEE J. Solid-State Circuits, 27(6), 1992, pp. 883-891.

[542] K. Wasaki, "Self-Stabilizing Model of a Memory Controller based on the Cellular Automata", Int. J. Comp. Sc. and Netw. Security, 8(3), 2008, pp. 222-227.

[543] P.D. Hortensius, R.D. McLeod, W. Pries, D.M. Miller, H.C. Card, "Cellular Automata-Based Pseudorandom Number Generators for Built-In Self-Test", IEEE Trans. Comp. Designs, 8(8), 1989, pp. 842-859.

[544] P. Dasgupta, S. Chattopadhyay, P.P. Chaudhuri, I. Sengupta, "Cellular Automata-Based Recursive Pseudoexhaustive Test Pattern Generator", IEEE Trans. Comp., 50(2), 2001, pp. 177-185.

[545] N. Ganguly, B.K. Sikdar, A. Deutsch, G. Canright, P.P. Chaudhuri, "A Survey on Cellular Automata", Technical Report, Centre for High Performance Computing, Dresden University of Technology, Dec. 2003.

[546] A.J. Heinrich, C.P. Lutz, J.A. Gupta, D.M. Eigler, "Molecule Cascades", Science, 298(5597), 2002, pp. 1381-1387.

[547] A. Bandyopadhyay, R. Pati, S. Sahu, F. Peper, D. Fujita, "Massively Parallel Computing on an Organic Molecular Layer", Nature Physics, 6(5), 2010, pp. 369-375.

[548] A. Destexhe and D. Contreras, "Neuronal Computations with Stochastic Network States", Science, 314(5796), 2006, pp. 85-90.

[549] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, G. I. Bourianoff, "Limits to Binary Logic Scaling – A Gedankin Model", Proc. IEEE, November 2003.

[550]] K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches", Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, Volume 98, Issue 12, Dec 2010, pp. 2169-2184.

[551] Keyes, R.W, "The evolution of digital electronics towards VLSI," IEEE Transactions on Electron Devices, Volume 26, Issue 4, Apr 1979 Page(s):271 – 279.

[552] Doug Matzke, "Will Physical Scalability Sabotage Performance Gains"? IEEE Computer, Volume 30, Issue 9, September, 1997, Page: 37 – 39.

[553] J. Welser and K. Bernstein, "Challenges for Post-CMOS Devices & Architectures," IEEE Device Research Conference Technical Digest, Santa Barbara, CA, Jun 2011, pp. 183-186.

[554] K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches,", Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, Volume 98, Issue 12, Dec 2010, pp. 2169-2184.

[555] T. N. Theis and P. M. Solomon, "In Quest of the 'Next Switch': Prospects for Greatly Reduced Power Dissipation in a Successor to the Silicon Field-Effect Transistor," Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, Volume 98, Issue 12, Dec 2010, pp. 2005-2014.

[556] K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches," Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, Volume 98, Issue 12, Dec 2010, pp. 2169-2184.

[557] J. Welser and K. Bernstein, "Challenges for Post-CMOS Devices & Architectures," IEEE Device Research Conference Technical Digest, Santa Barbara, CA, Jun 2011, pp. 183-186.

[558] K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches," Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, Volume 98, Issue 12, Dec 2010, pp. 2169-2184.

[559] I. Sutherland et al., Logical Effort: Design Fast CMOS Circuits, 1st ed. San Mateo, CA: Morgan Kaufmann, Feb. 1999, ISBN: 10:1558605576

[560] George Bourianoff, et.al., "Boolean Logic and Alternative Information-Processing Devices," Computer, May 2008, pp. 38-46

[561]An extremely valuable collection of different approaches to post-CMOS technology can be found in Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing, ed. G. Bourianoff, M. Brillouët, R. K. Cavin, III, T. Hiramoto, J. A. Hutchby, A. M. Ionescu, and K. Uchida, Volume 98, Issue 12, Dec 2010.

[562] A. Rusu, G. A. Salvatore, D. Jiménez, A. M. Ionescu, "Metal-Ferroelectric-Metal- Oxide-Semiconductor Field Effect Transistor with Sub-60mV/decade Subthreshold Swing and Internal Voltage Amplification", IEDM 2010 , San Francisco, USA, 06-08 December 2010.

[563] Asif Islam Khan, Debanjan Bhowmik, Pu Yu, Sung Joo Kim, Xiaoqing Pan, Ramamoorthy Ramesh, Sayeef Salahuddin,"Experimental Evidence of Ferroelectric Negative Capacitance in Nanoscale Heterostructures," arXiv:1103.4419,2011.

[564] T. Sakamoto, N. Iguchi and M. Aono, 'Nonvolatile triode switch using electrochemical reaction in copper sulfide', Appl. Phys. Lett., **96** (2010) 252104.

[565] T. Hasegawa, Y. Itoh, H. Tanaka, T. Hino, T. Tsuruoka, K. Terabe, H. Miyazaki, K. Tsukagoshi, T. Ogawa, S. Yamaguchi and M. Aono, 'Volatile/Nonvolatile Dual-Functional Atom Transistor', APEX, **4** (2011) 015204.

[566]I. Valov, R. Waser, J. R. Jameson and M. N. Kozicki, 'Electrochemical metallization memories-fundamentals, applications, prospects', Nanotechnol., **22** (2011) 254003.

[567] C. Zhou, D. M. Newns, J. A. Misewich and P. C. Pattnaik, Appl Phys Lett **70** (5), 598-600 (1997)

[568] D. M. Newns, J. A. Misewich, C. C. Tsuei, A. Gupta, B. A. Scott and A. Schrott, Appl Phys Lett **73** (6), 780-782 (1998)

[569] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[570] A.M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M.J. Declercq, P. Renaud, C. Hibert, P. Fluckiger, G.A. Racine, "Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal-over-gate architecture," Proc. of International Symposium on Quality Electronic Design, ISQED 2002, pp. 496 – 501

[571] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[572]S. Fujita, K. Nomura, K. Abe, T. H. Lee, "3-D nanoarchitectures with carbon nanotube mechanical switches for future on-chip network beyond CMOS architecture," IEEE Trans. Circ. and Syst. I, 54(11), pp. 2472-2479, 2007.

[573]W. Y. Choi, H. Kam, D. Lee, J. Lai, T.-J. King Liu, "Compact Nano-Electro-Mechanical non-volatile memory (NEMory) for 3D integration," IEEE International Electron Devices Meeting Technical Digest, pp. 603 - 606, 2007.

[574]K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.–S. P. Wong, "Design considerations for complementary nanoelectromechanical logic gates," IEEE International Electron Devices Meeting Technical Digest, pp. 299-302, 2007.

[575] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): A proposed new logic device," IEEE Electron Device Lett. **30**, 158-160 (2009).

[576] H. Min, R. Bistritzer, J.-J. Su, and A. H. MacDonald, "Room temperature superfluidity in graphene bilayers," Phys. Rev. B **78**, article no. 121401 (2008).

[577] http://www.src.org/program/nri/