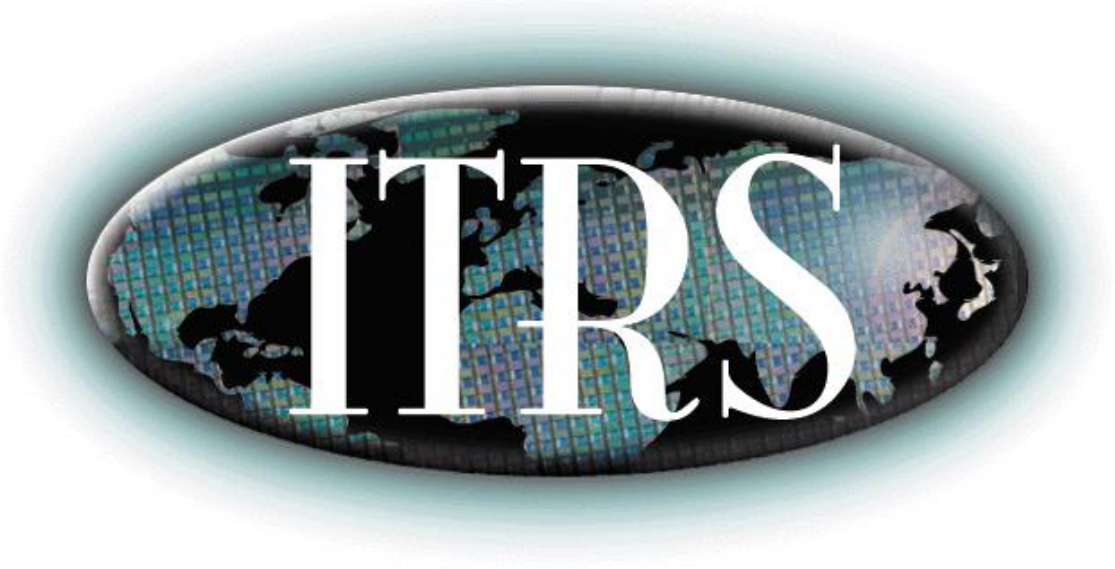

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

EMERGING RESEARCH MATERIALS

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TABLE OF CONTENTS

Emerging Research Materials 1

1. Scope 1
2. Difficult Challenges 1
3. Introduction 3
4. Emerging Research Device Materials 3
   - 4.1. Emerging Memory Materials 3
   - 4.2. Emerging Logic Materials 6
   - 4.3. Spin Materials 15
   - 4.4. Complex Metal Oxide Materials, Interfaces, and Superlattices 18
5. Lithography Materials 20
   - 5.1. Resist Materials 20
   - 5.2. Directed Self Assembly for Lithgraphy Extension 24
6. Emerging Front End Processes' and Process Integration, Devices, and Structures' Material Challenges and Options 27
   - 6.1. Doping and Deposition 27
   - 6.2. Directed Self Assembly of Useful Nanomaterials (See the Lithography Section Discussion) 29
   - 6.3. Selective Etch and Clean/Surface Preparation 29
   - 6.4. Low Damage Dopant Processing 30
   - 6.5. Contacts 30
7. Interconnects 30
   - 7.1. Novel Ultrathin Barriers 30
   - 7.2. Novel Interconnects 31
   - 7.3. Low K Interlevel Dielectric 33
8. Assembly and Packaging 33
   - 8.1. Materials for 3D Interconnects 34
   - 8.2. Polymer Materials for Future Packaging 35
   - 8.3. Low Dimensional Materials for Future Packaging 36
9. Environment, Safety, and Health 38
10. Metrology 38
    - 10.1. Characterization and Imaging of Nano-scale Structures and Composition 39
    - 10.2. Metrology Needs for Interfaces and Embedded Nano-structures [1,2] 39

    Characterization of Vacancies and Defects in Nano-scale Structures [3] 39
    - 10.3. Wafer Level Mapping of Properties of Nano-scale ERM [2, 5-8] 39
    - 10.4. Metrology Needs for Simultaneous Spin and Electrical Measurements [10-15] 40
    - 10.5. Metrology Needs for Complex Metal Oxide Systems [19-24] 40
    - 10.6. Metrology for Molecular Devices 41
    - 10.7. Metrology Needs for Macromolecular Materials [28-36] 41
    - 10.8. Metrology Needs for Directed Self-assembly [37-44] 41
    - 10.9. Modeling and Analysis of Probe-Sample Interactions 41
    - 10.10. Metrology Needs for Ultra-scaled Devices [45-48] 41
    - 10.11. Metrology for ERM Environmental Safety and Health 42
    - 10.12. Progress of Metrology for ERM Device Materials 42
    - 10.13. Low-K/Cu Interconnect Metrology 43
11. Modeling and Simulation 44
    - 11.1. Synthesis 46
    - 11.2. Structure and Properties 46
    - 11.3. Development of Platform for Different Simulation Tools, Such as TCAD and Ab-Initio 48

11.4. Metrology and Characterization 48
12. ERM Transition Table 49
13. References 50

LIST OF FIGURES

Figure ERM1 Polymer Composite Materials' Coupling Example 36
Figure ERM2 Modeling from Synthesis to Predicting Properties 44
Figure ERM3 Multi-scale Perspective in Nanotechnology where Materials Form an Important Role at Different Levels. 45

LIST OF TABLES

Table ERM1 Emerging Research Materials Difficult Challenges 2
Table ERM2 Applications of Emerging Research Materials 3
Table ERM3 ERM Memory Material Challenges 4
Table ERM4 Challenges for ERM in Alternate Channel Applications 7
Table ERM5 Alternate Channel Materials Critical Assessment 12
Table ERM6 Spin Devices versus Materials 14
Table ERM7 Spin Material Properties 15
Table ERM8 Challenges for Lithography Materials 20
Table ERM9 Directed Self Assembly Critical Assessment 27
Table ERM10 FEP / PIDS Challenges for Deterministic Processing 27
Table ERM11 Interconnect Material Challenges 30
Table ERM12 Nanomaterial Interconnect Material Properties 30
Table ERM13 Assembly and Packaging ERM Challenges 34
Table ERM14 ITWG Earliest Potential ERM Insertion Opportunity Matrix 38
Table ERM15 Transition Table for Emerging Research Materials 49

EMERGING RESEARCH MATERIALS

1. SCOPE

This chapter provides the material research community with guidance on specific research challenges that must be addressed in a laboratory setting for an emerging family of candidate materials to warrant consideration as a viable ITRS solution. Each international technology working group (ITWG) has identified applications that need new materials with significantly improved properties to meet future technology requirements, enable increased density of devices, and increase energy efficiency for computing and reliablity. Based on these requirements, the ERM has identified emerging materials that have properties that could potentially meet their needs for improved density, energy efficiency, and reliability. Materials that could potentially provide solutions for these requirements include III-V compounds, Ge, low dimensional materials (carbon nanotubes (CNTs), nanowires, graphitic systems, and nanoparticles), macromolecules, self-directed assembled materials, spin materials, complex metal oxides, and selected interfaces. For these emerging materials, this chapter presents requirements for materials, processes, interfaces, and supporting metrology, modeling, and simulation. In the 2011 ERM, we include critical assessments of alternate channel materials for CMOS extension and directed self-assembly for lithography extension.

The scope of emerging research materials (ERM) covers materials properties, synthetic methods, metrology, and modeling required to support future emerging research devices (ERD), lithography, front end process (FEP), interconnects, and assembly and package (A&P) needs. For ERD memory and logic devices, the scope includes planar p-III-V, n-Ge, nanowires, carbon nanotubes, graphene and graphitic materials, spin materials, and complex metal oxides. Furthermore, the special assessment of beyond CMOS logic identified that carbon based (carbon nanotubes and graphene) materials and devices receive increased focus, so a potential solutions table is included. A special assessment of emerging memory devices indicated that STT RAM and Redox RAM were promising, but needed special focus to accelerate progress, so a more detailed identification of materials and interface research needs is included. Some of the evolutionary and some of the revolutionary ERD can be fabricated with conventional materials and process technologies that are already covered in other sections of the ITRS, so the ERM chapter will not cover these materials and processes. Emerging lithographic materials include novel molecules, macromoloecules, and mechanisms that exhibit the potential to enable ultimate feature patterning with resist, or directed self assembling technologies. FEP materials include ERM required for future device technologies including technologies to place dopants in predetermined locations (deterministic doping) with low damage to the semiconductor material as well as novel materials to support selective etch, deposition, and cleaning of future technologies. Interconnect materials include emerging materials for extending Cu interconnects (novel ultrathin barriers), novel low resistance sub-20 nm electrical contacts, interconnects, vias, and ultra-low κ inter level dielectrics (ILD). Assembly and Packaging materials include novel materials to enable reliable electrical and thermal interconnects, polymers with unique and potentially useful combinations of electrical, thermal, and mechanical properties, and ultra-high power density high speed capacitors.

Due to their maturity, the ERM has transitioned n-InGaAs and p-Ge to FEP and PIDS and added p-III-V and n-Ge to the ERM chapter. Furthermore, the ERM is transitioning Zr and Ru ultrathin barrier layers to the Interconnect TWG.

This year's ERM chapter includes the following material families: p-III-V and n-Ge materials, low dimensional materials, macromolecules, self assembly mechanisms and self-assembled materials, spin materials, interfaces, complex metal oxides, and heterointerfaces. Many of these materials exhibit potential to enable higher density integrated circuits with higher energy efficiency and reliability in multiple application areas. Table ERM2 in the Introduction section maps families of ERMs to potential applications identified by the above Focus ITWGs. Future editions of this chapter also will comprehend and evolve projected ERM requirements for targeted functional diversification related applications.

2. DIFFICULT CHALLENGES

The Difficult Challenges for Emerging Research Materials is summarized in Table ERM1. Perhaps ERM's most difficult challenge is to deliver material options, with controlled and desired properties, in time to impact insertion decisions. These material options must demonstrate the potential to enable high density emerging research devices, lithographic technologies, interconnect fabrication and operation at the nanometer scale, and packaging options. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted

material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

Table ERM1 Emerging Research Materials Difficult Challenges

Difficult Challenges – 2018– 2026	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile, and non-volatile memory technologies to replace SRAM and / or FLASH for manufacture by 2018.	SRAM and FLASH scaling in 2D will reach definite limits within the next several years (see PIDS Difficult Challenges). These limits are driving the need for new memory technologies to replace SRAM and possibly FLASH memories by 2018. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond 2018 - 2026	Develop 2nd generation new materials to replace silicon (or InGaAs, Ge) as an alternate channel and source/drain to increase the saturation velocity and to further reduce Vdd and power dissipation in MOSFETs while minimizing leakage currents for technology scaled to 2018 and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in this development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A new information processing technology must also be compatible with a systems architecture that can fully utilize the new device. A new non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for a new systems architecture. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials Reliability issues should be identified & addressed early in the technology development
Invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless/analog and eventually in power devices, MEMS, image sensors, etc.	The industry is now faced with the increasing importance of a new trend, "More than Moore" (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled directions, dimensions, and compositions. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. For novel nanometer scale materials emerging within the research environment, methodologies and data also must be developed that enable the hierarchical assessment of the potential environment, safety, and health impact of new nanomaterials and nanostructures.

The difficult challenges listed in Table ERM1 may limit the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of

significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and nanostructure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish quantitative relationships between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the design and optimization of the required materials properties. The need for validated models requires strong alignment between experimentalists and theorists when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

3. INTRODUCTION

The Emerging Research Materials chapter identifies materials to support other technology work groups that could enable continued scaling of integrated circuits with improved energy efficiency for applications where no solutions are known. Many of the ERM material classes, with novel properties, may be applied to solving applications in multiple areas and this is highlighted in Table ERM2.

Table ERM2 Applications of Emerging Research Materials

To support ERD logic devices, the ERM is evaluating a number of alternate channel materials and structures that have the potential to enable smaller devices with less carrier scattering and thus higher energy efficiency. In 2008, the ERD identified that carbon based devices had a high potential for increasing information processing efficiency and also may be extendable to beyond CMOS device applications, so the ERM has highlighted research needed to accelerate progress on these materials. For beyond CMOS devices, the ERM is exploring materials that could enable information processing with state variables other than charge, such as spin, and that could potentially enable dramatic increases in energy efficiency of information processing and extend it many generations. For ERD Memory devices, the ERM is evaluating materials that could enable higher density memory with improved energy efficiency to change the memory state or read the memory state. In 2010, the ERD identified that STT RAM and Redox RAM had high potential as future high density memory technologies that needed further research to accelerate progress, so the ERM has identified critical research to support advances in these technologies.

For Lithography, the ERM is reviewing the viability of a number of novel photoresist to extend 193nm lithography and support EUV resist. The ERM is also performing a critical assessment of directed self assembly (DSA) to potentially extend lithography though pattern density multiplication. For FEP, the ERM is evaluating DSA and other novel concepts to control dopant positioning and reduce ion implant damage, which could improve device operation and improve energy efficiency. To support the Interconnect TWG, the ERM is evaluating novel materials to extend copper interconnects that reduce energy losses and signal delays. In addition, the ERM is exploring carbon (carbon nanotubes and graphene) based electrical interconnects to potentially dramatically reduce electrical resistance and improve energy efficiency of computing. For Assembly and Packaging, the ERM is exploring materials to modify polymer properties to enable increased product reliability, and novel electrical attach materials to allow lower assembly temperatures and improved product reliability.

For the ERM to be successfully improved in research and prepared for applications, the environmental safety and health properties of the materials must be understood and available, and metrology and modeling are needed to improve and assess the ERM for the applications. Metrology is needed to characterize the structure and composition at the nanometer scale, and important physical properties whether exposed or embedded in a structure. Modeling is needed of synthesis to determine whether desired structures can be achieved and the properties of these structures modeled to determine how they will function in the application. The requirements for these are explained in more detail in their respective sections.

4. EMERGING RESEARCH DEVICE MATERIALS

The emerging research device materials are listed in the approximate order that they appear in the ERD chapter and are not listed in any order of priority.

4.1. EMERGING MEMORY MATERIALS

Emerging Research Memory Devices includes capacitive memories (Fe FET), and resistive memories including Fe resistance, nanoelectromechanical, Redox memories, Mott electronic effect, macromolecular, and molecular memories. The ERM used in these devices includes, carbon nanotubes, nanowires, complex metal oxides, transition metal oxides, magnetic materials as well as engineered interfaces between these materials. The potential advantages and challenges of

ERM for Memory Devices are summarized in Table ERM3. Since many of these devices use complex and transition metal oxides, a section will review challenges for these materials.

Table ERM3 ERM Memory Material Challenges

4.1.1. FERROELECTRIC MEMORY MATERIALS

Emerging Ferroelectric Memories includes the FeFET and the Ferroelectric polarization resistance RAM. The FeFET operates with two stable polarization states available in the ferroelectric film used as a gate oxide. The main issues in FeFETs for non volatile memories are the short retention time and charge traps at the Si-ferroelectric interface.[1] Insertion of a dielectric layer such as HfO_2 or Hf-Al-O between silicon and the ferroelectric has strongly improved the retention time. Ferroelectrics with a lower P_r are optimal, which is why $YMnO_3$ (P_r ~5.5 μC/cm^2) has been considered for such applications. However, recently promising results have been achieved with a Pt/$SrBi_2Ta_2O_9$/Hf-Al-O/Si structure.[2] Since the integration of these ferroelectric materials with dielectric layers is challenging, others have evaluated the integration of polymer ferroelectrics with carbon nanotubes[3] or graphene[4] and demonstrated retention times less than a month.

Ferroelectric polymers and oligomers, which show polarization reversal by 180 degree rotation of individual molecular chains with external bias application, are also promising for nonvolatile memory applications. Copolymers of vinylidene fluoride and trifluoroethylene (P(VDF/TrFE)) have been well studied for some decades. Recently, a 50-nm-thick P(VDF/TrFE) film sandwiched with thin films of a conductive polymer, polypyrrole-poly(stylene sulfonic) acid (Ppy-PSSH), showed the retention of more than 10^7 switching cycles and the low coercive field of 2.6 V [5]. The importance of these interface layers between metal electrodes and a ferroelectric polymer was suggested before by using poly(3,4-ethylenedioxythiophene):poly(stylene sulfonic) acid (PEDOT:PSS) as another conductive polymer, where ferroelectric properties were maintained even after the change of the P(VDF/TrFE) thickness from 210 to 65 nm [6]. These interface engineering will cause further developments in future organic ferroelectric devices.

Vinylidene fluoride oligomer thin films also revealed clear polarization reversal with a larger value of remanent polarization (13 μC/cm^2) compared to conventional ferroelectric polymers [7]. High crystallinity of oligomeric materials gives rise to this large polarization and can be another strategy for improving nonvolatile memory performance based on organic ferroelectrics.

Vertically-stacked ferroelectric capacitors with these VDF materials were demonstrated recently[8,9]. This device structure is quite promising for realizing high-density integration of nonvolatile ferroelectric memories with multilayered memory arrays.

As described in the ERD, in the FE polarization ReRAM, the polarization of the ferroelectric material changes the barrier height of an adjacent semiconductor interface which changes the tunneling resistance of the structure. Since this is a tunneling structure, the ferroelectric material must be as thin as possible which is limited to ~1nm thickness[10] which is challenging to control.

In both devices, the retention time needs to be significantly longer to be used as a nonvolatile memory.

4.1.2. NANOELECTROMECHANICAL MEMORY MATERIALS

As mentioned in the ERD, the carbon nanotubes and conventional materials that have been patterned and etched are being investigated for nanoelectromechanical memories. Suspended or free-end structures are caused to physically move, contacting and decontacting to bridge an electrical gap under the influence of an applied field. A number of challenges must be overcome for this to be viable including being able to fabricate these devices with a high density and optimize the design so the cantilever doesn't get stuck in one state. First of all, these devices are large and scaling to smaller dimensions increases the voltage required for switching. The switching times of these devices are 10-100 nsec., which may be difficult to reduce due to scaling challenges.

4.1.3. REDOX MEMORY MATERIALS

The category of "Redox RAM" encompasses a wide variety of MIM structures and materials connected by the fact that they share reduction/oxidation (redox) electrochemistry as an important component of their physical mechanism for changing the resistance state from high to low or the reverse [11-13]. These redox electrochemical mechanisms can operate in the bulk I-layer, along the filamentary conducting path in the I-layer, and/or at the I-layer/metal contact interfaces in the MIM structure. Until recently, this category (Redox RAM) was further divided into two subcategories, "Thermal Chemical Mechanism" (i.e. Fuse/antifuse) and "Nanoionic" (i.e. Valence Change Mechanism and Electrochemical).

The electric field control of the distribution of the oxygen vacancies has been demonstrated in a similar MIM structure, such as a Pt / TiOx / Pt stacking structure [14, 15]. The charged oxygen vacancy was regarded as a mobile dopant in the

oxide material and the electrical control of the vacancies used as the analog resistance change necessary to imitate the axon coupling in a synaptic junction, namely one of the important elements for constructing emerging research architecture.

All Redox RAM technologies consist of an insulating dielectric sandwiched between two metal electrodes, to form a Metal-Insulator-Metal (MIM) structure. Following fabrication, the first operation that is conducted in these devices is a "forming" process where a voltage is applied to form low resistance channels. After a low resistance channel is formed, a "RESET" operation is performed and the "channel" returns to a higher resistance state. The device can then be placed in the high conductance "SET" state by application of a field. As discussed in the ERD, competing electrochemical and thermochemical mechanisms are involved in the operation of these devices. These mechanisms may occur and compete with with each other to different degrees depending on the electrode metallurgy and the oxides used.

The electrodes can use ionic metals (i.e. Cu, Ag, etc.) that can diffuse through the dielectric at high fields or non-ionic metals that don't diffuse through the dielectric. The ionic metals typically diffuse through the dielectric under electric field and form a conductive path[16] in the "forming" process and the conductive path can be turned off by the application of a reverse electric field (bipolar). With non-ionic electrodes, the application of a high electric field is believed to cause high concentrations of vacancies that change the valence state of transition metals such as Ti or Ta[17]. This results in the formation of a conductive filament that is induced by a localized high concentration of vacancies. In these devices, switching is achieved by applying a high "unipolar" field which activates thermochemical and electrochemical mechanisms. If the switching electrode has a metal that interacts with oxygen, such as Ti or Ta, oxygen can be released from the electrode that could annihiliate vacancies in the vicinity of the electrode[17].

In the case of the ionic metal electrodes, there is experimental evidence that multiple metal filament segments are formed from the cationic (inert) electrode to the anionic (oxidizable) electrode, but it is not clear that a totally continuous filament is formed. In the case of both electrodes being inert, the metal does not migrate, but it is commonly believed that an oxygen vacancy (Vo^{++}) rich path forms between the electrodes, and this induces a valence change of transition metals and this produces a low resistance path. In the case of TiO_2, the formation of Ti_4O_7 (Magneli phase) filaments has been reported [18]; however, this needs further study to determine whether the same mechanism would apply to materials grown in a wider range of conditions. To understand the scalability of these devices, it is important to characterize the spatial extent of the "filament" and determine whether this changes with memory cycling. It is also critical to understand whether one continuous filament connects the electrodes or whether multiple sub-filaments form a path with "communication" through dielectric gaps, since the switching mechanisms could be very different.

Metrology is needed to characterize and validate the switching mechanisms of devices in realistic materials (typically polycrystalline) that have grain boundaries and dislocations that could act as nucleation sites for formation of the conductive filaments in these materials. This metrology is needed to validate the "filment" formation mechanism and the switching mechanism in operating devices.

4.1.4. MOTT MEMORY MATERIALS

As mentioned in the Emerging Research Devices Memory Section, the Mott Transition (a metal-insulator transition driven by a gate induced change in carrier concentration) has been reported in a number of transition metal oxides and complex metal oxides. While this transition is proposed to be electronically driven by strongly correlated electron effects, several of these materials (e.g., VO_2[19]) or NSMO[20] also undergo a first order structural phase transition below 100°C. If the first order phase structural transition is required for this switching process, the material may need to be cooled below the transition temperature to restore the insulating state. Also, control of temperature for this device could be crucial to maintain the material close to the phase transition temperature; however, $SmNiO_3$ was recently reported to have this metal-insulator transition[21] with a structural transition at 130°C. Also, the properties of these materials are sensitive to oxygen vacancy concentration, strain, and other factors, so memories based on these materials may difficult to fabricate reproducibly.

Recent discoveries of 2D electron gases in complex metal oxide heterointerfaces[22] may open opportunities to couple ferroelectrics[23] with the 2DEG and produce a memory effect that is less sensitive to temperature.

4.1.5. MACROMOLECULAR MEMORY MATERIALS

As is discussed in ERD Memory Devices, macromolecular memory devices consist of a polymer with two electrodes and often other materials embedded in the structure (i.e. oxides on one electrode, metal or oxide nanoparticles, etc). While differences exist between the opertation of these structures, progress has been made in understanding the operation of the macromolecular memory with an oxide on one metal electrode. In this structure, the switching occurs in the oxide and the polymer acts as a current limiting element[24]. For oxide nanoparticles embedded in polymers, TiO2 and ZnO

nanoparticle films were switched between states with opposite polarity voltage pulses, while Al2O3, CeO2, ZrO2, and Y2O3 could be switched between states with unipolar or bipolar voltages. Based on this work, the switching involves changes in the state of the oxide nanoparticle[25]. Also, the state of the memory can be very sensitive to the presence of oxygen and UV light and this is hypothesized to be caused by interactions with the nanoparticle electronic states. Furthermore, repeated switching required a dead time of msec. These sensitivities potentially limit the usefulness of this memory to high performance applications.

4.1.6. MOLECULAR MEMORY MATERIALS

Molecular devices are described in the ERD chapter. Significant challenges must be overcome for them to be useful, including; fabrication of low potential barrier electrical contacts, reliable operation, the high resistance of molecules in their "on" state, and deposition of the top contacts that don't change molecular properties. Molecular state devices are reported to exhibit a range of useful properties, including non-linear IV and bi-stable behavior, but the electrical performance of many molecular-based devices currently under study appear to be dominated by the high potential barriers of each molecule-electrode contact or defect-like processes. Results suggest that changes in molecule-contact conformations or near neighbor interactions may be responsible for observations of electrical switching.[26, 27] Despite significant challenges and knowledge gaps, these emerging molecular systems show some promise for reducing device variability and enabling very high density circuit functionality.

Fabricating reliable molecular-scale devices requires identifying molecule/substrate contacts and top contact materials and deposition processes that produce high quality electrical contacts. Parameters ranging from the bond dipole to molecular orientation affect charge-transport parameters and switching voltages. Research is needed to elucidate the structural and electronic properties of molecule/substrate and top contacts, in order to engineer these contacts with reliable performance characteristics. Additional molecular modeling, synthetic, and experimental work, exploring the dependence of the metal work function on new molecular contacts, is needed.

4.2. EMERGING LOGIC MATERIALS

Emerging logic materials includes alternate channel materials to extend CMOS, materials for charge based Beyond CMOS devices, materials for non-charge based Beyond CMOS devices, and spin materials for multiple Beyond CMOS applications.

4.2.1. ALTERNATE CHANNEL MATERIALS

Emerging logic materials include alternate channel materials to extend CMOS to the end of the roadmap, materials to support charge based non-conventional FETs, and materials to support non-FET, non-charge-based Beyond CMOS devices. In some cases, materials and processes will be useful for multiple device types, so they will be discussed in detail for one application and differences highlighted for the other applications.

Alternate channel materials to silicon MOSFET's are being intensively explored, because increasing the performance and energy efficiency of integrated circuits by scaling silicon CMOS is becoming more difficult even with strained silicon channels. The principal property where performance can be enhanced is the channel mobility. The mobility for current silicon n-channels varies from 620 cm^2/V-s at low inversion carrier density (N_{inv}<1e12 cm^{-2}) to 250 cm2/V-s for N_{inv}=1.2e13 cm^{-2}. The mobility for current silicon p-channels varies similarly from about 150 cm^2/V-s to about 60 cm^2/V-s. Alternate channel materials with potentially higher mobilities are being explored to extend CMOS scaling with high performance and improved energy efficiency. The ITRS ERD and ERM are transitioning n-InGaAs and p-Ge to PIDS and FEP due to their performance and maturity; however, n-Ge and p-III-V materials will be evaluated in the ERD and ERM in addition to nanowires, carbon nanotubes, and graphene. The replacement of silicon channels by other semiconductors, such as III-V, Ge, graphene, carbon nanotubes, and semiconductor nanowires offers the possibility of reduced power consumption and enhanced performance for MOSFETs in future technologies. These benefits come from the higher field effect mobility of other semiconductors such as Ge for p-channels and III-V's for n-channels, graphene, carbon nanotubes, or nanowires. These carrier-transport enhanced channels can provide both higher on-currents, I_{on}, and lower gate capacitance at constant I_{on}. This combination can result in higher MOSFET performance at reduced power. To achieve complimentary MOS high performance, co-integration of different materials (i.e. III-V and Ge) on silicon may be necessary. Significant materials issues such as defect reduction, interface chemistry, metal contact resistivity, and process integration must be addressed before such improvements can be achieved.

The potential advantages and challenges of these nanostructured semiconductors are described in more detail in Table ERM4.

Table ERM4 Challenges for ERM in Alternate Channel Applications

Carbon based (CNT and graphene) devices have been identified as needing more focus to accelerate their potential use as alternate channel materials and for use in Beyond CMOS applications. The ERM and ERD chapters also identify when solutions are needed to overcome the difficult challenges that must be overcome for these materials to be viable in the required timeframe as is highlighted in Table ERM4.

4.2.1.1. *CARBON NANOTUBE FET MATERIALS*

The primary potential advantages for carbon nanotubes are their very high carrier mobility[28], and ultra-thin body but very difficult challenges must be overcome for them to be practical. Key challenges for carbon nanotubes to be viable in high performance FETs is the requirement for processes that provide a tight distribution of semiconductor bandgaps, with each nanotube placed in a desired location, with a specified direction, high adhesion to gate dielectric, low contact resistance, and catalyst compatible with CMOS. The advantages and challenges are highlighted in more detail in Table ERM4. Please refer to the 2009 ITRS ERD chapter for detail on these devices.

4.2.1.1.1. *NANOTUBE BANDGAP CONTROL*

Carbon nanotube FET-related applications are motivated by their high mobility and ballistic transport. [28] For SWCNTs to be viable for future CMOS applications, the ability to grow them with a tight bandgap distribution must be demonstrated. To achieve *in situ* bandgap distribution control, the diameter and chirality must be controlled in the growth process. Little progress has been reported in the past two years with the best results being (~95%) of semiconducting CNTs by CVD[29, 30, 31] Wet processing has achieved purities of 97%[32], with DNA purification purities approaching 99% have been achieved[33]. These levels of bandgap distribution control are far short of the projected requirements (better than parts per trillion). Considerable research is needed to develop understanding that will enable design of catalysts and processes for *in situ* growth of CNTs with sufficiently controlled bandgap distributions. Alternatively, a separation process is needed to improve purity of semiconducting CNTs to ppt level, and a cleaning process is also needed to remove dispersants attached to CNTs in the separation process. In addition, a methodology to evaluate a purity of semiconducting CNTs with a ppt-level precision should be developed. A viable technique to control bandgap of carbon nanotubes needs to emerge from research before 2014.

4.2.1.1.2. *CONTROL OF POSITION AND DIRECTION*

For CNTs to be used for devices, they must be placed in precise locations and aligned in required directions. Progress has been made in the past two years in growing nanotubes in desired locations with catalyst patterned on quartz to grow 20-50 aligned CNTs per micron.[34,35,36] Solution process has achieved ~20 per micron of aligned semiconductor-enriched CNTs[37] A potentially manufacturable process to control nanotube position and direction must be demonstrated in research before 2014 for this to be a viable technology.

4.2.1.1.3. *CONTROL OF CARRIER CONCENTRATION (NANOTUBE DOPING)*

A critical device challenge is carrier concentration control in embedded p-type and n-type materials. Typically, semiconducting CNTs tend to be p-type in ambient air. Little progress has been reported in the past two years in doping technology to control of carrier concentration. A CMOS compatible technique to control carrier polarity has been reported using charges incorporated in gate dielectric[38], but its controllability and reliability should be assessed. Techniques to control carrier concentration in channel and source/drain regions need to be demonstrated in research before 2014.

4.2.1.1.4. *GATE DIELECTRIC INTERFACE*

Since a CNT's sidewall is relatively inert, it is hard to deposit uniform ultra-thin film on them, but chemically functionalizing the surface may improve dielectric adhesion. Research and guiding material design principles are needed for enhancing functionalization, interface passivation, and dielectric deposition. Alternatively, some metals such as Y and Ti adhere to CNTs, and can be oxidized to form high-k dielectric. Uniform 5-nm Y_2O_3 has been realized on a CNT[39]; however, the interface quality and reliability should be determined. A viable technique to deposit a passivated high κ gate dielectric needs to emerge from research before 2014.

4.2.1.1.5. *CONTACT FORMATION*

Pd is the most commonly used contact material with resistance approaching the quantum contact resistance[40], but recently Sc-CNT [41] and Y-CNT contacts[42]have been employed to fabricate n-FETs. On the other hand, researchers have also reported high variability in contact resistance for small diameter nanotubes. A method to reduce Schottky barrier has been proposed by modulating potential in the vicinity of contact interface.[43] A recent important finding is the contact length dependence of contact resistance, suggesting carrier reflection at the contacts.[44] Further investigation is necessary to

understand the origin of these effects on contact resistance. A CMOS compatible, reproducible contact formation technique needs to emerge from research before 2014.

4.2.1.2. *GRAPHENE FET MATERIALS*

The primary advantage of these materials is their potentially high mobility (as seen in carbon nanotubes) and the ability to process in a planar form. The critical issues for graphene include the ability to:

1. Deposit graphene over large areas with controlled grain size, thickness, and orientation
2. Generate and control a bandgap in graphene
3. Reduce or control surface and interface effects on charge transport
4. Achieve a high mobility on a silicon compatible substrate
5. Deposit a high κ gate dielectric with a high quality passivated interface
6. Form reproducible low resistance contacts to graphene (contacting without etching through a monolayer film)
7. Integration, doping and compatibility with CMOS

As is identified in the ERD chapter, graphene should receive additional focus to accelerate progress for potential application as an alternate channel material and then for extension to Beyond CMOS applications.

4.2.1.2.1. *GRAPHENE DEPOSITION*

The preferred approach for deposition of graphene would be a CVD "like" process or epitaxial process on a silicon wafer; however other techniques could be used. Currently studied graphene deposition techniques include mechanical, chemical oxidation, or solvent exfoliation from highly oriented pyrolytic graphite (HOPG), direct CVD epitaxy on metal substrates, catalysed growth on silica or alumina, and sublimation of silicon from SiC. Emerging methods such as growth on polyethylene terephtalhate (PET) or polydimethylsiloxane (PDMS) which provide moreover underlying substrates that can be twisted or stretched (up to 11% without any conductivity loss) are also worth investigating. Obviously, physicochemical characterization of the graphene layers should be developed to determine thickness control and chemical purity of the layers. For graphene to be a viable technology, as CMOS compatible, potentially high volume deposition technique needs to emerge from research before 2014.

4.2.1.2.2. *FORMATION OF HIGH CRYSTALLINE QUALITY GRAPHENE MATERIALS*

Mechanical exfoliation of graphene has produced high quality films on silicon[45], but control of location and thickness may not be adequate for development of integrated circuit technologies. The decomposition of SiC[46] has the advantage that the graphene is grown on a silicon-like substrate, but it requires process temperatures of ~1200C or above. Epitaxial graphene on SiC has exhibited carrier mobilities as high as 15,000cm^2/V-s[47] and 250,000cm^2/Vs [48] at room temperature and liquid helium temperatures respectively.

Initial progress was made in growing CVD graphene on single crystal Ni[49], Ir[50,51], and Pt[51], but this would be very costly. Recently small areas of graphene has been grown by CVD on a polycrystalline Ni thin films[52,53], and patterned polycrystalline Ni films[54], but most recently large areas of graphene have been grown with CVD on Cu foil[55] with room temperature electron mobilities as high as 16,000$cm^2V^{-1}sec^{-1}$ [56]. While these graphene films are deposited on metals, transfer of these films has been demonstrated to SiO2/Si substrates where device structures have been fabricated and properties characterized[52,53,55, 56]. While these CVD techniques are not directly on a silicon compatible substrate, the use of polycrystalline substrates with thin film transfer may offer a more cost effective approach. On the other hand, transfer-free fabrication of graphene-channel transistors has recently been demonstrated [57,58]. More recently, a novel approach for wafer-scale transfer has been proposed [59]. This appears to be a fast developing area, so new work may quickly surpass these results.

An alternative approach for selectively growing graphene on desirable substrates is through the evaporation of silicon from silicon carbide.[46] This technique requires annealing the SiC in H2 ambient at 1200°C to effectively evaporate the silicon. Thickness control of several monolayers on a mm scale has been demonstrated, with room temperature field mobilities in excess of of 15,000 cm^2/V-s.[47,60] Recently, a technique has been demonstrated to deposit a thin layer of SiC on a silicon wafer and then "evaporate" the silicon leaving a thin layer of graphene several atomic layers thick.[61] One of the drawbacks of these approaches, however, is that the required high temperature processing may produce defects in 300mm or 450mm wafers.

Mechanical exfoliation of graphene from HOPG has produced the highest mobility graphene reported to date. A more detailed description of exfoliation techniques is included in the 2009 ITRS ERM Chapter.

4.2.1.2.3. *GRAPHENE MOBILITY*

The highest mobility of free-standing graphene at 240K is 120,000 $cm^2/V\text{-}s$[62], which was achieved by driving adsorbed molecules from the surface of the graphene, and it has been proposed that flexural phonons limit the room temperature mobility of free standing graphene. Mobility of 70,000 $cm^2/V\text{-}s$ has been achieved at room temperature by using dielectric screening with solvent dielectrics having a dielectric constant of 47.[63] Graphene sandwiched between h-BN crystals have shown mobilities of ~100,000 $cm^2/V\text{-}s$. For top gated graphene transistors with a high κ dielectic, mobilities as high as 8000 $cm^2/V\text{-}s$[64] have been reported.

4.2.1.2.4. *GENERATION OF A GRAPHEN BANDGAP*

Graphene has a zero bandgap but several techniques for generating a bandgap have been reported include fabricating graphene nanoribbons, apply a back gate bias to a bi-layer of graphene to open the bandgap, plasma O2 treatment of graphene[65], hydrogen surface treatment[66], and through interactions with substrates such as SiC[67], BN[68] or MgO[69] or superlattice substrate interaction structures on Ir[70]. Furthermore, modeling predicts that a bandgap can be induced in graphene by application of shear strain[71]. Electrically tunable bandgaps have been fabricated using dual gate structures and different dielectrics for each gate so that the bandgap and carrier concentrations can be independently varied by different top gate and bottom gate biasing.[72, 73] With graphene nanoribbons, the bandgap increases with decreasing width, which can be approximated as $Eg(eV)=0.8/w(nm)$[74]. A bandgap can also be produced by making periodic holes in graphene[75,76] where the "neck" between holes acts as a nanoribbon. The nanoribbons electronic properties will be sensitive to edge states[77-79], so passivation of edge states will be critical. Applying a back gate bias effectively separates the conduction and valence bands and enables an on-off ratio of 5-10X.[73] Another option is to design the structure with a built in field due to work function differences or fixed charges in the structure. A bandgap of ~2eV has been reported for graphene treated with O_2 plasma[65], and a patterned treatment with H_2 is reported to generate a bandgap of 330 meV[66]. Deposition of graphene on a SiC substrate produced a 0.26eV bandgap[67], BN substrate is reported to produce an 18meV bandgap[68], while deposition on MgO produced a bandgap of 0.5-1eV69. A viable technique to control bandgap needs to emerge from research before 2014.

Some applications, i.e. microwave FETs, don't require a bandgap, so device applications may emerge that don't require a bandgap.

4.2.1.2.5. *HIGH K GATE DIELECTRIC DEPOSITION*

Since the graphene surface is chemically unreactive high κ dielectric deposition is normally initiated at edges or defects in the film. This has been demonstrated with the deposition of HfO_2 and Al_2O_3 on graphene.[80] In order to deposit these films uniformly on graphene, a thin Al buffer layer was deposited and oxidized. This served as a nucleation layer for ALD Al_2O_3 on graphene which resulted in mobility above 6000 $cm^2/V\text{-}s$ at room temperature[81], an improvement over previously obtained results produced by surface functionalization of graphene. It was also demonstrated that a low-κ polymer worked as a buffer layer for high-κ dielectric deposition onto graphene with a resultant mobility of up to 7,600 $cm^2/V\text{-}s$[82]. A viable high-κ dielectric deposition technique needs to emerge from research before 2014.

4.2.1.2.6. *DOPANT INCORPORATION AND ACTIVATION*

If graphene is to be used for extreme CMOS applications, processing must be capable of doping the material p-type and n-type for the channel region and either metallic or n-type or p-type for the S/D region. To date, the proposed approaches for doping the channel regions are to 1) deposit the graphene on a surface that injects carriers into the graphene layer and 2) chemically bonding dopants at edge states of a graphene nanoribbon. Modeling has predicted that graphene could be controllably doped by charge transfer from a substrate layer or materials deposited onto the surface, and a number of experiments have demonstrated that n-type and p-type graphene can be fabricated through deposition of metals with different work functions. More recently, graphene nanoribbon edge states have been doped n-type through high temperature electrochemical ammonia treatment.[83] Experiments have demonstrated that n-type graphene can be produced through deposition of NH_3 and CH_4[84], while p-type graphene can be produced through deposition of H_2O and NO_2.[85] Experiments on graphene ribbons indicate that edges can convert to p-type, while the center of the ribbon is n-type.[86] More recently, n-doped graphene has been synthesized by using pyridine as the source gas[87,88] .

The challenge with these doping techniques will be to maintain the carrier doping in an integrated structure with interconnects. Since the S/D doping will be affected by the contact metallurgy, as will be covered in the contact formation section below. A viable technique to control doping and carrier concentration in graphene needs to emerge from research before 2014.

4.2.1.2.7. *CONTACT FORMATION*

The source-drain contacts need to provide a low resistance electrical contact to the graphene, but also maintain the graphene in the conductivity type that is needed for the n-channel or p-channel device. Ohmic contact formation may be easier than in small diameter carbon nanotubes, but more research is needed. There have been several studies regarding the contact resistance between electrodes and graphene channel [89-91]; however, the contact resistance obtained so far is not yet low enough for CMOS application. Clearly, more research is needed for this issue. A viable graphene contact formation technique needs be demonstrated in research before 2014.

4.2.1.3. *NANOWIRE FET MATERIALS*

Metal-catalyzed nanowires(NW) and patterned and etched(top down fabricated) NW have been suggested as the channels of MOSFETs. The top down fabrication of NW enables precise control of location and direction, which is an advantage over metal catalyzed growth of NW. The potential advantages of nanowires are 1) compatibility with gate-all-around structure that improves electrostatic control, 2) nonclassical physics at small dimensions. Furthermore, with nanowires it is possible to fabricate defect free lattice mismatched heterojunctions in the growth direction[92] and low defect density heterojunctions in the lateral direction[93], which could enable flexibility in device design. On the other hand, there are significant challenges to realizing these advantages with catalyst grown nanowires integrated into CMOS including identifying catalyst materials compatible with CMOS, control of placement, size and shape, direction, and doping. These are described in more detail in Table ERM4.

Non-classical quantum effects depend significantly on the Bohr radius and this varies widely between materials. The Bohr radius in Si is short, and bandgap changes have been observed to occur below 6nm[94], which could increase variations in Vt. Top down fabricated nanowires that have rectangular cross sections had higher mobility at low fields than those that had been annealed to round the edges of the structures[95]. The cause of this mobility degradation with the rounded edges was an increase in Dit[96] for the devices. The mobility in nanowires of selected compound semiconductor field-effect transistors can be much higher than that in corresponding Si nanowires, making nanowires of these alternative materials attractive. In addition, selected compound semiconductors, as well as Ge, have larger Bohr radii, so non-classical effects are more likely to be observed in nanowires of practical dimensions. The introduction of heterojunctions in FET structures may also be employed to improve device functionality.[97]

III-V nanowires offer the potential advantages of higher mobility, on-off current ratio, and subthreshold swing than can be achieved with conventional silicon circuitry. The ease with which the band structure can be engineered also opens the possibility for transistors that use two-dimensional electron gas conduction for even higher mobility than can be achieved in the homojunctions, or for devices based on tunneling through epitaxial barrier layers made from semiconductor layers with higher band gap. III-V nanowires with the best performance are generally grown with the same crystal growth methods that are used for epitaxial layer growth for other III-V devices, namely organometallic vapor phase epitaxy (OMVPE) and molecular beam epitaxy (MBE). Most of these nanowires are grown using catalysts[98] but non-catalytic methods have been identified as well.[99-102] In addition to the common issues with nanowires, III-V nanowires have the challenge of passivation of a compound semiconductor with multiple crystal orientations exposed.

Although horizontally grown NW have not made much progress in controlling direction, progress has been made in controlling location and direction of vertical NW. Furthermore, n-type doping in SiNW has been increased to 1.5E20cm^{-3} [103] and p-type doping has increased to 2E18cm^{-3} at growth temperatures of <500C. Furthermore, MOSFETs[104], Schottky Barrier FETs[105], IMOS[106] and Tunnel FETs[107] have been fabricated on grown nanowires.

Although nanowires have potential advantages as the channels of field-effect transistors, significant challenges must be overcome for them to be integrated in high density applications. Processing of dense arrays of laterally placed nanowires with surround gates and low resistance contacts may be challenging.

4.2.1.4. *P-III-V CHANNEL MATERIALS*

For n-channels, InGaAs quantum well FET's on silicon have been reported with mobilities of 10,000 to 3000 cm^2/V-s [108] using 1.2-micron buffer layers and for strained Ge quantum well p-channels, mobilities of 770 cm^2/V-s at 5e12 cm^{-2} [109] have been reported. The n-channel enhancement is a 30X improvement over Si channels and the p-channel mobility is a 2X improvement. These mobility increases over silicon channels are significant and would result in reduced power and higher drive currents if they could be successfully integrated in a CMOS FET process without degrading the mobilities. However process complexity and costs would be greatly reduced if the n-channels could be made from strained Ge and the p-channel made from strained InGaSb. Then the choice of complementary channel materials and processes could be based on either Ge or III-V alternate channels rather than both in the same process. This section describes progress being made on Ge n-channels and InGaSb p-channels in silicon MOSFET's. The n-channel InGaAs and p-channel Ge status may be found in the PIDS chapter of this ITRS.

p-channel III-V quantum wells: the hole mobilities of III-V materials are generally lower than Si with narrow bandgap materials such as the antimonides showing the highest values. Similar to electron mobility in Ge channels, the hole mobility in III-V channels is affected by the high density of interface traps in these materials near the valence band edge, while there are fewer traps near the conduction band edge so that there are more free electrons available for the n-channel. The challenge for raising the hole mobility is to address this issue. A hole mobility of 820 cm^2/V-s has been reported for InGaAs in a III-V heterostructure [110]. However there have been no reports of InGaAs p-channel mobilities that have been integrated onto Si. Also a mobility of 800 cm^2/V-s has been reported in p-channel InGaSb heterostructure wells [106], which are significantly better than previous p-channel mobilities for III-V semiconductors that have been in the range of 100 to 300 cm^2/V-s. [111,112,113,114]. The Table below summarizes the antimonide mobility work. However more work is needed on gate insulator and contact effects on mobility for p-channels of III-V materials on Si at short channel lengths.

Material	Structure	Channel Length	p-Type Mobility
In0.41Ga0.59Sb [113]	80nm thick QW with 2% strain HEMT	200nm	1500cm^2/V-sec
GaSb [112]	SL HEMT		1350cm^2/V-sec
GaSb[114]	Quantum Well	1000nm	850cm^2/V-sec

An important materials consideration for III-V channels is the possibility of strain-enhanced mobilities similar to that in Si and Si-Ge channels. Elastic strains arise from both thermal expansion and lattice parameter mismatches. Lower bandgap III-V semiconductors have lower critical resolved shear stresses for plastic deformation [115] so that elastic strains are difficult to sustain at temperatures in the 400-500C range. Nevertheless recent results have shown that compressive strains around 1% in GaSb heterostructures increased the hole mobility from 280 to 800-1300 cm^2/V-s (10) for growth temperatures from 400-500C. This suggests that similar improvements may be possible for the InGaAs system as well. Some hole mobility enhancement has been observed in strain-enhanced InGaAs MODFET structures [116]. However these enhancements would need to compensate for degradation due to the presence of interface traps near the valence band and thus require Fermi-level pinning dielectric layers (see PIDS section for details). In addition, reduction of film defects such as dislocations and antiphase domain boundaries will be required to enhance mobility.

4.2.1.5. *N-GE CHANNEL MATERIALS*

The Hall electron mobility of bulk Ge is significantly higher (3900 cm^2/V-s) than bulk Si (1600 cm^2/V-s) but degrades significantly in the n-channel of MOSFET's to 150 cm^2/V-s at N_{inv}=1.2e13 cm^{-2} whereas Si electron mobility is 250 cm^2/V-s at this N_{inv}. The main reason for this degradation in Ge n-channel mobility is the presence of high density of interface traps near the conduction band resulting from germanium oxide instability. Germanium oxide contains two valence states over a wide range of temperatures. The use of ozone (O_3) for oxidation has reduced the number of interface traps by forcing the oxide to be mostly tetravalent[117, 118]. In addition As and Sb implants [119] and reduction of source/drain parasitic resistance [120] has allowed the Ge –channel mobility to be increased to over 400 cm^2/V-s at Ni_{nv}=1.2e13 cm^2/V-s (1.5x universal Si) n-channel mobility. These results are extremely important in the quest to use Ge channels for both p- and n-MOSFET's. However the mobilities are still well below those for n-channel InGaAs mentioned above. The next challenges are to pursue strain enhancements of mobility and to explore interface trap physics for high-dielectric constant deposition on Ge channels to determine whether this and other integration and device structures will maintain this high value of n-channel mobility. Also the application of these findings to SiGe n-channels will need to be explored. As for III-V channels, it will be important to reduce dislocation densities during deposition and subsequent processing to achieve these mobility increases.

4.2.1.5.1. *CO-INTEGRATION OF III-V AND GE*

The integration of either III-V compounds or Ge with CMOS devices will be challenging, but if both are integrated on CMOS the challenges will be even more complex. These challenges include defect control, interface chemistry control, dopant incorporation and activation, and source/ drain formation with low resistance contacts.

4.2.1.5.2. *DOPANT INTEGRATION AND ACTIVATION*

Incorporation and activation of dopants in III-V materials can be achieved at low temperatures, but activation of dopants in Ge requires high process temperatures for n-type dopants.[121] Recent work using metal-induced dopant activation in Ge has shown that activation may be achieved as low as 380°C.[117] Thus, if Ge and III-V devices are fabricated on the same

substrate, these competing requirements may require the Ge devices to be fabricated prior to the growth of III-V materials, which may significantly increase the integration complexity.

4.2.1.5.3. *SOURCE/DRAIN FORMATION*

Incorporation and activation of dopants in III-V materials can be achieved at low temperatures, but activation of dopants in Ge requires high process temperatures for n-type dopants.[121] Recent work using metal-induced dopant activation in Ge has shown that activation may be achieved as low as 380°C.[122] Thus, if Ge and III-V devices are fabricated on the same substrate, these competing requirements may require the Ge devices to be fabricated prior to the growth of III-V materials, which may significantly increase the integration complexity.

4.2.1.6. *TUNNEL FET MATERIALS*

Tunnel FETs employ band to band tunneling to achieve sharper turn-on characteristics. They can be fabricated with conventional processing of the alternate channel materials discussed above, so new materials will not be required. A more detailed discussion on the Tunnel FET can be found in the ERD Logic Section.

4.2.1.7. *ALTERNATE CHANNEL CRITICAL ASSESSMENT*

The ERM and ERD have performed critical assessments of some of the same devices. The ERD assessment assumes that all of the integration and fabrication issues are resolved, while the ERM assesses the difficulty of resolving the materials, processing, and integration issues. This ERM survey is based on votes of whether an alternative should be better than CMOS (3), the same as CMOS (2) or worse than CMOS (1). In the ERM critical assessment, Table ERM5, all alternate channel materials were viewed to have potentially better mobility than silicon CMOS. From an integration perspective, Ge, and III-V were viewed as comparable to silicon with average scores of (2.0) and nanowires were close with a score of (1.9), while CNTs and graphene had averge scores of (1.5)As indicated in the table, entries that exceeded an average vote of 2.0 over the categories were viewed as being "easy' to integrate into CMOS (none of the options met this criteron). Entries that exceeded an average vote of above 1.7 were viewed that they should be possible to integrate onto CMOS with significant work, and Ge, III-V, and Nanowires met this criteron. Based on the voting, carbon nanotubes and graphene had more votes indicating that multiple technical issues didn't have potential solutions demonstrated and there are highlighted in red, so significant research is required to demonstrate potential solutions. Even though Ge, III-V, and nanowire materials were viewed more favorably, each had significant issues that must be addressed. For Ge and III-V materials, the biggest concern was the ability to grow defect free material on silicon and this is fundamental to integration of these materials. For nanowires, the voting indicated the biggest concern to be the ability to form low resistance contacts to the nanowires, but this should be soluble with additional focus and research. The technical challenges for all of these materials are described in more detail in the alternate channel section.

This critical assessment is based on voting by ten ITRS participants from the ERM, ERD, FEP and PIDS technology workgroups and will be updated in the ERM in future ERM revisions.

Table ERM5 Alternate Channel Materials Critical Assessment

4.2.2. CHARGE BASED BEYOND CMOS MATERIALS

4.2.2.1. *SPIN FET AND SPIN MOSFET MATERIALS*

The spin transistor includes both "Spin FET" and "Spin MOSFET" devices. Both devices have magnetic Source/Drain with a semiconducting channel and a MOS gate, materials used are described in Table ERM6. The channel of the spin FET is a material with high spin orbit coupling such as GaAs or other III-V compounds, while the channel region of the Spin MOSFET is a material with low spin orbit coupling. In both devices, the spin is injected from the ferromagnetic source, and then transported through the channel to the drain and electrons with spin aligned with the drain are passed and generate current. In the case of the Spin FET, the source and drain have the same spin alignment, the gate voltage couples to the spin through the spin-orbit coupling and changes the spin precession angle, and the drain accepts spins with the same alignment, so current is modulated. In the case of the spin MOSFET, the alignment of the drain magnetization is fixed, while that of the source can be changed, so the gate allows current to flow from the source to the drain without modulation. In these devices, the injection of spin is important and can be achieved through either a Schottky barrier or a tunnel barrier, and both of these materials are described in the (Spin Materials Section). The channel materials and gate dielectrics are described in the ERM Alternate Channel Section and the Spin Transport Materials Section while material options for the S/D are described in Ferromagnetic Materials Section. A more detailed description of these devices is found in the ERD chapter. A recent review of spin transistor highlights the concepts and challenges of these devices.[123]. Recent work has demonstrated successful electrical injection, detection and manipulation of spin accumulation in Si using

ferromagnetic metal / SiO2 tunnel barrier contacts at temperature to 500K, encouraging results for realization of Spin MOSFET operation at practical temperatures.[124]

4.2.2.2. *IMPACT IONIZATION MOS MATERIALS*

IMOS is a gated p-i-n structure where the gate overlaps the n+ region and intrinsic regions.[125] The gate modulates the breakdown of the n+/i junction and controls the impact ionization. Since this structure generates hot carriers, this may cause shifts in the threshold voltage as these hot carriers cause damage in the gate or buried oxide in the case of SOI. This would require either designing the device to keep hot carriers from being generated close to these oxides or developing oxides that are immune to hot carriers. These devices could be fabricated with planar Si, Ge, or III-V materials or nanowires which are described in the alternate channel materials section.

4.2.2.3. *NEMS SWITCH MATERIALS*

The materials for this device are discussed in the ERM Memory Materials Section

4.2.2.4. *ATOMIC SWITCH MATERIALS*

The atomic switch operates with oxidation /reduction processes where a metal atom moves to form a bridge between two different electrodes. The materials include a metal such as Cu and sulfur.[126] Research is needed to determine the mechanism and determine its potential reliability; however, the mechanisms appear to be similar to those in the Redox memory.

4.2.2.5. *MOTT FET MATERIALS*

The Mott FET is based on a metal insulator(MI) transition caused by the gate field inducing charge in the Mott insulator, as described in the ERD Logic section. This has been observed in a VO_2[19]; however, material also undergoes a first order structural phase transition at 68C to a metallic state. Recently, $SmNiO_3$ has been reported to have a MI transition temperature of 130C. [21] For the switching to be electrically reversible, the temperature must be maintained below 68C, or the material must be cooled to lower temperature to restore the insulating phase. The MI transition has also been identified in a FET made of an organic Mott insulator at low temperature. [127] Other materials, heterointerfaces and superlattices of complex metal oxides and strongly correlated electron state materials should be investigated to identify materials that undergo the Mott transition without the structural phase being in the operating temperature range. Complex metal oxides and strongly correlated electron state materials will be discussed later in the chapter.

4.2.2.6. *FERROELECTRIC NEGATIVE CG MATERIALS*

Ferroelectric oxides have been proposed as a gate oxide in field effect transistor for steep substhreshold slope (SS)[128,129] . In a conventional FET, the intrinsic limit for the SS is of 60mV/dec at room temperature, which puts a fundamental lower limit on the operating voltage and thus the power dissipation. For future generation of switches, low voltage operations will be of utmost importance [130,131]. In the Salahuddin and Datta's proposal, the replacement of the dielectric by a suitable thickness of a FE material should lead to a large increase of the capacitance thanks to the negative capacitance contribution of the ferroelectric (ideally the negative capacitance of the FE compensates exactly the positive capacitance of the stack). As a consequence, the drain current increases sharply under low voltage. The negative capacitance effect has been quantified in a recent paper for $SrBi_2Ta_2O_9$ as a ferroelectric gate oxide [132]: a reduction by ~150 mV of the operating voltage is predicted.

Experimentally, the first evidence of a SS smaller than 60 mV/dec has been obtained on a metal-ferroelectric-metal-oxide gate stack using a ferroelectric polymer (P(VDF-TrFE))[133]. Minimum SS values of 46-58 mV/dec are reported for the FE polymer; however, no evidence of such steep SS has been so far demonstrated using a ferroelectric oxide.

Numerous questions remain to be addressed such as the suitability of the switching speed of the ferroelectric oxide for such devices and the effect of domains on the transistor response. Moreover, the integration of complex oxides directly on silicon is still very challenging[134].

4.2.3. NON-CHARGED BASED DEVICE MATERIALS

4.2.3.1. *SPIN WAVE DEVICE MATERIALS*

The key challenges in building a practical spin wave logic circuit are the efficient injection, detection, and modulation of spin waves in the wave guide. For this to be a viable option, efficient spin wave generators and modulators need to be integrated onto the spin wave guides, which requires an optimized interface between materials. At present, research on magnetic modulators is based on spin valves/magnetic tunnel junctions or multiferroic materials.[135, 136] This section will

discuss material properties required for fabricating an efficient spin wave guide and spin wave modulator, based on multiferroics. The materials used in spin wave devices are described in Table ERM6.

Table ERM6 Spin Devices versus Materials

The fundamental physical property required for fabricating an optimized spin wave guide is to have high saturation magnetization (~10 KG), low Coercive field (tens of Oersteds), and long attenuation time (at least 0.5 ns). Currently, the most popular materials used for a spin wave bus are soft ferromagnetic metallic conducting films, such NiFe, CoFe, CoTaZr that are sputter deposited. These ferromagnetic metals possess high saturation magnetization (about 10kG) and Curie temperatures much higher than room temperature (Ni 627K, Fe 1043K, Co 1388K). Another advantage of using these materials are their compatibility with the silicon platform. Prototype spin wave devices are also fabricated using ferrite materials, such as Yttrium Iron Garnet (YIG). However, achieving nanometer thick and uniformly dense ferrite materials on silicon substrate is a challenge.

There are theoretical models demonstrating how to integrate a multiferroic structure onto a spin wave guide[136], but this integration has yet to be experimentally demonstrated. There are two major requirements for multiferroic materials: (i) Prominent magnetoelectric coupling (in V/cm Oe), and (ii) a fast switching time. Conducting and insulating materials are applicable to the spin wave based logic devices. They may be single phase multiferroics (e.g. $BiFeO_3$ 7 mV cm^{-1} Oe^{-1}) or composite (two phase) multiferroics comprising piezoelectric and ferromagnetic materials (e.g. PZT/$NiFe_2O_4$ (1,400 mV cm^{-1} Oe^{-1}), $CoFe_2O_4$/$BaTiO_3$ (50 mV cm^{-1} Oe^{-1}), PZT/Terfenol-D (4,800 mV cm^{-1} Oe^{-1}). Two-phase composite structures show magnetoelectric coefficients almost three orders of magnitude higher than those of single phase systems, while single-phase multiferroics switching speeds are intrinsically higher. Experimental studies have shown about 100ps (10GHz) switching times in single-phase multiferroics, and only 1 ns(1GHz) in the composite multiferroics.

The above approaches to material selection are postulated for fabricating an efficient spin wave bus or an interferometer based spin wave majority logic device.[136]

4.2.3.2. *NANOMAGNETIC LOGIC MATERIALS*

Magnetic cellular automata for logic is based on ferromagnetic islands arranged in cellular arrays, where local interconnectivity is provided by magnetic field interactions between neighboring magnetic dots.[137] In early work, 100nm diameter dots of 30-50nm thick islands were made of permalloy and supermalloy.[138] Since the state of one MCA is changed by the magnetic field generated by other local MCA, a critical challenge for this technology is to have reliable propagation of alignment between multiple MCAs. One option is to use magnetic materials with magnetocrystalline biaxial anisotropy. The biaxial anisotropy creates a metastable state for a rectangular nanomagnet, when it is polarized along the hard axis[139] and improves switching reliability. Material systems that exhibit such biaxial anisotropy include: epitaxial Co on single crystal Cu substrates[140], epitaxial Fe on GaAs[141], and epitaxial Co/Cu on Si.[141] The materials used in nanomagnetic logic are described in Table ERM6

To increase the magnetic flux density in the MCA, one option is to surrounding magnets with a different material to increase absolute permeability. This effect has been demonstrated in MRAMs, where enhanced permeability dielectrics had embedded magnetic nano-particles to increase a word/bit line's field strength without increasing current.[142] Proposed materials could increase the absolute permeability range by 2-to-30. Moreover, the fact that particle sizes are below the superparamagnetic limit should help ensure that magnetic the state is not unduly influenced.

While these approaches are based on magnetic islands with in-plane magnetization, utilization of layered stacks, e.g., cobalt-platinum multi-layers with magnetization perpendicular to the plane, is possible. A recent study demonstrated single-domain magnetically-coupled islands with perpendicular magnetization, fabricated with focused-ion-beam patterning of Co-Pt multilayers.[143]

4.2.3.3. *EXCITONIC FET MATERIALS*

Excitonic FETs can be constructed of alternate channel materials, but with different design. The parallel channel device separates electrons and holes and forms an exciton that is controlled by a gate electrode. Since this can be fabricated with alternate channel materials, it will not be discussed further in the ERM. A more detailed description of this device can be found in the ERD Logic Section.

4.2.3.4. *BISFET MATERIALS*

The Bilayer Pseudo-Spin FETs (BISFET) is proposed to be constructed of two layers of graphene separated by a thin insulating dielectric. The goal is for an excitonic collective superfluid of electrons to form in one graphene layer coupled

to a collective superfluid of holes in the other graphene layer at room temperature. There is considerable debate over whether this coupling can occur at room temperatures. A more detailed description of this device can be found in the ERD Logic Section. The materials used in BISFET devices are described in Table ERM6.

4.2.3.5. *SPIN TORQUE MAJORITY GATE MATERIALS*

Spin torque majority gates consist of multiple spin devices connected to a common "free" spin layer. Two different spin devices are proposed for use in this logic, spin torque nano-oscillators (STNO) or magnetic tunnel junctions. These two devices use different effects in their operation and are described in more detail in the ERD Logic section. The materials used in spin torque majority gate devices are described in Table ERM6

The STNO majority gate operates by sending spin waves through the "free" layer and the wave frequency in the free layer is the same as the majority of the oscillators. These devices are constructed of ferromagnetic materials and thin nonmagnetic films. As these devices are reduced in size, it will be important to have low damping in the free layer. Damping can be intrinsic to the material, but can be caused by surface roughness and damage in the surfaces of the free layer. Thus, it will be important to develop processes that minimize surface or sidewall damage and roughness. While it is important to have low damping, some is required to dissipate switching energy and enable fast switching.

In the magnetic tunnel junction device, the magnetic alignment of each input is transported through a tunnel barrier with spin polarized electrons providing the torque to the free layer. For these devices to be energy efficient, a small amount of tunneling current should produce the change of magnetization in the free layer. Thus, the tunnel barrier needs to have a very small amount of spin scattering and the damping in the "free" layer needs to be very small. Thus, as in the STNO device, the free layer needs to be a material with low damping, and be fabricated with low extrinsic damping. Furthermore, to enable scaling to very small feature sizes it is important to develop MTJs that operate with out of plane magnetization rather than the current in plane structures. This may require a new set of materials for these devices.

4.2.3.6. *ALL SPIN LOGIC MATERIALS*

All spin logic consists of magnetic or spin devices that communicate their state to other devices through the transmission of spin waves through magnetic interconnects. For this to be scalable to small geometries, the magnetic material will need to have low intrinsic damping and be processed to produce interconnects with low roughness and low damage at surfaces and interfaces. More details about all spin logic can be found in the ERD Logic section. The materials used in all spin logic devices are described in Table ERM6

4.3. SPIN MATERIALS

A number of spin based devices are being evaluated in the Emerging Research Devices Chapter for Memory and Logic applications. In these devices, electron spin orientation is employed to represent information by either using an individual spin or a collection of spins in a magnet. The operation of these devices depends on nanometer scale material properties and multiple materials will be needed to enable these devices. A few of the basic functions required for most devices are 1) Electrical signal to spin conversion, 2) spin state storage, 3) spin transport, 4) electric or magnetic field induced spin modifications, and 5) spin state to electrical signal conversion. Materials that support these functions need to operate up to ~400ºK. These functions may be performed in a single material, at an interface, or in a combination of coupled materials and will need to operate in nanometer scale structures. These spin-based materials, along with their critical properties and challenges, are listed in Table ERM7.

Table ERM7 Spin Material Properties

4.3.1. SPIN MATERIAL CHALLENGES

The key material challenges for the realization of a device are: (1) reproducible synthesis of semiconducting magnetic materials with higher Curie temperature, i.e., Tc > 400 K and high remnant magnetization, (2) materials or structures with high coupling of electrical potential to magnetic alignment or spin alignment, (3) compatibility of these materials with CMOS processing, and (4) metrology to characterize spin and domain physics. A more detailed list of spin metrology needs is included in the ERM Metrology Section.

4.3.2. SPIN MATERIAL PROPERTIES

The set of critical properties for different spintronics materials, Table ERM7, will depend on the specific device applications, as discussed in the ERD Chapter. Within the context of evaluating progress in fabricating a semiconductor based or an all metallic spin device (as in the ERD), this section focuses on materials that exhibit the following physical

phenomenon: (1) Spin wave propagation and modulation for Bus and logic, (2) nanomagnetic logic (3) the field effects of spin polarized electrons and holes for memory and logic. Thus, this section sequentially focuses on the following materials and their properties.

Dilute Magnetic Semiconductors

- Ferromagnetic transition temperature (T_C)
- Size dependence of T_C – Nano materials
- Wide band gap magnetic doped oxides and nitrides
- Group III-V and Group IV

Spin Injection/detection Materials
Spin Tunnel Barriers
Semiconductors and Nanostructures
Materials for Spin Wave Spintronics devices
Materials for Nanomagnetic logic

4.3.3. DILUTE MAGNETIC SEMICONDUCTORS

The potential value of dilute magnetic semiconductors, also known as ferromagnetic semiconductors, is that the magnetism can be turned on or off by changing the carrier concentration in the material. Several III-V compounds doped with Mn have been validated to have carrier mediated magnetic properties at low temperature and group IV Mn doped alloys have also been reported to be ferromagnetic. Wide bandgap transition metal oxides doped with Mn or Co also have been reported to exhibit magnetic properties, but carrier mediated (coupled) magnetism has yet to be validated in these materials. Since many of these materials are group III-V semiconductors doped with 3d transition metals, such as Mn and Co, it is feasible to integrate them with the current CMOS technology. Since magnetic material properties can be induced with the application of an electric field and their spin alignment can be manipulated electrically, these materials could have many applications in spin devices. However, the primary constraint in using this material, (Ga,Mn)As, is that its highest ferromagnetic transition temperature, with verified carrier mediated exchange achieved to date (Tc=200 K)[144], is still well below room temperature. Research is needed to identify alloys compatible with semiconductor technology, having Curie temperatures above 400ºK, high remnant magnetization, and carrier mediated exchange. A more detailed discussion on this is included in the 2009 ITRS ERM Chapter.

4.3.4. SPIN INJECTION MATERIALS

The purpose of the spin injection material is to inject a highly spin polarized current into a semiconductor. This can be accomplished either through high intrinsic spin polarization, or band symmetry matching with the adjacent semiconductor and/or tunnel barrier, as discussed in "Spin Tunnel Barriers."

The material to be used for a spin injecting contact should have several key attributes.

(a) It must be ferromagnetic, with a Curie temperature of over 400ºK;

(b) It must have significant easy axis remnant magnetization, i.e., zero field magnetization, of at least 50% of the saturation magnetization;

(c) Provide high spin polarization of the injected current, producing high spin polarization in the semiconductor; and

(d) Be thermally stable against intermixing with adjacent layers, and degradation of its FM properties with processing.

Requirements (a) and (b) provide the non-volatile reprogrammable characteristics, which are highly desirable for applications such as field programmable gate arrays, logic elements, or memory. In general, the spin injection contact material needs to be selected and tailored for a particular semiconductor or tunnel barrier.

Three broad families of materials could be used for polarized spin injection, ferromagnetic metals, half metals, and ferromagnetic semiconductors, but each has different challenges.

Ferromagnetic metals (FMMs)—Traditional FMMs such as Fe, Co, Ni and alloys are well-known to the magnetic recording industry and readily meet criteria (a) and (b) above. Because of the large conductivity mismatch between a FMM and a semiconductor, an intervening tunnel barrier is required to enable efficient spin injection. This may take the form of a tailored reverse-biased Schottky contact or a discrete metal oxide layer (e.g., Al_2O_3, MgO, etc.). Several FMMs have been shown to meet criteria (c) for selected semiconductors and/or tunnel barriers. These materials are described in more detail in the 2009 ITRS ERM Chapter.

Half Metals—Half metals are characterized by the absence of occupied states near the Fermi energy for one spin channel, so that they are 100% polarized, making them very attractive as spin contacts. They generally meet criteria (a) and (b). In principle, such a 100% spin polarized metal does not require a tunnel barrier contact to alleviate the conductivity mismatch with a semiconductor. However, their polarization is highly sensitive to defects (a relatively low density of bulk defects reduces their polarization very rapidly), so these materials exhibit spin polarizations ~ 50%, typical of other FM metals at room temperature to 400ºK. In addition, defects associated with the semiconductor interface also appear to severely suppress the ideal spin polarization. Only modest electrical spin injection into a semiconductor (GaAs) has been reported to date[145,146] and, thus, half metals have not yet been demonstrated to meet criterion (c). Criterion (d) will likely pose significant challenges, although a few carefully tailored systems may be viable.

Ferromagnetic Semiconductors (FMS)—FMS are materials that are simultaneously semiconducting and ferromagnetic. As semiconductors, there is no issue of conductivity mismatch, and device design follows the standard principles of semiconductor band gap engineering. They can readily be grown epitaxially on other semiconductors, and incorporated into complex heterostructures, unlike most metals. FMS generally have Curie temperatures well below room temperature ~200ºK), as noted in the section under "Ferromagnetic Semiconductors." Therefore, they fail criterion (a). There are a few notable exceptions which are currently being investigated as discussed before.

4.3.5. SPIN TUNNEL BARRIERS

The large difference in conductivity between a ferromagnetic (FM) metal and a semiconductor precludes efficient spin injection, since the semiconductor accepts spin-up and spin-down carriers with equal equally and very low conductivity. The resulting polarization is essentially zero regardless of the spin polarization of the FM metal. To solve this "conductivity mismatch" issue, the interface resistance must be the largest in the series to control current flow, and also provide some spin selectivity. A tunnel barrier fulfills both criteria.[147,148]

Crystalline MgO has been used successfully as a tunnel barrier in CoFeB/MgO/CoFeB heterostructures with a TMR(300K) ratio of 350% with a 400C anneal and a TMR(300K) ratio of 600% with a 600C anneal[149]. The symmetry of the Δ_1 propagating state in single crystal MgO (001) matches that of the majority spin band in FM metals such as Fe. Therefore, majority spins are readily transmitted in Fe/MgO contacts, while minority spins are blocked. In principle, this results in a higher spin polarization of the injected current than produced by the Fe contact alone. Such band symmetry assisted spin injection may be a promising avenue for highly polarized contacts, complementing the Heusler alloy approach.

4.3.6. SPIN TRANSPORT IN SEMICONDUCTORS AND THEIR NANOSTRUCTURES

For several devices, once the spin is injected into a semiconductor, it is important that the spin not loose coherence in the time that transport, manipulation, and detection occur. Most experimental work on spin transport in semiconductors typically focuses on III-V direct gap materials, such as GaAs, because polarization dependent optical absorption / emission spectroscopies provides easy, direct and quantitative insight into carrier spin polarization and dynamics. The long spin lifetimes expected for the low-Z (weak spin orbit) Group IV semiconductors make spin angular momentum especially attractive. Spin transport, via electrical injection and detection of spin polarized carriers from FM metal contacts (e.g., Fe, CoFe) into Si, has been demonstrated[150, 151], with reported electron spin polarizations of 30% or more. Magnetic field induced coherent precession of the pure spin current and spin polarized charge current has been demonstrated in lateral and vertical transport geometries, respectively.[152, 153] These results collectively show that information can be fed in, processed and read out using spin rather than charge as the state variable. However, these results have previously been limited to low temperature, due to thermal noise generated by the contact resistance. Options to reduce this contact resistance, by controlling the depletion width in the Si, have been identified.[154] Recent work has demonstrated successful electrical injection, detection and manipulation of spin accumulation in Si using ferromagnetic metal / SiO2 tunnel barrier contacts at temperature to 500K, easily exceeding the operating temperature requirements for commercial application [S3].[155]

Graphene exhibits *spin* transport characteristics that surpass those of any other semiconductor studied to date, demonstrating large magnetoresistance (MR) at room temperature.[156] Such large MR has not been seen in any other semiconductor materials or nanostructures, including InAs to GaN to Si.

For low dimensional materials, CNTs are attractive as spin transport materials because their low dimensionality results in a suppression of certain spin orbit scattering mechanisms at higher temperatures (>70K), leading to longer spin lifetimes. Limited successes have been reported for spin injection into CNTs from magnetic metal contacts at low temperature. However, obtaining reliable contacts and reproducible results continue to be challenges. At present, for nanowires of any

semiconductor, there are limited results for spin injection and transport, though several experimental groups are currently working in this area.[157]

4.3.7. MAGNETOELECTRIC COUPLING (MULTIFERROICS)

This is covered in Complex Metal Oxides (below)

4.3.8. INTERFACES AND HETEROINTERFACES

All of the devices fabricated with these materials depend on having high quality interfaces, and the important properties depend on the application. For spin tunnel barriers, the interface must not scatter the majority spin carriers. For spin transport, the interfaces must have spin specular reflections that don't cause decoherence.

4.4. COMPLEX METAL OXIDE MATERIALS, INTERFACES, AND SUPERLATTICES

Complex oxides exhibit an extremely wide variety of electrical, magnetic and optical properties, including superconductivity, piezoelectricity, ferroelectricity, pyroelectricity, ferromagnetism and multiferroicity. Most complex oxides are strongly correlated electronic systems[158,159]. Their properties result from strong interactions between spin, charge, orbital and lattice. Many of them have a perovskite-type structure. The several competing states give rise to complex phenomena and rich phase diagrams. Typical examples are the high-T_c superconductivity in cuprates[160,161] or the colossal magnetoresistivity in manganites[162-164]. Due to the strong correlations in these systems, a small external perturbation leads to a large electrical, magnetic or mechanical response. Furthermore, interfaces and heterointerfaces in these complex oxides can lead to new properties arising from surface, electronic or orbital reconstructions[165-167]. Oxide heterostructures are artificial materials that can be engineered to tune the properties or even obtain completely new properties [165-172]. Recent examples include the superconductivity at the interface between the two insulators $SrTiO_3$ and $LaAlO_3$ or the improper ferroelectricity arising from the combination of a proper ferroelectric and an insulator. These properties may be exploited for memory and logic devices and to add new functionalities in silicon electronics.[173-175]

A major challenge is to control the properties with an external field, for example, modulating and controlling conductivity with an electric field. In the case that the material which shows a metal – insulator transition is used as the channel material in a FET structure, the transition can be controlled by the gate voltage. Actually, in an electrolyte-gated FET structure, with $NdNiO_3$ as the channel material, the metal–insulator transition temperature was reduced by 40K[176] with a gate voltage of -2.5V. With increasing hole concentration through the application of the negative gate voltage, the conductivity changed by one order of magnitude. A critical question is whether oxygen vacancies may also diffuse with high gate voltage and change the electronic property of the channel material. The investigation of field effect transistors in these materials is important not only to open up the possibility to realized Mott transistor but also elucidate the fundamental understanding of the metal – insulator transition in a strongly correlated electron material.[176,177]

4.4.1. COMPLEX OXIDES FOR SPINTRONICS

Spintronics is a domain where complex oxides are of particular interest with the possible coupling of magnetic and electric properties, so that magnetic readable storage media could be written electrically.

4.4.1.1. *MAGNETIC AND MAGNETORESISTIVE OXIDES*

The manganite $La_{0.7}Sr_{0.3}MnO_3$ is ferromagnetic and conducting. It is used as a conducting electrode in various devices when heteroepitaxy with other perovskites is needed. It has been used for example to act as the base in a perovskite heteroepitaxial metal-base transistor functioning at room temperature.[178] Moreover, it is a half metal, exhibiting nearly 100% spin polarization below its Curie temperature of 360K. Thus it is an attractive ferromagnetic electrode for spintronics devices, such as magnetic tunnel junctions or spin filters. Progresses in the growth of this oxide and control of its interfaces have pushed down to ~2 unit cells the limit of the critical thickness when a surface "dead layer" dominates with a lower Tc and lower spin polarization. However, since the Curie temperature is close to room temperature, the half metallicity is strongly reduced at room temperature.

Double perovskite manganites such as Sr_2FeMoO_6 are also half metallic with a higher Curie temperature (~400K). However, the magnetism is strongly related to the ordering of the Fe and Mo ions, which is very difficult to control. Thus there is a need for materials development for magnetic oxides with suitable Curie temperature and half metallicity.

Writing information using a magnetic field requires large local magnetic field or currents which has drawbacks for power dissipation and scaling-down capabilities. Thus the use of a voltage for the writing process would be ideally suited. Magnetoelectric multiferroics are potential candidates for electrically-controlled magnetic data storage or logic devices.

4.4.1.2. *MAGNETOELECTRIC COUPLING USING MULTIFERROICS*

Multiferroic compounds of interest are both ferroelectric (FE) and ferromagnetic (FM) or antiferromagnetic (AFM).[179-182] If the electric and magnetic orders are coupled (magnetoelectric effect), it opens up the possibility to have a mutual control of the properties: controlling a polarization by a magnetic field or controlling a magnetization by an electric field.

The electrical control of the ferromagnetism in a thin film such as switching the orientation of the magnetization by applying an electric field is particularly attractive for spintronics. However, FE-FM materials show only weak coupling between the 2 order parameters and there is no available room-temperature single-phase FE-FM compounds. There is, however, a room-temperature FE-AFM multiferroic: $BiFeO_3$.[183] It has a high ferroelectric polarization (Pr ~ 60 μC/cm^2 normal to the (001) plane) with a ferroelectric Curie temperature T_c of ~ 1100K and an antiferromagnetic Néel temperature T_N of ~ 650K. Electrical control of antiferromagnetism in $BiFeO_3$ has been demonstrated both in single crystals [184,185] and thin films [186]. The electrical control of a ferromagnetic film can thus be envisaged using exchange bias coupling which couples AFM and FE orders at the interface of a bilayer: the FE order of $BiFeO_3$ couples then indirectly to the FM order of the FM film.

Exchange bias between a metallic ferromagnet such as CoFeB [187,188] or $Co_{0.9}Fe_{0.1}$ [189] and the antiferromagnet $BiFeO_3$ has been demonstrated at room temperature. The exchange bias leads to a shift of the hysteresis loop of the ferromagnetic layer. The coercive field H_c depends on the ferroelectric domain structure.[188] Exchange bias coupling using $BiFeO_3$ to electrically control locally the magnetization in a ferromagnetic layer of $Co_{0.9}Fe_{0.1}$ [190] and in permalloy[191] has been demonstrated at room temperature.

Recent progresses have been done also using a manganite as the FM layer. Significant exchange bias owing to orbital reconstruction was evidenced between $BiFeO_3$ and $La_{0.7}Sr_{0.3}MnO_3$ [192]. Following this finding, a reversible electrical control of this exchange bias was achieved, however at low temperature (<10K) using a field effect device.[193] This is a first step towards the electric control of the half metal $La_{0.7}Sr_{0.3}MnO_3$. Further material development with higher blocking temperatures is required to achieve room temperature operation.

Both the ferromagnetic and insulating characters of another multiferroic film such as $BiMnO_3$ can also be exploited to design spin filters. By inserting a thin layer of $BiMnO_3$ or (Bi,La)MnO_3 between $La_{2/3}Sr_{1/3}MnO_3$ and Au electrodes, a spin efficiency up to 36 % was measured[194]. The ferroelectric character of the insulating barrier is also expected to influence the properties of the tunnel junction, which was observed [186]. Eventually, combining the ferromagnetic and ferroelectric characters of the insulating barrier allows to control both magnetically and electrically the tunnel current, leading to a 4-state memory device [195]. This 4-state memory device, however, operates so far only at low temperature.

Recent progress has been made on the possible control of magnetism using a ferroelectric tunnel barrier. The tunnel current across a ferroelectric barrier depends on the direction of the ferroelectric polarization due to electrostatic, interface and strain effects[196]. Local, large, and nonvolatile control of carrier spin polarization by electrically switching ferroelectric polarization has been shown in a tunnel junction with Fe and $La_{0.7}Sr_{0.3}MnO_3$ electrodes and $BaTiO_3$ barrier[197], however, also at low temperature. These results suggest a low-power approach for spin-based information control.

Tunneling electroresistance can also be used to read the polarization state of a ferroelectric film. Tunneling electroresistance has been evidenced at room temperature with ultrathin ferroelectric $BaTiO_3$ barrier (1-3 nm) on a $La_{0.7}Sr_{0.3}MnO_3$ electrode using the tip of an AFM as a top electrode. [198] TER of ~ 10000% are obtained with a 2nm $BaTiO_3$ barrier. Other junctions with $BiFeO_3$ and $PbTiO_3$ ferroelectric barriers also demonstrate tunneling electro resistance (TER)[199,200] at room temperature. Since ferroelectricity is robust down to few nanometers, memory junction based on this tunneling electroresistance can be fabricated at nanometer scale, which offers a potentially high integration density. Moreover, a low current is necessary for the writing of the information which is very attractive for low power operation.

For these various examples of the use of the multiferroic $BiFeO_3$ to achieve switchable non volatile devices, it is important to selectively control the switching path and the structure of the switch domain(s) [201] . The phase structure and domain structure can be controlled *via* strain.

In addition to spintronics applications the complex oxide $BiFeO_3$ exhibit also promising properties for piezoelectric effects, photoconduction or photovolataic effects and for spin-wave generation, conversion and control, which opens up the perspective of combining various functionalities (magnetic, electric, optical and mechanical) in future devices.[202-205]

4.4.2. METAL OXIDE HETEROINTERFACES AND SUPERLATTICES

Complex metal oxide heterostructures and heterointerfaces often have new properties that are not exhibited in the individual materials.[206] Forming interfaces between two band insulators, LaAlO3 (LAO) and SrTiO3 (STO), can lead to

highly conducting n-type interface (LaO/TiO_2) while a p-type one (AlO_2/SrO) is insulating.[207,208] The origin of the 2D electron gas is still debated. First-principles calculations of the polar-discontinuity, in terms of screening of internal electric field by ionic and electronic responses, provide a reasonable explanation for experimental results[209]. Another potential origin for the conducting nature of the interface may be the presence of oxygen vacancies. A recent study shows the existence of localized and delocalized Ti *3d* carriers in such superlattices that may originate from oxygen vacancies and electronic reconstruction.[210] Mobile electron gas at interfaces between insulating oxides has been also found in $LaTiO_3/SrTiO_3$[211], $KTaO_3/SrTiO_3$[212], $LAVO_3/SrTiO_3$[213], and $La_{0.5}Ca_{0.5}MnO_3/CaMnO_3$[214] heterostructures. Heterointerfaces in superlattices between antiferromagnetic insulators have exhibited ferromagnetism[215]. Furthermore, heterointerfaces between metallic and insulating cuprates exhibited high Tc superconductivity.[216]

Not only charges but also orbitals at an interface may undergo a reconstruction. Orbitals can be deformed from their normal shape and electrons at the interface may occupy a combination of orbitals that can strongly differ from that of the bulk. This provides an opportunity to engineer the bonding at the interface and thus modify the properties. Such orbital reconstruction has been evidenced in the $YBa_2Cu_3O_7$ / $La_{2/3}Ca_{1/3}MnO_3$ system, combining a high-T_c superconducting oxide and a colossal magnetoresistive one.[217] Across the interface between both oxides, a charge transfer from Mn to Cu ions induces an orbital reconstruction (changing its occupation and symmetry) in the interfacial CuO_2 layers.

Interfaces in superlattices can also change the nature of the coupling between competing instabilities and produce new properties. For example, superlattices combining ultrathin films of the proper ferroelectric $PbTiO_3$ and of the paraelectric $SrTiO_3$ oxides behave like a prototypical improper ferroelectric due to interface coupling based on rotational distortions.[218,219] In manganite superlattices of $Pr_{0.5}Ca_{0.5}MnO_3/La_{0.5}Sr_{0.5}MnO_3$, competition between the antiferromagnetic insulating phases and the ferromagnetic metallic phases of the materials with a 5:5 unit cell layers results in large change in the resistance with an applied magnetic field. [220] Thus, the physical phenomenon at oxide heterointerfaces may enable new devices and also enable new properties in superlattices.

To achieve novel properties in oxide heterointerfaces, the interface must be abrupt[221] and the films adequately thick on each side of the interface[222]. These heterointerface effects need to be characterized in superlattice structures to understand how they affect or limit resulting properties.

The study of these heterointerfaces and superlattices is progressing with a combination of modeling and simulation and experimental expertise to control the interface properties and coupling. The possibility of designing new materials to couple multiple properties should be explored for future spin or field effect based device technologies.

5. LITHOGRAPHY MATERIALS

The future of scaled technologies depends upon emerging patterning materials (resist or self assembled) to enable extensible lithographic capabilities. New resist materials must concurrently exhibit higher resolution, higher sensitivity, reduced line edge roughness, and sufficient etch resistance to enable robust pattern transfer. Evolutionary approaches for enhancing positive, negative, and chemically amplified families of resists will continue to be evaluated. Several process approaches to pitch division, such as spacer patterning (SP), multiple patterning (MP) and double exposure (DE) are under consideration as options for extending 193nm immersion lithography. Alternate technologies that utilize patterning materials include directed self assembly and imprint patterning. The advantages and challenges to these patterning materials are summarized in Table ERM8. Please see the 2009 ITRS Lithography chapter for a more detailed review of pitch division technologies.

Table ERM8 Challenges for Lithography Materials

5.1. RESIST MATERIALS

Critical Resist Challenges: Advanced lithographic processes are challenged to simultaneously achieve high resolution (R), low line width roughness (L) and high sensitivity (S), with sub-100 nm resist thicknesses. Additionally, these resists must meet other requirements such as adhesion, etch resistance, and FAB material compatibility, for example, for each specific exposure technology.

The current set of extensible exposure technology potential solutions include: 1) ArF immersion lithography, which represents a significant increase in process complexity, such as multiple patterning with aqueous and organic developers; 2) EUV lithography; and 3) maskless lithography[1-3]. Advanced resist materials must be developed to satisfy the RLS

requirements, as well as specific ArF dry, ArF immersion, EUV or maskless lithographic technology requirements. For chemically amplified resist (ArF or EUV), diffusion control, without loss of throughput, is critical for resolution improvement. Emerging materials options include specifically designed polymers and photoacid generators (PAGs) that minimize diffusion blur, but maintain high polymer deprotection efficiency by the photoacid. Polymerically bound PAGs have been reported widely for EUV resist design, as this system offers slow diffusion for resolution enhancement and uniform PAG distribution for better LWR. It is also possible to apply polymeric PAGs in ArF resists for high volume manufacturing. ArF double exposure (DE) single development lithography may provide a lower cost of ownership than the process intensive spacer patterning (SP) or double resist patterning (DP) methods. Aggressive research and development are needed for potential DE materials that satisfy 193 nm insertion targets. Non-Reciprocal PBG system and combination of PAG and PBG system have been proposed as double exposure (DE) resist[4-6].

For ArF immersion lithography, NTD resist development requires aggressive research to meet the demands of <22nm node technology. Key challenges include missing CH bond defects, film loss[7], etch resistance, pattern collapse and compatibility with the substrate,[8] top coating and other alternative options for CD shrinkage, for example Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS) and DSA contact hole shrinkage. Preliminary results indicate that the defectivity and CD uniformity of NTD resists can be significantly improved by optimizing the development process,[8-10] while the etch resistance can be compensated for by using a hard mask.[8] NTD also will be applied in EUV lithography for contact hole and trench resolution enhancement and may also have advantages for isolated lines. Research on top coat free ArF lithography, including both positive tone development (PTD) and NTD, will continue to demonstrate its cost of ownership reduction and defect control at the high scan speeds required by high volume manufacturing. [7]

ArF dry resists may be used in implant applications to replace KrF resists for the advanced nodes.[11] New resist materials must be developed to meet the projected resolution and reflectivity control requirements on topography, particularly for deep well and source drain type implant layers. Negative tone resists with TMAH developer and NTD resists with organic solvent developer can be useful for footing and scumming reduction.[12]

EUVL and maskless lithography require revolutionary resist materials that address the RLS tradeoff and, in the case of EUVL, also exhibit greatly reduced outgassing.[13-16]In order to meet the requirements of resolution and line width roughness on projected 11nm devices, several different EUV resist types, such as molecular glass resist, polymer bound resist and inorganic resist have been investigated. One of option for resolution enhancement is EUV with wavelength reduced from 13.1 down to 6.7nm.[17] Since most organic materials increase transparency with smaller wavelength, dramatically change of resist platform is necessary for adequate absorbance in a resist less than 100nm resist thick. .Resist film thicknesses may continue to shrink with feature size, in part, to avoid pattern collapse.[18,19] Below a critical thickness, the resist's mechanical and thermal properties change.[20-22] For example, the glass transition temperature of ultrathin multicomponent ArF and EUV resist films depends on the PAG/resist combination.[23] Also, line width roughness appears to increase with decreasing film thickness.[13,24,25] Future semiconductor processes might also require several different post processing methods to reduce serious pattern collapse and line width roughness at tighter pitch.[26,27] While work on positive chemically amplified resists will continue, research is underway to explore other potential material candidates that satisfy projected requirements for enabling emerging lithographic technologies. Organic, inorganic, and hybrid materials are under consideration for targeted resist applications that include: non-chemically amplified resists, novel negative resists, and 193 nm double exposure resists.

5.1.1. ARF RESIST EXTENSION OPTIONS

The primary focus of resist development will continue to be the evolutionary design of positive chemically photoresists. However, the challenge of simultaneously achieving resolution, sensitivity, and line edge roughness remains daunting. Consequently, older material systems, such as nonchemically amplified resists, negative resists, and materials that enable pitch division are also being explored.

5.1.1.1. *ARF NON-CAR MATERIALS*

With concerns of diffusion blur limiting the resolution of chemically amplified resist [28] and the impact of molecular weight on LWR,[29] there is renewed interest in non-CAR resists, especially those that use chain session as the primary dissolution switch mechanism. Also, up to 7× sensitivity improvement can be realized by reducing the PMMA film thickness to ~ 20 nm.[30] Polymeric chain scission of polysulfones, which are more sensitive than PMMA, also are under consideration for 193 immersion lithography applications. A post exposure bake can accelerate polysulfone depolymerization. 193 nm irradiation of polynorbornenesulfone[30, 31] results in film thinning, reduced SO_2 content, and an E_0 of <20 mJ/cm^2, when developed in a MIBK solvent. Successful non-CAR thin film materials must demonstrate enhanced ArF sensitivity, resolution, and plasma etch resistance, while improving LWR. Additionally, the photoproducts

should not diffuse into the immersion puddle in quantities sufficient to cause concerns about potential lens or tool damage. These considerations may limit the applicability of chain scissioning type chemistries, or constrain polymer designs.

5.1.1.2. *ArF Negative Tone Resist Materials*

Several ArF negative tone resist materials were developed to operate by a cross-linking or a polarity change mechanism.[32,33] Negative resists tend to perform better than positive tone resists with binary masks, but tend to respond less well to 6% phase-shift mask designs. They also tend to exhibit pattern bridging, when the aerial image has significant flare or when light is diffracted into dark areas (low κ_1). Research is needed to address these challenges. Organic solvent developable negative tone resist with polarity change mechanism becomes more potential chandidate with bright mask patterning[34-37]. The resist dissolution properties are controlled from the point of solubility parameters and that modified resist shows promising results on DOF, MEEF and CD uniformity on 40nm contact hole at NA 1.35 single exposure. Moreover, collected defectivity on 45nm contact holes indicates less than 0.1counts/cm^2. The process maturity has been proved, but the resist material for negative tone development should be improved in terms of dissolution contrast.

5.1.1.3. *ArF Inorganic Resist Materials*

As CDs continue to shrink, thin resist films with high etch resistance will increasingly be required to avoid pattern collapse and effect robust pattern transfer. Inorganic cross-linkable nanoparticle resists provide an interesting approach to achieving high etch resistance in the exposed regions. Early 193 nm studies, at NA=1.3, with these inorganic systems have demonstrated lines with a 50nm half pitch and an etch rate almost an order of magnitude slower than that observed for polyhydroxysterene (PHS) based resists, with an added potential benefit for enhanced depth of focus.[38] Research also is needed to reduce LWR roughness by optimizing the material, nanoparticle, and component structure with respect to desired properties and projected patterning requirements.

5.1.2. Materials for Pitch Division with a Single Exposure

Spacer patterning and multiple patternng are recognized as standard pitch division methods. But pitch division via the single exposure method is suggested as a simpler alternative process for spacer patterning. This pitch division method requires new resist materials, which includes a photo-base-generator (PBG).[9,10] When exposed to extremely low doses of irradiation, neither acid nor base are generated. Exposure of the PAG and PBG to low doses of irradiation generates more acid than base, which deprotects the polymer, creating a positive tone pattern. Subsequent exposure to high doses generates sufficient base to overcome the generated acid amount, which protects the polymer and yields a negative tone pattern. Research is needed to explore the design considerations, benefits and trade-offs for this novel class of patterning material systems.EUV Resist

5.1.2.1. *Challenges*

5.1.2.1.1. *Shot Noise* [39-41]

At the very low exposure doses desired for high throughput EUV lithography, stochastic variation becomes a significant issue in the image formation process. To address this challenge, research is needed in several key areas, i.e. to increase: EUV light absorption; secondary electron yields (SEYs), through polymer design; and finally electron capture efficiency of the secondary electrons by the PAG.[41]

5.1.2.1.2. *EUV Light Absorption* [40,41]

Fluorine is the second row element on the periodic table with the highest absorption at 13.5 nm. In a lithographically useful series of fluorinated polymers, the highest practical EUV absorption is maximized at a value of about seven.[42] The extreme of maximum absorption is about 18.5 (impractical, PTFE), which for resist film of 40nm thickness would still have 50% transmittance. Much higher z elements can have a higher EUV absorption cross section than fluorine or oxygen. However, it can be chemically challenging to incorporate high z atoms into an effective EUV formulation (See the section on inorganic EUV resists). Increasing film density can play a big role by increasing the number of light absorbent atoms per unit volume.

5.1.2.1.3. *Acid and Electron Blur*

Shot noise and photoacid diffusion are intimately linked in governing resolution, photospeed, and LWR.[43] Multiple reports demonstrate and confirm that RLS variables can't be independently optimized.[43] The interdependence of these critical factors has been shown repeatedly in ArF and EUV lithography. In a chemically amplified system, may be impossible to overcome the inherent issues of the diffusion blur problem.[44] The diffusion of photoacid necessary to accomplish chemical amplification may fundamentally limit the achievable resolution, photospeed and LWR of these systems.

A stochastic resist model has been applied to estimate the acid diffusion length for a polymer bound PAG (PBP).[45] A PBP methacrylate resin currently under consideration showed an acid diffusion length of just 9.7nm. However for sub-20 nm lithography the acid diffusion length will probably need to be less than 6 nm, which may be attainable. The stochastic model methodology was used to estimate the electron blur, which represents the contribution from the electron motion relative to the acid blur, of the EUV resist exposure; and calculated a value of 2.5nm, a much lower value than reported by others.[40]

5.1.2.1.4. *OUT OF BAND RADIATION*

OOB is defined as unwanted radiation emitted from the EUV source that extends from 140 to 300nm.[46] Most resist platforms are extremely sensitive to OOB, and this appeared to correlate with the resist absorbance at the longer wavelength.[47] For example, PAGs containing the triphenyl sulfonium cation [TPS] have a very high absorption in the UV band, spanning 180-370 nm, which makes it particularly sensitive to OOB radiation. PAGs with poor absorption efficiency in the same deep-UV band region will decrease resist sensitivity to OOB.[48] OOB sensitivity is measured by comparing the resists exposure dose sensitivity at multiple wavelengths.

5.1.2.1.5. *RESIST OUTGASSING*

Some PAGs outgas extensively with EUV irradiation in a vacuum. For example, PAGs containing the TPS cation generate high levels of diphenyl sulfide.[49] Gaseous carbon containing photoproducts, especially unsaturated groups, can readily deposit on EUV optics and masks. As a result, new PAGs are being designed for EUV lithography that do not generate diphenyl sulfide and other gaseous byproducts that avoid optics coating issues.[41]

5.1.2.1.6. *CONTINUED IMPROVEMENT OF POLYMER-BOUND PAG (PBP ANION) RESIST SYSTEM*

Research continues to design improved PBP systems with the following improvements[39]: 1.) increased photon capture, via increased EUV absorption and film density; 2) decreased the OOB photon capture efficiency; 3.) optimized electron affinity of the matrix polymer to increase thesecondary electron yield; 4.) increased acid generation efficiency, by tuning the electron PAG capture rate; 5.) improved PBG film homogeneity; and 6) decreased organic outgassing during exposure.

5.1.2.2. *NON-CA RESIST AND INORGANIC RESIST*

Several groups have demonstrated excellent resolution demonstrated with non-CA resists.[50-61] High MW PMMA, which switches via a chain scission mechanism, has been shown to resolve 12 nm hp;. However, PMMA's 40 mJ/cm^{2}dose to size is too high for high volume EUV manufacturing applications.[54] Other non-CA resists with a chain scission mechanism to mitigate chemical blur induced by acid diffusion during post-exposure bake step commonly used in chemically amplified resist. Polycarbonate based non-CA resist consists of the unit providing etch resistance/high Tg and the other unit for degradation induced by EUV irradiation.[62,63] This non-CA resist could achieve 28.6 nm line CD on 50 nm lines/spaces mask at the dose of 104 mJ/cm^2. LER was about 5.2 nm. Since it is reported that roughness induced by mask was 3.5 nm of LER on patterned photoresist on the Sematech-Berkley micro-field exposure tool[64], the LER observed is only 1.7 nm greater than that of mask induced roughness. The poly(olefin sulfone) backbone was designed to be highly sensitive to EUV radiation.[65] The related materials possessed high sensitivity towards degradation by EUV radiation (E0 in the range 4 to 6 mJ/cm^2). EUV interference patterning has shown capability of resolving 30 nm lines/spaces features. From the results of outgassing test, contamination thickness on witness sample test and carbonization rate on residual gas analysis increased as molecular weight of olefin unit wtih functional groups increases.[66,67] Current non-CA negative tone resists exhibit poor EUV efficiencies, and they require more than twelve times the minimum dose required for high volume manufacturing. Without significant enhancements in EUV source power, research is needed to improve the efficiency of radiation scission or crosslinking events for non- CA resists to satisfy projected EUV lithography requirements.

Inorganic approaches to non-CAR materials appear to hold a greater promise of achieving sensitivity and other goals. For example, electron-beam resists with Zr and Hf[55] have demonstrated sensitivities as low as 8 μC/cm^2, achieved 15-nm lines and 36-nm dense features at higher doses, with a line-width roughness of approximately 2 nm. These resists also exhibit high etch resistance (>7× that of thermal SiO_2) in reactive-plasma etching. The high absorption cross-section of these heavy atoms aids somewhat in reducing the photospeed. Low film thicknesses are possible because of the very high plasma etch resistance, and the high density (4.7 g/cm3, compared to about 1.2 g/cm3 for polyhydroxstyrene) is thought to decrease electron blur significantly. Zero hydrocarbon outgassing was observed, due to the resist's inorganic nature. Work continues on improving resist sensitivity, shelf life, and resist integration.

5.1.2.3. *HYBRID EUV APPROACHES*

EUVL technology can leverage the extensive ArF lithography knowledgebase. Interlaced double pattern processing, using EUV lithography, would enable a variety of pitch doubling techniques.[48] EUV resists with negative-tone development should be investigated to take advantage of the improved aerial image NILS for the formation of contacts and certain other pattern features. Polarity reversal and organic solvent development approaches could be helpful for improved contact CD uniformity, and improvements in preventing pattern collapse. Combining EUV with DSA could be a way to rectify LWR in EUV patterning. Alternatively, EUV could be used to form graphoepitaxially defined wells for DSA, or chemoepitaxially defined pre-patterns for DSA alignment[68]. These approaches are still nascent, but they hold very strong promise for extending EUV to 11nm node and beyond.

5.1.3. RESIST SUMMARY

Several lithographic techniques are emerging that may drive and enable the continued area scaling of transistors. EUVL EBL, NIL and 193nm with multiple patterning are all candidates. These techniques will need new resist materials in order to meet various roadmap requirements. One or more breakthroughs in resist materials will be required in for each lithographic technique in order to concurrently achieve the required resolution, sensitivity, and LER. Additionally, other resist requirements, adhesion, etch resistance, aspect ratio and cost must be met. Material developments in DSA patterning may enable current extension of 193nm and future extension of EUVL, however, other challenges with DSA must be solved. While the main challenge remains defectivity, pattern transfer and domain size requirements are also major obstacles for deployment of this approach.

Presently, there are multiple organizations working on producing viable material approaches in order to enable each lithographic technique. Immersion 193nm with multiple patterning remains the current technique of choice until such time as a breakthrough enables disruption of this path.

5.2. DIRECTED SELF ASSEMBLY FOR LITHGRAPHY EXTENSION

Directed self-assembly (DSA) refers to the alignment of self-assembled patterns in desired locations, with predictable shapes, controlled dimensions, and registered within a lithographically generated pattern. Potential applications of DSA to extending lithography include sparse pattern multiplication, line edge or width improvement, and improved control of feature sizes (i.e. contact size distribution, etc.). Progress has been made in demonstrating alignment to sparse patterns, improving LER and contact size distribution. Furthermore, domain sizes down to 5 nm, and lithographically useful anneal times have been demonstrated with different techniques. The challenges for directed self-assembly are summarized in ERM8.

For lithography extension applications, polymer self-assembly is driven by phase segregation of different polymers, with the driving force proportional to χN (χ is the Flory Huggins parameter and N is the number of monomers in the polymer). The direction to assembly in predefined locations is provided by structures or chemicals on surfaces that preferentially attract one of the polymers. The natural assembly dimensions are proportional to $N^{2/3}$ (in the strong segregation limit) the number of monomers in the polymer, so the driving force for assembly will be decrease as natural assembly dimensions are reduced. Since self-assembly is a thermodynamic process, defects are inherent, but the "directing forces" can make the formation of defects energetically unfavorable.[69]

5.2.1. CRITICAL CHALLENGES

If DSA is to be considered a viable and competitive patterning option, it must be able to assemble useful patterning nanostructures with defect densities $<0.01 cm^{-2}$. Clearly there are many challenges in Table ERM 8, and many of these may require engineering, but the main question is whether defect density is limited by thermodynamics or can it be reduced to the required level through the use of aligning features.

Recent research has brought progress in each of these aspects, but no material/process combination currently satisfies all of these requirements. Block copolymer self-assembly can easily define a limited set of highly symmetric patterns, i.e. repeating lines/spaces, hexagonal arrays and square arrays of cylindrical holes, that may be useful in defining circuit elements. The most important issue is whether DSA features can be assembled with defect densities approaching $<0.01cm^{-2}$, and recent reports indicate that progress has been demonstrated in reducing defect densities significantlyto $<25cm^{-2}$ [70]. DSA features can be aligned to pre-existing structures through graphoepitaxy or surface energy patterns. Annealing times, have been reduced from days to a few minutes through the use of either higher annealing temperatures or solvent annealing, which represents a realistic timescale for potential processing applications. Self-assembled structures have been generated with dimensions well below 10 nm, providing evidence of this approach's extensibility.

5.2.2. DSA MATERIAL OPTIONS

5.2.2.1. *DIBLOCK COPOLYMERS*

For lithography, diblock co-polymers are limited to assembly of lines and "contacts" in close packed hexagonal arrays. The phase diagram of the diblock copolymer, which depends on the composition of the material and χN, determines the structures that can form for different ratios of the polymers and this in turn determines the spacing between features.

5.2.2.2. *TRIBLOCK COPOLYMERS*

Triblock copolymers have a richer suite of patterns that can assemble for lithography which includes lines with larger ranges of separation and "contacts" in square arrays. Furthermore, the addition of the third polymer has been exploited to add new functionality such as chemical sensitivity[71] or photosensitivity and enable selective activation or deactivation of specific features.

5.2.2.3. *POLYMER BLENDS*

The addition of one of the polymers to a diblock copolymer has been employed to enable smoothing of features [72], such as corners. More recently directed self-assembly of polymer blends has demonstrated the ability to assemble featuressimilar to those assembled with block co-polymers. So, it is possible that addition of polymers to a block copolymer may enable improved control of features. In the case of assembly of polymer blends, this may enable assembly of structures with more abrupt interphase transitions than is achievable with block-co-polymers.

5.2.2.4. *HYBRID POLYMERS*

Recent work using hybrid blends of block copolymers with organisilicate oligomers[73] and blends of homopolymers with triblock polymers[74] have demonstrated characteristic microdomain spacing well below 10 nm, an indicator of potential extensibility. In another recent report, supramolecular assembly of hydrogen-bonding units was combined with the controlled phase segregation of diblock copolymers to fabricate highly-ordered square arrays of sub-20 nm via structures, instead of the hexagonal ordering that is normally observed.[75] A more evolutionary path may require a hybrid resist formulation that incorporates phase segregating diblock copolymers to yield a resist that can self-assemble within the patterned feature, and a proof of concept has been demonstrated.[76] However, significant research in these areas is needed for these systems to warrant consideration for sub-22 nm potential solutions.

5.2.2.5. *DSA GRAPHOEPITAXY*

In this approach, lithographically-defined topographic features and boundaries direct the ordering of a self-assembled block copolymer film with sublithographic resolution on a surface that is "neutral" to the polymer blocks. This is described in more detail in the ITRS ERM 2009.

5.2.2.6. *DSA CHEMICAL PATTERNED*

Directed block copolymer assembly on substrates with lithographically defined chemical nanopatterns, that preferentially attract one of the polymers, offers a second route for aligning and registering patterns of block copolymer microdomains.[77] This is described in more detail in the ITRS ERM 2009.

5.2.2.7. *DEFECT DENSITY*

A fundamental concern for DSA is whether defects are intrinsic to the thermodynamically driven assembly process or whether defect formation can be made energetically unfavorable by the constraining fields. If defect densities could be reduced to ITRS requirements, many of the other challenging requirements could be addressed through polymer innovation and engineering of processes. Experiments by the mass storage industry indicated that constraining fields eliminated dislocations, and point defects were reduced to less than 100ppm. Recent experiments on DSA structures fabricated in non-cleanroom environments reported DSA defects $<25cm^{-2}$ when particulate related defects were

eliminated. Furthermore, modeling and simulation results indicate that constraining structures can increase so that defect formation is energetically unfavorable. At this point, the free energy of formation of specific defects depend on the block copolymers, the structure being assembled, the deviation of the constraining structure from the natural dimensions of the copolymer, and the interaction strength of the interfaces with the polymers, the energetics must be calculated for each defect with specific copolymers and structures. It is extremely important to determine the sensitivity of defect formation energy to variations in the lithographically defined patterns and validate whether low defect densities can be achieved with filtered copolymer processed in a cleanroom.

Experiments and modeling indicate that under some circumstances self-assembled structures are not always vertical but can have a 3D structure. Furthermore, under some conditions, experiments have observed different morphology at the top of the self assembled structure than at the bottom of the material. Thus, it is important to determine the structure and defect density that is transferred to the underlying material after development and etch. Thus, it will not be adequate to characterize the defect density on the top surface of the developed copolymer structure.

Metrology is needed to characterize defect densities over large areas with assembled block copolymers. Significant challenges exist to characterize the defect density in the thin block co-polymer films. Furthermore, existing defect inspection instruments are optimized for patterns that defined by a photomask, while DSA features may have more variability in position of features when performing pattern multiplication. This may be detected as a defect when it is within the allowable registration of features, alternately variability of feature location may make the system insensitive to defects.

5.2.2.8. *ANNEALING TIME*

Significant progress has been made in reducing annealing time from days to minutes through either increasing the annealing temperature close to the glass transition temperature or though solvent annealing. It is not clear which will be most appropriate in manufacturing. It is also not clear whether solvent annealing is thermodynamically or kinetically driven assembly process and this could affect defect formation. Another option is to anneal the block-copolymers with microwave radiation to provide local energy in a short time to accelerate assembly processes. [78]

5.2.2.9. *PROCESS SIMPLIFICATION*

A critical challenge is to simplify the process used to define the patterns that direct the alignment of the block co-polymers. Graphoepitaxy requires multiple process steps to pattern, etch, and tune the substrate surface energy. The integration of photoresist functionality with self assembly[76] could provide a potential path to process simplification, but significant research is needed to make this a viable technology.

5.2.3. DSA CRITICAL ASSESSMENT

The ERM conducted a voting based survey of the potential viability of directed self assembly to extend lithography. The potential applications of DSA considered were 1) line edge roughness (LER) improvement; 2) Contact or via CD improvement; 3) density multiplication for memory array patterning; and 4) density multiplication for logic. The average scores for all applications were (2.1) indicating that the technology is promising; however, individual scores also identified important issues. The results of the DSA Critical Assessment are shown in Table ERM9. For the LER improvement application the average score was only 1.5 indicating that 50% of the votes believe that, based on the current state-of-the-art, DSA wouldn't provide sufficient improvement to satisfy LER requirements at the projected insertion window. The need to improve LER remains a key research challenge. For the contact CD improvement application, the average score for improving contact size control was 2.4 indicating that DSA looks promising for this application. For Memory and Logic pattern density multiplication, the ability to achieve a low defect density was a significant issue with a score of (1.6) for both, and this will be followed closely. Voting indicated a high confidence that DSA could achieve pattern density multiplication and pattern small features with short annealing times; however, there were concerns about the ability to exclude features and contaminant limits. So, this first critical assessment of DSA indicates that significant progress has been made in specific areas, but there are challenges in defect density and integration. This critical assessment will be updated in the future.

This critical assessment is based on voting by 20 participants from the ERM, Lithography, and partipants in the DSA workgroups.

Table ERM9 Directed Self Assembly Critical Assessment

6. EMERGING FRONT END PROCESSES' AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES' MATERIAL CHALLENGES AND OPTIONS

Key challenges for future FEP and PIDS materials and processes are to support extending CMOS to smaller dimensions with reduced variation in device performance. This will require more accurate placement of dopants in active device areas, directed self assembly of useful nanomaterials, and materials to enable selective deposition, etch, and cleans to enable self aligned structures in future devices. The requirements and challenges for ERM applied to FEP and PIDS applications are summarized in Table ERM10.

Table ERM10 FEP / PIDS Challenges for Deterministic Processing

6.1. DOPING AND DEPOSITION

Semiconductors, the basic material of a transistor, show its real worth by adding dopants that tailor the electronic properties, conventionally achieved by doping. Doping control becomes an ever more critical process when devices scale into the deep sub-30 nm regime. A key challenge for scaling semiconductor devices towards 10 nm is the ability to achieve high doping levels within source/drain regions, with abrupt dopant gradients with small variations at the source/drain interface to the channel, as well as controlled dopant positions within the channel. For example, the threshold voltage is sensitive to small variations in channel dimensions, the gate stack structure, and dopant variations in the depletion layer[1-5]. The threshold voltage variability will gate the extensibility of bulk planar CMOS device technology. Over the next five to ten years, MPU physical gate lengths are projected to scale from 17 nm to 10.7 nm. Also, the trend in the number of channel electrons suggests that by the year 2015 there may less than 20 active dopant atoms in the channel region. For channel doped devices, this low number of channel dopants may emerge as another critical performance and yield limiter. Non-doped three-dimensional transistors provide a significant solution for the random dopant fluctuation. These new transistors still pursue the doping technology advancement, shifting the general interests from the channel to the shallower junction as well as the source/drain interface to the channel. One positive outcome of ultimate doped transistor has been the demonstration that it is possible to tune electrical properties by controlling, not an ensemble of dopants but, the placement of individual dopants[6]. Research is needed to develop new materials and fabrication methods that enable deterministic control of the composition and structure of doped material and gradient systems. One way to control the doping profile is by deterministic processing and doping[7-10].

For FEP and PIDS applications, deterministic fabrication refers to 3D nanopatterning and assembly methods that provide sufficient control of the composition and structure of doped interfaces and components to yield several orders of magnitude improvements in device to device performance variability. Doping processes with atomic-scale placement and concentration control will enable tunable device performance characteristics and reduced device-to-device variations. A reduction in device noise enlarges the useable design space, circuit-level uniformity, and system performance. The ability to accurately place dopants also may enable radically new device concepts, such as emerging quantum computing devices, based on coherent manipulation of single dopant atomic states within Si[11-13] or diamond matrices.

6.1.1. DETERMINISTIC DOPING

As device dimensions continue to scale, tighter doping concentration tolerances will be required to achieve projected performance control requirements. The reality for transistor doping, as planar CMOS devices approach 16 nm characteristics, is that both implantation and annealing techniques face significant challenges. The general nature of these challenges; i.e. increasing random dopant fluctuation, dopant activation, controlling dopant diffusion and minimizing junction leakage current, are certain to remain relevant as transistor/switch design extends towards atomic-level materials and designs. Candidate doping options must address the following: 1) atomic scale control of dopants and massively parallel dopant delivery; 2) random dopant fluctuation in the active channel region, ultra shallow junctions in the source/drain region and abrupt transitions between the source/drain regions and the channel; 3) compatibility and integration with existing fabrication platforms; and 4) economics, which depends upon on R&D and equipment costs, yield, and throughput.

Deterministic doping is a method based on the premise that atomistically precise control of dopant position and composition are needed as device dimensions scale. Deterministic fabrication refers to 3D nanopatterning and assembly methods that provide sufficient control of the composition and structure of doped interfaces, which yield several orders of

magnitude improvements in device performance variability. Deterministic doping focuses on: 1) Introducing single-dopant/few-dopants within the channel, as well as the source/drain regions, with placement accuracy of <<10nm; 2) activating the low number of deterministically introduced dopants effectively; 3) measuring and imaging single-dopant/few-dopants precisely; 4) exploring potential application opportunities through the atomistic control of materials, devices, and processes for better device performance. New metrologies can enable the characterization and realization of well designed atomic scale devices. A review article on single dopant control can be found in the supplemental document[14].

6.1.1.1. *STATE OF THE ART*

The deterministic 3D dopant placement and structural control technology required to enable atomically abrupt and reproducible source-channel-drain interfaces are in the early phases of exploratory research. This year's revision reviews recent progress in this area and considers potential options for enabling extensible doped CMOS channels and leveraging related emerging materials, devices and processes, and new device concepts, including quantum computing devices in Si or diamond, for sub-16nm applications.

6.1.1.1.1. *SINGLE ION IMPLANTATION (SII)* [15-20]

Several groups have now demonstrated the feasibility of single ion implantation, which is becoming a more important tool for enabling systematic studies of single atom devices. This technology seeks to deposit a specified number of desired dopant ions at precise locations within the active region. Key objectives are to achieve single ion implantations with high spatial resolution and flexibility in dopant species, as well as 100% single dopant detection. Single ion implantation can be measured by the detection of secondary electrons, photons, electron-hole pairs, changes in transistor channel currents, or direct imaging changes in surface topography. Significant sources of dopant positioning errors, such as implantation spot size, straggling range, and diffusion and segregation during annealing, must be addressed for SII to be relevant for ultimately scaled doped devices and related application opportunities, such as single atom device development, systematic studies of dopant fluctuation effects and tests of quantum computer architectures (qubit readout, control and coupling) in relevant device platforms and substrates, e.g., silicon and diamond.

6.1.1.1.2. *SELF-ASSEMBLY AND SURFACE CHEMISTRY* [21-24]

This chemistry based approach teaches that the dose can be modulated precisely by the formation of a mixed monolayer, consisting of tunable blank and active precursor components. Additionally, controlled nanoscale semiconductor doping by self-assembled molecular monolayers with loaded dopants can achieve sub-5 nm ultra-shallow junctions with spike anneals, due to the lack of transient enhanced diffusion often encountered in ion implantation. A key objective is to heavily dope 'self-aligned' semiconductor materials for nanowire and planar device applications.

6.1.1.1.3. *STM ATOM POSITIONING* [9, 10, 25-28]

Extremely small functional devices have recently been reported with atomic scale placement accuracy. Fabrication of the first atomically architected functional transistor, with all epitaxial in plane highly phosphorus doped gates, has been demonstrated in silicon, using a combination of scanning probe microscopy and molecular beam epitaxy. The method provides high stability and full activation in a high density n-type systems and low temperature process. Potential benefits of the STM approach include: The ability to pattern with atomic precision in three dimensions; extremely high density, atomically planar and abrupt doping profiles; the investigation of novel device architectures; and applicability to other dopant sources/metal/organics. It is highly unlikely that this technique will warrant consideration as a potential solution for advanced device fabrication, because of low throughput, STM tip stability, reproducibility. On the other hand, the patterning accuracy of this technique may enable exploration of unique devices, including 3D device architectures.

6.1.1.1.4. *LOW THERMAL BUDGET ACTIVATION* [29-30]

Very low thermal processing with microwave radiation, as well as millisecond energy pulses from flash lamps and laser, could keep dopant diffusion minimal. Extrinsic silicon has slight electrical conductivity and dipoles originated from dopants and vacancies. Microwave anneals could selectively generate heat directly inside the exposed material in the form of molecular rotational or polarization energies. That locally deposited energy becomes ergodically transferred throughout the material, retarding dopant diffusion and achieving the desired activation. Microwave anneals $<500^{o}$C have been demonstrated for B, P, As in Si, Ge, poly-Si. For STM-fabricated devices a low temperature incorporation anneal has been found to activate the dopants with minimal dopant diffusion[31].

6.1.1.1.5. *SINGLE DOPANT IMAGING* [32-34]

Tools for observing single atoms are now available. These include 3D atom probe tomography (APT), local electrode atom probe (LEAP), scanning spreading resistance microscopy (SSRM), low temperature Kelvin force microscopy (KFM), and scanning transmission electron microscope (STEM), etc.

6.1.1.1.6. *DISCRETE DOPANT MODELING* [35-39]

Steady progress has been made in resolving individual discrete dopants in drift diffusion (DD), Monte Carlo (MC) and quantum transport (QT) simulation tools. DD: The introduction of density gradient quantum corrections for electrons and holes has resolved the problem of artificial charge trapping in the coulomb well of the ionized impurity's attractive potential. MC: The introduction of ab-initio impurity scattering has allowed the characterization of transport variations related to individual dopant positions via 3D ensemble MC simulations. QT: Full 3D QT simulators are now readily available, which use effective mass and tight binding Hamiltonians. These transport simulation tools are essential, especially when developing concepts for nanoelectronic devices that can benefit from the deterministic doping.

6.1.1.1.7. *SINGLE DOPANT TRANSPORT* [40-48]

Recent studies have demonstrated transport through single donor/acceptor systems, memory effects in 2-donor systems, single electron transport in multi-donor systems, charge pumping, and single-dopant current spectroscopy. These findings are creating a more foundational quantitative knowledgebase that will enable the design of future CMOS devices, while they approach the ultimate single atom transistor limit.

6.1.1.1.8. *SINGLE DOPANT SPIN CONTROL* [49-50]

The spin of the electron or the nucleus on single dopant in silicon has been identified as an excellent system to encode and manipulate quantum information. Single shot readouts of electron spin on a single P donor in Si has been demonstrated, with a lifetime up to 6 seconds. The observed 92% readout visibility may enable electron spin qubit applications.

6.1.1.1.9. *SINGLE NITROGEN-VACANCY (N-V) SPIN CONTROL IN DIAMOND* [51-52]

Beyond silicon, the number of studies on single color centers in diamond has grown significantly in the last 5 years. The direct room temperature optical access to single electron spin control, with close to 2.4ms lifetimes, allowed great advances in the control of quantum states. This includes the demonstration of basic quantum logic, with a few qubits and transfer of quantum information from electrons to photons. These isolated spins may be located using confocal microscopy, initialized via optical pumping, and read out through spin dependent photoluminescence measurements. However, while single color centers can easily be found, the 1% to 60% yield appears to be energy dependent.

6.1.1.2. *KEY MESSAGES*

Functional devices with atomic scale placement accuracy can be fabricated; however, cost effective techniques are needed to place dopants with minimal damage to the crystal lattice. The fabrication of these devices currently requires the use of atomically accurate positioning techniques, such as STM assisted doping. Such techniques are not likely to become manufacturable, since they would require massively parallel tool architectures and face significant data management challenges. However, these methods may enable the exploration of fundamental device limits and new functionality, such as symmetry and quantum effects. Designed self-assembled dopant loaded monolayers can achieve controlled sub-5 nm ultra-shallow junctions with spike anneals. While the average spacing between dopants can be somewhat tuned by the choice of carrier molecule, the creation of complex dopant patterns, with required dopant control, remains a challenge. Medium placement accuracy, ~10 nm, doping methods (i.e., single ion implantation) exhibit the potential for device development applications. The projected manufacturing requirements create a need for new doping concepts. Research is needed on high throughput doping options that also deliver high placement accuracy. Emerging candidate doping research focus areas include directed self-assembly and the use of molecular monolayers as scaffolds for accurate and controlled dopant delivery. Deterministic doping will lead scaling semiconductor devices towards the single dopant limit. Novel characterization techniques, such as 3D atom probe tomography, will help to guide the evolution and assessment of emerging deterministic doping technologies words this goal.

6.2. DIRECTED SELF ASSEMBLY OF USEFUL NANOMATERIALS (SEE THE LITHOGRAPHY SECTION DISCUSSION)

The use of directed self assembly to position nanostructured materials, such as carbon nanotubes[53,54] has made progress but, considerable improvement in control of location direction and defect density is needed before this would warrant consideration for fabricating future charge based devices.

6.3. SELECTIVE ETCH AND CLEAN/SURFACE PREPARATION

With the wide range of new materials potentially being integrated into future technologies, there are significant needs for materials that enable selective and customized etching, cleaning or material deposition. Either macromolecules or self assembly processes that can enable coating of a specific material in the presence of other chemical processes, such as etching or chemical mechanical polishing could improve process selectivity and yield. Similarly, as feature sizes are reduced, cleaning processes will need to be more selective in removing particles without disturbing the desired structures.

Thus, there are opportunities for macromolecules and self assembled materials to enable the enhanced selectivity of future manufacturing processes.

Etch represents a critical step in conventional top-down pattern transfer processing. The lithographic and etch processes are significant contributors to the final dimension, dimensional variation, and functionality of a patterned feature. It may be advantageous to consider simplified fabrication scenarios that reduce the number of pattern transfer steps and the corresponding process related variability. The directed self-assembly of electronically useful materials represents an identified set of emerging technology options that show some potential for process simplification and for reducing patterning related variability. Early approaches for directed self assembly target resist applications that complement and leverage existing and projected lithographic and etch technologies. Future generations of self-assembling systems may be designed to incorporate electronically useful materials that would obviate the need for some etches.

6.4. Low Damage Dopant Processing

FEP has identified that post implant cleans are removing damaged silicon and this produces variability in the amount of dopant remaining in the silicon. Furthermore, as the industry integrates III-V materials ion implantation introduces damage that increases resistivity and can't be reduced through annealing. Thus, there is a need for methods to introduce dopants into source drain and channel regions with minimal damage to the channel material crystal structure. In deterministic doping, two approaches have emerged that have a potential to introduce dopants with minimal damage to the crystal 1) using a Langmuir deposition of a macromolecule with a dopant that bonds close to the surface of the channel material followed by an annealing step to drive the dopant into the crystal and activate the dopant in the crystal and 2) after the Langmuir deposition of the dopant with a macromolecule, dissassociate the macromolecule from the dopant and grow a thin epitaxial layer on the crystal to integrate and activate the dopant.

6.5. Contacts

Understanding and engineering atomic level contacts is critical for molecular scale devices. For these systems, nanoscopic factors, such as bond formation and configuration, significantly impact contact potential barriers.[55] Additionally, metal molecule interactions[56] and deposition variability may dominate nanoscale device operation. The nature of the metal-molecule orbital overlap will be important in determining the properties of their combined occupied states and available conduction pathways. For good mechanical or electrical contacts to be established with a low potential barrier[55], significant orbital overlap optimization between the molecule and the electrode is needed. Research is needed to understand the structure and properties of metal-molecule interactions and to design and synthesize new molecule-electrode material systems that enable stable, reproducible low potential barrier contacts.

7. Interconnects

Key challenges for continued increased performance of future integrated circuit interconnects consist of maintaining reductions of RC time constants for delivery of signals and power with high reliability. For copper interconnects to be extendible through 2024, the sidewall copper barrier thickness must be reduced to less than 2nm, which is challenging for technologies, as is summarized in Table ERM11. For post copper interconnect scaling, novel interconnects, such as carbon nanotubes, are being explored for their low resistivity and electromigration resistance and the challenges for these technologies are summarized in Table ERM12. Also, lower dielectric constant (κ for both intra and inter level dielectric are needed; however, each of these emerging families of materials must overcome significant challenges for them to warrant adoption. Airgap, another approach to reducing the effective κ, if adopted, would place additional requirements on barrier layers or novel interconnects.

Table ERM11 Interconnect Material Challenges

Table ERM12 Nanomaterial Interconnect Material Properties

7.1. Novel Ultrathin Barriers

The scaling of Cu barrier layer thicknesses below 2nm faces several challenges including the ability to block diffusion of Cu during processing, packaging and operation, have good adhesion to Cu and the low-κ ILD, block H_2O/O_2 diffusion into the Cu, and be compatible with Cu interconnect processing, such as CMP, ILD etch, and photoresist ashing. New trench/via barrier materials, such as Ru and CuMn that are discussed in the Interconnect chapter, are in development and expected to maintain barrier thickness scaling for several generations, but forecasts project Cu barrier layer thicknesses of < 2 nm by 2015 and < 1 nm by 2021. At these dimensions, it is anticipated that all barrier materials in development may fail and new materials or multilayer thin films will be needed. If the industry moves to airgap ILD technology, the barrier

requirements for these structures will become still more challenging. A serious issue is that all research on alternate barrier layers materials typically only report results down to 5nm. This needs to be extended down to 1nm.

A logical extension of the current trench/via barrier materials would be to identify new transition metal nitrides or direct plate metals with improved barrier capabilities that meet future requirements. To date, a host of alternate transition metal nitrides and direct plate metals have been investigated but only demonstrated at thicknesses down to 5nm. While, recent results for a 2.5nm MnN barrier have been reported[1], more research on new barrier metals at < 5 and ultimately < 1-2 nm is needed. Additionally, research is needed to determine whether metal (nitride) barrier films deposited by industry standard techniques are continuous at these dimensions - particularly in the presence of 2nm surface roughness likely present from patterning line edge roughness and low-k ILD porosity.

As an alternative to new "hard" metal barrier materials, research is also needed on so called "soft" Cu barrier materials such as self assembled monolayers (SAMs) and other organic films. SAMS were added to the 2009 ITRS and have shown the ability to impede Cu diffusion and improve adhesion between Cu and dielectric materials[2,3]. However, SAM barriers have not exhibited equivalent barrier performance to industry standard TaN [4]. More research is therefore needed to characterize and benchmark the performance of 1-3 nm thick SAM barriers versus hard barrier materials of similar thickness. Concerns over the survivability of SAMS in downstream processing and their barrier performance when combined with porous low-k ILDs, 2nm surface roughness, topography, and defects also need to be addressed. Organic films as Cu barrier materials are highly attractive due to their relatively low dielectric constant, but have yet to be demonstrated as Cu barriers at thicknesses of interest (< 2 nm) [5]. Lastly, graphene as a Cu barrier material also deserves some consideration and research. Recent results have shown the ability of monolayer graphene to protect Cu and Cu/Ni alloys against oxidation [6] and it's < 1nm thickness would be ideal for beyond 2020 technologies.

Cu capping barrier layers are also forecasted to approach thicknesses of < 2nm by 2020. At these dimensions, it can be anticipated that the current SiN/SiCN/SiOC materials will fail and that new materials will need to be sought out. While the key technical challenges for Cu capping layers are similar to those for the via/trench barrier layer, there are additional requirements including dielectric constant scaling where it can be anticipated that the current k values of > 4.0 for these layers will become unacceptable by 2020. While alternate paths focused on removing the Cu capping layer may be pursued, parallel research is needed on new Cu capping materials such as SAMS, organic films and other potential candidate materials such as a-C:H, a-CN_x, and a-BCN_x.

In summary, all of the candidate < 2nm barrier materials have their strengths and weaknesses. As means to perhaps address some of the weaknesses of each material, research that investigates combinations of "hard" and "soft" barrier materials should be considered and is highly encouraged as a means to address the needs of future technologies.

7.2. NOVEL INTERCONNECTS

7.2.1. NANOTUBE INTERCONNECTS

Emerging SWCNT or MWCNT nanotube interconnects or vias must demonstrate high densities of highly conducting nanotubes in desired locations, with controlled directionality and, low-resistance contacts. Additionally, the CNTs must be gown with a catalyst that is compatible with the ILDs and general semiconductor processing. CNTs exhibit ballistic transport over longer distances,[7,8] but SWCNTs consist of a mixture of metallic and semiconducting tubes, thus limiting their viability. MWCNTs, however, are distinctly metallic making them attractive as an interconnect candidate. A potential advantage of CNT vias is their ability to carry high current density without electromigration; however, electromigration at metal interfaces may be an issue.[9] Further, their low resistivity may offer potential advantages for interconnect applications, which include their ability to achieve ballistic transport. Since CNTs also exhibit quantum limited contact resistance, their length must be sufficient to yield favorable effective resistivities, as described in the Interconnect chapter. Additionally, CNT conductivity must remain high and stable during operation. Research and guiding material-design principles are needed for improved CNT functionalization, deposition, and positional control.

7.2.1.1. *GROWTH IN CONTROLLED LOCATIONS WITH ALIGNMENT*

For CNTs to be used as either devices or interconnects, they must be grown in precise locations and aligned in required directions. While progress has been made in growing nanotubes in desired locations,[10] directional alignment remains a challenge. Recent results suggest that CNTs grown in a directed electric field[11] can achieve general directional alignment. Additionally, growth on catalyst patterned sapphire or quartz crystal steps has grown aligned CNTs[12-14], although, placement remains a challenge. While growth on this substrate is less than the required density, this alignment is significantly better than other techniques. Another challenge is the controlled growth of CNTs. A zeolite can be used to

control CNT growth diameter[15], location and direction, however it must be demonstrated that such a templating matrix has no impact on the CNT conductivity. While several approaches to produce CNTs have been identified, the practical implementation of this concept to manufacturing remains elusive. Post-growth assembly options also are being explored.

Since interconnects span relatively long distances, high speed growth method should be strongly pursued.[16-18] The quality of CNTs affect the ballistic length of carrier transport in a tube. Therefore, high quality CNT growth and evaluation of their quality are important. The length must be sufficient to yield favorable effective resistivities, as described in the Interconnect chapter.

7.2.1.2. *NANOTUBE VIAS*

Vertical interconnects (vias) may benefit from the integration of CNTs into future technologies. Although an approach for the integration of CNTs into contemporary CMOS technology has already been demonstrated[19,20] a number of unsolved critical issues still remain to be addressed. Thus, new hybrid integrating schemes (combining top down and bottom up paths) compatible with the actual CMOS technologies and engineered at a level that also use thermal budgets (below 600 °C to reduce the thermal damages to LSI) are needed. In addition, theoretical studies have been carried out to derive electrical properties and offer an important guidance and insight on the applications of CNTs vias for gigascale-integration chips.[21-25] CNTs can significantly improve the RC delay and thermal conductivity at the intermediate and global level. For CNT vias to be viable they must be fabricated with a catalyst that is compatible with the ILD and semiconductor devices and their electrical and thermal reliability must be demonstrated. A number of key processes for which a control needs to be established to realize the potential of CNTs are described in the following sections.

7.2.1.3. *CONTROL OF CHIRALITY AND OF METALLIC VERSUS SEMICONDUCTING FRACTION*

In order to achieve comparable resistances predicted for Cu-based wirings, dense arrays (~1E14 tubes/cm^2) of small diameter (~1.2 nm) metallic SWCNTs and DWCNTs will be required. The variability of intrinsic CNT-via resistance is a function of the distribution of chiralities, which could exceed projected requirements. Hence, additional research is needed to elucidate chirality control. In the case of MWCNTs tradeoffs need to be made in the diameter and number of walls to achieve the highest density; however, the chirality control is less of an issue as the overall behavior is metallic.

7.2.1.4. *CONTROL OF CONTACT RESISTANCE AND ELECTRICAL CONDUCTIVITY*

The lower intrinsic limit of the resistance for a metallic SWCNT (or a metallic shell of MWCNTs) is 6.5 kΩ (independent of the tube diameter)[26] and reflections at the CNT-metal contact interface and phonon scattering contribute to an increase in total resistance.[27-30] Therefore, reliable and reproducible low resistance ohmic contacts are needed, since high resistances results in current reduction. Transparent SWCNT ohmic contacts, scaled to diameters <1.5 nm, remain a key challenge to achieving high-performance in nanoelectronic devices, due to the presence of positive Schottky (semiconducting nanotube) and tunneling barriers (metallic nanotubes). Fabricating direct metallic connections between all the nanotube shells also remains a technological challenge, since contact resistances at the bottom and top of CNT-based vias may enhance the risk of local heating and electromigration.[20] In the case of vias filled with MWCNTs, resistances down to 0.6 Ω have been reported for 2 μm diameter vias[20], and 34 Ω was reported for 160 nm diameter vias.[31]

7.2.1.5. *HIGH DENSITY CNT ARRAYS IN SMALL VIAS*

Ideal SWCNT arrays and contacts exhibit potential to improve intermediate and global RC delays by >40% over Cu wires. Locally, short low resistance CNT vias are needed that reduce the total capacitance, relative to Cu. Also, in-situ CNT growth and integration on relevant substrates is currently far from manufacturable. A catalytic process is needed that exclusively promotes growth of metallic SWCNTs, with the required density of ~1E14cm^{-2}. Also, appropriate, reliable, and reproducible analytical tools and statistical methods must be developed to help guide the integration and assess the insertion potential of this potential via technology. [22,23,32,33]

In the case of MWCNTs, the resistance of a 70 nm diameter via filled with close packed nanotubes of 4 nm diameter 6-wall MWCNTs including the top and bottom barrier layer can be estimated to be as low as that of Cu via. Based on this estimation, the target density of the MWNTs is 5 ×10^{12} cm^{-2}. To date, density of 1-2.5×10^{12} cm^{-2} vertically aligned diameter-controlled MWCNTs has been reported.[34,35] Independently, the fabrication of 70-nm diameter vias with MWCNTs grown by pulse-excited remote plasma-enhanced CVD has been also reported.[16,36]

7.2.2. GRAPHENE AND GRAPHITE CARBON INTERCONNECTS

Graphene is also a possible candidate for an interconnect material to replace Cu. Graphene is inherently a two-dimensional material, so it may be ideal for horizontal interconnects. Graphene, like carbon nanotubes, can sustain a high-

density current. In fact, research demonstrated that a few-layer graphene peeled off from graphite could sustain a current larger than 10^8 A/cm^2. [37] Numerical simulations predict that graphene nanoribbons can potentially have lower resistance compared to copper with a unity aspect ratio for widths below 8nm. Additionally, the simulations show stacks of non-interacting nanoribbons can have significantly smaller resistivities than Cu wires.[38] In order to realize graphene interconnects, a low temperature method for synthesis of graphene on a suitable substrate must be realized. Recently, synthesis of graphene by chemical vapor deposition (CVD) has been reported.[39-41] However, the synthesis temperatures are typically around 1000^{o}C, which is too high for interconnect applications. Recently, growth of multilayer graphene at 650^{o}C [42] and 580^{o}C [43] has been demonstrated, and the reliability of CVD-grown graphene interconnects have been investigated [42,44]. More research is needed in low temperature deposition to achieve graphene interconnects. Moreover, synthesis by CVD usually requires a catalyst film, which may have to be removed after the synthesis. In order to solve this problem, the catalyst-free growth of networked nanographite (NNG) on Si and SiO_2 substrates has been developed by using photoemission-assisted plasma-enhanced CVD.[45]

7.2.3. Cu and Silicide Nanowire Interconnects and Vias

If single crystal nanowire metals could be grown with smooth surfaces[46-48], they could reduce many of the issues associated with grain boundary induced resistivity increases and sidewall roughness scattering, as illustrated in the Interconnect Cu Resistivity chart in the Interconnect chapter. Research is needed to demonstrate the feasibility of the following: self-assembled nanowires with smoother surfaces and reduced surface scattering; hydrogen passivation to reduce the diameter dependence of resistivity, diffuse surface scattering, and the grain boundary scattering in polycrystalline nanowires.

Successful copper replacement materials must provide lower resistivity and higher electromigration resistance than copper, at the same dimensions. Potential interconnect replacement materials, such as carbon nanotubes for vias and interconnects and possibly single crystal copper metal nanowires for interconnects, must overcome significant challenges to warrant insertion consideration as identified in Table ERM12.

7.3. Low K Interlevel Dielectric

As identified in the interconnect chapter, to realize lower κ effective interconnects, mainly two different approaches are being pursued 1) pore introduction into ILDs and 2) air gap ILD. Porous low-κ materials exhibit low dielectric constant as low as 2.3 due to low density and pore sizes in the range of less than several nm. Reducing κ value below 2.0 is possible but requires increasing the pore volume in ILDs; however, integration issues such as mechanical properties, process compatibility, and moisture absorption, limit their adoption in manufacturing. In order to overcome these issues, alternative molecular designs should be investigated. The second approach is air gap ILD with a κ value close to 1.0. Two typical methods for fabricating air gap interconnect are described below. One is non-conformal CVD deposition on metal lines with materials between them partially or completely removed, and another is damascene metal lines with an embedded sacrificial material which can be selectively removed through a dielectric cap. One of critical challenges in air gap interconnects from the view point of materials is developing sacrificial materials. A summary of the low κ dielectric challenges is included in Table ERM11.

In order to reduce dielectric constant of ILD materials, polarizability per unit volume needs to be decreased. For polarizability reduction, one existing method is lowering density of the film and other is using chemical structure having low polarizabilities, and combinations of these two methods are also studied. As a low density ILD material, silica-zeolite is a possible candidate[49], which exhibits low-κ characteristics due to a porous structure in its silica skeleton, and high mechanical strength due to a three dimensional silica network. Polycarbosilane-based dielectrics with Si-C bonds have smaller dipole moments than Si-O bonds with nonporous films had dielectric constant as low as 2.3[50] and excellent resistance to Cu diffusion under a standard bias temperature stress test conditions. This fact indicates that interconnect structure without barrier metals can be formed by polycarbosilane low-κ dielectrics as ILD, and low resistive Cu wiring can be realized due to barrier-metal-less wiring structure. With smaller volume of pores, κ-value of polycarbosilane may become lower than 2.0. Another low polarizability chemical structure was reported for nonporous fluorocarbon film deposited by plasma enhanced chemical vapor deposition using C_5F_8.[51] The dielectric constant of the films is less than 2.0, and the elastic modulus is higher than 8GPa. Moreover, the fluorocarbon films exhibits excellent adhesion to SiCN barrier dielectric and low leakage current density measured by a current density-electric field characteristics. This film also has a good thermal stability arising from preventing overdecomposition of C_5F_8 gas which results in volatile CF radical generation.

Airgap formation using sacrificial materials is another candidate for realizing low κ effective interconnects. Although the materials are common polymers, the application is new and the potential impact on other interconnect ERM could be significant. Sacrificial polymers must decompose cleanly for forming airgaps without any harmful residues, and be

compatible with Cu wiring fabrication before airgap formation. A sacrificial polymer based on poly(cyclohexyl methacrylate) formed by initiate chemical vapor deposition left less than 0.3% residue[52] when annealed in a nitrogen ambient with a thermal decomposition temperature of 270°C, which may be compatible with Cu interconnects. By using Poly(neopentyl methacrylate-*co*-ethyleneglycol diacrylate) copolymer, onset temperature can be adjusted from 290°C to 350°C with removal percentages varying from 93% to 98%.[53] The sacrificial materials exhibit adequate elastic modulus (3.9-5.5GPa) and high onset decomposition temperatures compatible with Cu interconnect fabrication. Process simplification is needed to enable this technology and this would place additional requirements, such as stress migration on the other interconnect materials. The Cu and barrier layers must have good adhesion to the air gap polymer, but must also provide mechanical constraint and electromigration resistance.

8. ASSEMBLY AND PACKAGING

Key challenges for future assembly and package technologies are to provide a controlled stress package that meets electrical and thermal requirements and is reliable through assembly and product life. Future technologies will require complex packages to electrically connect the boards and other components and with the ability to protect them from stresses, moisture, and other environmental stresses and cost effectively. ERM including nanomaterials, macromolecules, and complex metal oxides may provide solutions to these future requirements, but they must overcome a number of challenges identified in Table ERM13. (3D package and system in package overlap with interconnects) Highly coupled and shared problems and solutions.

Table ERM13 Assembly and Packaging ERM Challenges

8.1. MATERIALS FOR 3D INTERCONNECTS

3D interconnects need materials to support a thermal hierarchy of assembly, both solders and polymers, and polymers with high thermal conductivity to spread heat from local hot spots in a chip. The solders will be described in the next section, polymers will discussed later and high thermal conductivity will be discussed in the nanotube thermal section (8.3.2).

8.1.1. MATERIALS FOR LOW TEMPERATURE AND HIERARCHICAL ASSEMBLY

To support assembly of "system on a package" and high performance flip chip packages a hierarchy of lower assembly temperature solders is needed. For system on a package, lower melting point solders are needed to initial mount components and keep them mechanically in place when other components are attached and alloyed with all solder joints form high reliability joints on a final cure. The initial low temperature solder joints need to provide mechanical strength through the following higher temperature reflow operations. For high performance flip chip packages, lower temperature assembly is needed to reduce stress thermal expansion stress. The move to Pb-free electronic packaging, has resulted in the use of higher melting point (>30ºC higher) Pb-free solders, such as those based on the Sn-Ag-Cu (SAC) family, and these have higher mechanical modulus and lower wettability to common surface finishes. Due to the higher melting point and higher mechanical modulus of these solders, this increases the thermo-mechanical stresses in the package. Key emerging research challenges are to identify novel interconnect materials that exhibit potential for addressing these issues, associated with SAC alloys, and provide for lower temperature and stress electronic packaging processes. A few novel materials have been identified, including nano-solders based on Pb-free alloys and electrically conductive adhesives. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements.

For lower temperature flip chip assembly other options under investigation include: Conventional low temperature soldering using the Sn-Bi or Sn-In family of alloys, flip-chip packaging with all-copper connections to replace soldered copper interconnects[1], and carbon nanotube based first level interconnections. Each of these potential options faces significant challenges. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements

8.1.1.1. *NANOPARTICLE BASED SOLDERS*

For many metallic nanoparticles, e.g., Cu, Sn, In, Bi, Ga, Au, it has been shown[2] that their melting points and latent heats of fusion decrease with particle size. This behavior is attributed to the surface pre-melting characteristics, due to their increased surface to volume ratio, which is a key factor in determining the melting behavior. Solders based on low-melting point nanoparticles, could be useful for low-temperature electronic packaging assemblies, forming relatively compliant interconnects. However, their current-carrying capability, electromigration resistance, and scalability remain to

be understood. For example, it has been demonstrated[3] that SnAg based nano-solders, with an average particle size < 10 nm, showed a melting point reduction from ~225ºC for bulk material to 194ºC. The corresponding 10nm SAC alloy melting point was reduced to 199ºC). The key challenge to synthesizing solder nanoparticles is to prevent oxidation, which can be reduced by surface passivation. Surfactants de-bond/decompose at the low temperatures to form an initial "half-solder joint." The final solder joint can then be formed in the conventional reflow process. While this may meet the needs of some applications that require an initial low temperature solder attach followed by higher temperature cure, most package applications need the lower temperature solder to produce a good solder joint. The key challenge for nanoparticle based solders is to identify novel techniques, including optimizing nanoparticle size and surfactant chemistries to enable a complete low temperature solder joint formation process.

It is critical that experiments be completed to determine the mechanical strength of the "fused" solder joint after the initial joint is formed to determine whether it is robust enough to support assembly of multiple chips. It is also important to characterize the kinetics of joint annealing with subsequent processing and determine how the mechanical properties of the final joint are affected by this. Further, it is important to determine whether shrinkage of the nanosolder joint occurs through the assembly process. It will also be important to characterize the electromigration of completed nanosolder joints.

8.1.1.2. *ELECTRICALLY CONDUCTIVE ADHESIVES*

Electrically conductive adhesives (or ECAs) represent another family of emerging research material under consideration for low temperature assembly. ECAs contain metallic nano-fillers, typically Ag and Ni flakes, embedded in an epoxy matrix.[4] These embedded materials can be cured at much lower temperatures than solder reflow temperatures, ~175ºC, between the two surfaces requiring the interconnection. Key challenges for implementing isotropic or anisotropic ECAs include: Unstable contact resistance, due to formation of metal hydroxide or oxide on the nano-flake surfaces during aging, poor impact performance, lower electrical and thermal conductivity, poor current carrying capability, and metal migration compared to Pb-free solders. Additionally, materials innovation is needed to improve drop strength, (improved polymer adhesion), electro-migration resistance, integration compatibility that enables a scalable, reliable package level interconnection technology.

8.2. POLYMER MATERIALS FOR FUTURE PACKAGING

Polymers are used in a wide number of assembly and packaging applications including as adhesives for a wide range of applications, underfill materials, molding compound, thermal interface materials, and others. These polymers must protect the integrated circuit and interconnects from mechanical, thermal, and environmental stresses while providing the required functional performance through the life of the product. It is critical that materials be developed that block diffusion of water into the package and make it immune to mobile ions. In addition, these materials must have one set of properties during application, a different set in process, and then the final product properties. Unfortunately, many of the properties are coupled with current materials, so adding a material to change one property often has a detrimental effect on other properties. A critical challenge is to identify materials additives that can modify polymer properties independently.

8.2.1. PACKAGE POLYMER PROPERTIES

New packaging related polymers are needed to meet the requirements of future technologies. For most applications, these polymers primarily serve as an adhesive layer that provides moisture protection and mechanical properties including coefficient of thermal expansion (CTE), modulus, fracture toughness, and adhesion to other materials. Additionally, it also must provide application specific properties such as dielectric constant, for high κ and low κ applications, electrical resistance, and thermal/ electrical conductivity. If low thermal resistance is required for a composite polymer, the interfacial thermal resistance between the thermal conducting materials and the other materials interfacing to the polymer must be very low.

Future underfills will need to accommodate smaller gaps between the chip and package. Capillary underfills will require polymers with lower viscosity in application, good wetting to multiple surfaces, low shrinkage during cure, and low CTE (10-14 ppm) post cure. Current approaches to achieving the low CTE often increase viscosity, but nanomaterials may offer the opportunity to add small amounts of fillers, and meet the CTE without increasing viscosity. Research is needed into techniques to effectively integrate nanomaterials into epoxy systems and modify CTE without degrading viscosity in application and adhesion. Alternate approaches to underfill such as wafer level adhesives need to have low CTE and good adhesion to solder, polymers and the other materials, but not shrink upon cure. Again research is needed in integrating nanomaterials that will enable low CTE, low shrinkage thermoset polymers and not interfere with solder joint formation.

Molding compounds will need to support a wide range of applications from high performance stacked chips to flexible electronics, such as smart cards. With increased use of flip chip molding compounds will be needed to underfill the gap between the chip and substrate as well as encapsulating the chip, so viscosity in application and adhesion to all surfaces will be important. Innovation is also needed for materials with designed properties including flexibility to avoid cracking from bending stresses with thin silicon, compatible CTEs between silicon and the flexible substrate, and strong adhesion to IC materials. A critical need is to develop materials and methods to block the diffusion of water and mobile ions into the molding compound. Water and mobile ions are very detrimental to the reliability of packages and products, so eliminating their absorption by he molding compound is critical.

For wafer or die level and stacked chip packaging, adhesives are needed to provide a stress absorbing attachment between silicon and other die materials, and exhibit a low shrinkage, low CTE, low modulus and low dielectric constant and in some cases has a high lateral thermal conductivity. Again, research is needed integration of nanomaterials into thermoset polymers to independently modulate mechanical, thermal and moisture absorbance.

Nanotechnology provides benefit in terms of multi-functional nano-composites, with simultaneous and step-function improvements in properties and novel property modifications.[5] Such composites may find potential applications in future mold compounds, under-fills, or die attach materials. Decreasing particle size helps to lower the composite CTE.[6] Another benefit of nano-composites is their potential for decoupling stiffness and toughness. However, persistent challenges with processing and dispersion (intercalation-delamination) remain barriers to nanocomposites realizing their full potential. Filler surface chemistries, such as: epoxy, acids, amines, and siloxanes onto silica-like fillers can play crucial role in achieving in matrix filler intercalation and dispersion. Once the fillers are well dispersed and intercalated (bonded) with the matrix, they act as temporary cross linkers during deformation, thereby improving toughness and preventing or diverting cracks. If well bonded, the fillers may move with the polymer chains during deformation. While the resulting nano-composites express only a marginal increase in modulus, they also exhibit a significant increase in toughness, with lower CTE. The addition of oxide fillers has shown increase in composite surface energy, thereby improving adhesion. However, research is needed to understand the fundamental factors that enable this improvement in adhesion.[7] The grand challenge, as identified in the 2007 ITRS ERM chapter, is the concurrent requirements of achieving low CTE, low modulus, high fracture toughness, high adhesion, and lower moisture absorption.

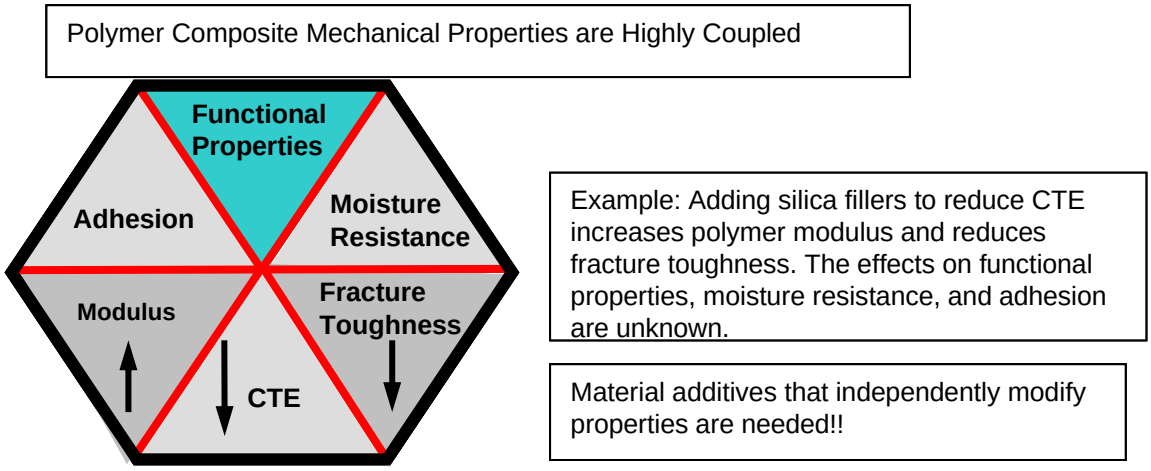

Figure ERM1 Polymer Composite Materials' Coupling Example

Package polymers must simultaneously meet mechanical and moisture resistance requirements and functional properties such as resistance, dielectric constant, thermal conductivity. In current approaches, the properties are highly coupled so addition of fillers to decrease CTE is often detrimental to the other properties. Research is needed to determine whether nanomaterials can be added into the polymers to independently modulate many of these properties.

8.3. Low Dimensional Materials for Future Packaging

8.3.1. NANOTUBE INTERCONNECTS

The 2007 ITRS ERM chapter introduced low-dimensional materials, such as carbon nanotubes, as potential candidate materials for electro-migration resistant chip interconnects. However, several key challenges were identified for these materials, such as: 1) Packaging compatible assembly processes; 2) demonstrating the required electrical resistance and reliability, including interface electro-migration, and 3) low assembly cost.

While the challenges remain daunting, research is underway to explore two potentially packaging compatible nanotube assembly methods, which include: 1) *in situ* low temperature (< 300°C) nanotube growth, or 2) remote synthesis of nanotube arrays, which are subsequently transfer to substrate. In the first approach, growth temperatures as low as 350-500°C have been reported.[8] The second approach has demonstrated an increase in MWCNT density to 50% of the theoretical value [9], and been successful at transferring CNT bumps to a package [10].

A critical challenge is the high contact resistance associated with nanotubes. Certain metals, such as Pd, Rh are known to lower contact resistance with nanotubes, by matching of work functions.[11] Modeling reports[12] suggest that high nanotube densities must be achieved to satisfy the projected contact resistance requirements. Thus, future efforts need to be geared towards growth of high density nanotube arrays, with low contact resistance metal contacts.

8.3.2. NANOTUBES FOR PACKAGE THERMAL MANAGEMENT

The 2007 ITRS ERM chapter also introduced nanotubes and other low dimensional materials as potential thermal management candidates for future package applications. The intrinsic high thermal conductivity of nanotubes justifies their consideration as potential candidates for thermal interface materials. The key challenges that must be overcome for this material to be viable include: 1) Lower thermal contact interface resistance and 2) a high density of nanotubes that provide a direct thermal path between the heat source and the heat sink. Nanotube density and adhesion with Si or Silicon dioxide, through a metallic interface, needs to be optimized for the best thermal performance.

3D packaging also needs to have thermally conducting polymers between some of the chips to spread heat and minimize local heating of the adjacent integrated circuits or memory arrays. Thus, in this application, incorporating CNTs in high density laterally in a polymer is important. The polymer must also have good adhesion to the components and low modulus and low coefficient of thermal expansion.

8.3.3. ADVANCED THERMOELECTRIC NANOMATERIALS FOR PACKAGE THERMAL MANAGEMENT

Thermoelectric cooling offers the potential for satisfying projected thermal management requirements of advanced semiconductor packages. The thermoelectric cooling ability is estimated by the non-dimensional figure of merit ZT that has hovered below 1 until recently when a spike has been seen in semiconductor nanostructures.[13] Values of ~1.3-1.6 have been reported for PbSeTe/PbTe quantum dot superlattices.[14] The highest reported ZT (~2.4) so far has been in nanostructured thin-film superlattices of Bi_2Te_3 and Sb_2Te_3[15] and devices based on these systems were recently demonstrated.[16] While these new nanomaterials show some promise for enabling extensible thermal management of semiconductor packages significant challenges remain. These include contact parasitics that emerge whenever a device is fabricated and which severely degrade the intrinsic cooling potential of these nanomaterials.

8.3.4. HIGH PERFORMANCE CAPACITORS

High speed, high power density capacitors are needed for power isolation in high performance logic. Future power isolation capacitors need to work at GHz frequencies and deliver high amounts of current quickly. Materials needed to support this are high dielectric constant materials, low resistance interconnects, and fabrication of the structure with a small spacing between the electrodes. The highest dielectric constant materials are complex metal oxides which are discussed in the Device Materials Section and have challenges with cation and oxygen vacancies reducing reliability. Nanotubes and nanowires described in the interconnect section have potential as low resistance interconnects, but the largest issues will be in developing low cost techniques to assemble the electrodes in close proximity with a low resistance structure. Potential options would be to use directed self assembly of the electrode materials and the high dielectric constant capacitors, but this would require the materials to also have low defect densities when integrated.

9. ENVIRONMENT, SAFETY, AND HEALTH

Over the past decade, the introduction of new materials has enabled the semiconductor industry to continue increasing the density of transistors, increasing information processing performance and energy efficiency through "equivalent scaling. Examples of this include the introduction of Cu and low κ interconnects to increase interconnect speed and reduce energy losses and the introduction of high κ gate dielectric with new gate electrodes to extend transistor performance and increase energy efficiency. The introduction of these new materials into the integrated circuit also required the use of multiple new materials in the manufacturing process. The semiconductor industry faces many significant challenges to continue delivering higher density, more energy efficient, higher functionality technologies in the future and very few material options could provide solutions. Since the difficulty of introducing a new material into a technology is high, the new material would need to provide a significant performance and energy efficiency advantage over evolutionary approaches. However, in some cases all of the options have known hazards or unknown toxicological behavior. In cases where a new material can provide a compelling societal benefit and toxicological behavior is unknown, the need for research to characterize potential acute toxicity and chronic effects will be highlighted. As the materials become more viable as technology options, our industry needs to better understand technical and ESH properties and behavior so mitigation and management strategies can be developed. Study on toxicological behavior of emerging materials is steadily progressing, and needs to be pursued in parallel with material research and development. Technological demand will make speed of development of new material and finding new use of conventional material even faster. A more comprehensive sustainable approach should include capacity building of researchers, risk management strategy, and life cycle assessment of emerging materials for managing ESH issues.

To identifying when new materials are becoming more viable for providing solutions, the earliest potential insertion timing table (ERM 14) has been developed in collaboration with the other technology work groups. The goal of this table is to highlight when research is needed to identify potential hazards for new materials and structures. As can be seen in Table ERM14, earliest potential time varies greatly depending on the application with potential applications in 3-5 years for carbon and metal nanotubes, oxide nanoparticles, macromolecules, and self assembled materials. Assembly and Packaging has potential applications for carbon and metal nanotubes in this timeframe in embedded applications. Oxide nanoparticles may have application as package polymer additives in Assembly and Packaging. Metal nanoparticles may have potential applications as nanosolders to provide lower melting point solders for attaching chips to packages or other chips; however, after assembly processing these materials would be converted into "bulk" materials. Novel macromolecules have potential for application in process chemicals and photoresist in Lithography. Self assembled materials could also be used in embedded package applications to provide high energy density capacitors. These are viewed as the potential earliest insertion times for the ERM and the longer term applications are described in the appropriate sections of this chapter. This table will be updated in future ERM Roadmaps.

In cases where the potential hazards of ERM are unknown, the ITRS encourages researchers to use conservative handling procedures to limit exposure of workers and the environment.

Table ERM14 ITWG Earliest Potential ERM Insertion Opportunity Matrix

10. METROLOGY

Metrology is needed to characterize the composition, properties, and the 3D structure of emerging research materials (ERM), at nanometer dimensions and below. Also needed are non-destructive methods for characterizing embedded materials, interfaces, and defects, as well as platforms that enable the simultaneous measurement of complex nanoscopic properties. Among the many high level challenges are the need to monitor local variation at nanoscale dimensions while providing this information across a large area such as a 300 mm wafer. The Metrology Roadmap continues to emphasize the need to link modeling and simulation studies with metrology, so as to help bridge the gap between nanoscale characterization and metrology capable of monitoring properties across a large area.

One of most overlooked challenges in metrology is need for valid nanoscale materials property values for use in metrology. For example, the optical properties of top layer of SOI depend on the thickness of the film thickness below 10 nm. Furthermore, recent data show that measured properties for such films also depend on the properties of layers deposited above the top SOI film. This dimensional and materials stack dependence points to the need for developing databases of these properties with entries for critical materials stacks. In some instances, it seems that both carrier and phonon confinement impacts numerous properties including dielectric function (complex refractive index), carrier mobility, thermal transport.

10.1. CHARACTERIZATION AND IMAGING OF NANO-SCALE STRUCTURES AND COMPOSITION

To enable improvement of new materials for integration into nanometer scale structures, metrology is needed to characterize the atomic structure and composition of a wide range of complex materials. These materials include III-V semiconductors, low atomic weight (z) materials such as carbon nanotubes, 2-dimensional materials such as graphene, boron nitride, MoS_2, etc.. Additionally, nanostructured materials such as nanowires with multiple compounds, dielectrics, metal interconnects, spin materials including dilute magnetic semiconductors, complex metal oxides and doped transition metal oxides also require metrology for their characterization.

Nondestructive in-situ measurement methods are needed that offer real time characterization of material nanostructure, composition and orientation, whilst also allowing for correlation to macro properties. For example, there is a need for precise doping control, as a few misplaced dopant atoms can induce significant variability in the device performance of nanoscale circuits and systems, but deterministic fabrication may enable tighter control of functionality and novel devices. The work on these emerging materials could benefit from the standardization of electrical characterization methodologies, to enable direct comparison of the data from various laboratories.

10.2. METROLOGY NEEDS FOR INTERFACES AND EMBEDDED NANO-STRUCTURES [1,2]

The ERMs under consideration for device or interconnect applications will be integrated with other materials that form interfaces; the resultant nanostructures are predominantly surfaces, with little or no bulk. The understanding and the control of the atomic structure, composition, interfacial bonding, defects, stress, and their effect on nanoscopic properties is critical. For embedded contacts and other heterostructures, the ability to nondestructively characterize the structural and electronic properties and stability of these interface structures is very difficult but important. 3-D Metrology of the atomic architecture, as well as the polarization and electronic states at these interfaces will enable our understanding of whether interface states are affecting their operation. Current subsurface / buried interface imaging and measurement techniques are cumbersome / complicated and are marginally adequate for understanding interface phenomena and many current techniques are destructive, since they require cross-sections. The challenge of understanding these environmentally sensitive properties requires for the development and application of appropriate nondestructive 3D characterization tools and methods. In addition, as alternate state variables are explored for beyond CMOS, there is a need for correlated, multimodal microscopies to maximize information return from nanoscale objects and interfaces. Here techniques are combined, simultaneously or asynchronously, through nanoscale registration techniques to characterize properties such as electron and spin concentration and alignment. In addition, modeling is needed to separate the probe-specimen interactions to determine the unperturbed interface structure and properties.

CHARACTERIZATION OF VACANCIES AND DEFECTS IN NANO-SCALE STRUCTURES [3]

The properties of most nanostructured materials are dramatically affected by small concentrations of vacancies and defects. Therefore, the ability to accurately map vacancies, defects, dopant atoms, and interface structures, in 3-D, may be needed to enable future emerging device options. In the case of CMOS or alternate channel transistors, statistical changes in dopant distribution cause variations in threshold voltage distributions. When interfaces are formed between materials, bonds can be broken, defects are generated and they diffuse into the structure. For example, in the case of graphene and carbon nanotubes, a local C-H bond or missing carbon atom can change the electronic properties of the system. Alternatively, functionalization also can result in the formation of vacancies, or rehybridization of the carbon that introduces states in the gap. Such material perturbations can dramatically change these materials' electronic or thermal properties. Complex metal oxide properties, including electrical, ferroelectric, and ferromagnetic, also are strongly affected by the presence and location of oxygen vacancies, since they create local distortions of the crystal structure that can break symmetry and induce different and uncontrolled electronic states. In complex metal oxide heterointerfaces, the interface carrier concentration can be changed by the presence of oxygen vacancies. Process induced defects and microstructure of individual nano-magnetic tunnel junctions (MJTs) have been correlated with the transport properties. A unique set of defects and microstructure can be correlated to transport properties, including energy barrier, from individual nano-magnetic tunnel junction (MTJ) devices. [4] The challenge will be to detect the positions of small concentrations of vacancies and defects in nanometer scale structures. In addition to the identified need for developing enhanced microscopy capabilities, other physical measurement methods also should be improved so that the relationship between defects and properties can be measured, quantified, and understood.

10.3. WAFER LEVEL MAPPING OF PROPERTIES OF NANO-SCALE ERM [2, 5-8]

New and existing materials, such as MoS_2, are being studied in the context of electronics applications[9], which still require characterization. The ability to measure and map properties of a large number of low-dimensional materials is needed to

support improvements in materials synthesis for a wide range of potential applications. Such synthetic advances depend on the reproducible production of high-quality materials, and rapid methods for characterizing the structure, purity, and properties of such samples. For example, some methods for growing graphene tend to yield varying numbers of graphene layers [6], and samples with various defects [7]. While spectroscopic techniques have distinguished between graphene monolayers, bilayers, and bulk graphite [8], rapid predictions of the number of 2-D layers of materials, such as graphene, MoS_2 and boron nitride, or the presence of defects are needed. Robust fabrication requires an ability to map bandgap distributions, preferably in-line, across a wafer, to identify those regions with properties outside of the target, and assess the interaction of graphene with the underlying substrate. While some techniques, such as Raman spectroscopy, fluorescence and other spectroscopic techniques, are sensitive to the local chemical environment, alternative options are needed to support the local electronic characterization of these materials. Emerging characterization methods require further advancements that are appropriate for specific potential application opportunities, especially with respect to improving the balance between measurement speed, accuracy, and precision.

10.4. METROLOGY NEEDS FOR SIMULTANEOUS SPIN AND ELECTRICAL MEASUREMENTS [10-15]

Multiple beyond CMOS devices are based on control of spin as an alternate state variable including spin transfer torque magnetic random access memory (MRAM), nanoscale spin transistors, spin wave devices, hybrid-ferroelectric/ magnetic structures, and other spin-based logic concepts[10]. These types of emerging nanoscale spin-based devices and materials have characteristics and properties that do not exist in conventional CMOS devices, which are based on the transport of charge. The specific challenges for spin materials that need advanced characterization include the atomic scale imaging of domains, the dynamics of domain wall motion, the interface conditions needed for efficient and fast spin injection from ferromagnetic to semiconductor materials, and the measurement of spin transport and lifetime. Measurement and imaging techniques for magnetic materials characterization have been recently summarized [14]and include scattering based techniques (neutron, x-ray, electron, and photon) and proximal probe techniques (force microscopies, spin-polarized STM, scanning near-field magneto-optic microscopy). More recently, magnetic circular dichroism (XMCD) has been used to image domain wall motion in multilayer film stacks [15]. Electron scattering methods for domain imaging include Lorentz imaging in the transmission electron microscope and polarization analysis in the scanning electron microscope (SEMPA). Scanning near-field optical microscopy is being developed to measure Kerr rotations at the nanometer scale. Work function lowering effects are being measured by photoelectron spectroscopy. Magnetics resonance force microscopy (MRFM) is being used to detect individual electron spins[16] and for looking at buried devices. This technique could be quite useful for investigating failed devices

Efforts are underway to develop measurements of switching with ~10^7-10^9 statistics. The work shows that the switching tails are issues for times <50 ns. Both experiments and simulations show qualitatively similar results. In particular, the write error rates as a function of pulse voltage amplitude increase at higher rates for pulse durations below ≈50 ns. Simulations show that the write error rates can be reduced only to some extent by the use of materials with perpendicular anisotropy and reduced damping, whereas non-collinear orientation of the spin current polarization and the magnetic easy axis increases the write error rates. The cause for the write error rates is related to the underlying physics of spin-torque switching and the occurrence of the stagnation point on the magnetization switching trajectory where the spin-torque disappears and the device loses the energy needed to switch. The stagnation point can be accessed either during the initial magnetization distribution or by thermal diffusion during the switching process.[17] Therefore, characterization of buried interfaces in metallic/tunnel junction structures is needed. There is also a need to understand how nanoscale structures interact with their environments, for instance, in high speed measurements, thermal noise is not simply averaged out.

Low power dissipation and non-volatility requires that spins interact weakly, to preserve coherence (classical as well as quantum). Defects degrade spin coherence through single defect fluctuations; we need to understand the interplay between spin coherence and defects.

Efforts are being made to develop ferromagnetic insulator tunnel junctions for generating spin currents directly in silicon thereby bypassing interface and impedance matching problems. This entails, among other things, using isotropically enriched ^{28}Si materials. ^{28}Si has no net nuclear spin and does not interact or interfere with the T2 coherence time of the electron or nuclear spin being used as a qubit.[18]

10.5. METROLOGY NEEDS FOR COMPLEX METAL OXIDE SYSTEMS [19-24]

Correlated oxide systems, such as multiferroics, have competing and coupled charge, spin, orbital and lattice degrees of freedom, result in the formation of new electronic and magnetic phases. These materials have the potential to enable new device concepts that could couple electric and magnetic spin alignment for spin logic novel memories. It has been shown that the domain walls possess unique functionalities not inherent in the parent multifunctional material, such as being

electrically conductive 19. For these electrically conducting interfaces to be useful, their nucleation and positioning must be understood and controlled reproducibly 20. Piezoforce microscopy may be useful for characterizing static and dynamic properties of ferroelectric and piezoelectric materials at the nanometer scale 21. The coupled phases have been found to be sensitive to cationic disorder and vacancies, so metrology is needed to characterize these, and correlate them to the electric, magnetic and orbital order.

10.6. METROLOGY FOR MOLECULAR DEVICES

New metrology capabilities such as inelastic electron tunneling spectroscopy 25, and backside FTIR 26 for the study of vibrational states, and techniques such as transition voltage spectra, 27 STM, Conductive AFM, and Kelvin Probe AFM are beginning to enable understanding of the transport through individual molecules and molecular interfaces. However, additional research is needed to develop new metrologies, such as nondestructive, in situ 3D methods, to characterize contact interactions with molecules and the electronic properties of the embedded interfaces and molecules.

10.7. METROLOGY NEEDS FOR MACROMOLECULAR MATERIALS [28-36]

New families of designed macromolecules and corresponding material characterization methods are needed to satisfy projected long term patterning requirements. For example, nanoimprint lithography (NIL) is emerging as a potential patterning solution beyond 22 nm. This technology faces several performance challenges related to the templates, release layers, and resist and imprinted functional materials. New metrologies are needed to assess projected critical materials requirements, such as pattern fidelity, distortions and defects, shear stresses and pattern collapse, adhesion and release behavior.

10.8. METROLOGY NEEDS FOR DIRECTED SELF-ASSEMBLY [37-44]

For directed self assembly to be viable as a lithography extension or to assemble nanostructured materials in predefined locations and alignment, metrology is needed to evaluate critical material properties, the size and location of features, and the registration to previously patterned structures. However, these sub-100 nm thick organic films are difficult to image with conventional metrology tools. For block co-polymer based directed self assembly to be a viable potential lithographic solution, robust non-destructive nanoscale measurement methods are needed that enable 3D characterization critical performance factors of the phase segregated films, which include: feature sizes, line width roughness, alignment to existing structures, engineered surface energies, anneal dynamics, and defects, etc.

Need metrology to characterize directed self-assembled structures over large patterned areas (Where defects may be displacements of structures in addition to missing or added structures). The DSA films are extremely thin (the thickness of the dimensions patterned).

10.9. MODELING AND ANALYSIS OF PROBE-SAMPLE INTERACTIONS

Nanometer scale measurement tools, such as electron microscopes or scanning or optical probes, exhibit significant coupling between the probe and sample states. Significant research is needed to develop methods for decoupling these interactions and to accurately determine nanoscopic structures and properties. Also needed are sample-probe interaction models for characterizing nanoscale structure, defect locations, composition, electronic, magnetic, and optical properties. Additionally, improved algorithms are needed to enable the extraction of actual structures and properties from the coupled signals.

10.10. METROLOGY NEEDS FOR ULTRA-SCALED DEVICES [45-48]

New metrologies and models are needed to characterize the performance and reliability of emerging nano-scale devices. Emergent nanoscopic properties will introduce new mechanisms for trading device performance with reliability. For example, the trend towards increasing percent variability with scaling, is becoming a critical challenge in achieving robust device attributes and drive the perceived lower limits for device operation. Analog circuits are particularly susceptible to decreasing signal-to-noise ratios. A thorough understanding of the sources of variability and its impact on device noise is critically needed for enabling the successful design and integration of emerging materials into nanoelectronics.[37] This foundational need will drive the development of tools for identifying and characterizing the significant emergent nanoscopic sources of variability and noise in nanoscopic systems. There is need to characterize and understand the aging of nano-materials, nanostructured devices, and the consequences of such aging on device performance since most of the existing data based on bulk material properties may not be applicable.

Nanowires for device applications have a number of unique metrology challenges. Although total resistance of nanowires is relatively easy to measure, distinguishing the various materials parameters that contribute to resistance is still difficult. The initial attempts to characterize nanowire mobility from single nanowire FET measurements included a number of

simplifications that led to large systematic errors in mobility and therefore carrier concentration numbers.[49,50] Although some of the difficulties can be addressed with analysis modeling refinements, the derivation of mobility from transistor transconductance relies on an accurate measure of the gate capacitance. Because this capacitance is typically some tens of aF, it is easily overwhelmed by parasitic capacitances in measurement systems. While some efforts are beginning in this area,[51, 52] more work is needed along with three-dimensional electrostatic modeling to support the interpretation of these measurements. A related problem is the identification of dopant atom distribution and composition. Atom probe tomography,[53] scanning probe[54] and electron microscopies[55] have been applied to this problem, but the minimum detection limits are still quite high, around 10^{18} atoms/cm^{-3} for atom probe and 10^{20} atoms/cm^{-3} for electron microscopy. Optical spectroscopy has also been useful in compound semiconductor nanowires for defect, dopant and compositional identification.[56]

10.11. METROLOGY FOR ERM ENVIRONMENTAL SAFETY AND HEALTH

Metrology is needed to detect the presence of nanoparticles in the workplace and in the environment. Understanding nanomaterials' behavior in the workplace and environment is required to establish good risk assessment and material management practices (i.e. selecting appropriate protective equipment, ventilation equipment, etc.).

10.12. PROGRESS OF METROLOGY FOR ERM DEVICE MATERIALS

Scanning-transmission electron microscopy (STEM) with spherical aberration correction (Cs-correction) has provided a major improvement in the ability to characterize materials[57]. The effects of this device are mainly following three points.

-Spatial resolution improvement (~50pm) with minimization of the electron beam diameter (less than 0.1nm) with improved spatial resolution.

-Realization of high sensitive / high TAT elemental or state analysis by increasing of the electron beam current

-Achievement of ultra-high resolution analysis at low acceleration voltage which reduced the electron beam irradiation

By combination of these advantages, for example in complex oxides, elemental mapping at the heterointerface in the atomic column level has been achieved[58]. In the nanocarbon materials, not only direct observation of carbon atom which form a six-membered ring, but also the direct observation of the random structure of the edges of graphene nanoribbons has been achieved[59]. Metrology needs at atomic level observation have been satisfied by the scanning transmission electron microscope with Cs-correction.

In addition, three-dimensional atom probe (3DAP) has been well-utilized for various ERMs by introducng a femtosecond laser to assist the ionization of atoms.[60,61] It is expected to be applied to samples that possesses very little amount of dopant atoms such as deterministic-doped materials and devices with three-dimensional structure such as a Fin-FET which cannot be analyzed by conventional SIMS.

Recently, SPM (AFM) with the ultra-fast scanning operation[62,63] has realized 5 to 20 times faster scan speed compared to conventional tools. One can use the SPM in the similar sense of SEM and optical microscope, namely. The newly developed SPM overcomes the problem of the low TAT of SPM. Crystallization of the polymer and movement of molecules were captured almost at real time.

10.12.1. MAGNETIC TUNNEL JUNCTION (MTJ) METROLOGY

In MTJ technologies, various efforts have been paid to improve the characteristics. In particular, the interface structure MTJ (the tunnel insulating film MgO and magnetic film above and below of MgO) should be evaluated in the atom level. The typical issues are shown below.

-Evaluation of crystal orientation of the magnetic film and MgO film

-Observation of magnetic domain structures in magnetic film and changes of them under device operation (real-time observation of domain wall motion)

-Elemental diffusion at the interface between MgO and magnetic film (in particular, the diffusion of B in the case of the CoFeB magnetic film)

-Identification of the ordered structure and the degree of ordering in magnetic film in the case of magnetic film is long-period ordered alloy

-Atomic arrangement at the interface between magnetic film and MgO (identification of kind of metals in contact with the film MgO, for example whether Fe or Co)

Since the MTJ is composed of ultra-thin multilayered films, it is very difficult to analyze them in the atom scale. STEM with Cs-corrector can contribute to the investigation. By using high-resolution HAADF-STEM and EELS / EDX elemental mapping at the atomic column order, there is a possibility to solve the issues listed above. Actually, Miyajima et al differentiated the ordered phase ($L2_1$-type) from disordered phases (B2-type) in the CoMnSi magnetic film by high-resolution HAADF-STEM observation.[64] Lorentz microscopy has become to operate in STEM with Cs-correction mode. The electron beam interferometric method combined with electron holography and Lorentz microscopy mentioned above should be developed for dynamic observation of the magnetic structures.[65] 3DAP analysis enables us to obtain the atom-level element profiles in the MTJ stacked structure. These profiles will be useful for the design of MTJ and the process optimization.

10.12.2. REDOX RAM METROLOGY

It is indispensable to observe directly at the interface where the redox reaction plays a crucial role of the Redox-RAM's operation. It is essential to evaluate the distribution of oxygen vacancies and the change of the valence state of the metal element contained in metal oxides. The possible candidate to investigate them is STEM-EELS with Cs-correction. However, the electrode material and the metal element in the complex metal oxides currently being used are heavy metals, and EELS has poor sensitivity for such materials. In addition, HfO2, which is a candidate of metal oxide, has been known to change the chemical state by the thinning (using ion-beam processing) prior to electron microscopy analysis and the electron beam irradiation. To find the solution to prevent the change is very important for the quantitative investigation. By the detection of soft X-ray from materials under the electron beam exposure, the electronic states (valence band density of states) of the materials can be investigated with the high sensitivity (X-ray emission spectroscopy: SXES).[66] This technique will be the strong tool to study the Redox-RAM operation.

10.13. LOW-K/CU INTERCONNECT METROLOGY

Due to the increasing fragility of the low-k dielectric materials being introduced into Cu interconnect structures, accurate measurements of the thermal-mechanical properties of all the materials in the interconnect stack are needed including the low-k ILD, Cu capping/Etch Stop layer, Cu barrier layer, and Cu as well as materials that may be utilized in patterning the low-k ILD such as dielectric or metal hard mask layers. The mechanical property typically of most interest within the industry is Young's Modulus and is most commonly determined by nanoindentation (NI). However as metal layers continue to shrink, the thickness of most layers in interconnect structures are thinning to levels that can represent the entire indentation depth of a typical NI measurement. For this reason, new methods for determining the Young's Modulus of thin films in the range of 2 – 50 nm are needed [67]. Continued advancement of NI techniques for this purpose should be explored. However, other techniques such as surface acoustic wave spectroscopy (SAWS) [68], Brillouin Light Scattering (BLS) [69], and contact-resonance AFM (CR-AFM) [70] deserve more attention and development as a metrology for not only R&D but manufacturing and failure analysis as well. In addition to characterizing Young's Modulus for blanket nano-scale films, the industry would also benefit from the capability to measure this property in integrated structures and monitor how this property changes as materials are integrated together (particularly for low-k ILD materials) [71]. In this regard, CR-AFM and related techniques are of great interest due to the ability to perform these measurements with nm spatial resolution directly on the structures of interest.

Another area of need in low-k dielectric metrology is detailed characterization of the complex bonding structure in these materials. Numerous techniques exist for quantifying the elemental composition of low-k materials such as x-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), seconday ion mass spectroscopy (SIMS), and Rutherford back scattering (RBS). However, only Nuclear Magnetic Resonance (NMR) and Fourier Transform-Infrared (FTIR) spectroscopy have proven useful for qualitatively examining both the network and terminal bonding in low-k materials. Quantification of NMR and FTIR measurements, however, is extremely difficult and rare. In this regard, increased research and attention is needed for developing quantitative NMR and FTIR metrologies capable of better guiding development of future low-k dielectric and other materials. Quantitative FTIR measurements in particular would benefit from improved methods to account for coherent and incoherent multiple reflections within both the substrate and thin film as well as other artifacts related to light scattering from internal pores, interfaces or compositional variation [72].

Lastly, as new < 2nm Cu barrier materials will be needed for future technologies, new metrologies for assessing the performance of these materials will also be needed. In particular, new or improved methods will be needed for both robustly imaging and determining the chemical composition of barrier materials formed on the ***sidewall*** of trenches and vias patterned in porous low-k ILD materials. The analysis of the chemical composition of sidewall materials would also benefit research of advanced low-k dielectric materials where characterization and understanding of both low-k sidewall damage and sidewall polymer deposition forming during patterning is greatly needed.

11. MODELING AND SIMULATION

With device dimensions 22 nm or below, materials modeling or computational materials is becoming a critical part of technology development and is needed to address several components of technology development[1];

1) *Synthesis to structure & composition*, especially on the interfaces and multi-interface material structures
2) *Properties* of these structures including interface physics of state transition, defects states, etc. In addition, non-equilibrium properties of these structures such as conductance, mobility,
3) *Probe interactions* with samples to enhance quantification of structure, composition, and properties.

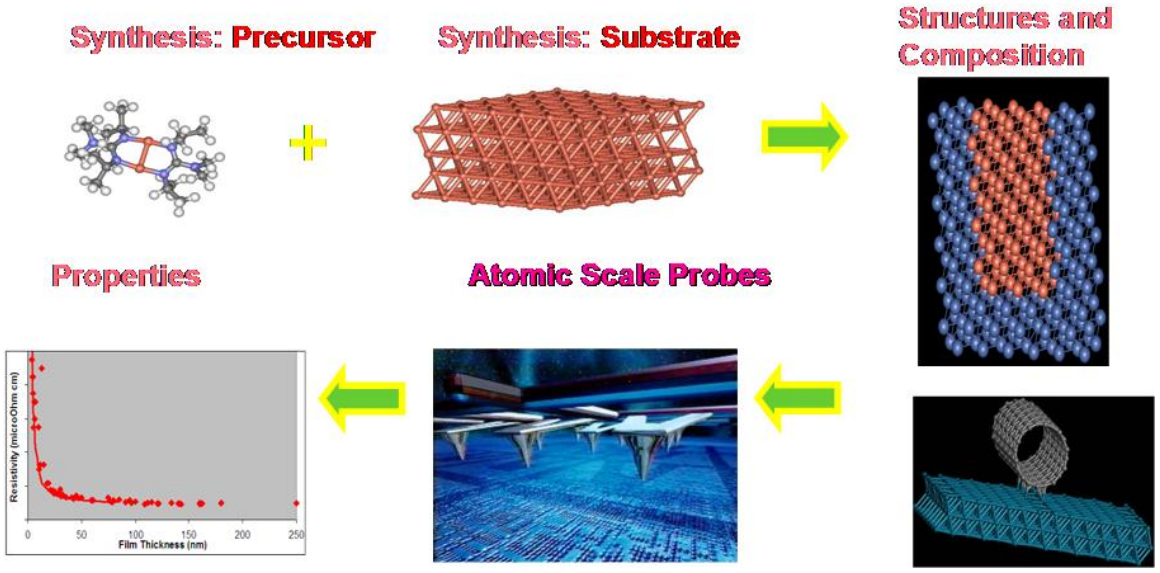

Figure ERM2 Modeling from Synthesis to Predicting Properties

Materials modeling is applied at different levels based on the accuracy and the end application requirements. All material applications require simultaneous optimization of multiple properties such as electronic, mechanical, thermal, surface chemical reactivity, etc. If the dimensions of the materials are in tens of nanometers, they are of the same order of magnitude as the domains in the materials such as grain sizes. These lead to nanomaterials possessing unique properties making them optimal candidates to enhance or replace conventional materials and approaches for new devices. However, the need for optimization of multiple properties requires models that correlate nanostructure to properties. There are multiple stages in which materials modeling can provide value in technology development. In the *first* stage during early material development, the need is to relate structure and chemistry to desired material properties. This is done in conjunction with a specific metrology and is used to characterize both structures and their properties. In addition the models are needed to optimize synthesis and transport processes including film growth. In the *second* stage, the models are applied to material improvement where they are used to optimize structure, composition, purity, and interfaces. Here as we have mentioned above, the models relate structure and composition to properties. In the *third* stage, models are used to relate material properties to the functional properties of the device. The properties of the resulting structure needed to be understood in terms of transport of electrons, phonons, and atoms. The models at this stage in conjunction with experimental observations are used to optimize synthesis and integration.

The behavior of devices and materials are directly correlated to their electronic structure and lattice physics. This is equally valid for both charge-based and non-charge-based technologies, as physical and chemical effects in these dimensions are directly related to the electronic structure. Physical modeling and numerical simulations are critical for multiple reasons;

1. *explain observed phenomena,*
2. *predict new phenomena,*
3. *direct experimental studies to desired outcomes,*

4. *interpret metrology.*

In addition, they provide fundamental understanding of both the mechanisms and the interactions between processes and materials.

Application of materials for ERM constitutes fundamental understanding and characterization of synthesis, structure, and properties. This is the natural logical flow for designing and integrating newer materials to develop structures whether it is for switching device, interconnects, or packaging. The method and conditions of synthesis determine the structure and composition of the engineered materials. Structure in turn, determines the material properties and performance. As can be seen in the following figure, models span multiple scales and need to be simulated using appropriate assumptions. The key intent of material simulation is to identify and quantify chemical knobs at the levels of atomic, nano, and thin film dimensions that modulate the behavior in the integrated devices.

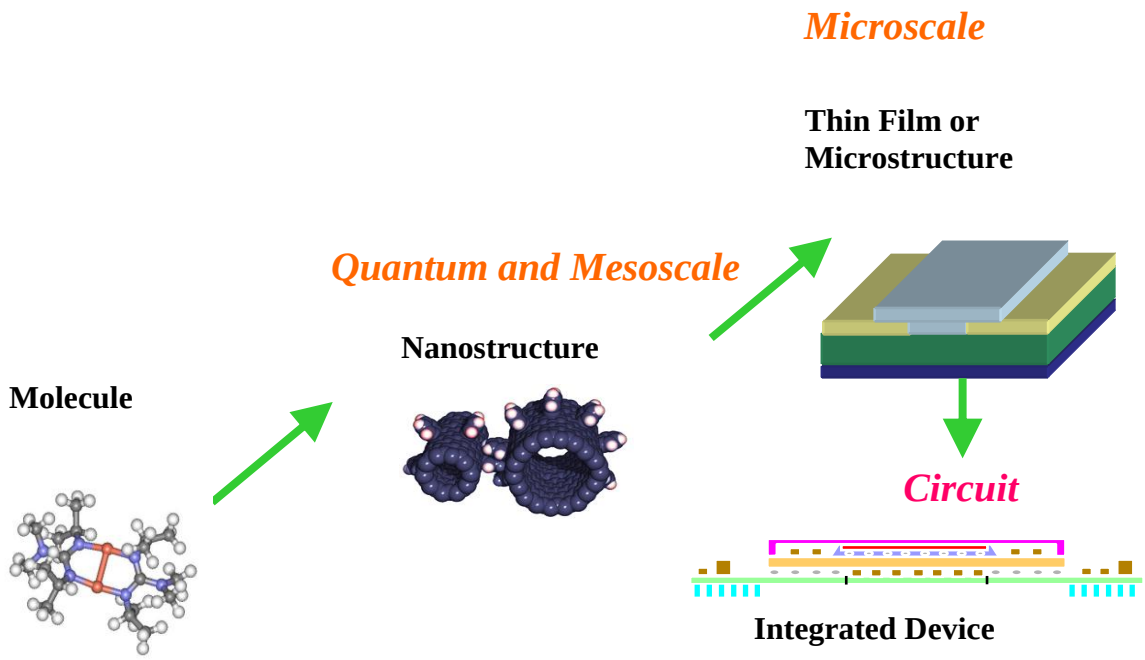

Figure ERM3 *Multi-scale Perspective in Nanotechnology where Materials Form an Important Role at Different Levels.*

The complexity of materials modeling in nanotechnology is increasing due to increasing complexity from a variety of factors.

1. ***Combinatorial System****:* Number of materials has continued to increase with the development of several new material systems including high-k/metal gate, porous dielectrics, copper interconnects, and polymer materials for packages (leading to over 3X increase in number of elements over a period of 20 years). This effect is further augmented as materials are used in combinations estimated to be 6X increase in number of material combinations over the same time period as above.
2. ***Size***: Most of the devices have dimensions close to material domain sizes (e.g. grain size, thin film thickness). As a result, the \performance of the device is determined by the material properties at their characteristic dimensions. For example. Surface scattering is estimated to dominate interconnect resisitivity for any metal as dimensions scale down farther. In addition, with scaling, ratio of surface to volume leads to interface properties determining overall behavior of devices unlike the earlier technologies where bulk properties determined the device properties. In addition, smaller number of atoms in smaller dimensions lead to larger statistical variations.
3. ***Topography***: For non-planar devices, topography of material structures modulates device behavior since the same single crystalline material may have multiple orientations dependent on the interfaces. This is further

complicated by polycrystalline or amorphous materials with grain boundaries. These in turn lead to property variations.

4. ***Topology*** of the nanostructures and molecules. Electronic and phonon densities of states are determined by the chemical bonding and electronic band structures. Since the topology determines the functional properties of devices, efforts to analyze these effects are necessary both from characterization and modeling studies. For example, carbon nanotubes and graphene sheets demonstrate large conductivities and strong mechanical properties which can be affected by their orientation and topology.
5. ***Complex Material Properties*** of strongly correlated materials cannot be easily predicted from band theory. This is because traditional Density Functional Theory fails for these classes of materials. Another associated property is the metal-to-insulator transition. The complexity of physics is due to multiple mechanisms attributed for the transition[2]

11.1. SYNTHESIS

Synthesis determines the structure and composition of thin films. To predict the material properties, we need both characterization and physical modeling of the relevant structures. The materials themselves may be crystalline, poly-crystalline, semi-crystalline, amorphous, or visco-elastic. Even in bulk materials, structure of the materials determines their behavior.[3, 4] For example, the resistivity of films in a certain crystallographic orientation (100) is different from (111) orientation. Realistic structures are not ideal single crystalline films and need advanced metrology for their complete characterization including characterization of grain morphology and size.

Materials synthesis influences the material morphology and the desired end user application. For example, nanotube growth and functionalization are determined by the chemical and electrical conditions in the reactor and the interactions with the substrate. Depending on the method of synthesis, in-situ and ex-situ requirements are different. For example, in a low pressure process, ex-situ measurement may result in oxidation and altering of the properties of the film. From a modeling perspective, a key requirement is to understand roles/mechanism of processing and the specific structure resulting from the synthesis. As an example, in atomic layer deposition, the physical model must comprehend gas phase and surface chemistry in addition to mass and energy transport. Film nucleation and subsequent growth, which determine the morphology of the nanostructure and thin films, also require modeling. In addition to description of the temporal evolution of a new phase, it becomes necessary to describe the spatial ordering in many systems (e.g. quantum dots, nano-wires[5,6]). Classical nucleation and growth concepts adequately describe phase transitions in some nanoscale phase change memory materials.[7]

Controlling the morphology of the nanoscopic material requires detailed information on phase stability and dynamics of atomistic processes. In small nanoscale systems in which dimensions may not be significantly larger than the range of interatomic interactions, classical thermodynamic concepts such as extensive and intensive properties may no longer be valid. In these cases, the classical concept of a phase transition, including the Gibbs Phase Rule that occurs in the thermodynamic limit of an infinitely large system, may not hold.[8,9] Development of a theory of phase transition in such finite size systems for understanding the dynamics of phase transition may be critical to control nucleation and growth of certain nanoscale materials. Description and prediction of fragmentation, a process by which phase transitions have been observed to occur in nanoscopic systems, presents a significant challenge in statistical mechanics. Density functional theory[10,11] which is based on density fluctuations rather than existence of clusters of classical and atomistic nucleation should investigated as a tool for describing phase transitions in small systems and fragmentation. Structures characterized based on synthesis methods serve as inputs into the physical models. Given the limited size of problems that can be solved, a combination of techniques spanning different length and time scales are needed to model structures effectively (More details are covered in the section on Modeling and Simulation).

11.2. STRUCTURE AND PROPERTIES

The material properties themselves are based on the electronic band structure of condensed matter. For a given structure, the Schrodinger equation determines chemical, electrical, mechanical, and thermal properies. In turn, the nature of the hyper-dimensional Schrodinger equation is determined by the number of electrons in the structure. As the number of electrons are very high in condensed matter (~ 10^{22} - 10^{23} in an unit cubic centimeter of material), any solution of the equation for realistic macroscopic system is generally done using one of two simplified techniques; 1) single particle approximation and/or 2) multi-scale techniques with distinct formalisms representing different scales. The models themselves have different scales based on the specific physical phenomena. Atomic or molecular scale is based on self-consistent solutions of Schrödinger equation as mentioned above. Nanostructural scale uses multi-scale techniques based on kinetic and quantum formalism (e.g. device, or interconnect with barrier layers). The thin film scale (e.g. gate oxide or

barrier layer) is mesoscale in nature, and links with kinetic models at the macroscopic level and atomic models at the microscpic level. In the macroscopic scale (e.g. die, package), bulk or effective properties are used in constitutive models that describe the response of materials to different stimuli. For the area of ERM, the main focus of research should be on the first three levels, with an emphasis on atomic or molecular and nanostructural scale. Since structural dimensions are currently targeting below 32 nm, the materials properties at this scale may behave differently when integrated than in the bulk. In addition, optimization of the performance reliability of devices or materials in nano-dimensions during ambient and accelerated usage conditions requires model extension to include phonon interactions and other long time scale processes. More details of the other scales are covered in the Modeling and Simulation section in the roadmap.

Most of the full quantum simulations or *ab-initio* simulations can be done for smaller systems up to 1000-5000 atoms, which are approximately about 30 cubic nanometers. The models which cover these domains are mostly based on quantum methods which solve Schrödinger equation in 3N dimensions, where N is the number of electrons in the system. As mentioned above, most of the devices are in condensed matter, N is of the order of 10^{22}. In addition, the computational time scales as $O(N^3)$, N is the number of particles (could be electrons or atoms depending on the approximation). This poses the problem in solvability of the equations for practical applications. As a result, the most widely used technique is the Density Functional Theory (DFT) in which the 3N dimensional system is reduced to three dimensional problems for most of the ground state problems.[12, 13] The approximations are generally of two types, one in which the density functions are systematically improved to capture more and more non-local features of the wave functions and the second one in which the exchange-correlation functional are approximated by analytical models (e.g. meta functionals). One of the most widely used approximations is the Local Density Approximation (LDA) where local densities of N-1 electrons are used to approximate the interaction potentials leading to a 3 dimensional problem. More accurate approximations such as Generalized Gradient Approximations (GGA) are used to increase the applicability of the DFT methods.

In addition, due to the complex properties of materials (e.g. Mott transition, spin-orbital coupling), many-body theories are entering mainstream in applications.[14-17] Some examples of these higher-order approximation techniques are Green's Function techniques (GW), Quantum Monte Carlo, Path Integral methods etc. These techniques model both the equilibrium and non-equilibrium properties without approximations of mean field theories as mentioned above. The first technique uses perturbation technique to comprehend many-body interactions in a self-consistent manner. The other techniques mentioned above model quantum phenomena in a variety of ways 1) Solve the Schrodinger equation using statistical methods, or 2) Use Feynmann's path integral method for directly estimating properties. All these techniques are computationally intensive and are limited in the size of the physical problems to which they can be applied.

Semi-empirical models for extending to larger systems of million atoms are characterized by a variety of techniques in which interaction energies are characterized by different potentials. The applicability of atomistic models can be increased to over 100 million atoms by using more of semi-empirical characterization like force fields. Some of the semi-empirical methods used for modeling materials include following:

1. Classical molecular dynamics which are based on interaction potentials formulated from quantum simulation. This technique has been widely applied to synthesis methods such physical vapor deposition[18] and thermal properties[19].
2. Kinetic Monte Carlo methods which use energies estimated from *ab initio* methods, are used to simulate time-dependent states of a system. Unlike molecular dynamics, these methods do not calculate the dynamics of the system and hence can be used to simulate longer time scales. The technique has been applied to nucleation[20], ultra-low pressure chemical vapor deposition[21], or devices[22].

Although the techniques have been demonstrated to be useful in certain applications, they still need to be scaled to meet realistic system sizes (~100 nanometers) and physical times (microseconds or seconds).

Despite recent advances, theory has many limitations that prohibit applicability to systems of practical interest for quantitative correlations. Current applications include: equilibrium energies, density of states, reaction rates, effects of defects in parts per thousand, and transport within nanostructures with interfaces. At the quantum scale, the current applicability of available models is rather limited. Major issues that need to be addressed in the modeling are:

1) Extension to larger scales (tens of nanometers) for equilibrium calculation and temperature dependence of properties and processes. (This could be enabled by linear scaling DFT methods or multi-scale methods).

2) Metallic systems specifically transition and inner transition metals. These need specific functionals that could be tested with more rigorous techniques.

3) More generalized extension for band gaps. Currently hybrid and metal functionals are being developed but they need to be thoroughly characterized before their applicability is adopted. Well-characterized time-dependent methods like Quantum Monte Carlo or Time-Dependent Density Functional Theory for nanosystems still need to be applied widely[23]. This includes newer capabilities and also extension to larger systems.

4) Strongly correlated systems require model development to explain the interaction between spin, charge, and lattice dynamics. This requires quantification of the energy associated with spin switching and transport and the identification of speed limitations. Development of well-characterized methods for strongly correlated systems (LDA + U, DMFT[17], GW[16]) need focus both from the scientific and engineering communities.

5) Coupling of electronic structure predictions to non-equilibrium process such as transport and excitation are necessary since most of the devices operate in non-equilibrium. However, most of the current capabilities are limiting in extensions to realistic systems with multiple interfaces. This is one of the areas in more research need to focus on developing applications with demonstrated capability for a wide variety of systems; metals (conduction), semiconductors (mobility), and insulators (frequency-dependent dielectric response). In addition, extension of non-equilibrium to strongly correlated systems is necessary for understanding complex oxides and Mott insulators.

6) Lattice Physics includes atomic and ionic response to externally applied fields and are based on liner perturbation methods. This has been successfully modeled for bulk materials. Extension of this to nanosturctures with interfaces and in presence of external fields is necessary for addressing realistic devices.

7) Extension or linking of quantum models from femtoseconds to microseconds or longer to emulate realistic synthesis and transport. These extensions are specifically critical for molecular dynamics and Monte Carlo methods (both based on both quantum and classical approaches).

11.3. DEVELOPMENT OF PLATFORM FOR DIFFERENT SIMULATION TOOLS, SUCH AS TCAD AND AB-INITIO

As already mentioned above, simulations needed for understanding and predicting "synthesis, structure, and property" requires different computational techniques based on different principles depending on the size, and time-scale of the system of interest. Even though the computational techniques are different, there should be common input data to bridge the phenomena in different scales of size and time; for example, atomic scale model relate with elastic model of matters so the lattice constant and external fields (e.g. force) can be common input data for both models. When the system is non-uniform, for example includes defects and impurities, establishing the multi-scale modeling is not easy and extracting common input data for different models are not straightforward. The difficult challenge is establishing a way to bridge different models (different physical principles) needed for numerical simulation in order to build a platform for the multi-scale simulation.[21] Wide range of knowledge expanding physical and chemical principles, material properties, devices and practical ways for fabrications are required to build a platform which is open so multiple tools and data structures can be intergrated seamlessly. A more detailed description of the modeling technical issues, such as Monte Carlo simulation[24], is found in the *Modeling and Simulation chapter*.

11.4. METROLOGY AND CHARACTERIZATION

As mentioned previously, when new material properties are characterized, models must be developed to guide synthesis to further enable exploration of new structures and more complex interactions between materials. Establishment of an experimental database with results from well-characterized structures could accelerate the development of more accurate full ab initio and self-consistent reduced models. More quantitative material property mapping at the nanometer-scale requires development of models to probe interactions of nanostructured materials. Improved structure and property mapping for more accurate TEM, AFM, Conductance AFM, Kelvin Probe AFM, Magnetic Force Microscopy (MFM) and other new techniques could improve development of nanometer scale material models.

Summarizing, the properties that need to be addressed from both modeling and metrology are summarized below;

Electronic Properties (Metals, carbon, semiconductor & insulators)

Size & structure dependence of

Energy Levels including bandgap

Mobility

Spin-orbit coupling

Density of States

Surface Energy & Defect Energy Levels

Interface Properties

Interface states

Interface Transport

Debonding and chemical reactivity

Transport Properties

Electrical conductivity and mobility

Thermal conductivity

Optical Properties

Real & imaginary optical constant matrixes for:

Individual nanostructured materials

Matrixes of nanomaterials

Nanomaterials with ultra-thin film coatings

Mechanical properties

Interface adhesion (see above under interface properties)

Short and long range forces including van der Waal's, etc.

12. ERM TRANSITION TABLE

In 2011, a number of changes were made in the scope of materials included in the ERM Chapter, as shown in Table ERM15. Due to their maturity, n-III-V and p-Ge were transitioned out of the ERM and ERD chapers and are being added to the FEP and PIDS chapters. On the other hand, due to potential for developing complementary devices based on III-V and Ge, p-III-V and n-Ge were retained by the ERM and focus on these materials and processes was increased, Thus, p-III-V and n-Ge are shown as being transitioned into the ERM. Also, due to maturity of the zirconium (Zr) and ruthenium (Ru) materials and their compounds as Cu barrier materials, they are being transitioned out of the ERM and will be added to the Interconnect chapter.

Table ERM15 Transition Table for Emerging Research Materials

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