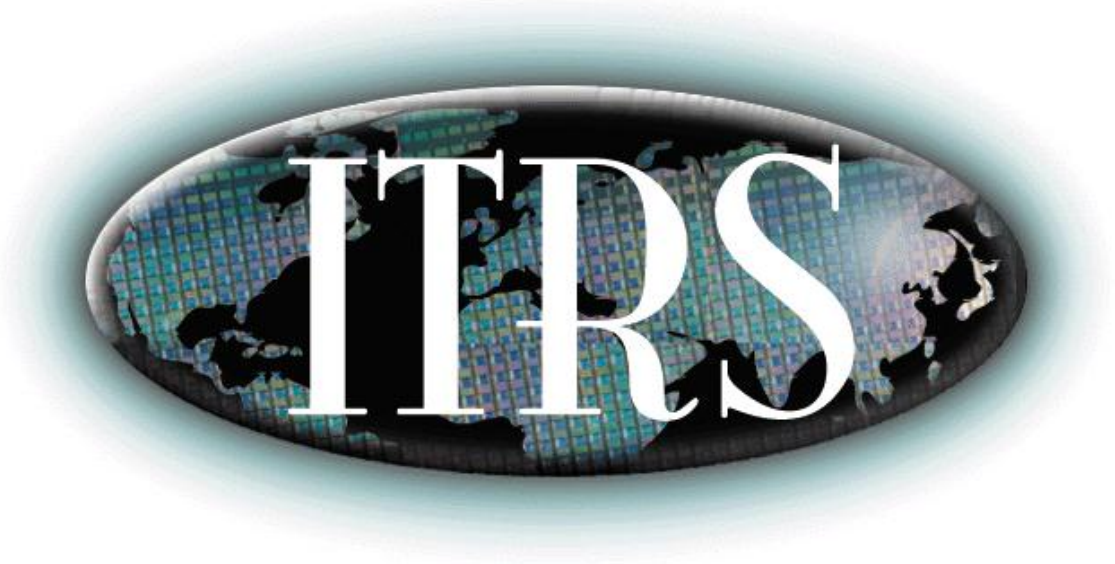


INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

LITHOGRAPHY

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LITHOGRAPHY

SCOPE

Extending optical lithography as we know it beyond 2011 is becoming increasingly difficult. Single optical exposure has reached its limit at 40nm half-pitch (hp). Today, 32 nm hp flash devices are being manufactured using double patterning (DP) as a way of extending the half-pitch while keeping the numerical aperture (NA) and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm hp and flash starts to test the limits of optical solutions at the 22 nm hp in 2013. It is at this point that non-optical lithography must be introduced into manufacturing to ensure a smooth transition beyond 22 nm. Extreme ultraviolet lithography (EUVL) has been gaining significant momentum with several manufacturers taking delivery of pilot line tools. Some are even announcing their intent to purchase production tools as soon as 2012. If EUVL should not be ready on time, the industry will likely further extend DP to multiple patterning (MP). Other non-optical lithography may also be used in a complementary fashion for small volume application and/or prototyping.

Beside the invention of novel technical solutions, it is also critical that die costs remain economical with rising design, process development, and mask costs and cost of ownership (CoO) of the tool and process. Extending optical projection lithography and developing next generation lithographic technology requires advances in the following areas:

- Exposure equipment
- Resist materials and processing equipment
- Mask blanks materials, mask making, and mask-making equipment
- Metrology equipment for critical dimension measurement, thickness and overlay control, and defect inspection

This chapter outlines a fifteen-year roadmap of difficult challenges (Table LITH1), technology requirements (Table LITH2), and potential solutions (Figures LITH3A and LITH3B) in lithography. Additionally, it defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for *Environment, Safety, and Health (ESH)*, *Factory Integration*, *Yield Enhancement*, *Metrology*, *Modeling and Simulation*, *and Emerging Research Materiasl (ERM)*.

The key requirements of lithography for manufacturing integrated circuits are summarized below. *Table LITH2* lists the requirements that are needed based on the device type and half-pitch:

- *Critical Dimension (CD) Control*—The size of many features in a design needs to be precisely controlled. CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer. CD control is required for obtaining adequate transistor, interconnect, and consequently overall circuit performance.
- *Overlay*—The placement of the image with respect to underlying layers needs to be accurate in all locations on each integrated circuit to achieve adequate yield.
- *Defect Control*—The desired pattern must print in all locations with no additional anomalies. No particles should be added to the wafer during the lithography process.
- *Low Cost*—The cost of tools, materials (including resists), and masks needs to be as low as possible while still meeting the CD control, overlay, and defect control requirements. To minimize cost, the lithography step should be performed as quickly as possible. Masks should be used to expose as many wafers as possible. Equipment needs to be reliable and ready to expose wafers when needed.

Although the near-term challenges are many, the industry is addressing them. Lithographic systems are being made to run at throughputs that are about 2× that of older steppers, thus addressing some of the CoO issues associated with double patterning. Registration and overlay issues with lithographic mask patterning systems are also being improved to move more products into double patterning into manufacturing. The industry is likewise addressing the fundamental challenges associated with the non-optical lithography, in particular the EUV mask infrastructure that is needed. The long-term lithography challenge is technology extendibility. It is unlikely the industry will fund any solution that can be used for only 1-2 nodes without the possibility of extension. With these gains and mind sets in place, the lithography industry will again be back on course for improving future return on investment (ROI).

DIFFICULT CHALLENGES

Table LITH1 shows the most difficult near-term and long-term challenges of the continuously shrinking minimum half-pitch. The dividing point between near term and long term (beyond 2018) comes somewhat arbitrary as the industry has to overcome the transition from traditional optical single patterning to either double and multiple patterning or patterning using EUV light already in the near term time frame. In the long term the question arises if these technologies can carry the industry through down to 11 nm half pitch resolution or alternative solutions like Maskless Lithography (ML2), Imprint, Directed Self Assembly or 6,x nm Lithography have to be implemented.

DIFFICULT CHALLENGES—NEAR TERM: 2012-2018 (≥ 16 NM LOGIC/DRAM, > 11 NM FLASH)

DOUBLE PATTERNING/SPACER TECHNOLOGY

Meeting the required resolution using an optical wavelength is driving the use of multiple exposures to define each device layer. Some double exposure techniques are already being used, including alternating phase shift plus trim and double dipole exposures. These techniques allow for imaging at closer to the diffraction limit (k_1=0.25). Further multiple exposure techniques have been designed to form images beyond the single-exposure diffraction limit; these place additional requirements on lithography that vary by the specific type of multiple exposure technique *(*Table LITH5).

Two basic processes, *pitch splitting* (PS) and *spacer patterning* (SP), and their requirements are defined by the differences in their critical lithography patterning steps. PS includes the traditional double *patterning* (DP) of two separate lithography/etch steps to define a single device layer, often called (litho etch litho etch [LELE]), and double exposure (DE), which is two lithographic exposures into one material with only one etch step. This can incorporate non-linear resists or a litho freeze process. The SP process uses one critical lithography step and then additional thin film deposition and etches steps in a spacer-like process to define two sets of critical features. (Note that this process also requires a second cut mask similar to the dipole lithography cut mask.) Spacer double/multiple patterning eliminates one or more critical exposures, but the allowable shapes are limited because the single exposure defines the location of the features. Figure LITH1 is a schematic of the process flows for these different approaches.[1, 2, 3, 4]

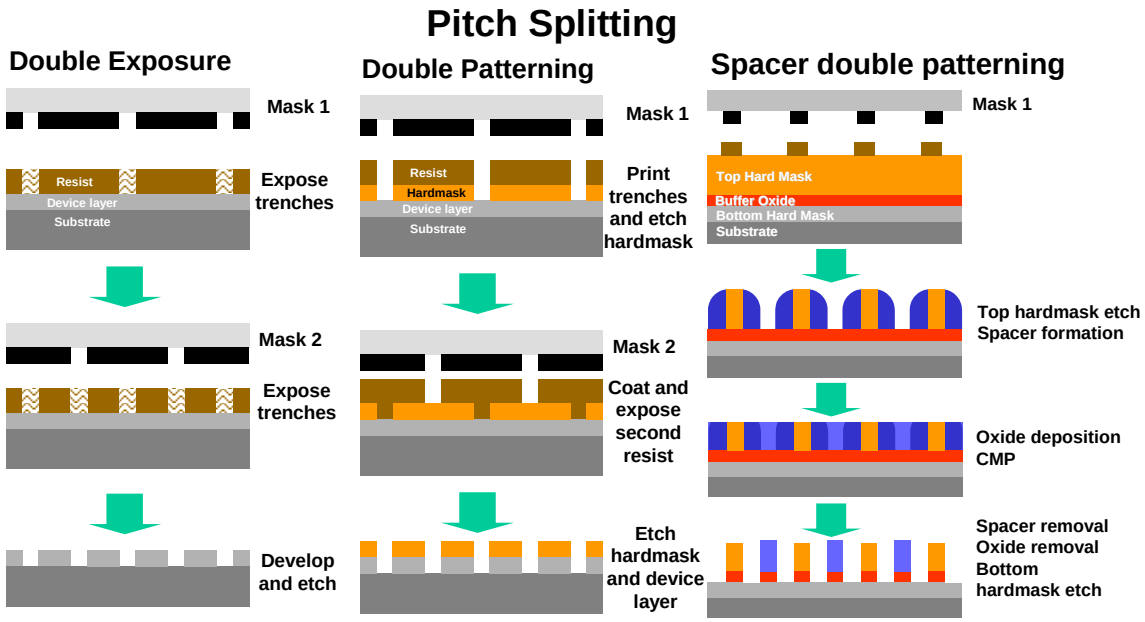


Figure LITH1 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

All these technologies present their own challenges, as there are:

- Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
- Photoresists with independent exposure of multiple passes
- Implementing and controlling additional process steps for spacer technology
- Fab logistics and process control to enable low cycle time impact efficient scheduling of multiple exposure passes and/or additional process steps for spacer technology.
- Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining a minimum amount of "pitch doubling/spacering steps" for arbitrary designs
- Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
- Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
- Lithography and pitch splitting/spacering friendly design and design for manufacturing (DFM)

All these methods for pitch doubling break down latest at the diffraction limit of the single patterning step i.e. for devices with half pitches below 40 nm which is eminent for flash and according to the Roadmap will happen within the short time frame also for Logic and DRAM devices. To overcome this, a switch to multiple applications of the pitch splitting and spacering steps has to be performed, which will result in ever increasing above mentioned challenges for complexity, throughput and cost.

OPTICAL MASK – COMPLEXITY, LONG WRITE TIME, COST

The leading challenge for the near term and a significant challenge for the long term is the mask. Mask-making capability and cost escalation are critical to future progress and will require continued focus. Masks are both a commodity and an enabler of progress along the roadmap. The need for expensive high-end capital equipment in the mask shop along with low initial market volumes makes the market difficult for commercial mask shops. As a consequence, the mask industry has experienced numerous consolidations and partnerships to address the issues. This has in turn decreased the volume of capital equipment that is sold into the leading-edge market, further driving costs up, resulting in just-in-time capital equipment that is needed to develop the mask process for the industry.

The mask specifications have increased more quickly than the half-pitch designated by the roadmap.[5] Historically, this increase has been driven by the MPU gate line width (post-etch), contact printing and the greater mask error enhancement factor (MEEF) associated with low k_1 lithography. The need for 2X patterns on the mask (i.e., sub-resolution enhancement patterns) has also contributed to the specifications, and double patterning demands mask registration specifications that far outpace the half-pitch in the roadmap (See *Table Lith5*).

Note also that the combined cost of the two masks is about 1.5× the cost of single masks due to more data for the two masks and longer inspection and repair times. For each successively smaller node, content on the mask typically grows by a factor of 2. In fact, to accommodate the optical pattern correction to achieve sub-wavelength imaging, the data growth per node has been expanding much faster than what doubling the pattern content would imply. The historical data growth rate has been 2.7× per node over the last 8 years rather than 2× would be expected. At the 32 nm node the mask cost of an optical mask far outweighs litho tool costs because of the excessive data to write these masks. Write time estimates for an optical mask at the 32 nm node exceed 35 hours because of extensive use of OPC. This effect accelerates into the 22 nm node and beyond.

Progressive defect formation has become a greater problem with organic and inorganic deposits forming on masks after many wafers are exposed. This has caused a 13X increase in the reworking of masks made for 193 nm lithography compared to older 248 nm technology.[6] Mask damage from electrostatic discharge (ESD) has long been a concern; it is expected to be even more problematic when mask feature sizes shrink. As CDs become more critical, electric field migration (EFM) has also been shown to change CD sizes.

A way out of the difficulties in optical lithography is seen in EUV technology, which by itself imposes its own set of challenges.

EUV TECHNOLOGY – SOURCE POWER / MASK AVAILABILITY

The observed challenges on EUV are:

- Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
- Fabrication of Zero Printing Defect Mask Blanks
- Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection)
- Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs)
- Protection of EUV masks from defects without pellicles
- In fab EUV masks handling , storage and requalification
- Cost control and return on investment

Among these EUV concerns, source power is most prominent followed by mask defects and resist. These issues have been at the forefront of EUV issues for over the 5 years that they have been tracked.[7] The technology choice between DPP and LPP sources for achieving the required source power is still open. The achieved values in both technologies are currently limiting the achievable throughput of EUV lithography, which raises the concerns about CoO on EUV technologies.

The mask issues are numerous, involving many new changes that must be met simultaneously. Masks will require LTEM substrates, zero-defect multilayer reflecting surfaces, and new pattern absorber materials. The greatest concern is with phase defects, which for 22 nm half-pitch lithography can be as small as a 20nm disk that is 180 deg in phase (*Table LITH6*). The infrastructure for detecting this size has still not been developed on either substrates or blank or patterned masks, although programs are underway to realize this.

The next prominent challenge on EUV is resist.

RESIST AT 16 NM AND BELOW

Resist challenges involve:

- Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution
- Limits of chemically amplified resist resolution capability for < 20 nm half pitch due to acid diffusion length
- Materials with improved dimensional and LWR control add (limits)

Resist materials will require significant improvements. Acid diffusion in chemically amplified resist might limit the ultimate minimum half-pitch that can be achieved with high sensitivity resists unless diffusion length is reduced or new methods of sensitizing resists are found. New non-chemically amplified resists which show resolutions below 16 nm and acceptable LER are developed but they suffer under low sensitivities and other process issues.

PROCESS CONTROL ON KEY PARAMETERS SUCH AS OVERLAY, CD CONTROL AND LWR

Many challenges are associated with variability control, not just scaling. Variability control not only must keep up with dimensional scaling, but often needs to improve even faster. New and improved alignment and overlay control methods independent of technology option have to be developed. Also controlling LWR and CD changes induced by metrology, and defects < 10 nm in size are a challenge as well as greater accuracy of resist simulation models and accuracy of OPC and OPC verification.

To achieve demanding CD control tolerances, resolution enhancement techniques, design restrictions, and automated process control are being employed. All these aspects are particularly challenged with the insertion of double and especially multiple step options. To further extend optical lithography, new practices are required to better comprehend the increasing variation of critical dimensions as a fraction of the feature size in the design process. These practices are usually referred to as “design for manufacturing” (DFM). DFM allow designers to account for manufacturing variations during circuit design optimization, enabling the IC fabrication process to be optimized to provide the highest performance at a minimal cost. Ultimately, the

designer could optimize the circuit with knowledge of all physical variations in the fabrication process and their statistical distribution. At the simplest level, designers are being made aware of library cells that have yielded well in manufacturing. Furthermore, simulations of the lithography, etch, and CMP processes are being used to examine the full chip area for weak spots in the layout that are most susceptible to manufacturing variations. Coordinates of these weak points are provided to mask and wafer CD metrology tools. Focus and exposure are optimized for printing weak spot regions with maximum process latitude rather than for test structures. The topographical features of these printed weak spots need to be evaluated with pattern fidelity metrology. The weak spot locations are then targeted for layout modification and monitoring during manufacturing. Automation of software to analyze these weak spots in design and feedback to the physical layout of cells is being aggressively pursued by electronic design automation (EDA) suppliers. DFM tools and techniques will be essential to minimizing mask revisions and achieving adequate yield in the wafer fab. See the *Design chapter* for more information on DFM.

450 MM TRANSITION

In addition to these challenges in the near term time frame transition to 450 mm diameter wafer processing is scheduled. This requires that all tools in the fab environment are adapted to 450 mm diameter wafers. A focused development path for equipment suppliers has to be established to make all necessary tools needed for 450 mm and make fab infrastructure available at the required need time. Return on the investment on supplier side is an issue as well as CoO on manufacturers' side.

DIFFICULT CHALLENGES--LONG TERM: 2019-2025 (< 16 NM LOGIC/DRAM, 11 NM FLASH HVM)

The long term challenges are dependent on the potential solutions which will be chosen out of the potential solution table. As shown there the transition to new technologies might even be necessary already at larger half pitches. All solutions will require new infrastructure support, which makes it necessary to narrow down to 2-3 options at an early stage for implementation and in order to be able to focus financial support in developing the necessary technology together with its infrastructure.

As EUV remains the leading candidate for 22nm and 16 nm half pitch, its extension to higher resolutions is in the focus of the long term challenges. Even higher source powers will be required for the resist needs and an increase in NA for resolution enhancement could result in larger chief ray angles on the mask. In order to overcome shadowing and other 3D effects on the mask one will have to optimize absorber materials and absorber thickness as well as the multilayer stacks.

Multiple patterning with EUV will also be an option which will imply solutions to CoO and process difficulties as mentioned in above Multiple Patterning chapter.

Resist difficulties will be prolonged and enhanced from the near term challenges as is true for the other challenges mentioned in the near term section. So even more demanding overlay, defect, and CD control requirements will continue to pose challenges for process control, resist development, and mask development.

The possible use of maskless lithography will probably require die-to-database inspection of wafers to replace die-to-database inspection of masks.

If imprint lithography finds its way as volume manufacturing solution, mask fabrication, defectivity control, and metrology becomes even more challenging as imprint lithography templates have the same dimensions as the wafer pattern.

Directed self assembly, in which the molecular structure of the imaging material drives the sub-lithographic feature sizes and control, is a new star on the horizon to overcome the potential limitations of the so far considered next generation lithography technologies. The major challenge here will be to cope with the requirement of defect free processing where it is not clear yet if this challenge is a chemical engineering or a fundamental physical issue.

A more classical solution path would be to reduce the EUV wavelength to 6.x nm. This path would inherit all the challenges of EUV we are confronted with currently in the near term time frame from source availability to mask infrastructure and resist performance.

Apart from these challenges also the implication of further shrinks to supporting infrastructure should not be forgotten. Examples are metrology tool availability to measure and control key parameters like CDU, overlay, material thicknesses, defect, etc.

6 Lithography

Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions within industry and among industry, universities, and governments are necessary to narrow the options for these future generations and focus support to enable one or perhaps two technologies to be ready for manufacturing at the desired time.

The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities for continued adherence to Moore's Law. This shift will drive major changes throughout the lithography infrastructure and require significant resources for commercialization. These development costs must necessarily be recovered in the costs of tools, masks, and materials.

	Near Term Challenges (2011-2018) (16nm Logic/DRAM @ HVM; Flash 11nm @ optical narrowing with 16nm in HVM)
1	Multiple patterning - cost, throughput, complexity
2	Optical mask - complexity with SRAF, long write time, cost
3	EUV source power to meet throughput requirement; Defect "free" EUV masks availability; mask infrastructure availability; EUV mask in fab handling, storage, and requalification.
4	Resist at 16nm and below that can meet sensitivity, resolution, LER requirements
5	Process control on key parameters such as overlay, CD control, LWR at 16nm HVM
6	Retooling requirements for 450mm transition

	Long Term Challenges (2019 - 2025) (11nm @HVM)
1	Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
2	Defect free DSA processing
3	Infrastructure for 6.Xnm Lithography or multiple patterning for EUVL 13.5nm
4	Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect
5	Early narrow and implement ~2 options with viable infrastructures support

Table LITH1 Lithography Difficult Challenges

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Table LITH2)
- Resist Requirements (Tables LITH3A and 3B)
- Optical Mask Requirements (Tables LITH4)
- Multiple Patterning Reuirements (Table LITH5)
- EUV Mask Requirements (Table LITH6)
- Imprint Mask Requirements (Table LITH7)
- Maskless Lithography Requirements (Table LITH8)

Table LITH2 Lithography Technology Requirements

The format of Table LITH2 reflects the differences in the lithographic requirements that are set by ORTC - Product Generations and Chip Size Model Technology Trend Targets. The table specifies three device types that push the lithographic requirements the most: DRAM half-pitch (contacted), MPU/ASIC Metal half-pitch, and Flash half-pitch (uncontacted poly). The Flash device pushes the half-pitch the most while MPU pushes the physical gate length and CDs the most. Each of these technologies needs a different set of specifications for CD control, contact size, and overlay depending on the half-pitch and design. The table uses the values from the ORTC table (fixed numbers) and then equations to determine the other specific parameters associated with a particular specification. For example, CD control for the DRAM device is 12% of the DRAM half-pitch times the percentage of the error budget shared between lithography and etch (in quadrature).

Requirements for a short MPU gate length after etch create significant challenges for metrology and process control. Controlling critical dimensions to the required ± 12% tolerance of the final etched gate CD is becoming increasingly more difficult. This 12% includes cross-field, cross-wafer, wafer-to-wafer, and lot-to-lot variations. Post-development line width reduction techniques are becoming more prevalent and more capable. Printing larger features in resist improves CD control by providing for a larger lithography process window. Similarly, for the contact size in resist, the printed size with 193nm immersion process is limited to 55nm. It is assumed that various etch shrinking techniques are applied to achieve the final desired size as indicated in Table LITH2. Contact size below 30nm is assumed to be printed with either EUV lithography or next generation lithography process, which is targeted to be ready for volume production by 2013~2014 time frame. Integrated circuit manufacturers are also modifying design rules to make the patterning task more feasible. Metrology will play a critical role in defining these lithography-friendly design rules.

The mask counts (not masking layers) for three different products have been updated. The survey results from relevant IDM are used as the projected roadmap. There is no implicit clarification on the causes of mask count reductions in 2014 for flash and DRAM and 2016 for MPU. However, they appear to have correlation with the implementation of charge trap architecture for memory in 2012, multi-layer 3D in 2016, and EUV Lithography for MPU in 2015.

Table LITH3A Resist Requirements

Table LITH3B Resist Sensitivities

Photoresists need to be developed that provide good pattern fidelity, good line width control, low line width roughness, and few defects. As feature sizes get smaller, defects and monomers will have comparable dimensions with implications for the filtering of resists. See Table LITH3A.

The effects of line edge roughness (LER) and line width roughness (LWR) are continuing to be issues and affecting device performance. Therefore, metrology tools are needed to be modified to accurately measure these variations. High frequency line width roughness affects dopant concentration, profiles and interconnects wire resistance. Line width roughness at higher spatial frequencies results in variations of transistor gate length over the active region of the device. This variation increases leakage and causes the speed of individual transistors to vary, which in turn leads to IC timing issues. The line width and line edge roughness also contributes to the CD uniformity error budget for small gate lengths and long LER/LWR correlation lengths. The CD uniformity component from LER/LWR is likely to drive the required LER/LWR numbers even more aggressively than in previous roadmaps. Because of the particular challenges associated with imaging contact holes, the size of contact holes after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gate length. See *Table LITH2* for the technology requirements. Post exposure bake (PEB) sensitivity continues to be reduced. The values are no longer rounded to the nearest nanometer.

The resist sensitivity tables are based on the CoO associated with the different lithography approaches. The more sensitive the resist, the more wafers could be processed. However, in general there is a limit associated with the three parameters that the resist has to maintain: sensitivity, resolution, and LWR. Improvements of any one of these usually come at the cost of the other specifications. Moves to improve the photon quantities by increasing the illumination power associated with the lithography tools are going on. This will allow higher throughput or may allow users to use less sensitive resists for improved resolution and LWR. High voltage e-beam resist sensitivities have been changed to TBD but the target range is from 5-30 µC/cm2 based on the need from Cost of Ownership perspective. Shot noise may push this range to be significantly higher. There will be more discussion in the 2012 revision.

Table LITH4 Optical Mask Requirements

Earlier editions of the ITRS split optical mask requirements into two tables, one for single-patterning and the other for double-patterning. In the 2011 edition, LITH4 focuses exclusively on masks intended for multiple patterning. Instead of relying on incremental improvements to wavelength and numerical aperture, the favored approaches are either to stay with the current 193 nm immersion, 1.35 NA systems and continue shrinking with multiple patterning steps, or move to an alternative patterning technology. It was because resolution of 193 nm, 1.35 NA systems is limited to about 80 nm pitch, only multiple-patterning optical solutions can meet ITRS requirements from 2011 onward. This consideration has prompted significant changes to Table LITH4.

Most of the changes follow from the fact that mask patterns will stop shrinking with wafer patterns according to scanner reduction. Various multiple-patterning techniques use side-wall spacers to define wafer patterns, or apply significant etch bias or other post-lithography process bias. In all cases, the simple correspondence of mask dimensions to wafer dimensions is lost. Mask features will continue to shrink to about 80 nm, corresponding to a 3:1 duty cycle at 320 nm pitch (80 nm pitch at wafer scale). The rapid growth of data volume per mask will also slow significantly when we reach this limit. Data volume per layer will continue to grow as before; it will just be split among multiple masks.

Although mask patterns may stop shrinking, CD control and overlay tolerances must continue to track wafer requirements. These are the most challenging requirements for optical masks. Greater sensitivity of image errors to mask errors (MEEF) drives this as we approach 80 nm wafer pitch in a single patterning step. Values of MEEF in the 2011 version of LITH4 are higher than those from prior years, an adjustment that was based on published data. This will increase the relative contribution of masks to total CD errors, and is accounted for by changing the fraction from 40% in 2010 to 50% in the current table. Despite the larger allocation, improvements in equipment, process technology, and metrology will be necessary to meet CD control requirements.

Increased reliance on computation of mask patterns has helped to provide necessary process control as lithographic resolution approaches its limits. Starting with optical proximity correction to put nominal images on target, mask patterns are now designed to improve depth of focus, increase contrast, and reduce MEEF. The scope of computational lithography also includes illuminator design, which has expanded as exposure systems with more versatile illuminators have become available. Entries in the 2011 ITRS tables related to line width control, MEEF, and mask specifications assume that mask patterns are optimized with computational methods that comprehend process control. Significant progress has occurred regarding algorithms to solve the inverse imaging problem and synthesize mask patterns that yield larger process windows. Taking advantage of computational lithography depends on continued improvement of mask writers and inspection systems to produce more complex patterns, and reduction of measurement uncertainty to calibrate accurate models. Integration of computational lithography with multiple patterning must address where pattern decomposition belongs in the data flow from design to mask data preparation. Although computational lithography is most often associated with 193 nm immersion exposures now, it also may be applied to extend EUV capability using similar methods.

Table LITH5 Multiple Patterning Requirements

The multiple patterning table is divided into three parts, leading with half-pitch requirements for the different device types, followed by two process requirement sections: Generic pitch splitting by multiple exposures and pitch splitting by sidewall spacer double and quadruple patterning. The roadmap for *Generic Pitch Splitting* is driven principally by MPU metal half-pitch while the *Spacer Patterning* requirements are driven principally by NAND-Flash; as such the lithography requirements are substantially different for each technique. The fundamental premise is that both the line and the space must meet the 12% CD specification. Since the space depends on the overlay and printed line width, meeting the 12% specification drives the overlay specification for multiple exposure double patterning and drives CDU specifications for spacer patterning techniques. In both cases, control of space CDU (and thus overlay requirements) is convoluted also with CD control for the line. Therefore, to make the overlay specification as large as possible, process requirements for manufacturing steps which control the line CDU are also tightened to the fullest extent of existing process capability.

Although the optical mask table is extended to 8nm NAND half-pitch and 6nm DRAM half-pitch, no optical solutions (up to quadruple spacer patterning) are yet known to pattern below the 11nm half-pitch starting in 2020 for NAND and 2021 for DRAM. Assumptions are that EUV lithography will be part of the patterning solutions by 2020.

Sidewall Spacer Patterning Discussion:

The sidewall spacer patterning section of the table has been revised into two principal sections, (a) manufacturing process capability requirements and (b) resulting patterning performance per-feature. This format simplifies the presentation of the

spacer patterning roadmap requirements by distinguishing the equipment performance needs (module inputs) from calculated CD-control for the various types of line/space data pools (module outputs). Currently, NAND flash is driving the sidewall spacer patterning requirements, where the design requirement is to have all spacer patterned features meet the target half-pitch +/- 12% (from ITRS table DESN9, row title "% CD Variability"); as such, the manufacturing process requirements are set so that all patterned features (lines & spaces) have a mean + 3 sigma less than 12% of the half-pitch after all the tolerance stack-up is combined.

Definitions: In this section, MTT refers to wafer mean-to-target; i.e. for 32nm half-pitch SADP a mandrel target is 32nm. A wafer with a mean of 33nm has a MTT equal to 1nm. Likewise, the sidewall spacer would have a target of 32nm. A wafer with a sidewall spacer measuring 33nm would have a MTT equal to 1nm. MTT for mandrel and spacer are important because they generate placement errors of the lines and spaces (similar to overlay in litho-etch-litho-etch). In these tables, CDU refers to the combined 3-sigma for inter-field and intra-field locations. MTT + 3sigma refers to the root-mean-square of the two errors; where NAND flash requires that all features have MTT + 3sigma <12% after factoring in the various tolerance stack-up contributions for each feature type.

Limited by the 80nm pitch of water immersion lithography, a transition from spacer double patterning to spacer quadruple patterning occurs below 20nm half-pitch. This transition is indicated in the table by the row titled "multiplication factor". Most of the spacer related equations undergo change during this transition from double to quadruple patterning. Figure LITH2A shows spacer double patterning process schematic with feature definitions, and figure LITH2B shows spacer quadruple patterning process with schematic and feature definitions. Note that the sidewall spacer quadruple pattering scheme is nothing more than two cycles of sidewall spacer double patterning. There is, however, the addition of a new data pool for spaces (called "spacer defined space") see figure LITH2B. Space #1 and #3 (indicated in figure LITH2B) are defined as "spacer defined space" because they originate from the first spacer deposition. Space #2 is defined as the "core space" (similar to double patterning) which originates from the first mandrel (core) and space #4 is defined as the "gap space" (similar to double patterning) which originates from the gap space formed between the first two spacers. In both the spacer double patterning and spacer quadruple patterning, the "gap" space contains the most tolerance stack-up and is the performance limiting feature which drives the manufacturing process error budgeting.

Manufacturing Process Capability: The two performance limiting steps within a sidewall spacer patterning scheme are (1) the CD control of the mandrel and (2) the CD control of the spacer deposition process. When referring to the mandrel, some processing techniques utilize photo-resist as a mandrel while other techniques use resist as a mask to etch a mandrel into another material. In the former case, the photo-lithography process must meet the mandrel CDU (combined inter-field and intra-field 3-sigma) along with MTT; in the latter case, where the mandrel is formed by litho and etch, the final etched mandrel must meet the listed CDU and MTT performance requirements. The CD control of the spacer deposition process also has both CDU and MTT requirements. The ITRS lithography working group uses the following error budgeting guidelines, so that all features will meet the MTT + CDU < 12% requirements: mandrel CDU < 6% of half-pitch, mandrel MTT < 4% of half-pitch, spacer deposition < 3% of half-pitch for both MTT and CDU. More error budgeting is allocated to the mandrel than to the spacer deposition because of the greater challenges to control this dimension. Regarding the mandrel, more error budget is allocated to the within wafer CDU, which is a combination of both inter-field and intra-field, than to the wafer's MTT. Figure LITH2C shows the corresponding equations and percentages for the various table rows related to spacer patterning. Note that "gap space MTT + 3sigma" is 11.1% during the double patterning era and 10.8% during the quadruple patterning era, which is the performance limiting feature. Also note that "spacer defined space" appears as a third data-pool for spaces after the transition to quadruple patterning. Additionally, to accommodate the additional tolerance stack-up involved with the spacer quadruple patterning process, the error budget for the spacer deposition process tightens to 2% of half-pitch.

For current NAND layouts, the cut (trim) mask overlay requirements are quite relaxed. Although NAND flash is driving the half-pitch scaling, there are other spacer patterning user groups, such as those using spacer patterning to produce fins (FinFET devices) and active islands (DRAM) using line and cut techniques. These approaches will have moderately aggressive overlay requirements and scale with the spacer pattern array pitch. A cut mask must be applied for the purpose of cutting lines, removing dummy-fins on pitch, or blocking trenches in BEOL patterning. A row specifically addressing the overlay requirements for spacer cutting (or trench blocking) is added to the spacer patterning section. Figure LITH2D shows a schematic and equation for approximating these overlay requirements. It is assumed that a cut mask (for a single line cut) is designed with edges that fall exactly half-way between spacers. Thus, as a first order approximation the alignment tolerance without guard-banding is ¼ of the array's pitch. From this starting point, we need to guard-band by the placement shift of the spacer, which results from CD errors on the spaces. The tolerance stack-up analysis shows that the gap space has the most CD error, and will generate the maximum spacer placement offsets; therefore we need to guard-band by the gap space (MTT + 3 sig)/2. Secondly, we need to guard-band by the CDU control of the cut mask opening. Assuming a cut mask opening equal to

the array's pitch, and assuming a CD control of that feature of 5%, then we need to guard-band by an additional 5% of the array's pitch. Thus the equation presented in the table is that overlay requirements for applying cut masks to a spacer patterned array (Fin cutting, DRAM island cutting, dummy line removal, etc) is equal to 25% of the pitch minus gap space (MTT+3sigma)/2 minus 5% of pitch. Please note that NAND cut masks are substantially relaxed.

Within the spacer patterning section of table LITH5, the manufacturing process requirements are colored to indicate the state of readiness to achieve the forecasted requirements. The assumptions used when assessing the ability to meet mandrel CDU (intra-field and inter-field) is that users will be performing high order dose corrections across wafer and fields in mass production, which may even be applied to correct for dedicated etch chamber fingerprints; furthermore, to control MTT it is assumed that users will be applying some form of feed-forward and feed-back process control as well.

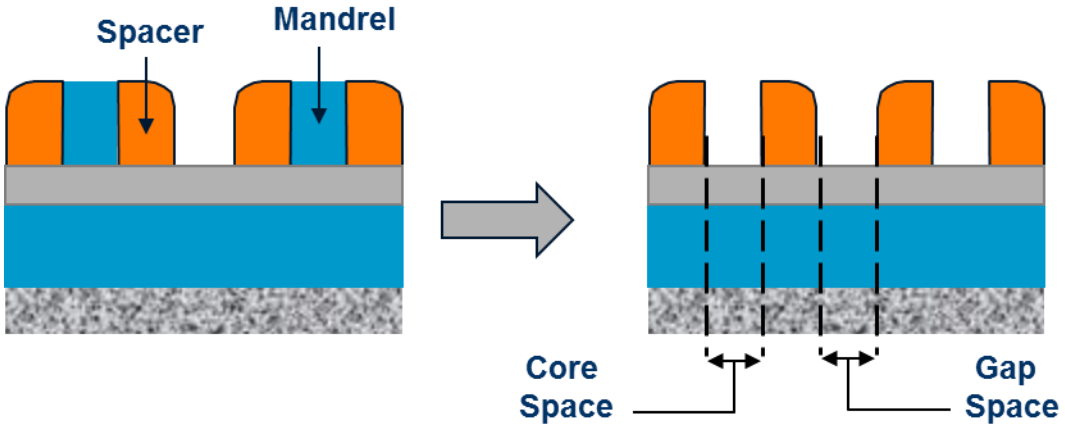
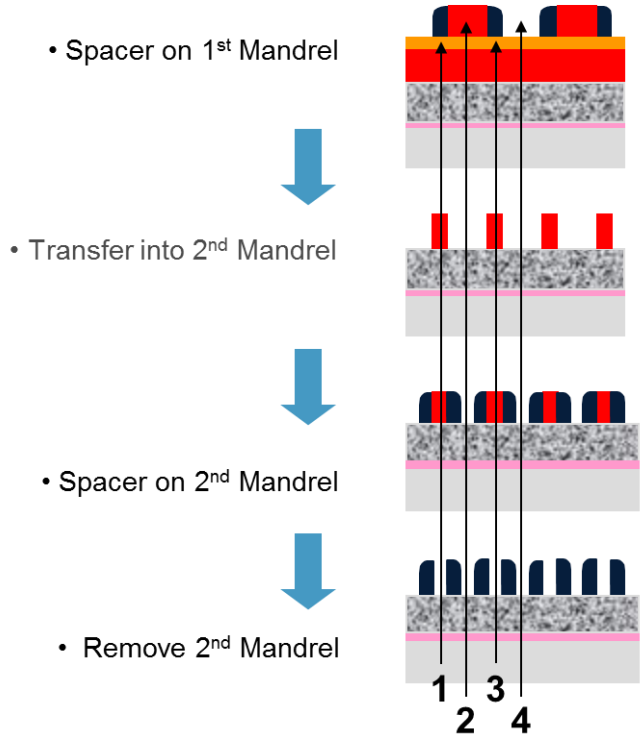


Figure LITH2A: Schematic of positive tone Sidewall Spacer Double Patterning, with definition of "core space" and "gap space". Gap space always has the greatest tolerance stack-up.



Quad Patterning: 3-data pools for spaces:

"Spacer Defined Space"
- **Space #1 & Space #3 originate from the first spacer deposition, and share a single mean & distribution.**
- **This is a new data pool compared to spacer double patterning.**

"Core Space"
- **Space #2 in this diagram; originates from first mandrel, which is therefor a lithography derived feature.**
- **In quad patterning the second spacer deposition contributes additional CD-error, compared to the spacer double patterning core space.**

"Gap Space"
- **Space #4 in this diagram; originates from first lithographically generated space, which is therefore a lithography derived feature.**
- **In quad patterning, both the first and second spacer deposition contributes additional CD-error, compared to the spacer double patterning core space.**

Figure LITH2B: Schematic of Sidewall Spacer quadruple patterning, indicating and defining the various data pools for spaces.

	A	B	C	D	E	F	G	H	I	J	K
1			**SADP Formula's**					**SAQP Formula's**			
2											
3		NAND 1/2 pitch	Half-Pitch	100%	22	20		Half-Pitch	100%	15	12
4											
5	Mfg. Process Capability	Mandrel CDU	=6%*C3	6.0%	1.3	1.2		=6%*H3	6.0%	0.9	0.7
6		Mandrel MTT	=4%*C3	4.0%	0.9	0.8		=4%*H3	4.0%	0.6	0.5
7		Spacer CDU	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
8		Spacer MTT	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
9											
10	Resulting Patterning Performance	Line CDU	=C7	3.0%	0.7	0.6		=H7	2.0%	0.3	0.2
11		Line MTT	=C8	3.0%	0.7	0.6		=H8	2.0%	0.3	0.2
12		Line MTT+3sigma	=SQRT(C7^2+C8^2)	4.2%	0.9	0.8		=SQRT(H7^2+H8^2)	2.8%	0.4	0.3
13		Core Space CDU	=C5	6.0%	1.3	1.2		=SQRT(H5^2+(2*H7)^2)	7.2%	1.1	0.9
14		Core Space MTT	=C6	4.0%	0.9	0.8		=SQRT(H6^2+(2*H8)^2)	5.7%	0.8	0.7
15		Core Space MTT+3-sigma	=SQRT(C5^2+C6^2)	7.2%	1.6	1.4		=SQRT(H13^2+H14^2)	9.2%	1.4	1.1
16		Gap Space CDU	=SQRT(C5^2+(2*C7)^2)	8.5%	1.9	1.7		=SQRT(H5^2+(2*H7)^2+(2*H7)^2)	8.2%	1.2	1.0
17		Gap Space MTT	=SQRT(C6^2+(2*C8)^2)	7.2%	1.6	1.4		=SQRT(H6^2+(2*H8)^2+(2*H8)^2)	6.9%	1.0	0.8
18		Gap Space MTT+3-sigma	=SQRT(C16^2+C17^2)	11.1%	2.4	2.2		=SQRT(H16^2+H17^2)	10.8%	1.6	1.3
19		Spacer Defined Space CDU						=H7	2.0%	0.3	0.2
20		Spacer Defined Space MTT						=H8	2.0%	0.3	0.2
21		Spacer Defined Space MTT+CDU						=SQRT(H7^2+H8^2)	2.8%	0.4	0.3

Figure LITH2C: Shows that corresponding equations and percentages for the various table rows; note that "gap space MTT+3sigma" is 11.1% during the double patterning era and 10.8% during the quadruple patterning era, which is the performance limiting feature. Also note that "spacer defined space" appears as a third data-pool for spaces after the transition to quadruple patterning. All features have MTT+3Sigma < 12% per NAND flash requirements.

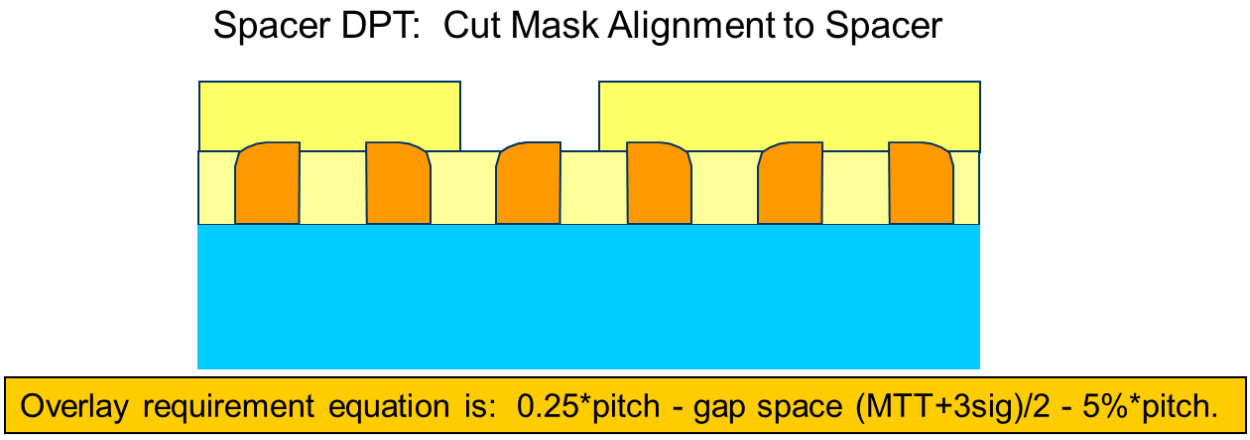


Figure LITH2D: Schematic of a cut mask applied to a spacer array for the purpose of line cutting, such as in Fin formation, DRAM island formation, or dummy fin removal, where one needs to critically cut one line on pitch. The equation describes the overlay requirements of the cut mask accounting for the various guard-banding due to spacer placement errors and cut mask CD-control errors.

Table LITH6 EUV Mask Requirements

Table LITH6 covers the EUV mask requirements. Common requirements such as CD and overlay are developed in the same way as the optical requirements. The MEEF values have been updated in the equations based on calculations with assumed

resist and tool blur. The CD uniformity, particularly for contacts, has quickly becoming a challenging parameter due to the increase in MEEF values.

The EUV-specific mask requirements include substrate/blank defects, blank multilayer reflectivity, absorber film thickness control, absorber sidewall angle, LWR, and mask flatness. The absorber film thickness control is new this year and based on simulation results from print CD control with inputs on pitch, NA, resist and lens blurs. The illuminator setting is assumed to be Quasar 45 and an assigned CD tolerance of 25% that of DRAM/Flash.

Multilayer surface roughness is a key EUV mask parameter. It affects both the LWR with defocus in lithography and the signal-to-noise ratio in inspection. Replicated multilayer surface roughness (RSR) is that roughness which is replicated in at least the top 10 layers of the multilayer stack. Based on simulation with a sigma value of 0.5, roughness correlation length of 100 nm, and the appropriate NA, initial RSR specification should be ~50pm. CD scaling is assumed to be achieved with increasing NA for shrinking CD. Total allowable mask contribution to resist LWR is set at 10% in quadrature, and for the RSR effect to be limited to 70% of the mask contribution in quadrature. The increased LWR is allowed to shrink the NILS = 2 focus latitude by at most 30%. RSR measurement metrology is currently based on X-ray reflectivity and scattering (XSR) measurements. Such tool is not commercially available. AFM data have been used as measurement of roughness by the blank manufacturers and mask makers. Correlation assessment between AFM and RSR for typical commercial ML blank is needed to determine the appropriate roughness values. Once such assessment is completed, roughness will be included in the table in the 2012 revision.

EUV mask flatness has a very tight specification, since mask non-flatness along with the off-axis illumination causes a distortion error which must be kept small. The specification for flatness is such that it contributes an equal amount to the wafer registration error as mask patterning does. Ongoing research may allow this specification to be loosened in the future. This research is based on the concept of measuring a mask's non-flatness and then correcting the position of the patterns such that when the mask is imaged the pattern will be in the correct location even if the mask did not meet the flatness specification. Final mask bow and backside local slope are new parameters added. When clamped, reticle bow adds primarily to in plane distortion (IPD) as a residual distortion. A bowed reticle will lead to magnification error which can be corrected by the scanner. However, the distortion is not linear due to the edge effects of the clamp. Local slope of 20mm X 20mm area was chosen as a compromise to have a single spatial frequency for simpler specification.

Defect free mask availability has been regarded in the last several years as one of the top two priorities for EUV high volume manufacturing (HVM). EUV printing defects can derive from traditional opaque defects in the patterning layer as well as small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. This is a complicated term since a phase defect has an associated phase (driven by height) and a size characteristic. This specification is based on a worst-case defect approach as is done with all the defect specifications in the roadmap. Thus the specification is the size of a 180 degree defect, which is 3 nm high for an EUV reflective mask. As is noted in the footnote, a 90 degree defect (1.5 nm high) will also cause a CD defect if it is about twice the specification size. As EUV moves closer to manufacturing, this specification and the substrate specification will be improved. [8, 9, 10, 11] Another major challenge is that these phase defects are beyond the limits of today's metrology capability, making them difficult to observe and improve upon. Currently, the infrastructure inspection equipment (substrate, blank, patterned mask, AIMs) needed for EUV mask manufacturing at the 16 nm half-pitch are being developed.

Solutions for protecting the masks from added defects during use, handling, and storage need to be developed and tested because there are no known pellicle options for EUV masks. EUV-pod as defined in SEMI E152 standard is the vehicle used for handling blanks and masks in critical manufacturing steps and for shipping among various factories. They are also used for in fab handling and exposure tools in the semiconductor manufacturing facilities. There are still works to be done in improving the SEMI Standard and the EUV-pod performance capability. Reticle storage requirements in HVM are being investigated.

Table LITH7 Imprint Template Requirements

Imprint may take several forms. The table lists requirements specific to ultraviolet nanoimprint lithography (UV-NIL), in which UV radiation is used to cure the liquid filling the template. Imprint templates have surface relief features that are the same size as the wafer features, but the area that needs to be controlled for CD, pattern placement, and defects is 16× smaller than for comparable 4× masks for other technologies. The mask specifications are developed the same way that optical mask specifications are but they are tighter because the magnification is 1×. Inspecting defects on these masks is difficult because the wafer requirements are translated directly to the mask as 10% of the wafer CD specification. The registration is also difficult but is shared equally in quadrature between the two masks and the system overlay.

Table LITH8 Maskless Technology Requirements

The requirements for wafer patterning using Maskless Lithography (ML2) are the same as the wafer requirements in the ITRS tables. There are several proposed equipment configurations for ML2 lithography. Each design has unique variations in key features such as accelerating voltage, number of columns/beams, writing strategy, etc. Proposed tools for ML2 wafer patterning have voltages that range from 5Kev to 100KeV. The variation in system implementation approaches makes defining a single, unique set of requirements difficult. Because ML2 does not include a mask, the error budgets may shift to allow more variation in the wafer writing system that normally shared between the tool and the mask in conventional optical or EUV lithography. However, the result on the wafer is the same regardless of the patterning technology utilized.

Data volume and transmission is a unique requirement for ML2 but each implementation has different needs and limitations.

ML2 implementations may require within field stitching. The specifications for stitching are covered by CD and LWR specifications.

There is potential to apply ML2 in combination with other patterning techniques. Using ML2 as a cut mask makes good use of the capabilities of ML2 while minimizing the limitations. A cut mask application greatly reduces the amount of data that written on the wafer, which increases the effective throughput. The critical CD and overlay requirements must be met by the primary imaging technique (193nm immersion, EUV, DSA, etc.) utilized in combination with ML2.

POTENTIAL SOLUTIONS

The potential solutions for leading-edge, critical layer lithography are presented in Figures LITH3A DRAM and MPU Potential Solutions and LITH3B Flash Potential Solutions. The order of the options represents the probability of a particular technology to be the dominant solution for a given technology generation with the most probable options listed first. All of the infrastructures required to use the lithography technologies at the time shown must be ready—including tools, masks, and resist. The limit of single patterning by immersion optical lithography at 193 nm wavelength is 40 nm half pitch. Below 40 nm, some form of double patterning or spacer doubling will be used. Flash memory is the pitch driver into the future. It is leading the way at the 22nm half pitch in 2011. It is using a spacer technology to achieve the half pitch with the litho imaging technology of the 45 nm node. Starting in this same year, MPU and DRAM will use either a double patterning or spacer technology. EUV is expected to be inserted in mass production in 2014 if all of the infrastructures are ready for the flash 16 nm and MPU/DRAM 25 nm half-pitch respectively. ML2 and Imprint still are a possibility at this time but they appear not to be the most cost effective solutions.

However, a likely option for the flash 16nm half-pitch technology is the self-aligned quadruple patterning (that consists in nesting two spacer double patterning schemes together). The post-optical alternatives are potential solutions at and below 22 nm half-pitch. Of the possible alternative technologies, multiple geographical regions consider EUV, maskless, and imprint lithography as potential successors to optical lithography. Considering only post-optical approaches, EUV is viewed as the most likely for 22 nm and 16 nm half-pitch patterning. Maskless lithography has been applied to niche applications for prototyping and transistor engineering and to low volume application-specific integrated circuit (ASIC) production, but its role could be expanded. Breakthroughs in direct-write technologies that achieve high throughput could be a significant paradigm shift, eliminating the need for masks and reducing cost and cycle time. Many technological challenges will need to be overcome for ML2 to be viable for cost-effective semiconductor manufacturing. Imprint lithography has the potential to be a cost-effective solution, but several problems need to be solved for this to happen, including the difficulties associated with 1× templates, defects, template lifetime, and overlay. This technology appears to have found a niche market in the pattern media market that will help evolve many of the solutions that are needed for the semiconductor market place. This technology also has beta tools strategically placed in the semiconductor community to help understand and solve its manufacturing difficulties.

It is unclear whether any technology currently identified as a potential solution will indeed be capable of meeting the requirements for MPU/DRAM 16 nm half pitch and below, necessitating innovative technology development. Among these, directed self-assembly, in which the molecular structure of the imaging material drives the sub-lithographic feature sizes and control, is thought to be a viable and promising option. EUV with wavelength of 6.x nm is a new technology for 11nm half pitch.

14 Lithography

Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions within industry and among industry, universities, and governments are necessary to narrow the options for these future generations and focus support to enable one or perhaps two technologies to be ready for manufacturing at the desired time. The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities for continued adherence to Moore's Law at Flash 16nm and DRAM 22 nm half-pitch and beyond. This shift will drive major changes throughout the lithography infrastructure and require significant resources for commercialization. These development costs must necessarily be recovered in the costs of tools, masks, and materials.

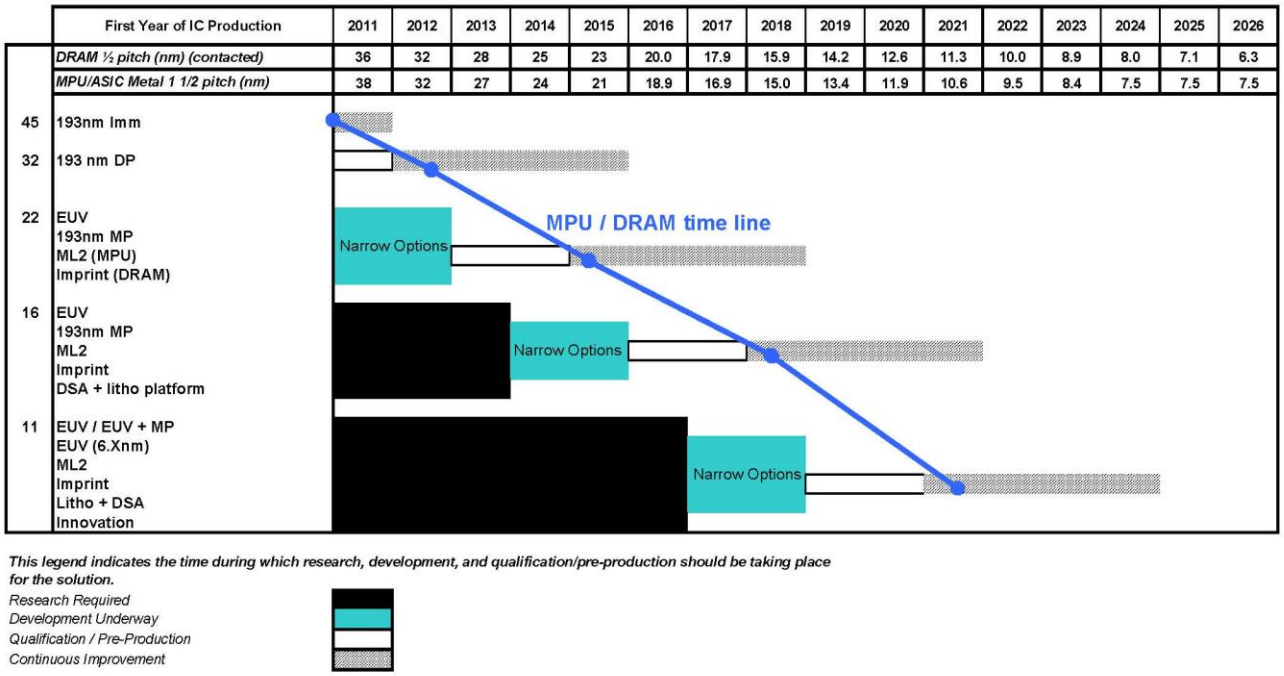


Figure LITH3A Lithography Exposure Tool Potential Solutions for MPU and DRAM Devices

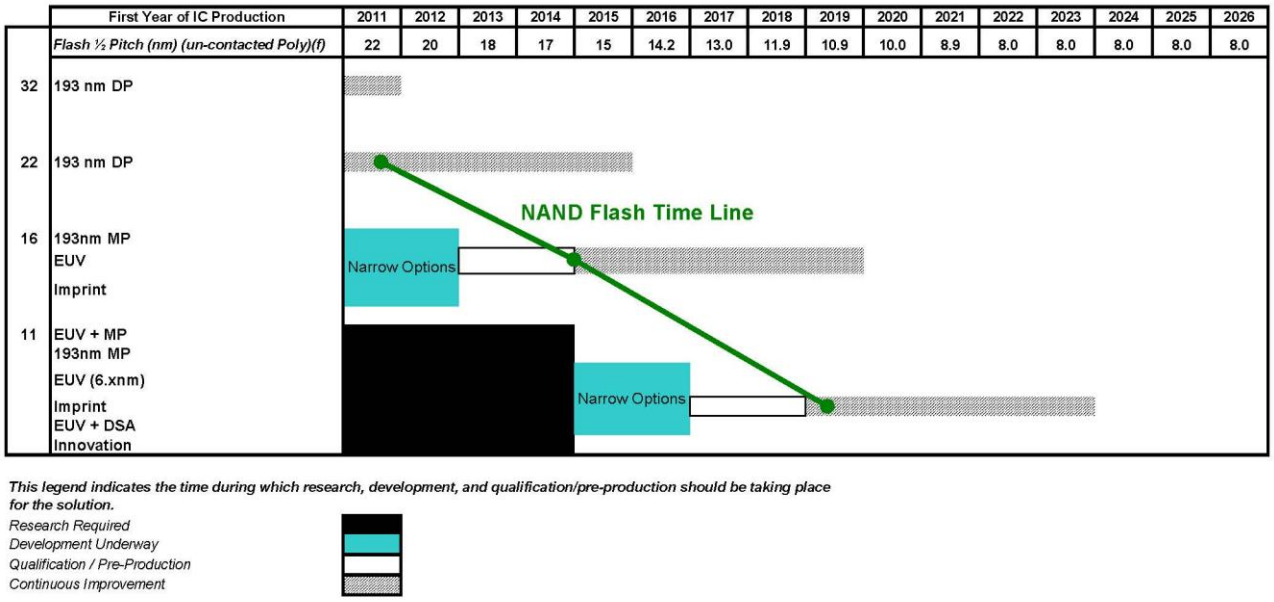


Figure LITH3B Lithography Exposure Tool Potential Solutions for NAND Flash Devices

CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions involving Lithography, *ESH*, *Factory Integration*, *Yield Enhancement*, *Metrology*, *Modeling and Simulation*, and *Emerging Research Materials* are outlined in this section.

ENVIRONMENT, SAFETY, AND HEALTH

Recent discussion of the continued use of perfluoroalkyl sulfonates (PFAS) in photochemicals has shown that long and commonly used materials can have ESH issues that only now are being comprehended. The introduction of new technologies necessarily means the use of materials and chemicals whose health and environmental implications are even less well known. One of the basic challenges is government ESH legislations and regulations become more aggressive but the global requirements less harmonized.

Practices for using and disposing of the chemicals used in lithography must evolve with careful regard for the safety of workers and their environment. Refer to the *Environment, Safety, and Health* chapter for comprehensive information.

FACTORY INTEGRATION

To maintain adequate process control, advanced process control capabilities are essential in the lithography cluster in the wafer fab. These capabilities are becoming increasingly important in mask-making facilities as well. Leveraging the learning from the wafer factory automation experience will also be essential to mask making. Several mask shops have developed custom solutions for automating data handling for defect inspection and repair. Further opportunities for automation exist. Leveraging existing standards that are used today in wafer fabs, such as the adoption of SECS/GEM into the mask-making tool infrastructure, will help reduce manufacturing errors.

An accurate wafer tracking system across various process modules is required to identify the working flow of any wafer in process. Several integrated metrology modules able to evaluate one or more parameters—CD, litho stack thickness, target profile, overlay, macro inspection with automated defect classification, and wafer flatness—are also recommended. Track and stepper/scanner should be able to use data recorded by any kind of internal or external sensors to adjust processes. Other possible requirements, which may call for major upgrades of equipment software and in several cases even of related hardware, include simultaneously managing different module flows on tracks to accommodate optimal metrology sampling plans and accepting overrides to downloaded (or selected) recipe set points. Moreover, on any track module, being able to

update all relevant set points wafer by wafer, even within the same lot, is desirable. On exposure tools, the software should allow the host to update dose, focus/tilt, and overlay input parameters wafer by wafer, even within the same lot or perhaps for each exposure field. Calibration, self-calibration, and matching activities on metrology modules should be allowed without a significant loss in litho cell throughput.

The efficiency of EUV sources also needs to be maximized to minimize the facility and power requirements to operate these sources at the power needed for high throughput EUV lithography. Specifically, the wall-plug efficiency of the sources needs to be increased to minimize the power to generate EUV photons and to cool the source components.

YIELD ENHANCEMENT

Yield enhancement is expected to become a major challenge as critical defect sizes become smaller than the limits of optical detection. Inspection systems are increasingly challenged to meet the required sensitivity and speed requirements. Non-optical methods of defect detection have not yet demonstrated the acquisition rates for controlling defects in semiconductor manufacturing on the entire wafer, but they are being used to control the lithographic hot spots and improve yield. Furthermore, die-to-database inspection of wafers is probably required for using ML2.

DFM practices are being used, but need to be developed further to minimize systematic sources of yield loss. Mask handling practices and storage to maintain EUV masks and imprint templates free from defects remain a significant challenge.

METROLOGY

Beyond the traditional challenges in lithography field (i.e. adequate measurements of wafer and mask level CD and overlay), the insertion of the EUVL option calls for extremely accurate metrology in material thickness (the most sensitive layer is the absorber in the EUVL mask fabrication) and surface roughness. Both parameters are expected to have impact on wafer CD uniformity. EUVL mask bow and local slope just before shipment to wafer factory are also relevant indicators to keep under strict monitor. In all these areas substantial improvements in metrology are requested to support the tight budgets required for a sustainable litho process.

Existing TMU (total measurement uncertainty which includes both accuracy and precision in a single metric) of CD measurement tools marginally meets the 20% measurement precision-to-process tolerance metric for the most advanced technology generations. Wafer and mask CD technology is evolving to meet the need for 3D measurements. A key requirement is the measurement of line width roughness. Measurement precision for LWR must even be better than line width precision. The quantitative effects of LWR on device performance need to be better understood to optimize metrology for LWR.

Overlay metrology is also challenged by future technology generations. Memory makers are requiring more stringent overlay control to achieve desired circuit yields. Traditional overlay test structures do not capture all possible overlay errors that can occur to phase shift and optical proximity correction masks. In the MPU arena, the usage of double exposure/double processing techniques will require even more accurate measurements to guarantee an adequate degree of alignment between the two masks composing the final layer layout and total CDU.

A key aspect to be also addressed in the next future is the detection and correct measurement of defects (both in unpatterned, i.e. in resist coated wafers, and patterned units, i.e. in developed wafers before etching) at sizes as tiny as few nanometers: again, proper solutions should be sought for. There is no commercially available equipment that can meet the requirements in HVM.

The complete discussion of Lithography Metrology is in the Lithography Metrology and Microscopy sections of the *Metrology* chapter, which also includes lithography metrology technology requirements and potential solutions.

MODELING AND SIMULATION

Support from modeling and simulation is critical both to push the limits of traditional optical lithography and to assess new next generation lithography technologies. Simulation of multiple exposure / patterning including database splitting is needed to support accurate and seamless implementation as MP becomes one of the main techniques to support feature sizes reduction in HVM. Taking advantage of computational lithography depends on continued improvement of mask writers and inspection systems to produce more complex patterns, and reduction of measurement uncertainty to calibrate accurate models. Integration of computational lithography with multiple patterning must address where it and pattern decomposition belong in the data flow from design to mask data preparation.

New techniques used in next generation lithography techniques, such as using reflecting masks for EUV lithography must be appropriately modeled and included in the simulation programs. Defect printability and CD impact as related to the sizes, height, and locations with the multilayers and defect optical properties are not well understood. Simulation and modeling are critical for the understanding of defect influences and possible compensation techniques. Simulation of maskless lithography by e-beam direct write (shaped beam/multi beam) including advanced resist modeling (shot noise and LER) is needed. In order for DSA to become a plausible lithography solution, it is also vital to have simulation of DSA of sub lithography patterns well in advance of the development phase.

A specific challenge for lithography modeling and simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as line edge roughness. Better calibration techniques are required to both develop models and to customize models in commercial tools to appropriately describe the photoresists in question. Calibration obviously depends on the quality of input data, for example, CD measurements. Therefore, measurement errors must be better understood and estimated. Systematic errors should be dealt with by models of the measurement tools. With the growing importance of LWR and LER, lithography simulation needs to help assess their influence on device and interconnect performance (LER) and variability (LWR). Since the roughness of etched structures and not the resist pattern ultimately affects device performance, intimate coupling between resist and etching simulation is indispensable. Intimate links with etching simulation must also be established to predict the geometry of non-ideal mask edges that frequently result from mask-making lithography steps.

See the *Modeling and Simulation* chapter for details on developments needed to satisfy these requirements.

IMPACT OF FUTURE EMERGING RESEARCH MATERIALS

Future device fabrication is expected to migrate from a lithography defined feature approach into combinations of lithographic patterning with various density multiplications or resolution enhancement techniques (RET). Some examples are sidewall spacer density multiplication and hole-shrink as well as Directed Self Assembly (DSA) density multiplication and hole-shrink.[12] This relaxes the resolution burden on lithography by using novel process, chemical resolution enhancement, and pitch enhancement techniques (PET). Since feature placement is a dependent on the initial lithographically generated mandrel or stencil, lithography tools must still continue to drive toward the overlay targets in the roadmap.

DSA is on the ITRS potential solutions list as a future patterning technology candidate. It provides resolution and pitch enhancement (RET)/PET by chemical phase separation.[13,14] The phase separated domains form masks for subsequent etch, and these domains are 'directed' (registered) by lithographic techniques such as pre-patterning stencils or pre-patterning chemical registration marks into the substrate.[14] Development of DSA has been proven for hard-disk patterned media[15], and now significant progress has been made towards demonstrating the potential for application to semiconductor fabrication [16,17]; DSA technology is rapidly moving from the research phase into development. There are multiple materials which must work synergistically to get low defectivity [18], CD control, and image placement. These new materials include not only the phase-separating polymers but also surface energy engineering of the guiding materials used in the stencils and the chemical registration marks.

The application of materials based patterning techniques will impact all aspects of lithographic technology, including masks, resists, exposure tools, and metrology. It will also require a substantial increase in the system development between lithographic patterning and materials development.

REFERENCES

[1] Andrew J. Hazelton, Shinji Wakamoto, Shigeru Hirukawa, Martin McCallum, Nobutaka Magome, Jun Ishikawa, Céline Lapeyre, Isabelle Guilmeau, Sébastien Barnola, and Stéphanie Gaugiran. "Double-patterning requirements for optical lithography and prospects for optical extension without double patterning", *J. Micro/Nanolith. MEMS MOEMS 8*, (2009).

[2] Christopher Bencher, Huixiong Dai, and Yongmei Chen. "Gridded design rule scaling: taking the CPU toward the 16nm node", Proc. SPIE 7274, (2009)

[3] Chris Bencher, Yongmei Chen, Huixiong Dai, Warren Montgomery, and Lior Huli. "22nm half-pitch patterning by CVD spacer self alignment double patterning (SADP)". Proc. SPIE 6924 (2008)

[4] Pitch doubling through dual-patterning lithography challenges in integration and litho budgets. Mircea Dusa, John Quaedackers, Olaf F. A. Larsen, Jeroen Meessen, Eddy van der Heijden, Gerald Dicker, Onno Wismans, Paul de Haas, Koen van Ingen Schenau, Jo Finders, Bert Vleeming, Geert Storms, Patrick Jaenen, Shaunee Cheng, and Mireille Maenhoudt*," Proc. SPIE 6520*, (2007)

[5] Mack, C. "Mask specifications: It's not getting any easier" *Microlithography World, (May, 2008).*

[6] Hughes, G., Yun, H., "Mask industry assessment: 2009," Proceedings of SPIE Vol. 7488, 748803 (2009)

[7] International EUV Initiative (IEUVI), http://ieuvi.org/index.html

[8] Chris H. Clifford, Tina T. Chan, Andrew R. Neureuther, Kenneth A. Goldberg, Iacopo Mochi, and Ted Liang. "Investigation of buried EUV mask defect printability using actinic inspection and fast simulation," Proc. SPIE 7488, (2009)

[9] Ichiro Mori, Osamu Suga, Hiroyuki Tanaka, Iwao Nishiyama, Tsuneo Terasawa, Hiroyuki Shigemura, Takao Taguchi, Toshihiko Tanaka, and Toshiro Itani. "Selete's EUV program: progress and challenges," *Proc. SPIE 6921*, (2008)

[10] Hakseung Han, Wonil Cho, Kenneth A. Goldberg, Eric M. Gullikson, Chan-Uk Jeon, and Stefan Wurm. "Determining the critical size of EUV mask substrate defects," Proc. SPIE 6921, (2008)

[11] Investigation of EUV mask defectivity via full-field printing and inspection on wafer. Rik Jonckheere, Dieter Van Den Heuvel, Fumio Iwamoto, Nickolay Stepanenko, Alan Myers, Matt Lamantia, Anne-Marie Goethals, Eric Hendrickx, and Kurt Ronse. "Investigation of EUV mask defectivity via full-field printing and inspection on wafer'" *Proc. SPIE 7379*, (2009)

[12] C. Bencher, et al, "Density Multiplication Techniques for 15nm nodes", SPIE 7973-19, 2011.

[13] D. Herr, "Directed Block Copolymer Self-Assembly for Nanoelectronics Fabrication", DOI:10.1557/jmr.2010.74

[14] D. Sanders, J Cheng, et al, "Integration of Directed Self-Assembly with 193nm lithography", J. of Photopolymer Science and Tech, Volume 23, number 1 (2010).

[15] Ruiz, R., Kang, H., Detcheverry, F. A., Dobisz, E., Kercher, D. S., Albrecht, T. R., de Pablo, J. J., Nealey, P. F., "Density Multiplication and Improved Lithography by Directed Block Copolymer Assembly", Science 321, 936-939 (2008).

[16] L.-W. Chang*, et al, "*Experimental Demonstration of Aperiodic Patterns of Directed Self-Assembly by Block Copolymer Lithography for Random Logic Circuit Layout" *IEDM*, p. 752, 2010.

[17] X.Bao, et al, "SRAM, NAND, DRAM Contact Hole Patterning using Block Copolymer Directed Self-assembly Guided by Small Topographical Templates", *IEDM* (Dec 2011).

[18] C. Bencher, et al, "Self-Assembly Patterning for sub-15nm half-pitch", SPIE 7970-14, 2011.