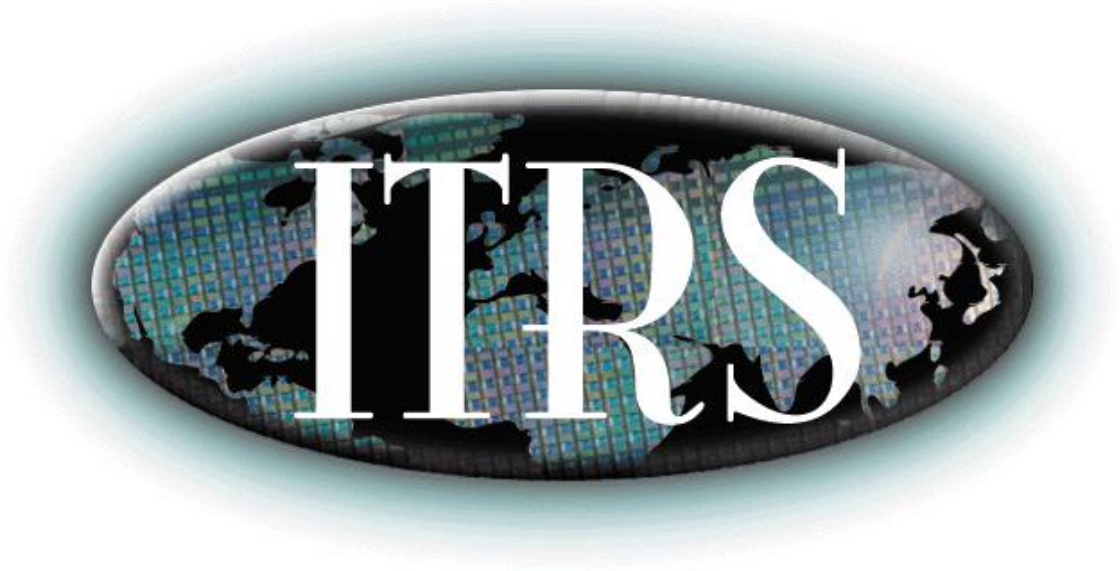

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR COMMUNICATIONS

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR COMMUNICATIONS

1. SCOPE

Radio frequency and analog/mixed-signal (RF and AMS) technologies are essential and critical technologies for the rapidly diversifying semiconductor market that comprises many more applications than the wireless communications market, which was the focus of this chapter in previous years. The *Systems Drivers* chapter discusses some of the circuit topologies for which we describe the requisite technology elements. While the circuits presented there address wireless and wireline communications, the RF and AMS chapter also considers requirements for low-frequency analog applications, for example, power management and display drivers.

The technologies presented herein depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe and others of which have not traditionally been compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table. Compound semiconductors become more significant as today's emerging research devices, especially those devices based on the More than Moore (MtM) technologies that are described elsewhere in this 2011 edition of the ITRS are deployed in the marketplace.

The purposes of this 2011 ITRS RF and AMS chapter are as follows:

1. Present the challenges that RF and AMS technologies have in meeting the demands of exemplary applications shown in Figure RFAMS1. Application frequency bands from 0 to 0.4 GHz, 0.4 GHz to 30 GHz, and 30 GHz to 300 GHz generally drive different technology requirements and this is reflected in the chapter. In future years, we will be addressing applications beyond 300 GHz as they emerge in the marketplace.

2. Present the challenges and requirements of Si complementary oxide semiconductor (CMOS), BiCMOS (bipolar + CMOS), and SiGe heterojunction bipolar transistors (HBTs), III-V compound semiconductor devices, High-Voltage MOS, and passive device technologies to meet the needs of these applications.

This 2011 RF and AMS Chapter presents the challenges, technology requirements, and potential solutions for the basic technology elements (transistors and passive devices) used in radio-frequency and analog/mixed signal circuits. It contains five technology-based sections on CMOS, bipolar, III-V, passive devices and HVMOS.

Analog - Carrier Frequency Bands			
LF Analog (0.0 GHz-0.4 GHz)	**RF (0.4 GHz-30 GHz)**	**Millimeter-Wave (30 GHz-300 GHz)**	**THz (> 300 GHz)**
Example applications			
Automotive controls	Cellular	60 GHz point-to-point	No products yet
On-chip regulators	WLAN	Imaging	
Power management	SerDes	Automotive radar	
	ADC,DAC	Wireless backhaul	

Figure RFAMS1 Analog and Carrier Frequency Bands and Example Applications considered in formulating this Roadmap

1.1. CMOS

As in previous years, the application drivers for the CMOS section are mobile transceivers in the 0.4 GHz – 30 GHz frequency range and various commercial applications in the 30 – 300 GHz frequency range. In addition, this year, the ITRS is putting additional effort to cover CMOS for mixed-signal analog applications. Therefore, we also consider the impact of CMOS device parameters on analog circuits that are not commonly used with RF application. A DC to high frequency wide-band amplifier is a typical building block seen in wire-line receivers with bandwidth reaching many GHz or higher. In optical communication with CMOS photonics, the data rate is already above 10 Gbps and is well on its way to top 40 Gbps and likely will reach 100 Gbps in the not too distant future. Wide-band trans-impedance amplifiers (TIA) are often used to convert photo-diode (PD) output to voltage levels suitable for CMOS digital signal processing.

The technology bases of this section are the CMOS devices of the *Process Integration, Devices, and Structures (PIDS)* chapter utilizing the low standby power (LSTP) roadmap for microwave applications and the high performance (HP) roadmap for millimeter-wave applications. The LSTP roadmap was selected as the basis for mobile microwave applications because portable applications require lower standby power and higher bias voltages than afforded by HP CMOS. The HP roadmap was selected for millimeter-wave applications because of the added device performance. The devices in the RF and AMS roadmaps are assumed to be identical to those in the PIDS roadmaps, but modifications may prove necessary if key analog properties cannot be realized. Contrary to previous editions of the RF and AMS roadmaps, the devices are now placed into production concurrently with the PIDS roadmap to reflect the System-on-a-Chip (SoC) nature of some applications requiring RF and AMS functions on mainly digital chips. The quality of high-frequency models and other tools to support RF and AMS design may improve over the first few years of production. The roadmap treats a performance-RF/analog device modeled after the LSTP or HP device. Such devices are used in circuits for transceivers; frequency synthesizers, frequency converters and amplifiers. Supporting analog-specific applications requires device characteristics that are difficult to achieve with scaled MOS. Driving RF signals off-chip also requires higher voltage devices. Requirements for such devices include analog precision MOS device scaling and relatively high voltage compatibility to achieve high signal-to-noise ratios and low signal distortion. Such devices are typically available in CMOS technology offerings to support interfacing to higher-voltage input/output (I/O) ports. The performance of these devices can be found technical requirements sections of prior years of the ITRS RF and AMS chapter. Furthermore, many foundries also are including optional analog-friendly FETs in their CMOS offering. For such devices, the DC voltage gain

would increase with increasing gate length in contrast to digital FETs where the halo implant causes the gain to effectively saturate and remain constant with increasing gate length. [1]

1.2. SILICON BIPOLAR AND BICMOS

1.2.1 DEVICES COVERED BY THE ROADMAP AND THEIR APPLICATIONS

Bipolar transistors covered by this roadmap are Si/SiGe heterojunction bipolar transistors (HBTs). The roadmap does not cover all types of Si/SiGe HBTs available in today's technologies, but focuses only on those for which performance increases are driven by RF/AMS applications. Wireless transceiver applications in the 0.4 GHz to 5 GHz range used to be the largest market for bipolar and BiCMOS technologies, but these applications are now moving to RFCMOS technologies. High-voltage NPN and PNP bipolar transistors are used and are the topic of research for applications operating at frequencies below 5 GHz such as cellular and WLAN power amplifiers (PA), operational amplifiers, etc. These developments are tied to specific applications for which the performance of the bipolar transistors may no longer be the key driver. As an example, performance and cost of cellular and WiFi PAs are now dominated by the integration choices (passives, packages …). The roadmapping exercise of these devices is complicated because establishing the link between device and product performance may not be clear. For this reason, it has been decided to drop the PA NPN transistor from this chapter. Therefore the scope of this section is then to provide requirements for high-speed NPN (HS-NPN) and high-speed PNP (HS-PNP) devices, which remain drivers for their respective applications. Research on these devices also provides benefit to high-voltage NPN and PNP devices.

Improvements in the performance of the HS-NPN device are driven by the requirements of millimeter-wave products. These include circuits for wireless (~60 GHz WLAN) and wireline communications (40 Gb/s, 100 Gb/s Ethernet and beyond), automotive radar (~77 GHz) and emerging applications up to ~170 GHz for industrial, medical, security, space, radio-astronomy, and other technologies. [2,3] The goal of extending the performance of the Si/SiGe HBTs is twofold. First, it is to allow the robust design of systems forecasted to operate at frequencies up to ~300 GHz by the end of the roadmap (which corresponds to ~ f_{MAX} / 3). Secondly it is to improve the performance (gain, noise figure, power consumption, etc.) of circuits operating at lower frequencies for existing applications; those already addressed or targeted by present bipolar / BiCMOS technologies.

The HS-PNP roadmap is driven by the applications of complementary bipolar and BiCMOS technologies (C-BiCMOS). Complementary bipolar circuits are attractive for (operational) amplifiers with low quiescent power consumption and high linearity across a large frequency range that often includes DC. Typical applications include: analog to digital conversion, high speed operational amplifier, and cable drivers for video and hard disk R/W head.[4]. These circuits greatly benefit from complementary technologies that offer NPN and PNP transistors with matched performance. Because PNP transistor development has significantly lagged that of the NPN, performance improvements for these applications tend to be limited by the PNP transistor. However, the PNP device technology has improved considerably in the last decade due to introduction of affordable silicon-on-insulator technology and SiGe PNP devices. The HS-PNP roadmap seeks to provide a set of goals to continue these improvements in order to address the increasingly demanding specifications of the applications listed above.

1.2.2 BIPOLAR / BICMOS TECHNOLOGIES SPECIFICITIES

The years indicated in the bipolar roadmap are not the start of production year but rather the start of prototyping year. The life span of BiCMOS technologies (defined by length of time at a significant production volume) is much longer (~10 years) than that of CMOS technologies. This is because, for a given application, they may not benefit appreciably from simple (critical dimension) scaling. The end result is that BiCMOS technologies are not available for each CMOS node. For these reasons, the roadmap provided here does not attempt to tie bipolar performance to a given CMOS node. CMOS node choice depends on many factors, some of which are company specific: bipolar performance requirements, gate density requirements, process integration compatibility, development time, and cost. However, a year-by-year roadmap is maintained to reflect the continued increase in bipolar performance as applications require higher operating frequencies.

Today, the most advanced BiCMOS technologies utilizing the HS-NPN offer 180 nm and 130 nm CMOS. This represents a four to five generation technology-node gap between advanced CMOS and BiCMOS technologies. This is explained by the lack of product drivers requiring dense digital functions, the cost advantages of integration on mature CMOS nodes, and the ability to achieve excellent HS-NPN performance at these CMOS nodes. In the coming years, 90 nm to 45 nm BiCMOS technologies could appear for mm-wave SOC applications that cannot be addressed by pure CMOS technologies. HV-BiCMOS technologies, which include C-BiCMOS, usually lag behind HS-BiCMOS technologies with

CMOS nodes ranging between 350 nm and 180 nm today. They tend to cover applications for which large gate densities are usually not required and for which cost is of primary importance.

1.3. COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

In previous editions of the RFAMS chapter, III-V compound semiconductor devices were treated in two different sections, each associated with their applications, namely power amplifiers (0.4 – 10 GHz) and millimeter wave (10 – 100 GHz) and integrated into tables with silicon based devices. For 2011 III-V devices are being addressed as a single group covering the frequency range of 0.4 – 300 GHz. We have extended the upper frequency range to 300 GHz to cover the traditional millimeter wave frequency band (30 – 300 GHz). For RF, microwave, millimeter wave and mixed signal applications, if the performance requirements can be satisfied by silicon they will be, primarily for cost and integration density reasons. Therefore, the drivers for continued development of III-V devices are based on applications that require higher frequency, wider bandwidth, higher power, higher gain, higher dynamic range, higher efficiency or lower noise performance than can be achieved with silicon based devices. III-V devices will continue to serve niche or performance driven applications where silicon performance is not adequate. In addition, recent advances in the heterogeneous integration of III-V devices with Si CMOS on silicon substrates will enable the realization of RF and mixed signal circuits that take advantage of the superior performance of III-V devices and the high integration density of Si CMOS.

1.3.1 MICROWAVE DRIVERS

Wireless communications require both portable and fixed transmitters and receivers to form a connected network. The public is most familiar with portable devices that take the form of cellular telephones and wireless personal digital appliances (PDAs). The III-V devices required to implement these services include: III-V HBTs in power amplifier (PA) modules in portable devices and GaN FETs or HEMTs for high voltage devices in base station power amplifiers. The key driving forces for these two devices are integration of components and cost.

For portable applications, the PA module is a multichip assembly that contains a Si power management chip, RF matching networks, RF switches, and PA chips capable of supplying 1 - 4 watts of RF power to the antenna. While silicon technology is typically used for power control circuitry and the switch functions, GaAs HBTs are typically used for the power amplifier chips. The trend is to combine several components/functions on the same semiconductor chip. For example, PA controller function is being combined with the switch function or the PA controller could be integrated with the PA. Even some linear PAs are starting to include a CMOS-assist bias circuit to meet stringent current consumption vs. output power requirements. Combining several different PA module functions on a single chip reduces component count and wire bonding complexity and may lead to lower cost modules. These technology combination approaches will become more prevalent as PA modules are required to service an increased number of frequencies and modulation formats in years to come. The choice of which technology to use for each function depends on the RF performance specifications, die size, availability, and most importantly, total product cost.

The cellular base station, which also contains power amplifiers, completes the communications link between MULTIPLE portable devices. Compared to handsets, however, substantially higher power RF devices up to 300 W are required to achieve the desired cellular phone coverage. A single base station may contain multiple of these 300 W devices to handle all of the cellular phone traffic at a particular base station site. Operating frequencies range between 400 MHz and 3.5 GHz. The heart of base station transceiver is the RF semiconductor power device that must provide the final amplification to the data signal in order to achieve the desired output power. Typically, several semiconductor devices are connected in parallel to achieve these high powers. While Silicon LDMOS transistors are now the technology of choice for cellular systems from 400 MHz through 3.5 GHz because of their combination of technological maturity, good performance, and low cost, Gallium nitride (GaN) continues to receive considerable attention as a potential next generation device technology. Gallium nitride has power densities four to five times greater than LDMOS. This tremendous increase in power density is the result of GaN's higher breakdown voltage and higher current density that offer many advantages to the PA design. For the same amount of power, GaN HEMT device capacitances are also much lower leading to the ability to increase instantaneous bandwidths without losing efficiency - this is key to next generation 4G/LTE+ systems. Other additional reasons for using GaN-on-SiC for Basestations:

- For Remote Radio Heads
  - High efficiency
    - Power Supply Economies
    - Heat Sink Economies

  - Small form factors
  - Lighter weights and wind loading factors
  -
- For LTE/4G + Higher Data Rates
  - Larger bandwidths not possible with Si LDMOSFETs
  - Co-location for several frequencies and standards
  - Higher power than present systems
  - Higher peak to average ratios than present systems (up to > 10 dB)
  - Efficiency enhancements with increased bandwidths
  -
- For Pico-cells and Femto-cells
  - GaN HEMT MMIC building blocks for average powers up to several watts

Similar drivers exist for microwave transceivers for point-to-point communications systems like LMDS and radar and multifunction systems used for military applications. Microwave transceivers are typically multichip assemblies similar to the PA module in portable devices, and, in the case of radar and multifunction systems used for military applications, multiple transceivers are assembled into a phased array for electronic beam steering. Control functions are realized in silicon, whereas the power and low noise amplifiers are typically realized in GaAs pHEMT, with some systems using either GaAs MHEMT or InP HEMT in the receive chain due to superior noise performance. In recent years the trend has been to higher levels of integration and for some applications with less stringent power or noise requirements the entire transceiver is being realized in SiGe BiCMOS. In addition, for applications requiring higher power, GaN HEMTs are beginning to replace the GaAs pHEMT PA.

Note: In the tables and chapter, less emphasis has been placed on III-V devices for RF and microwave frequencies. This decision is based on the fact that III-V devices for RF and microwave applications (< 30 GHz) are mature, production devices available at multiple foundries. The main drivers for device improvements for RF and microwave applications are not device performance or scaling, but rather cost, linearity/dynamic range/efficiency, and integration density. Cost and integration density are a function of manufacturing maturity, whereas linearity/dynamic range/efficiency depend on circuit design techniques.

1.3.2 MILLIMETER WAVE DRIVERS

Commercial interest in the mm-wave spectrum has grown steadily over the past decade. Unlike most of the lower frequency spectrum, where silicon based technologies dominate, III-V devices still provide a distinct performance advantage at millimeter wave frequencies and a number of III-V materials and device technologies compete in the applications marketplace. This is in spite of recent advances in device performance and circuit design techniques that has enabled silicon to start capturing the mm-wave application space, as well.

Each of the III-V technologies offers unique tradeoffs in cost, performance, and availability. Currently, III-V devices and integrated circuits are manufactured on three substrate materials: GaAs, InP, and SiC.

For performance driven applications in which high levels of integration are needed, we expect a drive towards heterogeneous integration of III-V and silicon technologies. Such an approach would enable designers to take advantage of the high-frequency performance of the III-Vs and the high-density integration and processing capabilities of silicon. In the future, we may see other III-V compound semiconductors, and even carbon-based semiconductors, including diamond and graphene, being developed for this spectrum.

In this section we present III-V transistor technologies, which are, or are forecast to be, in commercial production. Because this field is rapidly expanding, and because performance is not tied so tightly to lithographic dimensions as are digital integrated circuits, we have purposely omitted projections into the long-term years. III-V semiconductors do not enjoy the long-term heritage of silicon-based devices, nor do they follow Moore's Law. As the mm-wave spectrum markets and products develop and become more of a technology driver, it may be more plausible to carry the roadmap for mm-waves into the long term for future ITRS editions.

The scope of this section includes low noise and power transistors that are based on the following materials and device technologies: GaAs PHEMT, GaAs MHEMT, InP HEMT, GaN HEMT and InP HBT. All device types employ epitaxial layers that are composed of ternary or quaternary compounds derived from column III and V of the periodic chart. There is great diversity in the nature and performance of these devices because device properties are critically dependent on the selection of materials, thickness, and doping in the epitaxial layers that are proprietary to the manufacturer. Trade-offs

exist among power, efficiency, breakdown, noise figure *(NF)*, linearity, and other performance parameters. One consequence of these trade-offs is that the "lithography roadmap" is not the only driver for III-V performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit, such as maximum transit or cutoff frequency (f_T) and maximum frequency of oscillation *(f_{MAX})*. Performance trends are driven primarily by a combination of desirable trade-offs and "bandgap engineering" of the epitaxial layers in concert with shrinking lithography.

1.4. PASSIVE ON-CHIP DEVICES

Passive elements are indispensable in analog and RF systems and are used for matching networks, LC tank circuits, attenuators, filters, decoupling capacitors, loads, and more recently, on-die antennas or antenna reflectors. Passive elements can be simply classified into distributed elements including transmission lines, waveguides and antennas, and lumped elements including inductors, transformers, linear and variable capacitors (varactors) and resistors. The distributed circuits take into account the phase shift occurring when the signal wave propagates along circuits. As the operating frequency moves into the microwave and millimeter wave spectrum, distributed passives are used more frequently because they have larger quality (Q)-factors. On the other hand, lumped elements have physical dimensions which are insignificant with respect to the wavelength, typically less than $\lambda/20$, so that phase effects may be ignored. They are typically used at RF (GHz) and lower frequencies, but also at microwave and mm-wave frequencies when their physical dimensions are small. The scope of this section includes primarily lumped passives as on-chip (SoC) components such as:

1) linear capacitors,

2) resistors,

3) inductors and

4) varactors.

The on-chip lumped passives are used pervasively in applications in the Low Frequency (LF) analog (from direct current (DC) to 0.4 GHz) and Radio Frequency (RF) (from 0.4 GHz to 30 GHz). However, they are sometimes used through the mm-wave and higher frequencies as well. Therefore, some discussion also given for passives employed in the higher frequency ranges of mm-waves from 30 GHz - 300 GHz.

Because the low frequency analog and mixed signal applications require uniform and stable linear capacitors and resistors, the roadmap addresses voltage and temperature coefficients and matching as their key parameters. RF and microwave applications (0.4 GHz to 30 GHz) impose the additional requirement for high Q-factors of energy storage for inductor and capacitor (L/C) components. The Q-factor limitations of L/C passives integrated on-chip originate primarily from the resistive losses in series connections and the parasitic capacitors in parallel connections. These losses and parasitics are significantly affected by the silicon substrate and, increasingly, by the processing features associated with interconnects, vias, and metal fills and slotting. Further interdependency on properties of the interconnects is prominent at the highest frequency range of 30-300 GHz addressed in this section. This high frequency range makes use of distributed passive components, e.g., transmission lines. The figures of merit for transmission lines include the loss per unit length and per unit area and are determined mainly by the basic interconnects R-L-C characteristics.

The ITRS Chapters on Assembly and Packaging and on Interconnects contain sections on off-chip passives. This section focuses exclusively on on-chip passive devices.

1.5. HIGH VOLTAGE MOS

High-Voltage (HV) MOS devices can be defined as those MOS transistors designed to support a drain-to-source voltage substantially greater that the maximum allowable gate-to-source voltage. The application drivers for the HVMOS section are portable devices. Specifically, we treat the NMOS and PMOS high-voltage transistors to support power management and display driver applications. While this is a limited set of the applications of high-voltage MOS devices, these allow the creation of this new technology section of the RF and AMS chapter which will expand in time. The key FOM for each device is the breakdown voltage, which determines the maximum drain-to-source voltage a transistor can tolerate and is driven by application requirements. The gate-to-source voltage is limited by the thickness of the gate oxide. We assume these devices are formed using the gate oxide of the digital CMOS or that of the accompanying IO FETs that are typically included in a CMOS offering, thereby limiting gate-to-source voltage to less than 3.3V. The other important FOM is the on- resistance (R_{ON}), which determines the low-limit of voltage across the transistor in the on-state. We also consider the digital CMOS lithography node onto which the HVMOS devices are integrated. Other FOMs, while they may be

important factors in differentiating a technology offering, are not considered, due to the lack of consensus among the few participants in the roadmapping effort. They include the energy capability, which determines the highest safe operating voltage of the transistor in its on-state, and the breadth of the menu of passive devices offered with HVMOS. The scope of this roadmap will expand in future years with the growth of interested membership.

2. DIFFICULT CHALLENGES

2.1. CMOS

It is easy to assume that the steady improvement in the digital performance of the basic devices in the HP and LSTP roadmaps derived from scaling will also result in continuous improvement in RF and analog performance. But in fact, many of the dimensional, materials-oriented, and structural changes being invoked in the digital roadmap degrade or at least alter RF and analog device behavior. For example, it is well know that the halo or pocket implant degrades transistor gain even at long channel lengths. As dimensions shrink, new tradeoffs in physical design optimization for RF performance will be necessary as different mechanisms emerge as limiting factors determining parasitic impedances in local interconnects to the device.

The gate resistance, for the most part ignored in considering the performance of digital circuits, becomes a critical limiter of RF FOMs. Consider the expression for the minimum noise factor of a FET. [5]

RFAMS-EQ (2.1.1) $$F_{MIN} \approx 1 + \frac{2f}{f_{Teff}}\sqrt{k_1}\sqrt{g_m(R_g + R_s) + 1}.$$

Also consider the following expression for maximum frequency of oscillation,[6]

RFAMS-EQ (2.1.2) $$f_{MAX} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g)g_o + 2\pi f_T R_g C_{gd}}}.$$

The conventional definitions of the variables apply; R_i is the intrinsic channel resistance, R_s in the series resistance, R_g is the gate resistance, g_o is the output conductance, g_m in the transconductance, C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitance. High gate resistance reduces f_{MAX} and raises F_{MIN}. For a given device, gate resistance depends on the specific details of the device geometry. For example, assume a gate contacted from two-sides as shown below. Furthermore, assume that the gate is composed of a stack of material(s) that can be characterized by a horizontal sheet resistance, R_{SH}. Then, one can find an optimal channel width, minimizing gate resistance, as follows.

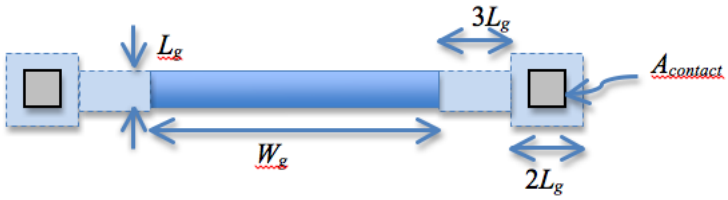


Figure RFAMS2 An Illustration of the Physical Layout of One Gate Finger of a MOSFET

The gate resistance is modeled to have 3 additive components: 1) contact resistance (two in parallel for the structure shown), 2) horizontal resistance of the link between the contact and active gate, and 3) the active gate resistance) as

RFAMS-EQ (2.1.3) $R_{GATE} = R_{CONT} + R_{LINK} + R_{ACTIVE}$.

The contact contribution is given by the via resistivity divided by the contact area. To this is added the resistance of two horizontal links between the contacts and the active gate. The horizontal contribution of the active device is given by the well-known expression for distributed gate resistance contacted on both sides.[7] Here the link regions are assumed to be three gate lengths. This gives the expression,

RFAMS-EQ (2.1.4) $$R_G = \frac{r_{via}}{2A_{contact}} + \frac{3}{2}R_{SH} + \frac{R_{SH}W_g}{12L_g}$$

Optimum gate width is generally found empirically, considering effects of parasitic capacitances of a given layout, the FOM one is trying to optimize, and resistances intrinsic to the transistor. For example, considering the term (R_s + R_g) in the expression for F_{MIN}, one could find the optimum gate width as;

RFAMS-EQ (2.1.5) $$W_{g,opt.} = \sqrt{\frac{12L_g R_s'}{R_{SH}}}$$

where R'$_s$ is the source resistance expressed in Ω-m. For estimating the figures of merit (FOMs) presented in the Technology Requirements we used an empirical value of device width based on recent publications and the authors' experience and scaled this in time proportionally with gate length.

Consider next the gate-to-drain and gate-to-source capacitances found in the expressions for f_{MAX} above or for the cutoff frequency,[8]

RFAMS-EQ (2.1.6) $$\frac{1}{2\pi f_T} = \frac{C_{gs}+C_{gd}}{g_m} + C_{gd}(R_s+R_d) + (C_{gs}+C_{gd})(R_s+R_d)\frac{g_{out}}{g_m}$$

Typical device models capture only the intrinsic transistor capacitances, or in the common practice for high-frequency models, they will capture wiring capacitances of the first or second level of wiring for a specified device layout. This permits a single model to represent the behavior of the device in many wiring configurations but requires that parasitic impedances of the wiring be extracted and included in circuit simulations. This presents a challenge especially for mm-wave designs, which typically wire individual transistors to transmission lines formed on the top metal level.

As reflected in the HP and LSTP roadmaps, fundamental changes in device structures such as the introduction of multiple-gates and/or fully depleted SOI will be required to sustain continued performance and density improvement. These structures prohibit a contact to the device body. Thus, the electrical characteristics of these devices are fundamentally different from those of conventional CMOS. Potential benefits include higher voltage-gain and lower coupling between the drain and body. But these differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries. Thus, the fabrication of conventional precision analog / RF driver devices to be integrated alongside the scaled CMOS devices may require separate process steps. Even now, the impetus to enable system-on-chip (SOC) applications is encouraging the incorporation of optional analog or high-voltage devices and thereby expands the menu of potential devices albeit with the attendant cost increases.

2.2. SILICON BIPOLAR AND BICMOS

The primary challenge for the HS-NPN is increasing the unity current gain cut-off frequency f_T by more aggressive vertical profiles while still maintaining $f_{MAX} > f_T$ i.e. low base resistance and low base-collector capacitance (C_{BC}). A number of novel device architectures have been proposed with new self-alignment schemes to improve the $R_B \times C_{BC}$ trade-off. Continued development and evaluation of these architectures is required to drive manufacturing robustness for these solutions. In addition, BiCMOS compatibility for these structures needs to be proven, as digital content requirements for the highest frequency applications will likely increase over time. The second major challenge facing bipolar devices, in general (including III-V), is the reduction of the emitter width in order to mitigate the increase of peak f_T operating current. With decreasing collector thickness and increased collector doping the peak f_T current density (J_C) will increase up to 30 mA/μm². It serves to increase the base-collector junction switching speed (C_{CB}/I_C) but handling this current from both a wiring and a self-heating perspective is increasingly challenging. One way of reducing the total current and power is to reduce the emitter width, which is lithographically not challenging given that current emitter widths are around 0.13 μm, but the obstacle lies in the emitter resistance. Key portions of the emitter resistance are the interface resistances formed at the via-silicide-poly interface and at the emitter poly to base junction region, which scales as the inverse emitter area.

Similar to the HS-NPN, the main challenge for the HS-PNP is increasing f_T by more aggressive vertical profiles. In addition to the inherent minority carrier mobility differences between electrons and holes, shrinking the vertical profile of a SiGe PNP is more challenging because it requires controlling the valence band offsets to avoid the appearance of parasitic barriers. Another challenge for the HS-PNP is the difficulty of the co-integration with HS-NPN and CMOS. This integration always adds more constraints on the HS-PNP fabrication.

2.3. COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

III-V compound semiconductor technologies have a number of similarities with silicon technologies and yet in many ways are distinctly different. Among the unique challenges faced by III-V devices are yield (manufacturability), substrate size, thermal management, integration density, dielectric loading, and reliability under high fields. Among the challenges common with Si based circuits are the need to improve efficiency and linearity/dynamic range, particularly for power amplifiers for communications applications.

Unlike silicon based circuits technology, III-V microwave and millimeter wave circuits are typically built on high resistivity or semi-insulating substrates. Semi-insulating GaAs wafers that are 150 mm in diameter are routinely available and are becoming the *de facto* standard, although many foundries still manufacture 100 mm. The move to larger diameter substrates will be driven not only by economies of scale and chip cost but also by equipment availability. GaAs tends to be two generations behind Si in wafer size, with InP and SiC one generation behind GaAs. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from the advances in processing equipment. Today there is no production source of semi-insulating GaN substrates. Most GaN device epitaxy relies on SiC for a host substrate and several firms now supply GaN epitaxial layers, tailored to customer specifications, on SiC substrates. Device quality, high resistivity SiC substrates are now available in 100 mm diameter from multiple suppliers, with plans to scale to 150 mm based on industry demand. Recently, significant progress has been made on the growth of GaN on Si and device quality GaN epi on 200 mm diameters wafers has been demonstrated. However, this development is being driven by the power conditioning/converter circuit market whose circuits operates in the MHz frequencies and do not require high resistivity substrates. The growth of GaN on Si opens up the possibility of fabricating GaN circuits in a silicon foundry as well as the heterogeneous integration of GaN amplifiers with Si CMOS control circuitry.

Power amplifiers are among the largest uses of III-V devices. Improving amplifier efficiency is a major challenge for III-V power amplifiers for all applications including commercial (e.g, handset and base stations), military (e.g, radar) and millimeter wave. This is primarily being addressed by exploring more efficient amplifier architectures: Doherty, drain modulation, and higher efficiency classes of operation (Class D, Class F, and Class S). These high efficiency architectures must continue to meet the stringent linearity performance requirements and cannot substantially increase system cost. Adaptive digital pre-distortion (DPD) designs where the input signal is pre-distorted in the digital domain to compensate for device non-linearities will help meet the linearity requirements. The adaptive behavior of the pre-distorter also mitigates issues with thermal time constants and device performance drift over time. For example, for base stations, GaN may offer advantages over LDMOS in certain classes of high efficiency architectures. Today, the above linearization techniques are realized in multichip assemblies. Higher levels of integration and/or the heterogeneous integration of III-V devices with Si CMOS control circuitry could offer compact, higher performance, lower cost solutions.

High efficiency architecture deployment represents an opportunity to design devices with attributes that are compatible with the architecture and can further enhance efficiency. For example, a Doherty-friendly device will have peak power and peak efficiency impedances designed to achieve maximum benefit from the load modulation that this architecture relies upon to improve efficiency without sacrificing peak power. The figures-of-merit that drive device development are a function of the PA architecture. Improving such figures of merit may potentially lead to devices that are designed for a specific PA architecture. That is, a device designed for use with a Doherty amplifier may not perform well in an input signal envelope tracking architecture. Understanding these figures-of-merit will enable device manufacturers to further enhance PA efficiency.

Another major challenge facing power amplifier devices and modules for communication and radar is the need to increase their functionality in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity requirements at the same or lower cost. For example, the consumer expects increasing portable device functionality without a substantial increase in portable device cost. Meeting these conflicting requirements is the biggest challenge facing the development of future PA modules. Some examples of recent customer requirements that impact technology choices are listed below.

For linear PAs used for such protocols as code division multiple access (CDMA), personal communications services (PCS), wideband CDMA (WCDMA) and the like, there is increasing focus on mid-power (16 dBm) efficiency. There are two popular solutions to this problem currently. The first is using a balanced architecture that requires no new process development. The second is including on-chip switching to by-pass one or all of the PA stages. This on-chip switching drives the integration of RF FETs and HBTs on the same die. More recently, such integration is being extended to have the efficiency measured at multiple power points that increases the complexity of the bias control and switching operations.

Load-insensitivity is another challenging requirement. Phone manufacturers are asking PA vendors to develop modules that are not sensitive to the load that the PA module sees. Previously, the major requirement was that the PA should be robust enough to withstand the voltage standing wave ratio (VSWR) when the isolator was removed. The current challenge is to meet performance specifications (e.g., noise figure, linearity, and PAE) over the same VSWR condition. The responses to this challenge will be varied and place differing demands on the selected technology.

PA users are requesting increasingly sophisticated bias circuits. Some examples of user requests include: 1) enable pins/mode control, 2) temperature compensation circuitry, 3) automatic bias control in which the PA senses power and resets bias based on the power it senses, and 4) circuits that do not require a reference supply voltage. The above request 3 may require integration of the power detector/coupler into the PA module. Also, using only npn transistors to meet the above request 4 is challenging. In general, meeting the above requests or demands is the driver for BiFET integration where the FET is required to be a high quality analog FET. Continued emphasis on this area also makes BiCMOS, although it has RF shortcomings, an attractive alternative to GaAs HBT.

Enhanced data rates for global system for mobile (GSM) evolution (EDGE) PAs are typically integrated with GSM PAs, so there will be some convergence of the needs of linear PA and saturated PAs as PA designers must now provide linear operation as well. Some future modules may contain, not only the GSM-EDGE PA described above, but also long term evolution (LTE) and WCDMA – high speed packet access (HSPA) as well which will require more switching functions and possibly built-in load-tunability to minimize the number of required amplifiers while still maintaining specification compliance. LTE is a set of enhancements to the Universal Mobile Telecommunications System (UMTS) that will be introduced in the 3rd Generation Partnership Project (3GPP) Release 8. Much of 3GPP Release 8 will focus on adopting 4G mobile communications technology.

Another challenge that is presented to all portable applications is the migration of battery technology. The likely near-term decrease in the end-of-life battery voltage presents a major technology and design challenge to PA vendors. This has huge implications for what has to happen at a system level. The PA will still need to work on a 4 V to 5 V charger, but also operate at lower voltages such as 2.4 V. Thereby, the operating range of the PA will increase. If the required output power remains unchanged, then some form of load-line switching will needed. Whether or not the phone manufacturer supplies this or the PA supplier will impact the choice of technology used. Another consequence will be that the transistors used in the power amplifier will be required to operate at a much higher current density to meet the same requirements and this will also have ramifications for which technologies can be used.

The incredible cost sensitivity and the fact that PAs tend to use a system-in-a-package (SIP) approach make the technology trends difficult to forecast.

The challenge facing the adoption of GaN FETs for base station applications is continual product price pressure even though the technology offers outstanding advantages compared to Si technology. Inevitably when production volumes exceed millions of transistors for new infrastructure applications in the next few years the cost reduction curve will be relatively dramatic just as happened with GaAs and SiGe technologies for handsets.

Additional III-V device challenges include:

1. Reliability of scaled devices, particularly for power applications
2. Efficient production techniques for fabrication of through substrate vias (TSVs) required for low inductance grounds in microstrip circuits;
3. Techniques for heat removal including wafer thinning and site specific cooling for high power density devices such as GaN;
4. High breakdown voltages for power devices and associated passive components, such as capacitors and thin film resistors;

5. Non-native oxide passivation and dielectric materials for mixed signal, enhancement/depletion (E/D) mode devices and scaled devices.
6. Reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
7. High yield multilayer interconnects for mixed signal and increased functionality of PA and transceiver modules including understanding and mitigating impact of dielectric loading on FETs due to multi-layer interconnects/dielectrics
8. Overall yield and uniformity improvements to drive cost

2.4. PASSIVE DEVICES INCLUDING RESISTORS, INDUCTORS, CAPACITORS, AND VARACTORS

The implementation of on-chip passive components required for RF and AMS circuits poses serious challenges to SoC integration of these functions. The processes to form the active transistor devices and the interconnects can be utilized to form passive elements but frequently, dedicated masks and processing steps are required to implement these devices with desirable properties. So, the co-integration of active and passive devices introduces process complexity and can lead to manufacturing control challenges.

The parasitic impedances such as capacitance of interconnects, resistances of the films used to form devices, substrate resistance, and dielectric leakage limit the performance of passive devices. The impact of these parasitic impedances on the performance of passive devices will be captured in the Technology Requirements section.

A key challenge for any semiconductor technology, whether CMOS, BiCMOS, III-V or HVMOS is to implement passive devices required for the intended application at the lowest costs possible. With the exception of the MIM capacitor, on-chip passives components can be formed using of the readily available layers in the semiconductor for resistors and varactors and in the interconnect layers for inductors and inter-metal capacitors. If the properties of such devices are not adequate, it may be necessary to introduce added masks and processing to form high-performance passive devices.

There are challenges to providing low-cost and high-quality passive devices that are imposed directly by the scaling of interconnect dimensions. The decreasing overall stack as well as the individual metal heights results in increasing resistive losses and vertical parasitic capacitances. This limits the Quality-factors of the on-chip integrated inductors, transformers, MIM and inter-metal capacitors.

2.5. HIGH VOLTAGE MOS

The primary challenge for implementing HVMOS technology is choosing the lithographic node upon which to base the HVMOS technology. There are several aspects of high voltage devices and the associated base technology which make it difficult and unlikely that the HV roadmap for the future will follow the lithographic shrink seen for Digital CMOS and RF CMOS. The reasons can be summarized as follows:

1) As the lithographic node decreases, the resulting electric field within the device increases for a given V_{DS} and V_{GS}. For HV devices the drive is toward supporting higher-voltage HV device design. So, the HV device designs can not take advantage of the lithography capability to shrink the intrinsic HV device dimensions. The device interconnect dimensions will improve, but not the internal device dimensions.
2) HV device and chip designs are analog based where noise and mismatch are key concerns. The analog devices are usually large in order to improve the noise and mismatch in order to take advantage of any 'shrink', there would also be a requirement to improve these parameters. Given the complexities of achieving high-voltage operation, this is not likely or straightforward and, therefore, intrinsic HV device dimensions are considered constant.
3) Digital content of a HV chip is usually a small fraction of the chip area so that a relatively small portion of the chip would take advantage of smaller allowed lithography dimensions. The digital content would need to significantly increase in order for the cost savings associated with a smaller chip size to compensate for the increased processing cost at smaller lithography nodes.

So the conclusion is that there will be a modest rate of change to 130 nm and 90 nm but unlikely to project a migration into the smaller nodes. We therefore truncate the roadmap in 2021 to illustrate that we do not expect a migration of HVMOS technologies beyond the 90 nm lithography node.

3. TECHNOLOGY REQUIREMENTS

We first discuss in this Section on Technology Requirements those figures of merit (FOM) that are common to many RF and AMS technologies.

Extracting reliable FOMs from high-frequency measurements becomes more difficult as device performance levels increase while their resistances increase and capacitances must decrease. For these reasons a sufficient device area is recommended to measure capacitances exceeding 20 fF, which is a lower limit for reliable data. Measurement, de-embedding, and parameter extraction methodologies may have a significant impact on high frequency FOMs. Although some companies use complex procedures to obtain the accuracy required for compact modeling of silicon and SiGe devices, most companies use rather basic techniques to measure and monitor device cut-off frequencies. [9,10]

The most common method used both for silicon bipolar and field-effect transistors is a two-dummy (Open + Short) de-embedding technique following a standard [short-open-load-through (SOLT) or line-reflect-reflect-match (LRRM)] impedance substrate standard (ISS) calibration. Even though the layout of these de-embedding structures and the precise de-embedding methodology may vary from one company to the other, the de-embedded device generally must keep the metal lines required to connect its electrodes, i.e., Metal 1 or Metal 1 + Metal 2 levels. This usually yields very repeatable results for unity current gain *(h21)* cut-off frequency, f_T. For lower performance devices, like high-voltage and p-type devices, single-dummy (Open) de-embedding may be sufficient.

The calibration and de-embedding approach described in the previous paragraph is in general not used for mm-wave III-V devices. For III-V device measurements, a single TRL (thru-reflect-line) calibration using on-wafer calibration standards is preferred. One of the main benefits of this approach is that the pad and interconnect parasitics to the edge of the device under test (DUT) are de-embedded automatically in the calibration step. TRL with on wafer calibration standards has recently been used by several groups to measure and de-embed silicon devices above 100 GHz. [11,12] The unity power gain maximum frequency of oscillation, f_{MAX}, is extracted and reported from Mason's gain (U) at a given frequency. However, the accuracy of this approach is the subject of much debate as this FOM is highly dependent on the cleanliness of the 20 dB/dec roll-off of U as a function of frequency. A conventional approach to verify f_{MAX} is plotting f_{MAX} = freq × $\sqrt{U}$ across a range of frequencies. This allows a reasonable estimate of f_{MAX} if a constant value is obtained over a wide frequency range, while at the same time providing information on measurement error for f_{MAX}.

The accurate extraction of the minimum noise factor, F_{MIN}, (or minimum noise figure, NF_{MIN}, in dB) of a transistor is even more challenging than f_{MAX}. At frequencies below 50-GHz, and very rarely at W-band where commercial equipment is available, a source-pull technique is employed whereby the noise figure of the transistor is measured for several carefully selected source impedance states along with the S-parameters of the transistor. After de-embedding, the minimum noise figure and the IEEE noise parameters of the transistor are extrapolated using a least squares fitting algorithm. Above 50 GHz, the minimum noise figure of the transistor is usually estimated from the noise figure of a low-noise amplifier or receiver measured for 50-Ohm signal source impedance. Other approaches above 100 GHz include the integration of a source-pull setup on the die. In the case of bipolar transistors, it is possible to extract all IEEE noise parameters only from either S-parameter or Y-parameter measurements. [13] Unfortunately, this much simpler technique is not applicable to FETs. [14]

Another important FOM extracted from the measured and de-embedded S-parameters, and road-mapped at 24 GHz, 60 GHz, 94 GHz, 140 GHz and/or 220 GHz, is the maximum available power gain (MAG) of a common-emitter or common-source stage. At frequencies where the transistor is not unconditionally stable, MAG reduces to the maximum stable gain (MSG). More complex circuit figures of merit such as that of power amplifiers are linked to MAG.

3.1. CMOS

The technology requirements tables for CMOS have changed dramatically from those in the 2009 roadmap. We continue to use the HP and LSTP technologies from the *PIDS* chapter as the basis for millimeter-wave and microwave applications respectively. But, with the 2011 edition, we specifically reflect the three different technology options reflected in the PIDS chapter; Bulk CMOS, Fully-depleted SOI, and multi-gate allowing the user to more readily assess the differences in RF and analog performance resulting from these technology options. Furthermore, using device parameters from the PIDS chapter and film properties reflected in the *Front-end Process (FEP)* and *Integration* chapters, we attempt to reflect the performance limitations resulting from the parasitic impedances of the device structure.

These changes are evident in the roadmap for cutoff frequency (f_T) for the LSTP transistor where closer linkage to the device parameters in the PIDS tables resulted in a significant uplift in the tabulated values in the far term years. The

roadmap for maximum frequency of oscillation (f_{MAX}) for both technologies now better reflects the impact of device parameters and parasitic impedances. Its near term value has dropped but it increases over time in a similar fashion compared to the 2009 edition.

In order to reflect requirements for narrow-band and broadband applications discussed in the System Drivers chapter, we provide roadmaps for analog gain at low frequency and maximum stable gain (MSG) and minimum noise figure NF_{MIN} for example application frequencies of 24 GHz for the LSTP technology and 60 GHz for the HP technology. We also tabulate the analog gain for an analog-friendly transistor that is provided as an option by some foundries.

Table RFAMS1 CMOS Technology Requirements

3.2. SILICON BIPOLAR AND BICMOS

We discuss in this section those FOMs that are specific to bipolar transistors. The effective emitter width W_E is not a FoM but a key feature size of the transistors. The emitter width W_E and the collector current density at peak f_T (J_C), provided for the HS-NPN, determine the current flowing through the transistor, which must be considered to avoid any electromigration issues.

The four FoMs common to the two types of bipolar transistors are the peak value of the frequency of unity current gain, f_T, the maximum oscillation frequency, f_{MAX}, the emitter-to-collector breakdown voltage BV_{CEO} and the collector-base breakdown voltage BV_{CBO}.

Simplified formulas of f_T and f_{MAX} are given in equations RFAMS-EQ(3.2.1) and RFAMS-EQ(3.2.2) respectively, where τ_{EC} is the total delay between the emitter and the collector and $\tau_F = \tau_E + \tau_{EB} + \tau_B + \tau_{BC}$ is the sum of the transit times in the neutral and space charge regions. Charging times depend on the transconductance g_m, the emitter – base (C_{BE}) and base – collector (C_{BC}) capacitances and on the emitter (R_E) and collector (R_C) resistances. f_{MAX} depends on f_T, the base resistance R_B and C_{BC}.

RFAMS-EQ (3.2.1)
$$f_T \approx \frac{1}{2\pi \cdot \tau_{EC}} \approx \frac{1}{2\pi\left(\tau_F + \frac{(C_{BE} + C_{BC})}{g_m} + (R_E + R_C)C_{BC}\right)}$$

RFAMS-EQ (3.2.2)
$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B C_{BC}}} = \frac{1}{4\pi\sqrt{\tau_{EC}.\tau^*_{BC}}}$$

where $\tau^*_{BC} = R_B . C_{BC}$.

Low-frequency (1/*f*) noise and matching numbers have been removed from the table since circuits' requirements are expected to remain constant. Maximum values of 1 $(\mu V)^2$ - $(\mu m)^2$/Hz and 2 % - µm are targeted for 1/*f* noise and collector current matching ($\sigma(\Delta I_C/I_C)$), respectively. While meeting this 1/*f* noise target should not be a concern, a degradation of the matching with the reduction of the emitter width is expected. This degradation will likely depend on the choice of the transistor architecture, which is not presumed in the roadmap. Indeed, contrary to CMOS, the ITRS requirements for bipolar transistors could potentially be reached by different transistor architectures just like it is today for the BiCMOS technologies on the market

Parameters critical for some of the targeted applications are also given. Some of these parameters are frequency dependent, like the minimum noise figure, NF_{MIN}, the maximum available gain, MAG, all given for the HS-NPN. The minimum noise factor F_{min} of a bipolar transistor (NF_{min}=10log(F_{min})) can be expressed by the equation RFAMS-EQ(3.2.3) where β is the current gain, f the frequency, f_T the current gain transit frequency.[13] As explained previously NF_{min} can be measured with off-wafer or on-wafer source-pull methods but its determination based on Y parameters gives very good results and can therefore be trusted.

RFAMS-EQ (3.2.3)
$$F_{min} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T}\sqrt{2\,g_m(R_E + R_B)\left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{\beta f^2}}$$

Others, newly introduced, track more specifically the ability of the transistors to address key functions. These are the intrinsic slew rate (*SLi*) and the linearity efficiency cutoff frequency (f_{LE}) for the HS-NPN and HS-PNP respectively. The intrinsic slew rate, *SLi* (V/s), is defined (cf. RFAMS-EQ 3.2.4) as the ratio of the collector current and the output capacitance (sum of C_{BC} and C_{CS} the collector – substrate capacitance) and is an indicator of the ultimate switching speed of the transistor in high-speed DACs, large-swing 50-Ohm output drivers, and in laser- or optical-modulator drivers.

The delay τ of a chain of identical CML HBT inverters is related to the intrinsic slew rate by RFAMS-EQ (3.2.5).

RFAMS-EQ (3.2.4) $$SLi = \frac{I_C}{C_{BC} + C_{CS}}$$

RFAMS-EQ (3.2.5) $$\tau = \frac{\Delta V}{SL_i} + \frac{\Delta V}{V_T}\left[\frac{1}{\omega_T}\left(1 + \frac{R_b}{R_L}\right) + R_b C_\mu\right]$$

where $\Delta V = I_T \times R_L$ is the CML logic swing (typically 250-300 mVpp per side), I_T is the tail current, R_L is the load resistance of the CML inverter, R_b is the base resistance, and V_T is the thermal voltage.

SLi is given as an indication to circuit designers based on published data (for L_E between 2 to 5µm) but it may be different for two transistors featuring identical f_T and f_{MAX} since this FoM strongly depends on the integration choices (collector isolation and doping, device architecture, …)

The linearity efficiency cutoff frequency f_{LE} (Hz) benchmarks the tradeoff between linearity, power consumption, and bandwidth and is defined (cf. RFAMS-EQ (3.2.6) as the ratio between output third order intercept (*OIP3*) and quiescent power consumption (P_{DC}) multiplied by the bandwidth (*BW*). The decrease of *OIP3* divided by P_{DC} with increasing bandwidth is based on empirical data collected from datasheets of commercially available amplifier products. Qualitatively, this is consistent with decreasing available loop gain with increasing frequency (bandwidth).

RFAMS-EQ (3.2.6) $$f_{LE}[Hz] = \frac{BW \times OIP3}{P_{DC}}$$

Changes in the 2011Technology Requirements Tables for bipolar devices are as follows:

1. Dropped the general analog NPN parameters i.e. 1/*f* noise and current matching (cf. scope).
2. Completed an update of the HS-NPN roadmap to line up with the ongoing f_T/f_{MAX} trend and related W_E scaling, in line with application requirements:
    a. Small decrease in the pace of f_T and f_{MAX} improvements with a slowing down of W_E reduction.
    b. Updated all the other parameters accordingly.
    c. Added intrinsic slew rate (*SLi*).
    d. Updated coloring.
3. Completed a major update of the HS-PNP roadmap to cover the applications of the revised scope:
    a. Increased of the breakdown voltages and decreased f_T accordingly.
    b. Rewiewed the pace of the emitter width reduction.
    c. Updated all the other parameters accordingly.
    d. Added collector-base breakdown voltage (BV_{CBO}).
    e. Added linearity efficiency cut-off frequency (f_{LE}).
    f. Updated coloring

Table RFAMS2 RF and Analog Mixed-Signal Bipolar Technology Requirements

3.3. COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

The changes in the tables (compared to the power amplifier and millimeter wave tables of past chapters) are:

1. The focus of the tables is scaling of gate length for FETs and emitter width for HBTs and hence frequency response for each material system.
2. We have aligned low noise and power device gate lengths for each materials system with the exception of MHEMT
3. We added FOMs for 140 and 220 GHz low noise and power amplifiers
4. We shifted production dates for all scaled devices to the right.

III-V devices are produced at relatively low volumes when compared silicon devices. This is especially true for scaled III-V devices (gate length < 100 nm) where wafer volumes can be quite small due to limited or highly specialized applications. In this regard, the values in the ITRS tables represent device/fabrication processes that demonstrate the capability to produce components (devices/circuits) in a production representative environment that includes availability of production 'released' fabrication processes, a design kit with robust device models, and device reliability data.

In addition to f_T and f_{MAX}, the III-V tables show a projection of key parameters intrinsic to the device, such as breakdown voltage, maximum current, and transconductance, as well as performance factors for low noise and power transistors at fixed frequencies, namely, noise, power, gain, and efficiency. We present predicted performance data at five frequencies of interest across the 10 GHz to 300 GHz frequency spectrum: 24 GHz, 60 GHz, 94 GHz, 140 GHz and 220 GHz. For low noise devices we use F_{min} and Associated Gain, both in dB, as the figures of merits below 100 GHz. For frequencies above 100 GHz in the table (i.e., 140 GHz and 220 GHz), device F_{min} measurements are not readily available as it is difficult to provide the optimum impedance ("Gamma opt") in a source pull measurement as input impedances become low. The noise figure *(NF*), in dB, of a single stage low noise amplifier MMIC (with 50 ohm matching at the input of the MMIC) is used in the table as a substitute for device F_{min}. (FET gate periphery at these frequencies is 2 x 25 micrometers). We note that when the small signal gain of a technology is high at a given frequency, the noise figure of a single stage MMIC will be similar to the noise figure of a multi-stage MMIC. Both device F_{min} and single stage MMIC *NF* are provided at 94 GHz to provide the reader with the expected relationship between the two parameters. For power devices simultaneous Output Power, Gain, and Efficiency of a single stage power amplifier at each frequency are used as the FOM.

In comparison to Si CMOS, scaling of III-V devices, particularly for RF applications, presents a challenge. For example, in addition to improving transistor speed, gain (or frequency), the device engineer must simultaneously optimize the device for higher breakdown or operating voltages which are requisite for power and high dynamic range applications. In addition to geometry scaling, the device designer has an additional degrees of freedom in device optimization, epi engineering – tailoring of device layers to support high breakdown fields and high mobility/saturation velocity. The III-V devices in this chapter are all formed with epitaxial layers (and not ion implantation). This has numerous advantages as well as challenges. Advantages include quantum well structures to enhance channel transport properties, barriers layers for channel confinement and heavily doped cap layers to minimize sources and drain parasitics. Challenges include: no planar device structures and the use of recess technology to tailor electric fields in the vicinity of the gate electrode. In addition III-V FETs typically use T or mushroom shaped gates to reduce gate resistance.

Breakdown voltage is determined by a combination of material properties and gate recess geometry and, in general, material systems with better channel transport properties sacrifice breakdown voltage. For example InP HEMTs offer better high frequency performance (due to high In content InGaAs channels), where as GaAs pHEMTs offer better breakdown characteristics (lower In content). The GaN HEMT system offers superior breakdown characteristics with transport properties comparable to GaAs pHEMTs. For a given material system there is a tradeoff between high frequency and high voltage performance.

To first order the Johnson Figure of Merit (JFOM = v_{sat} * breakdown field) is independent of gate length for a given material system varying only slightly with gate length/device scaling. GaAs pHEMT, GaAs MHEMT, InP HEMT have similar values (related to the tradeoff of breakdown voltage and channel In content or saturation velocity) whereas GaN HEMTs JFOM is 10X higher due primarily to the larger breakdown field.

To first order f_T scales with channel composition and gate length, predominately due to the increase in transconductance. Gate-source capacitance, C_{GS}, the other parameter that directly impacts f_T, to first order, is invariant with gate length, primarily due to the fact that the reduction in capacitance due to shorter gate lengths is offset by the smaller gate-channel spacing required to eliminate short channel effects and the higher channel charge used to increase transconductance.

F_{max} exhibits a more complex behavior with scaling due to the additional R and C terms that provide multiple additional variables for device optimization. For example, the same gate recess that is used to tailor the electric field at the gate edge optimizes gate-drain capacitance, C_{GD}. Both C_{GD} and breakdown voltage increase with increasing drain side recess dimension. Thus f_{max} decreases with increasing breakdown voltage resulting in a compromise between high frequency performance and high voltage operation. While R_G is expected to increase with decreasing gate length, this increase is offset by the use of T-shaped gates, however, at the expense of increased C_{GD} due to the gate T-top overhang as well as the added fabrication process complexity. The same holds true for field plates, commonly used in GaN HEMTs to tailor the electric field on the drain side of the gate. Regardless, compared to Si based devices, III-V devices collectively provide superior high frequency performance due superior material properties.

Due to the multiple degrees of freedom in the optimization of III-V devices the FOM values for a given material system and gate length will vary from foundry to foundry. Therefore, the values in the tables are meant as trends and not as absolutes and where chosen to be consistent between different device types.

The 24 GHz spectrum is being positioned for wireless LAN applications. The 60 GHz frequencies, long used by the military for secure satellite cross links, falls in a region where atmospheric absorption is high, and as a consequence is ideal for short range, "last mile" connectivity in congested areas, where the short range facilitates frequency re-use. Within the scope of this roadmap, we expect to see applications opening at 94 GHz, 140 GHz and 220 GHz, such as point to point communication, concealed weapons detection and imaging all weather aircraft landing systems. The spectrum from 100 GHz to 1000 GHz holds promise for many applications in the areas of medical imaging, spectroscopy, and security. The III-V Technology Requirements Section summarizes the diverse technology choices for the frequencies, 24 GHz, 60 GHz, 94 GHz, 140 GHz and 220 GHz.

A review of the tables shows that no one material or device technology has the monopoly at any frequency. The user has many choices. We have made no attempt to select a preferred component for any particular application, because the choice can be driven by many factors, not the least of which is cost. Other factors are integration level, reliability heritage, operating voltage, and of course, performance, which is the focus of the roadmap. We have, however, made implicit predictions regarding the obsolescence and preferences for certain technologies. These predictions are implied by the "white space" (absence of parameters) in the out years for a particular technology. The general trends are summarized below:

- III-V power devices fall into two regions: low power (a few to tens of watts) provided by GaAs PHEMT and MHEMT and InP HEMT, and high power (tens to hundreds of watts) dominated by GaN.
- III-V MESFETs are not included in the tables. Although GaAs MESFETs may stil play a role in applications under 10 GHz, there is no development work in this technology nor do we see new designs forthcoming due to superior performance along with cost and reliability parity of GaAs PHEMT technologies.
- GaAs pHEMTs will slowly be retired from the table as the technology will not be scaled beyond 70nm and there are no known plans to use GaAs pHEMTs above 120 GHz. While GaAs pHEMTs are currently offered as foundry processes (L_G = 500, 250, 150, and 100 nm) and will continue to be used into the foreseeable future, GaAs PHEMTs will eventually be replaced by InP HEMTs for emerging high frequency applications and more importantly by GaN for power and high frequency applications due its superior power performance.
- Metamorphic technologies (MHEMT devices) offer greater flexibility for optimization of material structures. We expect to see an increase in indium mole fraction for low noise transistors to achieve improved gain and NF into mm-wave. However, because higher mole fractions compromise operating voltage and thus power capability, we expect a concomitant lowering of mole fraction as well as a lag in scaling of gate length for power devices
- Low noise MHEMT technology continues to evolve with trends towards shorter gate lengths for mm-wave applications, and we see this trend continuing to the 35 nm node in the latter half of this decade. Since MHEMTs are manufactured on GaAs substrates, the availability of commercial 6" GaAs semi insulating wafers can be expected to offer a cost advantage over 4" InP HEMT wafers for high volume applications in foundries that have invested in 6" processing infrastructure. Nevertheless, we expect to see continued competition performance with InP HEMTs as InP technology continues to advance towards higher In-mole fraction epitaxial layers, thus blurring the distinctions between GaAs MHEMTs and InP HEMTs.
- The use of pseudomorphic, composite InGaAs/InAs channels in InP HEMTs has been shown to offer electron mobility enhancement relative to an equivalent random alloy channel.[15] The table for InP HEMT shows increasing indium mole fraction in the channel as gate lengths scale to 70nm, 50nm, 35nm, and 25nm in future years. The listed indium mole fraction values should be viewed as equivalent alloy compositions for composite InGaAs/InAs channels.

- Power MHEMT technology is expected to scale to, at best, 50 nm. Since breakdown voltages are compromised at shorter gate lengths and higher In-mole fractions, the MHEMT advantage may give way to other competing technologies - GaN and/or InP HEMTs - by the end of the decade.
- The III-V device community has continued to focus significant effort on the performance and maturation of GaN HEMT devices, particularly for millimeter-wave transmitters. Device operating frequencies have increased significantly, with f_T and f_{MAX} from highly scaled devices reaching frequencies above 200 GHz and 400 GHz, respectively. The Johnson figure of merit for these devices (~f_T * breakdown voltage) is in the 5 THz-V range for existing millimeter-wave device technologies. Recent device research features have included regrown ohmic contacts enabling 0.1 ohm-mm source and drain contact resistances, enhancement and depletion mode operation on the same wafer, self-aligned gate processes, incorporation of InAlN barrier layers, and gate lengths below 50nm. W-band (94 GHz) GaN MMICs have been demonstrated by multiple organizations with power output levels roughly 5x greater than InP HEMT and GaAs pHEMT MMICs at in this frequency range.
- Microwave GaN, especially for base stations, is not included in the table. Microwave GaN is in production at multiple foundries. The main performance driver for GaN for microwave frequencies is cost, efficiency and linearity. For base stations linearity and efficiency is driven by circuit design. For 10GHz – 30 GHz applications, users will adopt 150 nm GaN technology to provide gain at the harmonics required for high efficiency switching mode operation. 150 nm GaN is predicted to be in production in 2012.
- GaN may also have a niche in the low noise area for applications requiring high robustness and linearity. GaN noise measure is comparable to GaAs PHEMT, and because limiters can be eliminated from the front end of receivers, GaN devices will offer distinct advantages in system noise figure. Low noise amplifiers in GaN HEMT technology have demonstrated wide bandwidth, high linearity, and competitive noise figure at frequencies ranging from 1 to 24 GHz. RF Receivers using GaN HEMT LNAs are under development for applications requiring high dynamic range or co-location with high power transmitters. Improved device operating frequencies have led to improved gain over wide bandwidths and reduced noise figure
- While InP HBTs offer superior high frequency performance, they will compete with SiGe HBTs for mixed signal applications. SiGe BiCMOS offers clear cost and integration level advantages, while for equivalent lithography, InP may offer up to 4X improvement in performance. Alternatively, InP HBTs offer 3-4X higher breakdown voltage for the same cut-off frequency and may be a good solution for analog and power circuits at the upper end of the mmWave frequencies and the emerging sub-mmWave frequencies.
- InGaP HBTs are not included in the table. Similar to GaN for base stations, development is focused on driving cost, increasing integration density and improving efficiency and linearity (which are circuit driven). There is no driving force to scale the emitter width.

Table RFAMS3 Compound Semiconductor FET and Bipolar Transistors

3.4. PASSIVE ON-CHIP DEVICES

With only minor changes, the Technology Requirements tables are the same as those published in 2009 but delayed 2 years. This reflects the fact that passive device requirements are evolving slowly and the limited participation of subject-area experts in this committee. Future work will attempt to more closely tie the performance of relevant passive devices to the Interconnect roadmap and to define application requirements that passive devices formed in any technology must meet.

Table RFAMS4 On-Chip Passives Technology Requirements

3.4.1 INDUCTOR

The inductor is one of the most critical elements in RF and microwave circuits for high-frequency wireless applications. If the Q-factor value is too low, the lumped circuit will not reach the desired performance targets. Spiral inductors providing a high Q-factor and inductance value are commonly used for wireless SoC. The important characteristics of an inductor are its inductance value and its parasitic capacitance and resistance that determine its Q-factor and self-resonant frequency. The inductance value is determined, in the first order approximation, by length and doesn't scale with conventional interconnect scaling. The series resistance of a SoC inductor that presents the dissipative loss is given by a sum of three components: 1) the DC resistance of the inductor, 2) the resistance due to skin effect in the conductive trace,

and 3) the resistance due to eddy current excitation and dielectric loss in the substrate. Achieving a predetermined inductance at a small resistance *R* contributes to an increase in the Q-factor. The DC resistance increases with the scaling of interconnects. Even though the better conductors allow somewhat lower DC resistance, the AC resistance becomes higher. Typically, SoC inductors make use of the thick metal layer(s) that are today conventionally provided for this purpose to circumvent the trend of local interconnects scaling in resistance critical applications and potentially aluminum thick layer.

When self-resonance occurs, the inductive reactance and the parasitic capacitive reactance become equal. For frequencies greater than the self-resonant frequency, the inductor becomes capacitive and loses its inductor property. The self-resonant frequency of an inductor is supposed to be much higher than its operating frequency. To increase the self-resonant frequency, the parasitic capacitance C in an inductor has to be suppressed. Parasitic capacitance of an inductor is determined by its area that gets smaller for higher frequencies and by the dielectric/semiconductor stack below inductor. The dielectric portion increases with the interconnect scaling, which is one more reason to provide an additional metal layer.

The maximum diameter of an inductor should be less than $\lambda/30$ in order to avoid distributed effects. Higher frequency applications require a smaller size and higher self-resonant frequency. As a result, the inductance density also becomes more and more important. Therefore, a major design goal for inductor components is to increase the Q-factor by minimizing series resistive losses, density of inductance and self-resonant frequency by minimizing parasitic parallel capacitance. All three of these are in contradiction with interconnect scaling. Such a situation is typically resolved by additional (dedicated) thick metal layer(s).

3.4.2 CAPACITOR

There are two types of linear capacitors generally used in SoC RF and microwave circuits: interdigitated and metal-insulator-metal (MIM). The choice between the interdigitated and MIM capacitors depends mainly on the capacitance. Usually interdigitated capacitors are only used to realize capacitance values less than 1 pF. For capacitance values greater than 1 pF, MIM structures are generally used to minimize the overall size and to avoid the distributed effects. For a capacitance values greater than 200 pF, off-chip capacitors are necessary.

Capacitor performance is strongly associated with the Q-factor and parasitic inductance of the capacitor. Resistive losses and the parasitic inductance are caused by the connection to the capacitor electrodes. To achieve a high Q-factor, it is essential to reduce the conducting loss in the wiring and electrodes and to use dielectric materials with small loss-tangents.

To increase high-frequency performance and the passive circuit density and reduce the cost, a large capacitance density is highly desirable. Silicon oxide and nitride are commonly used in conventional MIM capacitors. They can provide good voltage linearity and low-temperature coefficients. But, their capacitance density will be limited by their low dielectric permittivity. Attempts to increase the capacitance density by reducing the dielectric thickness usually cause an undesired high leakage current and poor loss-tangent. Therefore, high-k dielectric materials are used to provide good electrical performances and increase the circuit density.

3.4.3 VARACTOR

A varactor diode is a diode for which the capacitance varies as a function of the voltage applied between its terminals. It is employed to realize tuneable oscillators, filters, phase shifters, and the like.. The figures of merit that describe the performance of a varactor at high frequency are:

1) capacitance ratio C_{MAX}/C_{MIN},

2) Q-factor over the entire range of control voltages, and

3) linearity of the tuning characteristics: dC/dV..

It is always desirable to have a large Q-factor, a capacitance ratio that is typically greater than 2, and very linear tuning characteristics. The variable capacitance is usually obtained by modulating the depletion region width of a reverse-biased pn junction or of a MOS capacitor.

Three types of varactor structures are typically encountered in silicon integrated circuits:

1) pn junctions implemented in the BC region of an HBT or in the source/drain-substrate junction of a MOSFET,

2) accumulation mode n-well MOS (AMOS) varactors formed using an n-channel MOSFET placed in an n-well (rather than in a p-well) to reduce channel resistance and maximize the quality factor,especially at mm-wave frequencies,

3) hyperabrupt pn or Schottky varactors which require a special implant and exhibit the highest capacitance ratio but are only available in specialized processes.

During the last decade, due to the proliferation of nanoscale CMOS technologies, the AMOS varactor has become the most popular variable capacitance device. Typical varactor capacitance values range from a few fractions of a fF to tens of pF. The varactor Q-factor is inversely proportional to frequency, and is determined by the series loss resistance and the reactance of the variable capacitance.

3.4.4 RESISTOR

Integrated resistors can be produced either by using thin films of lossy metal on a dielectric substrate (such as intermetal dielectrics (IMD) in the interconnects) or by reusing the transistor gate such as poly or metal in the high-*k* integation schemes. Nichrome (typically is NiCr but may also contain iron Fe) and tantalum nitride (TaN) are the most popular film materials for thin-film resistors. SiCr and poly-silicon thin films are also used for thin-film resistors. TaN is preferred to NiCr for RF applications because the presence of undesirable magnetic material, i.e., nickel, in NiCr, may introduce unwanted intermodulation products in multi-carrier wireless systems. In addition, TaN is relatively readily available in Cu-based interconnects. NiCr and TaN are commonly used in III-Vs as well. A common problem with planar film resistors is the parasitic capacitance arising from the underlying dielectric region and the distributed inductance. These parasitics in these resistors have frequency dependences at high frequencies. Shortening the resistor length by introducing films with larger sheet resistivities is helpful for suppressing these parasitics. Desirable characteristics of resistors can be summarized as:

1) Resistance values that do not change with time,
2) Low temperature coefficient of resistance (*TCR*),
3) Large sheet resistivity (kΩ/square to MΩ/square) to minimize the parasitics and to guarantee that the resistor length is less than 0.1 λ so that distribution effects may be ignored, and
4) Adequate power dissipation capability

The required tolerances for passive components are roughly summarized in Figure RFAMS3. Analog and RF applications typically necessitate small tolerances of less than ±5% and high performance characteristics such as high Q-factors and high self-resonance frequency.

Application / Element / Values / Typical Required Tolerance
Damping Resistor /(10-33Ω)/ ±30%
Bypass /Capacitor/ (50 pF-1 μF)/ ±30%
Pull-up, Pull-down/ Resistor/ (500-1 MΩ)/ ±10%
Integral calculus circuit/ Capacitor /(100 pF-1 μF)/ ±15%
Differential circuit/ Capacitor (10 pF-10 μF)/ ±5%
Oscillation circuit/ Capacitor (10 pF-10 μF)/ ±5%
Bias circuit Resistor/(1 k-10 MΩ) /±1%
IC controlling Resistor/(>10 kΩ)/ ±1%
Filter Capacitor/ (< 1 μF) and Inductor(< 100 nH)/ both ±5%
Impedance matching/ Resistor(50-100 Ω)/, Capacitor/ (< 10 nF)/ and Inductor/ (< 100 nH)/ all ±5%

Figure RFAMS3 Required Tolerances depending on the Application

3.4.5 MM-WAVE PASSIVES

The scope of the mm-wave on-chip passives includes capacitors, resistors, inductors, varactors, antennas and antenna resonators. As in the RF range discussed previously, lumped inductors, transformers, MiM/MoM capacitors, pn junction and AMOS n-well varactors continue to play significant roles in minimizing the area occupied by LNAs, PAs, phase shifters, VCOs, and mixers in emerging silicon SoCs. Successful applications of all these components have been demonstrated in CMOS and SiGe BiCMOS circuits operating up to at least 170 GHz in both "RF" and "standard digital"

backends as well as III-V circuits. However, a concerted effort is needed from foundries to provide mm-wave friendly inductor/transformer and capacitor values in the 10 pH to 100 pH and 5 fF to 100 fF ranges, respectively. For transformers, close lateral and vertical spacings (fine pitch) between the top two metal layers are needed to achieve large coupling coefficients in the 0.8 to 0.9 range. A thick-metal, thick-dielectric "RF" back-end also benefits high-quality passives in the mm-wave regime. Because the skin depth decreases with increasing frequencies, one-micrometer thick metals are often sufficient for many applications at 60 GHz and above. In contrast, thick dielectrics are even more important at mm-wave than at RF frequencies in reducing parasitic capacitance and substrate losses. The much more common use of transmission lines as matching elements because of reduced wavelengths is special to mm-wave circuits. Transmission lines are typically implemented in silicon circuits as microstrip lines in the top metal, with the ground plane placed above the silicon substrate and formed in the first 2-5 lower-level metals, often shunted together to reduce loss. Grounded coplanar waveguides with the ground plane above the silicon substrate and coplanar waveguides directly over the silicon substrate have also been employed. Sometimes, especially in "standard" backends, "slow-wave" transmission lines, employing lower-level metal floating bars perpendicular to the signal flow have been employed to increase inductance per area and minimize loss and the area occupied by matching elements. Increasingly, at frequencies above 100 GHz and in thick-metal back-ends, it has become feasible to integrate antennas or antenna resonators with the overall antenna efficiencies now exceeding 50 %.[16-18]

3.5. HIGH VOLTAGE MOS

Below is the first HVMOS technology requirements table considered by the RF and AMS technology working group of the ITRS. As described above, it treats on-resistance for NMOS and PMOS transistors as well as the lithography node of the integrated digital CMOS as a function of the breakdown voltage. The breakdown voltage is the primary FOM that defines the application space for which a given HVMOS device is suited.

Table RFAMS5 High-voltage MOS Technologies

4. POTENTIAL SOLUTIONS

4.1. CMOS

We propose potential solutions for reducing gate resistance, reducing parasitic capacitances, improved high frequency models, and cite the need for reducing device series resistances and output conductance.

The gate resistance is a significant limiter of f_{MAX} and NF_{MIN}. Reducing the interfacial resistivity between the various films composing the gate will help reduce the overall gate resistance. Forming the gate from a single metal layer would eliminate interfaces. Structural solutions like strapping the gate with overlying metal or forming a T-gate structure employed in III-V technologies would provide significant reduction in gate resistance.

The parasitic capacitances associated with connecting a multi-fingered device to transmission lines formed in the upper layers of the wiring stack, are a significant limiter to f_{MAX} and MSG. Increasing the size of the device and thereby increasing the spacing between wires will decrease the wiring capacitance, but this must be optimized with the increased resistances and junction capacitance that would result.

It is a typical foundry practice to provide device models that reflect the device behavior of the transistor plus wiring up to the first or second metal level leaving the connections to higher metal levels to the designers' discretion. While this allows for flexibility in design it requires the designer to extract the parasitic impedance of the full wiring stack in order to get an accurate simulation of circuit performance. A model reflecting a complete wiring stack or a method for locally extracting parasitic impedances would improve the accuracy of circuit simulations early in the design phase.

Device series resistances and transistor output conductance also limit transistor performance. Innovation in the digital device structure would be necessary to reduce these.

4.2. SILICON BIPOLAR AND BICMOS

Potential solutions for continuing to improve the f_{MAX} of bipolar transistors (all types) include lithography advancements that help drive lateral device scaling to reduce parasitic device resistances and capacitances. This enables narrower emitter widths for reduced base resistance (R_B), as well as reduces the unit length current at peak f_T. The improved f_{MAX} and reduced unit length current at peak f_T can be traded-off for more aggressive vertical profiles (thinner base width and higher collector doping concentration) to drive f_T increases while remaining within reliability limits for current handling

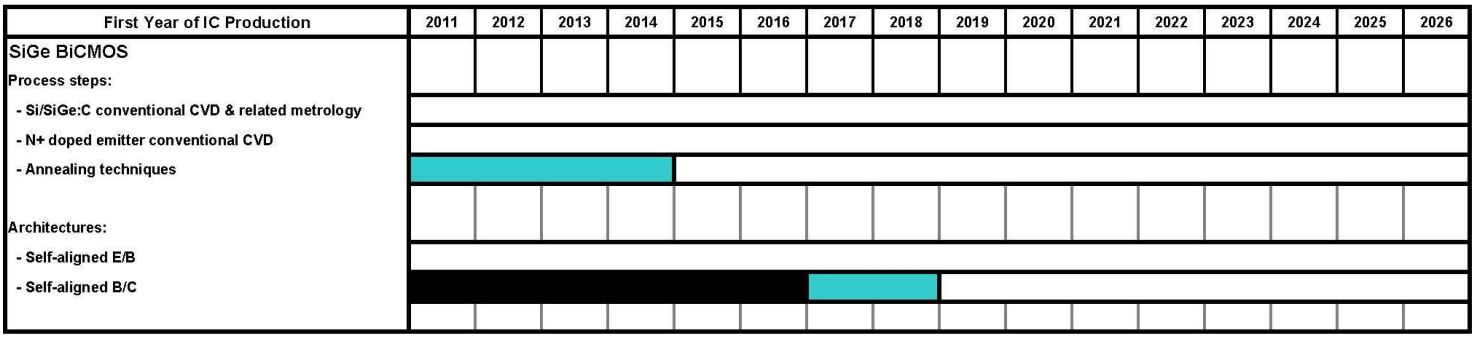
in the metal interconnects. The improved f_T and f_{MAX} will also improve the noise figure at high frequency to address mm-wave requirements.

Control of the vertical profile may limit this approach. The Chemical Vapor Deposition (CVD) technique does not appear as a showstopper since the control of the doping profile, including the collector, is today not limited by the control of the deposited thickness but by the dopants diffusion due to the subsequent thermal budget. Continuous improvements are therefore expected both in CVD concerning process uniformity and repeatability, and in metrology for the in-line control of the deposited layers (thicknesses and dopant concentrations). The associated challenges are bigger for selective epitaxial growth (SEG) than for non-selective epitaxial growth (NSEG). Potential solutions to better control the vertical profile include the reduction of the process thermal budget by leveraging advanced CMOS solutions, such as spike or flash anneals, laser annealing, and reduced thermal budget silicide modules.

Parasitic losses can significantly limit performance gains. Scaling of the intrinsic collector doping and extrinsic base doping profiles to drive f_T and R_B (f_{MAX}) improvements leads to continued pressure on the R_B–C_{BC} trade-off. Research and development of more advanced structures that transition from emitter-base self-alignment to emitter-base and base-collector self-alignment has led to the reporting of several innovative architectures. These structures further minimize the interaction between the extrinsic and intrinsic regions of devices, helping to reduce the B-C junction area. It is expected that continued development and improvement of these (and potentially other) architectures will enable scaling of f_{MAX} in accordance with the roadmap.

Concerning the issue of the emitter resistance increase with the reduction of the emitter width (W_E), no breakthrough is foreseen today. Continuous improvements to reduce the specific emitter resistance are required both on emitter deposition process and on transistor architecture. BiCMOS technologies will also benefit from improvements in CMOS technologies such as the expected reduction in silicide and contact resistances.

W_E reduction is also driven by the requirements to reduce power consumption and to maintain a constant $W_E \times J_C$ (J_C being the collector current density at peak f_T) in order to be compliant with the electromigration capability of the metallization (including contact). Although BiCMOS technologies will have to deal with the improvements foreseen in CMOS technologies to this respect, special care to the wiring of the transistors will be required. To some extent metallization design rules, coming from core CMOS, could be adapted to the bipolar transistors.



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement

Figure RFAMS4 SiGe BiCMOS Potential Solutions

4.3. COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

In the past, compound semiconductors have taken advantage of the advances in lithography and processing equipment that are available in the silicon industry. In order to continue to accomplish this, wafer diameters need to be within one or two generations of the silicon industry. However, the lower volumes/demand for III-V devices does not always justify the investment required to scale III-V substrates. Today, 150 mm diameter, semi-insulating GaAs substrates are in production (although many III-V foundries still operate at 100 mm). InP substrates are available at 100 mm with no known plans to scale to larger diameters. Silicon carbide semi-insulating substrates, the basis for GaN HEMTs for RF applications, are also at 100 mm with plans to scale to 150 mm, pending demand. Therefore III-V technology appears to be 2 – 3 generations behind Si that is pushing towards 450 mm diameter substrates for future nodes. Thus, the gap between III-V and Si fab infrastructures may actually be widening.

A potential solution may lie in fabricating III-V devices on silicon substrates and ultimately fabricating III-V devices in silicon foundries. For example, recent advances in the epitaxial growth of GaN on silicon has shown that the growth of device quality GaN HEMTs epitaxy on 200 mm diameter substrates is feasible,[19] opening up the possibility of fabricating GaN HEMTs in an existing 200 mm Si foundry for a more cost effective solution. It should be noted that the GaN on Si development is being driven by the power conversion/conditioning industry (i.e., switching transistors) whose circuits operate at 10's of MHz rather than the 10's of GHz of the RF industry and, as a result, substrate resistivity/loss is less important. Nonetheless, with continued advancements in epitaxial growth technology, GaN on Si will make inroads into the RF market and provide a significant cost advantage.

The fact that the silicon industry is exploring InGaAs channels for use in CMOS beyond the 8 nm node, also creates the opportunity for fabricating other III-V devices on large diameter Si substrates in a silicon fab. However, significant development is required to create Si fab compatible III-V process modules.

Uniformity, reproducibility, and yield for compound semiconductors still lag behind Si-based technologies. This is not surprising, given the much higher investment in infrastructure and research for silicon, as well as the extremely large disparity in production volume between the two. For example, III-V fabrication tend to still use 'evaporation and liftoff' and electroplating techniques (particularly for backend interconnects) which are inherently 'dirtier', and hence lower yield, fabrication processes when compared to the deposition/subtractive patterning/CMP processes perfected for Si. Again, transitioning III-V device fabrication into a silicon foundry to take advantage of the Si infrastructure and high yield processing techniques provides a potential solution to the uniformity, reproducibility, and yield challenge. Nevertheless, as production volume in a particular compound technology rises, unit costs are found to decrease on a learning curve not unlike that of silicon.

Another potential solution for the substrate scaling challenge, as well as the integration density challenge, is the heterogeneous integration of III-V devices with Si CMOS on a silicon substrate. This integration approach is analogous to the SiGe BiCMOS process in which the SiGe HBT is replaced by a III-V transistor. This integration approach marries high-density digital circuitry with high performance III-V transistors to create 'mostly digital' RF and mixed signal circuits whose performance cannot be achieved with either Si or III-V technology alone. Recent advances under DARPA's COSMOS program (integration of InP HBTs with Si CMOS) have demonstrated the feasibility of this integration approach.[20] Even more recently, GaN HEMTs have been successfully integrated on a silicon substrate with Si CMOS. Again, to realize the true cost and performance advantage of the heterogeneous integration approach, the entire fabrication processes needs to reside in a silicon foundry. Significant development is required to create Si fab compatible III-V process modules.

While significant advances are being made in optical lithography tools, the cost of these tools along with the cost of masks to define sub 0.25 μm features is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beam is a solution to the mask cost, but wafer through-put, which is measured in hours per III-V wafer as compared to silicon wafers per hour, needs to be increased with high current electron sources and fast alignment systems. Since the III-V market for process tools is small, tool vendors have no incentive to develop tools for III-V foundries. Fortunately, high throughput, high resolution e-beam lithography tools are under development for the silicon industry.

While silicon carbide substrates are the defacto standard for GaN RF (power) devices due to their high resistivity and thermal conductivity, substrate (and epi) quality still has room for improvement. The use of GaN substrates provides a path to the growth of higher quality GaN HEMT epitaxy though homoepitaxy, however, while research on GaN substrates is continuing, GaN substrate maturity lags significantly behind SiC substrates in both quality and diameter, not to mention GaN substrates exhibit poorer thermal conductivity compared to SiC. Improved power densities in III-V devices made possible by advanced materials and device structures place an increased burden on thermal management. For example, while SiC substrates have significantly higher thermal conductance values compared to GaAs, InP and Si, the 5× to 10× higher power densities typically present in GaN transistors somewhat offsets the advantage in higher thermal conductance. Typical solutions to date have relied on substrate thinning to remove heat from the backside of the device and into a passive or active heat spreader in the ground plane. While this approach has been effective for GaAs and InP microwave devices, the trend toward high power density GaN technologies as well as power applications into the mm-wave spectrum pose additional issues related to the high thermal resistance of ternary and quaternary epitaxial layers in bandgap engineered devices as well as the much smaller size of mm-wave devices. As substrates are thinned, the contribution of the high thermal resistance epitaxial layers and the die attach medium increases disproportionally, particularly for small gate geometries, due to the thermal spreading resistance factor. While thermal management will include substrate thinning, the substrate thickness will also be dictated by RF considerations, particularly for microstrip transmission lines.

In addition to substrate thinning, solutions to device thermal management may include such techniques as thermal vias, topside heat removal structures, and site specific cooling. Thermal vias, in which a high thermal conductivity plug of material in placed beneath the power dissipation site in a transistor, have been explored using gold as a plug. However, mechanical stress due to thermal mismatch is a problem. Engineered nano materials, in which high conductivity materials which match the substrate thermal coefficient of expansion (CTE), are a possible solution. Topside gold shunts have also been demonstrated, but can interfere with the electric field distribution in the circuits. More recently GaN HEMTs on diamond substrates is beginning to emerge as a potential solution to the thermal challenge. Several companies are developing techniques to transfer device quality GaN HEMT epitaxy onto relatively low cost polycrystalline diamond substrates thus providing a very low thermal resistance path to the heat sink. Significant development is required to mature this approach and scale it to usable substrate diameters. A new Defense Advanced Research Projects Agency (DARPA) program to address site specific cooling will be underway by 2012. This program, "Near Junction Thermal Transport (NJTT)," is one of a portfolio of programs addressing high conductivity heat spreaders, micro-air cooling and high conductivity die attach materials. Solutions to thermal management will include all components in the thermal path from the junction outward. Other forms of carbon, such as graphene thermal spreaders and graphitic thermal interface materials,may also provide viable thermal solutions.

In contrast to Si CMOS which uses planar, self aligned gates and implanted or epitaxially regrown contact layers to engineer the device, gate recessing is typically used to engineer GaAs and InP based FETs to achieve high frequency performance and higher breakdown voltages. The recess process utilizes epitaxially grown etch stop layers and high etch selectivity to create high yield processes. This approach is also being used to scale GaN HEMTs to millimeter wave frequencies, although significant development is still required to achieve high yield selective recess process. Other approaches for engineering of III-V FETS is the use of field plates to tailor the electric field on the drain side of the gate to achieve high breakdown voltages, although the use of filed plates compromise high frequency performance. Due to the high fields present in III-V power devices, continued improvement of passivation and hot carrier effects is also needed. The creation of high density, nano-composite/laminate dielectric layers by ALD (dielectric engineering) is a potential solution that leverages recent developments in Si technology.

It is highly desirable in mixed signal electronics to have transistors capable of accommodating voltage swings of 10 V or more. As transistor speed is scaled for many mixed-signal or analog applications, it comes at the cost of low breakdown voltage values that greatly restrict the dynamic range of the circuits and represent a severe limitation. In this regard, InP HBTs that exhibit higher breakdown voltage for a give emitter geometry or transistor speed offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe is orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs. Gallium nitride HEMTs offer even higher promise due to the potential for a 10x increase in the Johnson figure of merit.

The performance of other RF circuit elements, such as mixers, can be also directly related to the dynamic range of the device. Therefore, it is necessary to scale the dimensions of a transistor to achieve the desired frequency performance while maintaining desirable breakdown voltage to allow large voltage swing for high dynamic range.

Currently, the GaN technology is primarily driven by microwave frequency power amplifier applications due to its ultra high breakdown field. The cut-off frequencies of GaN field effect transistors are about 100 GHz and existing monolithic microwave integrated circuits (MMICs) only consist of no more than ten transistors with air-bridge interconnect system. Both the transistor performance and integration level of circuits are too low to enable high-performance mixed signal circuits. To fully exploit the potential of GaN devices for desired wide dynamic range circuits, a next-generation nitride electronic technology is being developed to achieve high transistor speed (~ 500 GHz) and high integration level (> 1000 transistors) by scaling the transistors, reducing parasitic resistances and capacitances, and utilizing multi-level interconnects as has been done in silicon technology. In addition, the development of a stable enhancement mode (E-mode) operation is critical. This will offer many important practical advantages in circuit applications, including greater simplicity in mixed-signal and RF circuits and the ability to implement enhancement/depletion (E/D) logic capability (direct-coupled FET logic). Further, large scale integration of hundreds to thousands of transistors demands a manufacturing technology that can achieve high yield.

Uniformity of transistors is particularly important for mixed-signal electronics and further underscores the need to develop a robust, manufacturable device process. The impact of the future GaN technology will be profound and will, lead to dramatic improvements in the performance of RF and mixed-signal electronic circuits, which include high-speed high power amplifiers, ultra-linear mixers, and high-output-power digital-to-analog converters.

High-frequency performance in III-Vs, and now even in CMOS, is driven as much by epitaxy, bandgap and strain engineering (vertical scaling), as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by properly engineering the epitaxial layer stack, the source and drain regions, the substrate orientation, and/or the dielectric stack above the device. We expect continued improvements by bandgap and strain engineering in all of the III-Vs.

Simultaneously achieving high power added efficiency, high linearity, and high output power is a significant challenge for III-V power amplifiers used in RF and mm-wave transmitters. In most narrowband applications, a switched-mode amplifier (Class D, E, or F) is a potential solution to meet these simultaneous requirements. For example, a Class-F architecture uses a pinched-off transistor (high negative V_{GS}) and allows the input power to turn the device on and off, generating an RF square-wave voltage waveform that is out of phase with the half sinusoidal current waveform. This design approach minimizes power dissipation (I-V product) during amplifier operation. For Class F amplifier operation to be highly efficient, all harmonics generated due to the non-linear voltage waveform have to be suppressed using even and odd harmonic resonant matching networks. This type of amplifier can theoretically achieve > 95% PAE for an ideal narrowband case. Transistor device requirements for this level of efficiency are extremely low on-resistance and low drain-source capacitance. These device requirements are commensurate with devices with unity gain cutoff frequencies (f_T) 10x greater than the desired amplifier operating frequency. Therefore, devices with f_T in the submillimeter wave range (> 300 GHz) are needed for efficient, Class F amplifier operation of mmW amplifiers (30-100 GHz).

Circuit design solutions have shown utility for improving the combination of efficiency and linearity from an amplifier. The Doherty amplifier enables improved efficiency relative to conventional architectures. Doherty amplifiers are typically used in applications requiring high linearity, such as communications rather than those requiring wide bandwidth, such as electronic warfare. The Doherty amplifier power-combines two amplifiers that are biased differently – one is at Class AB while the other is at Class C that only conducts at half of the cycle. The benefit of the Doherty amplifier is improved power-added efficiency, at power levels well below saturation. Adaptive digital pre-distortion (DPD) designs, where the input signal is pre-distorted in the digital domain to compensate for device non-linearities, have also been used to improve linearity.

For receiver applications requiring wide bandwidth, in addition to high linearity and power added efficiency, recent circuit design innovations in feedback linearization, similar to classical operational amplifier techniques, offer potential solutions. In these approaches, excess gain-bandwidth product (such as that available in InP HBT amplifiers operating at 2 GHz) is traded for linearity without increasing DC power dissipation. Wideband microwave operation amplifiers have recently demonstrated a 5x improvement in the ratio of output third-order intercept point (*OIP3*) to DC power.

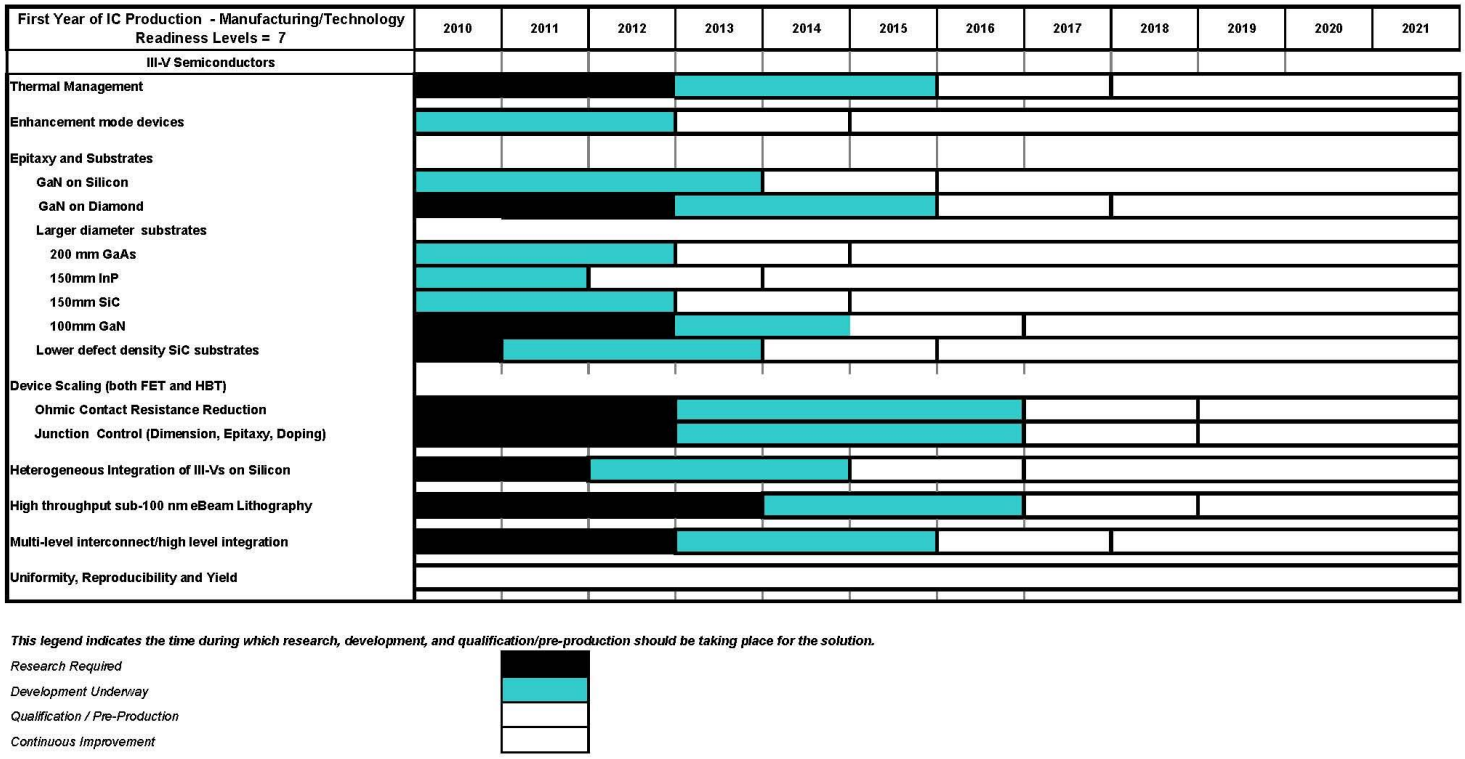


Figure RFAMS5 III-V Potential Solutions

4.4. PASSIVE ON-CHIP DEVICES

Passive devices are challenged by cost-performance trade-offs. A low-cost device implemented on-chip with adequate performance is the preferred solution. The advent of small-pitch through-silicon vias enabling stacking of different technologies will be used to integrate high-performance transistors with high-performance passive devices on different substrates with low-loss connections at device-level geometries. This ultimately pushes passive devices off-chip.

4.5. HIGH VOLTAGE MOS

Because of the nascent level of this section of our chapter, potential solutions are not being presented this year.

5. CROSS-CUT ISSUES

5.1. ESH, METROLOGY, YIELD ENHANCEMENT, MODELING AND SIMULATION

In coming years the RF and AMS TWG needs to expand its interaction with both the Metrology and the Modeling and Simulation TWGs. The measurement of device parameters and FOMs at frequencies in the mm-wave bands is becoming necessary both in understanding the physical mechanisms limiting device performance and in being able to accurately simulate this performance. Commercial equipment capable of performing these measurements has recently become available for frequencies up to 750 GHz. But, such equipment has not been in use long enough to establish standardized methodologies for de-embedding devices parameters from the parasitics. There is a need for building a consensus and establishing standardized methodologies. Even below 50 GHz a consensus is at best limited and a standard methodology does not exist. Production measurements above 50 GHz are practically non-existent.

Some of the most important measurement and standards needs include:

1) Improve dynamic ranges in small-signal measurements, equipment, and methodology.
2) Better measurements and instrumentation in the mm-wave range for noise performance characterization. Noise sources above 200 GHz are not currently readily available.
2) Pushing large-signal network analysis up to millimeter-wave frequencies. This would let designers see the voltages and currents inside their nonlinear devices as they operate, and develop large-signal models that they can use to optimize efficiency and linearity at the same time.
3) Better signal measurement tools to allow modulation formats to be standardized.

5.2. OTHER CROSS-TWG DISCUSSIONS

This year we have expanded our interactions with the Assembly and Packaging TWG as we defined better the treatment of passive device and helped inaugurate the MEMS TWG. We also had very fruitful interaction with the System Drivers TWG in re-writing the Mixed Signal Driver section of that chapter. This allowed us, for the first time, to make some comments on the suitability of a given technology for a given application.

5.3. IMPACT OF FUTURE EMERGING RESEARCH DEVICES AND MATERIALS

The Emerging Research Devices and Emerging Research Materials Groups use the concept of the future RF transceiver as the context in which to consider selected new devices and materials for RF applications that are within the ITRS domain called "More than Moore" (MtM). At the 2011 ITRS Summer meetings, they presented the following three emerging technologies as future candidates for RF transceiver functions of transistors, mixers, local oscillators, and resonators:

1) Sub-100 nm graphene RF FET transistors fabricated using nanowire gates have the possibility of THz cut-off frequencies. The high Fermi velocity of the carriers in grapheme results in a high drift velocity of about 4×10^7 cm/s in the channel. For example, a 70 nm channel length graphene RF FET is likely to have a cut-off frequency f_T of about 1 THz. Such transistors have possible applications as low noise amplifiers and mixers.
2) Nanometer-sized spin-torque oscillators (STOs) are likely to have low phase noise and be tuned from 0.1 GHz to more than 40 GHz by external magnetic fields, spin-torque currents, and magnetic materials and structures.
3) Resonators made from NEMS devices (nano-resonators) will be used for RF filters that are expected to have high Q values and be ultimately be tunable. Materials of interest for this application include silicon nanowires, III-V-compound semiconductor nanowire, carbon nanotubes, and graphene.

5.4. ANALOG CHALLENGES/TOPICS

This year, the ITRS took up a challenge from the Semiconductor Industry Association (SIA) to increase its treatment of analog technologies. In response, we expanded the scope of the application drivers considered when defining technology requirement. These applications span the range of frequencies from 0 to 300 GHz and are described in Figure RFAMS1. The chapter was re-organized by technology and each section addresses those applications generally produced in that given technology. We consider 5 circuit types as reflected in the Mixed Signal Drivers section of the *System Drivers* chapter. In addition, we consider general analog circuits such as voltage regulators, operation amplifiers and current sources. New members with subject-area expertise drove the expansion into these new areas. Conversely, the extent of our treatment of the available analog technologies was limited by the participation of subject area expert. Readers wishing to see the treatment of additional analog technologies are encourage to volunteer their efforts.

5.5. RF MEMS STRUCTURES

The new MEMS ITRS Chapter includes section on difficult challenges and technology requirements for RF MEMS resonators, capacitive switches, and varactors and a more complete discussion of cross-cut issues with RF and AMS technologies for communications. RF MEMS metal contact switches are not included.

RF MEMS devices not only include thin-film bulk-acoustic wave resonators (FBAR), surface acoustic wave resonators (SAW), capacitive switches, and metal contact switches, but also other MEMS devices types such as sensors (e.g., accelerometers and gyroscopes), microphones, and displays that add functionality to RF products. These MEMS accelerometers, gyroscopes, microphones, and displays devices are discussed in the 2010 iNEMI MEMS Chapter and except for display, are not discussed in this MEMS ITRS Chapter. For these reasons, they are not discussed in the RF and AMS Chapter. In general, the above four device types have found or will find use in wireless communication products as discrete devices, e.g., a FBAR filter mounted to a board or mother chip, or a Si MEMS oscillator replacing a quartz part in

an existing socket. The time at which the RF MEMS devices are produced in high-volumes often occurs when the MEMS function is integrated with the CMOS, BiCMOS, or bipolar semiconductor die. The timing for this integration will be primarily driven by cost. Until that time, initial introductions will occur in the following order: 1) favor discrete die (e.g. FBAR devices), 2) above or below IC implementations (e.g. variable capacitors), and 3) monolithic integrations with semiconductor die, which will potentially reduce the bill of materials by removing customized MEMS packaging from some devices and enable new applications due to integration and cost reduction.

6. OTHER CONSIDERATIONS

6.1. INTERNATIONAL STANDARDS AND ASSOCIATED MEASUREMENTS

The global competition to manufacture high-volume innovative RF and AMS products with enhanced functions and performance, such as those enabled by nano-electrotechnologies, e.g., MEMS/NEMS, is intense because nations want to strengthen their economies and create new jobs for their citizens and companies want to grow market share and profits by being the first to introduce higher value devices using the newest technologies. International standards and their associated metrologies are significant enablers for success at all stages of RF and AMS innovation - from research, development, initial deployment, high-volume commercialization, end of initial useful life, to recycling and disposal. Standards can be the catalysts for more efficient innovation and successful commercialization of technologies, provided they incorporate the best available engineering and science in which contributors to ITRS roadmapping activities excel. Standards can insure interoperability and reduce the number of times different designs are implemented, thereby freeing engineering resources to innovate where it will be a true differentiator. Equally important, standards greatly affect business models and outcomes. Those who contribute to ITRS roadmapping also excel in the skills essential for contributing to international standards and supporting measurements. By so doing, they increase the likelihood that international standards and supporting measurements will be better aligned with future ITRS goals and roadmaps.

Collaborations that involve many diverse organizations such as semiconductor companies, trade associations, R and D laboratories, national measurement institutes, and international standards and technology roadmapping bodies are required to ensure that the essential standards, associated measurements infrastructure, and scientific/engineering-knowledge base are all adequate to overcome technology barriers, especially barriers associated with nano-electrotechnologies identified in the ITRS. Such collaborations enable the successful development and subsequent manufacture of next generation materials (ERM) and devices (ERD) and appropriate packaging and assembly. For example, the Technical Committee 113 on nano-electrotechnologies, a technical committee of the International Electrotechnical Commission, has as one of its major goals that IEC's standards for nano-electrotechnnologies occur through collaborations with other organizations whenever such collaboration is in the best interests of the international standards community. The complete title for TC 113 is *Nanotechnology standardization for electrical and electronic products and systems* . TC 113 is developing an international roadmap on standards for nano-electrotechnologies that includes nanoelectronics. More information about IEC TC 113 is available at http://www.iec.ch > Quick links > List of Technical Committees > TC 113.

"Standards enable innovative products and new markets."
– Patrick Gallagher, NIST Director, November 2009

7. CONCLUSIONS

We list here some trends common to many of the RF and AMS technologies. These trends offer a framework in which to develop future editions of the RF and AMS Chapter and its updates.

Mesh-networks using mobile millimeter-wave communications are very promising solutions for addressing the spectrum crunch. Because of this, there is a lot of exploratory work on mobile devices at millimeter wavelengths. We expect to include more of the technologies that support mesh-networks in future editions of this RF and AMS Chapter. This potential application is considered by many to be the holy grail of RFICs, especially silicon RFICs that would bring down cost and bring commercial applications closer. Even though we are still a long way from this goal, there are several innovations that will assist in attaining this goal such as the following:

1) Stacked devices to improve output power, more efficient amplifier configurations than the traditional, combining InP or GaN with silicon to get the best of both worlds.

2) Using silicon digital processing power to linearizing inherently nonlinear but efficient transmitters.
3) MIMO to get the connectivity in channels that are characterized by high multipath and fading, and to make the most of the silicon processing power and small antenna size.

7.1. CMOS

The CMOS roadmap this year attempts to more accurately reflect the RF and Analog performance of the transistors of the high-performance and low standby-power technologies presented in the PIDS chapter. Where PIDS presents three CMOS transistor architecture options, overlapping in time, we reflect the same options.

It is instructive to consider two of the circuit level FOMs, presented in the *System Drivers* chapter, the values of which we can estimate using transistor-level FOMs. First, the upper-limit of LNA FOM allows us to compare the performance potential of CMOS, SiGe HS-NPN and the InP HEMT. Figure RFAMS6 shows that CMOS is roughly equally suited for implementing a 60 GHz LNA when compared to the SiGe and III-V transistors.

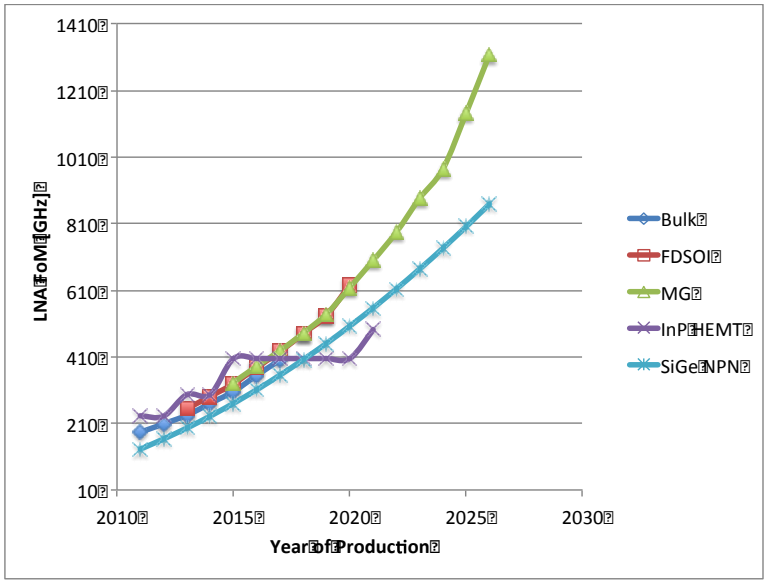


Figure RFAMS6 LNA Performance comparing CMOS, SiGe and InP Transistor Roadmaps

The result is different if we consider power amplifiers. The FOM for power amplifiers can be estimated from device FOMs as described in the System Drivers Chapter. The technology comparison in Figure RFAMS7 now shows a clear advantage of InP and especially GaN HEMTs over CMOS. Furthermore, SiGe NPNs are shown to perform equally well to GaN HEMTs. One must note that these FOMs do not provide the whole picture. For example, they ignore the fact that the load resistance needed to achieve the assumed output power will be extremely low for Si devices and essentially illustrate an unrealistic design point.

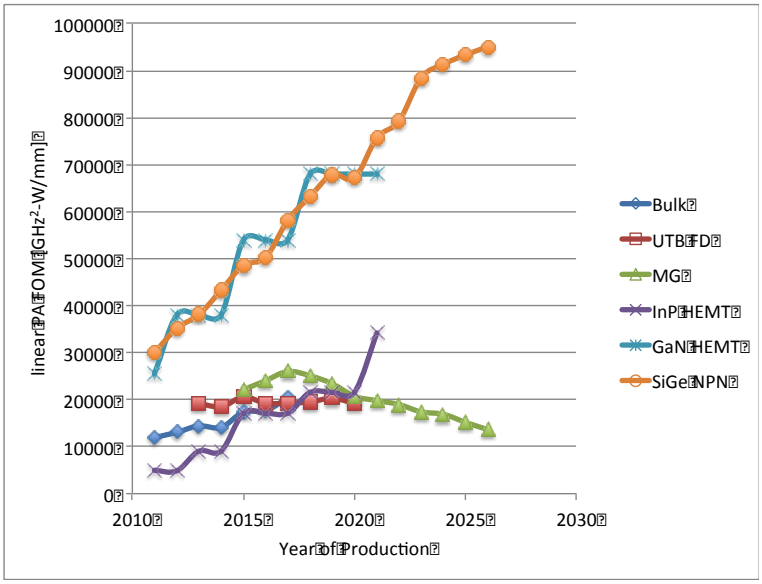


Figure RFAMS7 PA Performance comparing CMOS, with InP and GaN HEMT Transistor Roadmaps

CMOS technology performance for the PA application is projected to roll-off dramatically with technology scaling. This highlights the fact that while bandwidth may be high, the transistor gain is limited by its low-frequency value. The suitability of CMOS relative to other device technologies to implement a given application will depend on performance but also on other factors including cost and integration level.

7.2. BIPOLAR AND BICMOS DEVICES

Technical challenges facing the Si bipolar and BiCMOS roadmap are multiple and differ between the NPN portion of the roadmap that focuses of the development of new architectures and integration with advanced CMOS nodes and the PNP portion of the roadmap that focuses on control of the vertical profile of PNP transistors and their co-integration with NPN transistors. These challenges may impact the evolution of their respective performances such as the trade-offs among f_T, f_{MAX} and the breakdown voltages. But these challenges are probably not the main show-stoppers today. Indeed, the pace of the roadmap is driven by the market, as it should be. In this respect, the development of high-speed NPN BiCMOS technologies, for example, is tied to emerging millimeter-wave markets. Volumes related to these markets are difficult to estimate today, first because they deal with new applications, the development of which depends on marketing success, and second because some and possibly many of these markets may also be covered by CMOS technologies. But markets with sufficient volumes must justify the development of new technologies.

7.3. COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

Because of their superior transport properties and higher breakdown fields, devices based on III-V compound semiconductors will continue to serve niche markets, in applications 1) that are driven more by performance and less by cost and 2) where silicon technology can not meet the performance requirements such as high dynamic range or low noise figure. Examples include InGaP HBTs for cell phone PAs, GaN HEMTs for base stations PAs, and InP HEMTs and HBTs for millimeter wave and submillimeter wave transceivers. Compound semiconductors will continue to advance through a combination of gate length scaling and more importantly epi or bandgap engineering and over time III-V devices will merge with Si technologies (through heterogeneous integration) resulting SoCs with the 'best junction for the function'.

7.4. PASSIVE ON-CHIP DEVICES

This year we address the challenges and requirements of on-chip passive devices only. The Assembly and Packaging chapter treats off-chip and embedded passive devices. We address lumped devices; capacitors, resistors, inductors, and varactors, primarily for applications operating at frequencies less than 30GHz. We also begin to treat distributed passive devices, based on transmission lines, primarily for applications operating at frequencies above 30 GHz.

7.5. HIGH-VOLTAGE MOS.

This technology is being treated by the ITRS for the first time this year as we expand our treatment of analog technologies. The full breadth of hvmos technologies in production today is not captured by our roadmap. The scope of our treatment was limited by the number of contributing members with knowledge in this field. Interested readers are encouraged to volunteer time to expand and improve the roadmap.

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