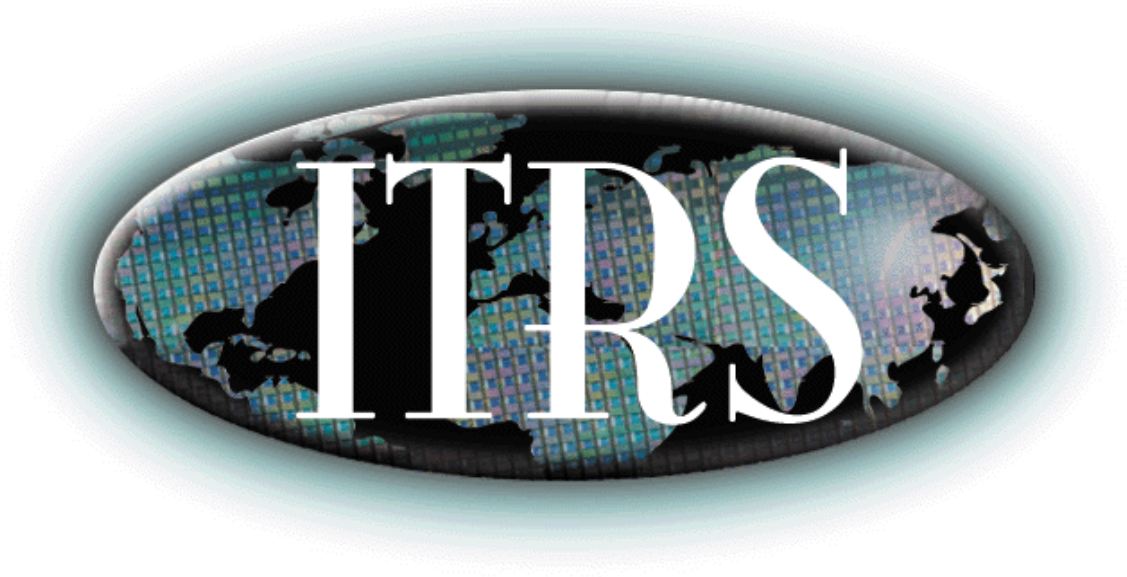

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

EMERGING RESEARCH MATERIALS

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EMERGING RESEARCH MATERIALS

1. SCOPE

This chapter provides the material research community with guidance on specific research challenges that must be addressed in a laboratory setting for an emerging family of candidate materials to warrant consideration as a viable ITRS solution. Each international technology working group (ITWG) has identified applications that need new materials with significantly improved properties to meet future technology requirements, enable increased density of devices, and increase energy efficiency for computing and reliability. Based on these requirements, the ERM has identified emerging materials that have properties that could potentially meet their needs for improved density, energy efficiency, and reliability. This chapter includes materials to support future memory and logic devices, lithography, front end processing, interconnects and assembly and package. For these emerging materials, this chapter presents requirements for materials, processes, interfaces, and supporting metrology, modeling, and simulation. Furthermore, it also identifies potential environmental safety and health issues that should be evaluated on ERM as they are being evaluated in research. In the 2013 ERM, we include critical assessments of alternate channel materials for CMOS extension and directed self-assembly for lithography extension.

The scope of Emerging Research Materials (ERM) covers materials properties, synthetic methods, metrology, and modeling required to support future Emerging Research Devices (ERD), lithography, front end process (FEP), interconnects, and assembly and package (A&P) needs. For *Device Materials*, the scope includes memory and logic devices, the scope includes planar p-III-V, n-Ge, nanowires, carbon nanotubes, graphene and other 2D materials, spin materials, and complex metal oxides. Some of the evolutionary and revolutionary ERD can be fabricated with conventional materials and process technologies that are already covered in other sections of the ITRS, so the ERM chapter will not cover these materials and processes. *Emerging Lithography Materials* includes novel molecules, macromolecules that exhibit the potential to enable ultimate feature patterning with resist, and directed self-assembling technologies which is getting increased attention as a potential lithography enhancement technology. *FEP Materials* include ERM required for future device technologies including technologies to deposit ultra-high κ dielectrics with low leakage, place dopants conformally in predetermined locations (deterministic doping) with low damage to the semiconductor material as well as processes for ultralow resistance contacts and novel materials to support selective etch, deposition, and cleaning of future technologies. *Interconnect Materials* includes emerging materials for extending Cu interconnects (novel ultrathin barriers), novel low resistance sub-10 nm electrical contacts, interconnects, vias, and ultra-low κ inter level dielectrics (ILD). *Assembly and Packaging Materials* includes novel materials to enable reliable electrical and thermal interconnects, polymers with unique and potentially useful combinations of electrical, thermal, and mechanical properties, and ultra-high power density high speed capacitors.

Significant challenges must be overcome for these emerging materials to provide viable solutions for future integrated circuit technologies. To deliver these capabilities, enhanced *Metrology* and *Modeling and Simulation* will be needed to accelerate material evaluation, improvement and capabilities. Furthermore, *Environmental Safety and Health (ESH)* research is needed to enable safe handling of materials in development and manufacturing and environmentally benign use in manufacturing and product life.

2. DIFFICULT CHALLENGES

The Difficult Challenges for Emerging Research Materials are summarized in Table ERM1. Perhaps ERM's most difficult challenge is to deliver material options, with multiple required properties, in time to impact insertion decisions. These material options must demonstrate the potential to enable high density emerging research devices, lithographic technologies, interconnect fabrication and operation at the nanometer scale, and packaging options. This challenge, to identify materials that simultaneously achieve multiple properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies

2 Emerging Research Materials

Table ERM1 Emerging Research Materials Difficult Challenges	
Difficult Challenges 2013-2020	*Summary of Issues*
Achieving desired properties in integrated structures	Identify integrated high k dielectrics with EOT <0.5nm and low leakage Identify integrated contact structures that have ultralow contact resistivity Achieving high hole mobility in III-V materials in FET structures Achieving high electron mobility in Ge with low contact resistivity in FET structures Achieving a bandgap in graphene in FET structures Multiferroic with Curie temperature >400K and high remnant magnetization to >400K Ferromagnetic semiconductor with Curie temperature >400K Synthesis of CNTs with tight distribution of bandgap and mobility Electrical control of the electron correlation, ex. Mott transition, Spin dynamics Simultaneously achieve package polymer CTE, modulus, electrical, thermal properties, with moisture and ion diffusion barriers Thermal interface materials with low interface thermal resistance and high thermal conductivity with desired electrical and mechanical properties. Nanosolders compatible with <200C assembly, multiple reflows, high strength, and high electromigration resistance NanoInks that can be printed as die attach adhesives with required electrical, mechanical, thermal, and reliability properties. NanoInks that can be printed as conductors, via hole fillers, solders, or die attach adhesives with required electrical, mechanical, thermal, and reliability properties.
Characterize and control coupled properties of embedded materials and their interfaces	High mobility transition metal dichalcogenides TMD with unpinned Fermi level and low resistance ohmic contacts High electron mobility in Ge with unpinned Fermi level and low resistance ohmic contacts High mobility in nanowires with unpinned Fermi level Graphene with a bandgap, high mobility, and unpinned Fermi level at dielectric interfaces Complex metal oxides with unpinned Fermi levels Nanoscale observation of the magnetic domain structure, for example, the domain in STT-RAM under the magnetic field, i.e., the dynamic operation Characterization of electrical properties of molecule / metal contact interfaces (i.e. Pentacene/Au) Characterization of electrical properties of embedded nano contact interfaces (i.e. CNT/Metal) CNTs with low resistance contacts on both ends Characterization for density of dislocations and anti-phase boundary generating interface between Ge/III-V channel materials and Si
Identifying manufacturable methodologies to enable deterministic fabrication with required property control	Dopant placement and activation i.e. deterministic doping with desired number at precise location for Vth control and S/D formation in Si as well as alternate materials HVM compatible methods to place dopants in predetermined positions with minimal damage to the semiconductor Manufacturing and purification methodologies of CNT to achieve required purity levels (pure semiconductor with bandgap) Identify DSA process simplification methodologies that can achieve required overlay requirements Wafer scale growth of high quality graphene with desired process conditions (ex. Low temperature growth on metal or insulator) Controlling edge-termination / molecular absorption to graphene to achieve required bandgap Synthesis or assembly of CNTs in predefined locations and directions with controlled diameters, chirality and site-density III-V: Correlation between antiphase domains and electrical properties
Ability to control defects in material processing	Methods to reduce directed self assembly based defects to <0.01cm^{-2} for litho extension Control defects in carbon nanotubes Control defects in growth and processing of graphene Control concentration and locations of cation and anion defects in complex metal oxides Control precipitation in ferromagnetic semiconductors Characterization for density of dislocations and anti-phase boundary generating interface between Ge/III-V channel materials and Si
Control of Self-assembly processes to achieve desired properties reproducibly	DSA for Litho Extension: Simultaneously achieve required feature sizes in predetermined arrays with low anneal time, low defect density DSA for Litho Extension: Efficient CAD models to enable translating design features to guide structures on photomasks. DSA for Litho Extension: Registration of self-assembled patterning materials in desired locations with control of geometry, conformation, interface roughness, and defects DSA for Litho Extension: Achieve realistic device pattern with reduced pattern roughness and defects Demonstrate self assembly's ability to deterministically control locations of dopants conformally on 3D structures

Table ERM1 Emerging Research Materials Difficult Challenges

Difficult Challenges 2021-2028	Summary of Issues
Electric field control of the electrochemical reaction in a nanoscaled device and at an interface	Complex Oxides: Control of oxygen vacancy formation at metal interfaces and interactions of electrodes with oxygen and vacancies Switching mechanism of atomic switch: Improvements in switching speed, cyclic endurance, uniformity of the switching bias voltage and resistances both for the on-state and the off-state. Nano-Carbon / metal functional junction, such as new switch, by using electrochemical reactions Molecular device fabrication with precise control using electrochemical reactions
Metrology to characterize structure and properties of materials at the nanometer scale	Development of the method to evaluate the validity of the measurement result for each ERM Electrical and thermal properties of each carbon nanotube Nanowire characterization of mobility, carrier density, interface states, and dielectric fixed charge effects Graphene and TMD mobility and carrier concentration Complex metal oxide characterization of carrier density, dielectric and magnetic properties Spin materials: characterization of spin, magnetic and electrical properties and correlation to nanostructure Characterization of electrical properties of embedded nano contact interfaces (ex. CNT/Metal) Evaluating material properties in realistic device structures Nanoscale observation of the magnetic domain structure, for example, the domain in STT-RAM under the magnetic field, i.e., the dynamic operation
Metrology to characterize defects at the nanometer scale with atomic resolution	CNT vacancy and interstitial ordering around dopants Nanowires: Characterization of vacancies, interstitials and dopants within the NW and at interfaces to dielectrics Graphene: Characterization of edge defects, vacancies and interstitials within the material and at interfaces Metal nanoparticles: Native oxide interface and crystal defects in the nanoparticle Complex Oxides: Location of oxygen vacancies and the valence state of the metal ions Spin materials: characterization of vacancies in spin tunnel barriers, and defects within magnetic materials and at their interfaces Evaluating material properties IN realistic nm scale devices Characterization of edge structure and termination with atomic resolution (ex. Graphene nano ribbon, TMD, etc.)
Accurate multiscale simulation for predictions of unit processes the resulting structure, properties and device performance.	Linkage between different scales in time, space, and energy bridging non-equilibrium phenomena to equilibrium phenomena Transferable simulation tools for many kinds of materials Development of platform for different simulation tools, such as TCAD and ab-initio calculations Nanowires: Simulation of growth and defect formation within and at interfaces CNTs: Simulation of growth and correlation to bandgap Graphene: Simulation of synthesis, edge defects, vacancies, interstitials, interfacial bonding, and substrate interactions. Atomistic simulation of interfaces for determining Fermi level location and resulting contact resistivity Nanoparticles: Simulation of growth and correlation to structure and defects Complex Oxides: Multiscale simulation of vacancy formation, effect on metal ion valence state and effect of the space charge layer Spin: Improved models for multiscale simulation of spin properties within materials and at their interfaces.
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

A critical ERM factor for improving emerging devices, interconnects, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties.

The difficult challenges listed in Table ERM1 may limit the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and nanostructure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish quantitative relationships between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the design and optimization of the required materials

properties. The need for validated models requires strong alignment between experimentalists and theorists when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

3. INTRODUCTION

The Emerging Research Materials chapter identifies materials to support other technology work groups that could enable continued scaling of integrated circuits with improved energy efficiency for applications where no solutions are known. Many of the ERM material classes, with novel properties, may be applied to solving applications in multiple areas and this is highlighted in Table ERM2.

Table ERM2 Applications of Emerging Research Materials

For ERD Memory devices, the ERM is evaluating materials that could enable higher density memory with improved energy efficiency to change the memory state or read the memory state. To support ERD logic devices, the ERM is evaluating a number of alternate channel materials and structures that have the potential to enable smaller devices with less carrier scattering and thus higher energy efficiency. For beyond CMOS devices, the ERM is exploring materials that could enable information processing with state variables other than charge, such as spin, and that could potentially enable dramatic increases in energy efficiency of information processing and extend it many generations.

For Lithography, the ERM is reviewing the viability of a number of novel photoresist to extend 193nm lithography and support EUV resist. The ERM is also performing a critical assessment of directed self-assembly (DSA) to potentially extend lithography though pattern rectification and pattern density multiplication. Since interest in DSA has increased as a technology to potentially enhance and extend lithography, the ERM is evaluating several block-copolymers to enable sub 10nm patterning to less than 5nm.

For FEP, the ERM is evaluating materials and processes to enable ultrahigh κ dielectrics (EOT<0.5nm) with low leakage, novel concepts to conformally dope multigate structures with precise dopant position control, and identify novel processes and material interfaces to produce ultralow resistance contacts.

To support the Interconnect TWG, the ERM is evaluating novel materials to extend copper interconnects that reduce energy losses and signal delays. In addition, the ERM is exploring carbon (carbon nanotubes and graphene) based electrical interconnects to potentially dramatically reduce electrical resistance and improve energy efficiency of computing.

For Assembly and Packaging, the ERM is exploring materials to modify polymer properties to enable increased product reliability, novel electrical attaching materials to allow lower assembly temperatures and improved product reliability, and techniques to increase the thermal conductivity of electrically insulating flexible materials.

For the ERM to be successfully improved in research and prepared for applications, the environmental safety and health properties of the materials must be understood and available, and metrology and modeling are needed to improve and assess the ERM for the applications. Metrology is needed to characterize the structure and composition at the nanometer scale, and important physical properties whether exposed or embedded in a structure. Modeling is needed of synthesis to determine whether desired structures can be achieved and the properties of these structures modeled to determine how they will function in the application. The requirements for these are explained in more detail in their respective sections.

4. EMERGING RESEARCH DEVICE MATERIALS

The emerging research device materials are listed in the approximate order that they appear in the ERD chapter and are not listed in any order of priority.

4.1. EMERGING MEMORY MATERIALS

Emerging Research Memory Devices includes capacitive memories (Fe FET), and resistive memories including Fe resistance, nanoelectromechanical, Redox memories, Mott electronic effect, macromolecular, and molecular memories. The ERM used in these devices includes, carbon nanotubes, nanowires, complex metal oxides, transition metal oxides, magnetic materials as well as engineered interfaces between these materials. In addition, a number of nanomaterials including carbon nanotubes, graphene, and 2D transition metal chalcogenides are exhibiting properties that may enable new memory devices. The potential advantages and challenges of ERM for Memory Devices are summarized in Table

ERM3. Since many of these devices use complex and transition metal oxides, a section will review challenges for these materials.

Table ERM3 ERM Memory Material Challenges

4.1.1. FERROELECTRIC MEMORY MATERIALS

Emerging Ferroelectric Memories includes the FeFET and the Ferroelectric polarization resistance RAM. The FeFET operates with two stable polarization states available in the ferroelectric film used as a gate oxide. The main issues in FeFETs for nonvolatile memories are the short retention time and charge traps at the Si-ferroelectric interface.[1] Insertion of a dielectric layer such as HfO_2 or Hf-Al-O between silicon and the ferroelectric has strongly improved the retention time. Ferroelectrics with a lower Pr are optimal, which is why $YMnO_3$ (Pr ~5.5 μC/cm^2) has been considered for such applications. However, recently promising results have been achieved with a Pt/$SrBi_2Ta_2O_9$/Hf-Al-O/Si structure.[2] Since the integration of these ferroelectric materials with dielectric layers is challenging, others have evaluated the integration of polymer ferroelectrics with carbon nanotubes[3] or graphene[4] and demonstrated retention times less than a month.

4.1.1.1. FERROELECTRIC TUNNEL JUNCTION MATERIALS

The concept of ferroelectric tunnel junction was proposed by L. Esaki in 1971[3]. A renewed interest has emerged in the last decade due to significant advances in oxide heterostructure deposition and in the control of ferroelectricity in films down to few unit cells thickness[4]. Tunneling electroresistance (TER) has been evidenced at room temperature with a variety of ferroelectric complex oxides such as $BaTiO_3$, $PbTiO_3$ or $BiFeO_3$[5-11]. Ferroelectric tunnel junctions are promising devices for nonvolatile memory applications[12]. Since ferroelectricity is robust down to few nanometers, memory junctions can be fabricated at nanometer scale, which offers a potentially high integration density.

While polarization is switched by the application of an external electric field, it was recently shown that mechanical writing can be used to induce polarization reversal[13] in ultrathin $BaTiO_3$ films (through the tip-induced pressure of an AFM) and thus to induce a TER effect[14]. This could lead to a drastic reduction of energy consumed during the programming steps and further improve the density capabilities of these devices thanks to the localized tip pressure.

These devices are also promising as multiple resistive programmable state devices such as memristors[15,16]. Moreover, it was shown that the ratio of the TER, which has been reported to be up to 100 when using metallic electrodes[15], could be enhanced by two orders of magnitude with a semiconducting material as one of the FTJ's electrodes[17].

4.1.1.2. FeFET MEMORY MATERIALS

The Ferroelectric FET (FeFET) Memory is essentially a MOSFET where the gate dielectric is a ferroelectric film and the memory state is determined by the polarization of the ferroelectric as described in ERD Memory. A primary challenge for this device is the integration of the ferroelectric with the semiconductor channel, because of interface states and interfacial interactions. These issues have been resolved by inserting a thin (13nm) oxide (HfAlOx) buffer layer between the semiconductor and the ferroelectric material $SrBi_2Ta_2O_9$[18]. The gate dielectric passivates the semiconductor surface and is a barrier to interactions between the semiconductor and the ferroelectric. Recently, doped HfO_2 has been found to be ferroelectric[19] and the compatibility of HfO2 with silicon processing may enable better performing FeFETs in the future. In both devices, the retention time needs to be significantly longer to be used as a nonvolatile memory.

4.1.2. REDOX MEMORY MATERIALS

The category of "Redox RAM" encompasses a wide variety of metal-insulator-metal (MIM) structures and materials connected by the fact that they share reduction/oxidation (redox) electrochemistry as an important component of their physical mechanism for changing the resistance state from high to low or the reverse [20-22]. The mechanism depends on both the electrode material and the oxide material used. The Emerging Research Devices Chapter identifies different Redox memories by their mechanism as 1) Electrochemical Metallization Bridge, 2) Metal Oxide: Bipolar Filament, 3) Metal Oxide: Unipolar Filament, and 4) Metal Oxide: Bipolar Interface Effects. In the Electrochemical Metallization Bridge, an electrode such as Cu or Ag is used, these electrodes provide ions that can migrate through the oxide and produce metallic filaments and are turned on and off by the movement of ions at the tip of the filament. The metal oxide: bipolar filament and the metal oxide: unipolar filament employ "inert" electrodes such as Pt, Ti, TiN, that don't migrate through the oxide and the differentiation of operation (bipolar vs. unipolar) is determined by the selection of oxide material. In the oxides used for these devices, a filament is formed in the high voltage "forming" process and the switching occurs at the "tip" of the filament. For bipolar switching materials, application of a negative voltage causes ions to move out of the space between the filament and the electrode, thus producing a thin insulating high resistance region. For unipolar filament materials, application of a higher positive higher voltage causes increased current that generates

heat and causes conductive ions to be reintegrated into the lattice at the filament tip which produces an insulating region. For the metal oxide: bipolar interface effects, a thin metallic oxidizable film is placed between the inert electrode and the oxides that would normally be used for the "metal oxide: bipolar filament" devices and switching occurs as the thin oxidizable film increases or decreases oxygen vacancies in the oxide which increase and decreases the resistance of the thin oxide film. Multiple approaches are being employed to improve switching repeatability and reliability including bi-layer oxides with oxygen rich and deficient I-layer, doped oxides by metallic ions with manipulated valance values, voltage controlled forming processes. Recently, devices constructed of transition metal oxides have been demonstrated with less than 10nm feature size and improved switching properties and reliability[23].

Critical challenges for redox memory include establishing processes that enable reproducible resistance changes across many cells and processes that enable 3D integration with high on-off ratio select devices. With the filament forming materials and their devices, the resistance of devices doesn't correlate with the area of the device, while there is a stronger correlation of resistance of the interface devices with device area. For redox memory to be adopted, atomistic model of operation are needed that accurately correlate materials, processing, and interfaces with forming and switching behavior

4.1.2.1. ELECTROCHEMICAL METALLIZATION BRIDGE

In the Electrochemical Metallization Bridge structures, one of the electrodes is Ag or Cu, while the other electrode is "inert". As a "forming" field is applied to the structure, the Cu or Ag ions diffuse through the insulating layer to the opposite electrode and are reduced to form a metallic conductive filament[24,25]. Many chalcogenide compounds have been used to make these devices including, oxides, sulfides, and selenides. The switching mechanism is associated with a conductive bridge being completed and broken by the movement and reduction of ions at the tip of the conductive filament[25]. When metal electrodes with mobile ions, such as Cu and Ag are used, the RRAM devices exhibit either "nonpolar" switching characteristics or unipolar switching. Unipolar switching is often associated with the thermal breaking of the filament at the electrode either near the electrode interface or in the bulk of the I layer. On the other hand, nonpolar switching in HfO_2 devices with Cu and Ni top electrodes[26] may be the result of metal filaments with both oxygen vacancy and metal ions interacting between the filaments and the electrodes.

4.1.2.2. METAL OXIDE: BIPOLAR FILAMENT

For the "Metal Oxide: Bipolar Filament" the electric field of the forming process causes oxygen ions or vacancies to migrate and form a conductive filament in the insulating layer (I-layer). In the case of TiO_2, the formation of Ti_4O_7 (Magneli phase) filaments has been reported [27]; however, this needs further study to determine whether the same mechanism would apply to materials grown in a wider range of conditions. The exact composition of the filaments of different oxides has not been determined but these are believed to be caused by oxygen vacancies. While many transition metal oxides have been fabricated in these devices, the most popular materials are HfOx, TaOx, TiOx (x indicates that the materials may not have stoichiometric compositions.

4.1.2.3. METAL OXIDE: UNIPOLAR FILAMENT

For "Metal Oxide: Unipolar Filament" devices, the most common insulating material is NiO, although this effect has been recently identified in HfOx films with a Ni electrode[28]. A number of other transition metal oxides including TiO_2[29] HfO_2[30] are reported to operate with both bipolar and unipolar switching mechanisms and it is proposed that the reset to the high resistance state occurs through vacancy annihilation. With unipolar switching, the reset occurs as a result of thermal heat generation causing changes in the transition metal conductivity in the space between the filament and the electrode. Control of the thermal conductivity of adjacent structures is required for reproducible switching[31].

4.1.2.4. CONTROL OF VACANCIES AND FILAMENTS IN METAL OXIDE DEVICES

Significant research has been performed over the past two years to identify materials and processes that could enable reproducible switching that is reliable over the expected life of the memory. Approaches to improve reproducibility include performing the "forming" process with lowest possible voltages with pulses, doping the oxides with other materials, depositing novel electrode structures, and depositing electrode materials with processes that improve interface quality, multiple metal oxides stack, and optimized dielectric constant as well.

In transition metal oxide memories with "inert" electrodes, the forming process establishes conductive filaments that have high concentrations of oxygen vacancies and several approaches have been investigated to improve the reproducibility of these filaments. Applying low voltage pulses that eliminate breakdown has been found to improve device reproducibility and reliability[32]. Studies of the filaments suggest high concentrations of oxygen vacancies in HfO_2[33] and another study indicates that switching is accomplished by field assisted diffusion of oxygen vacancies moving out of the filament toward the electrode. Another study indicated that filament formation has both an exponential dependence on field and thermal activated processes[26]. Thus, for oxygen vacancy filament formation, it is important to avoid thermal runaway

situations. One study indicated that below a critical device area the rate of filament formation decreases inversely with the area[34], so filament formation times may increase for very small devices. One study identified growth of Ag nanocrystals on the top electrode which focused the fields and may have attracted vacancy filaments to the tip of the nanocrystals by electromigration in ZnO [35].

To understand the scalability of these devices, it is important to characterize the spatial extent of the "filament" and determine whether this changes with memory cycling. It is also critical to understand whether one continuous filament connects the electrodes or whether multiple sub-filaments form a path with "communication" through dielectric gaps, since the switching mechanisms could be very different.

4.1.2.5. METAL OXIDE: BIPOLAR INTERFACE EFFECTS

For "Metal Oxide: Bipolar Interface Effects", an insulating tunnel barrier oxide is placed between the electrode and a conductive oxide and switching is proposed to be caused by vacancy exchange between these layers. Since vacancy concentration is important in these structures, control of vacancy concentration is important. Depositing a thin Ti layer in the TiN/Ti/TiO2/TiN was reported to control oxygen vacancy concentration and thus control the resistance in the on and off states[32]. Similarly, the HfOx transition layer between Hf/HfO2 in TiN/HfO2/Hf/TiN structures is reported to be a source of oxygen vacancies that form the conductive filaments[23]. It has also been reported that deposition of the top TiN electrode with PEALD on a TiN/HfO2/Hf/TiN device produced more reproducible switching characteristics than those deposited with reactive PVD[37]. Studies of the effect of annealing conditions on TiN/Ti/HfOx/TiN indicate that oxygen accumulation in the electrode materials is important to switching in these devices[38]. Thus, the quality of interfaces to the insulator appears to play an important role for controlling vacancy concentrations in the insulator.

Doping the insulator is also proposed as a way of increasing controlling oxygen vacancy concentration. In TiO2, modeling predicts that doping with metals with manipulated valance values increased vacancy concentration[39] and this could be controlled by selecting metals based on their valence configuration..

4.1.2.6. REDOX MEMORY METROLOGY AND MODELING NEEDS

Metrology is needed to characterize and validate the switching mechanisms of devices in realistic materials (typically polycrystalline or amorphous) that have grain boundaries and dislocations that could act as nucleation sites for formation of the conductive filaments in these materials. This metrology is needed to validate the "filament" formation mechanism and the switching mechanism in operating devices.

Since metrology may not be able to validate switching mechanisms, accurate models of filament formation, vacancy and ion field assisted drift/diffusion are needed to validate the physical mechanisms. Since multiple models exist, developing accurate validated models of filament formation and switching mechanisms is critical for the industry to adopt this technology.

4.1.3. MOTT MEMORY MATERIALS

As mentioned in the Emerging Research Devices Memory Section, the Mott Transition (a metal-insulator transition driven by the injection of carriers into the insulating material) has been reported in a number of transition metal oxides and complex metal oxides. The nonvolatile switching mechanism in NiO[40] depends on control of oxygen vacancy concentration. Although this is attributed to a nonvolatile Mott transition, the switching behavior is very similar to that in doped ZrO_2 and Cu doped NiO[39]. Studies of $Pr_{0.7}Ca_{0.3}MnO_3$ indicate that oxygen vacancy concentrations increase at the surface, in the high resistance state, and change carrier concentration which drives the metal-insulator transition[41].Thus, the metal insulator transition, whether volatile or non-volatile, appears to be driven by either field dependent vacancy concentrations or field driven charge trapping in vacancies. Recent discoveries of 2D electron gases in complex metal oxide heterointerfaces[42] may open opportunities to couple ferroelectrics[43] with the 2DEG and produce a memory effect that is less sensitive to temperature.

4.1.4. MACROMOLECULAR MEMORY MATERIALS

As is discussed in ERD Memory Devices, macromolecular memory devices consist of a polymer with two electrodes and often other materials embedded in the structure (i.e. oxides on one electrode, metal or oxide nanoparticles, etc.). While differences exist between the operation of these structures, progress has been made in understanding the operation of the macromolecular memory with an oxide on one metal electrode. In this structure, the switching occurs in the oxide and the polymer acts as a current limiting element[44].

4.1.5. MOLECULAR MEMORY MATERIALS

Molecular devices are described in the ERD chapter. Significant challenges must be overcome for them to be useful, including; fabrication of low potential barrier electrical contacts, reliable operation, the high resistance of molecules in

their "on" state, and deposition of the top contacts that don't change molecular properties. Molecular state devices are reported to exhibit a range of useful properties, including non-linear IV and bi-stable behavior, but the electrical performance of many molecular-based devices currently under study appear to be dominated by the high potential barriers of each molecule-electrode contact or defect-like processes. Results suggest that changes in molecule-contact conformations, contact metal migration, or near neighbor interactions may be responsible for observations of electrical switching.[45, 46] Despite significant challenges and knowledge gaps, these emerging molecular systems show some promise for reducing device variability and enabling very high density circuit functionality.

The biggest challenge to fabricating reliable molecular devices may be deposition of the top contact materials without degrading the molecules while producing high quality electrical contacts. Parameters ranging from the bond dipole to molecular orientation affect charge-transport parameters and switching voltages. Research is needed to elucidate the structural and electronic properties of molecule/substrate and top contacts, in order to engineer these contacts with reliable performance characteristics. Additional molecular modeling, synthetic, and experimental work, exploring the dependence of the metal work function on new molecular contacts, is needed.

4.1.6. EMERGING NANOMATERIALS WITH POTENTIAL FOR MEMORY DEVICES

Several nanomaterials including carbon nanotubes, graphene, and 2D transition metal chalcogenides (e.g. MoS_2, WSe_2, etc.) have been integrated into device structures and demonstrated resistances changed after application of a field. After a forming process, the resistance of graphene nanoribbons was found to change between low resistance and higher resistance states with application of voltage[47]. It was proposed that the resistance change of the graphene was caused by changes of carbon hybridization from sp^2 to sp^3. A conventional floating gate memory was fabricated with a MoS2 channel, an HfO2 gate dielectric and a graphene floating gate[48]. Heterostructures of BN-MoS2-graphene were found to effectively trap charge depending on the order of stacking and thickness of the layers[49].

4.2. EMERGING LOGIC MATERIALS

Emerging logic materials includes alternate channel materials to extend CMOS, materials for charge based Beyond CMOS devices, materials for non-charge based Beyond CMOS devices, and spin state and transport materials for multiple Beyond CMOS applications.

4.2.1. ALTERNATE CHANNEL MATERIALS

Emerging logic materials include alternate channel materials to extend CMOS to the end of the roadmap, materials to support charge based non-conventional FETs, and materials to support non-FET, non-charge-based Beyond CMOS devices. In some cases, materials and processes will be useful for multiple device types, so they will be discussed in detail for one application and differences highlighted for the other applications.

Alternate channel materials to silicon MOSFET's are being intensively explored, because increasing the performance and energy efficiency of integrated circuits by scaling silicon CMOS is becoming more difficult even with strained silicon channels. The principal property where performance can be enhanced is the channel mobility. Alternate channel materials with potentially higher mobilities are being explored to extend CMOS scaling with high performance and improved energy efficiency. Examples include III-V semiconductors, Ge, graphene, carbon nanotubes, and other semiconductor nanowires. These carrier-transport enhanced channels can provide higher on-currents, I_{on}, and lower gate capacitance at constant I_{on} (due to the reduced device area). This combination can result in higher MOSFET performance at reduced power. To achieve complimentary MOS high performance, co-integration of different materials (i.e. III-V and Ge) on silicon may be necessary. Significant materials issues such as defect reduction, interface chemistry, metal contact resistivity, and process integration must be addressed before such improvements can be achieved.

The potential advantages and challenges of these nanostructured semiconductors are described in more detail in Table ERM4.

Table ERM4 Challenges for ERM in Alternate Channel Applications

Carbon based (CNT and graphene) devices have been identified as needing more focus to accelerate their potential use as alternate channel materials and for use in Beyond CMOS applications. The ERM and ERD chapters also identify when solutions are needed to overcome the difficult challenges that must be overcome for these materials to be viable in the required timeframe as is highlighted in Table ERM4.

4.2.1.1. CARBON NANOTUBE FET MATERIALS

The primary potential advantages for carbon nanotubes are their very high carrier mobility[50] and ultra-thin body, but very difficult challenges must be overcome for them to realize their promise. Key challenges for carbon nanotubes to be viable in high performance FETs are: the requirement for processes that provide a high purity of semiconductor tubes; the positioning of each nanotube in a desired location, with a specified direction, high adhesion to gate dielectrics; p- and n-type contacts with low resistance, and nanotube growth compatible with CMOS. The advantages and challenges are highlighted in more detail in Table ERM4. Please refer to the 2013 ITRS ERD chapter for details on these devices.

4.2.1.1.1. NANOTUBE PURITY CONTROL

For SWCNTs to be viable for future CMOS applications, the ability to have high semiconductor purity (vs. metallic CNTs) must be demonstrated. Recent experiments have been able to separate metallic CNTs from semiconducting CNTs and achieve purities of 99.9%[51] through multiple column gel chromatography separations. While this is not adequate for integrated circuit manufacturing, repetitive use of this technique may be able to achieve higher purity levels. Recently, temperature controlled interactions between SDS functionalized carbon nanotubes and an alkyl dextran-based gel has sorted specific chiralities of nanotubes[52]. Furthermore, the spontaneous separation of small diameter semiconducting nanotubes from larger diameter metallic nanotubes has been demonstrated in immiscible aqueous phases formed by the addition of polyethylene glycol (PEG) and dextran[53]. For aligned carbon nanotubes grown on quartz, the approaches for purification include electrical breakdown[54] and thermocapillary and etch[55]. Electrical breakdown is able to remove metallic CNTs and nanoscale thermocapillary and etch has been able to achieve a purity of 99.997%[56]. Once carbon nanotubes have been purified, with certain chiralities, they can be grown longer with vapor phase epitaxy; however, the length of extension depends on CNT chirality[57]. Growth of CNTs on quartz continues to make progress and two purification approaches are electrical breakdown of the metallic nanotubes and thermocapillary and etch.

4.2.1.1.2. CONTROL OF POSITION AND DIRECTION

For CNTs to be used for devices, they must be placed in precise locations and aligned in required directions, with high density. The ability to place 500CNTs/μm has been demonstrated from liquid with the Langmuir–Schaefer assembly method[57]. Growth of CNTs on quartz continues to make progress and two purification approaches are electrical breakdown of the metallic nanotubes.

4.2.1.1.3. CONTROL OF CARRIER CONCENTRATION (NANOTUBE DOPING)

A critical device challenge is carrier concentration control in embedded p-type and n-type materials. Typically, semiconducting CNTs tend to be p-type in ambient air. Little progress has been reported in the past two years in doping technology to control of carrier concentration. The use of gate work function to control carrier concentration seems the most likely path forward. A CMOS compatible technique to control carrier polarity has been reported using charges incorporated in gate dielectric[59,60], but its controllability and reliability should be assessed.

4.2.1.1.4. GATE DIELECTRIC INTERFACE

Since a CNT's sidewall is relatively inert, it is hard to deposit uniform ultra-thin film on them, but chemically functionalizing the surface may improve dielectric adhesion. Research and guiding material design principles are needed for enhancing functionalization, interface passivation, and dielectric deposition. Alternatively, some metals such as Y and Ti adhere to CNTs, and can be oxidized to form high-k dielectric. Uniform 5nm Y_2O_3 has been realized on a CNT[61]; however, the interface quality and reliability should be determined. A back gate dielectric of LaOx, with CNTs dispersed on the gate dielectric has demonstrated high dielectric constant and low subthreshold slope(~69mV/dec.)[62]; however, this was not deposited on the CNT.

4.2.1.1.5. CONTACT FORMATION

Pd is the most commonly used p-type contact material with resistance approaching the quantum contact resistance[63] recently Sc-CNT [64] have been employed to fabricate n-FETs. On the other hand, researchers have also reported high variability in contact resistance for small diameter nanotubes. A method to reduce Schottky barrier has been proposed by modulating potential in the vicinity of contact interface.[65] Furthermore, the contact resistance of solution processed CNTs was found to decrease after exposure to oxygen[66] and it was proposed that the oxygen improved the band alignment between the CNT and metal contacts and introducing a graphitic carbon interfacial layer also reduced contact resistance[67]. Recent important findings are the contact length dependence of contact resistance.[68] Further investigation is necessary to understand the origin of these effects on contact resistance. A CMOS compatible, reproducible contact formation technique needs to emerge from research before 2016.

4.2.1.2. GRAPHENE AND NEW 2D FET MATERIALS

These materials include graphene, silicene, germacane, MoS_2, $MoSe_2$, WS_2, Wse_2, and other 2D planar chalcogenides. The primary advantage of these materials is their potentially high mobility and the ability to process in a planar form. While graphene doesn't have a bandgap, germacane, and the transition metal chalcogenides have bandgap. The critical issues for these materials include the ability to:

1. For graphene, generate and control a bandgap
2. For all 2D materials, achieve a high mobility on a silicon compatible substrate
3. Reduce or control surface and interface effects on charge transport
4. Deposit 2D materials over large areas with controlled grain size, thickness, and orientation on silicon compatible dielectrics
5. Deposit a high κ gate dielectric with a high quality passivated interface
6. Form reproducible low resistance contacts (contacting without etching through a monolayer film)
7. Integration, doping and compatibility with CMOS

4.2.1.2.1. DEPOSITION OF GRAPHENE

The preferred approach for deposition of these materials would be a CVD "like" process or epitaxial process on a silicon wafer; however other techniques could be used. While progress has been made in growing large grain graphene on Cu foil[68], it must still be mechanically transferred to silicon wafers. .

4.2.1.2.2. FORMATION OF HIGH QUALITY 2D CRYSTALLINE MATERIALS

Mechanical exfoliation of graphene has produced high quality films on silicon[69], but control of location and thickness may not be adequate for development of integrated circuit technologies. The decomposition of SiC[70] has the advantage that the graphene is grown on a silicon-like substrate, but it requires process temperatures of ~1200C or above. Epitaxial graphene on SiC has exhibited carrier mobilities as high as 15,000cm^2/V-s[71] and 250,000cm^2/V-s [72] at room temperature and liquid helium temperatures respectively.

Large areas of graphene have been grown with CVD on Cu foil[73] with room temperature electron mobilities as high as 25,000$cm^2V^{-1}sec^{-1}$ [74]. While these graphene films are deposited on metals, transfer of these films has been demonstrated to SiO2/Si substrates where device structures have been fabricated and properties characterized[73,75-77]. While these CVD techniques are not directly on a silicon compatible substrate, the use of polycrystalline substrates with thin film transfer may offer a more cost effective approach. On the other hand, transfer-free fabrication of graphene-channel transistors has recently been demonstrated [78,79]. More recently, a novel approach for wafer-scale transfer has been proposed [80]. This appears to be a fast developing area, so new work may quickly surpass these results.

4.2.1.2.3. 2D MATERIAL MOBILITY

The highest mobility of free-standing graphene at 240K is 120,000 cm^2/V-s[81], which was achieved by driving adsorbed molecules from the surface of the graphene, and it has been proposed that flexural phonons limit the room temperature mobility of free standing graphene[82]. At the liquid helium temperature, the mobility of suspended graphene was shown to be as high as 1,000,000 cm^2/V-s[82]. Mobility of 70,000 cm^2/V-s has been achieved at room temperature by using dielectric screening with solvent dielectrics having a dielectric constant of 47.[83] Graphene sandwiched between h-BN crystals have shown mobilities of ~100,000 cm^2/V-s at room temperature [84]. For top gated graphene transistors with a high κ dielectric, mobilities as high as 8000 cm^2/V-s[85] have been reported. As for CVD graphene, recent characterization indicates that grain boundary scattering is responsible for this degradation of mobility[86]. However, mobility values as high as 25,000 cm^2/V-s have been obtained for CVD graphene[74], which are very close to those of exfoliated graphene.

For transition metal chalcogenides, the extracted mobilities depend on the contact materials and gate dielectrics used. For monolayer films, the highest reported mobilities are in the range of 200-380 cm2/V-s for FET structures.

Material	Thickness	Contact	Gate Dielectric	Mobility (cm2/V-s) (298°C)
MoS_2	10nm	Sc	15 nm Al_2O_3	700[87]
MoS_2	monolayer	Cr/Au	Top 20nm HfO_2, Back SiO_2	380[88]
WSe_2	0.7nm (ml)	Pd/Au	ZrO_2	Hole 250[89]
$MoSe_2$	3-80nm	Ni	SiO_2	Electron 50[90]

4.2.1.2.4. BANDGAP

Graphene has a zero bandgap but several techniques for generating a bandgap have been reported as discussed in the 2011 ITRS ERM Chapter. To date, a commercially viable technique for generating a bandgap in graphene has not been demonstrated. Furthermore, generation of a bandgap in graphene will result in a degradation of mobility in general. Some applications, i.e. microwave FETs, don't require a bandgap, so device applications may emerge that don't require a bandgap. Thus, interest in graphene as a FET material is declining, while interest in the transition metal dichalcogenides has increased. However, if graphene nanoribbons with smooth edges and a controlled band gap are formed, as demonstrated in recent studies [91, 92], their mobility can be as high as that of CNTs and they can be an ideal channel material for FETs. Thus, the mass production method of such nanoribbons is really awaited.

Indeed, transition metal dichalcogenide monolayers have bandgaps of: MoS_2 (1.9eV)[93], $MoSe_2$ (1.49eV)[93], WS_2 (1.93eV), WSe2 (1.60eV); however, their mobility has only been demonstrated to be in the 200-400cm^2/V-s range to date.

4.2.1.2.5. HIGH K GATE DIELECTRIC DEPOSITION

Since the graphene surface is chemically unreactive high κ dielectric deposition is normally initiated at edges or defects in the film. This has been demonstrated with the deposition of HfO_2 and Al_2O_3 on graphene.[94] High k dielectrics have been deposited on transition metal dichalcogenides with atomic layer deposition including HfO_2 deposited on MoS_2[88] and ZrO_2 on WSe_2 and MoS_2[89].

4.2.1.2.6. DOPANT INCORPORATION AND ACTIVATION

If graphene is to be used for extreme CMOS applications, processing must be capable of doping the material p-type and n-type for the channel region and either metallic or n-type or p-type for the S/D region. To date, the proposed approaches for doping the channel regions are to 1) deposit the graphene on a surface that injects carriers into the graphene layer and 2) chemically bonding dopants at edge states of a graphene nanoribbons, as was described in more detail in the 2011 ITRS ERM Chapter. For doping of transition metal dichalcogenides, WSe2 has been doped heavily p-type through chemisorption of NO_2 in the source/drain regions[95] while WSe2 and MoS2 have been degenerately doped n-type through the deposition of potassium in the S/D regions[96].The challenge with these doping techniques will be to maintain the carrier doping in an integrated structure with interconnects. Since the S/D doping will be affected by the contact metallurgy, as will be covered in the contact formation section below. A viable technique to control doping and carrier concentration in graphene needs to emerge from research before 2014.

4.2.1.2.7. CONTACT FORMATION

The source-drain contacts need to provide a low resistance electrical contact to the graphene, but also maintain the graphene in the conductivity type that is needed for the n-channel or p-channel device. Ohmic contact formation may be easier than in small diameter carbon nanotubes, but more research is needed. There have been several studies regarding the contact resistance between electrodes and graphene channel [97-99]; however, the contact resistance obtained so far is not yet low enough for CMOS application. Additionally, the charge transfer length at metal/graphene interfaces has been measured to be several hundred nanometers long and needs to be reduced significantly. Clearly, more research is needed for this issue. For contacting transition metal dichalcogenides, Pd/Au contacts with WSe2 has been doped heavily p-type through chemisorption of NO_2 in the source/drain regions[95] while Au contacts to WSe2 and MoS2 degenerately doped n-type with potassium in the S/D regions[96]. Use of a thin poly(ethylene oxide) PEO doped with $LiCLO_4$ as the gate dielectric increased mobility and reduced contact resistance in MoS_2[100].

4.2.1.3. NANOWIRE FET MATERIALS

Metal-catalyzed nanowires (NW) and patterned and etched(top down fabricated) NW have been suggested as the channels of MOSFETs. The top down fabrication of NW enables precise control of location and direction, which is an advantage over metal catalyzed growth of NW. The potential advantages of nanowires are 1) compatibility with gate-all-around structure that improves electrostatic control, 2) nonclassical physics at small dimensions. Furthermore, with nanowires it is possible to fabricate defect free lattice mismatched heterojunctions in the growth direction[101] and low defect density heterojunctions in the lateral direction[102], which could enable flexibility in device design. On the other hand, there are significant challenges to realize these advantages with catalyst grown nanowires integrated into CMOS including: (a) identifying catalyst materials compatible with CMOS, (b) control of placement, (c) size and shape, direction, and (d) doping. These are described in more detail in Table ERM4.

Non-classical quantum effects depend significantly on the Bohr radius and this varies widely between materials. The Bohr radius in Si is short, and bandgap changes have been observed to occur below 6nm[103], which could increase variations in Vt. Top down fabricated nanowires that have rectangular cross sections had higher mobility at low fields than those that had been annealed to round the edges of the structures[104]. The cause of this mobility degradation with the rounded edges was an increase in Dit[105] for the devices. Top down fabricated surround gate devices are an evolution of FinFET and other Multigate (MuG FET) approaches. Patterned and etched sub 5nm silicon NW has been reported to have room temperature quantum oscillatory behavior with back-gate voltage with a peak mobility approaching ~900 $cm^2\ V^{-1}\ s^{-1}$ [106]. For silicon and germanium grown nanowires, the key challenges are to demonstrate that they would have a higher performance than top down fabricated NW devices and to grow them in desired locations with required directions. Although incorporation of catalyst (i.e. Au) is a significant concern, the ability to fabricate Esaki diodes with good electrical properties[107] indicates that the Au catalyst didn't affect device performance. There have not been any reports of grown nanowires having higher mobility than patterned and etched structures. In addition, the ability to grow nanowires in controlled locations with controlled direction (especially in the wafer plane) continues to be challenging. On the other hand, the ability to grow Si nanowires with a square cross section has been demonstrated with cubic $\alpha NiSi_2$ catalyst[108] on Si(111) substrates. Thus, while progress has been made in the ability to control the shape Si nanowires, little progress has been made in demonstrating performance improvement over patterned and etched NW and controlling location and direction of growth (in plane).

III-V nanowires offer the potential advantages of higher mobility, on-off current ratio, and subthreshold swing than can be achieved with conventional silicon circuitry. The ease with which the band structure can be engineered also opens the possibility for transistors that use two-dimensional electron gas conduction for even higher mobility than can be achieved in the homojunctions, or for devices based on tunneling through epitaxial barrier layers made from semiconductor layers with higher band gap. InAs nanowires grown with CVD and Au catalyst have been reported to have mobility as high as $6000cm^2V^{-1}s^{-1}$. On the other hand, these nanowires are typically grown perpendicular to the wafer surface at CVD temperatures; however their optical properties could enable integration of lasers, and detectors on silicon circuits for high speed optical communication.

Although horizontally grown NW have not made much progress in controlling direction, progress has been made in controlling location and direction of vertical NW. Furthermore, n-type doping in SiNW has been increased to 1.5E20cm-3 109 and p-type doping has increased to 2E18cm-3 at growth temperatures of <500C. Furthermore, MOSFETs110, Schottky Barrier FETs111, IMOS112 and Tunnel FETs113 have been fabricated on grown nanowires.

Although nanowires have potential advantages as the channels of field-effect transistors, significant challenges must be overcome for them to be integrated in high density applications. Processing of dense arrays of laterally placed nanowires with surround gates and low resistance contacts may be challenging.

4.2.1.4. P-III-V CHANNEL MATERIALS

For n-channels, InGaAs quantum well FET's on silicon have been reported with mobilities of 10,000 to 3000 $cm^2/V\text{-}s$ [114] using 1.2-micron buffer layers and for strained Ge quantum well p-channels, mobilities of 770 $cm^2/V\text{-}s$ at 5e12 cm^{-2} [115] have been reported. The n-channel enhancement is a 30X improvement over Si channels and the p-channel mobility is a 2X improvement. These mobility increases over silicon channels are significant and would result in reduced power and higher drive currents if they could be successfully integrated in a CMOS FET process without degrading the mobilities. However process complexity and costs would be greatly reduced if the n-channels could be made from strained Ge and the p-channel made from Ge. Similarly, producing both n and p channel devices on III-V could also reduce complexity and cost. Then the choice of complementary channel materials and processes could be based on either Ge or III-V alternate channels rather than both in the same process. This section describes progress being made on Ge n-channels and

InGaSb p-channels in silicon MOSFET's. The n-channel InGaAs and p-channel Ge status may be found in the PIDS chapter of this ITRS.

p-channel III-V quantum wells—The highest hole mobility reported for InGaSb quantum well continues to be 1500cm2/V-s as reported on HEPT[116]. Furthermore, GaSb QW structures with 1-3% biaxial strain have been measured with Hall mobilities of 1200-1500cm^2/V-s[117]. Recently, an $In_{0.2}Ga_{0.8}Sb$ QW has been reported with electron mobility of 4000cm^2/V-s and hole mobility of 900cm^2/V-s[118] thus providing a potential path to complementary III-V logic.

4.2.1.5. N-GE CHANNEL MATERIALS

The Hall electron mobility of bulk Ge is significantly higher (3900 cm^2/V-s) than bulk Si (1600 cm^2/V-s) but degrades significantly in the n-channel of MOSFET's to 150 cm^2/V-s at N_{inv}=1.2e13 cm^{-2} whereas Si electron mobility is 250 cm^2/V-s at this N_{inv}. The main reason for this degradation in Ge n-channel mobility is the presence of high density of interface traps near the conduction band resulting from germanium oxide instability. Germanium oxide contains two valence states over a wide range of temperatures. The use of ozone (O_3) for oxidation has reduced the number of interface traps by forcing the oxide to be mostly tetravalent[119,120]. Recent results have demonstrated electron mobilities of 1050cm^2/V-s[121] with a rapid thermal passivation of GeO_2 and 1,500 cm^2/V-s[122] with a yttrium oxide (Y_2O_3) gate dielectric with low interface trap densities in both cases. GeSn alloys have also demonstrated to have higher hole mobility and modeling predicts higher electron mobility. Progress has been made in reducing the interface trap density at the GeSn-high k interface, but mobility has not been measured[123]. The recent progress in growing high k dielectrics with low interface trap densities and high electron mobilities make Ge and possibly GeSn promising candidates for complementary Ge CMOS devices.

4.2.1.5.1. CO-INTEGRATION OF III-V AND GE

The integration of either III-V compounds or Ge with CMOS devices will be challenging, but if both are integrated on CMOS the challenges will be even more complex. Recent progress with higher hole and electron mobility InGaSb and n-Ge may enable complementary CMOS with either Ge or III-V devices; however challenges remain that must be addressed including defect control, interface chemistry control, dopant incorporation and activation, and source/ drain formation with low resistance contacts. For growth of III-V materials on silicon, selective growth in deep trenches that "trap" dislocations and is called "aspect ratio trapping". An alternative approach to using InGaSb is to produce a compressively strained InGaAs layer which has an enhanced hole mobility and thus only needs the InGaAs for both n and p type devices.

4.2.1.5.2. DOPANT INTEGRATION AND ACTIVATION

Incorporation and activation of dopants in III-V materials can be achieved at low temperatures, but activation of dopants in Ge requires high process temperatures for n-type dopants.[124] Recent work using metal-induced dopant activation in Ge has shown that activation may be achieved as low as 380°C.[125] Thus, if Ge and III-V devices are fabricated on the same substrate, these competing requirements may require the Ge devices to be fabricated prior to the growth of III-V materials, which may significantly increase the integration complexity.

4.2.1.6. TUNNEL FET MATERIALS

Tunnel FETs employ band to band tunneling to achieve sharper turn-on characteristics. They can be fabricated with conventional processing of the alternate channel materials discussed above, so new materials will not be required. A more detailed discussion on the Tunnel FET can be found in the ERD Logic Section.

Nanostructure: As devices scale to smaller dimensions and 13multigate structures, this may affect the subthreshold characteristics of nanoscale devices. Silicon nanowire TFETs have been reported to have subthreshold slopes as low as 30mV/dec. for 20nm diameter nanowires, and the subthreshold slope increased to ~100mV/dec. as the diameter increased to 50nm[126]. Thus, gate all around structures with small diameter channels and TFET may improve device subthreshold slope.

4.2.1.7. ALTERNATE CHANNEL CRITICAL ASSESSMENT

The ERM and ERD have performed critical assessments of some of the same devices. The ERD assessment assumes that all of the integration and fabrication issues are resolved, while the ERM assesses the difficulty of resolving the materials, processing, and integration issues. This ERM survey is based on votes of whether an alternative should be better than CMOS (3), the same as CMOS (2) or worse than CMOS (1). In the ERM critical assessment, Table ERM5, all alternate channel materials except transition metal dichalcogenides and nanowires were viewed to have potentially the same or better mobility than silicon CMOS. From an integration perspective, Ge, and III-V were viewed as comparable to silicon

with average scores of (2.0) and (1.8) respectively while other materials were viewed less favorably with average scores of ~1.6. As indicated in the table, entries that exceeded an average vote of 2.0 over the categories were viewed as being "easy' to integrate into CMOS (none of the options met this criterion). Entries that exceeded an average vote of above 1.7 were viewed that they should be possible to integrate onto CMOS with significant work, and n-Ge and p-III-V met this criterion. Even though Ge, III-V, and nanowire materials were viewed more favorably, each had significant issues that must be addressed. For p-III-V materials, the biggest concerns were the ability to grow defect free material on silicon and high κ gate dielectric. One of the biggest concerns for the other materials was the ability to place them in desired locations with a manufacturable process, with CNTs having the lowest score. The technical challenges for all of these materials are described in more detail in the alternate channel section.

This critical assessment is based on voting by ten ITRS participants from the ERM, ERD, FEP and PIDS technology workgroups and will be updated in the ERM in future ERM revisions.

Table ERM5 Alternate Channel Materials Critical Assessment

4.2.2. CHARGE BASED BEYOND CMOS MATERIALS

4.2.2.1. SPIN FET AND SPIN MOSFET MATERIALS

The spin transistor includes both "Spin FET" and "Spin MOSFET" devices. Both devices have magnetic Source/Drain with a semiconducting channel and a MOS gate, materials used are described in Table ERM6. The channel of the spin FET is a material with high spin orbit coupling such as GaAs or other III-V compounds, while the channel region of the Spin MOSFET is a material with low spin orbit coupling. In both devices, the spin is injected from the ferromagnetic source, and then transported through the channel to the drain and electrons with spin aligned with the drain are passed and generate current. In the case of the Spin FET, the source and drain have the same spin alignment, the gate voltage couples to the spin through the spin-orbit coupling and changes the spin precession angle, and the drain accepts spins with the same alignment, so current is modulated. In the case of the spin MOSFET, the alignment of the drain magnetization is fixed, while that of the source can be changed, so the gate allows current to flow from the source to the drain without modulation. In these devices, the injection of spin is important and can be achieved through either a Schottky barrier or a tunnel barrier, and both of these materials are described in the (Spin Materials Section). The channel materials and gate dielectrics are described in the ERM Alternate Channel Section and the Spin Transport Materials Section while material options for the S/D are described in Ferromagnetic Materials Section. A more detailed description of these devices is found in the ERD chapter. A recent review of spin transistor highlights the concepts and challenges of these devices.[127]. Recent work has demonstrated successful electrical injection, detection and manipulation of spin accumulation in Si using ferromagnetic metal / SiO2 tunnel barrier contacts at temperature to 500K, encouraging results for realization of Spin MOSFET operation at practical temperatures.[128]

4.2.2.2. ATOMIC SWITCH MATERIALS

The atomic switch operates with oxidation /reduction processes where a metal atom moves to form a bridge between two different electrodes. The materials include a metal such as Cu and sulfur.129 Recently, STM has been used to characterize Ag filament growth in an RbAg4I5 solid thin film electrolyte which determined that the Ag critical nucleus formation was the limiting step130. More research is needed to determine the study these mechanism at an atomic scale and determine its potential reliability; however, the mechanisms appear to be similar to those in the Redox memory.

4.2.2.3. MOTT FET MATERIALS

The Mott FET is based on a metal-insulator (MI) transition caused by the gate field inducing charge in the Mott insulator, as described in the ERD Logic section. MOSFET structures have been fabricated with VO_2 that exhibit gated metal insulator transition switching[131]; however, details of the switching mechanism (electronic vs. structural) have not been resolved. Use of a electrolyte gate is able to induce significantly higher carrier concentrations in Mott insulators with lower voltages[132]. Phase transitions in $NdNiO_3$ from an insulator to a state that exhibits metallic conduction are observed upon hole doping. FET with the channel layer of $NdNiO_3$ showed the decrease in the phase transition temperature by as much as 40 K by the application of a gate voltage of 2.5 V[133,134]. These experimental results indicate that the decrease in the phase transition temperature was inversely proportional to the channel thickness, namely, carriers are uniformly induced by the electric field in the depth direction of the channel layer. This behavior is different from FETs using general semiconductors, where the field-induced carriers are localized at the top surface of the channel layer on the gate electrode side. This characteristic could become one of the solutions to solve the bottleneck of the semiconductor device miniaturization. Similar phenomena have been reported in transistors using VO_2[135]. Similarly, an insulator-metallic

transition in $CaMnO_3$[136] and recently $SmCoO_3$[137] thin film channel layer was induced by electron doping with both demonstrating a large change in resistance at room temperature with a low gate voltage. It has been proposed that the switching propagates from the charge accumulation region through the thickness of the thin film[138] in some materials. While the use of electrolyte gates has demonstrated clear carrier doping metal-insulator transitions, research is needed to identify solid state electrodes that can induce comparable carrier doping levels and room temperature metal insulator transitions.

4.2.2.4. FERROELECTRIC NEGATIVE CG MATERIALS

Ferroelectric oxides have been proposed as a gate oxide in field-effect transistor for steep subthreshold slope (SS)[139,140] . In a conventional FET, the intrinsic limit for the SS is of 60mV/dec. at room temperature, which puts a fundamental lower limit on the operating voltage and thus the power dissipation. For future generation of switches, low voltage operations will be of utmost importance[141,142]. In the original proposal[139], the replacement of the dielectric by a suitable thickness of a FE material should lead to a large increase of the capacitance thanks to the negative capacitance contribution of the ferroelectric (ideally the negative capacitance of the FE compensates exactly the positive capacitance of the stack). As a consequence, the drain current increases sharply under low voltage. Modeling performed for $SrBi_2Ta_2O_9$ as a ferroelectric gate oxide[143] predicts a reduction by ~150 mV of the operating voltage.

Experimentally, the first evidence of a SS smaller than 60 mV/dec. has been obtained on a metal-ferroelectric-metal-oxide gate stack using a ferroelectric polymer (P(VDF-TrFE))[144]. Minimum SS values of 46-58 mV/dec. are reported. Negative capacitance using a complex ferroelectric oxide has been reported in metal-insulating-ferroelectric-metal capacitors with $PbTiO_3/SrTiO_3$ bilayer[145]. No evidence for negative capacitance and steep SS has been so far demonstrated in a MOS structure using a ferroelectric oxide. Numerous questions remain to be addressed such as the suitability of the switching speed of the ferroelectric oxide for such devices and the effect of domains on the transistor response. Moreover, the integration of complex oxides directly on silicon is still very challenging[146] and the presence of a low-permittivity oxide at the interface between Si and the ferroelectric oxide is detrimental for the negative capacitance effect to be obtained with a reasonably thin ferroelectric layer.

The original device on Si also has some flaws, among which is electrical mismatch: while the ferroelectric capacitance does not vary a lot in the voltage region of interest, the Si capacitance does exhibit a large change when crossing from depletion to inversion region. Addition of a floating gate[147] provides a potential solution to this issue. . Furthermore, a modified device structure design[148] has been proposed to overcome these issues. The channel is a thin semiconductor on a conductor or on heavily doped silicon. The stack on top consists of a high-k oxide /metal/ ferroelectric stack. A non-hysteretic negative capacitance FET with sub-30mV/dec. swing over 6 orders of magnitude is simulated[148]. Note, however, that a floating gate is not desirable for a logic device.

4.2.3. NON-CHARGED BASED DEVICE MATERIALS

4.2.3.1. SPIN WAVE DEVICE MATERIALS

The key challenges in building a practical spin wave logic circuit are the efficient injection, detection, and modulation of spin waves in the wave guide. For this to be a viable option, efficient spin wave generators and modulators need to be integrated onto the spin wave guide, which requires an optimized interface between materials. At present, research on magnetic modulators is based on spin valves/magnetic tunnel junctions or multiferroic materials.[149, 150] This section will discuss material properties required for fabricating an efficient spin wave guide and spin wave modulator, based on multiferroics. The materials used in spin wave devices are described in Table ERM6.

Table ERM6 Spin Devices versus Materials

The fundamental physical property required for fabricating an optimized spin wave guide is to have high saturation magnetization (~10 KG), low Coercive field (tens of Oersteds), and long attenuation time (at least 0.5 ns). Currently, the most popular materials used for a spin wave bus are soft ferromagnetic metallic conducting films, such NiFe, CoFe, CoTaZr that are sputter deposited. These ferromagnetic metals possess high saturation magnetization (about 10kG) and Curie temperatures much higher than room temperature (Ni 627K, Fe 1043K, Co 1388K). Another advantage of using these materials is their compatibility with the silicon platform. Prototype spin wave devices are also fabricated using ferrite materials, such as Yttrium Iron Garnet (YIG). However, achieving nanometer thick and uniformly dense ferrite materials on silicon substrate is a challenge.

There are theoretical models demonstrating how to integrate a multiferroic structure onto a spin wave guide[150], but this integration has yet to be experimentally demonstrated. There are two major requirements for multiferroic materials: (i) Prominent 16magnetoelectric coupling (in V/cm Oe), and (ii) a fast switching time. Conducting and insulating materials are applicable to the spin wave based logic devices. They may be single phase multiferroics (e.g. $BiFeO_3$ 7 mV cm^{-1} Oe^{-1}) or composite (two phase) multiferroics comprising piezoelectric and ferromagnetic materials (e.g. PZT/$NiFe_2O_4$ (1,400 mV cm^{-1} Oe^{-1}), $CoFe_2O_4/BaTiO_3$ (50 mV cm^{-1} Oe^{-1}), PZT/Terfenol-D (4,800 mV cm^{-1} Oe^{-1}). Two-phase composite structures show 16magnetoelectric coefficients almost three orders of magnitude higher than those of single phase systems, while single-phase multiferroics switching speeds are intrinsically higher. Experimental studies have shown about 100ps (10GHz) switching times in single-phase multiferroics, and only 1 ns(1GHz) in the composite multiferroics.

The above approaches to material selection are postulated for fabricating an efficient spin wave bus or an interferometer based spin wave majority logic device.[150]

4.2.3.2. NANOMAGNETIC LOGIC MATERIALS

Magnetic cellular automata for logic is based on ferromagnetic islands arranged in cellular arrays, where local interconnectivity is provided by magnetic field interactions between neighboring magnetic dots.[151] In early work, 100nm diameter dots of 30-50nm thick islands were made of permalloy and supermalloy.[152] Since the state of one MCA is changed by the magnetic field generated by other local MCA, a critical challenge for this technology is to have reliable propagation of alignment between multiple MCAs. One option is to use magnetic materials with magnetocrystalline biaxial anisotropy. The biaxial anisotropy creates a metastable state for a rectangular nanomagnet, when it is polarized along the hard axis[153] and improves switching reliability. Material systems that exhibit such biaxial anisotropy include: epitaxial Co on single crystal Cu substrates[154], epitaxial Fe on GaAs[155], and epitaxial Co/Cu on Si.[155] The materials used in nanomagnetic logic are described in Table ERM6

To increase the magnetic flux density in the MCA, one option is to surround magnets with a different material to increase absolute permeability. This effect has been demonstrated in MRAMs, where enhanced permeability dielectrics had embedded magnetic nano-particles to increase a word/bit line's field strength without increasing current.[156] Proposed materials could increase the absolute permeability range by 2-to-30. Moreover, the fact that particle sizes are below the superparamagnetic limit should help ensure that magnetic the state is not unduly influenced.

While these approaches are based on magnetic islands with in-plane magnetization, utilization of layered stacks, e.g., cobalt-platinum multi-layers with magnetization perpendicular to the plane, is possible. A recent study demonstrated single-domain magnetically-coupled islands with perpendicular magnetization, fabricated with focused-ion-beam patterning of Co-Pt multilayers.[157]

4.2.3.3. EXCITONIC FET MATERIALS

Excitonic FETs can be constructed of alternate channel materials, but with different design. The parallel channel device separates electrons and holes and forms an exciton that is controlled by a gate electrode. Since this can be fabricated with alternate channel materials, it will not be discussed further in the ERM. A more detailed description of this device can be found in the ERD Logic Section.

4.2.3.4. BISFET MATERIALS

The Bilayer Pseudo-Spin FETs (BISFET) is proposed to be constructed of two layers of graphene separated by a thin insulating dielectric. The goal is for an excitonic collective superfluid of electrons to form in one graphene layer coupled to a collective superfluid of holes in the other graphene layer at room temperature. There is considerable debate over whether this coupling can occur at room temperatures. A more detailed description of this device can be found in the ERD Logic Section. The materials used in BISFET devices are described in Table ERM6.

4.2.3.5. SPIN TORQUE MAJORITY GATE MATERIALS

Spin torque majority gates consist of multiple spin devices connected to a common "free" spin layer. Two different spin devices are proposed for use in this logic, spin torque nano-oscillators (STNO) or magnetic tunnel junctions. These two devices use different effects in their operation and are described in more detail in the ERD Logic section. The materials used in spin torque majority gate devices are described in Table ERM6

The STNO majority gate operates by sending spin waves through the "free" layer and the wave frequency in the free layer is the same as the majority of the oscillators. These devices are constructed of ferromagnetic materials and thin nonmagnetic films. As these devices are reduced in size, it will be important to have low damping in the free layer.

Damping can be intrinsic to the material, but can be caused by surface roughness and damage in the surfaces of the free layer. Thus, it will be important to develop processes that minimize surface or sidewall damage and roughness. While it is important to have low damping, some is required to dissipate switching energy and enable fast switching.

In the magnetic tunnel junction device, the magnetic alignment of each input is transported through a tunnel barrier with spin polarized electrons providing the torque to the free layer. For these devices to be energy efficient, a small amount of tunneling current should produce the change of magnetization in the free layer. Thus, the tunnel barrier needs to have a very small amount of spin scattering and the damping in the "free" layer needs to be very small. Thus, as in the STNO device, the free layer needs to be a material with low damping, and be fabricated with low extrinsic damping. Furthermore, to enable scaling to very small feature sizes it is important to develop MTJs that operate with out of plane magnetization rather than the current in plane structures. This may require a new set of materials for these devices. Mn-Ga and MnAl are candidates, because they have low damping constant and large perpendicular magnetic anisotropy required to maintain a high thermal stability at reduced dimensions[158].

The critical current needed to switch the magnetization of the free layer in STT devices is typically of order 10^6-10^7 A/cm^2. This raises concerns over power consumption, local heating and dissipation, and electromigration, and there is keen interest in reducing this by orders of magnitude. Recent work has shown that one can use electric fields at the CoFeB/MgO interface to control the interface magnetocrystalline anisotropy and lower the energy barrier for magnetization reversal, reducing the spin-torque current required by two orders of magnitude[159]. Wang et al demonstrated reversible STT switching at a critical current of ~10^4 A cm^{-2} was observed in CoFeB/MgO/CoFeB MTJs with perpendicular anisotropy at 300K due to applied unipolar voltage pulses of 0.9-1.5V with a constant perpendicular bias magnetic field of 55 Oe[159]. A very different approach was used in FeCo/MgO/Fe MTJ structures[160]. Voltage pulses of selected duration enabled coherent precessional magnetization reversal with zero STT current, although a constant applied perpendicular magnetic field ~ 700 Oe was required. Similar results were reported by Kanai et al with a smaller applied field of 230 Oe in CoFeB/MgO/CoFeB MTJs[161]. These results represent significant progress in voltage controlled switching of the magnetic state in common MTJ structures.

4.2.3.6. ALL SPIN LOGIC MATERIALS

All spin logic consists of magnetic or spin devices that communicate their state to other devices through the transmission of spin waves through magnetic interconnects. For this to be scalable to small geometries, the magnetic material will need to have low intrinsic damping and be processed to produce interconnects with low roughness and low damage at surfaces and interfaces. More details about all spin logic can be found in the ERD Logic section. The materials used in all spin logic devices are described in Table ERM6

4.3. SPIN MATERIALS

A number of spin based devices are being evaluated in the Emerging Research Devices Chapter for Memory and Logic applications. In these devices, electron spin orientation is employed to represent information by either using an individual spin or a collection of spins in a magnet. The operation of these devices depends on nanometer scale material properties and multiple materials will be needed to enable these devices. A few of the basic functions required for most devices are 1) Electrical signal to spin conversion, 2) spin state storage, 3) spin transport, 4) electric or magnetic field induced spin modifications, and 5) spin state to electrical signal conversion. Materials that support these functions need to operate up to ~400ºK. These functions may be performed in a single material, at an interface, or in a combination of coupled materials and will need to operate in nanometer scale structures. These spin-based materials, along with their critical properties and challenges, are listed in Table ERM7.

Table ERM7 Spin Material Properties

4.3.1. SPIN MATERIAL CHALLENGES

The key material challenges for the realization of a device are: (1) reproducible synthesis of semiconducting magnetic materials with higher Curie temperature, i.e., Tc > 400 K and high remnant magnetization, (2) materials or structures with high coupling of electrical potential to magnetic alignment or spin alignment, (3) compatibility of these materials with CMOS processing, and (4) metrology to characterize spin and domain physics. A more detailed list of spin metrology needs is included in the ERM Metrology Section.

4.3.2. SPIN MATERIAL PROPERTIES

The set of critical properties for different spintronics materials, Table ERM7, will depend on the specific device applications, as discussed in the ERD Chapter. Within the context of evaluating progress in fabricating a semiconductor based or an all metallic spin device (as in the ERD), this section focuses on materials that exhibit the following physical phenomenon: (1) Spin wave propagation and modulation for Bus and logic, (2) nanomagnetic logic (3) the field effects of spin polarized electrons and holes for memory and logic. Thus, this section sequentially focuses on the following materials and their properties.

Dilute Magnetic Semiconductors
- Ferromagnetic transition temperature (T_C)
- Size dependence of T_C – Nano materials
- Wide band gap magnetic doped oxides and nitrides
- Group III-V and Group IV

Spin Injection/detection Materials

Spin Tunnel Barriers

Semiconductors and Nanostructures

Materials for Spin Wave Spintronics devices

Materials for Nanomagnetic logic

4.3.3. DILUTE MAGNETIC SEMICONDUCTORS

The potential value of dilute magnetic semiconductors, also known as ferromagnetic semiconductors, is that the magnetism can be turned on or off by changing the carrier concentration in the material. The primary constraint in using Ga,Mn)As, is that its highest ferromagnetic transition temperature, with verified carrier mediated exchange achieved to date (Tc=200°K)[162], is still well below room temperature and no significant progress has been reported since 2011. Research is needed to identify alloys compatible with semiconductor technology, having Curie temperatures above 400ºK, high remnant magnetization, and carrier mediated exchange. A more detailed discussion on this is included in the 2009 ITRS ERM Chapter.

4.3.4. SPIN INJECTION MATERIALS

The purpose of the spin injection material is to inject a highly spin polarized current into a semiconductor or other material. This can be accomplished either through high intrinsic spin polarization, or band symmetry matching with the adjacent semiconductor and/or tunnel barrier, as discussed in "Spin Tunnel Barriers."

The material to be used for a spin injecting contact should have several key attributes.

(a) It must be ferromagnetic, with a Curie temperature of over 400ºK;

(b) It must have significant easy axis remnant magnetization, i.e., zero field magnetization, of at least 50% of the saturation magnetization;

(c) Provide high spin polarization of the injected current, producing high spin polarization in the semiconductor; and

(d) Be thermally stable against intermixing with adjacent layers, and degradation of its FM properties with processing.

Requirements (a) and (b) provide the non-volatile reprogrammable characteristics, which are highly desirable for applications such as field programmable gate arrays, logic elements, or memory. In general, the spin injection contact material needs to be selected and tailored for a particular semiconductor or tunnel barrier.

Three broad families of materials could be used for polarized spin injection, ferromagnetic metals, half metals, and ferromagnetic semiconductors, but each has different challenges. A fourth class of materials which exhibits very large spin Hall effects has recently emerged and offers potential use for spin injection.

Ferromagnetic metals (FMMs)—Traditional FMMs such as Fe, Co, Ni and alloys are well-known to the magnetic recording industry and readily meet criteria (a) and (b) above. Because of the large conductivity mismatch between a FMM and a semiconductor, an intervening tunnel barrier is required to enable efficient spin injection. This may take the form of a tailored reverse-biased Schottky contact or a discrete metal oxide layer (e.g., Al_2O_3, MgO, etc.). Several FMMs

have been shown to meet criteria (c) for selected semiconductors and/or tunnel barriers. These materials are described in more detail in the 2009 ITRS ERM Chapter.

Half Metals—Half metals are characterized by the absence of occupied states near the Fermi energy for one spin channel, so that they are 100% polarized, making them very attractive as spin contacts. They generally meet criteria (a) and (b). In principle, such a 100% spin polarized metal does not require a tunnel barrier contact to alleviate the conductivity mismatch with a semiconductor. However, their polarization is highly sensitive to defects (a relatively low density of bulk defects reduces their polarization very rapidly), so these materials exhibit spin polarizations ~ 50%, typical of other FM metals at room temperature to 400ºK. In addition, defects associated with the semiconductor interface also appear to severely suppress the ideal spin polarization. Only modest electrical spin injection into a semiconductor (GaAs) has been reported to date[163,164] and, thus, half metals have not yet been demonstrated to meet criterion (c). Criterion (d) will likely pose significant challenges, although a few carefully tailored systems may be viable.

Ferromagnetic Semiconductors (FMS)—FMS are materials that are simultaneously semiconducting and ferromagnetic. As semiconductors, there is no issue of conductivity mismatch, and device design follows the standard principles of semiconductor band gap engineering. They can readily be grown epitaxially on other semiconductors, and incorporated into complex heterostructures, unlike most metals. FMS generally have Curie temperatures well below room temperature ~200ºK), as noted in the section under "Ferromagnetic Semiconductors." Therefore, they fail criterion (a). There are a few notable exceptions which are currently being investigated as discussed before.

A fourth class of spin injection material has recently emerged based on the spin Hall effect (SHE), in which an unpolarized charge current in a non-magnetic material generates an orthogonal pure spin current due to the spin-orbit interaction. The defining metric for such a material is the spin Hall angle, $\theta_{SH} = J_s/J_e$, where J_s and J_e are the spin and charge currents, respectively. Although the SHE has been known for many years[165] , it was too small an effect to be considered technologically useful. However, recent work discovered giant spin Hall effects in thin films of Ta[166] and W[167] sufficient to enable spin-torque switching and spin-torque induced magnetic oscillations of adjacent CoFeB layers at 300K[168]. The value $\theta_{SH} = 0.33$ in tungsten approaches the intrinsic spin polarization of the charge current in many FM metals such as Fe (~ 40%). Although spin Hall materials such as Ta and W lack attributes (a) and (b) noted above, they generate a pure spin current rather than a spin polarized charge current which may prove useful in some spintronic circuit applications. Relatively large $\theta_{SH} > 0.2$ was observed also in impurity doped Cu [169,170], and SHE-STT switching of adjacent CoFeB layer has recently been reported[171].

4.3.5. SPIN TUNNEL BARRIERS

The large difference in conductivity between a ferromagnetic (FM) metal and a semiconductor precludes efficient spin injection, since the semiconductor accepts spin-up and spin-down carriers with equal probability, but exhibits very low conductivity compared to the metal. Thus equal numbers of spin-up and spin-down electrons are transferred to the semiconductor, and the resulting polarization is essentially zero regardless of the spin polarization of the FM metal. To solve this "conductivity mismatch" issue, the interface resistance must be the largest in the series to control current flow, and also provide some spin selectivity. A tunnel barrier fulfills both criteria.[172,173]

Fabrication of ultrathin and defect-free tunnel barriers is an ongoing challenge in materials science. Even a well-developed and widely utilized oxide such as SiO_2 is known to have defects and trapped or mobile charge, which limit both charge and spin-based performance. An ideal spin tunnel barrier should exhibit the following key material characteristics: high spin filtering or injection efficiency, a uniform and planar habit with well-controlled thickness, minimal defect/trapped charge density, a low resistance–area product for minimal power consumption, and compatibility with both the ferromagnetic metal and the semiconductor of choice, ensuring minimal diffusion to/from the surrounding materials at the temperatures required for device processing.

Crystalline MgO has been used successfully as a tunnel barrier in CoFeB/MgO/CoFeB heterostructures with a TMR(300K) ratio of 350% with a 400C anneal and a TMR(300K) ratio of 600% with a 600°C anneal[174]. The symmetry of the Δ_1 propagating state in single crystal MgO (001) matches that of the majority spin band in FM metals such as Fe. Therefore, majority spins are readily transmitted in Fe/MgO contacts, while minority spins are blocked. In principle, this results in a higher spin polarization of the injected current than produced by the Fe contact alone. Such band symmetry assisted spin injection may be a promising avenue for highly polarized contacts, complementing the Heusler alloy approach. MgO is currently the industry standard spin tunnel barrier material used in hard disk read heads and MRAM, including spin-transfer torque MRAM. In such commercial applications, the actual TMR is typically 100%, and probably limited by the partial crystallinity (due to the thermal budget) and oxygen interdiffusion at the interfaces[175].

Graphene is predicted to be an effective spin tunnel barrier[176] and produce TMR values in Co/Gr/Co and Ni/Gr/Ni which exceed those realized for Fe/MgO/Fe. This arises because only one spin band of the FM metal crosses the Fermi energy of the heterostructure and is transmitted, while the other spin band is blocked, leading to near perfect spin filtering for several layers (3-5) of graphene. Calculations show that the spin filtering is quite insensitive to amounts of interface roughness and disorder which drastically influence the spin-filtering properties of conventional magnetic tunnel junctions or interfaces between transition metals and semiconductors. Recent experiment has confirmed that even single layer graphene serves as a spin tunnel barrier in a Co/Gr/NiFe MTJ structure[177] although the TMR(300K) was small because a single graphene layer does not produce sufficient spin filtering. Other experimental work has shown that single layer graphene serves as a spin tunnel barrier to solve the conductivity mismatch between a FM metal and a semiconductor, enabling efficient spin injection into Si at 300K while simultaneously reducing the contact resistance by three orders of magnitude relative to an SiO2 tunnel barrier[178].

Graphene's planar character provides excellent control over barrier morphology, and with other naturally layered compounds such as h-BN, may introduce a new paradigm in tunnel barrier technology. Graphene's inert chemical nature minimizes interfacial reaction and interdiffusion, ensuring well-defined interfaces and robustness for thermal processing, and preventing coupling through pinholes. The current challenge is to fabricate well-ordered graphene films 3-5 layers thick for optimal spin filtering. Initial work suggests that this can be accomplished by CVD type growth directly on a Ni, Fe or Co surface.

4.3.6. SPIN TRANSPORT IN SEMICONDUCTORS AND THEIR NANOSTRUCTURES

For several devices, once the spin is injected into a semiconductor, it is important that the spin remain coherent in the time that transport, manipulation, and detection occur. Most experimental work on spin transport in semiconductors typically focuses on III-V direct gap materials, such as GaAs, because polarization dependent optical absorption / emission spectroscopies provides easy, direct and quantitative insight into carrier spin polarization and dynamics[179]. The long spin lifetimes expected for the low-Z (weak spin orbit) Group IV semiconductors make spin angular momentum especially attractive. Spin transport, via electrical injection and detection of spin polarized carriers from FM metal contacts (e.g., Fe, CoFe) into Si, has been demonstrated[180, 181, 182], with reported electron spin polarizations of 30% or more. Magnetic field induced coherent precession of the pure spin current and spin polarized charge current has been demonstrated in lateral[182] and vertical[175] transport geometries, respectively. These results collectively show that information can be fed in, processed and read out using spin rather than charge as the state variable. However, these results have previously been limited to low temperature, due to thermal noise generated by the contact resistance. Options to reduce this contact resistance, by controlling the depletion width in the Si, have been identified.[183] Recent work has demonstrated successful electrical injection, detection and manipulation of spin accumulation in Si using ferromagnetic metal / SiO2 tunnel barrier contacts at temperature to 500K, easily exceeding the operating temperature requirements for commercial application.[184]

Graphene exhibits *spin* transport characteristics that surpass those of any other semiconductor studied to date, demonstrating large magnetoresistance (MR) at room temperature.[185] Such large MR has not been seen in any other semiconductor materials or nanostructures, including InAs to GaN to Si. Recent work reports room temperature spin lifetimes and diffusion lengths of 2.7 ns and 7 um, respectively, the highest obtained for single layer graphene on SiO_2[186]. However, graphene faces other practical challenges, primarily the lack of a technologically relevant band gap and limited control over doping.

For low dimensional materials, CNTs are attractive as spin transport materials because their low dimensionality results in a suppression of certain spin orbit scattering mechanisms at higher temperatures (>70K), leading to longer spin lifetimes. Limited successes have been reported for spin injection into CNTs from magnetic metal contacts at low temperature; however, developing reliable contacts and obtaining reproducible results continue to be challenges. At present, for nanowires of any semiconductor, there are limited results for spin injection and transport, though several experimental groups are currently working in this area.[187]

4.3.7. MAGNETOELECTRIC COUPLING (MULTIFERROICS)

This is covered in Complex Metal Oxides (below)

4.3.8. INTERFACES AND HETEROINTERFACES

All of the devices fabricated with these materials depend on having high quality interfaces, and the important properties depend on the application. For spin tunnel barriers, the interface must not scatter the majority spin carriers. For spin transport, the interfaces must have spin specular reflections that don't cause decoherence.

4.4. CONTACT RESISTANCE

As devices are scaled to smaller dimensions, contact resistance has a larger relative impact on device performance. The contact resistance is determined in part by the energy alignment between the metal Fermi level and the semiconductor bandgap, determining if the contact is of Schottky or Ohmic type. At metal/semiconductor interfaces, Fermi level pinning usually leads to a Schottky barrier; in the past, it was possible to reduce the contact resistance by highly doping the semiconductor to reduce the thickness of the potential barrier at the metal semiconductor interface; however, this is not possible in many nanoscale devices. In addition to this, metal contacts often form an alloy with the semiconductor and this would consume considerable amounts of a multigate FET such as a FinFETs. Furthermore, nanomaterial based devices such as carbon nanotube, graphene, or other 2D nanomaterials the only options are to reduce the barrier height, since the material is extremely thin. The emerging approaches to reducing the contact resistance include introducing a thin tunnel barrier at the interface or introducing a dipole or charge at the interface. For ultralow resistance contacts, it is ideal to have the Fermi level of the metal aligned with the Fermi level of the semiconductor majority carriers; however, Fermi level pinning often results in a Schottky barrier at the interface. Thus, it is important to eliminate Fermi level pinning that produces a high Schottky barrier and increases contact resistance. The interface material that doesn't pin the Fermi level may produce a barrier to carrier transport between the metal and semiconductor, so it must be as thin as possible. Furthermore, introducing dipoles or fixed charge in the barrier layer may be able to adjust the offsets between the metal and semiconductors.

4.4.1. TUNNEL BARRIER TO REDUCE CONTACT SCHOTTKY BARRIER

The deposition of metal contacts onto semiconductors delivers energy to the surface atoms as the metal condenses, which can result in breaking of semiconductor bonds. This breaking of bonds can introduce defect levels at the interface that can pin the Fermi level at the energy level of the defects. This can also occur with the deposition or growth of oxides on a surface, so it is critical to deposit an interface layer that does not pin the Fermi level. Often identifying materials and processes that don't introduce detrimental pinning levels at the semiconductor interface must be experimentally determined. For silicon, SiO_2 produces an unpinned interface, For Ge and some III-V materials, Al_2O_3 or AlO_x can, depending on the deposition technique, produce unpinned Fermi levels at these semiconductor interfaces.

4.4.2. DIELECTRIC DIPOLE TO REDUCE SCHOTTKY BARRIER HEIGHT

Once a non-pinning interface material has been identified, a dipole can be introduced in the barrier material by depositing a thin dielectric that has a low barrier to carrier transport. When two materials with different work functions are placed in contact, a dipole can form at the interface. Introduction of a 1nm thick AlO_x/SiO_x layer in Si contacts reduced the Schottky barrier height by ~100meV in a FinFET which reduced parasitic S/D resistance by 25%[188]. To achieve low contact resistance, the barrier to carriers must be as low as possible and as thin as possible.

4.4.3. INTRODUCING FIXED CHARGE IN THE INTERFACIAL LAYER

Introducing positive fixed charge in the interfacial layer can induce negative carriers at the semiconductor interface which can change the alignment of the semiconductor bands to the metal. This can be used to fine tune barrier height between the metal and the semiconductor.

4.5. COMPLEX METAL OXIDE MATERIALS, INTERFACES, AND SUPERLATTICES

Complex oxides exhibit an extremely wide variety of electrical, magnetic and optical properties, including superconductivity, piezoelectricity, ferroelectricity, pyroelectricity, ferromagnetism and multiferroicity. Most complex oxides are strongly correlated electronic systems[189,190]. Their properties result from strong interactions between spin, charge, orbital and lattice. Many of them have a perovskite-type structure. The several competing states give rise to complex phenomena and rich phase diagrams. Typical examples are the high-T_c superconductivity in cuprates[191,192] or the colossal magnetoresistivity in manganites[193-195]. Due to the strong correlations in these systems, a small external perturbation leads to a large electrical, magnetic or mechanical response. Furthermore, interfaces and heterointerfaces in these complex oxides can lead to new properties arising from surface, electronic or orbital reconstructions[192-194]. Oxide heterostructures are artificial materials that can be engineered to tune the properties or even obtain completely new properties [196-203]. Recent examples include the superconductivity at the interface between the two insulators $SrTiO_3$ and $LaAlO_3$ or the improper ferroelectricity arising from the combination of a proper ferroelectric and an insulator. These properties may be exploited for memory and logic devices and to add new functionalities in silicon electronics.[204-207]

A major challenge is to control the properties with an external field, for example, modulating and controlling magnetism or conductivity with an electric field. In the case that the material which shows a metal – insulator transition is used as

the channel material in a FET structure, the transition can be controlled by the gate voltage. Actually, in an electrolyte-gated FET structure, with $NdNiO_3$ as the channel material, the metal–insulator transition temperature was reduced by 40K[208] with a gate voltage of -2.5V. With increasing hole concentration through the application of the negative gate voltage, the conductivity changed by one order of magnitude. A critical question is whether oxygen vacancies may also diffuse with high gate voltage and change the electronic property of the channel material. The investigation of field effect transistors in these materials is important to elucidate the fundamental understanding of the metal – insulator transition in a strongly correlated electron material.[208,209]

4.5.1. COMPLEX OXIDES FOR SPINTRONICS

Spintronics is a domain where complex oxides are of particular interest with the possible coupling of magnetic and electric properties, so that magnetic readable storage media could be written electrically.

4.5.1.1. MAGNETIC AND MAGNETORESISTIVE OXIDES

Among the magnetic oxides of interest for devices, half-metallic compounds such as the perovskite manganite $La_{0.7}Sr_{0.3}MnO_3$ are of particular interest. It exhibits nearly 100% spin polarization below its Curie temperature of 360K. When epitaxially grown, it is therefore an attractive ferromagnetic electrode for spintronics devices, such as magnetic tunnel junctions or spin filters. Progresses in the growth of this oxide and control of its interfaces have pushed down to ~2 unit cells the limit of the critical thickness when a surface "dead layer" dominates with a lower Tc and lower spin polarization. However, since the Curie temperature is close to room temperature, the half metallicity is strongly reduced at room temperature. Besides its magnetic properties, it is also used as a conducting electrode allowing the epitaxial growth of another functional complex oxide on top of it. It has been used for example to act as the base in a perovskite heteroepitaxial metal-base transistor functioning at room temperature[210] or as a conducting electrode in ferroelectric tunnel junctions[211].

Double perovskite manganites such as Sr_2FeMoO_6 are also half metallic with a higher Curie temperature (~400K). However, the magnetism is strongly related to the ordering of the B-site cations (e.g. Fe and Mo ions), which is challenging to control. Recently, several double perovskites have been studied such as La_2CrFeO_6, $SrLaVMoO_6$, Ba_2FeMoO_6 or La_2VMnO_6 [212-217]. Research efforts should be focused on the control of the growth of these materials and on the search for new magnetic oxides with high-Curie temperature and half metallicity.

Writing information using a magnetic field requires locally large magnetic field or currents, which has drawbacks for power dissipation and scaling-down capabilities. Magnetoelectric multiferroics offer the ability to electrically-control magnetic data storage or logic devices.

4.5.1.2. MAGNETOELECTRIC COUPLING USING MULTIFERROICS

Multiferroic compounds of interest are both ferroelectric (FE) and ferromagnetic (FM) or antiferromagnetic (AFM).[218-221] If the electric and magnetic orders are coupled (22magnetoelectric effect), it opens up the possibility to have a mutual control of the properties: controlling a polarization by a magnetic field or controlling a magnetization by an electric field.

Multiferroic compounds present at least two ferroic orders[220,222-224]. Among them, ferroelectric (FE) and magnetic compounds (ferromagnetic FM or antiferromagnetic AFM) are of particular interest for 22magnetoelectric and spintronics. Indeed, if the electric and magnetic orders are coupled through 22magnetoelectric effect, it opens up the possibility to have a mutual control of the properties: controlling a polarization by a magnetic field or controlling a magnetization by an electric field. Such perspective has spurred the search for new multiferroic and magnetoelectric materials[225]. Only recently has a single-phase FE-FM compound at room temperature been reported[226]. The most studied multiferroic compound is $BiFeO_3$ which is FE and AFM at room temperature[227]. Electric control of antiferromagnetism in $BiFeO_3$ has been demonstrated in thin films[228]. The electrical control of a ferromagnetic film can thus be realized using exchange bias coupling, which couples AFM and FE orders at the interface of a bilayer. $BiFeO_3$ has been used to electrically control locally the magnetization in a ferromagnetic thin film layer of $Co_{0.9}Fe_{0.1}$ and in permalloy at room temperature[229,230]. In this structure, the magnetic orientation of the magnetic thin films are coupled to the antiferromagnetic orientation in the $BiFeO_3$ which is coupled to the ferroelectric orientation. Thus, changing the ferroelectric polarization changes the magnetic polarization of the thin magnetic film.

In spintronics, the ferromagnetic and insulating characters of a multiferroic film such as $BiMnO_3$ can be exploited to design spin filters[231].

While ferroelectric tunnel junctions and ferromagnetic tunnel junctions have both been proven to have a great potential for nonvolatile memory applications, the dual ferroelectric and magnetic characters of an insulating barrier can be exploited to create four non-volatile states[232,233]. Spin control can be achieved by selecting the spin direction of the tunneling electrons by electrical pulses that trigger the ferroelectric polarization switching in the tunnel barrier[234].

In addition to spintronics applications the complex oxide $BiFeO_3$ exhibit also promising properties for piezoelectric effects, photoconduction or photovoltaic effects and for spin-wave generation, conversion and control, which opens up the perspective of combining various functionalities (magnetic, electric, optical and mechanical) in future devices[235,236] .

4.5.2. METAL OXIDE HETEROINTERFACES AND SUPERLATTICES

Complex metal oxide heterostructures and heterointerfaces often have new properties that are not exhibited in the individual materials[237-239]. Like in semiconductor heterostructures, interfaces in oxide heterostructures play a major role and "are the devices"[240,241]. Forming interfaces between two band insulators, LaAlO3 and SrTiO3 may, for example, lead to highly conducting n-type interface (LaO/TiO2) while a p-type one (AlO2/SrO) is insulating[242]. Conducting interfaces between insulating oxides have been also found in several other systems such as LaTiO3/SrTiO3, KTaO3/SrTiO3, LaVO3/SrTiO3 or La0.5Ca0.5MnO3/CaMnO3. The interface between SrTiO3 and LaAlO3 has been particularly studied in the past years. The properties of the two-dimensional sheet of mobile electrons that is formed at the TiO2-terminated SrTiO3 / LaAlO3 interface differ from those of a two-dimensional electron gas as created at conventional semiconductor interfaces (such as GaAs / AlxGa1-xAs) and can be described as a two-dimensional electron liquid (2DEL)[243]. The mechanism that is at the origin of this 2DEL is still debated (polar catastrophe or doping at the interface via, for example, oxygen vacancies or cationic interdiffusion). A negative electronic compressibility has been evidenced from capacitors measurements resulting in an enhanced capacitance of the device[244] and confirmed by Kelvin probe microscopy[245]. Field-effect devices have been demonstrated utilizing the conducting n-type interface as drain-source channel and the LaAlO3 insulating layer as the gate oxide, with gate voltage below 1V and operation temperature up to 100°C[246]. While most studied heterostructures are grown on oxide substrates, it has been shown that a two-dimensional electron gas can also be created at an oxide interface on silicon[247], which may have strong technological impact[248].

Other properties can also be induced at interfaces such as ferromagnetism between antiferromagnetic insulators or high-Tc superconductivity between metallic and insulating cuprates. Orbital reconstruction provides an opportunity to engineer the bonding at the interface and thus modify its properties. Interfaces in superlattices can also change the nature of the coupling between competing instabilities and produce new properties such as in ferroelectric systems[249, 250].

To achieve novel properties in oxide heterointerfaces, the interface must be abrupt and the films adequately thick on each side of the interface. These heterointerface effects need to be further investigated to understand how they affect or limit resulting properties. The interface electronic structure is, for example, a strong function of surface boundary conditions: compositional effects as well as surface adsorbates can strongly influence the electronic conduction at the interface[251, 252].

The study of these heterointerfaces and superlattices is progressing with a combination of modeling and simulation and experimental expertise to control the interface properties and coupling. From an application standpoint, functional oxide interfaces promise great opportunities in the future. Engineering of these interfaces and structures could enable novel high κ dielectrics with low leakage for MOSFETs or structures that could induce large changes in carrier concentrations in Mott insulators for low voltage room temperature metal-insulator transition devices.

4.6. EMERGING CAPABILITIES FOR FUTURE ERD

4.6.1. RARE EARTH CHALCOGENIDES (PIEZORESISTIVE MATERIALS)

A novel logic 3-terminal switch named piezoelectronic transistor (PET) has been recently proposed[253]. The channel consists of a piezoresistive material, which undergoes a continuous reversible insulator to metal transition. The channel is in contact with a piezoelectric material. When a gate voltage is applied to the piezoelectric material, its expansion results in compressing the piezoresistive material, which then becomes electrically conducting. With suitable high-coefficient piezoelectric materials such as the relaxor PMN-PT, low voltage operation can be obtained. Suitable channel materials exhibiting a pressure-induced metal-insulator transition can be found amongst rare earth chalcogenides. For this to be a viable technology, materials must have a large "on/off ratio" and a high change in resistance with pressure[254](piezoresistive gauge)[255].

Piezoresistance gauge: $\pi_p=(d \ln\rho/dp)$[254,255]

SmSe is reported to have π_p of -3.98 and an on/off ratio of 1100 and $(Sm_{1-x}Eu_x)S$[256] is reported to have π_p of -4.6 with an on/off ratio of 10^5. Modeling may be able to identify rare earth chalcogenide compositions with higher piezoresistive gauge[257] and high on/off ratio. In addition to these properties, piezoresistive materials must have properties that support repeated cycling without fatigue, etc.

4.6.2. DETERMINISTIC DOPING FOR ATOMIC CONTROL

One way to control the doping profile is by deterministic doping. Doping processes with atomic-scale placement and concentration control will enable tunable device performance characteristics and reduced device-to-device variations. A reduction in device noise enlarges the useable design space, circuit-level uniformity, and system performance. One positive outcome of ultimate doped transistors has been the demonstration that it is possible to tune electrical properties by controlling not an ensemble of dopants, but the placement of individual dopants[258]. Deterministic doping also refers to 3D nanopatterning and assembly methods that provide sufficient control of the composition and structure of doped interfaces and components to yield several orders of magnitude improvements in device-to-device performance variability. Candidate doping options must address the following: 1) atomic-scale control of dopants and massively parallel dopant delivery; 2) random dopant fluctuation in the active channel region, ultra shallow junctions in the source/drain region and abrupt transitions between the source/drain regions and the channel; 3) compatibility and integration with existing fabrication platforms; and 4) economics, which depends upon R&D and equipment costs, yield, and throughput.

Deterministic doping focuses on: 1) introducing single-dopant/few-dopants within the channel, as well as the source/drain regions, with placement accuracy of <<10nm; 2) activating the low number of deterministically introduced dopants effectively; 3) measuring and imaging single-dopant/few-dopants precisely; 4) exploring potential application opportunities through the atomistic control of materials, devices, and processes for better device performance. New metrologies can enable the characterization and realization of well-designed atomic-scale devices. The ability to accurately place dopants may also enable leveraging related emerging materials, devices, processes, and emerging device concepts, such as single-atom devices[259-261] and quantum computing devices based on manipulation of single dopant atomic states within Si[262,263] or diamond matrices, which might stimulate emerging research architectures.

4.6.2.1. SINGLE ION IMPLANTATION (SII)[264-270]

The feasibility of single ion implantation (SII) has been demonstrated, and SII is becoming a more and more important tool for enabling systematic studies of single-atom devices. This technology seeks to deposit a specified number of desired dopant ions at precise locations within the active region. Key objectives are to achieve single ion implantations with high spatial resolution and flexibility in dopant species, as well as 100% single dopant detection. Single ion implantation can be measured by the detection of secondary electrons, photons, electron-hole pairs, changes in transistor channel currents, or direct imaging changes in surface topography. Significant sources of dopant positioning errors, such as implantation spot size, straggling range, and diffusion and segregation during annealing, must be addressed for SII to be relevant for ultimately-scaled doped devices and related application opportunities, such as single-atom device development, systematic studies of dopant fluctuation effects and tests of quantum computer architectures (qubit readout, control and coupling) in relevant device platforms and substrates, e.g., silicon and diamond.

4.6.2.2. STM ATOM POSITIONING[271-275]

Atomic-scale fabrication platform has recently been established by dopant positioning with scanning tunneling microscope (STM) lithography. First single-donor transistors with narrowest, lowest resistance conducting Si wires and, atomically abrupt delta-doping for shallow S/D contacts have been fabricated with deterministic precision in both Si and Ge substrates. Fabrication of the first atomically-architected functional transistor, with all-epitaxial in-plane highly phosphorus-doped gates, has been demonstrated in silicon, using a combination of scanning probe microscopy, subsequent low-temperature activation and molecular beam epitaxy. The method provides high stability and full activation in a high density n-type systems and low-temperature process. The mechanism of single dopant incorporation has been identified. Potential benefits of the STM approach include: the ability to pattern with atomic precision in three dimensions; extremely high density, atomically planar and abrupt doping profiles; the investigation of novel device architectures; and applicability to other dopant sources/metals/organics. Although it is highly unlikely that this technique will warrant consideration as a potential solution for advanced device fabrication, the patterning accuracy of this

technique enables exploration of fundamental device limits and new functionality, including quantum computing and 3D device architectures.

4.6.2.3. SINGLE ATOM BASED DEVICES

4.6.2.3.1. QUANTUM TRANSPORT THROUGH A SINGLE ATOM[276-285]

Recent studies have demonstrated quantum transport through single donor/acceptor systems at 100 K, memory effects in coupled-donor systems, single-electron transport in multi-donor systems, donor-band formation, Metal-insulator transition from delocalized to localized states in the donor arrays, dopant-based applications such as turnstiles, memories, photonic devices, or nanoscale pn junctions. Deterministic doping methods promote the understandings of single-atom-based phenomena and the device development. These findings are creating a more foundational quantitative knowledgebase that will enable the design of future CMOS devices as they approach the ultimate single-atom transistor limit.

4.6.2.3.2. MODELING FOR SINGLE ATOM DEVICES[286-288]

Steady progress has been made in resolving individual discrete dopants in drift diffusion (DD), Monte Carlo (MC) and quantum transport simulation tools. The introduction of density gradient quantum corrections for electrons and holes has resolved the problem of artificial charge trapping in the Coulomb well of an ionized impurity's attractive potential in drift diffusion simulation. The introduction of ab-initio impurity scattering has allowed the characterization of transport variations related to individual dopant positions via 3D ensemble MC simulations. Full 3D quantum transport simulators are now readily available, using effective-mass and tight-binding Hamiltonians. These transport simulation tools are essential, especially when developing concepts for nanoelectronic devices that can benefit from the deterministic doping.

4.6.2.3.3. SINGLE ATOM FOR QUANTUM COMPUTING IN Si[289—292] AND DIAMOND[293-295]

The spin of the electron or the nucleus on a single dopant in silicon has been identified as an excellent system to encode and manipulate quantum information. Electrical detection and coherent manipulation of a single ^{31}P nuclear spin qubit has been finally demonstrated with fidelities higher than 99.8% by integrating single-shot readout of the electron spin with on-chip electron spin resonance. The nuclear spin coherence time was 60 milliseconds and one-qubit gate control fidelity exceeding 98%. Beyond silicon, the progress for single-color centers in diamond has continued significantly in the last 2 years. Direct room temperature optical access to single-electron spin control allowed great advances in the control of quantum states. The entanglement between two engineered single solid-state spin quantum bits (qubits) has been demonstrated at ambient conditions and the lifetime of electron spin entanglement was extended to milliseconds. This includes the demonstration of basic quantum logic, with a few qubits and transfer of quantum information from electrons to photons. These isolated spins may be located using confocal microscopy, initialized via optical pumping, and read out through spin-dependent photoluminescence measurements. However, while single-color centers can easily be found, the 1% to 60% yield appears to be energy-dependent.

4.6.3. TOPOLOGICAL INSULATORS

Topological insulators have been identified to have potential for high mobility and novel physics. 2D topological insulating states had been reported to exist at the edges of HgTe/HgCdTe wells[296] with quantum spin Hall states. Manipulation of the these states in Bi2Te3 nanoribbons determined a carrier mobility of 5800cm^2/V-s with a Fermi velocity of 3.7×10^5 m/s through these topological surface states. Also, 3D topological insulators have been reported in the bulk of Bi0.9Sb0.1 with angular resolved photoemission[298]. Recently, coupling between 2D and 3D topological insulating states have been identified to exist on the surface of a Bi(111) layer on Bi_2Te_3[299]. It has been proposed that these 2D-3D topological insulators could enable quantum computing[298, 300]. The ERM will monitor research in these materials and potential devices that could emerge.

5. LITHOGRAPHY MATERIALS

The future of scaled technologies depends upon emerging patterning materials (resist or self assembled) to enable extensible lithographic capabilities. New resist materials must concurrently exhibit higher resolution, higher sensitivity, reduced line edge roughness, and sufficient etch resistance to enable robust pattern transfer. 193nm and EUV extension materials are being developed which can improve LWR, pattern shrink materials, and topcoats for EUV to ameliorate issues with out-of-band optical flare and outgassing. Evolutionary approaches for enhancing positive, negative, and chemically amplified families of resists will continue to be evaluated. Leading process approaches to pitch division include multiple patterning (MP) and spacer patterning (SP) as options for extending 193nm immersion lithography. Alternate technologies are utilizing patterning materials to create guide patterns for directed self assembly, which can

include resists to form chemoepitaxy and graphoepitaxy guides, or directly patternable brushes and SAMs. Directed self-assembly (DSA) with block-copolymers or polymer pairs has made significant progress in characterizing sources of defect formation and in applications such as contact rectification, fin patterning, and pattern density multiplication. The advantages and challenges to these patterning materials are summarized in Table ERM8.

Table ERM8 Challenges for Lithography Materials

5.1. RESIST MATERIALS

Critical Resist Challenges: Advanced lithographic processes are challenged to simultaneously achieve high resolution (R), low line width roughness (L) and high sensitivity (S), with sub-60 nm resist thicknesses. Additionally, these resists must meet other requirements such as adhesion, etch resistance, and FAB material compatibility, outgassing (EUV), OOB sensitivity (EUV), leaching (193i) for example, for each specific exposure technology. Etch resistance is emerging as increasingly important as films become thinner.

The current set of extensible exposure technology potential solutions include: 1) ArF immersion lithography, which represents a significant increase in process complexity, such as multiple patterning with integrated spacer processes, with resist materials specifically optimized for positive tone development (PTD) using aqueous tetramethylammonium hydroxide (TMAH) and other resists specifically optimized for negative tone development (NTD) using organic developers; 2) EUV lithography; and 3) maskless lithography.[1-3] Advanced resist materials must be developed to satisfy the RLS requirements, as well as specific ArF dry, ArF immersion PTD or NTD, EUV or maskless lithographic technology requirements. For chemically amplified resist (ArF or EUV), diffusion control, without loss of throughput, is critical for resolution improvement. Emerging materials options include specifically designed polymers and photoacid generators (PAGs) that minimize diffusion blur, but maintain high polymer deprotection efficiency by the photoacid. Polymerically bound PAGs have been reported widely for EUV resist design, as this system offers slow diffusion for resolution enhancement and uniform PAG distribution for better LWR. It is also possible to apply polymeric PAGs in ArF resists for high volume manufacturing. New leaving group chemistries have been optimized for NTD processes.[4] New 193i resists are being optimized for the specific demands of spacer-on-resist double patterning, which include improved LWR, profile control, thermal flow temperatures, but can tolerate loss of dry etch resistance.[5-7] Photobase generator (PBG)[8] and photodestroyable base (PDB)[9,10].

For ArF immersion lithography, NTD resist development requires aggressive research to meet the demands of <22nm node technology. Key challenges include missing CH bond defects, film loss[11], etch resistance, pattern collapse and compatibility with the substrate.[12] Top coating and other alternative options for CD shrinkage, for example Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS) and DSA contact hole shrinkage.[13] Preliminary results indicate that the defectivity and CD uniformity of NTD resists can be significantly improved by optimizing the development process, [11,14,15] while the etch resistance can be compensated for by using a hard mask.[12] On the PTD side, achieving good process window of isolate line or post through direct lithographic image process is extremely difficult due to poor aerial image contrast at defocus by comparing with dense line. To solve this problem, a post-develop chemical trimming process and coating material have been developed. As a result, the process window of isolated line is greatly enhanced. This also serves as an alternative way of CD slimming to dry etch trim.[13] The major challenge of the chemical trimming process has been maintaining post –trim profile.[16]

ArF dry resists may be used in implant applications to replace KrF resists for the advanced nodes.[17] New resist materials must be developed to meet the projected resolution and reflectivity control requirements on topography, particularly for deep well and source drain type implant layers. Negative tone resists with TMAH developer and NTD resists with organic solvent developer can be useful for footing and scumming reduction[18].Another option which is particularly useful for implant applications is to combine either a PTD or NTD resist with a developable or photodevelopable antireflective coating (DBARC).[19-21] The imaging challenges in critical level implant are becoming so challenging that even implant directly through the BARC is now being strongly considered.[22]

EUVL lithography continues to be delayed primarily due to a lack of a powerful EUV source.[19] In spite of the delay there has been steady improvement in resists and ancillary EUV materials. Reasonably sensitive EUV PTD resists have been reported with imaging capability down to 16 nm hp lines and spaces and 20nm hp contact holes.[20] Slow PTD resists have been shown to resolve 13nm hp lines and spaces and 18nm hp contact holes. These results are achieved in a single exposure.[21] If we apply double patterning SADP process, 9nm hp can be achieved with PTD resist.[13] There has also been rapid improvement in EUV NTD resist technology with reasonably fast resists showing 20nm hp lines and spaces and 20nm isolated trench.[22] Molecular glass resists continue to be active with materials based on calixarenes, Noria, and fullerenes.[23-25] However, the molecular glass resists have not performed as well as polymeric resists so the smaller radius of gyration for molecular glass does not lead to higher resolution. Lastly, high resolution inorganic resists

from Inpria and Dow Corning seem to show extremely high resolution but are considered too slow for practical use.[22] Ober et al have reported good sensitivity in a HfO_2 nanoparticle resist but they don't have the resolution capability of the other inorganic resists.[26] Ober has reported on the resist working by a ligand exchange mechanism.[26] One of the options for resolution enhancement is wavelength reduction from 13.4 down to 6.7nm.[27,28] Since most organic materials increase transparency with smaller wavelength, dramatically change of resist platform is necessary for adequate absorbance in a resist less than 100nm resist thick. Resist film thicknesses may continue to shrink with feature size, in part, to avoid pattern collapse.[29,30] Below a critical thickness, the resist's mechanical and thermal properties change.[31-33] For example, the glass transition temperature of ultrathin multicomponent ArF and EUV resist films depends on the PAG/resist combination.[34] Also, line width roughness appears to increase with decreasing film thickness.[35,36] Future semiconductor processes might also require several different post processing methods to reduce serious pattern collapse and line width roughness at tighter pitch.[37,38] Several ancillary materials have been introduced to enhance the EUV resist process: topcoat for reducing outgassing and out-of-band radiation, underlayers to enhance sensitivity and pattern profile; surfactanated rinse for reducing pattern collapse, low surface tension developer and tetrabutyl ammonium hydroxide developer for reduced swelling.[39-41]

5.1.1. ArF Resist Improvements and Extension Options

The primary focus of resist development will continue to be the evolutionary design of positive chemically photoresists. However, the challenge of simultaneously achieving resolution, sensitivity, and line edge roughness remains daunting. Consequently, there has been a strong focus on the photopackage design, both the photoacid generators and now also including photoactive quencher base materials. Increase etch resistance needs are being explored through integration of 193 resists with novel spin-on-metal-containing hardmasks (SOMHM). Another strong focus has been on the further development of the NTD concept of 193i resists using organic developers.

5.1.2. ArF Photo Package Design

As the lithography CD continues to shrink, the optical contrast for dark field patterns becomes extremely poor. Efforts in the industry have been devoted to novel photo package designs to enhance resolution and further extend ArF immersion photolithography. New photo sensitive materials have also been introduced, such as photo-base generator (PBG) and photo-decomposable base (PDB). Wang etc. has developed a new negative tone image (NTI) process using a positive resist that comprises thermal-acid generator (TAG) and PBG.[8] In the exposed areas, PBG decomposes to generate a base which neutralizes the acid from TAG. The new resist has shown improved resolution over conventional negative tone resists, but the resolution is not comparable to PTD and NTD resists. The self-deprotection issue of the new resist has been improved by increasing the TAG base loading and the use of slower diffusive TAG. Chen has found that MEEF, LWR, CDU, and end-to-end top view profile can be improved by controlling the diffusion lengths of PAG and PDB.[9] Hallett-Tapley has published the design novel ionic carbamate photoacid/photobase generators. The activation of the PBG unit allowed for the patterning of two lines with one laser dose. It has been demonstrated that amine quencher additives are able to adjust the energy required to initiate dual tone behavior. A mechanism involving 4-nitrobenzyl radicals was proposed. Thin film patterning results are needed to demonstrate the prospect of this method.[10]

5.1.3. Spin-on-Metal-Hardmask, SOMHM

Use of a hardmask in certain layers of integrated circuit (IC) fabrication has become popular, owing to shrinking film thicknesses as the nodes became smaller and the excellent etch selectivity of the hardmask materials. [42] Among the different hardmask approaches in recent years, metal hardmasks such as TiN hardmask, are applied using chemical vapor deposition (CVD), onto a processed wafer. Amorphous carbon hardmask, applied through either CVD or a spin-on technique, and silicon hardmask (or silicon antireflective coating or SiARC) are among the conventional technologies in IC fabrication. The application of a spin-on, metal hardmask (SOMMH) is now gaining its attraction in the IC industry, in part due to an attempt to replace the CVD metal hardmask for cost reduction and for simplification of fabrication processes. SOMHM can also be applied in tone reversal process.[42] SOMHM has shown good shelf-life, high coating quality and excellent resist compatibility. Titanium, Zirconium,[10] Hafnium and Tungsten[43] are among the many SOMHM materials that are being intensively investigated. Novel underlayer stacks are also being developed to be included with the application of SOMHM.

5.1.4. Negative Tone Resist

Several ArF negative tone resist materials were developed to operate by a cross-linking or a polarity change mechanism.[44,45] Negative resists tend to perform better than positive tone resists with binary masks, but tend to respond less well to 6% phase-shift mask designs. They also tend to exhibit pattern bridging, when the aerial image has significant flare or when light is diffracted into dark areas (low κ_1). Research is needed to address these challenges. Negative resist has been extended to EUV.[46]

Noria-based chemically amplified molecular resists that contain photo-catalyzed crosslinkers have shown 20nm resolution and 3.2nm LER. Trade-offs have been observed between image contrast and structural swelling. The negative tone development process enables the printing of dark field features on wafer using bright field masks with a manufacturing capability for back-end-of-line processing. The performance advantage of NTD photoresist was found to be especially in a larger process window for dense and semi-dense contacts and the resolution and LWR of isolated trenches. [47] It has also been demonstrated that a single photoresist formulation is capable of printing both line/space and contact hole. New NTD resists that show better "g-parameter" also show evidence of improved DOF, CDU, circularity, overdose margin, sensitivity and resolution, and the inclusion of deprotection reactions enhancer has been effective in improving collapse margin.[48]

5.1.5. EUV CHALLENGES

5.1.5.1. SHOT NOISE 49

At the very low exposure doses desired for high throughput EUV lithography, stochastic variation becomes a significant issue in the image formation process. To address this challenge, research is needed in several key areas, i.e. to increase: EUV light absorption; secondary electron yields (SEYs), through polymer design; and finally electron capture efficiency of the secondary electrons by the PAG.[49] Papers have emerged that show the deleterious effect of shot noise on CDU and LWR.[50,51]

5.1.5.2. EUV LIGHT ABSORPTION [52,53]

Fluorine is the second row element on the periodic table with the highest absorption at 13.5 nm. In a lithographically useful series of fluorinated polymers, the highest practical EUV absorption is maximized at a value of about seven.[36] The extreme of maximum absorption is about 18.5 (impractical, PTFE), which for resist film of 40nm thickness would still have 50% transmittance. Much higher z elements can have a higher EUV absorption cross section than fluorine or oxygen. However, it can be chemically challenging to incorporate high z atoms into an effective EUV formulation (see the section on inorganic EUV resists). Increasing film density can play a big role by increasing the number of light absorbent atoms per unit volume. Recent papers have reported on attempts to increase the fluorine content in EUV resists.[53,54]

5.1.5.3. ACID AND ELECTRON BLUR

Shot noise and photoacid diffusion are intimately linked in governing resolution, photospeed, and LWR.[55] Multiple reports demonstrate and confirm that RLS variables can't be independently optimized.[56] The interdependence of these critical factors has been shown repeatedly in ArF and EUV lithography. In a chemically amplified system, may be impossible to overcome the inherent issues of the diffusion blur problem.[57] The diffusion of photoacid necessary to accomplish chemical amplification may fundamentally limit the achievable resolution, photospeed and LWR of these systems.

A stochastic resist model has been applied to estimate the acid diffusion length for a polymer bound PAG (PBP).[58] A PBP methacrylate resin currently under consideration showed an acid diffusion length of just 9.7nm. However for sub-20 nm lithography the acid diffusion length will probably need to be less than 6 nm, which may be attainable. The stochastic model methodology was used to estimate the electron blur, which represents the contribution from the electron motion relative to the acid blur, of the EUV resist exposure; and calculated a value of 2.5nm, a much lower value than reported by others.[58] Recent results for EUV PTD resists show reduced acid blur to 4.9nm.[20]

5.1.5.4. OUT OF BAND RADIATION

OOB is defined as unwanted radiation emitted from the EUV source that extends from 140 to 300nm.[59] Most resist platforms are extremely sensitive to OOB, and this appeared to correlate with the resist absorbance at the longer wavelength.[59] For example, PAGs containing the triphenyl sulfonium cation [TPS] have a very high absorption in the UV band, spanning 180-370 nm, which makes it particularly sensitive to OOB radiation. PAGs with poor absorption efficiency in the same deep-UV band region will decrease resist sensitivity to OOB.[52] OOB sensitivity is measured by comparing the resists exposure dose sensitivity at multiple wavelengths. Recent work on topcoats to reduce OOB have been shown to be very effective. However, the topcoats add process complexity, cost and a dose penalty.[39]

5.1.5.5. RESIST OUTGASSING

Some PAGs outgas extensively with EUV irradiation in a vacuum. For example, PAGs containing the TPS cation generate high levels of diphenyl sulfide.[60] Gaseous carbon containing photoproducts, especially unsaturated groups, can readily deposit on EUV optics and masks. As a result, new PAGs are being designed for EUV lithography that do not generate diphenyl sulfide and other gaseous byproducts that avoid optics coating issues.[52,60] The witness plate test has

been difficult to obtain so recently four global witness plate test centers were formed to increase data generation cycles. As a result, more learning has been achieved to understand resist contribution to carbon growth on the witness plate.[61]

5.1.5.6. CONTINUED IMPROVEMENT OF LOW DIFFUSION PTD RESIST SYSTEM

Research continues to design improved low acid diffusion systems such as Polymer-bound PAG (PBP) with the following improvements[62]: 1.) increased photon capture, via increased EUV absorption and film density; 2) decreased the OOB photon capture efficiency; 3.) optimized electron affinity of the matrix polymer to increase the secondary electron yield; 4.) increased acid generation efficiency, by tuning the electron PAG capture rate; 5.) improved PAG film homogeneity; and 6) decreased organic outgassing during exposure. Recent results indicate the ability to optimize these systems to very low diffusion lengths less than 5nm with optimal dose in the 15-30mj dose range. It is very difficult to meet the resolution and LWR targets at a 10mj dose.

5.1.6. NON-CA RESIST AND INORGANIC RESIST

Several groups have demonstrated excellent resolution demonstrated with non-CA resists.[63-74] High MW PMMA, which switches via a chain scission mechanism, has been shown to resolve 12 nm hp;. However, PMMA's 40 mJ/cm^{2}dose to size is too high for high volume EUV manufacturing applications.[67] Other non-CA resists with a chain scission mechanism can mitigate chemical blur induced by acid diffusion during post-exposure bake step commonly used in chemically amplified resist. Polycarbonate based non-CA resist consists of the unit providing etch resistance/high Tg and the other unit for degradation induced by EUV irradiation.[75,76] This non-CA resist could achieve 28.6 nm line CD on 50 nm lines/spaces mask at the dose of 104 mJ/cm^2. LER was about 5.2 nm. Since it is reported that roughness induced by mask was 3.5 nm of LER on patterned photoresist on the Sematech-Berkeley micro-field exposure tool[77], the LER observed is only 1.7 nm greater than that of mask induced roughness. The poly(olefin sulfone) backbone was designed to be highly sensitive to EUV radiation.[78] The related materials possessed high sensitivity towards degradation by EUV radiation (E_0 in the range 4 to 6 mJ/cm^2). EUV interference patterning has shown capability of resolving 30nm lines/spaces features. From the results of outgassing test, contamination thickness on witness sample test and carbonization rate on residual gas analysis increased as molecular weight of olefin unit with functional groups increases.[79,80] Current non-CA negative tone resists exhibit poor EUV efficiencies, and they require more than twelve times the minimum dose required for high volume manufacturing. Without significant enhancements in EUV source power, research is needed to improve the efficiency of radiation scission or crosslinking events for non-CA resists to satisfy projected EUV lithography requirements.

Inorganic approaches to non-CAR materials appear to hold a greater promise of achieving sensitivity and other goals. For example, electron-beam resists with Zr and Hf[68] have demonstrated sensitivities as low as 8 μC/cm^2, achieved 15-nm lines and 36-nm dense features at higher doses, with a line-width roughness of approximately 2 nm. These resists also exhibit high etch resistance (>7× that of thermal SiO_2) in reactive-plasma etching. The high absorption cross-section of these heavy atoms aids somewhat in reducing the photospeed. Low film thicknesses are possible because of the very high plasma etch resistance, and the high density (4.7 g/cm3, compared to about 1.2 g/cm^3 for poly 4-hydroxstyrene) is thought to decrease electron blur significantly. Zero hydrocarbon outgassing was observed due to the resist's inorganic nature. Work continues on improving resist sensitivity, shelf life, and resist integration.

5.1.7. HYBRID EUV APPROACHES

EUVL technology can leverage the extensive ArF lithography knowledgebase. Interlaced double pattern processing and spacer-based multiple patterning using EUV lithography would enable a variety of pitch doubling techniques.[81,82] EUV resists with negative-tone development are being investigated to take advantage of the improved aerial image NILS for the formation of contacts and certain other pattern features. Polarity reversal and organic solvent development approaches could be helpful for improved contact CD uniformity, and improvements in preventing pattern collapse. Combining EUV with self assembly materials could be a way to rectify LWR in EUV patterning. Alternatively, EUV could be used to form graphoepitaxially defined wells for DSA, or chemoepitaxially defined pre-patterns for DSA alignment[83]. Trefonas et al reported on a top-down/bottom-up approach using a film composed of pre-assembled cylindrical polymer brush architectures that can be patterned as negative-tone resists.[84] These approaches are still nascent, but they hold very strong promise for extending EUV to 11nm node and beyond.

5.1.8. RESIST SUMMARY

Several creative lithographic techniques are emerging which extend or broaden the applicability of the current 193nm immersion workhorse, plus continued development of new materials and approaches to best meet the different requirements for success in EUV and EBL technologies as the insertion point feature dimensions continue to shrink as they scale further. Frequency multiplication through multiple patterning, particularly using spacer technologies, has

emerged as a dominant process for pitch shrinking. However, multiple patterning also creates the need for additional lithographic 'cut masking steps', to create the breaks in the patterns to form feature shapes useful for linearized circuit design. The cut masking steps, especially for quad and higher frequency multiplication offers new lithographic opportunities for EUV, EBL and DSA to simplify the processing, as the alternative of forming the small cuts using 193i lithography would require an unduly number of additional process steps. These techniques will need new resist materials in order to meet various roadmap requirements. One or more breakthroughs in resist materials will be required in for each lithographic technique in order to concurrently achieve the required resolution, sensitivity, and LER. Additionally, etch resistance is becoming an increasingly important parameter to consider as resist film thicknesses continue to decline in step with scaling dimensions. New material designs of spin on hardmasks, containing either silicon or even higher etch resistant metal atoms, are being increasingly integrated with the resist film.

Presently, there are multiple organizations working on producing viable material approaches in order to enable each lithographic technique. Immersion 193nm with multiple patterning remains the current technique of choice for linearized dense pattern formation, with the knowledge that breakthrough emerging technologies would greatly facilitate both the lithographic patterning of cut masking levels and the formation complex logic circuitry.

5.2. DIRECTED SELF ASSEMBLY FOR LITHOGRAPHY EXTENSION

5.2.1. DSA PROGRESS

Due to progress in reducing defects in block copolymer (BCP) directed self-assembly (DSA), industry's interest in evaluating potential application of DSA to extending lithography has increased dramatically; however, significant challenges must be overcome for this to be adopted. DSA would need to be used with conventional lithography such as 193i or EUV to either improve feature size control or increase the density of features. In DSA, lithography is used to pattern guide features that induce block copolymer domains to phase separate into modified versions of their natural patterns and in alignment to the guide features. Depending on the designed volume fractions of the BCP domains, the domains can assemble in vertical structures either as lines or contacts provided that the bottom and top surfaces are neutral wetting to both domains (the surfaces do not attract one polymer domain more than the other). The guide patterns are either trenches on the surface of the wafer (graphoepitaxy) or chemical patterns that attract one of the polymers on a surface that is neutral to the other polymers (chemoepitaxy). Potential applications include contact rectification[85], fin patterning[86] for multi-gate structures, contact density multiplication and line density multiplication[87].

5.2.2. DSA CRITICAL CHALLENGES

For DSA to be adopted, a number of critical challenges must be overcome and capabilities developed. First of all, DSA must continue to improve defect density toward the ITRS requirement of $<0.01 cm^{-2}$. DSA must be able to meet overlay requirements for the application. Block copolymers must be identified that reproducibly assemble sub 10nm features and have high differential etch rates for development. In addition, new capabilities must be developed to support processing including neutral surfaces and hard mask materials to support etching. Furthermore, CAD capabilities need to be developed to translate a design pattern into the guide features that need to be patterned on the surface. As feature sizes continue to decrease DSA will need to move to higher χ materials, but there may be challenges in simultaneously achieving low defect density, short annealing times and required feature size. Furthermore, each of the polymers in high χ materials will have very different properties and it may be difficult to identify a material that provides a neutral surface to both polymer blocks.

5.2.3. DEFECT DENSITY

Although defects are inherent in self-assembly processes above absolute zero, the guide structures can make defect formation energetically unfavorable if the guide structures are commensurate with the natural polymer pitch. An unresolved issue is how much variability in the guide structures can be allowed before defect densities increase to unacceptable levels. Since the requirement will be that total defects for the masking layer be <0.01cm-2, this requires that the sum of defects in the hard mask, neutral layer guide pattern and DSA itself meet this requirement. Preliminary experiments indicated that DSA defects could be reduced to $< 26 cm^{-2}$, when particulate defects were subtracted[88]. In depth studies of DSA-process interactions, for chemoepitaxy pattern density multiplication, indicated that defects from previous layers in the process could produce defects in the pattern. It was found that the neutral layer could be significant in generating defects in self assembled films[89]; however, DSA was able to heal some defects in the pattern. It was also found that significant deviations in CDs from optimal commensurability could also produce defects[89], so this must be studied. It was found that improvements in materials purity and processing were able to eliminate many of the DSA pattern defects. Implementing effective process test wafer strategies accelerated the rate of defect reduction[90]. For pattern

density multiplication of cylinder structures with graphoepitaxy, optimization of the guide structure dimensions, separation and thickness were required to produce conditions that produce no detectable defect configurations[91].

Modeling of defect formation energetics for graphoepitaxy guided lamella formation (lines and spaces) indicates defects are unfavorable with correct commensurability, but the probability of defects increases as a function of both the number of line pitches per guide feature as well as the degree of incommensurability between the guide structure pitch L_g and the BCP pitch L_0 (when commensurate, $Lg = nL_0$, n = 1, 2, 3…)[92]. For a given pitch size and guide structure size, increasing polymer weight (χN) significantly increased excess free energy which could increase defect formation potential. Similar results are seen in both modeling and experimental data with graphoepitaxy guided surface-parallel cylinders forming line-space patterns[93]. Modeling of defect formation energies of lamella formation guided by chemoepitaxy indicates that defect formation becomes energetically unfavorable as the interaction strength between the surface and the polymer increases and that patterns that stretch the polymer from commensurability are less prone to defects than structures that compress the polymers[94]. These studies provide guidelines for ranges process control required for "zero" defect structures; however, this will depend on specific block copolymers employed and needs experimental validation, since other kinetic factors such as entanglement may affect defect formation. Both modeling studies indicate that polymer compression from either guide structure, polymer weight, or polydispersity increases the potential for defect formation than polymers in tension. Thus, designs that place polymers in slight tension may reduce the potential for defect formation due to process fluctuations or polymer weight or dispersity variations.

Metrology is needed to detect defects in DSA structures in both 3D, because self-assembled structures may have different morphologies below the surface. This requirement is described in more detail in the Metrology Section of the ERM.

5.2.4. OVERLAY CAPABILITY

The overlay capability of DSA is dependent on the positioning of the guide structure relative to the alignment target (in the previous pattern), variations in guide pattern shape (such as LER, etc.) and the ability of DSA to assemble in the guide pattern (assuming a perfect guide structure). The first two capabilities are controlled by the lithography tool and process capability; however, using DSA to assemble smaller features than lithography that meet requirements of that technology will require the litho tool to have more stringent alignment capabilities than for the technology node. Similarly, variations in the shape of the guide structure may need to be smaller than required by the technology node.

A fundamental question is what is the variation of alignment capability of a DSA feature relative to a perfect guide structure that is perfectly aligned. Studies of contact hole alignment, of a BCP with 40nm pitch, to the graphoepitaxy guide feature centroid determined that deviation of the contact hole was ~1nm ($1\sigma_x$, $1\sigma_y$)[95]. Studies of contact holes in rectangular graphoepitaxy trenches determined that the variability of contact hole placement in the narrow trench dimension (4 contact rows with a pitch of 29nm) was ~4.4nm (3σ) for contacts at the edge of the trench, while it was ~3nm(3σ) for contact holes in the middle[96]. It was proposed that the higher variability of contact hole alignment at the edges of the trench was caused by LER being propagated to these contacts. It was proposed that variability of contact hole position relative to the target position could be improved with better annealing or chemoepitaxy; however, this is yet to be demonstrated. If we assume that total overlay is the geometric mean of the three factors (tool overlay, LER, and DSA alignment), with litho tool overlay and LER are each 10% of ½ pitch, DSA position variation(3σ) would need to be ~7% of the pitch. If the litho tools are capable of tighter overlay, this would slightly relax the DSA alignment requirement; however this would not be dramatic. The other option would be to find creative approaches to improve overlay from previous patterns, such as chemical markers or physical markers that guide the DSA.

5.2.5. POLYMERS FOR SUB 10NM PATTERNING

PS-b-PMMA has a minimum pitch of 20 nm and the driving force for phase separation decreases with the small χN at these small feature sizes. Thus, a new high χ BCP will be needed for technologies with half pitches less than 10nm. The χ (Chi) and minimum pitches of some candidate BCPs are shown in Table ERM9. From the perspective of minimum lamellar pitches that can be assembled, PS-PDMS (7.5nm, χ~0.26) and PS-PLA (8nm, χ~0.21)[97]appear to be promising candidates based on the limited data available. On the other hand, other materials have been reported to have higher χ PS-b-PHOST (1.46), PS-b-PAA (0.18) and PS-P4VP (0.3-0.37); however, minimum lamellar pitches have not been reported. For a candidate polymer pair (either block co-polymer or polymer blend) to be viable, it needs to have properties that support assembly of vertical structures, anneals in reasonable timeframes and can be selectively developed. Since χ decreases with increasing temperature and phase segregation may be done at elevated temperature, thermal coefficients for χ are listed in table ERM9 where available.

Table ERM9 Select Block Co-polymer Properties

For block co-polymers to vertically assembly, both the top and bottom surfaces must be neutral to the polymer pair so new materials may be needed on the wafer surface. If the block copolymers are not neutral to air or nitrogen, materials will be needed to provide a neutral surface on top of the BCP, particularly when thicker films are desired [98]. Such surfaces have been reported for PS-b-P2VP[99], PS-b-PLA[100], and poly(4-bromostyrene)-*b*-PMMA[101].

5.2.6. DEVELOPMENT & ETCH RESISTANCE

The polymer pair need to have a reasonable differential etch ratio to oxygen plasma, solvents or chemicals after anneal. As is shown in Table ERM9, the differential etch ratio of "B" block polymers with the highest etch rates in relative to polystyrene(PS), based on Ohnishi parameter, are PAA(4.5) and PLA(4.0) and PEO(3.5). On the other hand, polymers with inorganic content, PFS and PDMS, are expected to etch at a lower rate than PS. Thus, for the organic polymers, PS would be the mask material, while the inorganic containing polymers would be the mask material when they are paired with PS.

5.2.7. NEUTRAL SURFACE MATERIALS

Polymer brushes that are functionalized to attach to the coating on the wafer have been extensively used in DSA research; however, commercial materials are now being introduced to support industry evaluation of DSA. As higher χ polymers are evaluated, new neutral surface materials may be needed to coat a variety of films on wafers and in some cases materials may be needed to provide a neutral top surface coating. Processing for neutral materials needs to be compatible with wafer coating. Although polymer brushes have successfully provided neutral surfaces, processing can be time consuming. Using statistical copolymers of different composition has provided a neutral surface for DSA of PS-b-PDLA[102] and may provide a strategy for identifying neutral surfaces for new high χ block-copolymers. Recently, DSA of PS-bPEO has been successfully demonstrated on a surface without any neutral layer modification[103]. This technique was based on sequential thermal, solvent and water anneal process. Metrology may be needed to characterize surface wetting of new high χ materials at annealing temperatures.

5.2.8. MATERIALS FOR PROCESS SIMPLIFICATION

DSA processing currently requires multiple steps to pattern guide structures, produce a neutral layer, drive the self-assembly through thermal or solvent annealing, develop the pattern block, and then process the underlying layers. Materials are needed that can simplify the DSA process such as integrating a neutral layer in the hard mask[104], using the photoresist as the graphoepitaxy guide structure[105, 106], or integrating DSA functionality into photoresist[107].

5.2.9. GUIDE STRUCTURES

The specific guide structure to be used depends on the technology (graphoepitaxy or chemoepitaxy) and the application (lines or contacts, pattern rectification or pattern density multiplication, etc.). Details of the shape of the guide pattern also depend on proximity of features and for graphoepitaxy whether the sidewalls of the trench are neutral or attract one of the polymers. Although many pattern shapes may be possible, features and applications described will be limited to "contacts" (surface-normal cylinders) and "lines" (lamellar or surface-parallel cylinders).

5.2.9.1. LINE PATTERNING

For pattern density multiplication, the guide feature pitch must be an integer multiple of the DSA pitch or the lithography technique would be used to directly pattern the features. For graphoepitaxy, the lines can be formed with either lamella or embedded cylinders as is shown in figure 1a and 1b respectively. For array structures, the guide line width must be matched to the DSA domain "B"; this creates some process window constraints for array structures. However, this is a strength for graphoepitaxy when two or more line widths are needed from the same pattern. For chemoepitaxy, lines can be formed with lamella aligned to the chemical guide feature on the surface. The chemoepitaxy guide feature width has a relatively broad process window; this is advantageous for arrays but makes definition of two or more line widths in the same pattern more challenging.

5.2.9.1.1. GRAPHOEPITAXY OF LINES

For DSA of lines with lamellar forming polymers, the trench sidewalls should attract one of the polymers, while the trench bottom should be neutral to both polymers. The distance between the trench sidewall and the first feature edge ($y*L_0$) is determined by the process technology. The width of the trench would then be $N*L_0 + 1/2L_0 + 2y*L_0$ approximately as described in Figure 1 a. For embedded cylinder lines, all surfaces must attract block "A" for the assembly and block "B" will define the lines as shown in figure 1 b. The advantage of this is that all surfaces would need to attract block "A" instead of needing a neutral layer.

5.2.9.1.2. CHEMOEPITAXY OF LINES

For chemoepitaxy of lines, the surface must be neutral or slightly preferential to block "B" except where the guide lines are patterned to attract block "A" as shown in Figure 1 c and 1d. The number of lines that can be multiplied without losing fidelity must determined in process development. The guide patterns can be either $0.5L_0$ or $1.5\ L_0$ [108]; however, modeling indicates that subsurface defects may occur with $1.5L_0$[109]. If DSA is to be used for pattern density multiplication, the goal is to pattern features that are smaller than conventional lithography is capable of resolving, so the $1.5L_0$ would require less processing to provide the guide structures.

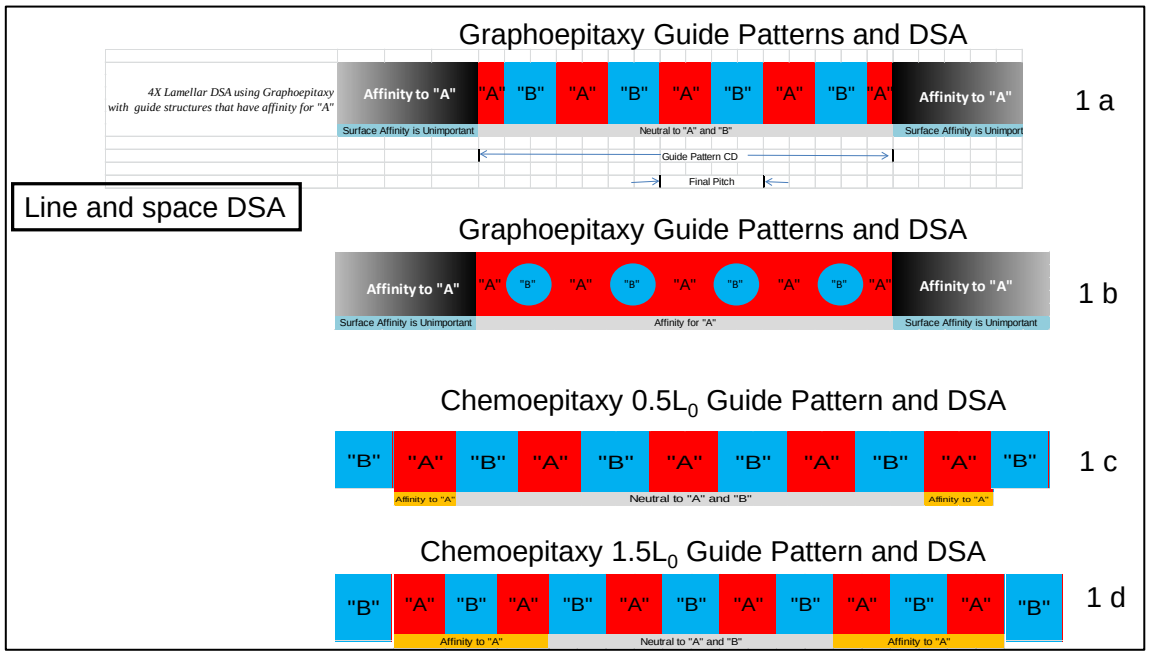

Figure ERM1 *Self Assembled Polymers Directed by Guide Patterns*

5.2.9.2. CONTACT PATTERNING

5.2.9.2.1. GRAPHOEPITAXY OF CONTACTS

For graphoepitaxy of contacts, the surface can be neutral over all areas or the trench sidewall can attract one of the blocks (Block "A" in Figure 2 a). The contacts will be larger when the surface is neutral (figure 2 b) than when the trench sidewall attracts block "A"(figure 2 a). Since the guide structure is significantly larger than the contact, this should be patternable by lithography. Furthermore with graphoepitaxy, it is possible to force assembly of multiple contacts in guide structures that could be used for assembling contacts in arrays (figure 3) that could be compatible with logic[85]. On the other hand, placing contacts in more complex arrays may require more complex guide features to achieve DSA alignment targets and the resulting overlay required.

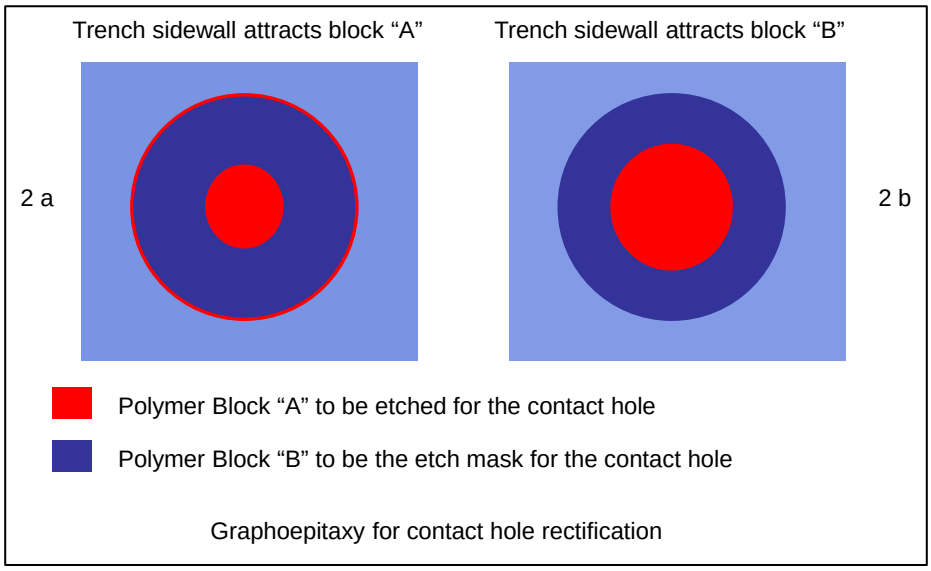

Figure ERM2 *Directed Self Assembly of Small Contacts in Guide Patterns*

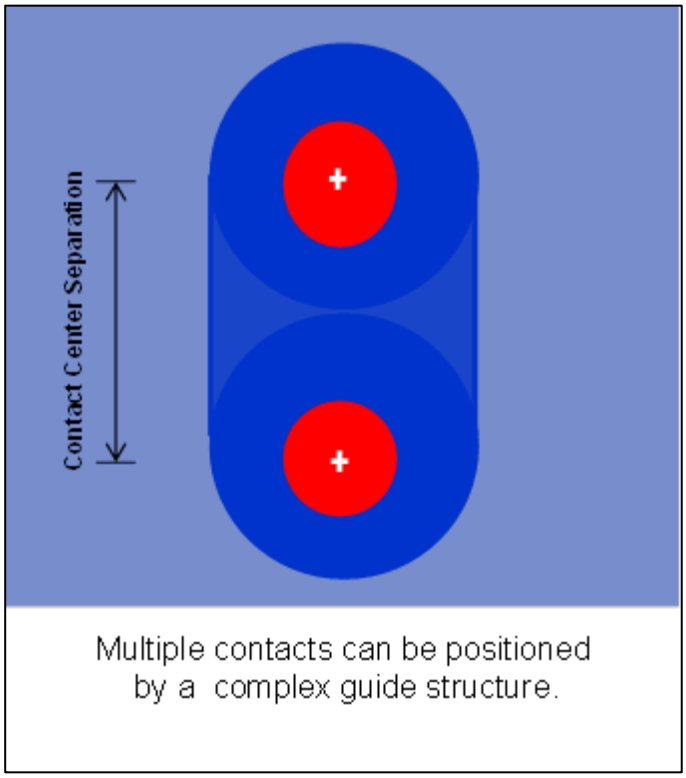

Figure ERM3 *Directed Self Assembly of Multiple Contacts in a Single Guide Pattern*

5.2.9.2.2. CHEMOEPITAXY OF CONTACTS

Chemoepitaxy is able to guide pattern density multiplication; however, the contacts tend to form in the hexagonal close-packed natural order that occurs with the self-assembly. Thus, it may not be suitable for driving assembly in arrays desirable for integrated circuit fabrication. It may have use in defining DRAM capacitor arrays provided that the guiding templates can enforce sufficiently low defect density. As this may require EUV patterning to define competent guiding templates, the cost starts to be come prohibitive.

5.2.10. DESIGN TOOLS

Design tools are needed to translate from the desired layout to the guide structures that need to be patterned on the wafer to drive assembly of features in required locations and shapes. The capabilities required will depend on the application and technology capabilities. The design tools need to include factors that include the process factors of DSA and Litho tool and process capabilities. Many of the basic concepts are described above in the Guide Structure section. Efficient models need to be developed that evaluate the effectiveness of a specific mask design in achieving positional and CD accuracy in the DSA patterns on the wafer similar to that recently demonstrated[110].

5.2.11. DSA CRITICAL ASSESSMENT

The ERM conducted a voting based survey of the potential viability of directed self assembly to extend lithography. The potential applications of DSA considered were 1) line edge roughness (LER) improvement; 2) Contact or via CD improvement; 3) density multiplication for memory array patterning; and 4) density multiplication for logic. The average scores for line and contact rectification were (2.1), while pattern density multiplication had average scores of (2.0) indicating that the technology is promising. The results of the DSA Critical Assessment are shown in Table ERM10. For all applications, several were concerned about etch resistance of the polymer patterns. Also, for contact rectification and pattern density multiplication, several were concerned about the availability of EDA tools to translate from layout to guide structures on mask. For pattern density multiplication, several were concerned about defect densities and line width roughness (LWR). There were also concerns about metrology to detect defects and material contamination limits for pattern density multiplication. Voting indicated confidence that DSA could achieve pattern density multiplication and pattern small features with short annealing times. So, this critical assessment of DSA indicates that significant progress has been made in specific areas, but there are challenges in defect density and integration.

This critical assessment is based on voting by 7 participants from the ERM, Lithography, and participants in the DSA workgroups.

Table ERM10 Directed Self Assembly Critical Assessment (2013)

6. EMERGING FRONT END PROCESSES' AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES' MATERIAL CHALLENGES AND OPTIONS

Key challenges for future FEP and PIDS materials and processes are to support extending CMOS to smaller dimensions while achieving technology goals for power, performance, and reliability as well as goals for device variation. This will require more accurate placement of dopants in active device areas, deposition of gate dielectrics with electrical oxide thickness (EOT) <0.5nm with ultralow leakage, and ultra-low resistivity contacts. Potential solutions include directed self-assembly of useful nanomaterials, novel materials to enable selective deposition, etch, and clean to enable self-aligned structures in future devices. The requirements and challenges for ERM applied to FEP and PIDS applications are summarized in Table ERM11.

6.1. DIFFICULT CHALLENGES

Multigate FET devices require accurate control of carrier concentration in channel and source/drain (S/D) regions of "fin" structures. While channel concentration can be controlled by use of gate metal work function, ion implantation in S/D regions can result in non-uniform channel lengths through the height of the fin, so doping approaches are needed to uniformly dope the S/D regions of a fin that is less than 10nm "thick". Future technologies will require higher dielectric (κ) gate dielectrics; however, the bandgap of potential materials is low and their barrier to electron tunneling is low. Future technologies will require lower contact resistivities; however, Fermi level pinning at the metal semiconductor interface often produces a Schottky barrier that increases the resistivity, so novel approaches are needed to eliminate Fermi level pinning.

Table ERM11 FEP/PIDS Challenges for Deterministic Processing

6.2. DOPING AND DEPOSITION

A key challenge for scaling semiconductor devices below 10 nm is the ability to achieve high doping levels within source/drain regions, with abrupt dopant gradients with small variations at the source/drain interface to the channel, as well as controlled dopant positions within the channel. Multigate structures require uniform S/D dopant location though the depth of a narrow fin. Potential approaches to producing these uniform S/D doping profiles in fins include: monolayer

doping with liquid, vapor or gas sources or novel ion implantation techniques. For threshold voltage control variations in channel dimensions, the gate stack structure, and dopant variations in the depletion layer[1-5] must be controlled. The threshold voltage variability will gate the extensibility of bulk planar CMOS device technology. Control of channel carrier concentration is achievable through selection of the gate electrode work function and the gate dielectric thickness; however, control of dopant location may also be needed. It has been demonstrated that it is possible to tune electrical properties by controlling, not an ensemble of dopants but, the placement of individual dopants[6]. Research is needed to develop new materials and fabrication methods that enable deterministic control of the composition and structure of doped material and gradient systems. One way to precisely control the doping profile is by deterministic processing and doping[7-10].

6.2.1. MONOLAYER AND CONFORMAL DOPING

Since multigate structures require uniform S/D doping on fin structures that are in close proximity, potential approaches to doping the surfaces uniformly include deposition of a Langmuir monolayer of dopants from liquid[11-13], vapor or gas[14]. This chemistry-based approach has demonstrated that the dose can be modulated precisely by the formation of a mixed monolayer, consisting of tunable blank and active precursor components. Additionally, controlled nanoscale semiconductor doping by self-assembled molecular monolayers with loaded dopants can achieve sub-5-nm ultra-shallow junctions with spike anneals[15,16], due to the lack of transient-enhanced diffusion, often encountered in ion implantation. A key objective is to heavily dope 'self-aligned' semiconductor materials for multigate and planar device applications.

6.2.2. DETERMINISTIC DOPING

One way to control the doping profile is by deterministic doping. Doping processes with atomic-scale placement and concentration control will enable tunable device performance characteristics and reduced device-to-device variations. A reduction in device noise enlarges the useable design space, circuit-level uniformity, and system performance. One positive outcome of ultimate doped transistors has been the demonstration that it is possible to tune electrical properties by controlling not an ensemble of dopants, but the placement of individual dopants[6]. Deterministic doping also refers to 3D nanopatterning and assembly methods that provide sufficient control of the composition and structure of doped interfaces and components to yield several orders of magnitude improvements in device-to-device performance variability. Candidate doping options must address the following: 1) atomic-scale control of dopants and massively parallel dopant delivery; 2) random dopant fluctuation in the active channel region, ultra shallow junctions in the source/drain region and abrupt transitions between the source/drain regions and the channel; 3) compatibility and integration with existing fabrication platforms; and 4) economics, which depends upon R&D and equipment costs, yield, and throughput.

Deterministic doping focuses on: 1) introducing single-dopant/few-dopants within the channel, as well as the source/drain regions, with placement accuracy of <<10nm; 2) activating the low number of deterministically introduced dopants effectively; 3) measuring and imaging single-dopant/few-dopants precisely; 4) exploring potential application opportunities through the atomistic control of materials, devices, and processes for better device performance. New metrologies can enable the characterization and realization of well-designed atomic-scale devices.

6.2.2.1. STATE OF THE ART

The deterministic 3D dopant placement and structural control technology required to enable atomically abrupt and reproducible source-channel-drain interfaces are in the early phases of exploratory research. This year's revision reviews recent progress in this area and considers potential options for enabling extensible doped CMOS channels and leveraging related emerging materials, devices and processes, and new device concepts, including quantum computing devices in Si or diamond, for sub-16nm applications. The ability to place dopants with atomic precision are described in more detail in the Device Materials Section of the ERM Chapter.

6.2.2.2. DIRECTED SELF ASSEMBLY FOR DETERMINISTIC DOPING [34-36]

Since SII and STM are not capable of supporting deterministic doping in high volume manufacturing, directed self-assembly, with either block co-polymers or Langmuir surface assembly are being explored to position dopants with precision in high volume. Controlled nanoscale semiconductor doping by self-assembled molecular monolayers with loaded dopants can achieve sub-5-nm ultra-shallow junctions with spike anneals, due to the lack of transient-enhanced diffusion, often encountered in ion implantation. Directed self-assembly with block-copolymers provides a potential path to assembling dopants in precise locations on surfaces of 3D Multigate structures and planar device structures. A well-developed infrastructure for wafer-scale directed self-assembly (DSA) in nanomanufacturing is available. Perpendicular lamellae for lines and cylinders for spot patterns with 12 nm through-film domains by DSA have been demonstrated.

Pathways exist to reach sub-10-nm features and possibly sub-10-nm pitch features with sub-1-nm placement accuracy. Potential use of DSA for form sacrificial templates for ion implantation or dopant diffusion could be considered based on monolayer approaches.

6.2.3. LOW THERMAL BUDGET ACTIVATION[37-40]

Very low thermal processing with microwave radiation, as well as millisecond energy pulses from flash lamps and laser, could keep dopant diffusion minimal. Microwave anneals could selectively generate heat directly inside the exposed material in the form of molecular rotational or polarization energies. That locally deposited energy becomes ergodically transferred throughout the material, achieving the desired activation with negligible diffusion. Microwave anneals at temperatures <500^{o}C have been demonstrated for B, P, As in Si, Ge, and poly-Si. In addition, to replace the conventional n+/p+ poly-Si gate materials and maintain the performance of CMOSFETs, it is necessary to use a suitable pair of metals with work functions that are near the conduction-band and valence-band edges of silicon. Microwave anneals shows great promise in realizing a gate-first process with metal gates, due to its low-temperature processing. For Ge CMOS, diffusion-less junction, no dopant diffusion in Ge with an ultrathin nickel germanide layer with low resistivity can be achieved by microwave anneals. The underlying physical mechanism should be well understood. For STM-fabricated devices, a low-temperature incorporation anneal has been found to activate the dopants with minimal dopant diffusion[31].

6.2.4. METROLOGY FOR DETERMINISTIC DOPING

A detailed description of metrology requirements is listed in the ERM Metrology Section of this Chapter.

6.2.5. KEY MESSAGES

Monolayer doping can achieve controlled sub-5-nm ultra-shallow junctions with spike anneals. This monolayer doping can be achieved through use of wet chemicals or Langmuir deposition of gas molecules on the surface of the semiconductor. Potential applications include channel doping, S/D doping and contact resistance engineering. This potentially enables controlled uniform doping of S/D regions of 3D multi-gate FET devices. For ultra shallow Source/Drain processing, microwave annealing offers the potential for activation of dopants at much lower temperatures with little diffusion. Channel carrier concentration can be controlled through gate work function selection or deterministic doping. Monolayer doping looks promising for ultra shallow S/D and more abrupt dopant profile. Novel dopant profiles may be needed to reduce contact resistance. Full low-temperature microwave processing for Si and Ge CMOS will help atomic control of dopant distribution.

For deterministic doping with DSA, although the average spacing between dopants can be somewhat tuned by the choice of carrier molecule, the creation of complex dopant patterns, with required dopant control, remains a challenge, but is still a promising route. Well-developed infrastructure for DSA for nanopatterning and potential use as sacrificial templates for ion implantation or dopant diffusion has been established. Tolerance for energetic implantation and single-dopant per domain are the challenges. Defects and contamination must be understood and controlled. For medium placement accuracy applications, ~10 nm, realized by present doping methods (i.e., single ion implantation) exhibit the potential for the development of device applications. Research is needed on high throughput doping options that also deliver high placement accuracy. Emerging candidate doping techniques focus on areas including directed self-assembly and the use of molecular monolayers as scaffolds for accurate and controlled dopant delivery.

Atomic-scale control of dopant position have been demonstrated by STM and deterministic ion implantation, enabling the exploration of fundamental device limits and new functionality, and practical realization may become more likely in a time frame of 10-15 years. However, higher temperature operation (i.e., 400°K), practical atomic-level control and cost-effective techniques are needed to move towards high-volume manufacturing within the next 10-15 years.

Novel characterization techniques, such as 3D atom probe tomography, will help to guide the evolution and assessment of emerging deterministic-doping technologies towards this goal. Deterministic, conformal and monolayer doping will lead scaling semiconductor devices towards the single-dopant limit and contribute to extend the CMOS platform.

6.3. ULTRA HIGH K DIELECTRIC

To extend scaling of CMOS devices, and ultra-high κ dielectric is needed with electrical oxide thickness (EOT) of ≤0.5, but it must also have ultra-low leakage current and high breakdown field for high reliability. The challenge is to identify materials and processes that can deposit the ultrahigh κ dielectric on the semiconductor surface with stable oxide and interface, low interface states and traps (unpinned Fermi level), low leakage current and the other desired properties. In addition, the high κ dielectric material must be etchable with conventional plasma chemistries.

The current high κ dielectric, HfO2, has a dielectric constant of 24 which is too low to enable EOT below 0.5nm. Transition metal oxides with higher dielectric constant include TiO_2 (κ~80) and $SrTiO_3$ (κ~300); however, these materials

have ~0eV conduction band offset to Si[51] which would allow significant electron leakage current. Furthermore, these materials may react with the semiconductor or form interface states when deposited on silicon, Ge or III-V surfaces.

One approach is to deposit an ultrathin medium κ dielectric that is known to produce stable interfaces and an unpinned Fermi level, and then deposit a thicker ultrahigh k dielectric on the medium κ material. To achieve low leakage, the high κ dielectric must present a potential barrier to carrier tunneling, so to block electron tunneling, the conduction band offset of the dielectric to the semiconductor should semiconductor conduction band. Similarly, the valence band offset of the dielectric to the semiconductor valence band must be adequate to prevent hole tunneling below the valence band of the semiconductor.

To achieve low EOT on Ge, several bi-layer films have been employed with each having a low interface state density film with a much higher κ dielectric on top. TiO2 has a dielectric constant of ALD films of TiO_2-AlOx-Ge had an effective EOT of 0.65nm with a low Dit[52]. This approach should be further explored to determine whether multiple layer gate insulators with ultra-high κ dielectrics can provide sub 0.5nm EOT and ultralow leakage currents.

6.4. SELECTIVE ETCH AND CLEAN/SURFACE PREPARATION

With the wide range of new materials potentially being integrated into future technologies, there are significant needs for materials that enable selective and customized etching, cleaning or material deposition. Either macromolecules or self-assembly processes that can enable coating of a specific material in the presence of other chemical processes, such as etching or chemical mechanical polishing could improve process selectivity and yield. Similarly, as feature sizes are reduced, cleaning processes will need to be more selective in removing particles without disturbing the desired structures. Thus, there are opportunities for macromolecules and self-assembled materials to enable the enhanced selectivity of future manufacturing processes.

Etch represents a critical step in conventional top-down pattern transfer processing. The lithographic and etch processes are significant contributors to the final dimension, dimensional variation, and functionality of a patterned feature. It may be advantageous to consider simplified fabrication scenarios that reduce the number of pattern transfer steps and the corresponding process related variability. The directed self-assembly of electronically useful materials represents an identified set of emerging technology options that show some potential for process simplification and for reducing patterning related variability. Early approaches for directed self-assembly target resist applications that complement and leverage existing and projected lithographic and etch technologies. Future generations of self-assembling systems may be designed to incorporate electronically useful materials that would obviate the need for some etches.

6.5. CONTACTS

As devices are scaled to smaller dimensions, contact resistance has a larger relative impact on device performance. The contact resistance is determined in part by the energy alignment between the metal Fermi level and the semiconductor bandgap, determining if the contact is of Schottky or Ohmic type. At metal/semiconductor interfaces, Fermi level pinning usually leads to a Schottky barrier; in the past, it was possible to reduce the contact resistance by highly doping the semiconductor to reduce the thickness of the potential barrier at the metal semiconductor interface; however, this is not possible in many nanoscale devices. In addition to this, metal contacts often form an alloy with the semiconductor and this would consume considerable amounts of a multigate FET such as a FinFETs. The emerging approaches to reducing the contact resistance include introducing a thin tunnel barrier at the interface or introducing a dipole or charge at the interface. For ultralow resistance contacts, it is ideal to have the Fermi level of the metal aligned with the Fermi level of the semiconductor majority carriers; however, Fermi level pinning often results in a Schottky barrier at the interface. Thus, it is important to eliminate Fermi level pinning that produces a Schottky barrier and increases contact resistance. The material that is that doesn't pin the Fermi level may produce a barrier to carrier transport between the metal and semiconductor, so it must be as thin as possible. Furthermore, introducing dipoles or fixed charge in the barrier layer may be able to adjust the offsets between the metal and semiconductors.

6.5.1. TUNNEL BARRIER TO ELIMINATE CONTACT FERMI LEVEL PINNING

Since Fermi level pinning occurs at most metal-semiconductor interfaces, which produces a Schottky barrier, introducing a material at the interface that passivates the interface and eliminates the formation of the Schottky barrier[53]. Often identifying materials and processes that don't introduce detrimental pinning levels at the semiconductor interface must be experimentally determined. For silicon, SiO_2 produces an unpinned interface, For Ge[54]and some III-V[55] materials, Al_2O_3 or AlO_x can, depending on the deposition technique, produce Fermi levels that are close to the contact metal energy levels at these semiconductor interfaces. A thin layer of ZnO[56] has been demonstrated to produce low resistance Ge-Ti contacts as a result of aligning the Ge Fermi level with the Ti Fermi level.

6.5.2. DIELECTRIC DIPOLE TO REDUCE SCHOTTKY BARRIER HEIGHT

Once a non-pinning interface material has been identified, a dipole can be introduced in the barrier material by depositing a thin dielectric that has a low barrier to carrier transport. When two materials with different work functions are placed in contact, a dipole can form at the interface. Introduction of a 1nm thick AlO_x/SiO_x layer in Si contacts reduced the Schottky barrier height by ~100meV in a FinFET which reduced parasitic S/D resistance by 25%[53]. To achieve low contact resistance, the barrier to carriers must be as low as possible and as thin as possible.

6.5.3. INTRODUCING FIXED CHARGE IN THE INTERFACIAL LAYER

Introducing positive fixed charge in the interfacial layer can induce negative carriers at the semiconductor interface which can change the alignment of the semiconductor bands to the metal. This can be used to fine tune barrier height between the metal and the semiconductor.

6.6. INGAAS ALTERNATE CHANNEL MATERIALS

For n-channels, InGaAs quantum well FET's on silicon have been reported with mobilities of 10,000 to 3000 $cm^2/V\text{-}s$ [57] using 1.2-micron buffer layers. For this to be a viable technology to enhance CMOS, multiple capabilities are needed including selective growth or multiple thin III-V materials on silicon, high k dielectric with EOT<0.5, and continued reduction of contact resistivity.

6.6.1. SELECTIVE III-V EPITAXY ON SILICON

InGaAs device structures for high performance require fabrication with multigate structures[58] and the simplest fabrication is with selective epitaxy. To fabricate high quality III-V materials on silicon a III-V buffer layer must be grown on a silicon surface that has steps, to eliminate formation of antiphase domains, and this has been accomplished with Ge/III-V growth in a silicon trench[59,60], which reduces defects and is called aspect ratio trapping . After the thick buffer layer is grown, multiple thin films are required to enable a thin buried high mobility channel[61]. MOVPE has been demonstrated that be capable of depositing high quality multilayer thin III-V films on silicon[62]. Thus, growth of high quality III-V films on silicon has been demonstrated in potentially high volume manufacturing tool.

6.6.2. HIGH K GATE DIELECTRICS

High k dielectrics including Al_2O_3[63] and $TaSiO_x$[64] have been deposited in InGaAs; however, even higher dielectric constant gate dielectrics will be needed in the future. A critical challenge is to fabricate EOT<0.5nm gate dielectrics on multigate III-V FET structures and the potential solutions will be similar to those identified in ERM Section 6.3.

6.6.3. CONTACT RESISTIVITY

Contact resistivities to n-InGaAs as low as $1.1\times10^{-8}\Omega\text{-}cm^2$ with Molybdenum have been reported with UV ozone/HCL/H cleans and recently sputtered Pd contacts had resistivities as low as $4\times10^{-9}\Omega\text{-}cm^2$ were reported. Pd silicide contacts to InGaAs doped to 1×10^{19} cm^{-3} were reported to have contact resistivities of $1\times10^{-8}\Omega\text{-}cm^2$ [67]. Thus, low contact resistivities are achievable with multiple contact metallurgies; however, as film thicknesses and contact areas decrease in size, contact resistivities may need to be reduced further. Further reduction in contact resistivity may require evaluation of interfacial passivation techniques discussed in ERM 6.5.

7. INTERCONNECTS

Key challenges for continued increased performance of future integrated circuit interconnects consist of maintaining reductions of RC time constants for delivery of signals and power with high reliability. For copper interconnects to be extendible through 2024, the sidewall copper barrier thickness must be reduced to less than 2nm, which is challenging for technologies, as is summarized in Table ERM11. For post copper interconnect scaling, novel interconnects, such as carbon nanotubes, are being explored for their low resistivity and electromigration resistance and the challenges for these technologies are summarized in Table ERM12. Also, lower dielectric constant (κ for both intra and inter level dielectric are needed; however, each of these emerging families of materials must overcome significant challenges for them to warrant adoption. Airgap, another approach to reducing the effective κ, if adopted, would place additional requirements on barrier layers or novel interconnects.

Table ERM12 Interconnect Material Challenges

7.1. NOVEL ULTRATHIN BARRIERS

The scaling of Cu barrier layer thicknesses below 2nm faces several challenges including the ability to block diffusion of Cu during processing, packaging and operation, have good adhesion to Cu and the low-κ ILD, block H_2O/O_2 diffusion into the Cu, and be compatible with Cu interconnect processing, such as CMP, ILD etch, and photoresist ashing. New trench/via barrier materials, such Ru and CuMn that are discussed in the Interconnect chapter, are in development and expected to maintain barrier thickness scaling for several generations, but forecasts project Cu barrier layer thicknesses of < 2 nm by 2015 and < 1 nm by 2021. At these dimensions, it is anticipated that all barrier materials in development may fail and new materials or multilayer thin films will be needed. If the industry moves to airgap ILD technology, the barrier requirements for these structures will become still more challenging.

A logical extension of the current trench/via barrier materials would be to identify new transition metal nitrides or direct plate metals with improved barrier capabilities that meet future requirements. To date, a host of alternate transition metal nitrides and direct plate metals have been investigated but only demonstrated at thicknesses down to 5nm. While, recent results for a 2.5nm MnN barrier have been reported[1] , more research on new barrier metals at < 5nm and ultimately < 1-2 nm is needed. Additionally, research is needed to determine whether metal (nitride) barrier films deposited by industry standard techniques are continuous at these dimensions - particularly in the presence of 2nm surface roughness likely present from patterning line edge roughness and low-k ILD porosity.

As an alternative to new "hard" metal barrier materials, research is also needed on so called "soft" Cu barrier materials such as self assembled monolayers (SAMs) and other organic films. SAMS were added to the 2009 ITRS and have shown the ability to impede Cu diffusion and improve adhesion between Cu and dielectric materials[2]. However, SAM barriers have not exhibited equivalent barrier performance to industry standard TaN[3]More research is therefore needed to characterize and benchmark the performance of 1-3 nm thick SAM barriers versus hard barrier materials of similar thickness. Concerns over the survivability of SAMS in downstream processing and their barrier performance when combined with porous low-k ILDs, 2nm surface roughness, topography, and defects also need to be addressed. Organic films as Cu barrier materials are highly attractive due to their relatively low dielectric constant, but have yet to be demonstrated as Cu barriers at the 1-2 nm thicknesses of interest[4] or in cases where significant topography or surface defects exist.

Graphene as a Cu barrier material also deserves some consideration and research. Graphene's < 1nm thickness would be ideal for beyond 2020 technologies, and recent results have shown the ability of monolayer graphene to protect Cu and Cu/Ni alloys against oxidation on the macro scale[5] . However, additional research has shown that microscale surface oxidation of Cu can occur due to rapid moisture diffusion under graphene surface edges and through graphene grain boundaries and defects[6,7]. Thus in addition to research into growth and transfer of graphene for Cu barrier layer applications, research focused on methods to seal terminal graphene edges and defects is also needed.

Dielectric Cu capping barrier layers are also forecasted to approach thicknesses of < 2nm by 2020. At these dimensions, it can be anticipated that the current SiN/SiCN/SiOC materials will fail and that new materials will need to be identified. While the key technical challenges for Cu capping layers are similar to those for the via/trench barrier layer, there are additional dielectric constant scaling requirements and it can be anticipated that the current k values of > 4.0 for these layers will become unacceptable by 2020. While alternate paths focused on removing the Cu capping layer may be pursued, parallel research is needed on new Cu capping materials such as SAMS, organic films and other potential candidate materials such as a-C:H, a-CN_x, and a-BCN_x. Hexagonal BN (h-BN) an analog of graphene with a large band gap of 6 eV and k of ~ 4.0 should also merit some attention for these applications[8].

In summary, all of the candidate < 2nm barrier materials have their strengths and weaknesses. As a means to perhaps address some of the weaknesses of each material, research that investigates combinations of "hard" and "soft" barrier materials should be considered and is highly encouraged as a means to address the needs of future technologies.

7.2. NOVEL INTERCONNECTS

Table ERM13 Nanomaterials Interconnect Challenges

7.2.1. NANOTUBE INTERCONNECTS

Emerging SWCNT or MWCNT nanotube interconnects or vias must demonstrate high densities of highly conducting nanotubes in desired locations, with controlled directionality and, low-resistance contacts. Additionally, the CNTs must be grown with a catalyst that is compatible with the ILDs and general semiconductor processing. CNTs exhibit ballistic transport over longer distances,[9,10] but SWCNTs consist of a mixture of metallic and semiconducting tubes, thus limiting

their viability. MWCNTs, however, are distinctly metallic making them attractive as an interconnect candidate. A potential advantage of CNT vias is their ability to carry high current density without electromigration; however, electromigration at metal interfaces may be an issue.[11] Further, their low resistivity may offer potential advantages for interconnect applications, which include their ability to achieve ballistic transport. Since CNTs also exhibit quantum limited contact resistance, their length must be sufficient to yield favorable effective resistivities, as described in the ITRS Interconnect chapter. Additionally, CNT conductivity must remain high and stable during operation. Research and guiding material-design principles are needed for improved CNT functionalization, deposition, and positional control.

7.2.1.1. GROWTH IN CONTROLLED LOCATIONS WITH ALIGNMENT

For CNTs to be used as either devices or interconnects, they must be grown in precise locations and aligned in required directions. While progress has been made in growing nanotubes in desired locations,[12] directional alignment remains a challenge. Recent results suggest that CNTs grown in a directed electric field[13] can achieve general directional alignment. Additionally, growth on catalyst patterned sapphire or quartz crystal steps has grown aligned CNTs[14-16], although, placement remains a challenge. While growth on this substrate is less than the required density, this alignment is significantly better than other techniques. Another challenge is the controlled growth of CNTs. A zeolite can be used to control CNT growth diameter[17], location and direction, however it must be demonstrated that such a templating matrix has no impact on the CNT conductivity. While several approaches to produce CNTs have been identified, the practical implementation of this concept to manufacturing remains elusive. Post-growth assembly options also are being explored.

Since interconnects span relatively long distances, high speed growth method should be strongly pursued.[18-20] The quality of CNTs affect the ballistic length of carrier transport in a tube. Therefore, high quality CNT growth and evaluation of their quality are important. The length must be sufficient to yield favorable effective resistivities, as described in the Interconnect chapter.

7.2.1.2. NANOTUBE VIAS

Vertical interconnects (vias) may benefit from the integration of CNTs into future technologies. Especially, recent three dimensional device structures require extremely high aspect-ratio vias. For these applications, CNTs are a suitable solution to fill very high aspect-ratio via holes [21]. Although an approach for the integration of CNTs into contemporary CMOS technology has already been demonstrated[22-25] a number of unsolved critical issues still remain to be addressed. Thus, new hybrid integrating schemes (combining top down and bottom up paths) compatible with the actual CMOS technologies and engineered at a level that also use thermal budgets (below 600 °C to reduce the thermal damages to LSI) are needed. In addition, theoretical studies have been carried out to derive electrical properties and offer an important guidance and insight on the applications of CNTs vias for gigascale-integration chips.[26-30] CNTs can significantly improve the RC delay and thermal conductivity at the intermediate and global level. For CNT vias to be viable they must be fabricated with a catalyst that is compatible with the ILD and semiconductor devices and their electrical and thermal reliability must be demonstrated. A number of key processes for which a control needs to be established to realize the potential of CNTs are described in the following sections.

7.2.1.2.1. CONTROL OF CHIRALITY AND OF METALLIC VS. SEMICONDUCTING FRACTION:

In order to achieve comparable resistances predicted for Cu-based wirings, dense arrays (~1E14 tubes/cm^2) of small diameter (~1.2 nm) metallic SWCNTs and DWCNTs will be required. The variability of intrinsic CNT-via resistance is a function of the distribution of chiralities, which could exceed projected requirements. Hence, additional research is needed to elucidate chirality control. In the case of MWCNTs tradeoffs need to be made in the diameter and number of walls to achieve the highest density; however, the chirality control is less of an issue as the overall behavior is metallic.

7.2.1.2.2. CONTROL OF CONTACT RESISTANCE AND ELECTRICAL CONDUCTIVITY:

The lower intrinsic limit of the resistance for a metallic SWCNT (or a metallic shell of MWCNTs) is 6.5 kΩ (independent of the tube diameter)[31] and reflections at the CNT-metal contact interface and phonon scattering contribute to an increase in total resistance.[32-35] Therefore, reliable and reproducible low resistance ohmic contacts are needed, since high resistances results in current reduction. Transparent SWCNT ohmic contacts, scaled to diameters <1.5 nm, remain a key challenge to achieving high-performance in nanoelectronic devices, due to the presence of positive Schottky (semiconducting nanotube) and tunneling barriers (metallic nanotubes). Fabricating direct metallic connections between all the nanotube shells also remains a technological challenge, since contact resistances at the bottom and top of CNT-based vias may enhance the risk of local heating and electromigration.[25] In the case of vias filled with MWCNTs, resistances down to 0.6 Ω have been reported for 2 μm diameter vias[36, 25], and 34 Ω was reported for 160 nm diameter vias.[37] To reduce bottom contact resistance, CNTs have been grown on conductive under layers such as TiN [25,37,38], RuO_2 [39] and Ti/Cu [40]. As for the top contact, CMP process [41, 42], surface treatment before metallization [43], contact metal selection [44], and annealing after metallization [43] etc. are issues that need significant research. It is also important to characterize

individual CNT resistance [43,45] to distinguish between contact resistance and tube resistivity. To lower the CNT resistivity, doping may be necessary. Various surface doping such as iodine [46] and metals [47] have been reported to enhance conductivity of CNTs; however, the doping would also need to be stable in interconnect processing environments.

7.2.1.2.3. HIGH DENSITY CNT ARRAYS IN SMALL VIAS:

Ideal SWCNT arrays and contacts exhibit potential to improve intermediate and global RC delays by >40% over Cu wires. Locally, short low resistance CNT vias are needed that reduce the total capacitance, relative to Cu. Also, in-situ CNT growth and integration on relevant substrates is currently far from manufacturable. A catalytic process is needed that exclusively promotes growth of metallic SWCNTs, with the required density of ~1E14cm^{-2}. Also, appropriate, reliable, and reproducible analytical tools and statistical methods must be developed to help guide the integration and assess the insertion potential of this potential via technology. [27,28,48,49]

In the case of MWCNTs, the resistance of a 70 nm diameter via filled with close packed nanotubes of 4 nm diameter 6-wall MWCNTs including the top and bottom barrier layer can be estimated to be as low as that of Cu via. Based on this estimation, the target density of the MWNTs is 5 ×10^{12} cm^{-2}. Moreover, such high-density growth has to be performed at low temperature, for instance, at 400 ºC. For low-temperature growth, MWNT growth at temperatures as low as 400 ºC or below has been demonstrated[37]. As for high-density growth, vertically aligned diameter-controlled MWCNTs with density of 1-2.5×10^{12} cm^{-2} has been reported.[38,50] Independently, the fabrication of 70-nm diameter vias with MWCNTs grown by pulse-excited remote plasma-enhanced CVD has been also reported.[18,51] CNT growth from a via holes with a diameter of 40 nm was also demonstrated using Co nanoparticles as a catalyst[36]. CNT growth from the bottom of extremely high aspect ratio (AR) holes such as AR=19 have been developing for extremely high AR contact via applications. [21,52] Wafer scale integration process of CNT vias are developing based on BEOL process. 200 mm and 300 mm wafer based CNT growth, CMP process and via fabrication have been reported. [21,53,54,55,56]

7.2.2. GRAPHENE AND GRAPHITIC CARBON INTERCONNECTS

Graphene is also a possible candidate for an interconnect material to replace Cu. Graphene is inherently a two-dimensional material, so it may be ideal for horizontal interconnects. Graphene, like carbon nanotubes, can sustain a high-density current. In fact, research demonstrated that a few-layer graphene peeled off from graphite could sustain a current larger than 10^8 A/cm^2. [57] Numerical simulations predict that graphene nanoribbons can potentially have lower resistance compared to copper with a unity aspect ratio for widths below 8nm. Additionally, the simulations show stacks of non-interacting nanoribbons can have significantly smaller resistivities than Cu wires.[58] In order to realize graphene interconnects, a low temperature method for synthesis of graphene on a suitable substrate must be realized. Recently, synthesis of graphene by chemical vapor deposition (CVD) has been reported.[59-61] However, the synthesis temperatures are typically around 1000^{o}C, which is too high for interconnect applications. Recently, growth of multilayer graphene at 650^{o}C [62] and 580^{o}C [63] has been demonstrated, and the reliability of CVD-grown graphene interconnects have been investigated[62,64]. Sub-100-nm-wide multilayer graphene wires were reported grown by plasma-enhanced CVD at 600°C under different growth conditions[65]. The resistivity of the CVD graphene wires is reduced when the crystalline quality of the graphene is improved. A resistivity as low as 600 μΩ·cm is obtained, which is about one order of magnitude higher than that of high-quality graphene exfoliated from bulk graphite. Although the resistivity is not reported, graphene was selectively grown on the Ni damascene interconnects at 500°C by 300 mm wafer CVD[66]. More research is needed in low temperature deposition to achieve graphene interconnects. Moreover, synthesis by CVD usually requires a catalyst film, which may have to be removed after the synthesis. In order to solve this problem, the catalyst-free growth of networked nanographite (NNG) on Si and SiO_2 substrates has been developed by using photoemission-assisted plasma-enhanced CVD.[67] In addition, multilayer graphene was obtained by annealing sputtered amorphous carbon film with a Co catalyst layer on it[68]. The upper Co film can be easily etched away after annealing, thus leaving multilayer graphene on SiO_2/Si substrate.

Transfer of graphene that is grown elsewhere at high temperature onto a target wafer is another option for interconnect application of graphene. For instance, 5-layer transferred graphene interconnects with high reliability were demonstrated [69]; however, their resistivity was much higher than that of Cu. More recently, high-quality multi-layer graphene (MLG) was grown on an epitaxial Co film and transferred onto another substrate for fabricating interconnects[70, 71]. The resistivity of MLG interconnects was as low as 50 μΩcm with better high-current reliability than Cu. The MLG interconnects were further intercalated with FeCl3, providing a resistivity as low as 4.1 μΩcm, which is close to that of Cu [70, 71]. The next step is to examine the resistivity of MLG nanoribbons with a width of 10 nm or narrower.

7.2.3. CU AND SILICIDE NANOWIRE INTERCONNECTS AND VIAS

If single crystal nanowire metals could be grown with smooth surfaces[72-74], they could reduce many of the issues associated with grain boundary induced resistivity increases and sidewall roughness scattering, as illustrated in the Interconnect Cu Resistivity chart in the Interconnect chapter. Research is needed to demonstrate the feasibility of the following: self-assembled nanowires with smoother surfaces and reduced surface scattering; hydrogen passivation to reduce the diameter dependence of resistivity, diffuse surface scattering, and the grain boundary scattering in polycrystalline nanowires.

Successful copper replacement materials must provide lower resistivity and higher electromigration resistance than copper, at the same dimensions. Potential interconnect replacement materials, such as carbon nanotubes for vias and interconnects and possibly single crystal copper metal nanowires for interconnects, must overcome significant challenges to warrant insertion consideration as identified in Table ERM12.

7.3. LOW K INTERLEVEL DIELECTRIC

New low κ dielectrics continue to be needed to reduce capacitive coupling between interconnects and reduce energy consumption; however, the integration challenges for new materials are very difficult as detailed in table ERM12. The processing of low κ dielectrics, etch, cleans, deposition of metals, and planarization often degrade their performance. Thus, metrology is needed to characterize their properties at different stages of processing and after integration with interconnects. The unique metrology needs for low-k / Cu interconnects in the general areas of low- κ glass structure characterization and nanometer scale mechanical property measurements have been previously detailed in the 2011 edition of the ITRS. Three new interconnect metrology areas of need include methods for (1 assessing the thermal conductivity and thermal boundary resistance (TBR) of interconnect structures, (2 zero charge imaging techniques, and (3 methods for performing nanometer scale structure-property characterization of low-k/Cu interconnects. Detailed description of the need for these new metrology capabilities in included in the ERM Metrology Section 10.7.

8. ASSEMBLY AND PACKAGE

Key challenges for future assembly and package technologies are to provide a controlled stress reliable package that meets z-height, motherboard fit as well as electrical and thermal requirements. Future technologies will require complex, thin packages to electrically connect the boards and other components and with the ability to protect them from stresses, moisture, and other environmental stresses and cost effectively. ERM including nanomaterials, macromolecules, and complex metal oxides may provide solutions to these future requirements, but they must overcome a number of challenges identified in Table ERM14. (3D package and system in package overlap with interconnects).

Table ERM14 Assembly and Packaging ERM Challenges

8.1. MATERIALS FOR PACKAGE SUBSTRATE FABRICATION

8.1.1. PHOTOPATTERNABLE LOW K INTERLEVEL DIELECTRICS

There is a need for photopatternable low κ interlevel dielectrics (ILD) for package substrate fabrication. These must meet a complex set of performance requirements including loss tangent, moisture and ion resistance, have a low coefficient of thermal expansion and other properties as identified in ERM Table 14.

8.1.2. PRINTABLE ELECTRICAL INTERCONNECT MATERIALS

Multiple applications are emerging that require printable conductors that can be processed and made conductive and reliable at temperatures below 200°C. Applications include printable Cu conductors for package substrates, printable via fill conductors, and printable die attach materials. Each of these applications has different requirements as shown in ERM Table 14. A number of nanomaterial inks have shown promise as printable conductors; however, each has significant challenges that must be overcome to be applicable to the applications. Several commercial nanoAg inks have melting points in the range of 200°C and claim resistivities of ~2.5 μΩ-cm; however cost may be a problem for some applications. Several commercial nanoCu inks have been reported with resistivities of 3.4-7 μΩ-cm; however, to prevent the Cu nanoparticle from corroding the NanoCu particles must be coated with a thin protective layer that breaks down at high temperatures and allows the NanoCu particles to fuse. In research, 100nm diameter $Cu(OH)_2$ particles[1] were reduced to Cu conductors with a resistivity of 5 μΩ-cm after annealing at 250°C for 60 minutes. NanoCu has significant challenges which include that they currently need to be processed in an inert environment, often have process temperatures above 200°C, and have higher than desired resistivities.

8.1.3. DECOUPLING CAPACITOR MATERIALS

High speed, high power density capacitors are needed for power isolation in high performance logic. Future power isolation capacitors need to work at GHz frequencies and deliver high amounts of current quickly. Materials needed to support this are high dielectric constant materials with low electrical leakage, low resistance interconnects, and fabrication of the structure with a small spacing between the electrodes. The highest dielectric constant materials are complex metal oxides which are discussed in the Device Materials Section and have challenges with cation and oxygen vacancies reducing reliability. Potential options would be to use directed self-assembly of the electrode materials and the high dielectric constant capacitors, but this would require the materials to also have low defect densities when integrated.

To support fabricating decoupling capacitors on substrates or in embedded layers of multi-chip packages, new high dielectric constant materials ($\kappa \geq 40$) are needed that can be processed below 200°C. These capacitor materials have low leakage, high breakdown fields and be photodefinable, as described in more detail in ERM Table 14. A serious challenge is to identify a high κ dielectric with a low leakage current, because the higher dielectric constant materials also have relatively small bandgaps[2] (e.g. TiO2 Eg~3.5eV). One possible approach to achieving low leakage is to insert a thin high bandgap insulating material between the electrodes and the high κ material[3]; however, this adds significant process complexity for a package process.

8.2. PACKAGE ASSEMBLY MATERIALS

8.2.1. MATERIALS FOR 3D INTERCONNECTS AND MORE THAN MOORE APPLICATIONS

3D interconnects need solders and polymeric materials to support thermal hierarchy within die, motherboard assembly as well as the reliability requirements to enable 3D stacked packages at small form factors and z-heights with good reliability. Nanocomposite based solders and conductive adhesives will be detailed in this section.

More than Moore based products will require assembly of materials and components with extremely different properties and requirements. Thus, materials will be needed in assembly that provide compliant interfaces between components, but also manage stress, thermal heat generation, electrical interconnection, electrical isolation, and potential EMI interference between components.

8.2.1.1. MATERIALS FOR LOW TEMPERATURE AND HIERARCHICAL ASSEMBLY

To support assembly of "system on a package" and high performance flip chip packages a hierarchy of lower assembly temperature solders is needed to minimize thermo-mechanical stresses in the package. For system in a package, lower melting point solders are needed to initially mount components and keep them mechanically in place when other components are attached and alloyed with all solder joints form high reliability joints on a final cure. The initial low temperature solder joints need to provide mechanical strength through the following higher temperature reflow operations. For high performance flip chip packages, lower temperature assembly is needed to reduce stress thermal expansion stress. The move to Pb-free electronic packaging, has resulted in the use of higher melting point (>30ºC higher) Pb-free solders, such as those based on the Sn-Ag-Cu (SAC) family, and these have higher mechanical modulus and lower wettability to common surface finishes. Due to the higher melting point and higher mechanical modulus of these solders, this increases the thermo-mechanical stresses in the package. Key emerging research challenges are to identify novel interconnect materials that exhibit potential for addressing these issues, associated with SAC alloys, and provide for lower temperature and stress electronic packaging processes. A few novel materials have been identified, including nano-solders based on Pb-free alloys and electrically conductive adhesives. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements.

For lower temperature flip chip assembly other options under investigation include: Conventional low temperature soldering using the Sn-Bi or Sn-In family of alloys, flip-chip packaging with all-copper connections to replace soldered copper interconnects[4], and carbon nanotube based first level interconnections. Each of these potential options faces significant challenges. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements.

8.2.1.2. NANOPARTICLE BASED SOLDER

In the past two years, significant progress has been made in demonstrating Cu nanosolders that form strong joints at temperatures below 200°C[5]. The Cu nanoparticles have a primary particle size of 1-2nm with a surfactant passivation that is stable in air for at least 24 hours. The Cu nanoparticles form agglomerates that are on the order of 1 µm diameter and grow Cu films with grains as large as 5 µm. This is a significant improvement over previous work where the nanoparticles would fuse into a "frit" like structure rather than a Cu grain structure. More work is needed to understand

the mechanical properties of the Cu solder joints and control these properties. There is clearly more work needed to make this a viable technology, but it appears to be promising and may transition out of materials research.

8.2.1.3. ELECTRICALLY CONDUCTIVE ADHESIVES

Electrically conductive adhesives (or ECAs) represent another family of emerging research material under consideration for low temperature assembly. ECAs contain metallic nano-fillers, typically Ag and Ni flakes, embedded in an epoxy or silicone matrix.[6] These embedded materials can be cured at much lower temperatures than solder reflow temperatures, ~175ºC, between the two surfaces requiring the interconnection. Key challenges for implementing isotropic or anisotropic ECAs include: Unstable contact resistance due to the rapid oxidation of the nano-fillers, due to formation of metal hydroxide or oxide on the nano-flake surfaces during aging, poor impact performance, lower electrical and thermal conductivity, poor current carrying capability, and metal migration compared to Pb-free solders. Additionally, materials innovation is needed to improve drop strength, (improved polymer adhesion), electro-migration resistance, integration compatibility that enables a scalable, reliable package level interconnection technology.

8.2.1.4. LOCALIZED HEATING USING MAGNETIC NANOCOMPOSITE SOLDER

Conventional techniques for making first (between silicon and package-FLI) and second level (package and motherboard-SLI) interconnects for electronic packaging involves the use of multi-zone convection or infrared ovens to cause solder (at the FLI or SLI interface) to melt and form interconnects. In this scenario, the entire stack-up (silicon+ package for FLI; silicon+ package+ motherboard (along with other discrete components) for SLI) is subjected to the high temperatures for an extended period of time required for the solder melting. Although this has the benefits of high throughput in high volume manufacturing, the disadvantage is that the stack-up is subject to high thermal stresses and induced warpage, which may lead to reliability issues. This issue has been exacerbated due to the adoption of Pb-free solders like SAC305, which typically have a higher melting point (~230-240°C) and longer reflow window.

Localized heating of interconnects can help alleviate these stresses by focusing the heat only to the regions that need to be processed. Localized heating is possible in conductors subject to AC magnetic fields by Joule heating from induced eddy currents. However, for micro-sized solders used in semiconductor packaging, losses due to eddy currents are negligible and do not contribute significant heating at reasonable AC fields. Also, eddy currents can also potentially heat up package metallic traces, which is not desirable. Magnetic materials when subjected to an AC magnetic field, can also dissipate energy via hysteretic (due to irreversible magnetization) and relaxation (due to thermal relaxation of magnetic moment) processes. These magnetic losses, unlike eddy current loss, can result in significant power loss within magnetic materials even down to sub-micron and nano-sized particles. A new class of solder composites[7],magnetic nanoparticle-solder composites, have shown the feasibility of locally melting using relaxation losses in RF fields. One of the key technology challenges moving forward is to minimize the effect of package eddy current heating, while still maintaining sufficient AC fields to provide the magnetic heating required for the magnetic heating of the solder[8] composites.

8.2.1.5. UNDERFILL MATERIALS

Future underfills will need to accommodate smaller gaps between the chip and package in the first level interconnect as well as the finer pitches to enable TSV stacking. Capillary underfills will require polymers with lower viscosity in application, good wetting to multiple surfaces, low shrinkage during cure, and low CTE (10-14 ppm) post cure. Current approaches to achieving the low CTE often increase viscosity, but nanomaterials may offer the opportunity to add small amounts of fillers, and meet the CTE without increasing viscosity. Research is needed into techniques to effectively integrate nanomaterials into epoxy systems and modify CTE without degrading viscosity in application and adhesion. Alternate approaches to underfill such as wafer level adhesives need to have low CTE and good adhesion to solder, polymers and the other materials, but not shrink upon cure. Again research is needed in integrating nanomaterials that will enable low CTE, low shrinkage thermoset polymers and not interfere with solder joint formation. Key focus areas need to be on rapid curing UF systems with minimal shrinkage and minimal CTE without significant filler loading to enable the tight pitches associated with 3D stacked configurations.

8.2.1.6. ADHESIVES

For wafer or die level and stacked chip packaging, adhesives are needed to provide a stress absorbing attachment between silicon and other die materials, and exhibit a low shrinkage. Also, the adhesive must have low CTE, low modulus and low dielectric constant and in some cases a high lateral thermal conductivity. Again, research is needed to integrate nanomaterials into thermoset polymers to independently modulate mechanical, thermal and moisture absorbance.

8.2.1.7. THERMAL INTERFACE MATERIALS

There is a critical need for thermal interface materials to spread heat from logic components and spread heat between chips in multi-chip packages such as system in package. For extreme microprocessor applications, it is possible to solder

the integrated circuit to a copper heat sink; however, for other applications a flexible polymer based material with thermally conductive electrically insulating fillers are more appropriate. Since many thermal interface materials are currently using boron nitride fillers, which are the most cost effective material with high thermal conductivity and electrical insulating properties, the question is "How can the effective thermal conductivity be further improved?". Two options to improve effective thermal conductivity of filled polymer thermal interface materials are to 1) reduce the interface thermal resistances and 2) use polymers with higher thermal conductivity.

8.2.1.8. INCREASING THERMAL INTERFACE CONDUCTIVITY

The thermal conductivity of an interface depends on the strength of bonding between the materials, interface roughness and intermaterial contact area. It has been shown that Au with van der Waals bonding (CH_3) had an interface thermal conductance of 36 MW/m^2 K while the interface conductance increased to 65 MW/m^2 K when covalent bonding or charge transfer occurred (Au-SH)[9]. It was also found that the bond strength and interface thermal conductivity increased linearly with the percentage of "covalent" bonds vs. van der Waals[9]. Furthermore, thermal conductivity of sputter deposited Au on SiO2 or Al2O3 had an interfacial thermal conductivity over 2X higher than Au transfer bonded to these materials[10]. For rough ridged surfaces, the interface thermal conductivity is determined by both the bonding strength and the effective contact area between the materials[11], thus rough materials will have significantly lower interfacial conductivity than smoother interfaces. It has recently been demonstrated that inserting a strongly bonding organic monolayer between Cu and SiO_2 increased the interface thermal conductivity from ~100MW/m^{2}K to over 400MW/m^{2}K[12]. This work also included a model of how the interface thermal conductance can be improved for other material combinations. This should offer opportunities to improve both the macro interfacial thermal conductivity and the micro interfacial thermal conductivity between the polymer and the fillers.

8.2.1.9. POLYMER THERMAL CONDUCTIVITY

Since many commercial thermal interface materials use high thermal conductivity fillers that are electrically insulating, polymers with high thermal conductivity and strong bonding to the fillers and good mechanical and thermal properties should be investigated. It has been demonstrated that polybenzoxazine filled with 87.5 wt. % boron nitride flakes had a thermal conductivity of 32.5 W/m-K[13]. The thermal properties of this polymer can be modified through changes in synthetic routes, so it may be possible to achieve high thermal conductivity with lower filler content. Furthermore, thermal conductivity could also be improved by functionalizing the fillers with organic molecules that bond strongly to the filler and the polymer.

8.2.1.10. MOLD COMPOUND

Molding compounds will need to support a wide range of applications from high performance stacked chips to flexible electronics, such as smart cards. With increased use of flip chip molding compounds will be needed to underfill the gap between the chip and substrate as well as encapsulating the chip, so viscosity in application and adhesion to all surfaces will be important. Innovation is also needed for materials with designed properties including flexibility to avoid cracking from bending stresses with thin silicon (with TSV), compatible CTEs between silicon and the flexible substrate, and strong adhesion to IC materials. A critical need is to develop materials and methods to block the diffusion of water and mobile ions into the molding compound. Water and mobile ions are very detrimental to the reliability of packages and products, so eliminating their absorption by the molding compound is critical. Graphene oxide and thermally reduced graphene nanofillers (0.003%[wt.]) in polyimides have been demonstrated to reduce moisture transmission by ~6X and ~20X respectively[14]. Nanoclays functionalized with urea in an epoxy matrix were found to provide improved the corrosion resistance in a 3.5%NaCl solution[15]. Although these are not using package polymers, they demonstrate that different functionalization of nanomaterials in polymers may be able enhance polymer resistance to water and ions.

8.2.1.11. EMI SHIELDING MATERIALS

Many components in packages will need to be shielded from electromagnetic interference (EMI), so thin conductive films will need to be integrated into the package and require low temperature processing (<200°C). Potential options include nanoinks, multilayer graphene[16], and carbon nanotube composites[17]. Three monolayers of graphene were found to have an EMI shielding effectiveness of 7dB[16], while a graphene-Fe_3O_4 PEDOT nanocomposite had an effectiveness of 22dB[18] and a functionalized graphene-PVDF foam[19] had a shielding effectiveness of 18-20dB. Single walled carbon nanotubes (SWCNT) dispersed in a reactive ethylene terpolymer (RET) had an EMI shielding effectiveness of 30dB with 4.5 volume percent SWCNT[17]. So, while these materials are promising, significant work is needed to improve EMI effectiveness while providing other required properties.

8.2.1.12. ZERO RESIDUE ADHESIVES

Sacrificial adhesives are used in multiple applications such as wafer thinning, dicing tapes, carrier wafers, etc.; however, considerable effort can be expended to remove adhesive residue prior to the next operation. Depending on the application, the adhesive can be applied as a dry film or by spin coating onto the wafer or carrier. It would be desirable to have a zero residue release process that can be activated through exposure to heat, UV radiation, or safe solvent; however, a thin residue may be acceptable if it integrates into the next process step. Potential release mechanisms that have been demonstrated in adhesive polymers, include photoacid generation, photoactive fuses in "click" chemistry links, and thermal decomposition of polymers.

8.2.1.12.1. THERMAL DECOMPOSITION OF ADHESIVES

Two approaches have been explored to enable thermal release of polymer are use of polymers that thermally decompose and adding a photoacid generator to a polymer to reduce the decomposition temperature. Polymers such as polypropylene carbonate (PPC) decomposes at 210°C into CO_2 and acetone, Polyethylene carbonate (PEC) decomposes at 180°C into soluble materials that must be dissolved[20]. PEC and PPC were found to freely release after heating above their decomposition temperature; however, after heating PCC and PCC/PPC required significant force for release and left significant residue on the surface[20]. The addition of a photo-acid generator (PAG) can reduce the decomposition temperature and also make the decomposition temperature photoactivated[21]. It was found that small amounts of Cu(I) impurities interacted with iodonium-based PAGs and raised the decomposition temperature, while the Cu ions didn't affect the interaction of the sulfonium based PAGs[21]. Thus, polymer and PAG must be evaluated with materials they will be contacting.

8.2.1.12.2. PHOTORELEASEABLE ADHESIVES AND POLYMERS

Photorelease properties have been integrated in polymer adhesives through integrating photoactive links in polymers and adding photoacid (PAG) into the polymer. Poly(siloxane imides) containing photo-active cyclobutane diimide and PDMS blocks released from surfaces upon exposure to 250nm UV radiation[22]; however, residue was not measured on the surface. Experiments with photoimagable PAG loaded polymers indicated that the PAG contributed significant residue to the silicon wafer surface; however, if the PAG were restricted to the top of the polymer layer the residue was significantly reduced[23]. So while residue has been reduced, it needs significant improvement to enable clean release of wafers after processing.

8.3. POLYMER MATERIALS FOR FUTURE PACKAGING

Polymers are used in a wide number of assembly and packaging applications including as adhesives for a wide range of applications, underfill materials, molding compound, thermal interface materials, and others. These polymers must protect the integrated circuit and interconnects from mechanical, thermal, and environmental stresses while providing the required functional performance through the life of the product. It is critical that materials be developed that block diffusion of water into the package and make it immune to mobile ions. In addition, these materials must have one set of properties during application, a different set in process, and then the final product properties. Unfortunately, many of the properties are coupled with current materials, so adding a material to change one property often has a detrimental effect on other properties. A critical challenge is to identify materials additives that can modify polymer properties independently.

8.3.1. PACKAGE POLYMER PROPERTIES

New packaging related polymers are needed to meet the requirements of future technologies. For most applications, these polymers primarily serve as an adhesive layer that provides moisture protection and mechanical properties including coefficient of thermal expansion (CTE), modulus, fracture toughness, compressibility for manufacturing friendliness and adhesion to other materials. Additionally, it also must provide application specific properties such as dielectric constant, for high κ and low κ applications, electrical resistance, and thermal/ electrical conductivity. If low thermal resistance is required for a composite polymer, the interfacial thermal resistance between the thermal conducting materials and the other materials interfacing to the polymer must be very low.

For wafer or die level and stacked chip packaging, adhesives are needed to provide a stress absorbing attachment between silicon and other die materials, and exhibit a low shrinkage, low CTE, low modulus and low dielectric constant and in some cases has a high lateral thermal conductivity. Again, research is needed to integrate nanomaterials into thermoset polymers to independently modulate mechanical, thermal and moisture absorbance.

Nanotechnology is proposed to provide benefit in terms of multi-functional nano-composites, with simultaneous and step-function improvements in properties and novel property modifications.[24] Such composites may find potential applications in future mold compounds, under-fills, or die attach materials. Decreasing particle size helps to lower the composite CTE.[25]Another benefit of nano-composites is their potential for decoupling stiffness and toughness. However, persistent

challenges with processing and dispersion (intercalation-delamination, phase separation, viscosity increase) remain barriers to nanocomposites realizing their full potential. Filler surface chemistries, such as: epoxy, acids, amines, and siloxanes onto silica-like fillers can play crucial role in achieving in matrix filler intercalation and dispersion. Once the fillers are well dispersed and intercalated (bonded) with the matrix, they act as temporary cross linkers during deformation, thereby improving toughness and preventing or diverting cracks. If well bonded, the fillers may move with the polymer chains during deformation. Novel ideas on filler surface chemistries have recently been proposed and researched by many companies/academia[26]. While the resulting nano-composites express only a marginal increase in modulus, they also exhibit a significant increase in toughness, with lower CTE. The addition of oxide fillers has shown increase in composite surface energy, thereby improving adhesion. However, research is needed to understand the fundamental factors that enable this improvement in adhesion.[27] The grand challenge, as identified in the 2011 ITRS ERM chapter, is the concurrent requirements of achieving low CTE, low modulus, high fracture toughness, high adhesion, and lower moisture absorption.

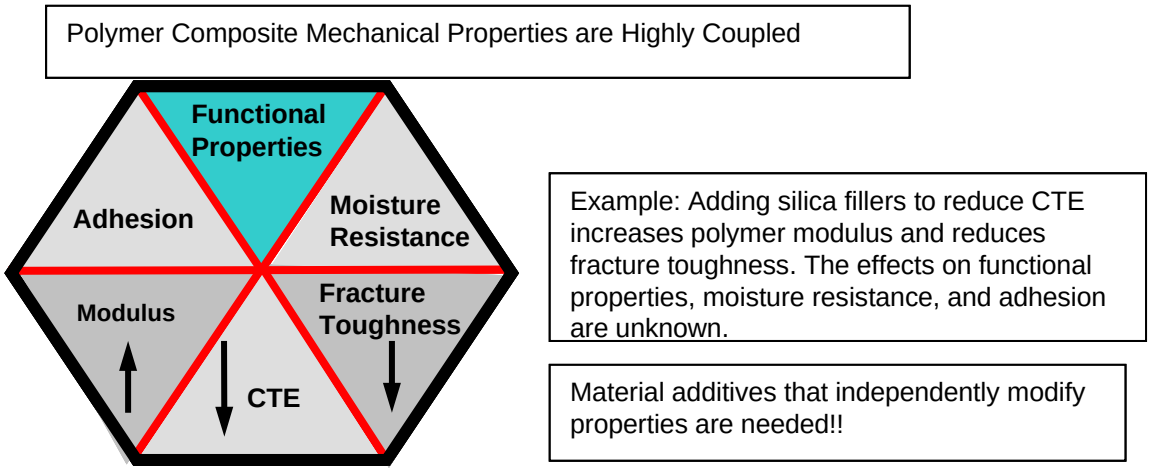

Figure ERM4 Complex Coupling of Polymer Properties

Package polymers must simultaneously meet mechanical and moisture resistance requirements and functional properties such as resistance, dielectric constant, thermal conductivity. In current approaches, the properties are highly coupled so addition of fillers to decrease CTE is often detrimental to the other properties. Research is needed to determine whether nanomaterials can be added into the polymers to independently modulate many of these properties.

8.4. Low Dimensional Materials For Future Packaging

8.4.1. Nanotube Interconnects

The 2007 ITRS ERM chapter introduced low-dimensional materials, such as carbon nanotubes, as potential candidate materials for electro-migration resistant chip interconnects. However, several key challenges were identified for these materials, such as: 1) Packaging compatible assembly processes; 2) demonstrating the required electrical resistance and reliability, including interface electro-migration, and 3) low assembly cost.

While the challenges remain daunting, research is underway to explore two potentially packaging compatible nanotube assembly methods, which include: 1) *in situ* low temperature (< 300°C) nanotube growth, or 2) remote synthesis of nanotube arrays, which are subsequently transfer to substrate. In the first approach, growth temperatures as low as 350-500°C have been reported.[28] The second approach has demonstrated an increase in MWCNT density to 50% of the theoretical value [29], and been successful at transferring CNT bumps to a package [30].

A critical challenge is the high contact resistance associated with nanotubes. Certain metals, such as Pd, Rh are known to lower contact resistance with nanotubes, by matching of work functions.[31] Modeling reports[32] suggest that high nanotube densities must be achieved to satisfy the projected contact resistance requirements. Thus, future efforts need to be geared towards growth of high density nanotube arrays, with low contact resistance metal contacts.

Graphene based interconnects are an interesting technology being investigated for silicon interconnects[33]; however there doesn't seem to exist a need for graphene interconnects for package level interconnects for the next few years.

8.4.2. NANOTUBES FOR PACKAGE THERMAL MANAGEMENT

The 2007 ITRS ERM chapter also introduced nanotubes and other low dimensional materials as potential thermal management candidates for future package applications. The intrinsic high thermal conductivity of nanotubes justifies their consideration as potential candidates for thermal interface materials. The key challenges that must be overcome for this material to be viable include: 1) Lower thermal contact interface resistance and 2) a high density of nanotubes that provide a direct thermal path between the heat source and the heat sink. Nanotube density and adhesion with Si or Silicon dioxide, through a metallic interface, needs to be optimized for the best thermal performance.

3D packaging also needs to have thermally conducting polymers between some of the chips to spread heat and minimize local heating of the adjacent integrated circuits or memory arrays. Thus, in this application, incorporating CNTs in high density laterally in a polymer is important. The polymer must also have good adhesion to the components and low modulus and low coefficient of thermal expansion.

8.5. ADVANCED THERMOELECTRIC NANOMATERIALS FOR PACKAGE THERMAL MANAGEMENT

Thermoelectric cooling offers the potential for satisfying projected thermal management requirements of advanced semiconductor packages. The thermoelectric cooling ability is estimated by the non-dimensional figure of merit ZT that has hovered below 1 until recently when a spike has been seen in semiconductor nanostructures.[34] Values of ~1.3-1.6 have been reported for PbSeTe/PbTe quantum dot superlattices.[35] The highest reported ZT (~2.4) so far has been in nanostructured thin-film superlattices of Bi_2Te_3 and Sb_2Te_3[36] and devices based on these systems were recently demonstrated.[37] While these new nanomaterials show some promise for enabling extensible thermal management of semiconductor packages significant challenges remain. These include contact parasitics that emerge whenever a device is fabricated and which severely degrade the intrinsic cooling potential of these nanomaterials.

9. ENVIRONMENT, SAFETY, AND HEALTH

Over the past decade, the introduction of new materials has enabled the semiconductor industry to continue increasing the density of transistors, increasing information processing performance and energy efficiency through "equivalent scaling. Examples of these enhancements include the introduction of Cu and low κ interconnects to increase interconnect speed and to reduce energy losses and the introduction of high κ gate dielectric materials with new gate electrodes to extend transistor performance and increase energy efficiency. The introduction of these new materials into the integrated circuit also required the use of multiple new materials in the manufacturing process. The semiconductor industry faces many significant challenges to continue delivering higher density, more energy efficient, higher functionality technologies in the future and very few material options could provide solutions. Since the difficulty of introducing a new material into a technology is high, the new material would need to provide a significant performance and energy efficiency advantage over evolutionary approaches. However, in some cases all of the options have known hazards or unknown toxicological behavior. In cases where a new material can provide a compelling societal benefit and toxicological behavior is unknown, the need for research to characterize potential acute toxicity and chronic effects will be highlighted. As the materials become more viable as technology options, our industry needs to better understand technical and ESH properties and behavior so mitigation and management strategies can be developed. Study on toxicological behavior of emerging materials is steadily progressing, and needs to be pursued in parallel with material research and development. Technological demand will make speed of development of new material and finding new use of conventional material even faster. Information on the potential environmental health and safety properties of new materials will be needed by the semiconductor industry, material suppliers, and many other industries. Data on the potential biotoxicity of new materials should be shared with all stakeholders in multiple industries and sectors through a common database. This information would be needed to properly manage manufacturing and products through their lifecycle. A more comprehensive sustainable approach should include capacity building of researchers, risk management strategy, and life cycle assessment of emerging materials for managing ESH issues. Such an approach would benefit from a more fundamental understanding and modeling of the interdependence and trade-offs between cost, performance, and ESH impact, which would enhance the timely development, qualification, and integration of emerging high performance green and sustainable materials and processes into high volume manufacturing, while lowering associated environmental and health risks.

To identifying when new materials are becoming more viable for providing solutions, the earliest potential insertion timing table (ERM 15) has been developed in collaboration with the other technology work groups. The goal of this table

is to highlight when research is needed to identify potential hazards for new materials and structures. As can be seen in Table ERM15, earliest potential times vary greatly depending on the application with potential applications in 3-5 years for carbon and metal nanotubes, oxide nanoparticles, macromolecules, and self assembled materials. Assembly and Packaging also has potential applications for carbon and metal nanotubes in this timeframe in embedded applications. Oxide nanoparticles may have application as package polymer additives in Assembly and Packaging. Metal nanoparticles may have potential applications as nanosolders to provide lower melting point solders for attaching chips to packages or other chips; however, after assembly, processing these materials would be converted into "bulk" materials. Novel macromolecules have potential for application in process chemicals and photoresist in Lithography. Self assembled materials could also be used in embedded package applications to provide high energy density capacitors. These are viewed as the potential earliest insertion times for the ERM and the longer term applications are described in the appropriate sections of this chapter. This table will be updated in future ERM Roadmaps.

In cases where the potential hazards of ERM are unknown, the ITRS encourages researchers to use conservative handling procedures to limit exposure of workers and the environment.

Table ERM15 ITWG Earliest Potential ERM Insertion Opportunity Matrix

10. METROLOGY

Metrology is needed to characterize the composition, properties, and the three-dimensional (3D) structure of emerging research materials (ERM), at nanometer dimensions and below. Also needed are non-destructive methods for characterizing embedded materials, interfaces, and defects, as well as platforms that enable the simultaneous measurement of complex nanoscopic properties. Among the many high level challenges is the need to monitor local variation at nanoscale dimensions while providing this information across a large area such as across a 450 mm wafer. As the dimensions of a material start to approach those of its phonon mean free path, thermal properties can start to be divergent from their bulk or thin film form. Thus, the Metrology Roadmap continues to emphasize the need to link modeling and simulation studies with metrology to help bridge the gap between nanoscale characterization and metrology capable of monitoring properties across a large area. This bridging effort will require valid nanoscale materials property values for use in metrology models. This is not a trivial matter; it seems that both carrier and phonon confinement impact numerous properties including dielectric function (complex refractive index), carrier mobility, thermal transport, etc., at the nano-scale. As an illustrative example, the optical properties of the top layer of SOI depend on the thickness of the film thickness below 10 nm. Furthermore, recent data show that measured properties for such films also depend on the properties of layers deposited above the top SOI film. This dimensional and materials stack dependence points to the need for developing validated databases of nanoscale material properties for critical thin film stack combination.

Table ERM16 Metrology Challenges and Needs Table

10.1. CHARACTERIZATION AND IMAGING OF NANO-SCALE STRUCTURES AND COMPOSITION

To enable fundamental understanding and improvement of new materials for integration into nanometer scale structures, metrology is needed to characterize the atomic structure and composition of a wide range of complex materials. These materials include III-V semiconductors, low atomic weight (z) materials such as carbon nanotubes, 2-dimensional materials such as graphene, boron nitride, MoS_2, etc. Additionally, nanostructured materials such as nanowires with multiple compounds, dielectrics, metal interconnects, spin materials including dilute magnetic semiconductors, complex metal oxides and doped transition metal oxides also require metrology for their characterization. Nondestructive in-situ measurement methods that offer real time characterization of material nanostructure, composition and orientation, while also allowing for correlation to macro properties are also needed. For example, there is a need for precise doping control, as a few misplaced dopant atoms can induce significant variability in the device performance of nanoscale circuits and systems. Furthermore, the research work on emerging materials could benefit from the standardization of electrical characterization methodologies to enable direct comparison of the data from various laboratories. Some attempt has been made in this regards, but more work is needed.[1]

10.2. METROLOGY NEEDS FOR INTERFACES AND EMBEDDED NANO-STRUCTURES

The emerging research materials (ERMs) will be integrated with other materials and will form interfaces. The resultant nanostructures, as with those incorporating nanoporous materials and ultrathin barrier layers, will be dominated by such

interfaces. Thus, the understanding and the control of the atomic structure, composition, bonding, defects, stress, and their effects on nanoscopic properties at these interfaces is critical. Progress has been made towards nondestructive characterization of structural and electronic properties of buried interfaces, embedded contacts and other heterostructures. For example, visible-ultraviolet internal photoemission has been leveraged to measure the energy band offset of heterojunction profiles and to determine the band alignment for materials combinations, such as those of interest in tunnel field-effect transistors[2]. Scanning microwave probe methods can distinguish changes in conductivity of buried layers as well as surface layers[3,4]. However, further progress is needed as current techniques for sub-surface / buried interface imaging and measurements are destructive, cumbersome or complicated, but marginally adequate for the prerequisite understanding of interface phenomena. The challenge of understanding environmentally sensitive properties requires the development and application of appropriate nondestructive three dimensional (3D) characterization tools and methods. 3D metrology of the atomic architecture, as well as the polarization and electronic states at interfaces will enhance our understanding of the impact and contributions of interface states to observed device performance. As alternate state variables are explored for beyond CMOS, there is a need for correlated, multimodal microscopies to maximize information return from nanoscale objects and interfaces. Finally, modeling is needed to separate the probe-specimen interactions to determine the unperturbed interface structure and properties.

10.3. CHARACTERIZATION OF VACANCIES AND DEFECTS IN NANO-SCALE STRUCTURES

The properties of most nanostructured materials are dramatically affected by small concentrations of vacancies and defects. Some progress has been made toward the ability to accurately map vacancies, defects, dopant atoms, and interface structures in 3D, but further work is needed to enable future emerging device options. When interfaces are formed between materials, bonds can be broken, defects are generated and they diffuse into the structure. Illustratively, in the case of graphene and carbon nanotubes, a local C-H bond or missing carbon atom can change the electronic properties of the system. Alternatively, functionalization also can result in the formation of vacancies, or rehybridization of the carbon that introduces states in the gap. Such material perturbations can dramatically change these materials' electronic or thermal properties. For the selective growth of III-V devices, characterization of dislocations and anti-phase domains required use of SEM, TEM, XRD, and Photoluminescence[5]. Complex metal oxide properties, including electrical, ferroelectric, and ferromagnetic, are also strongly affected by the presence and location of oxygen vacancies, since they create local distortions of the crystal structure that can break symmetry and induce different and uncontrolled electronic states. In complex metal oxide heterointerfaces, the interface carrier concentration can be changed by the presence of oxygen vacancies. Recently, by combining polarized neutron reflectometry, magnetometry, crystallography and modeling, the precise values of oxygen-vacancy concentrations in Europium oxide (EuO) thin films have been measured. The results suggest that electron doping mediates ferromagnetic interaction leading to an increase in ordering temperature[6]. Process induced defects and microstructure of individual nano-magnetic tunnel junctions (MJTs) have been correlated with the transport properties. A unique set of defects and microstructure can be correlated to transport properties, including energy barrier, from individual nano-magnetic tunnel junction (MTJ) devices. The challenge will be to detect the positions of small concentrations of vacancies and defects in nanometer scale structures. In addition to the identified need for developing enhanced microscopy capabilities, other physical measurement methods also should be improved so that the relationship between defects and properties can be measured, quantified, and understood.

10.4. METROLOGY FOR MONOLAYER CONFORMAL AND DETERMINISTIC DOPING[7-11]

Metrology for deterministic doping is required to confirm the presence, placement, and electronic state of individual dopants. Metrology needs for conformal doping span the continuum and atomistic regimes. Established continuum techniques, such as scanning probe based four-point probe, secondary ion mass spectroscopy (SIMS), and spreading resistance profiling (SRP), are still useful for characterizing ultra-shallow junctions formed by conformal doping. Ultra-shallow junction imaging techniques, i.e., scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM), are also available.

For devices whose properties depend on the position of the atoms in the channel, the device electrical characteristics are themselves a useful metrology tool. A few metrology tools sensitive to single dopants are well developed. Single dopants can be imaged with scanning tunneling microscopy (STM) and low-temperature frequency-modulated Kelvin force microscopy (FM-KFM). Direct observation of electron injection in individual dopants is conducted by KFM at low and room temperatures. Low temperatures to limit thermally-activated carriers and ultra-high vacuum to preserve the surface quality are essential. For the STM technique, sensitivity is limited to the first 2 or 3 atomic layers. Atom probe tomography (APT) / local electron atom probe (LEAP) can provide detailed three-dimensional atomic level images of the positions of all the atoms in the device. Current detection sensitivity is about 50%, limiting minimum dopant concentration sensitivity to around 5×10^{18} cm^{-3}. On the horizon, various implementations of scanning microwave microscopy (combining microwave measurements with atomic force microscopy (AFM)) and scanning probe based

electron spin resonance (ESR) are emerging. These techniques may provide single dopant and defect detection with improved subsurface imaging capability.

APT has high spatial resolution in 3D (X, Y: ~0.5 nm, Z: ~0.2 nm), high analytical sensitivity (~10 atomic parts per million), and equal detection efficiency for all elements. All of these capabilities make it an attractive valuable tool for not only basic physical properties in semiconductor materials, but also for elemental analysis in the devices. These information obtained by APT can further contribute to the research and development of device fabrication processes. To clarify the correlation between electrical characteristics and dopant distribution in future generation devices is a key challenge requiring sensitivity down to the single atom level. Therefore, improvement of APT tools toward almost 100% detection efficiency and a noise-free detection system is necessary. Improvement of reconstruction accuracy is also necessary because information on the positions of a few dopants is important.

10.5. WAFER LEVEL MAPPING OF PROPERTIES OF NANOSCALE EMERGING RESEARCH MATERIALS (ERM)

With the introduction of novel materials, such as metal-chalcogenides (e.g., $MoSe_2$, MoS_2, WS_2, etc.) [12], h-BN and graphene nano-sheets, and methods for their formation, metrology based on non-destructive techniques are needed. Such synthetic advances depend on the reproducible production of high-quality materials, and rapid methods for characterizing the structure, purity, and properties of such samples. While some techniques, such as Raman spectroscopy, fluorescence and other spectroscopic techniques, are sensitive to the local chemical environment, alternative options are needed to support the local electronic characterization of these materials. Furthermore, robust fabrication requires an ability to map distributions, preferably in-line, of both intensive properties, such as band-gap, and extensive properties such as the interactions with the underlying substrate. Specifically, there is the need to characterize such diverse material properties as thermo-mechanical structure (atomic level, roughness, grain boundaries, strain etc.), chemical structure (bonding, 3D atomic level band structure, dangling bonds, dopants and vacancies distribution), and electrical characteristics (mobility, electrically active defects, local properties, etc.).

For example, some methods for growing graphene tend to yield varying numbers of graphene layers and samples with various defects. While spectroscopic techniques have distinguished between graphene monolayers, bilayers, and bulk graphite, rapid predictions of the number of 2-D layers of materials or the presence of defects are needed. Recently, annular dark-field imaging in an aberration-corrected scanning transmission electron microscope optimized for low voltage operation has been used to resolve and identify the chemical nature of every atom in monolayer hexagonal boron nitride that contains substitutional defects[13]. Initial large-area microfocal-spectroscopic ellipsometry (μ- SE) mapping of thickness and electronic properties (e.g., mobility) of epitaxial graphene grown on thick bulk-like 3C-SiC (111) layers have been reported. The large area mapping showed that the interface structure on the Si- and C- polarity of the 3C-SiC (111) differ and has a determining role for the thickness and electronic properties homogeneity of the epitaxial graphene[14].

Overall, emerging characterization methods require further advancements especially with respect to improving the balance between measurement speed, accuracy, and precision. While some of the techniques used for characterizing emerging materials are not whole-wafer based, it is important for instrument developers to start thinking about solutions that work on large samples such as 300 mm and 450 mm wafers. This will ensure that the characterization techniques are production worthy, and not affected by across wafer variations and other production issues.

10.6. METROLOGY NEEDS FOR SIMULTANEOUS SPIN AND ELECTRICAL MEASUREMENTS

Multiple beyond CMOS devices are based on control of spin as an alternate state variable, including, but not limited to, spin transfer torque magnetic random access memory (STT-MRAM), nanoscale spin transistors, spin wave devices, hybrid-ferroelectric/ magnetic structures, and other spin-based logic concepts. Spin-based devices have unique metrology challenges; the reliability and speed of STT-MRAM devices depend on magnetization dynamics which are potentially complicated dependent on device nanostructure. Thus, metrology development depends on understanding nonlinear device dynamics, coupling, and noise. Metrology is needed for spin currents and transport in multilayered / heterogeneous systems; such metrology should comprehend the facts that spin orientation is not conserved, that there are many sources and sinks and transport is 3D. Metrology for novel spin current sources Spin Hall Effect (spin currents from nonmagnetic materials) and spin Seebeck effect (spin currents driven by thermal gradients) are being developed[15]. The specific challenges for spin materials that need advanced characterization include the atomic scale imaging of domains, the dynamics of domain wall motion, the interface conditions needed for efficient and fast spin injection from ferromagnetic to semiconductor materials, and the measurement of spin transport and lifetime, etc.

Differential phase contrast (DPC) is an emerging technique to measure the intrinsic magnetic and electric fields in nanometer-sized patterned materials, such as the patterned magnetic materials for spintronics applications. DPC imaging enhances the image contrast of weakly absorbing, low-atomic-number objects in optical and X-ray microscopy. When coupled with aberration-corrected scanning transmission electron microscopy, DPC imaging affords Atomic-resolution imaging of electromagnetic fields.[16] Both the mesoscopic polarization fields within each domain and the atomic-scale electric fields induced by the individual electric dipoles within each unit cell can be sensitively detected in ferroelectric $BaTiO_3$ have been demonstrated.

10.7. INTERCONNECT MATERIAL METROLOGY

The unique metrology needs for low-k / Cu interconnects in the general areas of low-k glass structure characterization, and nanometer scale mechanical property measurements, have been previously detailed[17]. Three new interconnect metrology areas of need include methods for assessing the thermal conductivity and thermal boundary resistance of interconnect structures, zero charge imaging techniques, and methods for performing nanometer scale structure-property characterization of low-k/Cu interconnects. As the size of interconnects continues to decrease, the thickness of the Cu diffusion barriers must be reduced to minimize the impact of this layer on the interconnect resistance. Metrology and characterization capabilities are needed to determine the effectiveness of sub-2 nm novel materials in blocking the diffusion of Cu into the interlayer dielectric (ILD) and device regions. It is important to determine such variables as, the mechanisms for Cu diffusion through the barrier when they fail (i.e., pinholes vs. diffusion, etc., and diffusion coefficient, etc.), and low k-metal interface structure and bonding. For example, there is a need to understand why molybdenum (Mo)-doped Ruthenium (Ru) thin films are thermally stable up to 725 °C, whereas those of a pure Ru film fail at a lower annealing temperature of 575 °C [18].

As transistor areal densities continue to increase and stacked die 3D integration schemes are considered to drive transistor densities even higher, heat dissipation through the metal interconnect is becoming an increasingly important consideration. While 3-omega, time domain thermal reflectance (TDTR) and other related techniques have provided greatly needed engineering data on the thermal conductivity of most interconnect materials in thin film form[19], relatively little is known regarding the thermal boundary resistance (TBR) for the numerous interfaces present in low-k/Cu interconnects. The thermal resistance of these interfaces is expected to become increasingly important for < 10 nm interconnect technologies where the ratio of interface to bulk is expected to start approaching unity. Recent theoretical and experimental investigations have shown that the chemical bonding and detailed structures of interfaces can have a significant influence on TBR.[20] Therefore, new methods for efficiently characterizing the TBR of the numerous interfaces present in low-k/Cu interconnects are needed, as well as research to better understand how the processes influencing interface formation and chemical bonding influence TBR.

Also of importance is that many interesting length scale phenomena have been observed in the thermal properties of materials of interest to the semiconductor industry[21]. Specifically, as the dimensions of a material start to approach those of its phonon (or other characteristic) mean free path, thermal properties can start to be divergent from their bulk or thin film form. For these reasons, increased attention is needed for developing methods for characterizing the thermal conductivity of nanometer scale thin films in both static and stressed conditions.

Etching of low-k dielectrics with plasma or reactive ion etching produces damage in the sidewalls of the oxide which can change the dielectric properties of this material[22]. As features become smaller, the damaged region can become a larger percentage of the ILD. Metrology is needed to characterize the extent of damage in the sidewalls and determine its effect on the dielectric constant of narrow separations between electrical interconnects. A metrology area of need for low-k/Cu interconnects is zero charge based imaging techniques with resolution comparable to standard scanning electron microscopes (SEM). Aside from extreme fragility, low-k materials exhibit an acute sensitivity to imaging using common electron beam based techniques. This sensitivity typically manifests itself as film shrinkage or "melting" during imaging and is a result of both sample heating and the injected electron charge rupturing chemical bonds in the material and initiating densification reactions. Typical electron beam based imaging techniques also prohibit the imaging of surfaces and in particular corrosion layers on metal surfaces in their pristine state due to film deposition by catalyzing reactions between the surface and background contaminants in the electron beam vacuum system. Low-k film shrinkage and contaminant film deposition can be minimized by utilizing lower beam currents and voltages, but cannot be completely eliminated as a source of error or confusion in measurements of low-k critical dimensions and failure analysis. For these reasons, zero charge based imaging techniques with high resolution are highly desired. In this regard, helium neutral atom microscopy (NAM) is an extremely attractive alternative. While spatial resolutions as low as only 350 nm have been currently demonstrated[23], recent analysis has shown that spatial resolutions as low as 10 nm may be possible through readily achievable improvements in He detection efficiency and further optimization of the technique[24]. For these reasons, NAM deserves significant support and investigation as a potential low-k/Cu interconnect metrology.

Continued advancement of low-k/Cu interconnects would greatly benefit from the ability to perform local structure property measurements of interconnect materials and interfaces at nanometer scales in actual fully integrated interconnect structures. Such a capability would be most beneficial for failure analysis of low-k dielectric materials which exhibit a complex chemical structure and extreme fragility and sensitivity to patterning and metallization processes. Recent advances in atomic force microscopy (AFM) technology have provided the ability to perform thermal[25] and mechanical analysis at nanometer dimensions[26]. However, glass structure characterization techniques such as Fourier-Transform Infra-red (FTIR) spectroscopy have been limited by diffraction effects to spatial resolutions of only 3 μm to10 μm. In this regard, new AFM-IR based techniques have recently demonstrated sub diffraction limited resolutions on the order of 50 nm in polymeric materials[27]. Such techniques merit significant consideration for investigation of both low-k/Cu interconnect and other nanoelectronic structures.

As stacked die 3D integration schemes are leveraged to drive transistor densities even higher, through substrate via (TSV) has emerged as a leading technology for 3D integration schemes. Heat dissipation through the metal interconnect is becoming an increasingly important consideration. For example, thermally induced defect formation and growth, as well as embedded materials degradation, affect the reliability of TSV. Any metrology to study TSVs must be capable of detecting discontinuities due to defects and material distortions in otherwise electrically contiguous structures. Broadband RF-based measurements have been used to study / probe physical changes in TSV[28]. Another metrology challenge presented by TSVs is the physical identification of defects in the structure. The current techniques such as field ion beam (FIB), scanning electron microscopy (SEM), etc. are destructive. Thus, there is a need for non-destructive detection of defects in TSVs; X-ray microscopy / tomography appears to be an effective metrology tool in this regard[29]. Finally, the large mismatch in the coefficient of thermal expansion (CTE) between Cu TSV and the surrounding Si is known to result in reliability challenges due to stress build up. Therefore, there is a requirement for a measurement technique that can quantify the full stress tensor in TSV and the surrounding Si. Synchrotron based micro-beam X-ray diffraction technique has been used to non-destructively determine the full strain tensor in these structures as a function of depth[30].

10.8. METROLOGY NEEDS FOR COMPLEX METAL OXIDE SYSTEMS

Correlated oxide systems, such as multiferroics, have competing and coupled charge, spin, orbital and lattice degrees of freedom, and they result in the formation of new electronic and magnetic phases[31]. These materials have the potential to enable new device concepts that could couple electric and magnetic spin alignment for spin logic novel memories. It has been shown that the domain walls possess unique functionalities not inherent in the parent multifunctional material, such as being electrically conductive. For these electrically conducting interfaces to be useful, their nucleation and positioning must be understood and controlled reproducibly. Piezoforce microscopy may be useful for characterizing static and dynamic properties of ferroelectric and piezoelectric materials at the nanometer scale. The coupled phases have been found to be sensitive to cationic disorder and vacancies, so metrology is needed to characterize these and correlate them to the electric, magnetic and orbital order.

10.9. METROLOGY FOR MOLECULAR DEVICES

New metrology capabilities such as inelastic electron tunneling spectroscopy[31A], and backside FTIR[32] for the study of vibrational states, and techniques such as transition voltage spectra, STM, Conductive AFM, and Kelvin Probe AFM are beginning to enable understanding of the transport through individual molecules and molecular interfaces. However, additional research is needed to develop new metrologies, such as nondestructive, in situ 3D methods, to characterize contact interactions with molecules and the electronic properties of the embedded interfaces and molecules.

10.10. METROLOGY NEEDS FOR MACROMOLECULAR MATERIALS

New families of designed macromolecules and corresponding material characterization methods are needed to satisfy projected long term patterning requirements. For example, nanoimprint lithography (NIL) is emerging as a potential patterning solution beyond 22 nm. This technology faces several performance challenges related to the templates, release layers, and resist and imprinted functional materials. New metrologies are needed to assess projected critical materials requirements, such as pattern fidelity, distortions and defects, shear stresses and pattern collapse, adhesion and release behavior.

10.11. METROLOGY NEEDS FOR DIRECTED SELF-ASSEMBLY

For directed self-assembly (DSA) to be viable, as a lithography extension or to assemble nanostructured materials in predefined locations and alignment, metrology is needed to evaluate critical material properties, the size and location of features, and the registration to previously patterned structures. However, these sub-100 nm thick organic films are difficult to image with conventional metrology tools. For block co-polymer (BCP) based directed self-assembly to be a viable potential lithographic solution, robust non-destructive nanoscale measurement methods are needed that enable 3D

characterization critical performance factors of the phase segregated films, which include: feature sizes, line width roughness, alignment to existing structures, engineered surface energies, anneal dynamics, and defects, etc.

Characterization techniques are needed to evaluate neutral surfaces and the interfacial energy between the chemical surfaces and the polymers. This interfacial energy determines how the block copolymers assemble, but current techniques such as contact angle measurements are inadequate for determining whether a surface is neutral to both blocks of a BCP. Furthermore, these techniques are incapable of measuring interfacial energies on nanometer scale topology (especially on vertical surfaces like sidewalls) or chemical patterns. Chemical force microscopy (CFM) may be useful in this regard; however it needs to be able to probe and characterize high aspect ratio narrow trenches for graphoepitaxy. CFM utilizes target specific chemically modified AFM tips and is capable of measuring topographical and chemical differences on polymer surfaces with high resolution; however its resolution is limited by the size and shape of the probe tips due to substrate-tip interactions. Thus, current CFM may not be able to probe effectively in graphoepitaxy trenches in reasonable timeframes[33,34,35]. Research has explored the use of chemically functionalized carbon nanotubes for CFM of small features[36]; however, these are not readily available. Chemically functionalized single walled carbon nanotubes (SWCNT) have the potential to provide nm scale mapping of chemical surfaces, but this has not been developed or validated for this application. While a technique like this is needed, current CFM is basically a research tool that requires considerable interpretation by an expert. Thus, the most valuable capability may be one that determines whether surfaces are neutral to the BCP, and this may be through self-assembly of a test sample. More work is needed to make CFM easier to use and interpret.

For DSA to be a viable lithography extension technology, it must be able to achieve defect densities less than $0.01cm^{-2}$; however, detection of defects over large areas in DSA films is challenging because the films are thin and defects occur in 3D. Unlike photoresist, the block copolymers used in DSA can have defects form below the surface that are not observable from the film-air interface. Potential 3D defects in segregated films after development include thermodynamics driven voids and bridging structures between lines, as well as process induced defects (e.g., partially open structures and polymer residue). Furthermore, the block-copolymer films are thin, on the order of the feature size, so optically detecting defects will be challenging. Thus, metrology is needed to detect defects in DSA structures over large patterned areas, and to capture process-related defects such as displacements of structures, missing or added structures. Novel optical techniques should be explored that include analysis of polarization and wavelength dependence of diffraction and scattering. Sophisticated analysis techniques are needed to detect defects in 3D and misaligned patterns.

Alternative metrology techniques with required spatial resolution can't detect defects over large areas with high throughput; however, they could be useful for detailed examination of defects in small areas. Hard x-rays also afford weak scattering because of the low electron density of carbon and similar electron densities of the polymer blocks in the BCP[37]. TEM of heavy metal stained samples and inert-gas ion based microcopy (e.g., Helium or Xenon ion) may distort the polymer film. Models assisted critical dimension small angel x-ray scattering (CD-SAXS) has shown some promise with enhanced scattering being obtained with resonant soft x-rays. Initial measurements have demonstrated that 4x lamella samples have non-uniform composition with depth and position and that resonant CD-SAXS is sensitive to the 5 nm chemical template[38]. Unfortunately, the transmission-mode resonant CD-SAXS measurements require TEM-style sample preparation and are available only at specialized synchrotron beam lines. It must be noted that x-rays inherently modify organic thin films, thus CD-SAXS may be limited as a non-destructive technology. Furthermore, CD-SAXS is currently incapable of detecting non-repetitive defects. The absence of large area metrology that is compatible for use in a wafer fabrication facility could limit progress in DSA. Thus, there is the need for nondestructive high throughput techniques such as optical scatterometry.

Finally, there needs to be increased focus on higher chi X materials for smaller features, and these may potentially require neutral top surfaces as well.

10.12. MODELING AND ANALYSIS OF PROBE-SAMPLE INTERACTIONS

Nanometer scale measurement tools, such as electron microscopes or scanning or optical probes, exhibit significant coupling between the probe and sample states. Significant research is needed to develop methods for decoupling these interactions and to accurately determine nanoscopic structures and properties. Also needed are sample-probe interaction models for characterizing nanoscale structure, defect locations, composition, electronic, magnetic, and optical properties. Additionally, improved algorithms are needed to enable the extraction of actual structures and properties from the coupled signals. For example, scatterometry relies on knowledge of the optical properties of all the materials in the probed structure. Novel materials present problems because their optical properties are not well known. Furthermore, the

confined dimensions of structures can modify optical properties from their bulk behavior[39]. Thus, further research is required to characterize the optical properties of novel materials in confined geometries.

10.13. METROLOGY NEEDS FOR ULTRA-SCALED DEVICES

Emergent nanoscopic properties will introduce new failure mechanisms which will require trading device performance with reliability. Hence, new metrologies and models are needed to characterize the performance and reliability of emerging nano-scale devices. A thorough understanding of the sources of variability and their impact on device noise is critically needed for enabling the successful design and integration of emerging materials into nanoelectronics. This foundational need will drive the development of tools for identifying and characterizing the significant emergent sources of variability and noise in nanoscopic systems. There is a need to characterize and understand the aging of nano-materials and nanostructured devices, and the consequences of such aging on device performance since most of the existing data based on bulk material properties may not be applicable.

The introduction of 3D device structures, such as tri-gate structure, comes with new measurement challenges, such as physical corners and sidewall orientations that need to be accurately measured. Furthermore, the integration of the newly introduced materials, such as high-k dielectrics in combination with metal-gate stack, needs careful optimization to produce excellent reliability[40]. This requires imaging of a complex 3D structure with atomic resolution of interfaces and chemistry. Some progress has been made in this regard; for example, using aberration corrected electron energy-loss spectroscopy, two-dimensional elemental and valence-sensitive imaging at atomic resolution, of a $La_{0.7}Sr_{0.3}MnO_3/SrTiO_3$ multilayer have been demonstrated, and the data show an asymmetry between the chemical intermixing on the manganese-titanium and lanthanum-strontium sublattices[41]. For 3D interconnects, penetration of x-rays provides a major advantage to nondestructively imaging a 3D volume. For example, X-ray microscopy has been used to study 3D interconnects (TSVs); the resolution is currently limited by optics and single digit nm resolution should be reached for 3D x-ray imaging eventually. Strategically, segmentation of 3D data allows objective, quantitative analysis of complex structures[42].Further research work is needed to avoid distortions due to interactions between probes and the very thin films used.

10.14. PROGRESS OF METROLOGY FOR ERM DEVICE MATERIALS

Direct imaging and chemical identification of all the atoms in a material with unknown three-dimensional structure will significantly improve understanding of ERMs.

10.14.1. MAGNETIC TUNNEL JUNCTION (MTJ) METROLOGY

In MTJ technologies, efforts have been made to improve the characterization and understanding of the various associated phenomena. In particular, the interface structure MTJ (the tunnel insulating film MgO and magnetic film above and below the MgO) should be evaluated at the atom level.

Since the MTJ is composed of ultra-thin multilayered films, it is very difficult to analyze them in the atom scale. STEM with Cs-corrector can contribute to the investigation. By using high-resolution HAADF-STEM and EELS / EDX elemental mapping at the atomic column order, there is a possibility to solve the issues listed above. Actually, Miyajima et al. differentiated the ordered phase ($L2_1$-type) from disordered phases (B2-type) in the CoMnSi magnetic film by high-resolution HAADF-STEM observation[43]. The electron beam interferometric method combined with electron holography and Lorentz microscopy should be developed for dynamic observation of the magnetic structures[44]. 3D AP analysis enables us to obtain the atom-level element profiles in the MTJ stacked structure. These profiles will be useful for the design of MTJ and the process optimization. It is also important to chemical states of magnetic layer at Interface between MgO. Ikeda et.al reported that TMR properties depend on the element of ultra-thin CoFe films locating at the interface[45]. For the purpose of estimating the chemical states of nano-hetero-interface, STEM-EELS is promising method. Kawasaki et al reported that only Fe atoms of CoFe are oxidized and the singular lattice arrangements exists simultaneously[46].

10.14.2. REDOX RAM METROLOGY

It is indispensable to observe directly at the interface where the redox reaction plays a crucial role of the Redox-RAM's operation. It is essential to evaluate the distribution of oxygen vacancies and the change of the valence state of the metal element contained in metal oxides. The possible candidate to investigate them is STEM-EELS with Cs-correction. However, the electrode material and the metal element in the complex metal oxides currently being used are heavy metals, and EELS has poor sensitivity for such materials. In addition, HfO_2, which is a candidate of metal oxide, has been known to change the chemical state by the thinning (using ion-beam processing) prior to electron microscopy analysis and the electron beam irradiation. To find the solution to prevent the change is very important for the quantitative investigation. By the detection of soft X-ray from materials under the electron beam exposure, the electronic states (valence band density of states) of the materials can be investigated with the high sensitivity (X-ray emission

spectroscopy: XES)[47]. This technique will be the strong tool to study the Redox-RAM operation. Some progress has been made in the understanding of resistive switching; for example, hard x-ray photoelectron spectroscopy (HAXPES) has been used in the in-situ non-destructive investigation of electric field induced chemical and electronic modifications during resistive switching events in resistive RAM film stacks[48].

10.14.3. METROLOGY FOR ERM ENVIRONMENTAL SAFETY AND HEALTH

Metrology is needed to detect the presence of nanoparticles in the workplace and in the environment. Understanding nanomaterials' behavior in the workplace and environment is required to establish good risk assessment and material management practices (i.e., selecting appropriate protective equipment, ventilation equipment, etc.). Furthermore, reliable metrology is also required for evaluating the applications of ERM in the practical devices. Industrial Hygiene (IH in factories, enabling reuse and recycling) needs to be broader for ERM.

11. MODELING AND SIMULATION

With device dimensions 14 nm or below, materials modeling or computational materials is becoming a critical part of technology development and is needed to address several components of technology development[1]:

1) *Synthesis to structure & composition*, especially on the interfaces and multi-interface material structures
2) *Properties* of these structures including interface physics of state transition, defects states, etc. In addition, non-equilibrium properties of these structures such as conductance, mobility,
3) *Probe interactions* with samples to enhance quantification of structure, composition, and properties.

11.1. DEVICE MODELING AND SIMULATION CAPABILITY NEEDS

With device dimensions continuing to shrink below 14nm, every device technology needs improved modeling capabilities to evaluate operating mechanisms and to optimize device structure. The material modeling needs for different Emerging Research Devices are identified, in Table ERM17, from synthesis to prediction of properties. ERM Modeling and Simulation Needs (columns C-H) are those required to help in the viability of the device materials in a research environment. For devices that are potentially closer to industrial evaluation, the ERM has identified modeling needs for potential optimization of device structures (columns J-R).

Table ERM17 Device Material Modeling and Simulation Challenges and Needs

11.2. LITHOGRAPHY MODELING AND SIMULATION NEEDS

For Lithography material modeling, the ERM has focused on directed self assembly (DSA) with block copolymers and the modeling needs are identified in table ERM18. As industry evaluates DSA as a potential technology to extend lithography beyond 10nm, new materials will be needed modeling is needed to aid in their evaluation. Clearly, modeling is needed to evaluate the potential for new high χ materials to form defect free patterns and identify allowable variations in guide structures that can produce these. There is also a critical need for efficient computational models to be used in EDA tools to translate from design patterns to guide structures on masks that will be patterned on wafers. Multiple applications of DSA are being considered and the placement of guide structures must comprehend self assembly effects, such as guide pattern density interactions) to minimize defects in the assembled patterns. ERM Modeling and Simulation Needs (columns C-G) are those required to help in the viability of the DSA materials in a research environment. For DSA materials that are potentially closer to industrial evaluation, the ERM has identified modeling needs for potential optimization of patterning structures (columns I-M).

Table ERM18 Lithography Material Modeling and Simulation Challenges and Needs

11.3. INTERCONNECT MODELING AND SIMULATION NEEDS

Interconnects face critical challenges with needs for lower κ dielectrics, ultra-thin Cu diffusion barrier layers, and novel interconnect materials. Modeling and simulation capabilities are needed to evaluate some of the critical issues for each of these technologies and these are highlighted in table ERM19. The important capabilities required to assess viability of an interconnect material or technology in research are highlighted in columns "C-E", while the models needed to accelerate industrial process evaluation and development from an ERM perspective are shown in columns "G-K". In all phases of evaluation, modeling would need significant interaction with experiments to improve the accuracy of modeling.

Table ERM19 Interconnect Material Modeling and Simulation Challenges and Needs

11.4. MODELING AND SIMULATION CAPABILITIES

With device dimensions approaching 10 nm, atomic- scale-based materials modeling or computational materials is becoming a critical part of technology development and is needed to address several components of technology development, as illustrated below; In the absence of modeling, empirical experimentation is used to characterize and drive technology development. This process is both expensive and time consuming. More importantly, the specific operating window identified experimentally may not be globally optimal. A faster rate of learning provides compelling reasons for materials modeling as with shrinking dimensions, device performance is very much driven material properties:

1) *Synthesis to structure & composition*, especially on the interfaces and multi-interface material structures
2) *Properties* of these structures including interface physics of state transition, defects states, etc. In addition, non-equilibrium properties of these structures such as conductance, mobility,
3) *Probe and metrology interactions* with samples to enhance quantification of structure, composition, and properties.

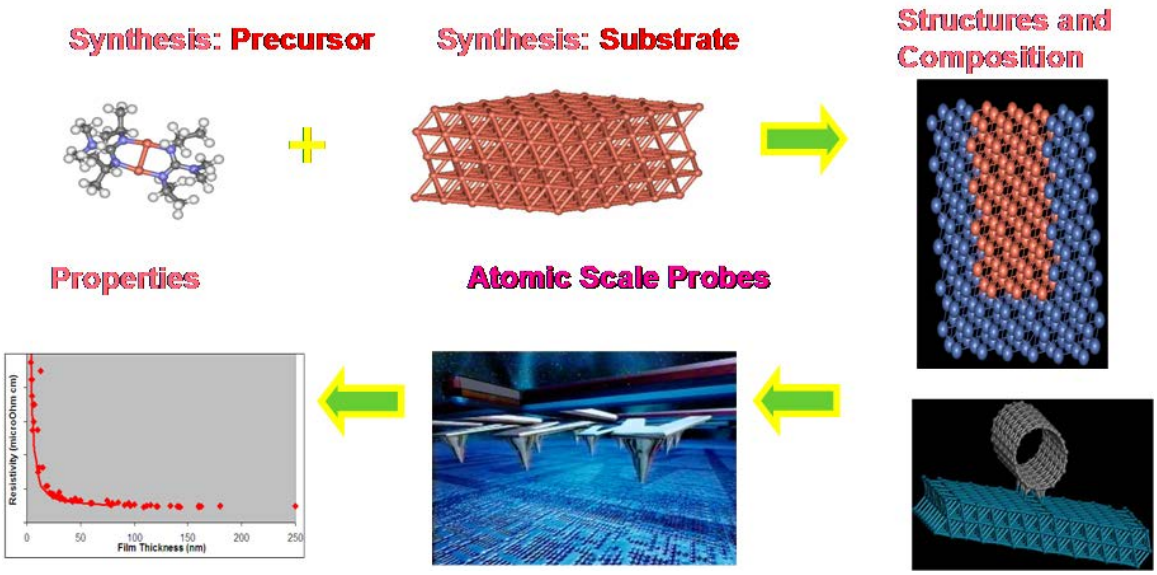

Figure ERM5 Modeling of Synthesis to Properties

Materials modeling is applied at different levels based on the accuracy and the end application requirements. All material applications require simultaneous optimization of multiple properties such as electronic, mechanical, thermal, surface chemical reactivity, etc. If the dimensions of the materials are in nanometers, they are of the same order of magnitude as the domains in the materials such as grain sizes. These lead to nanomaterials possessing unique properties making them optimal candidates to enhance or replace conventional materials and approaches. However, the need for optimization of multiple properties requires models that correlate nanostructure to properties. There are multiple stages in which materials modeling can provide value in technology development. In the *first* stage during early material development, the need is to relate structure and chemistry to desired material properties. This is done in conjunction with a specific metrology and is used to characterize both structures and their properties. In addition the models are needed to optimize synthesis and transport processes including film growth. In the *second* stage, the models are applied to material improvement where they are used to optimize structure, composition, purity, and interfaces. Here as we have mentioned above, the models relate structure and composition to properties. In the *third* stage, models are used to relate material properties to the functional properties of the device. The properties of the resulting structure needed to be understood in terms of transport of electrons, phonons, and atoms. The models at this stage in conjunction with experimental observations are used to optimize synthesis and integration.

The behavior of devices and materials are directly correlated to their electronic structure and lattice physics. This is equally valid for both charge-based and non-charge-based technologies, as physical and chemical effects in these

dimensions are directly related to the electronic structure. Physical modeling and numerical simulations are critical for multiple reasons:

1. *explain observed phenomena,*
2. *predict new phenomena,*
3. *direct experimental studies to desired outcomes,*
4. *interpret metrology.*

In addition, they provide fundamental understanding of both the mechanisms and the interactions between processes and materials.

Application of materials for ERM constitutes fundamental understanding and characterization of synthesis, structure, and properties. This is the natural logical flow for designing and integrating newer materials to develop structures whether it is for switching device, interconnects, or packaging. The method and conditions of synthesis determine the structure and composition of the engineered materials. Structure in turn, determines the material properties and performance. As can be seen in the following figure, models span multiple scales and need to be simulated using appropriate assumptions. The key intent of material simulation is to identify and quantify chemical knobs at the levels of atomic, nano, and thin film dimensions that modulate the behavior in the integrated devices.

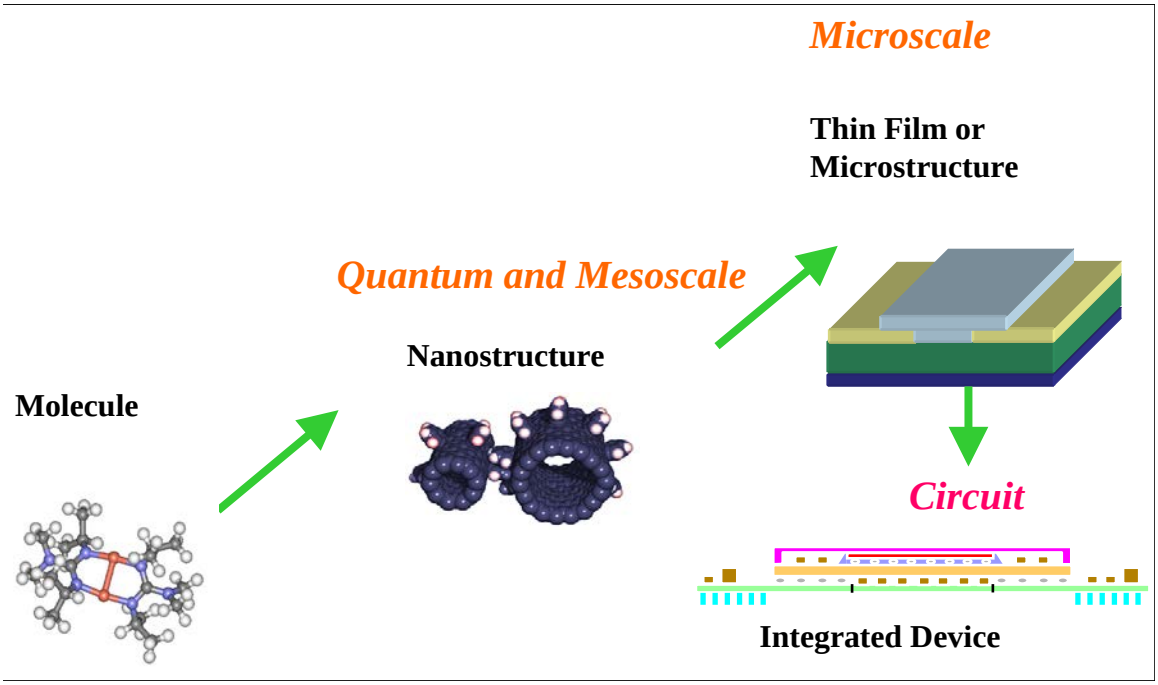

Figure ERM6 Modeling from Molecules to Circuits

The complexity of materials modeling in nano dimensions is increasing due to increasing complexity from a variety of factors.

1. *Combinatorial Nature:* Number of materials has continued to increase with the development of several new material systems including high-k/metal gate, porous dielectrics, copper interconnects, and polymer materials for packages (leading to over 3X increase in number of elements over a period of 20 years). This effect is further augmented as materials are used in combinations estimated to be increase by more than 10X in number of material combinations over the same time period as above.
2. *Nanodimensions*: Most of the devices have dimensions close to material domain sizes (e.g. grain size, thin film thickness). As a result, the \performance of the device is determined by the material properties at their characteristic dimensions. For example. Surface scattering is estimated to dominate interconnect resistivity for any metal as feature sizes are reduced to even smaller . In addition, with scaling, ratio of surface to volume leads to interface properties determining overall behavior of devices unlike the bulk properties

determined in the previous generations. In addition, smaller number of atoms in smaller dimensions leads to larger statistical variations.

3. *Topography*: For non-planar devices, topography of material structures modulates device behavior since the same single crystalline material may have multiple orientations dependent on the interfaces. This is further complicated by polycrystalline or amorphous materials with grain boundaries. These in turn lead to property variations.
4. *Topology* of the nanostructures and molecules. Electronic and phonon densities of states are determined by the chemical bonding and electronic band structures. Since the topology determines the functional properties of devices, efforts to analyze these effects are necessary both from characterization and modeling studies. For example, carbon nanotubes and graphene sheets demonstrate large conductivities and strong mechanical properties which can be affected by their orientation and topology.
5. *Correlated Properties* of strongly materials cannot be easily predicted from band theory given the nature of their interactions. This because traditional Density Functional Theory fails for these classes of materials. Another associated property is the metal-to-insulator transition. The complexity of physics is due to multiple mechanisms attributed for the transition[2].

11.4.1. SYNTHESIS

Synthesis determines the structure and composition of thin films. To predict the material properties, we need both characterization and physical modeling of the relevant structures. The materials themselves may be crystalline, poly-crystalline, semi-crystalline, amorphous, or visco-elastic. Even in bulk materials, structure of the materials determines their behavior[3]. For example, the resistivity of films in a certain crystallographic orientation (100) is different from (111) orientation. Realistic structures are not ideal single crystalline films and need advanced metrology for their complete characterization including characterization of grain morphology and size.

Materials synthesis influences the material morphology and the desired end user application. For example, nanotube growth and functionalization are determined by the chemical and electrical conditions in the reactor and the interactions with the substrate. Depending on the method of synthesis, in-situ and ex-situ requirements are different. For example, in a low pressure process, ex-situ measurement may result in oxidation and altering of the properties of the film. From a modeling perspective, a key requirement is to understand roles/mechanism of processing and the specific structure resulting from the synthesis. As an example, in atomic layer deposition, the physical model must comprehend gas phase and surface chemistry in addition to mass and energy transport. Film nucleation and subsequent growth, which determine the morphology of the nanostructure and thin films, also require modeling. In addition to description of the temporal evolution of a new phase, it becomes necessary to describe the spatial ordering in many systems (eg. quantum dots, nano-wires[4,5]. Classical nucleation and growth concepts adequately describe phase transitions in some nanoscale phase change memory materials[6].

Controlling the morphology of the nanoscopic material requires detailed information on phase stability and dynamics of atomistic processes. In small nanoscale systems in which dimensions may not be significantly larger than the range of interatomic interactions, classical thermodynamic concepts such as extensive and intensive properties may no longer be valid. In these cases, the classical concept of a phase transition, including the Gibbs Phase Rule that occurs in the thermodynamic limit of an infinitely large system, may not hold[7,8]. Development of a theory of phase transition in such finite size systems for understanding the dynamics of phase transition may be critical to control nucleation and growth of certain nanoscale materials. Description and prediction of fragmentation, a process by which phase transitions have been observed to occur in nanoscopic systems, presents a significant challenge in statistical mechanics. Density functional theory[9, 10] which is based on density fluctuations rather than existence of clusters of classical and atomistic nucleation should investigated as a tool for describing phase transitions in small systems and fragmentation. Structures characterized based on synthesis methods serve as inputs into the physical models. Given the limited size of problems that can be solved, a combination of techniques spanning different length and time scales are needed to model structures effectively.

11.4.2. STRUCTURE AND PROPERTIES

The material properties themselves are based on the electronic band structure of condensed matter. For a given structure, the Schrödinger equation determines chemical, electrical, mechanical, and thermal properties. In turn, the nature of the hyper-dimensional Schrödinger equation is determined by the number of electrons in the structure. As the number of electrons are very high in condensed matter ($\sim 10^{22}$ - 10^{23} in an unit cubic centimeter of material), any solution of the equation for realistic macroscopic system is generally done using one of two simplified techniques; 1) single particle

approximation and/or 2) multi-scale techniques with distinct formalisms representing different scales. The models themselves have different scales based on the specific physical phenomena. Atomic or molecular scale is based on self-consistent solutions of Schrödinger equation as mentioned above. Nanostructural scale uses multi-scale techniques based on kinetic and quantum formalism (e.g. device, or interconnect with barrier layers). The thin film scale (e.g. gate oxide or barrier layer) is mesoscale in nature, and links with kinetic models at the macroscopic level and atomic models at the microscopic level. In the macroscopic scale (e.g. die, package), bulk or effective properties are used in constitutive models that describe the response of materials to different stimuli. For the area of ERM, the main focus of research should be on the first three levels, with an emphasis on atomic or molecular and nanostructural scale. Since structural dimensions are currently at 32 nm or below, the materials properties at this scale may behave differently when integrated than in the bulk. In addition, optimization of the performance reliability of devices or materials in nano-dimensions during ambient and accelerated usage conditions requires model extension to include phonon interactions and other long time scale processes. More details of the other scales are covered in the Modeling and Simulation section in the roadmap.

The most widely used technique is the Density Functional Theory (DFT) in which the 3N dimensional system is reduced to three dimensional problems for most of the ground state problems[11,12]. The approximations are generally of two types, one in which the density functions are systematically improved to capture more and more non-local features of the wave functions and the second one in which the exchange-correlation functional are approximated by analytical models (e.g. meta functionals). One of the most widely used approximations is the Local Density Approximation (LDA)[13] where local densities of N-1 electrons are used to approximate the interaction potentials leading to a 3 dimensional problem. More accurate approximations such as Generalized Gradient Approximations (GGA)[14,15] are used to increase the applicability of the DFT methods. Yet the transferability of the exchange-correlation functional is a critical issue for application to variety of materials.

Most of the full quantum simulations or *ab-initio* simulations can be done for smaller systems up to 1000-5000 atoms, which are approximately about 30 cubic nanometers. The models which cover these domains are mostly based on quantum methods which solve Schrödinger equation in 3N dimensions, where N is the number of electrons in the system. As mentioned above, most of the devices are in condensed matter, N is of the order of 10^{22}. Different methods scale depending on the number of electrons or basis sets used in the approximation; $O(N^3)$ for Density Functional Theory, $O(N^4)$ for Hartree-Fock (N being the number of basis functions), $O(N^7)$ for some coupled cluster calculations. This poses the problem in solvability of the equations for practical applications in both the chemistry (needed for synthesis) and materials analysis. Efficient algorithms for large-scale quantum-mechanical calculations with aid of parallel computing technology are developing[16].

In addition, for materials, due to the complex properties (e.g. Mott transition, spin-orbital coupling), many-body theories are entering mainstream in applications[17-20]. Some examples of these higher-order approximation techniques are Green's Function techniques (GW), Quantum Monte Carlo, Path Integral methods etc. These techniques model both the equilibrium and non-equilibrium properties without mean field approximations as mentioned above. The first technique uses perturbation technique to comprehend many-body interactions in a self-consistent manner. The other techniques mentioned above model quantum phenomena in a variety of ways 1) Solve the Schrödinger equation using statistical methods, or 2) Use Feynmann's path integral method for directly estimating properties. All these techniques are computationally intensive and are limited in the size of the physical problems to which they can be applied.

Due to the limitations of the above techniques, semi-empirical models for extending to larger systems of million atoms are viable alternatives. These techniques are characterized by a variety of techniques in which interaction energies are characterized by different potentials. The applicability of atomistic models can be increased to over 100 million atoms by using more of semi-empirical characterization like force fields. Some of the semi-empirical methods used for modeling materials include following:

1. Classical molecular dynamics which are based on interaction potentials formulated from quantum simulation. This technique has been widely applied to synthesis methods such Physical Vapor Deposition (Voter,) and thermal properties[21].
2. Hybrid techniques such as Born-Oppenheimer approximations where the electrons are treated using quantum formalism, while the ions are treated as classical. Further extensions of these techniques to self-consistent formalism include Car-Parrinello methods where dynamic motion of electrons and ions are set to reach equilibrium state.
3. Kinetic Monte Carlo methods which use energies estimated from *ab initio* methods or use classical potentials, are used to simulate time-dependent states of a system in a stochastic way. Unlike molecular dynamics, these methods do not calculate the dynamics of the system and hence can be used to simulate

longer time scales. The technique has been applied to nucleation[22], and ultra-low pressure chemical vapor deposition[23].

Although the above techniques have been demonstrated to be useful in certain applications, they still need to be scaled to meet realistic system sizes (~100 nanometers) and physical times (microseconds or seconds).

Despite recent advances, theory has many limitations that gate applicability to systems of practical interest for quantitative correlations. Current applications include: equilibrium energies, density of states, reaction rates, effects of defects in parts per thousand, and transport within nanostructures with interfaces. At the quantum scale, the current applicability of available models is rather limited. Major issues that need to be addressed in the modeling are:

1) Extension to larger scales (tens of nanometers) for equilibrium calculation and temperature dependence of properties and processes. (This could be enabled by linear scaling DFT methods or multi-scale methods).
2) Metallic systems specifically transition and inner transition metals. These need specific functionals that could be tested with more rigorous techniques.
3) More generalized extension for band gaps. Currently hybrid and metal functionals are being developed but they need to be thoroughly characterized before their applicability is adopted. Well-characterized time-dependent methods like Quantum Monte Carlo or Time-Dependent Density Functional Theory for nanosystems still need to be addressed. This includes newer capabilities and also extension to larger systems.
4) Coupling of electronic structure predictions to non-equilibrium process such as transport and excitation are necessary since most of the devices operate in non-equilibrium. However, most of the current capabilities are limiting in extensions to realistic systems with multiple interfaces. This is one of the areas in more research need to focus on developing applications with demonstrated capability for a wide variety of systems; metals (conduction), semiconductors (mobility), and insulators (frequency-dependent dielectric response). In addition, extension of these strongly correlated systems is necessary for understanding complex oxides and Mott insulators.
5) Lattice Physics includes atomic and ionic response to externally applied fields and are based on liner perturbation methods. This has been successfully modeled for bulk materials. Extension of this to nanostructures with interfaces and in presence of external fields is necessary for addressing realistic devices.
6) Extension or linking of quantum models from femtoseconds to microseconds or longer to emulate realistic synthesis and transport. These extensions are specifically critical for molecular dynamics and Monte Carlo methods (both based on quantum and classical approaches). As a result, multi-scale techniques are becoming as more valid techniques depending on the nature of the system and the specific properties. One such relations between these models are given below[24].

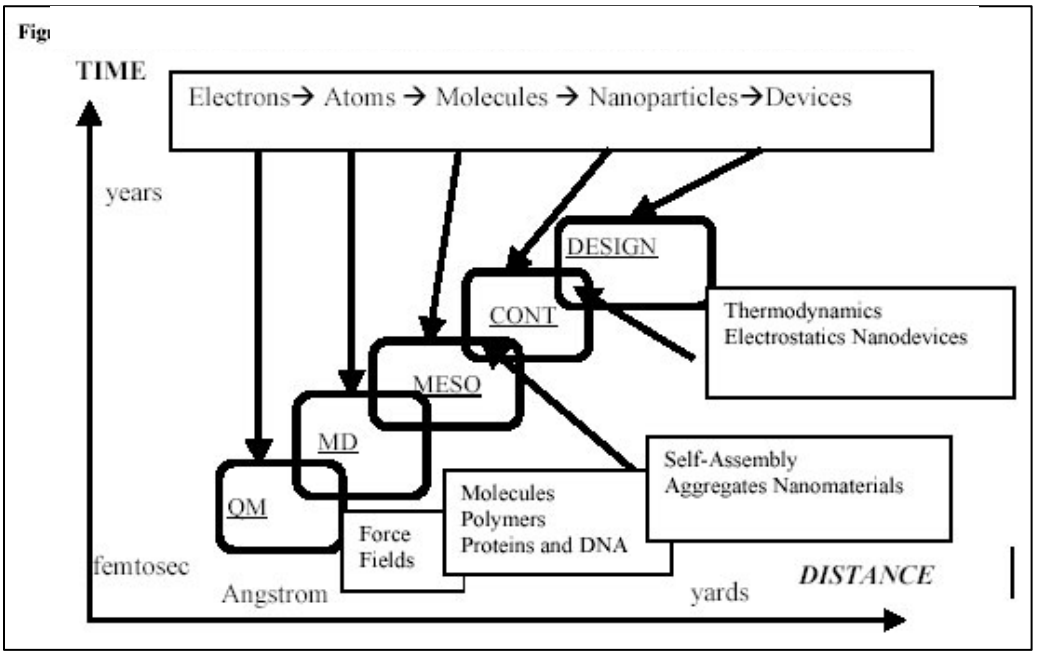

Figure ERM7 Multiscale Modeling

11.4.3. MODELING FOR METROLOGY AND CHARACTERIZATION

As mentioned previously, when new material properties are characterized, models must be developed to guide synthesis to further enable exploration of new structures and more complex interactions between materials. Establishment of an experimental database with results from well-characterized structures could accelerate the development of more accurate full ab initio and self-consistent reduced models. More quantitative material property mapping at the nanometer-scale requires development of models to probe interactions of nanostructured materials. Improved structure and property mapping for more accurate TEM, AFM, Conductance AFM, Kelvin Probe AFM, Magnetic Force Microscopy (MFM) and other new techniques could improve development of nanometer scale material models. Simulations, which help to interpret metrology, would also improve these techniques.

Summarizing, the properties that need to be addressed from both modeling and metrology are summarized below;

1) Electronic Properties (Metals, carbon, semiconductor & insulators)
   a. Size & structure dependence of
   b. Energy Levels including bandgap
   c. Spin-orbit coupling
   d. Density of States
2) Optical Properties
   a. Real & imaginary optical constant matrixes for:
      i. Individual nanostructured materials
      ii. Matrixes of nanomaterials
      iii. Nanomaterials with ultra-thin film coatings
   b. Photo-chemical Reaction (UV Resistivity, Degradation mechanism.)
3) Mechanical properties
   a. Interface adhesion and related interface properties)

b. Short and long range forces including van der Waal's, etc.

4) Thermal properties
   a. Heat capacity
5) Transport properties
   a. Electrical conductivity and mobility (electron carrier lifetime)
   b. Thermal conductivity (phonon-lifetime)
6) Interface Properties
   a. Interface states
   b. Work functions
   c. Interface Transport and Scattering
   d. Debonding and chemical reactivity
   e. Surface Energy & Defect Energy Levels

12. ERM TRANSITION TABLE

In 2013, a number of changes were made in the scope of materials included in the ERM Chapter, as shown in Table ERM20. Transition metal dichalcogenides (MoS_2, $MoSe_2$, WS_2, etc.) were added as potential alternate channel materials because they are 2D planar materials that have a bandgap and potential for high mobility. Rare earth chalcogenides were added to the Devices section because of their piezoresistive properties that could enable or support novel devices. Topological insulators were added to the Devices section to monitor progress on these emerging materials and surfaces as elements of potential novel devices and interconnects. To support FEP, the ERM has added focus on ultra high κ dielectrics (EOT<0.5nm) and ultra-low resistance contacts. To support Assembly and Packaging, NanoInks were added for multiple applications and novel EMI shielding materials were added to reduce packaging cost and provide adequate shielding properties.

Table ERM20 ERM Transition Table

13. REFERENCES

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