INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

EXECUTIVE SUMMARY

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INTRODUCTION: THE EVER CHANGING ENVIRONMENT

The Semiconductor Industry was born in the 70s as a component industry with two main business drivers. The first consisted in providing more cost effective memory devices to the computer industry. The second consisted in timely production of application specific integrated circuits (ASIC) to any company that required very specific functionalities to realize novel products. Customers demanded pin-out and functionality standardization for memory devices while ASIC products were typically customer specific. Logic devices reprogrammable by software (e.g., microprocessors) were developed to minimize cycle time of ASIC devices.

In the 80s *system specifications were solidly in the hands of the system integrators*. New semiconductor technologies were introduced every three years by memory devices and were subsequently adopted by makers of logic devices.

In the 90s the integrated circuit (IC) makers of logic devices were able to accelerate the introduction of new technologies to a more aggressive 2-year pace quickly followed by memory makers. The unusual strong correlation between technology improvements (obtained by scaling) and enhanced product performance shifted a *substantial part of the control of system performance and profits in the hands of IC manufacturers.* The IC manufacturers were able to capitalize on this new balance of power and the revenue of the entire semiconductor industry revenue grew at an average 17%/year during this period.

A completely new ecosystem has emerged during the past decade:

- First of all, the aggressive bi-annual introduction of new semiconductor technologies allowed ICs, consisting of even hundreds of million of transistors, to be produced cost effectively. This made it possible to integrate extremely complex systems on a single die or in a single package at very attractive prices. Furthermore, progress in packaging technology enabled the placement of multiple dice within a single package. These categories of devices are defined as system on chip (SOC) and system in package (SIP).
- Second, manufacturers of integrated circuits offering foundry services were able to provide, once again, the "New ASICs" at very attractive costs. This led to the emergence of a very profitable business for design "only" houses, i.e., companies that do not manufacture ICs themselves, but produce the designs that are manufactured elsewhere.
- Third, development of sophisticated equipment for advanced integrated circuits proliferated to adjacent technology fields and by so doing the realization of flat panel displays (FPD), MEMS sensors, radios and passives, etc., was made possible at reasonable costs. Under these conditions *system integrators were once again in the position to fully control system design and product integration.*

Finally, the successful adoption of the internet and the rapid rise of mobile phones led to the extensive deployment of fiber optic cables and the proliferation of multiple wireless technologies ranging from communication satellites to tens of thousands "repeater stations," which enabled an unprecedented level of global mobile connectivity.

This ecosystem has facilitated the creation of completely new and unexpected markets of which the "Social Network" represents the latest example.

Intense research on increased functionality of mobile devices, making them the ultimate customer interface to the world, is in progress. Furthermore, research on such exotic applications as making all the sensorial inputs communicable from the sender to the receiver via mobile devices is in progress.

All of the above elements today are often referred to as the "Internet of Things" (IOT). Innovative product houses, telecommunication companies, data and information distributors, as well as content providers, are battling for dominant positions in this newly created market. It is clear that all of these innovations could not have occurred without the support of the semiconductor industry that has provided the building blocks for all the above applications.

What is the role of the semiconductor industry in this new ecosystem?

2013 ITRS EDITION AND MOVING FORWARD…

The foundations of scaling were laid out with the invention of the self-aligned silicon gate process in the late 1960s. Moore's predictions of the rate of transistor bi-annual growth formulated in 1965 and in 1975 in conjunction with

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Dennard's scaling guidelines led the growth of the semiconductor industry until the beginning of the last decade. This was the (First) Era of *Classical (geometrically driven) Scaling*.

The ITRS laid out the foundations of the (Second) Era: *Equivalent Scaling* (e.g., strained silicon, high-K/metal gate, multigate transistors and integration of Ge and compound semiconductors) between 1998 and 2000. The implementation of these technologies has successfully supported the growth of the semiconductor industry in the past decade and it will continue to do so until the end of the present decade and beyond.

DEVICES

Device cost and performance will continue to be strongly correlated to dimensional and functional scaling[1] of CMOS as information processing technology is driving the semiconductor industry into a broadening spectrum of new applications according to 2013 ITRS.

Strained silicon, high- κ /metal-gate and multigate transistors are now widely used in IC manufacturing. A significant part of the research to further improve device performance is presently concentrated on III-V materials and Ge. These materials promise higher mobilities than Si devices.

In order to take advantage of the well-established Si platform, it is anticipated that the new high-mobility materials will be epitaxially grown on Si substrate. Beyond implementation of these new materials, the Emerging Research Device (ERD) section reports completely new transistors, operating on new principles like tunneling (e.g. TFET) or spin that offer the possibility of operating at very low power.

Furthermore, a large variety (like never before) of new memory devices operating on completely new principles is extensively reported in the 2013 ITRS.

Because 2D scaling will eventually reach fundamental limits towards the end of the 2013 ITRS period, both logic and memory devices are exploring the use of the vertical dimension (3D).

The combination of 3D device architecture and low power device will usher the (Third) Era of Scaling, identified in short as "3D Power Scaling". Increase in the number of transistors per unit area will eventually be accomplished by stacking multiple layers of transistors

Unfortunately no new breakthroughs are reported for interconnections since no viable materials with resistivity below copper exist. However, progress in manipulation of edgeless wrapped materials (e.g., carbon nanotubes, graphene combinations etc.) offer the promise of "ballistic conductors," which may emerge in the next decade.

3D integration of multiple dice offers possible avenues towards reducing interconnect resistance by increasing the conductor cross-section (vertical) and by reducing the length of each interconnect path. For instance, integrating memory device (die) immediately above logic device (die) and connecting them by means of wide through silicon vias (TSV) can accomplish this result.

Nevertheless, horizontal dimensional scaling of CMOS or any of the equivalent devices presently under study will eventually reach fundamental limits; the 2013 ITRS is reporting two additional ways of providing novel opportunities for future semiconductor products. The first consists in extending the functionality of the CMOS platform via heterogeneous integration of new technologies, and the second consists in stimulating invention of devices that support new information-processing paradigms.

SYSTEM INTEGRATION

System integration has shifted from a computational, PC-centric approach to a highly diversified mobile communication approach. The heterogeneous integration of multiple technologies in a limited space (e.g., GPS, phone, tablet, mobile phones, etc.) has truly revolutionized the semiconductor industry by shifting the main goal of any design from a performance driven approach to a reduced power driven approach. In few words, in the past performance was the one and only goal; today minimization of power consumption drives IC design.

This is demonstrated by the fact that SOC and SIP products have become the main drivers of the semiconductor industry as total volume of smart phones and tablets has surpassed production volumes of microprocessors in the past few years

[1] *Functional Scaling: Suppose that a system has been realized to execute a specific function in a given, currently available, technology. We say that system has been functionally scaled if the system is realized in an alternate technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost, and does not degrade in any of the other metrics.*

The foundation of heterogeneous integration relies on the integration of “More Moore” (MM) devices with “More than Moore” (MtM) elements that add new functionalities (non-CMOS) that do not typically scale or behave according to "Moore's Law.”

For instance, currently MEMS devices are integrated into small and large systems, such as automobiles, video projectors, tablets, smart phones, and game platforms. In most cases the MEMS devices add useful functionality to the system, and in some cases the MEMS devices enable the core functionality of the system. For example, MEMS accelerometers used in smart phones sense the vertical orientation of the phone and consequently rotate the image on the display. It could be said that the added functionality introduced by MEMs improves the user interface, but the phone would still operate without it. In contrast, a video projector using digital light projector (DLP) technology and an inkjet printer could not function without their MEMS devices. Multimode sensor technologies have also become an integral part of mobile devices and are key enablers of the IOT.

The rapid increase of digital data and connected technologies is also revolutionizing healthcare. Silicon, MEMS, and optical sensors technologies are making that revolution possible.

Today the mobile phone can already provide a great deal of health information. Accelerometers can track activity and sleep. Built-in optical sensors are available that can sense heart rate when the user is touching the phone. The camera in the phone can be used for purposes as diverse as checking the calorie content of a food item, or identifying your emotions based on facial expression recognition. A broad spectrum of mobile phone apps has been developed to analyze this data, and deliver it to the consumer in an intelligible and actionable manner.

Looking at long term devices and systems (7-15 years horizon, beyond 2020), the 2013 ITRS reports on completely new devices operating on completely new principles and amenable to support completely new architectures. For instance spin wave device (SWD) is a type of magnetic logic device exploiting collective spin oscillation (spin waves) for information transmission and processing. SWD converts input voltage signals into the spin waves, computes with spin waves, and converts the output spin waves into the voltage signals. Extensive parallel data processing on multiple frequencies in a single core structure can be performed at very low power by exploiting each frequency as a distinct information channel. Furthermore, some of the new devices stimulate the creation of new architectures. For instance, storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost of conventional hard-disk magnetic storage. Such a device requires a nonvolatile memory (NVM) technology that could be manufactured at a very low cost per bit.

Direct replacement of DRAM with a slightly slower M-class SCM has also been considered, for the particular example of STT-MRAM (spin torque transistor magnetic RAM).

MANUFACTURING

Manufacturing of integrated circuits, driven by dimensional scaling, will reach the few nanometers range well within the 15-year horizon of the 2013 ITRS. Is has become more and more difficult with each technology generation to measure dimensions of physical features on the wafers. This task has been largely accomplished by correlating process parameters with equipment parameters. By controlling equipment stability and process reproducibility accurate control of feature size and other process parameters has been successfully accomplished.

A major addition to the 2013 ITRS edition is a new sub-chapter on big data (BD) in the Factory Integration chapter. The fab is continually becoming more data driven and requirements for data volumes, communication speeds, quality, merging, and usability need to be understood and quantified. Challenges and solutions associated with these issues are also provided in the BD sub-chapter.

Looking at the Long Term, the 2013 ITRS addressed several 300 mm challenges, and how these challenges migrate to 450mm. The industry must focus on common technology development for 300mm and 450mm. 450mm factories would benefit by adaption of improved technology validated for 300mm

SoC and SiP integration continue to rise in prevalence throughout a number of business segments. Increased device integration forces a re-integration of test solutions to maintain scaling of test costs and product quality. The optimized test solutions may require access to and testing of embedded blocks and cores. Techniques for known good die (KGD) that provide high quality dice for multi-die packaging also become very important and an essential part of the test techniques and cost trade-offs.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

The ITRS process and content evolves to match the needs of the semiconductor industry. Collaboration of industry and research continues to be invaluable to understand and assess as well as possible the needs of future inventions and technical challenges in the various spectra of micro- and nano-electronics. Over the past few years, the ITRS teams have worked closely to assess emerging technologies. They indicate an approaching world of vast interconnectedness with humans and hardware, phrased as the internet of things (IOT), and the complex world of information processing known as big data. These examples are only part of the new frontier of invention and discovery. As these new focus topics emerge, the ITRS teams will continue to determine what this means for our global industry. The industry must define the new drivers to help it stay on a path of productivity and profitability, while promoting environmental health and encouraging areas of innovation for new scientists and technologists.

ITRS HISTORY

The most relevant subjects of the ITRS were originally divided among eleven International Technology Working Groups (ITWGs). As time went by the industry became more complex and the number of ITWGs increased to 17 in 2013. As we look forward to the 2015 ITRS it is clear that readjustments on how the ITWGs are configured and the addition of new subjects are necessary. As a result the drivers of the 2015 ITRS and the ITWGs will be redefined in 2014.

ITRS TEAMS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.) to convey messages from their respective regions. The five regions have worked together since the inception of the ITRS in 1998. The IRC is entirely responsible for all the decisions related to the ITRS. Additionally, IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the “product flow” at multiple critical points.

For the 2013 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging
- Microelectromechanical Systems (MEMS)

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement

- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

GRAND CHALLENGES IN THE NEAR-TERM (THROUGH 2020) AND LONG-TERM (2021 AND BEYOND)

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The conventional path of scaling planar CMOS will face significant challenges set by performance and power consumption requirements.

Reduction of the equivalent gate oxide thickness (EOT) will continue to be a difficult challenge in the near term despite the introduction of high-κ metal gate (HKMG). Integration of higher-κ materials while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing are also challenges to be faced. The complete gate stack material systems need to be optimized together for best device characteristics (power and performance) and cost.

New device architecture such as multiple-gate MOSFETs (e.g., finFETs) and ultra-thin body FD-SOI are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

High mobility channel materials such as Ge and III-V have been considered as an enhancement or replacement for Si channel for CMOS logic applications. High-κ metal gate dielectric with low interface trap density (DIT), low bulk traps and leakage, unpinned Fermi level and low ohmic contact resistances are major challenges.

MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. The drive to $4F^2$ type cell to increase bit density and to lower production cost will require high aspect ratio and non-planar FET structures.

Flash memory has become a new FEOL technology driver for critical dimension scaling, materials and processing (lithography, etching, etc.) technology, ahead of DRAM and logic. Continued Flash density improvements in the near term rely on the thickness scaling of the tunnel oxide and the intergate dielectric. To guarantee the charge retention and endurance requirements, the introduction of high-κ materials will be necessary. Cost effective implementation of 3-D NAND flash beyond 256 Gb with MLC and acceptable reliability performance remains a difficult challenge. New challenges also include the inception into mainstream manufacturing of new memory types and storage concepts such as magnetic RAM (MRAM), phase-change memory (PCM), Resistive RAM ReRAM and ferroelectric RAM (FeRAM).

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES, DESIGN]

Driving wireless transceiver ICs and the mm-wave applications by CMOS technologies (high κ dielectrics and strain engineering) may require techniques to keep the device mismatch and the 1/f noise within acceptable levels. Other challenges are incorporating less expensive/higher density integrated passive components, MEMS integration with active Si and off-chip passive network processes, and the development of low cost non-Si (GaN) based devices.

Signal isolation between the digital and the analog regions of the chip is becoming more critical as the chip complexity and operating frequencies increase while the power supply voltage decreases. Noise reduction may require innovation such as KΩ-cm high resistivity substrate in addition to addressing the power supply, the ground line and by design techniques.

Many of the materials-oriented and structural changes such as multiple-gates and SOI in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF, HF, and AMS performance, along with the steady reduction in supply voltages, pose significant circuit design challenges and to existing design libraries.

32, 22 nm half pitch and below [Lithography, Front End Processes, Process Integration, Devices, and Structures]

The lithography technology is becoming very expensive and most challenging.

For 22-nm half-pitch lithography, immersion 193 nm scanners with spacer lithography or multiple patterning will be applied to overcome the single patterning limitation, but with extremely large mask error enhancement factor (MEEF), wafer line edge roughness (LER), design rule restrictions and higher costs. Extreme-UV lithography (EUVL) with wavelength at 13.5 nm is the official hope of the industry to advance Moore's law. EUVL challenges are: delay by the lack of high-power sources, fast resists, defect-free and high-flatness masks. Further challenges include raising the numerical aperture of EUV systems to more than 0.35, and the likelihood of increasing the number of mirrors in the imaging system.

Multiple-e-beam maskless lithography has the potential to bypass mask difficulties, remove restricted design rules, and provide manufacturing flexibility. Progress has been made in demonstrating high-resolution imaging and CD control. Timing of manufacturing tools, costs, defects, overlay accuracy, and resists are other areas to further develop.

Direct Self-Assembly (DSA) has shown progress but defectivity and positional accuracy must see rapid improvements.

Other challenges are: gate length CD control of and suppression of LER in lithography and etching, metrology for new gate materials and non-planar transistor structure, LER of photoresist and for EUVL.

Introduction of New Materials [Interconnect]

Reduction of κ damage for low-κ dielectrics due to Etch and CMP processes becomes more important since low-κ material (include porous materials and air gap) must have sufficient mechanical strength to survive dicing, packaging, and assembling. For the metal, a very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability.

Power Management [Design, system, process technology]

Power management is now the primary issue across most application segments due to the 2× increase in transistor count per generation while cost-effective heat removal from packaged chips remains almost flat. The implementation of circuit techniques to contain system active and leakage power expands upwards into system design requirements, the improvements in CAD design tools, and downwards into leakage and performance requirements of new device architectures.

In the Near Term (through ~ 2020)—Cost-Effective Manufacturing

Lithography

Although EUVL with wavelength at 13.5 nm is the official hope of the industry, EUVL must achieve high source power to be cost-competitive at 10nm or beyond. Multiple-e-beam maskless lithography may become the most economical choice if it can keep the per-pass exposure and processing cost and the footprint similar to that of mask-based exposure tools. Pursuance of DSA with immersion 193nm is active since the process involves much lower mask counts.

Front End Processes

We need to achieve low parasitics and continued scaling of gate pitch and areal scaling with next generation substrates (450mm wafers) and adoption of disruptive technologies to meet lithographic challenges.

Factory Integration

Difficult challenges are as follows:

- Respond to rapidly changing, complex business requirements
- Manage ever increasing factory complexity
- Achieve financial growth targets while margins are declining
- Meet factory and equipment reliability, capability, productivity and cost requirements
- Cross leveraging factory integration technologies across boundaries such as 300mm and 450mm to achieve economy of scale
- Address unique challenges in the move to 450mm wafers

MEET THE CHANGING COST REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

The challenges for assembly and packaging include 3D IC chip stacking (testing: access, cost and KGD, 3D assembly and packaging; test access for individual wafer/die).

ESH

The challenges are: Chemicals and Materials Management and Efficiency; Process and Equipment Management; Facilities technology requirements; Product Stewardship, End-of-Life Reuse/Recycle/Reclaim.

METROLOGY

Factory-level and Company-wide Metrology Integration: Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO).

IN THE LONG TERM (2021 THROUGH 2028) —ENHANCING PERFORMANCE

IMPLEMENTATION OF NON-CLASSICAL CMOS CHANNEL MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESS, EMERGING RESEARCH DEVICES, AND EMERGING RESEARCH MATERIALS]

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to be integrated physically or functionally onto a CMOS platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate, which is challenging. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development.

IDENTIFICATION, SELECTION, AND IMPLEMENTATION OF NEW MEMORY STRUCTURES [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

Line-dense, fast, and low-operating-voltage non-volatile memory will become highly desirable, and ultimate density scaling may require three-dimensional architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness (EOT) and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or developing alternative emerging technologies.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Line edge roughness, trench depth and profile, via sidewall roughness, etch bias, thinning due to cleaning, CMP effects, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. Etching, cleaning, and filling high aspect ratio structures, especially low-κ dual damascene metal structures and DRAM at nano-dimensions are also big challenges. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo-mechanical effects. Novel/active devices may be incorporated into the interconnect lines. Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets is a key challenge.

EUV LITHOGRAPHY [LITHOGRAPHY]

As EUV lithography (EUVL) remains the leading candidate for the 22 nm and 16 nm half-pitches, extending it to higher resolutions becomes a significant long-term challenge. From what we know today, designs of 0.5 NA or larger at the current wavelength will necessitate either an eight-mirror unobscured or six-mirror center obscuration design. The eight-mirror design will have more diminished reflectance because of the added mirrors, requiring higher power sources for an equivalent wafer throughput. The angular spread in the six-mirror design is narrower, thus demanding a smaller field size and perhaps longer track length. The increase in NA will pose significant challenges in the depth of focus for both designs. Furthermore, to overcome shadowing and other 3D effects on the mask, absorber materials, absorber thickness, and multilayer stacks will have to be optimized.

An alternative solution path would be to reduce the EUVL wavelength to 6.x nm. In the near term, this path would inherit all the current challenges of EUVL, from source availability to mask infrastructure and resist performance. Multiple patterning with EUVL will also be an option, bringing with it added process difficulties and cost of ownership.

IN THE LONG TERM (2021 THROUGH 2028) —COST-EFFECTIVE MANUFACTURING

MEETING THE FLEXIBILITY, EXTENDIBILITY, AND SCALABILITY NEEDS OF A COST-EFFECTIVE, LEADING-EDGE FACTORY [FACTORY INTEGRATION]

The ability to load the fab within a manageable range under changeable market demand and to utilize task sharing opportunities such as manufacturing outsourcing is required to keep manufacturing profitable. Enhanced customer visibility for quality assurance of high reliability products, including manufacturing outsourcing, continues to be a challenge. Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] promotes reuse of building, production and support equipment, and factory information and control systems across multiple technology generations. Cost and task sharing schemes are highly expected on industry standardization activity for industry infrastructure development such as data standardization and visualization methodology.

SPECIAL TOPICS

MORE THAN MOORE

The term ‘More than Moore’ was introduced in the 2005 edition of the ITRS to denote the fact that, next to digital scaling, heterogeneous integration of new non-digital functionalities into smart systems became a driving factor for the technology roadmap. This trend, diversification in conjunction with miniaturization, led to an increasing complexity in the roadmapping process itself. Therefore, a methodology for the More than Moore roadmapping process was developed, as outlined in the ‘More than Moore White Paper’ (http://www.itrs.net/papers.html), which was released in 2010.

A prerequisite for the More than Moore roadmapping process is the identification of a number of figures of merit (FOM) for specific functionalities, such as wireless communication, power generation and management, sensing and actuating. An essential feature of More than Moore related technologies is that these are strongly dependent upon the application requirements, as determined by societal needs. For each of the relevant application domains (e.g. ICT, automotive, lighting, energy, healthcare), driving applications have to be identified, which are analysed to generate system views and, subsequently, generic functions. Due to the fact that More than Moore domain clearly constitutes a cross-over of the chip level and the system level, the ITRS has started a cooperation with iNEMI (International Electronics Manufacturing Initiative), in order to address the technology/design/application interaction in the most effective way. Various TWGs are involved in this effort, most notably Design & System Drivers, RF & AMS, MEMS, Assembly & Packaging, and ERD/ERM.

By nature, the More than Moore domain is multidisciplinary, involving expertise from many different areas, such as electrical and mechanical engineering, materials science, biology and medical science. This is reflected in the present ITRS edition, in which an increasing numbers of parameters associated with these new functionalities are being addressed.

2013 ITRS “EQUIVALENT SCALING” UPDATE TIMING AND PIDS PURDUE MODELING

BACKGROUND OF PIDS/PURDUE MODELING FOR THE ITRS

During their 2012 and 2013 Update work, and to enable the significant amount of modeling work and resources required to develop future ITRS guidance tables, the ITRS PIDS TWG received approval from the IRC to initiate a partnership with Purdue University. PIDS assumed primary responsibility for interfacing with Purdue to assure alignment of the past ITRS MASTAR model approach with the new Purdue TCAD long-range dynamic modeling tools output. The ITRS Modeling TWG agreed also to participate in reviews with the PIDS and Purdue team. Purdue University agreed to support the ITRS, and would allow use of the Purdue online public modeling review resources for additional public discourse and input to the project.

Up to this year, MASTAR (references in the PIDS chapter) has been the main tool used to generate these device characteristics. Since it is based on compact modeling, a more sophisticated modeling tool is necessary because channel lengths are getting to the sub-10-nm range and the body thicknesses for SOI and FinFET structures are substantially smaller. These small dimensions manifest in many quantum phenomena such as tunneling, carrier confinements in space and energy, ballistic transport, etc. Furthermore, two-dimensional finite-element methods are becoming more and more critical, and three-dimensional simulation will soon be mandatory for nanowire structures. Another consideration is new channel materials such as III-V and Ge. Thus, advanced, physics-based TCAD simulation tools are necessary.

The philosophy for PIDS logic team has been that the simulation tool will be open to the public, besides the input files and results, so readers not only will be able to reproduce the results, but also can vary the input parameters to see the effects and sensitivity. This requirement rules out commercial tools.

Given these requirements, PIDS is very fortunate to get the involvement from the simulation group of Purdue University, with approval and full support from the IRC. The Purdue group is well-known for their suite of device simulation tools. Their comprehensive, well-established website NanoHub (references in PIDS chapter) hosts many device simulation tools that are in public domain, and in fact are popular and widely used world-wide. With Purdue's engagement, the ITRS benefits from the additional help from the man-power of students, guidance of the faculty, and the continued maintenance and improvement of these tools. The goal is to have these tools reside in some part of NanoHub, dedicated to ITRS, and will include the input and output files, documents for all the assumptions made, as well as instructions to run these tools, all accessible to the public.

To be clear, this addition of TCAD simulation tool is not meant to replace compact models. A compact modeling tool is easier and faster to run. And it is the only way to connect to circuit simulators to explore circuit performance. It is the intention of the teams that a compact modeling tool, or actual compact models, are maintained in parallel with the new TCAD simulation capability to satisfy different needs.

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

Continuing Moore's Law functional density benefits and managing power and performance tradeoffs remain as the key drivers of the Roadmap grand challenges and potential solutions. Therefore, driving half-pitch reduction, combined with managing and gate-length and "Equivalent Scaling tradeoffs also remain as drivers.

The MPU/ASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. The trend targets have been updated in the 2013 ITRS ORTC tables from the 2011 and 2012 ITRS Roadmap editions. The MPU/ASIC M1 trend leveled off at 40nm in the period from 2010 to 2013, and is anticipated in the 2013 ORTC Table 1 to continue forward on a 3-year technology cycle (0.5x every 6 years). It is possible that the industry will continue to press for the historical 2-year cycle (0.5x per 4 years) trend through 2017. The actual industry trends will be monitored in 2014 and 2015 for updates in future ITRS renewals.

Note that Logic technology "Node Naming," is now included in the 2013 ORTC Table 1 as a helpful guide to typical industry naming convention. However, "Node Naming" is included for alignment purposes only, and will be monitored for changes, along with the best estimates of alignment to actual technology data in available public documents.

Although the DRAM M1 half-pitch target is unchanged in the first column year, 2013/28nm, the PIDS ITWG survey consensus updated the DRAM M1 half-pitch trend to a 4-year cycle (0.5x every 8 years), slowing from the 3-year pace of the previous roadmap version. The MPU/ASIC M1 half-pitch lags behind DRAM, however, the faster MPU/ASIC 3-year cycle trend crosses DRAM at 2026/9 nm, and then leads DRAM through the balance of the roadmap.

The Flash product half-pitch, unchanged for the 2012 ITRS ORTC Update, continues to be defined as an uncontacted polysilicon half-pitch; and was also revised in 2011 from the 2009 and 2010 ITRS additions by continuing the two-year cycle trend through 2009/39 nm, then matching the PIDS Flash survey 2010/24 nm before turning to the survey-forecasted 4-year cycle (0.5× per 8 years) through 2018/12 nm. At the 2018 point, the Flash Flash survey consensus forecasts the trends to remain flat to anticipated Flash cell design limitations and also due to costs of 2D processing approaching an unaffordable level.

The Flash 3D bit layer model was updated in 2013 to align with the recent introduction of a 24-layer 3D NAND device, processed at a relaxed 64nm process point. The 3D NAND range of layers was also updated, along with the anticipated trend of relaxed process technology reduction going forward. See the PIDS TWG chapter models discussion for additional details.

To reflect the diversity of product technology cycle needs and to continue close monitoring of future Roadmap trend shifts, it was agreed by the IRC to continue the practice of publishing annual technology requirements in the 2013 ITRS Renewal Work from 2013 through 2020, called the "Near-term Years," and also annual requirements from 2021 through 2028, called the "Long-term years." As seen above in Figures ORTC1 and ORTC2, the long-term years of the 2013 ITRS are now somewhat aligned with the timing of the especially-challenging sub-1× nm technology era (2019/13–14 nm M1 to 2026/6.3–6 nm M1).

As part of the 2013 ITRS Renewal work, the IRC agreed among their regional members to examine other options for ORTC technology trend drivers in the near term years which are typical of available industry data and expectations of the

chip IDM and foundry/fabless design communities. Specifically, it was agreed that the ORTC Table 1 would add line items which track and target: Logic SRAM (6-transistor) Cell Area (μm^2); and also Logic (4-transistor) NAND Gate Density (Gates/mm^2)—trends established by Design TWG and ORTC models. This work aligned also with recommendations for simplification of the tables around PIDS high performance and low power drivers of the 2013 ITRS ITWG work.

In their 2013 work, the IRC and the Cross-TWG study groups and subteams acted on the IRC recommendations and made proposals that would be suitable for the 2013 ITRS roadmap development work. This work addressed the need to be current to the latest status of industry needs and plans. The near term range industry technology status validation and alignment activities addressed the main priorities of the ITRS mission to create the Grand Challenges and Potential Solutions for pre-competitive research by academic and consortia and government laboratories.

The resulting consensus line item drivers are now included in a single table, Table ORTC1. Below is a summary of the details. *Follow this link to see the entire ORTC table details.*

Table ORTC1 Summary Table of ITRS Technology Trend Targets

Year of Production	*2013*	*2015*	*2017*	*2019*	*2021*	*2023*	*2025*	*2028*
Logic Industry "Node Name" Label	**"16/14"**	**"10"**	**"7"**	**"5"**	**"3.5"**	**"2.5"**	**"1.8"**	
Logic ½ Pitch (nm)	**40**	**32**	**25**	**20**	**16**	**13**	**10**	**7**
Flash ½ Pitch [2D] (nm)	**18**	**15**	**13**	**11**	**9**	**8**	**8**	**8**
DRAM ½ Pitch (nm)	**28**	**24**	**20**	**17**	**14**	**12**	**10**	**7.7**
FinFET Fin Half-pitch (new) (nm)	**30**	**24**	**19**	**15**	**12**	**9.5**	**7.5**	**5.3**
FinFET Fin Width (new) (nm)	**7.6**	**7.2**	**6.8**	**6.4**	**6.1**	**5.7**	**5.4**	**5.0**
6-t SRAM Cell Size(um2) [@60f2]	**0.096**	**0.061**	**0.038**	**0.024**	**0.015**	**0.010**	**0.0060**	**0.0030**
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	**0.248**	**0.157**	**0.099**	**0.062**	**0.039**	**0.025**	**0.018**	**0.009**
4-input NAND Gate Density (Kgates/mm) [@155f2]	**4.03E+03**	**6.37E+03**	**1.01E+04**	**1.61E+04**	**2.55E+04**	**4.05E+04**	**6.42E+04**	**1.28E+05**
Flash Generations Label (bits per chip) (SLC/MLC)	**64G /128G**	**128G /256G**	**256G / 512G**	**512G / 1T**	**512G / 1T**	**1T / 2T**	**2T / 4T**	**4T / 8T**
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	**16-32**	**16-32**	**16-32**	**32-64**	**48-96**	**64-128**	**96-192**	**192-384**
Flash 3D Layer half-pitch targets (nm)	**64nm**	**54nm**	**45nm**	**30nm**	**28nm**	**27nm**	**25nm**	**22nm**
DRAM Generations Label (bits per chip)	**4G**	**8G**	**8G**	**16G**	**32G**	**32G**	**32G**	**32G**
450mm Production High Volume Manufacturing Begins (100Kwspm)				**2018**				
Vdd (High Performance, high Vdd transistors)[**]	**0.86**	**0.83**	**0.80**	**0.77**	**0.74**	**0.71**	**0.68**	**0.64**
1/(CV/I) (1/psec) [**]	**1.13**	**1.53**	**1.75**	**1.97**	**2.10**	**2.29**	**2.52**	**3.17**
On-chip local clock MPU HP [at 4% CAGR]	**5.50**	**5.95**	**6.44**	**6.96**	**7.53**	**8.14**	**8.8**	**9.9**
Maximum number wiring levels [unchanged	**13**	**13**	**14**	**14**	**15**	**15**	**16**	**17**
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	**28**	**22**	**18**	**14**	**11**	**9**	**7**	**5**
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	**20**	**17**	**14**	**12**	**10**	**8**	**7**	**5**
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	**23**	**19**	**16**	**13**	**11**	**9**	**8**	**6**

*** Note: from the PIDS working group data; however, the calibration of Vdd, GLph, and I/CV is ongoing for improved targets in 2014 ITRS work*

WORKING GROUP SUMMARIES

Throughout 2013, all the working groups reviewed their previous assessments and adjusted their chapter reports and tables as determined by their world-wide teams. Most work resulted in significant revision. For this edition of the roadmap, several teams impacted most by recent developments in the industry and the prospect of new drivers and technologies continue to explore/assess technology needs and possible solutions. In some cases, this work continues into 2014.

We have summarized the 2013 work at this link: *http://www.itrs.net/Links/2013ITRS/Summary2013.htm.* The full version of the 2013 edition of the ITRS is found at *http://www.itrs.net/Links/2013ITRS/Home2013.htm.*