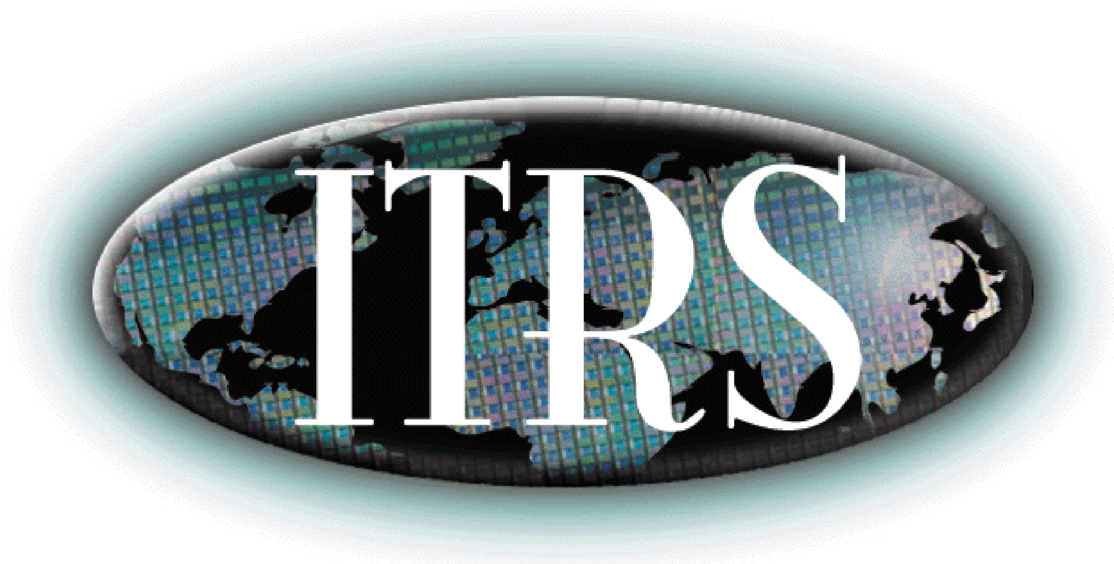

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

FRONT END PROCESSES SUMMARY

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

FRONT END PROCESSES

For 2013, the updated portions of the FEP Roadmap tables are High Performance Devices, Low Standby Power Devices, FeRAM, Thermal, Thin Film, Doping Process Technology, Starting Materials, and Surface Preparation. Updates to DRAM, Floating Gate Flash Non-Volatile memory (NVM), Charge Trap Flash NVM, Phase Change Memory, Etch and CMP will likely be completed in 2014. The chapter text was not updated in 2013.

It is acknowledged that there are many FEP challenges in the near future. It will be difficult to continue scaling of gate pitch while achieving low parasitics (resistance and capacitance). As the pitch tightens there needs to be improvement of Strain engineering for increasing device performance and the application to FDSOI and Multi-gate technologies. Continued areal scaling needs to occur with next generation substrates (450mm wafers) and adoption of disruptive technologies to meet lithographic challenges.

As the industry continues transitioning into non-planar HP Multigate devices, scaling must occur in all aspects : EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.

The 2013 roadmap captures the evolution of HP multigate devices as it involves the introduction and hetero-integration of high mobility channels (based on III-V and Ge) to replace strained Si. The continual scaling of device parasitics includes these new channel materials, especially for contact resistivity due to severe reduction in device pitch and contact area, and the continual EOT scaling and associated gate dielectrics with low DIT, low bulk traps and leakage for high mobility, and low bandgap channels materials (Ge, IIIV and 2D materials).

Table FEP1 Front End Processes Difficult Challenges

Difficult Challenges ≥ 10 nm	*Summary of Issues*
	Strain Engineering – continued improvement for increasing device performance at tight pitch – application to FDSOI and Multi-gate technologies
	Achieving low parasitics (resistance and capacitance) and continued scaling of gate pitch
	Continued areal scaling with next generation substrates (450mm wafers) and adoption of disruptive technologies to meet lithographic challenges.
Difficult Challenges < 10 nm	*Summary of Issues*
	Continued scaling of *non-planar* HP multigate device in all aspects : EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Introduction and heterointegration of high mobility channels (based on III-V and Ge) to replace strained Si for continual performance
	Continual scaling of device parastics with new channel materials, especially for contact resistivity due to severe reduction in device pitch and contact area.
	Continual EOT scaling and gate dielectrics with low D_{IT}, bulk traps and leakage for high mobility, low bandgap channels materials (Ge, IIIV and 2D materials)