INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

INTERCONNECT SUMMARY

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INTERCONNECT

SCOPE

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit, along with providing necessary power and ground connections. The process scope begins at the contact level with the pre-metal dielectric and continues up to the wirebond pads, describing deposition, etch and planarization steps, along with any necessary etches, strips and cleans. A section on reliability and performance includes specifications for electromigration and calculations of delay. Expanded treatment of Emerging Interconnects and 3D integration are new features included in the chapter.

INTRODUCTION

The Interconnect chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap for Semiconductors (ITRS) emphasized an ongoing change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low-κ dielectric introduction for microprocessors (MPUs) and application-specific ICs (ASICs) was one of the central issues for the 2003 ITRS Interconnect area. The 2005 ITRS showed the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A crosstalk metric was also introduced in 2007. Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, radio frequency (RF), or vertical integration combined with accelerated efforts in design and packaging will deliver the continuing ability to match the performance scaling expected with Moore's Law.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuit/system functions on a chip. The fundamental development requirement for interconnect is to meet the high-bandwidth low-power signaling needs without introducing performance bottlenecks as scaling continues.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, reduction of the insulator dielectric constant indicated by the ITRS has been problematic. Fluorine doped silicon dioxide ($\kappa = 3.7$) was introduced at 180 nm, however insulating materials with $\kappa = 2.7–3.0$ were not widely used until 90 nm. The reliability and yield issues associated with integration of these materials with dual damascene copper processing proved to be more challenging than expected. The integration of porous low-κ materials is expected to be even more challenging. Since the development and integration of these new low-κ materials is rather time invariant, the anticipated acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable κ to later technology generations. The various dielectric materials that are projected to comprise the integrated dual damascene dielectric stack for all years of the roadmap are depicted in the Dielectric Potential Solutions Figure, INTC 13. The range of both the bulk κ values and effective κ values for the integrated dielectric stack are listed in the Technology Requirements Table INTC2 The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformity requirements for barriers and nucleation layers, provides difficult integration challenges. (For a more thorough explanation, the Appendix illustrates the calculation of the effective κ for various integration schemes.) The imminent convergence of the M1 pitches for MPU and DRAM, expected by 2010, negates the need to identify a single technical product driver but technical specifications are included for both high performance logic and DRAM. A table of INTC3 dedicated for flash memory is still being a technology driver for the most advanced M1 pitch.

WHAT'S NEW FOR 2013?

- The Technology Requirements Table (INTC2) has been substantially kept with 2011 style as reorganized and divided into
  - General requirements – e.g., bulk resistivity and dielectric constant
  - Level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-κ roadmap – slightly changed due to little progress in materials

  - New range for bulk κ
  - Air gaps expected to be a possible solution for $\kappa_{bulk} < 2.0$
  - First implementation will be for Flash
  - Evaluation of new parametric indicator considering sidewall damage by RIE or wet cleaning
- Renewal of metallization potential solution with appropriate material candidates and their promising application.
  - Barriers (< 3.0 nm) and nucleation layers are a critical challenge
  - Approaches of new liners (Co, Ru and others) stacked with barrier layers are proliferating
  - Capping metal for reliability improvement nearing production
  - Reconsideration of appropriate material candidates with their potential duration as MnSiO, CuAl and CuTi.
- J_{max} current limit model kept as 2011 revision with relaxed on-chip clock frequency
  - J_{EM} improvement by capping metal
  - Detail discussion for A&P TSV with SIV
- TDDB description update with lifetime estimation model
- Revised 3D TSV roadmap tables
- Emerging interconnect solutions are being developed.
- All new interconnect variables are slow and will require substantial area savings to match/exceed the speed of repeated Cu/low-κ with CMOS drivers; applications will likely be driven by new functionality enabled by emerging interconnects
- Novel state variables are slow relative to repeater-driven Cu/low-κ and require significant area savings to maintain switching speed
- Evaluation of energy efficiency of emerging options necessitates joint consideration of switch and interconnect options

SUMMARY

For 2013, interconnect performance is at the forefront as a key challenge to achieve overall chip performance. Low-κ scaling (κ< 2.6) was greatly slowed down due κ-value increase by plasma and mechanical damages induced during interconnect integration. Air gap structures are now considered a mainstream potential solution for the ILD, recognizing their increased maturity. Air gap structure with SiO_2 ILD has started to be introduced into NAND Flash memory to reduce the word-line capacitance. The ITRS team firmly believes that any substantial reduction in effective κ will not be achieved by further materials improvements of porous ultra-low-κ ($\kappa \leq 2$) but by the use of low-κ scaled diffusion barriers and air gap structures. For low-κ, this is the end of materials solutions and the beginning of architecture solutions. Delays in the emergence of quality ALD processes prevent the deposition of the required sub-2 nm barriers, and are a top concern. Discussions on 3D interconnects have been moved out of the emerging interconnect section, with TSVs nearing production.

In addition, the ITRS chapter contains significant new content on the search for Cu replacements and the need to consider interconnect requirements for the inevitable replacement for the FET switch. There are more radical options beyond even carbon nanotubes—including molecular interconnects, quantum waves and spin coupling—that are in the infant stages of development but, in each case, the goal is propagating terabits/second at femtojoules/bit.

DIFFICULT CHALLENGES

Table INTC1 highlights and differentiates the five key challenges in the near term (≥ 16 nm [Mx hp]) and long term (< 16 nm [Mx hp]). In the near term, the most difficult challenge for interconnects is the introduction of new materials that meet the wire conductivity requirements and reduce dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be mitigated.

Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. Dimensional control is a key challenge for present and future interconnect technology generations and the resulting difficult challenge for etch is to form precise trench and via structures in low-κ dielectric material to reduce variability in RC. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional

control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels.

Table INTC1 2013 Interconnect Difficult Challenges

Five Most Critical Challenges ≥16 nm [Mx hp]	*Summary of Issues*
Materials *Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	*The rapid introduction of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.*
Manufacturable Integration *Engineering manufacturable interconnect structures, processes and new materials*	*Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool*
Reliability *Achieving necessary reliability*	*New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.*
Cost & Yield for Manufacturability *Manufacturability and defect management that meet overall cost/performance requirements*	*As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.*
Five Most Critical Challenges < 16 nm [Mx hp]	*Summary of Issues*
Materials *Mitigate impact of size effects in interconnect structures*	*Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) will be required*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.*
Process *Patterning, cleaning, and filling at nano dimensions*	*As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.*
Complexity in Integration *Integration of new processes and structures, including interconnects for emerging devices*	*Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.*
Practical Approach for 3D *Identify solutions which address 3D interconnect structures and other packaging issues*	*Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.*