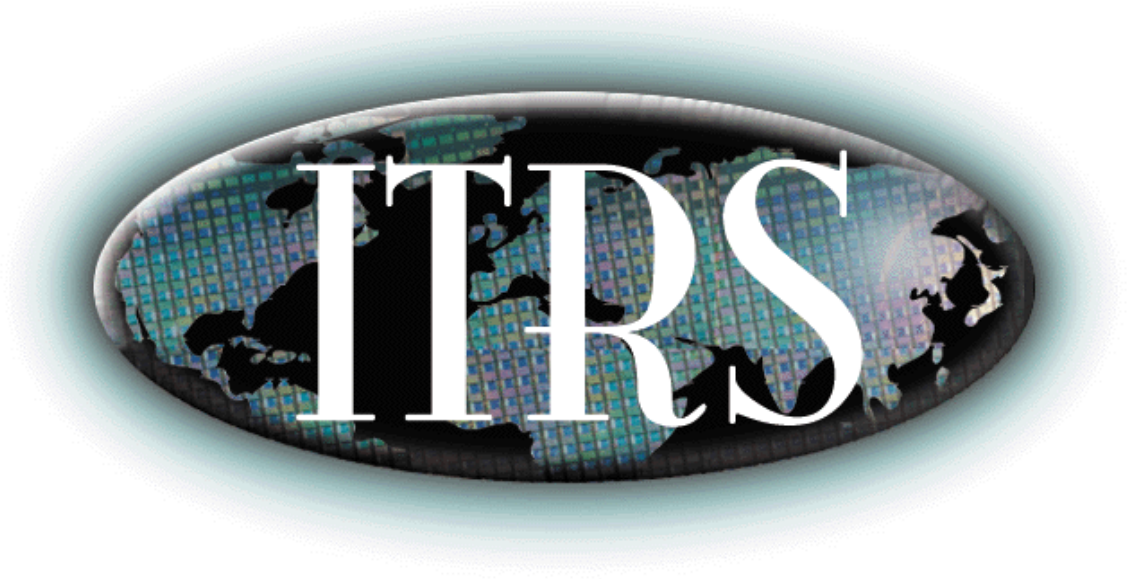

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

LITHOGRAPHY

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LITHOGRAPHY

1. SCOPE

This chapter discusses the different lithography methods that are potentially available to meet the resolution and pattern quality requirements needed to meet the device needs of the ITRS roadmap. Table LITH1, Lithography Technology Requirements, shows these basic patterning requirements from 2014 to 2028. For the first time, this table also includes contact hole pitches and finFET fin half pitches. FinFETs were introduced into production in 2012 and the fins are the smallest half pitches in a finFET containing chip. Contact holes and other hole types patterns such as vias and cuts for complementary lithography are some of the most difficult patterns to image. The minimum half pitches that can be achieved are always larger than what can be resolved for lines and spaces. The projected line and space half pitches and fin half pitches come from the basic device roadmap. Overlay and CD control requirements are calculated from these half pitches. The logic minimum contact hole pitches come from basic design requirements of CMOS logic devices. The memory contact hole pitches come from actual device construction data and are extrapolated assuming a similar ratio contact hole pitch to line and space pitch in the future. The table also shows chip size and wafer flatness requirements along with relevant tool numerical apertures (NAs).

Table LITH1 Lithography Technology Requirements

2. DIFFICULT CHALLENGES

In the near term, most of the key challenges relate to multiple patterning and EUV. The advent of quadruple patterning does not increase mask pattern complexity, but it does drive overlay, CD control mask image placement and process cost and cycle time. For EUV, the biggest issue is source power. Without enough source power, the cost of EUV is very high because throughput is very low. In 2013 it was reported that an EUV pilot tool was running at 2 to 3 wafers per hour.[1] There are EUV sources reported with powers in the range of 40 to 55 watts at intermediate focus,[2] which should give 43 wafers per hour with 15mJ/cm2 resist,[3] but there are not yet any reports of such sources being used in the field. Even if there is enough source power, there are other key short term challenges. EUV mask infrastructure needs to be in place to a large enough extent that customers can buy a reasonable number of defect free masks. And resists and resist post processing have to improve to give sufficient pattern quality to make functioning devices that meet performance targets. Directed Self-Assembly (DSA) is a possibility in the short term for simple patterns, but it needs to demonstrate sufficiently low defects and good pattern registration in order to be viable.

In the long term EUV source power has to increase. Not only will this reduce cost, but it will help with potential shot noise and resist performance issues that are expected to arise as the roadmap moves to smaller feature sizes. EUV will also need to be extended to NAs higher than 0.40. But such NAs require a wider range of reflection angles from the mirrors making up an EUV lens. This can create problems in lens design and problems in consistent reflectivity from EUV mirrors at different angles. One approach to this issue is to change the magnification factor of the lens. This requires either smaller exposure field sizes or larger masks, both of which create challenges of their own. All of the other alternative imaging technologies have challenges of their own. DSA will require DSA compatible designs or novel DSA implementations with more design flexibility. Maskless lithography needs to have actual working tools. Imprint has to improve its defectivity. Finally, there are many metrology challenges that will need to be addressed, no matter what patterning technology is used. A summary of these challenges is shown in Table LITH2.

Table LITH2 Lithography Difficult Challenges

	Near Term Challenges (2013–2016)
1	Cost and cycle time of multiple patterning – especially for more than 2x
2	Process control on key parameters such as overlay, CD control, LWR with multiple patterning
3	EUV Source power
4	EUV Mask Infrastructure (defect inspection and verification, mitigation, mask lifetime) Defect free EUV mask blanks, mask availability
5	EUV resist and/or process that meets sensitivity, resolution, LER requirements
6	DSA defectivity and positional accuracy
	Long Term Challenges (2017 and beyond)
1	Higher source power for EUV
2	Higher NA EUV tool and mask implementation and infrastructure
3	DSA compatible design rules
4	EUV Extension (wavelength, mask, mirrors, resist, etc.)
5	Maskless lithography production tool demonstration
6	Imprint defectivity, throughput and OL matching
7	Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect

3. LITHOGRAPHY TECHNOLOGY REQUIREMENTS

Lithography, as presently practiced in semiconductor manufacturing, uses projection steppers and scanners at several wavelengths in order to address the needs of patterning different layers within a semiconductor device. The highest resolution lithography is done using a wavelength of 193nm (ArF) and immersion scanners with 1.35NA lenses. This type of lithography is well established. It has a resolution limit of 40nm half pitch for simple patterns of lines and spaces and a somewhat larger resolution limit for other types of patterns. Smaller half pitches than 40nm are in production now and are produced by printing a pattern of 40nm half pitch or larger and then using process steps to halve the pitch (pattern doubling), or by doing more than one exposure per level in a way that combines two printed patterns into one higher resolution pattern. Relatively simple patterns such as the minimum half pitch patterns of flash memory or the fins in finFET devices are done with self-aligned double pattering (SADP). This creates lone parallel lines that then require an additional "cut" step that create shorter line segments. Using line and space patterning followed by "cuts" is known as complementary lithography. Metal levels in DRAM and Logic chips can have more complicated patterns that can't be done with SADP. These metal layers require Litho Etch Litho Etch (LELE) type double patterning rather than SADP. This technique requires two exposures and pattering steps per layer and is more expensive than SADP. Some further increases in resolution can be done by pattern quadrupling, where a pattern is doubled and then doubled again solely by process steps on a wafer patterned with immersion lithography. But this has only been demonstrated for very simple patterns. Other types of patterns require demonstration of more complicated multiple patterning or implementation of some new technique.

Historically, lithography resolution has been improved by decreasing the exposure wavelength, by increasing the NA of exposure tools and by using improved materials and processes. The NA of 193nm exposure tools cannot be extended since higher index immersion fluids are not available. Smaller optical wavelengths such as 157nm cannot be used due to lack of a suitable immersion fluid and/or the lack of a lens material. So the industry has been working on extending resolution by using EUV, which has a wavelength of 13.5nm. EUV exposure tools with 0.33NA started shipping in 2013 for use in chip research and development and pilot production and these tools should be operational in the first half of 2014. These tools have resolution capability of well under 30nm for contact hole half pitch and well under 20nm for line and space half pitch. But these tools will need source upgrades with brighter light sources if they are to have sufficient throughput for production use. Such EUV light sources have not yet been demonstrated. So EUV is considered a possible option for meeting the future needs of the lithographic roadmap. Details of the current capabilities and future challenges for EUV lithography are described in the section "EUV Lithography" below. There are subsections on resist, mask and tooling challenges for EUV, since each of these areas is critical to EUV's success.

There are other possible options for higher resolution that are also in development. Pattern multiplication could continue to be extended to greater multiplication factors. In principle, this can be done by using existing process technology and adapting it to smaller features and tighter tolerances. However, lithographic exposures are some of the most expensive

processes in a fab and doubling or tripling or more the number of exposures per layer for key layers can quickly become unaffordable. In addition, many exposures and/or many pattern multiplication process steps create many complicated tolerance stack ups and may require process control that is undoable. Since pitch multiplication is easier to do on simple lines and spaces, there has been growth in the use of complementary lithography. These sorts of processes avoid needing to increase the intrinsic resolution capability of an exposure tool. However, required overlay, CD control and pattern roughness still scale with the final patterned features size, so tools and processes still have to improve despite the use of multiple patterning. These are significant challenges. Details of these processes and the challenges of extending them to smaller features are described in the sections "Multiple Patterning/Spacer Technology" below.

E-beam lithography or maskless lithography (ML) uses e-beams to do direct write of features in e-beam sensitive resist. Writing high resolution features with a directed e-beam is intrinsically slow, so in order to get sufficient throughput, massively parallel writing with thousands of independently directed e-beams is necessary. Two different companies are developing tools to do this with a projected delivery date of pilot tools to semiconductor companies of sometime in 2016. The details and challenges of this technology are shown in the section "Maskless Lithography" below.

Nanoimprint is a potential solution that involves coating a thin pattern of liquid on a wafer and using a mask with high resolution relief patterns to physically stamp the wafer and create a relief pattern. The relief pattern can then be used as an etch mask in much the same way that patterned photoresist is. The leading implementation of this technique using step and flash, where a transparent mask is used to stamp one chip at a time and enable photochemical curing of the patterned material before the stamp is lifted from the wafer. Since this is a contact technique, defects are a significant concerns and a system of master and secondary masks is used to accommodate a short lifetime for the masks used for the actual chip patterning and improve the defectivity of the process. Pilot tools are available for companies that wish to test this and one semiconductor has a significant program evaluating the potential of this technology. Details of the capabilities and challenges of this technique are discussed in the "Nanoimprint" section below.

A patterning technique that has shown a lot of progress in the last two years is directed self-assembly (DSA). This technique takes advantage of the fact that required feature sizes are reaching a size similar to that of polymer molecules that can be readily made in the lab. The most common implementation uses special polymers called block copolymers, which consist of two connected polymers each made from a different monomer. If the monomers are selected properly, the blocks will separate into phase domains when annealed. The phase domains will have a size determined by the size of the individual polymer blocks and the shapes of the domains will be determined by the ratio of the sizes of each polymer block. By creating guiding features on a wafer, this domain formation process can be constrained to give line or hole patterns with the lines and holes in desired locations. Patterns printed with 193nm immersion lithography can be used as guide patterns and pitch multiplication factors of three or four times are readily accessible. This technique was considered a research topic two years ago, but now most major semiconductor producers have substantial programs exploring the possibility of implementing this technique in actual chip production. The details and challenges of this technology are shown in the section "Directed Self Assembly (DSA)" below.

4. LITHOGRAPHY POTENTIAL SOLUTIONS

Based on our assessments of industry needs and the availability and timing of each of these options, we have prepared possible options roadmaps that show the different paths the industry can take to meet future resolution needs. A key question for any leading edge patterning technique is what size lines and spaces it can resolve. Figure LITH1A shows published resolution for the various patterning techniques. The black cells indicate where there are published papers indicating the use of the technique in production. The gray cells and the cross hatched indicates where techniques have been demonstrated to be capable of smaller resolution. Resolution down into the 10 to 15nm range for lines and spaces is clearly demonstrated and further extensions to smaller features are expected. For example, published exposures at high EUV NAs are not available yet since such tools are not available, but there is clearly potential for further shrinking just based on scaling principles. Comparing these techniques' capability and expected time frame for implementation of the dimensions shown in Table LITH1 gives the options for each pitch range shown in LITH1B and LITH1C. They show possible options and timing for line and space patterning.

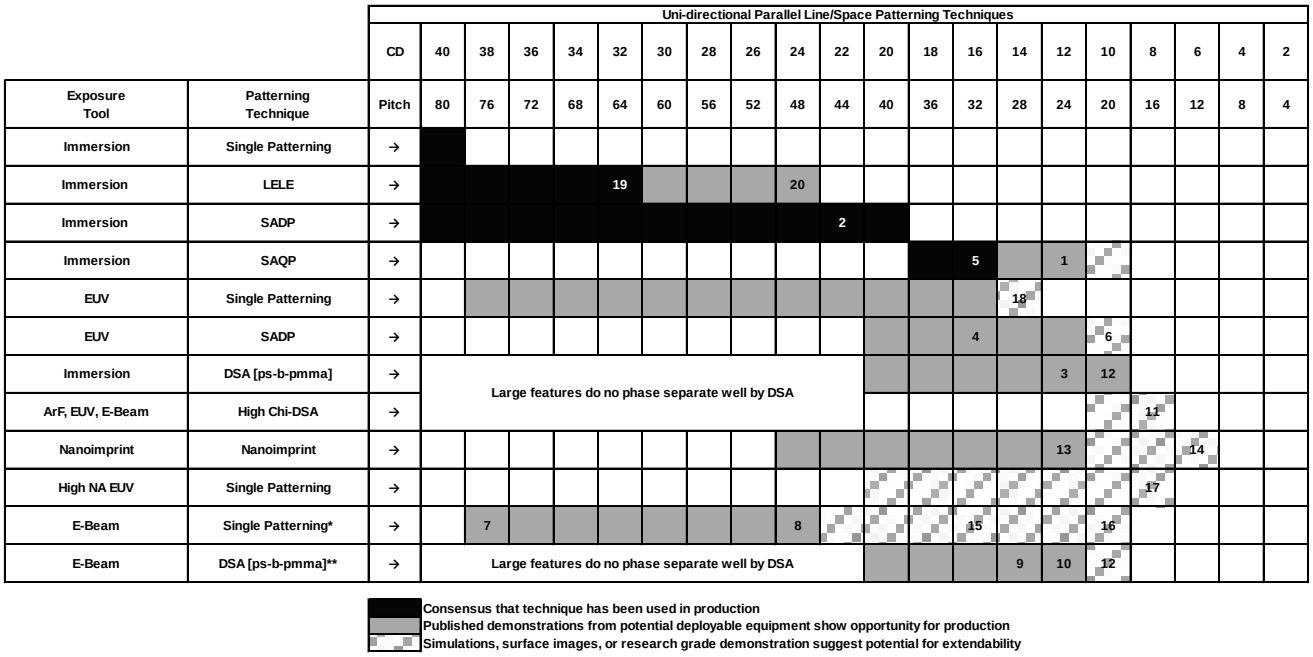

Figure LITH1A Demonstrated Line and Space Resolution of Potential New Patterning Techniques[4]

Figure LITH1B shows the possible options for patterning flash memory lines and spaces and for patterning fin levels in finFET type logic devices. Flash memory critical dimensions already require the use of Self Aligned Quadruple Patterning (SAQP). Since SAQP and 193nm immersion can resolve down to 12nm lines and spaces, and 2D flash half pitches plateau at this size, there is not a definite need for an alternative patterning technique for these levels. Replacement of SAQP for flash levels by an alternative patterning techniques will then depend on cost considerations. The earliest some alternative could be ready to be used in manufacturing is 2016. Implementation of an alternative technique for this sort of pattern will depend on whether it is expected to be cheaper than already demonstrated quadruple patterning. In 2022, when fin dimensions become smaller than the smallest flash dimension some novel technique will be required to resolve those feature sizes.

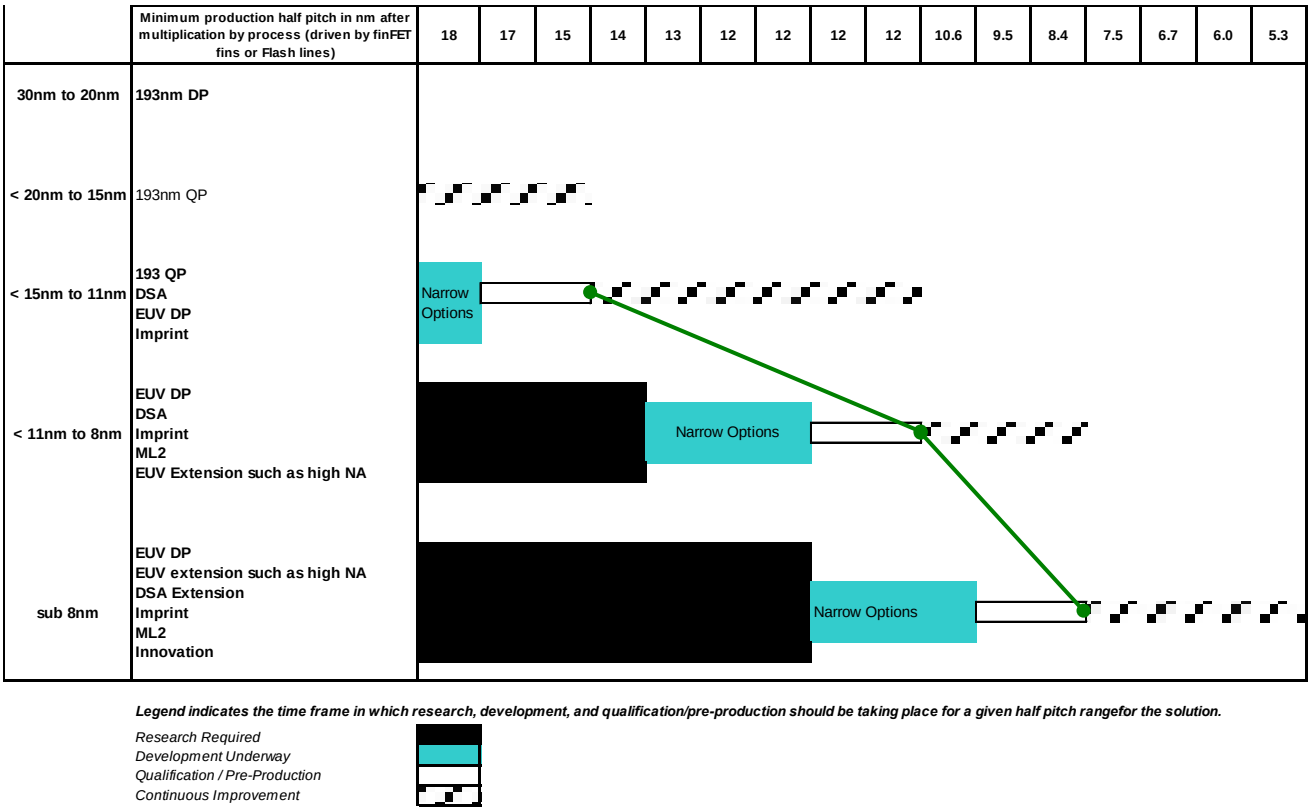

Figure LITH1B MPU Fin and Flash Memory Potential solutions

Figure LITH1C shows the possible options for metal levels in MPUs and DRAMs. These types of line and space patterns can have more complicated patterns and need litho etch litho etch type multiple patterning or require complementary lithography and cut levels to address design issues. Metal level minimum half pitches in production shrink below 20nm in 2018. At that time, quadruple pattering could be used. But the necessity to have cut levels or to have more than two LE steps will drive a need for a simpler and less expensive patterning method. If EUV source powers are such that it is cheaper than quadruple pattering, this would be a natural technique for these levels. DSA is expected to be the lowest cost patterning technology for these line and space levels, but has to resolve defectivity and design issues to be usable. The earliest this is conceivable is 2016. Nanoimprint and maskless lithography are also potential solutions for lines and spaces. Nanoimprint has to make substantial defectivity progress. Because of this, its first possible implementation is in relatively defect tolerant parts such as flash memory. Maskless lithography will not have production grade tools ready in 2016, so it is an option only for later nodes.

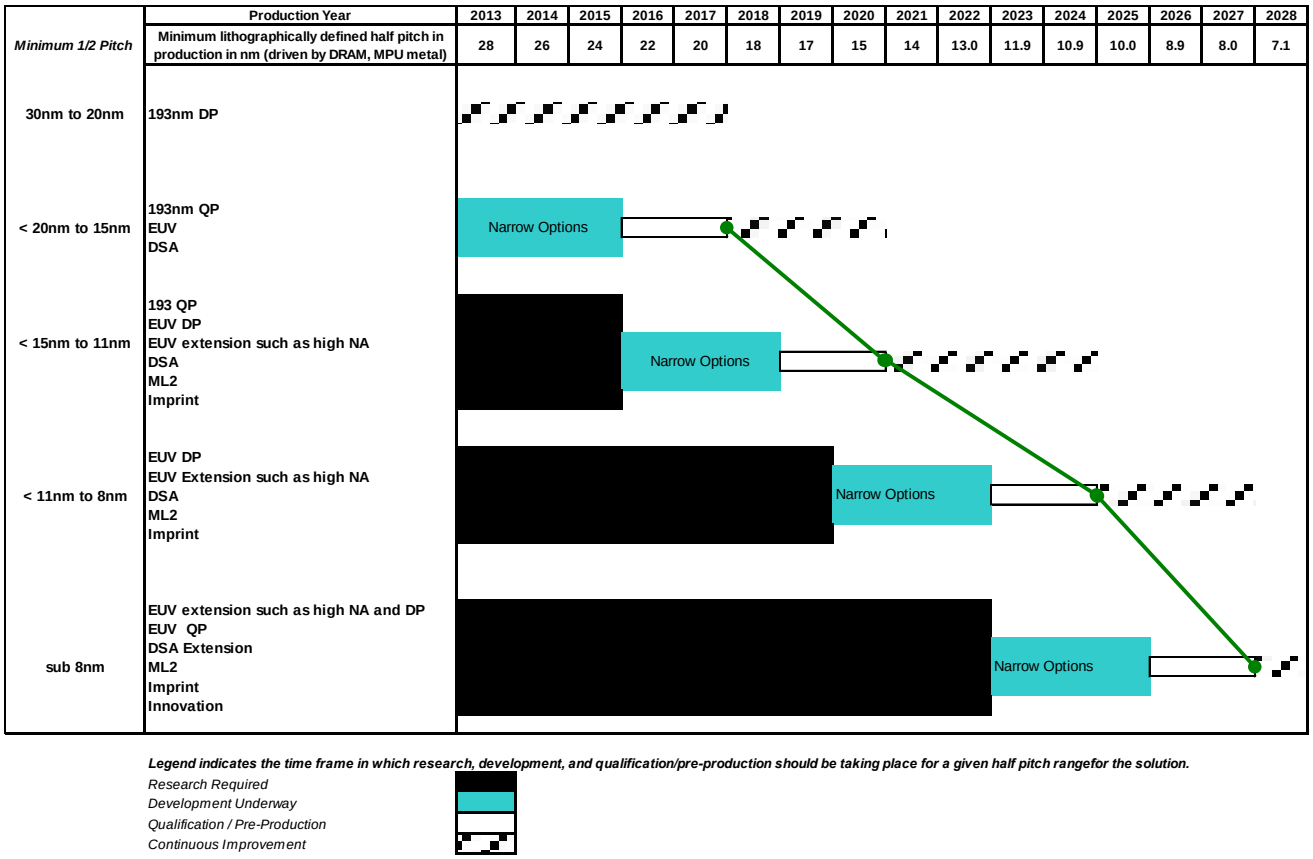

Figure LITH1C MPU and DRAM Metal Level Potential Solutions

Possible options for contact hole types of layers are shown in Figure LITH1D. The two-dimensional nature of contact hole arrays means that pattern doubling reduces the minimum achievable pitch of a contact hole array by one over the square root of two, or by 29%. This is much less shrink than the pattern doubling of lines and spaces, where the minimum pitch is reduced 50% by pattern doubling. Triple and/or quadruple patterning of contact holes will be needed in 2016 and more than four exposures in 2019. The implementation of EUV or other novel pattering techniques would shrink the pitch of contact holes just as much as it shrinks the pitch of lines and spaces. So the expected cost of LELELE and LELELELE processes drives an earlier need for novel pattering technology for contact holes than for lines and spaces. In 2016, EUV single patterning could replace triple or quadruple patterning for contact holes. If successful at this, it could remain the technique of choice for contact holes until 2022. But source power has to be enough to make such patterning manufacturable and cost effective. Other alternative technologies are also possible. They are shown as possibilities for manufacturing in 2019, when 193nm immersion quadruple pattering no longer meets resolution needs. But they could be implemented sooner if they are ready and more cost effective than other techniques.

CH Pitch	Production Year	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
	Minimum DRAM contact pitch	85	78	72	66	60	55	51	46	43	39	36	33	30	28	25	23
	Minimum logic contact pitch	144	115	115	102	91	81	72	64	57	51	46	41	36	32	29	26
100nm to 72nm (50nm to 36nm half pitch)	193nm DP																
< 72nm to 54nm (< 36nm to 27nm half pitch)	193 Triple or Quadruple Patterning EUV SP DSA	Narrow Options															
< 54 to 36nm (< 27nm to 18nm half pitch)	EUV SP 193nm 4+ exposures ML2 Imprint DSA		Narrow Options														
sub 36nm (sub 18nm half pitch)	EUV Extension such as high NA EUV DP DSA ML2 Imprint			Narrow Options													

Legend indicates the time frame in which research, development, and qualification/pre-production should be taking place for a given half pitch rangefor the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Figure LITH1D Contact Hole Potential Solutions

5. Specific Technology Requirements and Potential Solutions

5.1. Resist Requirements

Photoresists need to be developed that provide good pattern fidelity, good line width control, low line width roughness, and few defects. As feature sizes get smaller, defects and monomers will have comparable dimensions with implications for the filtering of resists. See Table LITH3. Resists for 193nm lithography are reasonable mature and, since 193nm lithography is not increasing its resolution, further improvement in this capability are not needed. EUV resists have already shown resolution down to 14nm half pitch for lines and spaces and to 22nm half pitch for contact holes. Resolution better than this for EUV won't be needed until 2022 per the potential solutions tables discussed above. So resist resolution per se is not a critical challenge.

Multiple patterning helps with resolution, but CD control can still be an issue, since CD variation affect the position of line edges and this affects the position of some double patterned features. More importantly, device requirements continue to scale. Line edge roughness (LER) and line width roughness (LWR) targets continue to be issues and affect device performance. High frequency line width roughness affects profiles and interconnects wire resistance. Line width roughness at lower spatial frequencies results in variations of transistor gate length over the active region of the device. This variation increases leakage and causes the speed of individual transistors to vary, which in turn leads to IC timing issues. The line width and line edge roughness also contributes to the CD uniformity error budget for small gate lengths and long LER/LWR correlation lengths. The LWR spec in the table is set at 12% of physical gate length and allows a certain amount of undesirable variation in device performance. Device manufacturers would like as little variation as possible, so these numbers reflect the maximum variation. Better control would immediately translate into better devices and is very desirable. Post-exposure Bake (PEB) temperature sensitivity also affects CD control and so also will be a challenge in the future as CD control requirements get tighter. Table LITH3 shows overall resist requirements.

Table LITH3 Resist Requirements

If EUV resist is used, requirements for LWR and LER are the same. However, the actual lines being imaged will be smaller since less pattern multiplication will be used. Assuming chemically amplified resist is used; the shrinking printed feature sizes will probably increase the LWR. It is easier to get low LWR and critical dimension uniformity (CDU) in chemically amplified resists by formulating them for slower photospeed. However, the limited brightness of current EUV

sources makes this approach low in scanner throughput and thus very expensive. So LWR and the related contact hole CDU are big challenges for EUV resists.

There are other areas in which better patterning materials can help meet requirements. These areas are described in more detail in the discussion of Table LITH10.

5.2. OPTICAL MASK REQUIREMENTS

Table LITH4 Optical Mask Requirements

In the 2013 revision, there are no major changes beyond minimal roadmap maintenances to the 2011 edition of Table LITH4. Most of the changes from 2011 follow from the fact that mask patterns will stop shrinking with wafer patterns according to scanner reduction. Various multiple-patterning techniques use side-wall spacers to define wafer patterns, or apply significant etch bias or other post-lithography process bias. In all cases, the simple correspondence of mask dimensions to wafer dimensions is lost. Mask features will continue to shrink to about 80 nm, corresponding to a 3:1 duty cycle at 320 nm pitch (80 nm pitch at wafer scale). The rapid growth of data volume per mask will also slow significantly when we reach this limit. Data volume per layer will continue to grow as before; it will just be split among multiple masks.

Although mask patterns may stop shrinking, CD control and overlay tolerances must continue to track wafer requirements. These are the most challenging requirements for optical masks. In multiple exposures, the position of the edge of a mask feature can become the position of a line. Better mask CD control and a better mask error enhancement factor (MEEF) are required to prevent overlay errors coming from CD errors on the mask or from elsewhere. This also drives greater sensitivity of image errors to mask errors and can force attention to minimizing MEEF through mask and pattern design. Positional errors on the mask also have to get smaller. This may force more reliance on computational lithography and double patterning mask designs that look less like the target features.

5.3. MULTIPLE PATTERNING/SPACER TECHNOLOGY

Meeting the required resolution using an optical wavelength is driving the use of multiple exposures to define each device layer. Some double exposure techniques are already being used, including alternating phase shift plus trim and double dipole exposures. These techniques allow for imaging at closer to the diffraction limit (k_1=0.25). Further multiple exposure techniques have been designed to form images beyond the single-exposure diffraction limit; these place additional requirements on lithography that vary by the specific type of multiple exposure technique *(*Table LITH5).

Two basic processes, *pitch splitting* (PS) and *spacer patterning* (SP), and their requirements are defined by the differences in their critical lithography patterning steps. PS includes the traditional double *patterning* (DP) of two separate lithography/etch steps to define a single device layer, often called (litho etch litho etch [LELE]), and double exposure (DE), which is two lithographic exposures into one material with only one etch step. This can incorporate non-linear resists or a litho freeze process. The SP process uses one critical lithography step and then additional thin film deposition and etches steps in a spacer-like process to define two sets of critical features. (Note that this process also requires a second cut mask similar to the dipole lithography cut mask.) Spacer double/multiple patterning eliminates one or more critical exposures, but the allowable shapes are limited because the single exposure defines the location of the features. Figure LITH2 is a schematic of the process flows for these different approaches.[5, 6, 7, 8] Spacer type double pattering can give features with better LWR than single resist patterning , but has less design flexibility than LELE type processes. Both of these types of multiple patterning can be extended to quadruple pattering or even octuplet patterning. LELE type processes will have sufficient resolution for logic or DRAM metal patterns until 2016 or 2017, depending on the complexity of the particular layer. For hole type patterns, which require LELE type patterning triple or quadruple patterning will be needed in manufacturing in 2016 or earlier. Spacer double patterning is already in use for logic fin patterning and for flash memory devices and quadruple is already in use for flash memory production.

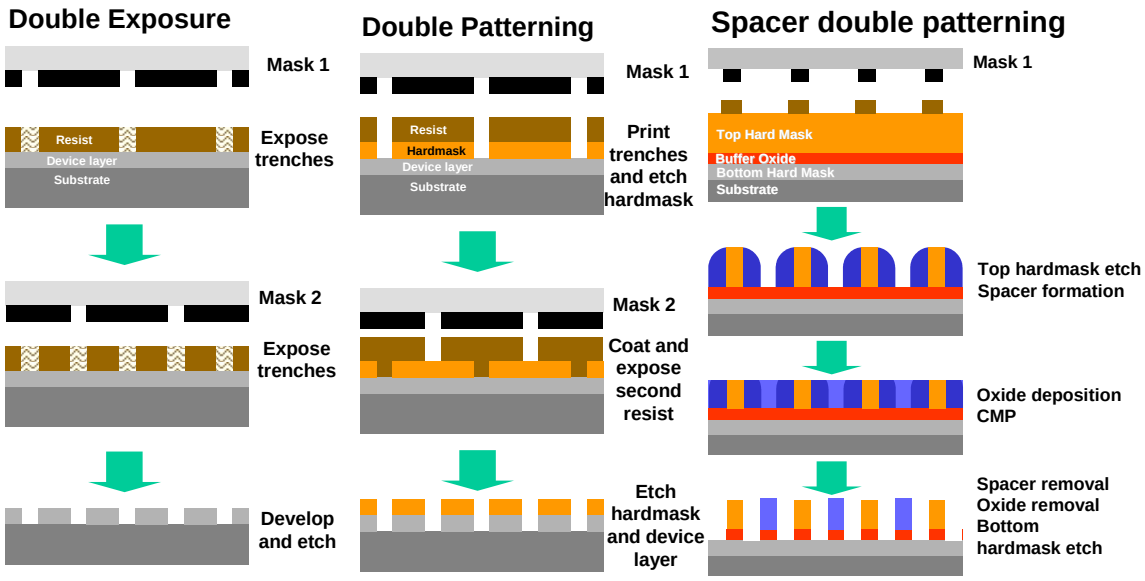

Figure LITH2 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

In general, multiple patterning processes have the following challenges

- Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
- Photoresists with independent exposure of multiple passes
- Implementing and controlling additional process steps for spacer technology
- Fab logistics and process control to enable low cycle time impact efficient scheduling of multiple exposure passes and/or additional process steps for spacer technology.
- Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining a minimum amount of "pitch doubling/spacering steps" for arbitrary designs
- Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
- Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
- Lithography and pitch splitting/spacering friendly design and design for manufacturing (DFM)

In some cases a particular combination of LELE and spacer defined patterning is referred to as "Complementary Lithography". In this case, rather than dividing different lines from the final pattern into two different masks and doing LELE, a fine pitch array of long lines is prepared using one exposure and spacer multiple patterning. After the pattern is doubled a second exposure and etch step is used to make "cuts" in the array of lines or to remove unwanted lines. Since hole patterns can't be printed on the same pitch as the lines as the final array of lines, more than one litho and etch cut step may be used. This process has overlay advantages and can give relatively low LWR but requires that all the features go in one direction and have no bends.

Table LITH5 Multiple Patterning/Spacer Requirements

The multiple patterning table is divided into three parts, leading with half-pitch requirements for the different device types, followed by two process requirement sections: Generic pitch splitting by multiple exposures and pitch splitting by sidewall spacer double and quadruple patterning. The roadmap for *Generic Pitch Splitting* is driven principally by MPU metal half-pitch while the *Spacer Patterning* requirements are driven principally by NAND-Flash; as such the lithography requirements are substantially different for each technique. The fundamental premise is that both the line and the space must meet the 12% after etch CD control specification. Since the space depends on the overlay and printed line width, meeting the 12% specification drives the overlay specification for multiple exposure double patterning and drives CDU

specifications for spacer patterning techniques. In both cases, control of space CDU (and thus overlay requirements) is convoluted also with CD control for the line. Therefore, to make the overlay specification as large as possible, process requirements for manufacturing steps which control the line CDU are also tightened to the fullest extent of existing process capability.

Definitions: In this section, MTT refers to wafer mean-to-target; i.e. for 32nm half-pitch SADP a mandrel target is 32nm. A wafer with a mean of 33nm has a MTT equal to 1nm. Likewise, the sidewall spacer would have a target of 32nm. A wafer with a sidewall spacer measuring 33nm would have a MTT equal to 1nm. MTT for mandrel and spacer are important because they generate placement errors of the lines and spaces (similar to overlay in litho-etch-litho-etch). In these tables, CDU refers to the combined 3-sigma for inter-field and intra-field locations. MTT + 3sigma refers to the root-mean-square of the two errors, where NAND flash requires that all features have MTT + 3sigma <12% after factoring in the various tolerance stack-up contributions for each feature type.

Figure LITH3A shows the spacer double patterning process schematic with feature definitions, and Figure LITH3B shows the spacer quadruple patterning process with schematic and feature definitions. Note that the sidewall spacer quadruple pattering scheme is nothing more than two cycles of sidewall spacer double patterning. There is, however, the addition of a new data pool for spaces (called "spacer defined space") see Figure LITH3B. Space #1 and #3 (indicated in Figure LITH3B) are defined as "spacer defined space" because they originate from the first spacer deposition. Space #2 is defined as the "core space" (similar to double patterning) which originates from the first mandrel (core) and space #4 is defined as the "gap space" (similar to double patterning) which originates from the gap space formed between the first two spacers. In both the spacer double patterning and spacer quadruple patterning, the "gap" space contains the most tolerance stack-up and is the performance limiting feature which drives the manufacturing process error budgeting. The numbers in the sidewall spacer section of the table are all for quadruple patterning, since that is in production already. Flash minimum half pitches are not expected to shrink below 12nm, so quadruple pattering suffices for all flash dimensions shown. However, fin half pitches are expected to drop below 10nm in 2023. If multiple patterning is to be used for these dimensions it will have to be octuple patterning at that time.

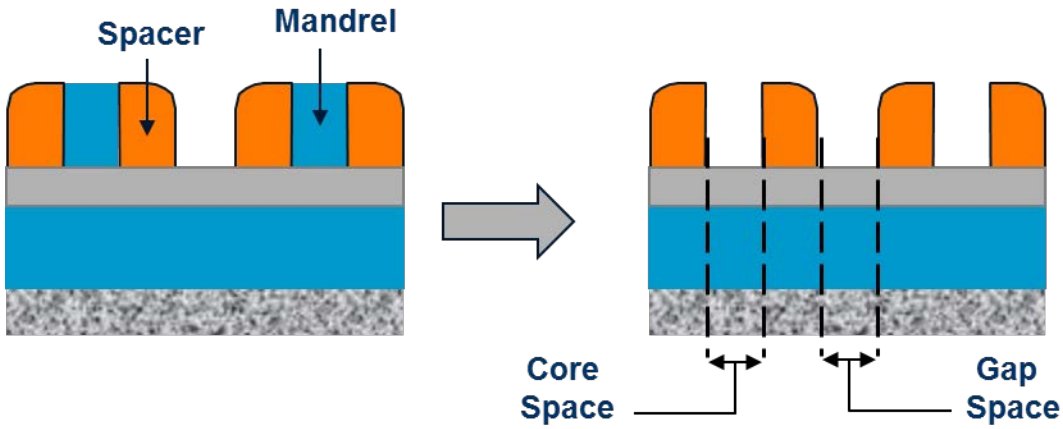

Figure LITH3A Schematic of Positive Tone Sidewall Spacer Double Patterning, with Definition of "Core Space" and "Gap Space". Gap space always has the greatest tolerance stack-up.

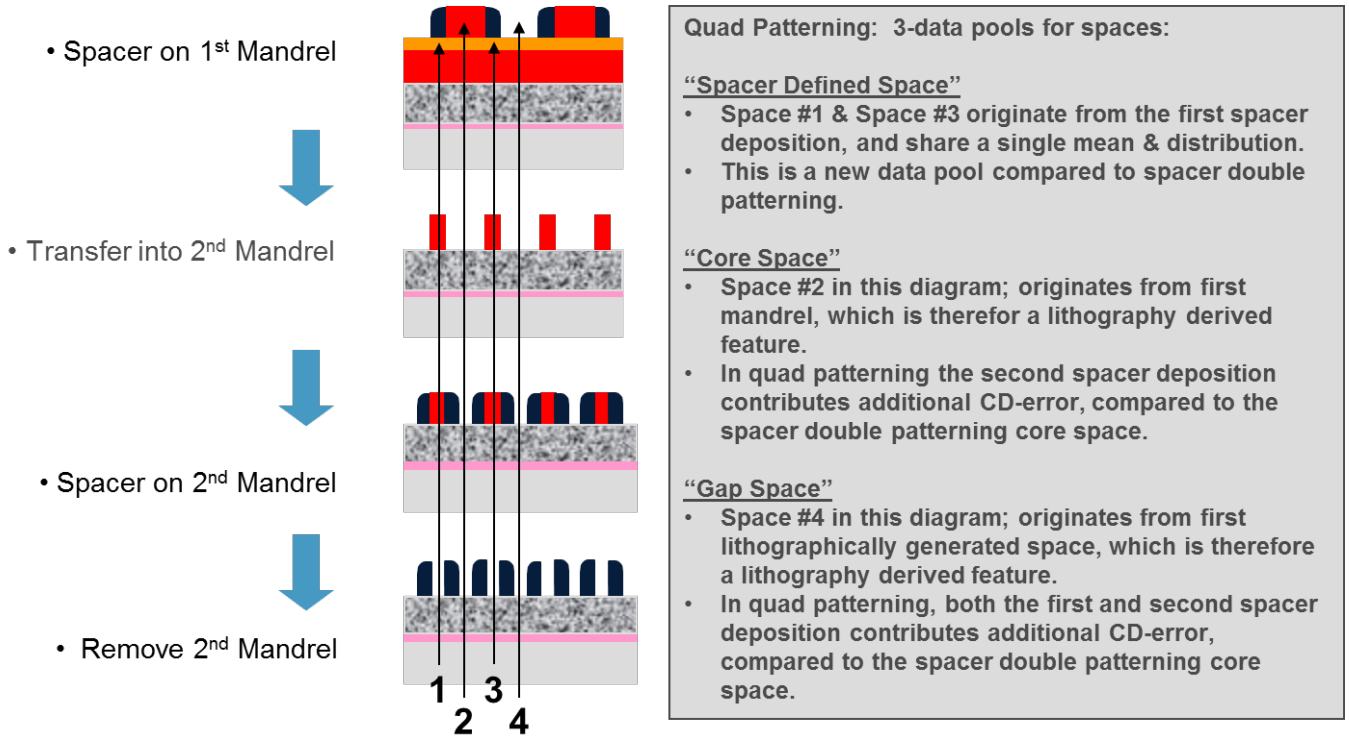

Figure LITH3B Schematic of Sidewall Spacer Quadruple Patterning, Indicating and Defining the Various Data Pools for Spaces

Manufacturing Process Capability: The two performance limiting steps within a sidewall spacer patterning scheme are (1) the CD control of the mandrel and (2) the CD control of the spacer deposition process. When referring to the mandrel, some processing techniques utilize photo-resist as a mandrel while other techniques use resist as a mask to etch a mandrel into another material. In the former case, the photo-lithography process must meet the mandrel CDU (combined inter-field and intra-field 3-sigma) along with MTT; in the latter case, where the mandrel is formed by litho and etch, the final etched mandrel must meet the listed CDU and MTT performance requirements. The CD control of the spacer deposition process also has both CDU and MTT requirements. The ITRS lithography working group uses the following error budgeting guidelines, so that all features will meet the MTT + CDU < 12% requirements: mandrel CDU < 6% of half-pitch, mandrel MTT < 4% of half-pitch, spacer deposition < 3% of half-pitch for both MTT and CDU. More error budgeting is allocated to the mandrel than to the spacer deposition because of the greater challenges to control this dimension. Regarding the mandrel, more error budget is allocated to the within wafer CDU, which is a combination of both inter-field and intra-field, than to the wafer's MTT. Figure LITH3C shows the corresponding equations and percentages for the various table rows related to spacer patterning. Note that "gap space MTT + 3sigma" is 11.1% during the double patterning era and 10.8% during the quadruple patterning era, which is the performance limiting feature. Also note that "spacer defined space" appears as a third data-pool for spaces after the transition to quadruple patterning. Additionally, to accommodate the additional tolerance stack-up involved with the spacer quadruple patterning process, the error budget for the spacer deposition process tightens to 2% of half-pitch.

	A	B	C	D	E	F	G	H	I	J	K
1			SADP Formula's					SAQP Formula's			
2											
3		NAND 1/2 pitch	Half-Pitch	100%	22	20		Half-Pitch	100%	15	12
4											
5	Mfg. Process Capability	Mandrel CDU	=6%*C3	6.0%	1.3	1.2		=6%*H3	6.0%	0.9	0.7
6		Mandrel MTT	=4%*C3	4.0%	0.9	0.8		=4%*H3	4.0%	0.6	0.5
7		Spacer CDU	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
8		Spacer MTT	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
9											
10	Resulting Patterning Performance	Line CDU	=C7	3.0%	0.7	0.6		=H7	2.0%	0.3	0.2
11		Line MTT	=C8	3.0%	0.7	0.6		=H8	2.0%	0.3	0.2
12		Line MTT+3sigma	=SQRT(C7^2+C8^2)	4.2%	0.9	0.8		=SQRT(H7^2+H8^2)	2.8%	0.4	0.3
13		Core Space CDU	=C5	6.0%	1.3	1.2		=SQRT(H5^2+(2*H7)^2)	7.2%	1.1	0.9
14		Core Space MTT	=C6	4.0%	0.9	0.8		=SQRT(H6^2+(2*H8)^2)	5.7%	0.8	0.7
15		Core Space MTT+3-sigma	=SQRT(C5^2+C6^2)	7.2%	1.6	1.4		=SQRT(H13^2+H14^2)	9.2%	1.4	1.1
16		Gap Space CDU	=SQRT(C5^2+(2*C7)^2)	8.5%	1.9	1.7		=SQRT(H5^2+(2*H7)^2+(2*H7)^2)	8.2%	1.2	1.0
17		Gap Space MTT	=SQRT(C6^2+(2*C8)^2)	7.2%	1.6	1.4		=SQRT(H6^2+(2*H8)^2+(2*H8)^2)	6.9%	1.0	0.8
18		Gap Space MTT+3-sigma	=SQRT(C16^2+C17^2)	11.1%	2.4	2.2		=SQRT(H16^2+H17^2)	10.8%	1.6	1.3
19		Spacer Defined Space CDU						=H7	2.0%	0.3	0.2
20		Spacer Defined Space MTT						=H8	2.0%	0.3	0.2
21		Spacer Defined Space MTT+CDU						=SQRT(H7^2+H8^2)	2.8%	0.4	0.3

Note that "gap space MTT+3sigma" is 11.1% during the double patterning era and 10.8% during the quadruple patterning era, which is the performance limiting feature. Also note that "spacer defined space" appears as a third data-pool for spaces after the transition to quadruple patterning. All features have MTT+3Sigma < 12% per NAND flash requirements.

Figure LITH3C Corresponding Equations and Percentages for the Various Table Rows

For current NAND layouts, the cut (trim) mask overlay requirements are quite relaxed. Although NAND flash is driving the half-pitch scaling, there are other spacer patterning user groups, such as those using spacer patterning to produce fins (FinFET devices) and active islands (DRAM) using line and cut techniques. These approaches will have moderately aggressive overlay requirements and scale with the spacer pattern array pitch. A cut mask must be applied for the purpose of cutting lines, removing dummy-fins on pitch, or blocking trenches in BEOL patterning. A row specifically addressing the overlay requirements for spacer cutting (or trench blocking) is added to the spacer patterning section. Figure LITH3D shows a schematic and equation for approximating these overlay requirements. It is assumed that a cut mask (for a single line cut) is designed with edges that fall exactly half-way between spacers. Thus, as a first order approximation the alignment tolerance without guard-banding is ¼ of the array's pitch. From this starting point, we need to guard-band by the placement shift of the spacer, which results from CD errors on the spaces. The tolerance stack-up analysis shows that the gap space has the most CD error, and will generate the maximum spacer placement offsets; therefore we need to guard-band by the gap space (MTT + 3 sig)/2. Secondly, we need to guard-band by the CDU control of the cut mask opening. Assuming a cut mask opening equal to the array's pitch, and assuming a CD control of that feature of 5%, then we need to guard-band by an additional 5% of the array's pitch. Thus the equation presented in the table is that overlay requirements for applying cut masks to a spacer patterned array (Fin cutting, DRAM island cutting, dummy line removal, etc.) is equal to 25% of the pitch minus gap space (MTT+3sigma)/2 minus 5% of pitch. Please note that NAND cut masks are substantially relaxed.

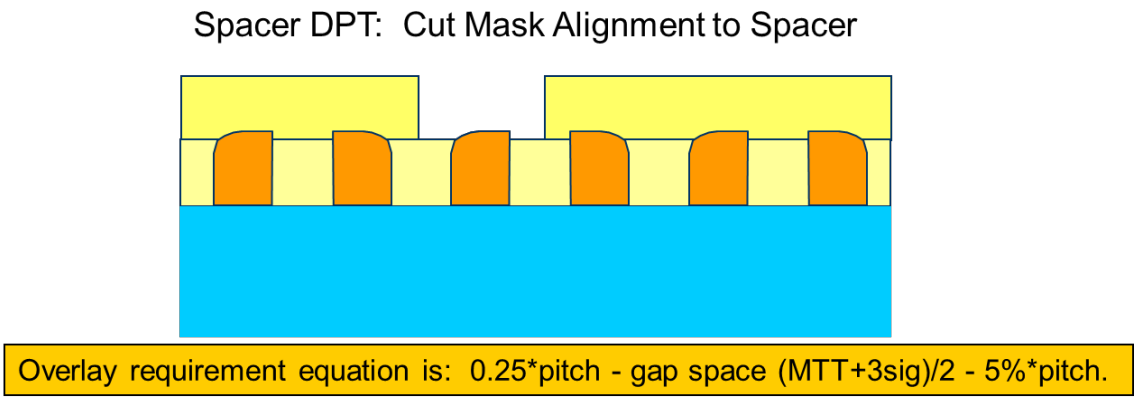

Figure LITH3D Schematic of a Cut Mask applied to a Spacer Array for the Purpose of Line Cutting, such as in Fin formation, DRAM island formation, or dummy fin removal, where one needs to critically cut one line on pitch. The equation describes the overlay requirements of the cut mask accounting for the various guard-banding due to spacer placement errors and cut mask CD-control errors.

5.4. EUV TECHNOLOGY – SOURCE POWER

Source power is a critical challenge for EUV lithography. The EUV exposure tools currently in use and being shipped have met targets for resolution, overlay, aberrations and other lens and stage performance metrics. But actual source powers have improved very slowly and limit current pilot type EUV exposure tools to perhaps 5 wafers per hour of throughput. This throughput is so little that building a factory with such tools would be financially and logistically impossible. Roadmaps for EUV exposure tools have projected sources rising from their current power of perhaps 10W of power at intermediate focus to 250W. 250W is projected to give roughly 125 wafers per hour using a 15mJ/cm^2 photoresist. But any increase in power significantly above the 10W level has proven very challenging.

Originally there were two approaches to generating EUV light, Discharged Pulsed Plasma (DPP) and Laser Pulsed Plasma (LPP). Now only LPP is in use in new EUV exposure systems. In DPP an electric spark is used to excite a tin plasma and in LPP a powerful laser is used to excite individual droplets of tin. Many sparks or laser bursts are used to create the total power for one exposure dose. The conversion efficiency to EUV light is low, on the order of 3%, and light of many wavelengths along with substantial tin debris is produced. The light is collected and focused with an EUV mirror or mirrors. The tin debris has to be controlled or removed so that it doesn't coat the mirrors and the light of unwanted frequencies has to be filtered or otherwise reduced or eliminated. Reaching high enough laser power with sufficient repeatability and dose control, alignment of the lasers pulses so that the accurately target the tin droplets at a fast repeat rate, getting sufficient conversion efficiency, preventing the source from being affected by tin debris, and thermal management are among the challenges LPP sources face.

Sources are already several years behind original projections for power. This has made the insertion point for EUV shift to smaller nodes. Even getting source power to the current level with reasonable availability was more difficult and more delayed than expected. Until the industry sees substantial increases in source power, no semiconductor maker will commit to EUV as a manufacturing technology. So source power is the biggest near term challenge for EUV.

5.5. EUV TECHNOLOGY – RESIST

Resist requirements for EUV are the same as the requirements in the resist table. Increasing resist resolution is a significant challenge but one the materials industry has a history of meeting given the availability of aerial images with reasonable contrast. But even if resolution is met, the key challenge will remain the control of stochastic effects leading to pattern variations such as LER, LWR and CDU. These stochastic effects come from both the resist chemistry and from the shot noise variation in impinging and absorbed photons. This is expected to be the most difficult challenge facing EUV resists.

5.6. EUV TECHNOLOGY – MASK

EUV mask issues are numerous, involving many new challenges that must be met simultaneously. Major challenges are:

- Mask yield & defect inspection/review infrastructure to support HVM ramp-up:
    - EUVL mask blank defect and yield
    - EUVL mask blank infrastructure including substrate defect inspection, actinic blank inspection
    - EUVL patterned mask infrastructure including actinic mask inspection and EUV AIMS
- Keeping masks defect free during use:
    - Availability of pellicles meeting HVM requirements
    - Minimizing defect adders during use
- Cost control and return on investment for mask making and production

Masks will require low thermal expansion (LTEM) substrates, zero-defect multilayer reflecting surfaces, and new pattern absorber materials. The greatest concern is with phase defects, which are either buried in, or propagated from substrate to, the multilayer stack and invisible to standard SEM or optical inspection but still print. For 22 nm half-pitch lithography those defects can be as small as sub-20nm. The infrastructure for detection and review of such small defects is still being developed in several industry programs. So stopgap tools and/or processes need to be used in pilot lines until commercial substrate, blank, and patterned mask inspection and review tools capable of supporting HVM become available.

Table LITH6 EUVL Mask Requirements

5.6.1. EUV MASK BLANK DEFECTIVITY AND MITIGATION, MASK AVAILABILITY

Availability of defect free masks has been regarded in the last several years as one of the top two priorities for EUV high volume manufacturing (HVM). EUV printing defects can derive from traditional opaque defects in the patterning layer as well as from defects originating from the EUV mask substrate or can be generated by a defect in the multilayer of the reflective blank. The multilayer defect can create phase and/or amplitude distortions when imaged. The specifications in Table LITH6 are based on a worst-case defect approach as is done with all the defect specifications in the roadmap. Thus the defect specification is targeted as the size of a 180 degree defect, which is 3 nm high for an EUV reflective mask. As is noted in the footnote, a 90 degree defect (1.5 nm high) will also cause a CD defect if it is about twice the specification size. Another major challenge is that these phase defects are beyond the limits of today's metrology capability, making them difficult to observe and improve upon. Currently, the defect inspection and review infrastructure, such as substrate, blank, patterned mask inspections and AIMs, needed for EUV mask manufacturing at the 16 nm half-pitch is being developed.

Although methods for repairing EUV blank defects have been proposed,[9,10] a practical means for repairing every EUV blank defect is not feasible. An alternate approach has been embraced in the industry is known as "pattern shift" or, more generically, "defect mitigation." The impact of a blank defect is mitigated by shifting the location of the blank defects relative to the mask pattern so that the defect is underneath the absorber. The absorber material absorbs strongly enough at EUV wavelengths, so only defects located on the exposed multilayer will result in a printing defect. Those that are under absorber will not.

The pattern shift process has multiple steps. First, fiducial marks are made on the EUV mask blank to provide alignment points. Second, blank inspection aligned to the fiducial marks provides information on the number, size, type and location of the blank defects. Third, the pattern shift calculation is performed combining the pattern data and blank defect data to generate the pattern shift vector and the blank rotation value. Finally, the aligned mask writing with the shift and the rotation is completed. Ultimately, the effectiveness of the pattern shift depends on the pattern density, defect size, number of defects, location accuracy of the defects and the alignment overlay of the mask writing process.[11,12,13]

Table LITH6 now includes a row to reflect "blank defect size with mitigation" to impose a more achievable maximum defect size for blank development. Since it is difficult to predict a unified quantification of all the error sources contained within pattern shift, nor embody a typical design, the minimum primary feature was selected to describe that size limit. It provides a scalable, defined parameter rather than a parameter that can be correlated directly to the success rate of pattern shift. Details of the exact size and number of defects that can be mitigated by pattern shift are too application-specific to be included in this table. Any attempt to do so would over-simplify the challenge and potentially mislead the industry.

5.6.2. EUV MASK TECHNOLOGY EXTENSION

Because the insertion of EUV lithography into manufacturing has taken longer than expected, EUV extendibility options are receiving increasing scrutiny. It now seems likely that the first high volume manufacturing (HVM) EUV exposure tools will be equipped with 0.33-NA projection optics and be able to support a variety of conventional (0.9σ) and off-axis illumination (OAI) modes.[14]

Once the contrast improvements that are possible with advanced illuminators have been made, including those that utilize lower pupil-fill-ratios, further improvements in the resolution of EUV systems will require higher numerical aperture projection optics or the introduction of 0.33 NA EUV double patterning techniques (DPT). Which of these extendibility options are ultimately employed in production will depend on exactly when EUV tools with high-NA projection optics become available and whether or not DPT EUV turns out to be a cost effective alternative to multiple patterning 193nm immersion lithography.

EUV exposure tool roadmaps from the major scanner companies[15,16,17] suggest that high NA systems will not be available until at least 2019, and it is possible that DPT EUV using 0.33 NA tools may be needed before EUV exposure tools with NA >> 0.33 become available. The values for EUV NA in Table LITH1have been updated to show 0.33 NA from 2013 – 2020 and a higher NA needed after that. This corresponds to the year in which DRAM and Logic metal level half pitches will be smaller than the single patterning limit for EUV. This limit assumes these patterns are not totally one-dimensional and require a Lith-Etch-Lith-Etch (LELE) type of process with EUV instead of an SADP type process if they are to be double patterned. In this case a higher NA EUV system is expected to be cost effective and allows more flexible patterning than doing EUV LELE at 0.33NA

There are two routes to higher NA EUV imaging: increasing the chief-ray-angle at the mask (CRAO) or increasing the imaging system demagnification above its current value of 4X. Increasing NA above 0.33 while maintaining the current 4X demagnification ratio leads to a wider range of imaging angles at the mask. It would decrease the net reflectivity,

which in turn would lead to reduced system transmission or lower tool throughput; it would increase 3D mask effects, which would lead to a larger shadow effect; it would create larger telecentricity errors; and it would give a substantial reduction in image contrast. The use of a more complicated multilayer stack on the EUV reflective mask can mitigate some of these effects, as can a thinner patterned absorber film, but the net effect will be EUV exposure tools with lower productivity and still worse aerial images. Because of this, higher NA EUV imaging systems that keep the current chief ray angle by employing higher demagnification ratios appear to be the better option. However, as the demagnification ratio increases either the image field must get smaller or the mask size must increase. Full-field high-NA imaging system designs will likely require more than 6 mirrors. Eight mirror designs will have only about 40% of the transmission of 6 mirror designs. A large number of 6 and 8 mirrors high-NA imaging system designs have already been explored.[18] Which high-NA EUV designs are acceptable to EUV stakeholders (chip makers, mask makers, tool and material suppliers) is currently the subject of an intense industry wide debate. While no decisions have yet been made, the leading high-NA candidates employ 6 mirrors, utilize a 6^0 CRAO, and make use of 8X demagnification ratio. This option will have image fields that are one quarter of the size of current full-field systems, i.e., 13 mm x 16.5 mm. The implications of such a choice are that the pattering of a full 26 mm x 33 mm chip with a quarter field system will require the use of stitching and/or a larger mask.

Since the current leading high-NA design choices involve quarter-field 6-mirror imaging systems utilizing 8X demagnification, the values for mask magnification in Table LITH6 have been updated to show mask magnification increasing from 4X to 8X in the ~2019 time frame. The year 2019 is specified because mask houses will have to produce such mask for pilot line use two years before volume production at high NA in 2021.

Up until this year, 4X has been the only mask magnification considered in Table LITH6. Many table values are calculated by multiplying a mask error allocation times a wafer dimension times the mask magnification. For example, the mask image placement value is calculated as 15% of the wafer overlay and is multiplied by the mask magnification. When an 8X mask magnification comes into use, the mask feature dimensions become twice as large and somewhat easier to manufacture. At that time, the error allocations between the mask and the wafer will be renegotiated between mask manufacturers and wafer lithographers. For the values in Table LITH6 derived from 8X mask magnification, we assume that about half of the benefit of larger mask magnification will go to the mask manufacturer and about half to the wafer lithographer.

To fully reflect the ongoing industry high-NA lithography discussions, Table LITH6 includes possible mask size increases and their potential impacts to EUV mask making capabilities. Any mask form factor increase will have much more profound impact to EUV mask infrastructure. Time line for such a possible change is synchronized to that of a potential mask magnification change which in 2019.

EUVL embedded phase shift masks (EPSM) can further extend the lithography resolution limit and provide better pattern fidelity as compared to EUVL binary masks for the 16nm node technology and beyond generations. EUVL EPSM absorber most likely will be a stack that contains two to three different materials to simultaneously satisfy mask inspection, phase, and reflection requirements at EUV wavelength. The EUV EPSM phase and transmission mean-to-target and uniformity control, therefore, depend on the absorber thickness control. In the Table LITH6, the specification of the absorber thickness control of 1.1% range reflects 2-degree phase and 3% transmission control range from that of the target values.

EUVL alternating phase shift masks (APSM) is likely needed for the 11nm (half pitch) technology generation and beyond. The fabrication of EUVL APSM is more difficult than EUVL binary mask or a conventional optical APSM mask. In the case of EUVL APSM, one of the options to create a phase difference in the two regions (0 and 180-degree phase regions) is by etching a phase step in the substrate prior to the ML coating. The step height that induces 180-degree phase mismatch in the ML is determined by $[\lambda/(4\cos\phi)](2m+1)$, where λ is the wavelength, in this case 13.5nm, ϕ is the angle of the illumination where 0 degrees indicates vertical illumination and where m is an integer (0, 1, 2, …). The smaller the step is, the less are adverse imaging effects such as imaging imbalance effects. The challenges of generating a phase step include tight step depth and depth uniformity control, conformal ML coating at the phase edge to minimize phase spread at the phase edge, and availability of EUV phase metrology. The specification for EUVL APSM phase control is similar to that used for optical APSM.

5.7. DIRECTED SELF ASSEMBLY (DSA)

Directed Self Assembly is considerably different in approach than the other potential solutions discussed here. Rather than relying on sophisticated tooling to control the dimensions of the smallest features in a device, it relies on the size of molecules to control dimensions. Thus, a bottle of DSA material comes with a CD and pitch already built in. This is

possible because the size of leading edge chip features is now similar to the size of polymer molecules that can readily be made in the lab.

Specialized polymers called block co-polymers are required for most DSA implementations. These types of polymers are well known. But such polymers with the tight molecular weight distribution, size control and purity needed for semiconductor applications are challenging to make, and are not available on the open market. The molecules have at least two sections, or “blocks”, each of which is composed of different molecules. Typically, there are two sections: one made up of one monomer, and one made up of another monomer. This is called a di-block copolymer. The two sections are chemically connected so that they can’t separate. Such polymers can readily dissolve in a solvent and be spin coated on a wafer. But after the solvent has evaporated from the material, energetically it is often more favorable for all the “A” blocks to be together and for all the “B” blocks to be together. After a thermal or solvent anneal the blocks can rearrange to the most energetically favorable arrangement. Since the blocks are small and bonded to each other it is impossible for there to be one big region of A and one big region of B. Instead, lots of small regions of each are formed. In each such region the blocks of similar composition project into the region from different directions and the attached blocks of the other composition project into a neighboring region. The chemical bonds between the blocks are roughly at the boundary of the region. The size of each block will control the size of the regions that are formed and the size of the molecule will control the pitch of the regions. The ratio of the size of the two blocks controls the type of annealed phase that forms. The types of annealed phases that are readily available to di-block copolymers include lamellae, or layers, cylinders of one phase embedded in the other phase and spheres of one phase embedded in the other phase.

In order for these patterns of phases to be useful, they have to be aligned, or “directed”, into useful patterns. There are many processes to do this. The directing processes fall into two distinct classes, chemoepitaxy, where the patterns are directed by regions on the surface of the wafer that have different affinities for the different polymer blocks; and graphoepitaxy, where physical topography in the wafer guides the features. Schematics of typical guide structures for lines and spaces are shown in Figure LITH4A and examples of typical structures for hole type patterns are shown in Figure LITH4B. The schematics show a cross section through a pattern. In the line and space case the pattern is a long array of parallel lines and spaces. In the hole case the pattern is an array of vertical cylinders with the cut going through the center of a row of cylinders. These patterns then have to be developed through some sort of dry or wet etch process to give features suitable for etching patterns or for other chip manufacturing processes.

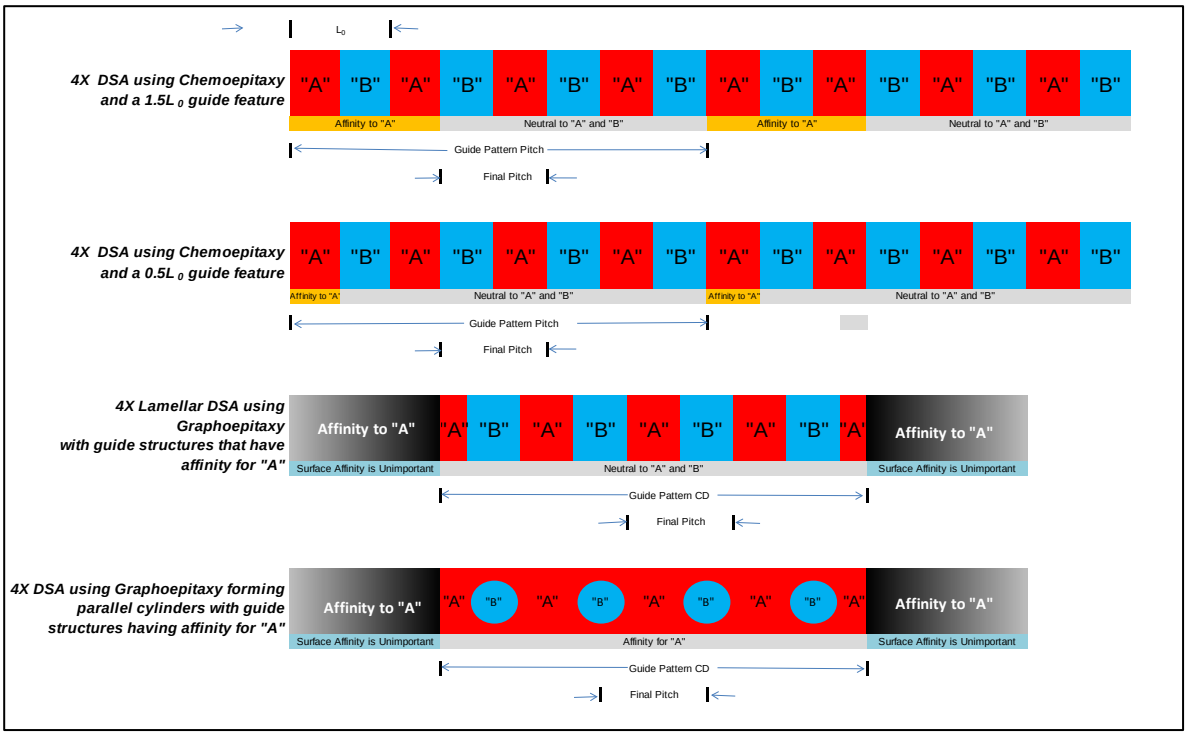

Figure LITH4A DSA Techniques for Lines and Spaces

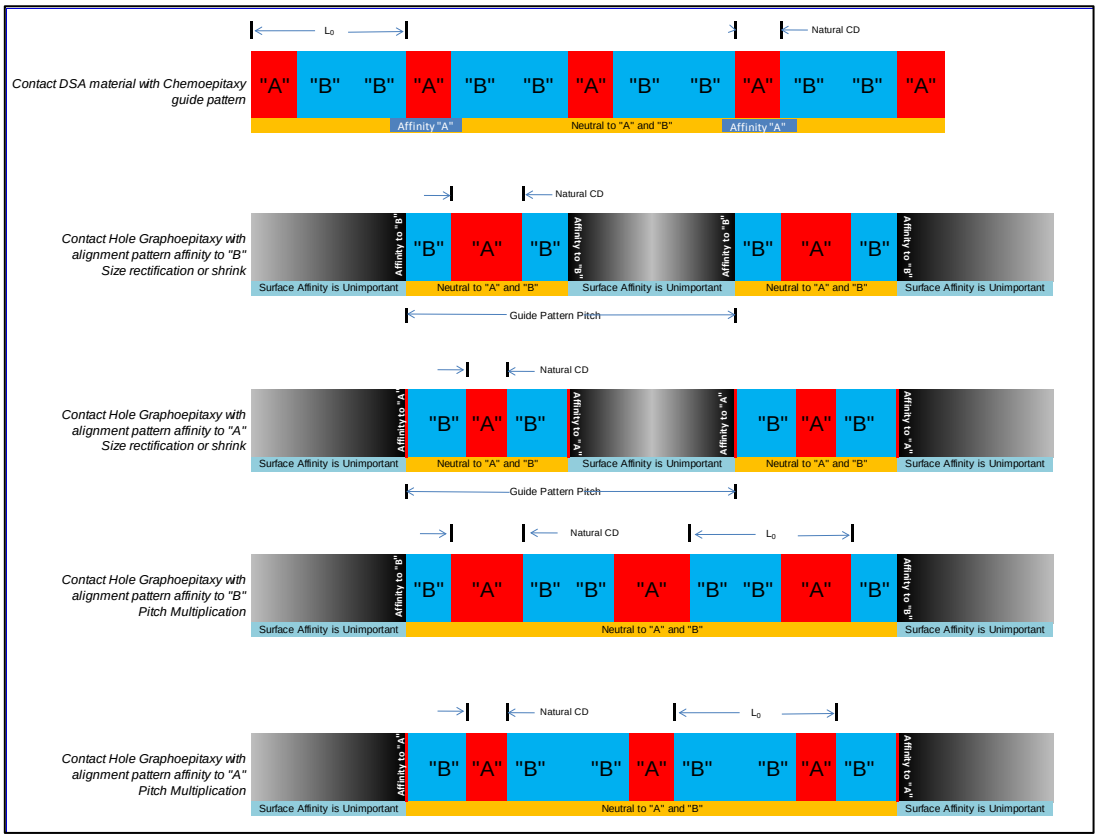

Figure LITH4B DSA Techniques for Hole Type Patterns

The chemical composition of the different polymer blocks controls the energy difference between the aligned state and the original spin coated random state. The energy difference between the two monomers, as reflected by the χ parameter, multiplied by the number of monomers in the block co-polymer, N, is a measure of the driving force for separation of the blocks. If product χN is less than roughly 10.5, there will not be enough of an energy benefit to phase separation and the polymer lowest free energy state will be a random arrangement with no discrete phases. Since χN, gets smaller as the polymers get smaller, and N relates to the pitch, or L_0, of the patterns formed; forming very small patterns require block copolymers with higher χs to have χN large enough to drive pattern formation.

The activation energy for annealing a block co-polymer gets bigger as χN gets bigger. This makes annealing large size patterns very difficult. Large patterns also require large polymers and such polymers can be very difficult to make and process very large polymers. This puts an upper limit on the size of the features for which DSA is appropriate.

The block co-polymer with the most demonstrated applicability to semiconductor pattering is polystyrene-b-poly(methyl methacrylate). This is shown as a separate line in Figure LITH1A. Patterns as small as 12nm lines and spaces have been demonstrated with this polymer. Smaller patterns made with higher χ polymers have also been demonstrated, with line and space half pitches as small as 8nm. An extensive discussion of the different materials available and required for DSA can be found in the Emerging Research Materials section of the ITRS roadmap.

There are many challenges to making DSA a usable chip manufacturing technique. Tables LITH7A and LITH7B give details of which pattern parameters are the biggest challenges. Table LITH7A is for line and space processes and has sections for both chemoepitaxy and graphoepitaxy processes. Both types of processes are under development. Table LITH7B is for contact holes and shows graphoepitaxy only. This is because to date, most of the work on hole type patterns use chemoepitaxy. Graphoexpitaxy processes for contact hole pitch multiplication are possible, but their development isn't as far along as graphoepitaxy ones are.

The immediate challenge for DSA is to show low enough levels of defects for manufacturing use. A key defect of worry is defects like dislocations, where the patterns don't anneal into the desired simple patterns. But other defects are also a concern. For example, the schematics show structures with idealized shapes. But actual structures can have more complicated three dimensional shapes that form because of small imperfections in the guiding patterns. Such defects

could make the desired pattern transfer of the DSA pattern by etch or other process impossible. Work has been published showing defect levels for pilot line processes, but the defect levels are not yet low enough for manufacturing.

Another area of concern is design. Current DSA processes can only demonstrate very simple patterns such as extended arrays of parallel lines. To use DSA effectively, chip designs based on such simple patterns have to be developed. In addition, ancillary patterning processes, such as cut levels for the large arrays of lines also have to be demonstrated.

Pattern placement or registration is a third area of concern. If DSA is used for pitch multiplication, usually several features will "float" between guiding features. For example, if parallel cylinders are being created and aligned with graphoepitaxy, the exact distance between neighboring cylinders will depend on the exact lateral dimension of the guiding trench.

Structures of lines and spaces where the line and space are not equal in dimension are also difficult to do. Lamellae only form if the sizes of the blocks are roughly equal, and this gives equal size lamellae from the two blocks and equal lines and spaces after etch. Cylinder forming processes for lines and spaces have analogous limitations. Solving this challenge will require some sort of processing that alters the line and space ratio, some sort of different gate design that can accept equal lines and spaces, or some sort of novel polymer that naturally gives sparse patterns of lamellae.

Table LITH7A Directed Self Assembly for Line and Space Type Patterns Requirements

Table LITH7B Directed Self Assembly for Hole Type Patterns Requirements

5.8. NANOIMPRINT

Imprint lithography has been shown to be an effective technique for the replication of nano-scale features. UV Imprint Lithography involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is cross-linked under UV radiation, and then the mask is removed leaving a patterned resist on the substrate.

Because of the leading edge requirements on half pitch and the more relaxed constraints on defectivity relative to logic devices, imprint lithography has targeted memory applications as an entry into the market. Resolution of dense features down to 6nm half pitch has been previously demonstrated. Key challenges that have been addressed over the years include, throughput, overlay, defectivity and mask infrastructure. Throughput is primarily a function of resist filling, and a target of one second filling is critical to achieving a throughput of 20 wafers per hour for an imprint module. Sub-one second filling was demonstrated during 2013[19]. Additionally, mix and match overlay of 8nm has been achieved[20]. The key challenges remaining for the technology are centered about defectivity and mask readiness.

Improved resist properties and separation mechanics, along with particle control have enabled defectivity to be reduced by several orders of magnitude over the last few years. The target for introduction of the technology into production is $1/cm^2$ for a lot of 25 wafers. By introducing a filtered recirculation system in the imprint resist reservoir, defectivity of $4.7/cm^2$ was demonstrated, resulting in electrical test yields on 10 meter structures of better than 90%[21] (See Figure LITH5). Additional contamination control will be critical in meeting the specifications required for production.

Standard practice for imprint involves creating a master template and using it to create replica masks and replicas of the replica masks to do the actual imprinting. Imprint lithography requires a mask infrastructure that addresses both master imprint masks and replica masks. Zero defect master masks with dimensions of 26nm have been demonstrated and used to fabricate replica masks[22]. Current best defectivity on replica masks (without repair) are $3/cm^2$, with a CDU of 1.5nm [23]. Advanced writing tools and processes will also be required to enable the fabrication of sub-20nm imprint masks.

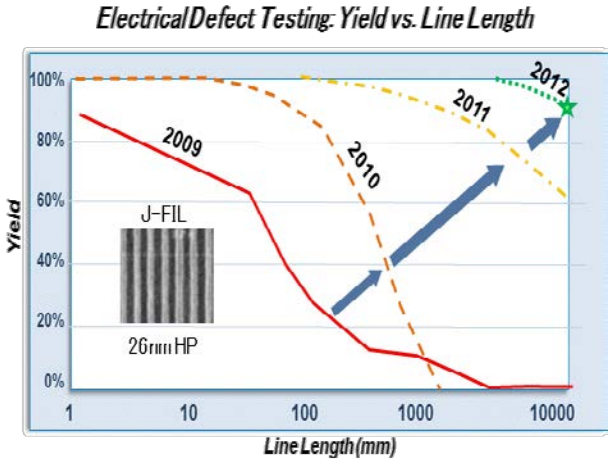

Figure LITH5 Electrical Test Yield Improvements for 10-Meter Serpentine Patterns

If imprint lithography finds its way as volume manufacturing solution, mask fabrication, defectivity control, and metrology becomes even more challenging as imprint lithography templates have the same dimensions as the wafer pattern. Electron beam inspection will be necessary for master template inspection, and high resolution optical inspection will be required for the replica masks.

Table LITH8 Imprint Template Requirements

Imprint may take several forms. The table lists requirements specific to ultraviolet nanoimprint lithography (UV-NIL), in which UV radiation is used to cure the liquid filling the template. Imprint templates have surface relief features that are the same size as the wafer features, and so are a 1x process. Thus the area that needs to be controlled for CD, pattern placement, and defects is 16× smaller than for comparable 4× masks for other technologies. The mask specifications are developed the same way that optical mask specifications are but they are tighter because the magnification is 1×. Inspecting defects on these masks is difficult because the wafer requirements are translated directly to the mask as 10% of the wafer CD specification. The registration is also difficult but is shared equally in quadrature between the two masks and the system overlay.

5.9. MASKLESS LITHOGRAPHY (DIRECT WRITE VIA E-BEAM)

The requirements for wafer patterning using Maskless Lithography (ML2) are the same as the wafer requirements in the ITRS tables. There are several proposed equipment configurations for ML2 lithography. Each design has unique variations in key features such as accelerating voltage, number of columns/beams, writing strategy, etc. Proposed tools for ML2 wafer patterning have voltages that range from 5KeV to 100KeV. The variation in system implementation approaches makes defining a single, unique set of requirements difficult. Because ML2 does not include a mask, the error budgets may shift to allow more variation in the wafer writing system. However, the result on the wafer will be the same regardless of the patterning technology utilized because the variation that normally comes from the mask in conventional optical or EUV lithography can be part of the actual wafer writing.

Data volume and transmission is a unique requirement for ML2 but each implementation has different needs and limitations. Fortunately, improvements in data volume and transmission are always possible. If data requirements can be met for one node, then data requirements should be met for future nodes using improved chips following the evolution in semiconductor technology.

ML2 implementations may require within field stitching. The specifications for stitching are covered by CD and LWR specifications.

There is potential to apply ML2 in combination with other patterning techniques. Using ML2 as a cut mask makes good use of the capabilities of ML2 while minimizing the limitations. A cut mask application greatly reduces the amount of data that needs to be written on the wafer, which increases the effective throughput. The critical CD and overlay requirements must be met by the primary patterning technique (193nm immersion and multiple patterning, EUV, DSA, etc.) utilized in combination with ML2.

Table LITH9 Maskless Lithography Technology Requirements

The near term challenges shown in the table relate to resolution and CD control. Since no manufacturing tool is available now and pilot tools to develop capability aren't planned until 2014, manufacturing capability for leading edge feature sizes has not been demonstrated. Longer term, data handling and data volume will be significant challenges if arrays of such tools are to be used in manufacturing with reasonable throughput.

6. CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions involving Lithography, *Design and Process Integration*, *Interconnect*, *Factory Integration*, *Metrology*, and *Modeling and Simulation* are outlined in this section.

6.1. DESIGN AND PROCESS INTEGRATION

The challenge of imaging patterns at the limits of 193nm lithography has driven the use of lithography friendly designs. All of the pattern doubling methods in use impose significant design constraints. Even without pattern doubling, tight pitches make jogs and more complicated 2-dimensional features more difficult to do. An example of such constraints are chip designs where M1 has a larger half pitch than M2 because of the need for a more complicated design in M1. These constraints result in costs. There is the cost of creating the mask and device designs using more complicated rules and software and there is the cost of the extra space needed for devices due the layout limitations imposed by new design rules. One of major appeals of EUV is that it improves design flexibility and reduces design costs. Maskless lithography and nano-imprint also improve design flexibility. DSA, on the other hand, has more difficult design constraints than current patterning but has exceptionally low processing costs for the CDs that it can resolve. It will be interesting to see how these factors resolve themselves in the future.

6.2. INTERCONNECT

Historically, interconnect has been one of the key drivers of lithography resolution. However, in the 2013 ITRS roadmap, the pace of logic interconnect shrinks is slower than predicted in 2011. This is because the intrinsic resistance of narrow interconnects limits the useful length of wires. Another factor is that tight pitch interconnects can require many masking levels per interconnect level because of the need for pitch multiplication followed multiple cut levels. This changes the tradeoffs between smaller pitch interconnect levels and other design solutions, such as more interconnect levels. Progress was still made in device size and performance, but it was made instead by the introduction of the finFET, that is, by the introduction of new devices. Now the leading resolution in the industry is driven by the needs of memory devices and by the size and pitch of the fins in finFET devices, rather than by interconnect. We expect this trend to continue. The introduction of new device types and new device materials will drive lithographic dimensions in the future as much as or more than interconnect requirements. We also expect that interconnect innovations in design and or materials may also affect lithographic requirements for leading edge devices.

6.3. FACTORY INTEGRATION

To maintain adequate process control, advanced process control capabilities are essential in the lithography cluster in the wafer fab. These capabilities are becoming increasingly important in mask-making facilities as well. Leveraging the learning from the wafer factory automation experience will also be essential to mask making. Several mask shops have developed custom solutions for automating data handling for defect inspection and repair. Further opportunities for automation exist. Leveraging existing standards that are used today in wafer fabs, such as the adoption of SECS/GEM into the mask-making tool infrastructure, will help reduce manufacturing errors.

An accurate wafer tracking system across various process modules is required to identify the working flow of any wafer in process. Several integrated metrology modules, able to evaluate one or more parameters—CD, litho stack thickness, target profile, overlay, macro inspection with automated defect classification, and wafer flatness—are also recommended. Track and stepper/scanner should be able to use data recorded by any kind of internal or external sensors to adjust processes. Other possible requirements, which may call for major upgrades of equipment software and in several cases even of related hardware, include simultaneously managing different module flows on tracks to accommodate optimal metrology sampling plans and accepting overrides to downloaded (or selected) recipe set points. Moreover, on any track module, being able to update all relevant set points wafer by wafer, even within the same lot, is desirable. On exposure tools, the software should allow the host to update dose, focus/tilt, and overlay input parameters wafer by wafer, even

within the same lot or perhaps for each exposure field. Calibration, self-calibration, and matching activities on metrology modules should be allowed without a significant loss in litho cell throughput.

The efficiency of EUV sources needs to be maximized to minimize the facility and power requirements to operate these sources at the power needed for high throughput EUV lithography. Specifically, the wall-plug efficiency of the sources needs to be increased to minimize the power to generate EUV photons and to cool the source components. Even if the cost of low throughput EUV tools was acceptable for resolution capability it provided, EUV would still not be a manufacturable technique because too many EUV tools and too much power and other facilities would be needed. These needs would prevent the building of usable chip factories. So the EUV need for enough source power is not just a cost issue but also a capability issue for the future.

6.4. METROLOGY

The traditional challenges in the lithography field (i.e. adequate measurements of wafer and mask level CD and overlay), are still challenges because the continued shrinkage of devices push the limits of lithography. Existing TMU (total measurement uncertainty which includes both accuracy and precision in a single metric) of CD measurement tools marginally meets the 20% measurement precision-to-process tolerance metric for the most advanced technology generations. As wafer and mask technology is evolving there are more situations that require 3D measurements. Examples of 3D measurements are the need to locate phase defects in EUV masks and the need for characterizing the three dimensional shape of finFET fins. Another key requirement is the measurement of line width roughness. Measurement precision for LWR must even be better than line width precision. The quantitative effects of LWR on device performance need to be better understood to optimize metrology for LWR.

When device geometries are shrunk by use of multiple patterning instead of by higher resolution imaging, the required overlay tolerances scale with the final device size, not with the size of the lithographically imaged features. So overlay metrology will continue to be challenged by future technology generations. If triple, quadruple or other multiple patterning beyond double patterning sees extensive use, the inherent stackup of tolerances in such methods will put more pressure on having tight overlay to ensure desired circuit yields. This will drive improvements in overlay test and overlay metrology.

Beyond these challenges, the insertion of next generation patterning creates new ones. EUV has traditional types of metrology requirements for printed features in resist (although at smaller dimensions of course). However, EUV masks create many new metrology requirements. EUV masks require extremely accurate metrology in material thickness (the most sensitive layer is the absorber in the EUVL mask fabrication) and surface roughness. Both parameters are expected to have impact on wafer CD uniformity. EUVL mask bow and local slope just before shipment to the wafer factory are also relevant indicators to keep under strict monitoring. Sub surface defects in EUV masks also require new methods of metrology and specifically, inspection at actinic (EUV) wavelength. In all these areas substantial improvements in metrology are requested to support the tight budgets required for a sustainable litho process.

A key aspect to be also addressed in the next future is the detection and correct measurement of defects (both in un-patterned, i.e. in resist coated wafers, and patterned units, i.e. in developed wafers before etching) at sizes as tiny as few nanometers; again, proper solutions should be sought for. There is no commercially available equipment that can meet the requirements in HVM. In the current litho tables, the minimum defect size shown is the limit of measurement of existing equipment, not the desired sensitivity. If the minimum detectable defect size is 10nm but a critical CD is the same size or smaller, this obviously shows a need for better defect detection.

Other possible next generation lithography techniques also require improved metrology. For maskless lithography, more detailed inspection of patterned wafers will probably be needed, since certain errors such as missing features cannot be detected by qualifying a mask in advance. For nanoimprint, a fab priority will be to detect repeater defects from dirt in a template before too many die are affected. For DSA, patterning defects can be below the surface of the annealed film and not detectable by top-down SEM. This may require the development of new inspection methods. For all these areas, innovations are both expected and needed.

The complete discussion of Lithography Metrology is in the Lithography Metrology and Microscopy sections of the *Metrology* chapter, which also includes lithography metrology technology requirements and potential solutions.

6.5. MODELING AND SIMULATION

Support from modeling and simulation is critical both to push the limits of traditional optical lithography and to assess new next generation lithography technologies. Simulation of multiple exposure / patterning including database splitting is needed to support accurate and seamless implementation as MP becomes one of the main techniques to support feature

sizes reduction in HVM. Taking advantage of computational lithography depends on continued improvement of mask writers and inspection systems to produce more complex patterns, and reduction of measurement uncertainty to calibrate accurate models. Integration of computational lithography with multiple patterning must address where it and pattern decomposition belong in the data flow from design to mask data preparation.

New techniques used in next generation lithography techniques, such as using reflecting masks for EUV lithography, must be appropriately modeled and included in the simulation programs. Defect printability and CD impact as related to the sizes, height, and locations with the multilayers and defect optical properties are not well understood. Simulation and modeling are critical for the understanding of defect influences and possible compensation techniques. Simulation of maskless lithography by e-beam direct write (shaped beam/multi beam) including advanced resist modeling (shot noise and LER) is needed. In order for DSA to become a plausible lithography solution, it is also vital to have simulation of DSA of sub lithography patterns.

A specific challenge for lithography modeling and simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. Current photoresist modeling is optimized for traditional novolak and chemically amplified resist platforms. EUV resist modeling also requires understanding of secondary electron behavior. There is a growing volume of research into nontraditional mechanisms for resist. These mechanisms do not necessarily follow classic photoresist simulation models. Work is needed in both of these areas.

See the *Modeling and Simulation* chapter for details on developments needed to satisfy these requirements.

7. Impact of Future Emerging Research Materials

Historically, patterning has made as much resolution progress through the introduction of new materials and processes as it has through the introduction of new tools. We expect this to trend to continue. Table LITH10 shows areas where new or improved materials are required, or where new materials that are currently being research or are under development could be useful. The table is separated into two sections. In the top section, potential improvements to current photoresist capability are shown. More negative tone materials, improved EUV resists, and new resist technologies for a better LWR/sensitivity/resolution trade-off and for better etch resistance are needed. DSA is shown separately in the bottom section because it is an entirely materials based method of improving resolution. DSA has already demonstrated high resolution, but it requires relatively inflexible designs. New materials are needed that enable more diverse types of patterns. New materials are also needed to improve defect levels, to simplify or improve the processing and to improve long range waviness in the lines.

Table LITH10 Lithography Materials Requirements

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