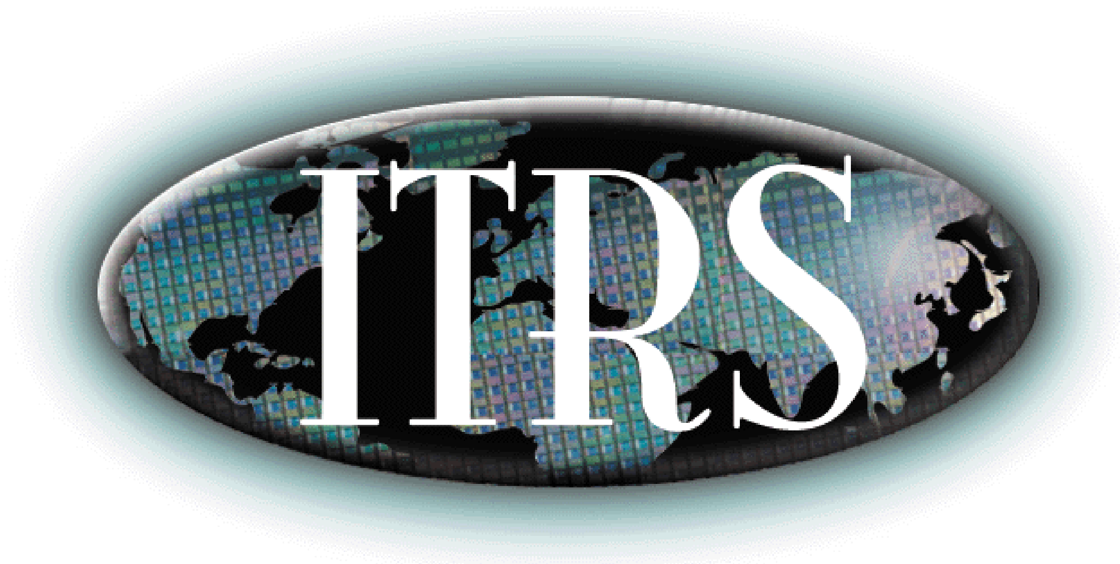

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

IRC OVERVIEW

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ITRS INTERNATIONAL ROADMAP COMMITTEE OVERVIEW

INTRODUCTION: THE EVER CHANGING ENVIRONMENT

The Semiconductor Industry was born in the 70s as a component industry with two main business drivers. The first consisted in providing more cost effective memory devices to the computer industry. The second consisted in timely production of application specific integrated circuits (ASICs) to any company that required very specific functionalities to realize novel products. Customers demanded pin-out and functionality standardization for memory devices while ASIC products were typically customer specific. Logic devices reprogrammable by software (e.g., microprocessors) were developed to minimize cycle time of ASIC devices.

In the 80s *system specifications were solidly in the hands of the system integrators*. New semiconductor technologies were introduced every three years by memory devices and were subsequently adopted by makers of logic devices.

In the 90s the integrated circuit (IC) makers of logic devices were able to accelerate the introduction of new technologies to a more aggressive 2-year pace quickly followed by memory makers. The unusual strong correlation between technology improvements (obtained by scaling) and enhanced product performance shifted a *substantial part of the control of system performance and profits in the hands of IC manufacturers.* The IC manufacturers were able to capitalize on this new balance of power and the revenue of the entire semiconductor industry revenue grew at an average 17%/year during this period.

A completely new ecosystem has emerged during the past decade:

- First of all, the aggressive bi-annual introduction of new semiconductor technologies allowed ICs, consisting of even hundreds of million of transistors to be produced cost effectively. This made it possible to integrate extremely complex systems on a single die or in a single package at very attractive prices. Furthermore, progress in packaging technology enabled the placement of multiple dice within a single package. These categories of devices are defined as system on chip (SOC) and system in package (SIP).
- Second, manufacturers of integrated circuits offering foundry services were able to provide, once again, the "New ASICs" at very attractive costs. This led to the emergence of a very profitable business for design "only" houses, i.e., companies that do not manufacture ICs for themselves, but produce the designs that are manufactured elsewhere.
- Third, development of sophisticated equipment for advanced integrated circuits proliferated to adjacent technology fields and by so doing the realization of flat panel displays (FPD), MEMS sensors, radios and passives, etc., was made possible at reasonable costs. Under these conditions *system integrators were once again in the position to fully control system design and product integration.*

Finally, the successful adoption of the internet and the rapid rise of mobile phones led to the extensive deployment of fiber optic cables and the proliferation of multiple wireless technologies ranging from communication satellites to tens of thousands "repeater stations," which enabled an unprecedented level of global mobile connectivity.

This ecosystem has facilitated the creation of completely new and unexpected markets of which the "Social Network" represents the latest example.

Intense research on increased functionality of mobile devices making them the ultimate customer interface to the world is in progress. Furthermore, research on such exotic applications as making all the sensorial inputs communicable from the sender to the receiver via mobile devices is in progress.

All of the above elements today are often referred to as the "Internet of Things" (IOT). Innovative product houses, telecommunication companies, data and information distributors, as well as content providers, are battling for dominant positions in this newly created market. It is clear that all of these innovations could not have occurred without the support of the semiconductor industry that has provided the building blocks for all the above applications.

What is the role of the semiconductor industry in this new ecosystem?

2013 ITRS EDITION AND MOVING FORWARD...

The foundations of scaling were laid out with the invention of the self-aligned silicon gate process in the late 60s. Moore's predictions of the rate of transistor by-annual growth formulated in 1965 and in 1975 in conjunction with Dennard's scaling guidelines led the growth of the semiconductor industry until the beginning of the last decade. This was the (First) Era of *Classical (Geometrically driven) Scaling*.

The ITRS laid out the foundations of the (Second) Era: *Equivalent Scaling* (e.g., strained silicon, high-κ/metal gate, multigate transistors and integration of Ge and compound semiconductors) between 1998 and 2000. The implementation of these technologies has successfully supported the growth of the semiconductor industry in the past decade and it will continue to do so until the end of the present decade and beyond.

DEVICES

Device cost and performance will continue to be strongly correlated to dimensional and functional scaling[1] of CMOS as information processing technology is driving the semiconductor industry into a broadening spectrum of new applications according to 2013 ITRS.

Strained silicon, high-κ/metal-gate and multigate transistors are now widely used in IC manufacturing. A significant part of the research to further improve device performance is presently concentrated on III-V materials and Ge. These materials promise higher mobilities than Si devices.

In order to take advantage of the well-established Si platform, it is anticipated that the new high-mobility materials will be epitaxially grown on Si substrate. Beyond implementation of these new materials the Emerging Research Device (ERD) section reports completely new transistors, operating on new principles like tunneling (e.g., TFET) or spin that offer the possibility of operating at very low power.

Furthermore, a large variety (like never before) of new memory devices operating on completely new principles are extensively reported in the 2013 ITRS.

Because 2D scaling will eventually reach fundamental limits towards the end of the 2013 ITRS period both logic and memory devices are exploring the use of the vertical dimension (3D).

The combination of 3D device architecture and low power device will usher the (Third) Era of Scaling identified in short as "3D Power Scaling". Increase in the number of transistors per unit area will eventually be accomplished by stacking multiple layers of transistors

Unfortunately no new breakthroughs are reported for interconnections since no viable materials with resistivity below copper exist. However, progress in manipulation of edgeless rapped materials (e.g., Carbon nanotubes, graphene combinations etc.) offer the promise of "ballistic conductors, which may emerge in the next decade.

3D integration of multiple dice offers possible avenues towards reducing interconnect resistance by increasing the conductor cross-section (vertical) and by reducing the length of each interconnect path. For instance, integrating memory device (die) immediately above logic device (die) and connecting them by means of wide through silicon vias (TSV) can accomplish this result.

Nevertheless, horizontal dimensional scaling of CMOS or any of the equivalent devices presently under study will eventually reach fundamental limits; the 2013 ITRS is reporting two additional ways of providing novel opportunities for future semiconductor products. The first consists in extending the functionality of the CMOS platform via heterogeneous integration of new technologies, and the second consists in stimulating invention of devices that support new information-processing paradigms.

SYSTEM INTEGRATION

System integration has shifted from a computational, PC-centric approach to a highly diversified mobile communication approach. The heterogeneous integration of multiple technologies in a limited space (e.g., GPS, phone, tablet, mobile phones, etc.) has truly revolutionized the semiconductor industry by shifting the main goal of any design from a

[1] *Functional Scaling: Suppose that a system has been realized to execute a specific function in a given, currently available, technology. We say that system has been functionally scaled if the system is realized in an alternate technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost, and does not degrade in any of the other metrics.*

performance driven approach to a reduced power driven approach. In few words, in the past performance was the one and only goal; today minimization of power consumption drives IC design.

This is demonstrated by the fact that SOC and SIP products have become the main drivers of the semiconductor industry as total volume of smart phones and tablets has surpassed production volumes of microprocessors in the past few years

The foundation of heterogeneous integration relies on the integration of "More Moore" (MM) devices with "More than Moore" (MtM) elements that add new functionalities (non-CMOS) that do not typically scale or behave according to "Moore's Law."

For instance, currently MEMS devices are integrated into small and large systems, such as automobiles, video projectors, tablets, smart phones, and game platforms. In most cases the MEMS devices add useful functionality to the system, and in some cases the MEMS devices enable the core functionality of the system. For example, MEMS accelerometers used in smart phones sense the vertical orientation of the phone and consequently rotate the image on the display. It could be said that the added functionality introduced by MEMs improves the user interface, but the phone would still operate without it. In contrast, a video projector using digital light projector (DLP) technology and an inkjet printer could not function without their MEMS devices. Multimode sensor technologies have also become an integral part of mobile devices and are key enablers of the IOT.

The rapid increase of digital data and connected technologies is also revolutionizing healthcare. Silicon, MEMS, and optical sensors technologies are making that revolution possible.

Today the mobile phone can already provide a great deal of health information. Accelerometers can track activity and sleep. Built-in optical sensors are available that can sense heart rate when the user is touching the phone. The camera in the phone can be used for purposes as diverse as checking the calorie content of a food item, or identifying your emotions based on facial expression recognition. A broad spectrum of mobile phone apps has been developed to analyze this data, and deliver it to the consumer in an intelligible and actionable manner.

Looking at long term devices and systems (7-15 years horizon, beyond 2020), the 2013 ITRS reports on completely new devices operating on completely new principles and amenable to support completely new architectures. For instance spin wave device (SWD) is a type of magnetic logic device exploiting collective spin oscillation (spin waves) for information transmission and processing. SWD converts input voltage signals into the spin waves, computes with spin waves, and converts the output spin waves into the voltage signals. Extensive parallel data processing on multiple frequencies in a single core structure can be performed at very low power by exploiting each frequency as a distinct information channel. Furthermore, some of the new devices stimulate the creation of new architectures. For instance, storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost of conventional hard-disk magnetic storage. Such a device requires a nonvolatile memory (NVM) technology that could be manufactured at a very low cost per bit.

Direct replacement of DRAM with a slightly slower M-class SCM has also been considered, for the particular example of STT-MRAM (spin torque transistor magnetic RAM).

MANUFACTURING

Manufacturing of integrated circuits, driven by dimensional scaling, will reach the few nanometers range well within the 15-year horizon of the 2013 ITRS. Is has become more and more difficult with each technology generation to measure dimensions of physical features on the wafers. This task has been largely accomplished by correlating process parameters with equipment parameters. By controlling equipment stability and process reproducibility accurate control of feature size and other process parameters has been successfully accomplished.

A major addition to the 2013 ITRS edition is a new sub-chapter on big data (BD) in the Factory Integration chapter. The fab is continually becoming more data driven and requirements for data volumes, communication speeds, quality, merging, and usability need to be understood and quantified. Challenges and solutions associated with these issues are also provided in the BD sub-chapter.

Looking at the Long Term, the 2013 ITRS addressed several 300 mm challenges, and how these challenges migrate to 450mm. The industry must focus on common technology development for 300mm and 450mm. 450mm factories would benefit by adaption of improved technology validated for 300mm

SoC and SiP integration continue to rise in prevalence throughout a number of business segments. Increased device integration forces a re-integration of test solutions to maintain scaling of test costs and product quality. The optimized test solutions may require access to and testing of embedded blocks and cores. Techniques for known good die (KGD) that

provide high quality dice for multi-die packaging also become very important and an essential part of the test techniques and cost trade-offs.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

The ITRS process and content evolves to match the needs of the semiconductor industry. Collaboration of industry and research continues to be invaluable to understand and assess as well as possible the needs of future inventions and technical challenges in the various spectra of micro- and nano-electronics. Over the past few years, the ITRS teams have worked closely to assess emerging technologies. They indicate an approaching world of vast interconnectedness with humans and hardware, phrased as the internet of things, and the complex world of information processing known as big data. These examples are only part of the new frontier of invention and discovery. As these new focus topics emerge, the ITRS teams will continue to determine what this means for our global industry. The industry must define the new drivers to help it stay on a path of productivity and profitability, while promoting environmental health and encouraging areas of innovation for new scientists and technologists.

ITRS HISTORY

The most relevant subjects of the ITRS were originally divided among eleven International Technology Working Groups (ITWGs). As time went by the industry became more complex and the number of ITWGs increased to 17 in 2013. As we look forward to the 2015 ITRS it is clear that readjustments on how the ITWGs are configured and the addition of new subjects are necessary. As a result the drivers of the 2015 ITRS and the ITWGs will be redefined in 2014.

ITRS TEAMS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.) to convey messages from their respective regions. The five regions have worked together since the inception of the ITRS in 1998. The IRC is entirely responsible for all the decisions related to the ITRS. Additionally, IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS workshops
- Editing the ITRS

The ITWGs are composed of experts in their respective fields. The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

These experts are actively engaged in conferences, committees, and working groups that are held throughout the year. The ITRS tables are often discussed and reviewed in technical events and used as benchmarking references in multiple presentations. (A SEMATECH library search conducted using Google in October 2013 indicated that the term "International Roadmap for Semiconductors" has been quoted 1,180,000 times!).

The ITWG members act as "talent scouts" looking for the most promising technologies in their fields of expertise. In many cases these technologies may be in their infancy, requiring skills and insight of the roadmap technology experts to identify them for further assessment. It is quite common for ITWG specialists to meet with their colleagues from other regions and also with other experts in their field, during the most relevant conferences held during the year. Also, for efficiency, teleconferences and virtual meetings among ITWGs members are frequent throughout the year.

These ITWG teams from each region report the results of their discussions and searches to other regional members and the IRC during the official ITRS face-to-face workshops. These meetings are more of an exchange of already digested recommendations and subsequent refinements than "discovery meetings."

2013 ITRS METHODOLOGY

In order to translate technology trends into measurable quantities, the ITWGs generate tables and figures that, to the best of their knowledge, represent measurable parameters assessing the progress of specific technologies. Data cells of these

technology tables are colored according to the level of confidence in achieving those specific results in time (refer to Roadmap Content below).

Each of the ITRS chapters addresses both near and long-term challenges. The near-term (1-7 years) challenges typically represent milestones of technologies already known while the long-term challenges typically introduce breakthrough technologies.

Every two years, the entire ITRS is completely revised, while in the alternate years typically only data tables are adjusted according to the latest assessments of each working group.

The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2013 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging
- Microelectromechanical Systems (MEMS)

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity and confidence levels, represented by colors in the tables, for these targets:

Manufacturable solutions exist, and are being optimized	(white)
Manufacturable solutions are known	(yellow)
Interim solutions are known	◆ (light yellow)
Manufacturable solutions are NOT known	(red)

The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions

are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

The 2013 Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS road-mapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

GRAND CHALLENGES IN THE NEAR-TERM (THROUGH 2020) AND LONG-TERM (2021 AND BEYOND)

IN THE NEAR TERM (THROUGH ~ 2020)—ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architectures, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) will continue to be a difficult challenge in the near term despite the introduction of high-κ metal gate (HKMG). Interfacial layer scaling and/or silicon-high-κ interface quality are critical to the EOT scaling for the 10 nm node and beyond. Integration of higher- κ materials, while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing, are also challenges to be faced in the near term. The complete gate stack material systems need to be optimized together for best device characteristics (power and

performance) and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as multiple-gate MOSFETs (e.g., finFETs) and ultra-thin body and BOX (UTBB) FD-SOI are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

High mobility channel materials such as Ge and III-V have been considered as an enhancement or replacement for Si channel for CMOS logic applications. High- κ metal gate dielectric with low interface trap density (DIT), low bulk traps and leakage, unpinned Fermi level and low ohmic contact resistances are major challenges.

MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now include both stand-alone and embedded DRAM and SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. The need to increase bit density and to lower production cost is driving toward $4F^2$ type cell, which will require high aspect ratio and non-planar FET structures.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory has become a new FEOL technology driver for both critical dimension scaling, materials and processing (lithography, etching, etc.) technology ahead of DRAM and logic. Continued FLASH density improvements in the near term rely on the thickness scaling of two key dielectrics of the memory cell, namely the tunnel oxide and the intergate dielectric, in a way that guarantees the charge retention and endurance requirements; the introduction of high-κ materials will be necessary. 3-D NAND flash is being developed to build high-density NVM beyond 256 Gb. Cost effective implementation of this new technology with MLC and acceptable reliability performance remains a difficult challenge. Non-volatile memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory (PCM), and FeRAM, for example. MRAM scalability of cell-size and write-power reduction still needs further breakthroughs. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size. Another challenge for MRAM and FeRAM going forward is their cost effective integration with logic technologies for integration in the backend of the flow.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES -]

Cost, power consumption and performance of wireless transceiver ICs in the <30GHz and the mm-wave applications continue to be the main technology drivers. The <10GHz application space, serviced by deep sub-micron CMOS technologies with emerging high κ dielectrics and channel strain engineering may require techniques to keep the device mismatch and the 1/f noise within acceptable levels. To adopt advanced RFCMOS early, incorporating less expensive integrated passive components as part of a total solution would become a technology trend where innovation would be needed to achieve higher density capacitors. Applications that use HBT devices will benefit from a more aggressive vertical scaling. MEMS development, MEMS integration with active Si and off-chip passive network processes are expected to significantly contribute to the overall system performance. Mm-wave applications will benefit from development of low cost non-Si (GaN) based devices.

Signal isolation between the digital and the analog regions of the chip is becoming more critical as the chip complexity and operating frequencies increase while the power supply voltage decreases. While noise coupling through the power supply and the ground line can be addressed by design techniques, substrate noise coupling reduction may require significant amount of innovation such as KΩ-cm high resistivity substrate.

Many of the materials-oriented and structural changes being invoked in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF, HF, and AMS performance occur as different mechanisms emerge as limiting factors. Examples include series resistances at gate, source and drain, that greatly affect parasitic impedances and the impact of such local interconnect parasitics on fMAX. Fundamental changes of device structures, e.g., multiple-gates and silicon-on-insulator (SOI), to sustain continued digital performance and density improvements greatly alter RF and AMS characteristics. Such differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries.

MEMS

The ITRS MEMS Technology Working Group (TWG) was established is in 2011 and tasked to develop a new chapter for the ITRS Roadmap. The MEMS devices considered in here (accelerometers, gyroscopes, microphones, and RF varactors) will generally see a continuous incremental increase in performance with key focus areas being decrease in package size, cost and reliability. The greatest challenges for the MEMS technologies are related to their integration and primarily linked to the back-end of manufacturing, packaging and test. As mobile internet device manufacturers work to decrease size and weight, extend battery life, and integrate new functionalities, their pull on MEMS device manufacturers is for smaller package size and integration. The near term challenges include: MEMS standard process modules to improve manufacturing efficiency and time to market; standardization of device datasheets and methodologies to “Design for Test;” knowledge of the reliability physics of failure is required to develop accelerated life tests; standardization for MEMS packaging to support integration 3D packaging technologies (TSV), and ability to accurately predict the effect of the package on device performance.

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Reduction of the equivalent gate oxide thickness (EOT) below -0.7 nm with appropriate metal gates remains as the most difficult challenge associated with the future device scaling. Higher dielectric constant dielectrics with adequate conduction and valence band offsets with silicon and thinner interfacial layers are required. Reduction of interface states for gate stack on multi-gate devices is one of the key challenges for -10 nm node and beyond. Another critical challenge is scaling the interfacial layer between the high-κ dielectric and the silicon without channel mobility degradation from increased Coulomb and remote phonon scattering. Higher mobility materials such as SiGe, Ge, and III-V compound semiconductors will be needed for channel transport enhancement which introducing additional challenges for future high-κ dielectric stacks due to the complex nature of their interfaces with channel materials. Furthermore, reliability requirements for newer high-κ oxides, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability) must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance requirement to 20-25- fFand, reducing the parasitic capacitances in buried bit line or buried word line technologies. Storage cell capacitance requirements resulted in the introduction of dielectric materials with a higher dielectric constant (higher-κ) now in production for DRAM capacitors using metal-insulator-metal (MIM) structures. Besides the high- κ dielectrics and high work function electrode, new technologies for storage node formation with ultra high aspect ratios are needed. Therefore, new oxide etching technology and sidewall cleaning technology for ultra high storage node pose significant challenges and needs to be developed.

Continued FLASH scaling in the near term relies on the thickness of two key dielectrics of the memory cell, namely the tunnel oxide and the intergate dielectric, in a way that guarantees the charge retention and endurance requirements. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. Scaling the tunnel dielectric thickness must simultaneously guarantee good charge retention properties (drive for thicker films) and high write/erase performance (drive thinner films). The present interpoly dielectric technology is based on oxy-nitride stacked layers and likely not suitable for aggressive reduction of equivalent oxide thickness, due to unacceptable charge retention properties. Thus, the introduction of high-κ materials at this step will be necessary. Aside from new materials, the structural stability and overall process integration represent critical challenges for the inception of 3D NAND technologies critical to continued effective flash memory density scaling.

22 NM HALF PITCH AND BELOW [LITHOGRAPHY]

The lithography technology is becoming very expensive and challenging. 22 nm half pitch remains a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double patterning or exposure; however the lithography cost will almost double.

For 22-nm half-pitch lithography, water-immersion 193 nm scanners with spacer lithography or multiple patterning will be applied to overcome the single patterning limitation, but with extremely large mask error enhancement factor (MEEF), wafer line edge roughness (LER), and design rule restrictions. Resorting to more than two passes through the patterning tools can alleviate some of the above problems at the expense of higher costs. Extreme-UV lithography (EUVL) with wavelength reduced to 13.5 nm, an order of magnitude smaller than that of the water-immersion wavelength of ArF excimer lasers, is the official hope of the industry to advance Moore's law. EUVL does not need double exposure until approaching the 11 nm half pitch. As a result there is less restriction in design rules. However, EUVL is delayed by the lack of high-power and high-efficiency sources, fast resists, defect-free and high-flatness masks, as well as related infrastructures. Development efforts in these areas are heavy. The numerical aperture of EUV systems will have to be raised to more than 0.36 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties, remove restricted design rules, and provide manufacturing flexibility, is in an early-stage of development. Two pre-alpha tools are in the field. Progress has been made in demonstrating high-resolution imaging and CD control. Timing of manufacturing tools, costs, defects, overlay accuracy, and resists are other areas to further develop. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate per beam or more parallelism to maintain the increased pixel count within the same-size field. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications. DSA has shown progress but defectivity and positional accuracy must see rapid improvements.

MASKS [LITHOGRAPHY]

The mask cost has escalated each generation. Increased resolution plus larger MEEF, due to higher levels of resolution enhancement technique (RET), make the mask CDU difficult to meet. Double and multiple patterning impose stringent requirement of mask pattern placement accuracy. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. EUV masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths. Actinic mask inspection and verification are eventually inevitable for EUVL. It further adds to the cost and complexity of the EUV mask infrastructure.

RESISTS [LITHOGRAPHY]

LER of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology-generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices. For EUVL, resist outgassing can contaminate the delicate reflecting optical surfaces. The tradeoffs between high resist sensitivity for throughput, low resist sensitivity for shot noise, and low LER, impose more problems than just resist collapse. E-beam resists also have to trade off for sensitivity and shot noise as well as LER. The sensitivity requirement is not as severe as that of EUVL.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. The inception of increasingly restrictive design rules aimed to promote design regularity have become mainstream as key enablers for near term scalable CD control. Line-edge-roughness (LER) has become also a critical element of device variability. Suppression of LER will continue to pose significant challenges to patterning processes (etch and lithography) as well to metrology in terms of accuracy and throughput. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

FRONT END PROCESSES

Strain engineering faces significant challenges for continued improvement of device performance due to tight space resulting from pitch scaling. Aside this effect, FDSOI technologies face additional strain engineering challenges due to the thin silicon film. We need to achieve low parasitics and continued scaling of gate pitch and areal scaling with next generation substrates (450mm wafers) and adoption of disruptive technologies to meet lithographic challenges. EOT scaling and gate dielectrics with low DIT, bulk traps and leakage remains a key challenge particularly for high mobility, low bandgap channels materials (Ge, IIIV and 2D materials). Likewise, effective containement of device parastics with new channel materials, especially for contact resistivity due to severe reduction in device pitch and contact area.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm logic technology M1 half-pitch. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. The fast introduction of new metal/dielectric systems becomes critical. For low-κ dielectrics, the conventional approach is the introduction of homogeneous porous low-κ material. Reduction of κ damage due to Etch and CMP processes becomes more important with more porous materials. Another approach is air gap. It attracted attention because it keeps same low-κ materials with more volume of air gaps that gives lower effective κ. Among various techniques to incorporate air gaps, thermal or UV degradable sacrificial layer method is one of the low-cost approaches. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling. For the metal, fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary has become a key challenge. A very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. The low-κ material with good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures, different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, optimization tools and low cost for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. Driven by the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expands upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

CIRCUIT ELEMENT AND SYSTEM MODELING FOR HIGH FREQUENCY (UP TO 160 GHZ) APPLICATIONS

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-,

CMOS-, and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

Front-End Process Modeling for Nanometer Structures [Modeling and Simulation]

Advanced USJ formation is critical to support continued scaling of device features. Definition of drain extension using millisecond anneal, solid phase epitaxial regrowth (SPER), as well as by in situ doped epitaxial layers, are expected to be widely used to reduce junction depth, sharpen junction gradient, and enhance activation. More physical models are needed to capture point and extended defects, dopant, and co-dopant evolution and interactions, during non-equilibrium transient process of millisecond anneal. Modeling capabilities need to be enhanced or developed to capture crystal/amorphous growth front evolution and defect generation during SPER. New models are needed to properly capture initial doping states created by various in situ epitaxial processes. Process modeling available for bulk silicon substrate will need to be adapted or extended to various Si-based substrate including SiGe:C, Ge, SOI, epilayers, and ultra-thin silicon on insulator, as well as high mobility compound materials such as GaAs, InGaAs etc. Additional factors, including, possible anisotropy, interface/surface type effects, and intrinsic strain effects, need to be take into account. Modeling of advanced implant technologies such as use of molecular species, non-beam line implant, and cooled or heated substrate, will be needed. Epitaxial processes such as SiGe:C will be expanded to multi-channel devices with complex geometries; therefore, modeling of epitaxially grown layers including the shape, morphology and defect generation will be critical to optimize such epitaxial processes. Extensive use of stress to enhance device mobility will continue. More accurate modeling of stress including material properties evolution during process such as plastic deformation during anneal, and stress relaxation due to defect generation will be needed. There will be continued needs for refining metrology of USJ - 2D/3D doping/stress profiling to sufficient resolution to help calibration of simulation models and parameters. Devices are expected to largely deviate from quansi-2D and become 3D in nature, therefore more advanced 3D meshing, and parallel processing to improve 3D computational efficiency and accuracy will be needed. Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces will be helpful in understanding nano-scale feature related effects. Modeling of the high-κ/metal gate work function, interfacial atomic structures and their influences on mobility and reliability, will be necessary. Tools for ab-initio modeling and quantum effects for the development of novel nanostructure materials, processes and devices will be needed.

In the Near Term (through ~ 2020)—Cost-Effective Manufacturing

Design Productivity and Design for Manufacturing [Design]

The number of available transistors doubles every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design to minimize performance/power variability, lithography-friendly designs (regular layout styles consistent with increasingly more restrictive design rules), and design for testability and reliability.

Test complexity [Test and Test Equipment]

The complexity of next generation testing technologies is further convoluted by design and process interaction of heterogeneous integration in one device such as 3D IC, which imposes challenges in yield learning for production ramp. The device characteristics of heterogeneous integration will not only be dependent on layout environment but also will be relative to integration of process procedure and the functionalities of design modeling. The effectiveness and efficiency of test and analysis of product failure becomes the gating factor for yield ramp. The intelligent test data mining feedback tests data to tune manufacturing and device's traceability. The areas for further improvement include new test equipment, test methodology, and design software for detecting systemic defects: testing for local non-uniformities, not just hard

defects, erratic, non deterministic, intermittent device behavior and mechanical damage during the testing process and multi-die stacks/TSV.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. The new test requirements for increasingly complex devices drive innovative new testing technology to continue economic scaling of test cost (such as DFT, concurrent testing, adaptive test and built-in testing.) and must consider overall equipment efficiency (interface hardware, setup/flex, lot sizes). In the opposite cost-direction, test tooling costs, including probe cards, are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. The intelligent test data mining with dynamic test flow, convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

FACTORY INTEGRATION

In responding to rapidly changing complex business requirements and meeting improvement in trade-off between manufacturing cost and cycle time, difficult challenges through 2021 are:

- Responding to rapidly changing, complex business requirements
- Managing ever increasing factory complexity
- Achieving financial growth targets while margins are declining
- Meeting factory and equipment reliability, capability, productivity and cost requirements per the Roadmap.
- Cross leveraging factory integration technologies across boundaries such as 300mm and 450mm to achieve economy of scale
- Addressing unique challenges in the move to 450mm (where 300mm technologies cannot always be leveraged)

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

The challenges for assembly and packaging include concerning 3D IC chip stacking:

- Testing: Access, Cost and KGD: Close gap between chip and substrate, Improved Organic substrates: Increased wireability at low cost; Improved impedance control and lower dielectric loss to support higher frequency applications; Silicon I/O density increasing faster than the package substrate technology.
- 3D assembly and packaging: Thermal management; Alignment/placement accuracy layer to layer; Wafer to wafer bonding.
- Test access for individual wafer/die: Cost of TSV and Bumpless interconnect architecture.
- Package cost does not follow the die cost reduction curve: Wafer level packaging and 3D equipment cost is not scaling with product cost; Increased device complexity requires higher cost packaging solutions.
- Small die with high pad count and/or high power density: Electromigration at high current density for interconnect (die, package); Thermal dissipation; Improved current density capabilities.
- High frequency die: Lower loss dielectrics and "hot spot" thermal management.
- Power Integrity: Power delivery in stacked die and reducing power supply voltage with high device switching currents.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process

simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

ESH

There is a need for Roadmap quality goals and metrics to be defined for a substantial number of ESH technology requirements. Some improvents in quantitative analysis have been made. The challenges are:

- Chemicals and Materials Management and Efficiency: Chemical assessment, chemical data availability, and chemical exposure management.
- Process and Equipment Management: Process chemical optimization, environment management, global warming emissions reduction, water and energy conservation, consumables optimization, by-products management, chemical exposure management, design for maintenance, and equipment end-of-life.
- Facilities Technology Requirements: conservation, and global warming emissions reduction.
- Sustainability and Product Stewardship: design for ESH, sustainability metrics, and end-of-life reuse/recycle/reclaim.

Detection of Multiple Killer Defects and Signal-to-noise Ratio [Yield Enhancement]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends. New techniques are needed such as high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation. Increasing aspect ratios and interconnect complexity will continue to pose increasingly difficult challenges and also opportunities to inspection tools development.

In-line Defect Characterization and Analysis [Yield Enhancement]

Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

Next generation lithography [Yield Enhancement]

Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.

Factory-level and Company-wide Metrology Integration [Metrology]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules and ever increasing aspect-ratio levels.

Measurement of Complex Material Stacks, Interfacial Properties, and Structures [Metrology]

New metrology techniques capable of characterizing stack structures and structural and elemental analysis at device dimensions and measurements for beyond CMOS, and emerging materials and devices are needed in the near term. Nondestructive, production worthy wafer and mask-level metrology for critical dimension measurement for 3D structures, overlay, defect detection, and analysis. New strategy for in-die metrology must reflect across chip and across wafer variation. Statistical limits of sub-12 nm process control. Determination of manufacturing metrology when device and

interconnect technology remain undefined. Metrology tools to address Directed Self Assembly (DSA) and EUV mask defects.

Critical Metrology Consideration—Precision and Uncertainty [Metrology]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term "precision" is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool, and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

Lithography Metrology [Metrology]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

In The Long Term (2021 through 2028) —Enhancing Performance

Management of Leakage Power Consumption [Design]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness, and threshold voltage. This presents severe challenges in light of both technology scaling and variability.

Implementation of Non-classical CMOS Channel Materials [Process Integration, Devices, and Structures, Front End Process, Emerging Research Devices, and Emerging Research Materials]

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to be integrated physically or functionally onto a CMOS platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate, which is challenging. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development.

Identification, Selection, and Implementation of New Memory Structures [Process Integration, Devices, and Structures]

Line-dense, fast, and low-operating-voltage non-volatile memory will become highly desirable, and ultimate density scaling may require three-dimensional architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness (EOT) and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or developing alternative emerging technologies.

Future Challenges of RF and AMS CMOS [Radio Frequency and Analog/Mixed-Signal Technologies]

Radio frequency and analog/mixed-signal (RF and AMS) CMOS technologies are based upon the CMOS devices of the Process Integration, Devices, and Structures (PIDS) chapter utilizing the low standby power (LSTP) roadmap for microwave applications and the high performance (HP) roadmap for millimeter-wave applications. As reflected in the HP & LSTP roadmaps, fundamental changes in device structures such as the introduction of multiple-gates and/or fully-

depleted SOI will be required to sustain continued performance and density improvement. The electrical characteristics of these devices are fundamentally different from those of conventional CMOS. Potential benefits include higher voltage-gain and lower coupling between the drain and body. But these differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries. Thus, the fabrication of conventional precision analog/RF driver devices to be integrated alongside the scaled CMOS devices may require separate process steps. Even now, the impetus to enable system-on-chip (SOC) applications is encouraging the incorporation of optional analog or high-voltage devices and thereby expands the menu of potential devices albeit with the attendant cost increases.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Line edge roughness, trench depth and profile, via sidewall roughness, etch bias, thinning due to cleaning, CMP effects, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. Etching, cleaning, and filling high aspect ratio structures, especially low-κ dual damascene metal structures and DRAM at nano-dimensions are also big challenges. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo-mechanical effects. Novel/active devices may be incorporated into the interconnect lines. Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets is a key challenge.

EUV LITHOGRAPHY [LITHOGRAPHY]

As EUVL remains the leading candidate for the 22 nm and 16 nm half-pitches, extending it to higher resolutions becomes a significant long-term challenge. From what we know today, designs of 0.5 NA or larger at the current wavelength will necessitate either an eight-mirror unobscured or six-mirror center obscuration design. The eight-mirror design will have more diminished reflectance because of the added mirrors, requiring higher power sources for an equivalent wafer throughput. The angular spread in the six-mirror design is narrower, thus demanding a smaller field size and perhaps longer track length. The increase in NA will pose significant challenges in the depth of focus for both designs. Furthermore, to overcome shadowing and other 3D effects on the mask, absorber materials, absorber thickness, and multilayer stacks will have to be optimized.

An alternative solution path would be to reduce the EUVL wavelength to 6.x nm. In the near term, this path would inherit all the current challenges of EUVL, from source availability to mask infrastructure and resist performance. Multiple patterning with EUVL will also be an option, bringing with it added process difficulties and cost of ownership.

TRANSITION TO NOVEL STRUCTURES [FRONT END PROCESSES]

Several scenarios coexist for keeping continued scaling of cmos and memory devices. it is anticipated to proceed with scaling (equivalent scaling), by introducing new materials, new structures, and/or 3d integration. among all, the selection of a fundamental structure for cmos is very challenging, for example, a channel material and a multi-gate structure will require new process technologies to be concurrently developed. these technologies include starting materials, surface preparation, lithography, pattern etching, and gate stack with booster technique, doping, metrology, process uniformity, and reliability. Once selected, there is no going back. Coordination and discussion are needed in all aspects among itwgs viewed from process integration and manufacturing.

NON-DESTRUCTIVE, PRODUCTION WORTHY WAFER AND MASK-LEVEL MICROSCOPY [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. The combination of high-resolution optics, waveform analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement including sidewall shape and trench structures of damascene process. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

POWER AND BANDWIDTH DESIGN IN 3D SCALING [ASSEMBLY AND PACKAGING]

Power delivery and thermal dissipation design in ever extending 3D scaling are indispensable for further system integration. Co-design, low loss dielectrics material and optical signal acceptance at package level are required to extend physical density of bandwidth for digital electronics. Replacing solder balls of flip-chip with low profile fine-pitch Cu posts and introduction of fragile low-k layer in a die would induce critical chip-package-interference. Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult.

TRANSITION TO NOVEL STRUCTURES FOR BOTH CMOS AND MEMORY DEVICES [FRONT END PROCESSES]

There are many challenges to define, prioritize, and reach consensus to recommend potential solutions that will deliver materials with controlled properties. These properties must be defined in sufficient detail to enable ultimately to transfer to the Process and Integrated Device Structures (PIDS) and the Front End Processes (FEP) teams in a timely fashion for further pragmatic research and development. These properties must be able to describe the operation of emerging research devices in high density at the necessary nanometer scale of the long-range roadmap timing horizon and beyond. In order to improve control of material properties for high density devices, research on materials synthesis must be coordinated and integrated in parallel with work on new and improved metrology and modeling. Metrology to characterize properties in a realistic device has an increased need for further development of integrated devices. Accurate multiscale simulation is required for prediction of the device performance. Furthermore, life cycle assessment and risk management of emerging materials become more essential both for business considerations and the sustainability of enterprises.

Long-term challenges for emerging research devices are divided into those related to memory technologies, those related to information processing or logic devices, and those related to heterogeneous integration of multi-functional components. New memory technologies that combine the best features of current memories are required in a fabrication technology compatible with CMOS process flow. New manufacturable “beyond-CMOS” information processing technology compatible with new system architecture is required. Implementation of new information carrier (state variables) other than charges is demanded. A non-binary data representation and non-Boolean logic may be required.

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Devices (see the ERD and the ERM chapters). In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Especially, computational material science tools need to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations. Furthermore, modeling must assist metrology to enable the characterization of novel materials and devices.

IN THE LONG TERM (2021 THROUGH 2028) —COST-EFFECTIVE MANUFACTURING

IN-LINE DEFECT CHARACTERIZATION AND ANALYSIS [YIELD ENHANCEMENT]

Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

TEST DEVELOPMENT AS A GATE TO VOLUME PRODUCTION [TEST AND TEST EQUIPMENT]

The increasing trend of functional divergence in a device results in the corresponding complexity of test for yield learning as well as that of test development. Also with the increasing reduction in feature (and defect) sizes well below optical wavelengths, the rapidly increasing failure analysis throughput time, the reduction in failure analysis efficacy, and the approaching practical physical limit to other physical techniques (PICA, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of Design-for-Test (DFT) and test-enabled diagnostics and yield learning become paramount. As the result, yield learning methods need to be augmented with more universal deployment of on-die circuitry (DFT, etc.) across and throughout products, as well as with improvements of the on-die circuitry itself and diagnostic software tools with respect to fault isolation specificity. Where it may have been sufficient to isolate the failing bit in an array or the failing gate in logic in the past, there is a real business need to enable

isolating electrically the failing transistor or interconnect, or the semiconductor industry would suffer the economic consequences of reduced yield improvement learning rates on new process technologies.

SUSTAINABILITY AND PRODUCT STEWARDSHIP [ESH]

Business considerations and also sustainability metrics (in a cost-effective and timely way) are required for product stewardship. In addition, Design for Environment, Safety, and Health (DFESH) should become an integral part of the facility, equipment, and product design as well as management's decision-making. Environmentally friendly end-of-life reuse/recycle/reclaim of facilities, manufacturing equipment, and industry products are increasingly important to serve both business and ESH needs.

MEETING THE FLEXIBILITY, EXTENDIBILITY, AND SCALABILITY NEEDS OF A COST-EFFECTIVE, LEADING-EDGE FACTORY [FACTORY INTEGRATION]

Ability to load the fab within manageable range under changeable market demand and to utilize task sharing opportunities such as manufacturing outsourcing is required to keep the manufacturing profitable. Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing continues to challenge. Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] promotes reuse of building, production and support equipment, and factory information and control systems across multiple technology generations. Cost and task sharing scheme is highly expected on industry standardization activity for industry infrastructure development such as data standardization and visualization methodology.

SPECIAL TOPICS

MORE THAN MOORE

The term 'More than Moore' was introduced in the 2005 edition of the ITRS to denote the fact that, next to digital scaling, heterogeneous integration of new non-digital functionalities into smart systems became a driving factor for the technology roadmap. This trend, diversification in conjunction with miniaturization, led to an increasing complexity in the roadmapping process itself. Therefore, a methodology for the More than Moore roadmapping process was developed, as outlined in the 'More than Moore White Paper' (http://www.itrs.net/papers.html), which was released in 2010.

A prerequisite for the More than Moore roadmapping process is the identification of a number of figures of merit (FOM) for specific functionalities, such as wireless communication, power generation and management, sensing and actuating. An essential feature of More than Moore related technologies is that these are strongly dependent upon the application requirements, as determined by societal needs. For each of the relevant application domains (e.g. ICT, automotive, lighting, energy, healthcare), driving applications have to be identified, which are analysed to generate system views and, subsequently, generic functions. Due to the fact that the More than Moore domain clearly constitutes a cross-over of the chip level and the system level, the ITRS has started a cooperation with iNEMI (International Electronics Manufacturing Initiative), in order to address the technology/design/application interaction in the most effective way. Various TWGs are involved in this effort, most notably Design & System Drivers, RF & AMS, MEMS, Assembly & Packaging, and ERD/ERM.

By nature, the More than Moore domain is multidisciplinary, involving expertise from many different areas, such as electrical and mechanical engineering, materials science, biology and medical science. This is reflected in the present ITRS edition, in which an increasing numbers of parameters associated with these new functionalities are being addressed.

2013 ITRS "EQUIVALENT SCALING" UPDATE TIMING AND PIDS PURDUE MODELING

BACKGROUND OF PIDS/PURDUE MODELING FOR THE ITRS

During their 2012 and 2013 Update work, and to enable the significant amount of modeling work and resources required to develop future ITRS guidance tables, the ITRS PIDS TWG received approval from the IRC to initiate a partnership with Purdue University. PIDS assumed primary responsibility for interfacing with Purdue to assure alignment of the past ITRS MASTAR model approach with the new Purdue TCAD long-range dynamic modeling tools output. The ITRS Modeling TWG agreed also to participate in reviews with the PIDS and Purdue team. Purdue University agreed to support the ITRS, and would allow use of the Purdue online public modeling review resources for additional public discourse and input to the project.

Up to this year, MASTAR (references in the PIDS chapter) has been the main tool used to generate these device characteristics. Since it is based on compact modeling, a more sophisticated modeling tool is necessary beacause channel

lengths are getting to the sub-10-nm range and the body thicknesses for SOI and FinFET structures are substantially smaller. These small dimensions manifest in many quantum phenomena such as tunneling, carrier confinements in space and energy, ballistic transport, etc. Furthermore, two-dimensional finite-element methods are becoming more and more critical, and three-dimensional simulation will soon be mandatory for nanowire structures. Another consideration is new channel materials such as III-V and Ge. Thus, advanced, physics-based TCAD simulation tools are necessary.

The philosophy for PIDS logic team has been that the simulation tool will be open to the public, besides the input files and results, so readers not only will be able to reproduce the results, but also can vary the input parameters to see the effects and sensitivity. This requirement rules out commercial tools.

Given these requirements, PIDS is very fortunate to be able to get the involvement from the simulation group of Purdue University, with approval and full support from the IRC. The Purdue group is well-known for their suite of device simulation tools. Their comprehensive, well-established website NanoHub (references in PIDS chapter) hosts many device simulation tools that are in public domain, and in fact are popular and widely used world-wide. With Purdue's engagement, the ITRS benefits from the additional help from the man-power of students, guidance of the faculty, and the continued maintenance and improvement of these tools. The goal is to have these tools reside in some part of NanoHub, dedicated to ITRS, and will include the input and output files, documents for all the assumptions made, as well as instructions to run these tools, all accessible to the public.

To be clear, this addition of TCAD simulation tool is not meant to replace compact models. A compact modeling tool is easier and faster to run. And it is the only way to connect to circuit simulators to explore circuit performance. It is the intention of the teams that a compact modeling tool, or actual compact models, are maintained in parallel with the new TCAD simulation capability to satisfy different needs.

2013 ORTC Status for the the PIDS/Purdue Modeling

Due to trade-offs with "equivalent-scaling" process enhancements (copper and low-κ interconnect, strained silicon, high-κ/metal gate, FinFETs, FDSOI, III/V Ge, etc.), as performance and power management alternatives, the *printed* MPU and *physical* gate length trends received major corrections back in the 2008 and 2009 ITRS ORTC versions. However, those PIDS table model revisions remained unchanged in the 2011 and 2012, and now the 2013, ITRS versions. The physical gate length (GLphy) trend has been aligned with historical and survey data by the PIDS TWG and is on a slower 3.8-year cycle trend beginning 2009/32 nm through 2028/5 nm. The printed gate length (GLpr) begins a delayed three-year cycle trend in 2011, and continues through 2028 on a "shrinking" ratio relationship (negotiated between Lithography and FEP TWGs) to the physical gate length, and eventually leveling off to match the physical gate length at 2028/5 nm. Refer to Fig ORTC2.

As a result of announcements in 2011 of production of FinFET and FDSOI technology in 2012, PIDS ITWG revised their 2012 ITRS Update version tables to match new timing of those "equivalent scaling" tradeoff options. PIDS also added a Table for III/V Ge gate material (responsibility for developing tables for III/V Ge technology was previously passed to PIDS in 2011 from ERD/ERM TWGs). Due to possible acceleration of III/V Ge from 2019 to 2015, there will need to be work in 2014 by the TWGs to prepare for the 2015 ITRS Renewal (and possible impact of a 4–5-year accelerations of III/V Ge"equivalent scaling" technology).

For the logic section of the PIDS chapter, one of the main responsibilities is to provide projection for transistor performance for the next fifteen years. This is a challenging mission because not only the process parameters have to be realistic, thanks to the inputs from other chapters such as FEP, reliable predictive device modeling has to be used to make sure that they make sense from device and circuit performance point of view, thanks to the inputs from other chapters such as Modeling and Simulation and Design. Therefore, device simulator is an important tool for PIDS to predict the device characteristics.

In their premier 2013 TCAD work, the PIDS/Purdue team developed the 2013 PIDS ITWG tables, which model both near term (tied to previous MASTAR modeling results) and long term (tied to Purdue/PIDS TCAD dynamic modeling) intrinsic transistor characteristic trends (and in future work, will include ring oscillator simulations). The new transistor characteristic trends supported the adjustment of the 2011 and 2012 version PIDS data table average 13% intrinsic frequency [1/(CV/I)] growth trends down to a slower trend. The average trend is across the technology "equivalent scaling" Bulk, FDSOI, and FinFET technologies (see details in the PIDS chapter). That slower trend is now more compatible with the present guidance from the Design ITWG (that only 4% growth of chip frequency is required both near and long term). The slower PIDS model intrinsic frequency growth should still allow adequate "headroom" for designers to plan complex SOC and MPU products over both the near and long term-ranges.

THE MEANING OF ITRS TIME OF INTRODUCTION

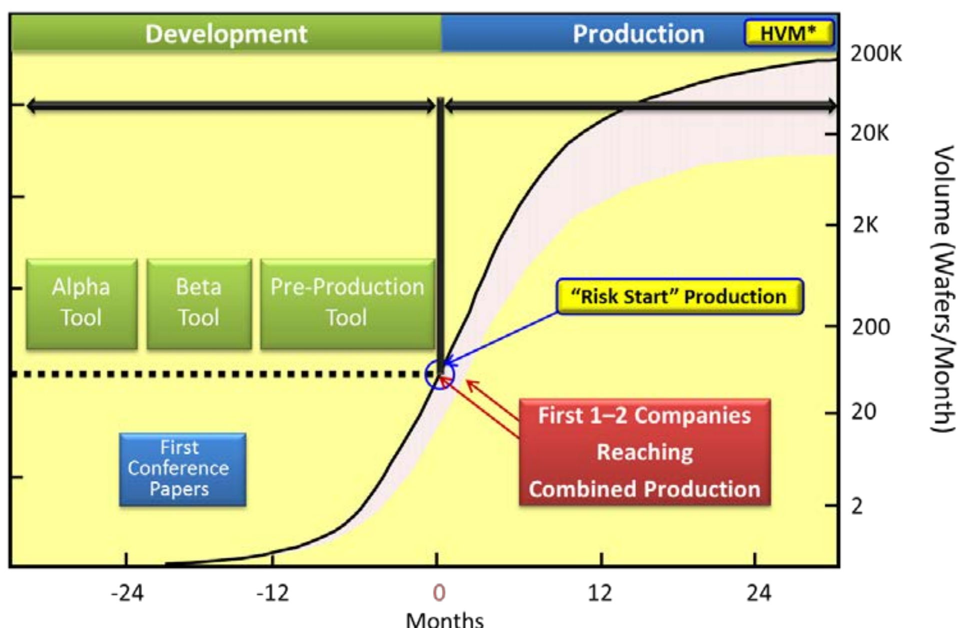
The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production." which is defined in Figure 1a.

Figure 1a was first revised in the 2011 ITRS to no longer include reference to volume parts per month, due to the variability of different product die sizes for first production targets. Therefore, only the typical industry high volume ramp scale is retained in the 2011 and 2012 roadmaps. After additional work on the 2012 Update, it was decided by the IRC that the timing of production could refer to one leading IDM or foundry company (representing many fabless companies) that would also represent a significant volume ramp of capacity and additional companies would follow that lead. A note was added to the ITRS timing graphic to describe this new change in definition of ITRS Production.

A graphical note was included, at the request of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) TWGs as seen in Figure 1b. The note is a reminder of the very wide time range required to capture early research activities that may result in potential solutions items for the ITWG Difficult Challenges. It has become increasingly important to communicate a broad horizon encompassing both the period preceding the first manufacturing alpha tools and materials and also the period that extends to the classic ITRS 15-year horizon and even beyond.

The preceding horizon is required to capture the period of the very first technical conference paper proposals until the start of development activities; at which point typically a transfer from ERD/ERM to PIDS/FEP ITWGs occurs. The early research horizon also reminds the readers and the ITRS participants of the influence of the National Technology Roadmap for Semiconductors (NTRS: 1991–1998) and the International Technology Roadmap for Semiconductors (ITRS: 1998 to present), as the work of the roadmaps tracked and influenced the manufacturing technology needs and priorities of industry R&D long before they turn into production. Many academic and industry studies have examined and commented on the uniqueness and the impact of pre-competitive cooperation provided by the International Technology Roadmap for Semiconductors.

For more explicit clarification, see Figure 1b, in which an example is shown for a new gate structure potential solution (III/V hi mobility gate) targeted for 2019 production. In this example, the first research papers appear in 2007, and the potential solution technology was transferred to PIDS during the 2011 ITRS roadmap work, when more detailed line item characteristics were defined by the PIDS ITWG in their 2011 work, and also included in the PIDS 2012 Update work.



Fewer leading IDM companies requires adaption of definition to allow one IDM company or a foundry representing many fabless companies to lead a technology production ramp timing

Figure 1a A Typical Technology Production "Ramp" Curve (within an established wafer generation)[2]

The "production" time in the ITRS refers to the time when the first leading company brings a technology to production. Typically, a second company follows within a short period of time, and ideally as soon as three months; however sometimes there is a longer time for the second company to get into production, especially when considering alternative "equivalent scaling" technology pathway options. Additional complexity of timing occurs when rapid accelerations occur and a leading company will go into production ahead of the ITRS Roadmap timing targets. This happened in the case of MugFET (aka FinFET) production announcements in 2011 (from 2015), and there is the possibility of III/V Ge technology acceleration to 2015 (from 2019). It remains to be seen how rapidly "fast following" companies provide their own announcements in response to production accelerations, and updates on this topic have been discussed by the IRC and is included in the 2012 Update (online at www.itrs.net).

For further clarification, "production" means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero" in Figures 1a and 1b can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM (also called "risk starts" in industry jargon) to full capacity can take nine to twelve months. As an example, this time would correspond to the same time for ramping device unit volume capacity from 6K units (samples/"risk starts") to 6M units per month [for the example of a chip size at 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month)].

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the industry is approaching the time for a new 450 mm wafer generation transition, additional scrutiny has been given to the historical ramp rate for a technology cycle that has been ramped in two wafer generations of the first leading companies at the same time. It is during that transition of a technology cycle coexisting within two wafer generations that the economic productivity gain modeling is also examined.

[2] *See Figure 1b below for ERD/ERM Research and PIDS Transfer timing*

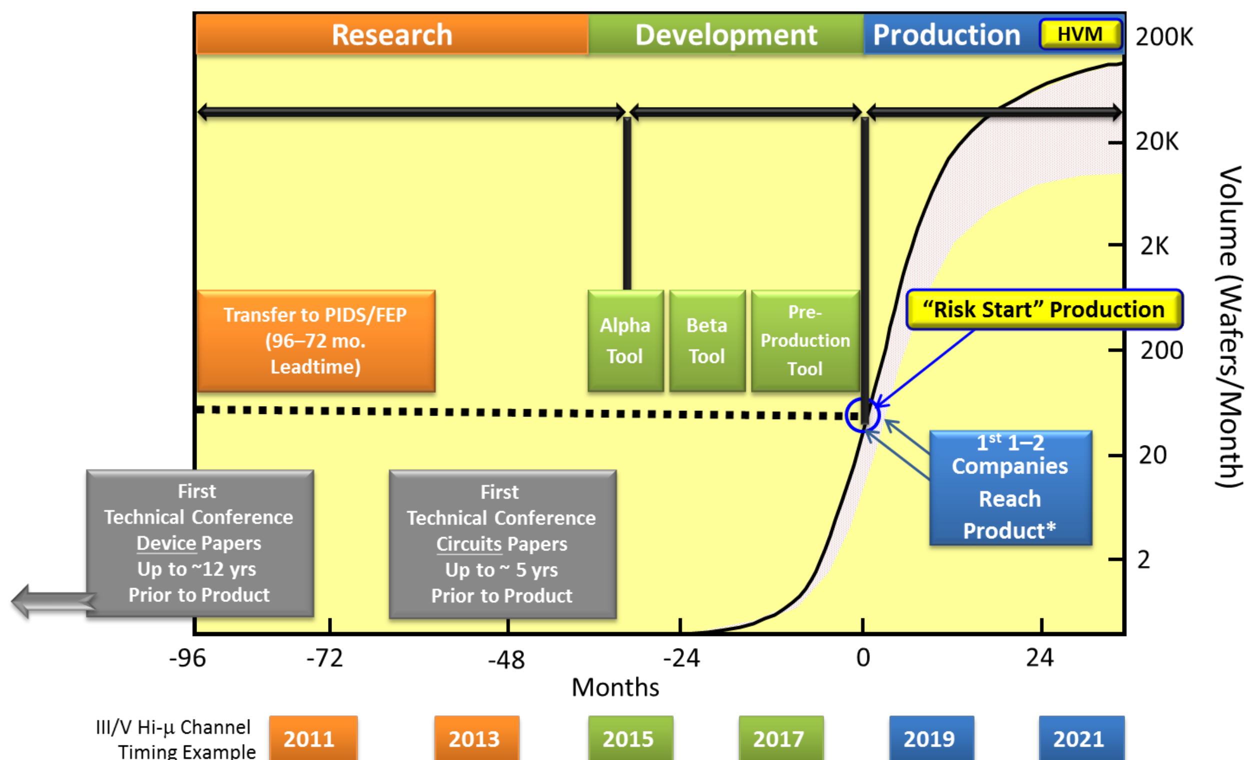


Figure 1b A Typical Technology Production "Ramp" Curve for ERD/ERM Research and PIDS Transfer

Overall Roadmap Technology Characteristics

"Moore's Law," established over five decades ago by Gordon Moore of Intel Corporation, is a concept that states that market pressures drive semiconductor chip functional density to double on a periodic basis; and the cycle of that period is set by the technological advancement of manufacturing process capability. In addition to the functional density, the "Moore's Law" concept also included the concept of affordability, observing that technology introduced too soon could increase the cost/function, causing the chip to be unaffordable to the market.

For many decades of technology advancement, the drive to meet the requirements of "Moore's Law" also had synergistic benefits due to the physics of semiconductor operation, which caused shrinking dimensions of the transistor gate thickness and channel length to reduce the voltage and power required for reliable operation of both switching and storage operations, while at the same time also increasing the speed of operation of the device.

This "triumvirate" of functionality, higher performance, and lower power market benefits to consumers continued into the early 2000's; when, passing through nano-scale dimensions, the shrinking of technology began to approach molecular and atomic levels (in the case of gate and channel thickness and length). The result was that voltage levels could no longer reduce due to causing breakdown and high current drain, both operating and standby.

As a result the usual dimensional reduction of the scaling of printed and physical gate length of transistors had to slow, compensated by a tradeoff with what became known as "Equivalent Scaling"—the inclusion of process techniques such as gate strain in the channel, HiK-metal gate materials in the transistor gate; and more recently, transistor 3D architecture called multiple gate FET (MugFET) or FinFET, and Ultra Thin Body and BOX Fully Depleted Silicon on Insulator. On the near horizon, new channel materials, such as III/V Germanium, will also enter into manufacturing to benefit performance and power of devices.

Additional chip and system-level architectural and software design “Equivalent Scaling” such as SRAM memory architecture, CPU multiple-core, and power software management enabled the chips, limited by slower voltage decreases and slower speed of operation, to still achieve the needed market low power and high performance requirements of the latest centralized Communications and Cloud Computing high performance and also the Portability and Mobility low power of the latest and future market applications.

These system-level alternative power performance tradeoffs are also enabled by the “Moore’s Law” functional density drivers, which are enabled by the dimensional size of the function itself. The size of the function is set fundamentally by the half-pitch of interconnect, in conjunction with the number and size of the vertical wiring levels, ultimately connecting to the finished device by assembly and packaging technology. Additional ITRS definition work on these important “Moore’s Law” functional density technology enablers is ongoing and includes the relationships of the new FinFET transistor layouts, and technology characteristics which are described in greater detail in the Interconnect and Design and PIDS Chapters.

The ITRS has guided the research and development community by identifying grand challenges and potential solutions that were narrowed, from the previous typical 12–15 years academic research horizon required lead time, into the 4–8 year manufacturer and equipment and material supplier development period; then ultimately into the production-ready manufacturing solutions available to the market today and in the near future.

Examples of the descriptions of grand challenges and the narrowing of potential solutions can be seen in the individual TWG chapters. It is in the ITRS chapters that the required process capability to create ORTC driver dimensions of both the interconnect and also the printed gate length features of transistors.

Continuing Moore’s Law functional density benefits and managing power and performance tradeoffs remain as the key drivers of the Roadmap grand challenges and potential solutions. Therefore, driving half-pitch reduction, combined with managing and gate-length and “Equivalent Scaling tradeoffs also remain as drivers.

The MPU/ASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. The trend targets have been updated in the 2013 ITRS ORTC tables from the 2011 and 2012 ITRS Roadmap editions. The MPU/ASIC M1 trend leveled off at 40nm in the period from 2010 to 2013, and is anticipated in the 2013 ORTC Table 1 to continue forward on a 3-year technology cycle (0.5x every 6 years). It is possible that the industry will continue to press for the historical 2-year cycle (0.5x per 4 years) trend through 2017. The actual industry trends will be monitored in 2014 and 2015 for updates in future ITRS renewals.

Note that Logic technology “Node Naming,” is now included in the 2013 ORTC Table 1 as a helpful guide to typical industry naming convention. However, “Node Naming” is included for alignment purposes only, and will be monitored for changes, along with the best estimates of alignment to actual technology data in available public documents.

Although the DRAM M1 half-pitch target is unchanged in the first column year, 2013/28nm, the PIDS ITWG survey consensus updated the DRAM M1 half-pitch trend to a 4-year cycle (0.5x every 8 years), slowing from the 3-year pace of the previous roadmap version. The MPU/ASIC M1 half-pitch lags behind DRAM, however, the faster MPU/ASIC 3-year cycle trend crosses DRAM at 2026/9 nm, and then leads DRAM through the balance of the roadmap. See the new 2013 ORTC MPU/ASIC and DRAM trends in Figures ORTC1 and ORTC2 below.

The Flash product half-pitch, unchanged for the 2012 ITRS ORTC Update, continues to be defined as an uncontacted polysilicon half-pitch; and was also revised in 2011 from the 2009 and 2010 ITRS additions by continuing the two-year cycle trend through 2009/39 nm, then matching the PIDS Flash survey 2010/24 nm before turning to the survey-forecasted 4-year cycle (0.5× per 8 years) through 2018/12 nm. At the 2018 point, the Flash Flash survey consensus forecasts the trends to remain flat to anticipated Flash cell design limitations and also due to costs of 2D processing approaching an unaffordable level (see Figure ORTC1).

The Flash 3D bit layer model was updated in 2013 to align with the recent introduction of a 24-layer 3D NAND device, processed at a relaxed 64nm process point. The 3D NAND range of layers was also updated, along with the anticipated trend of relaxed process technology reduction going forward. See the PIDS TWG chapter models discussion for additional details.

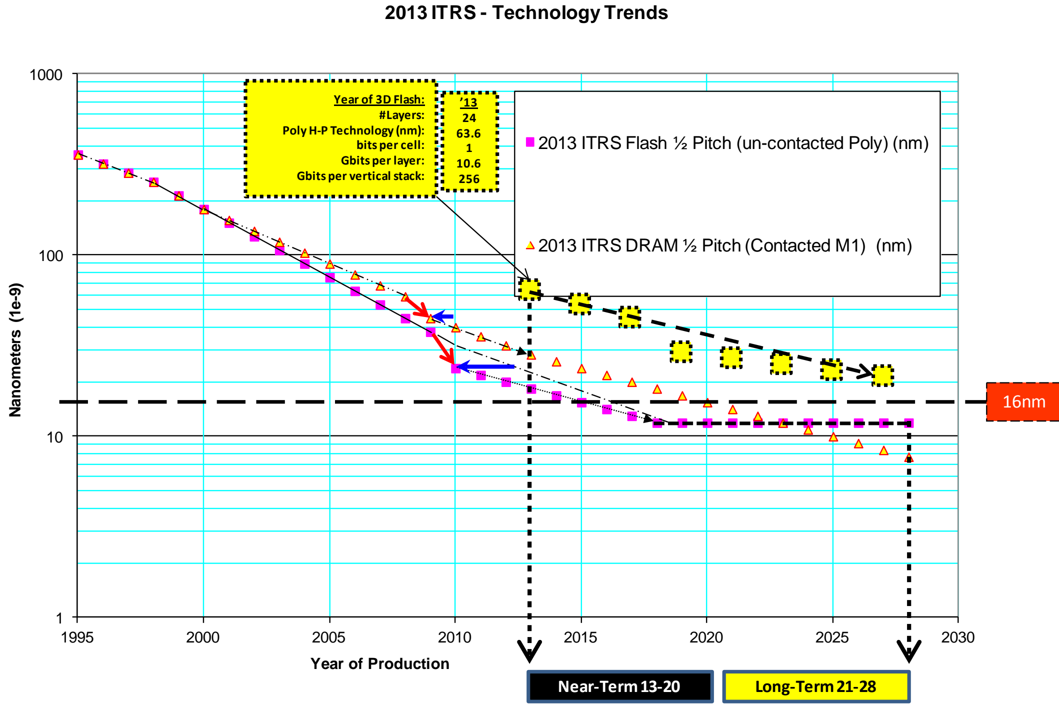


Figure ORTC1 2013 ITRS—DRAM and Flash Memory Half Pitch Trends

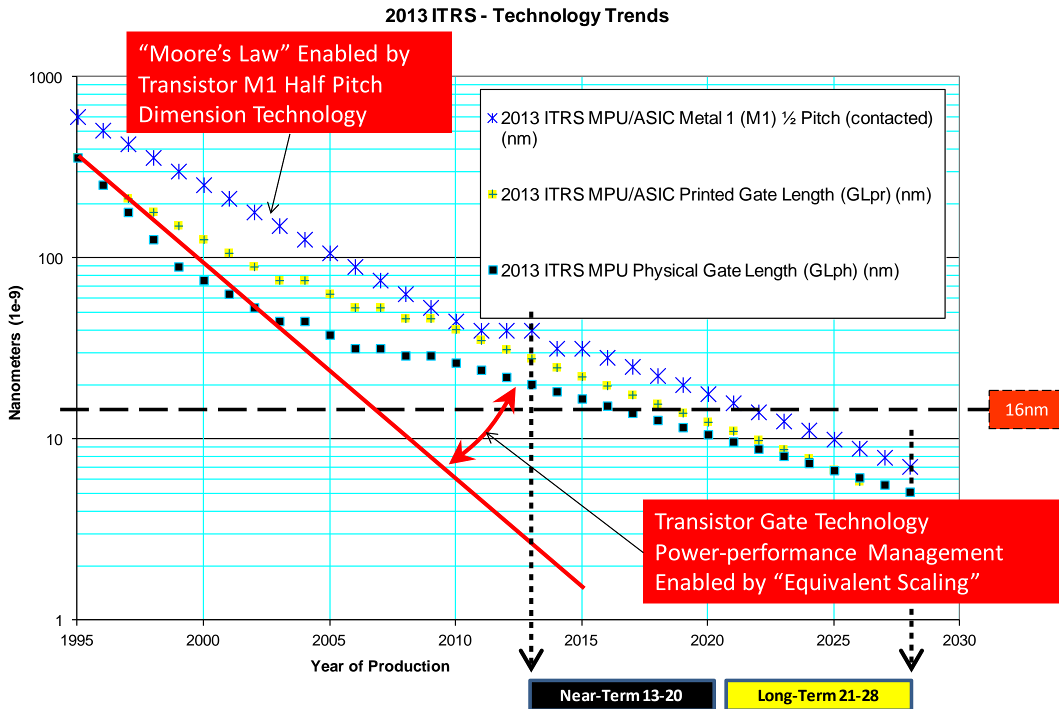


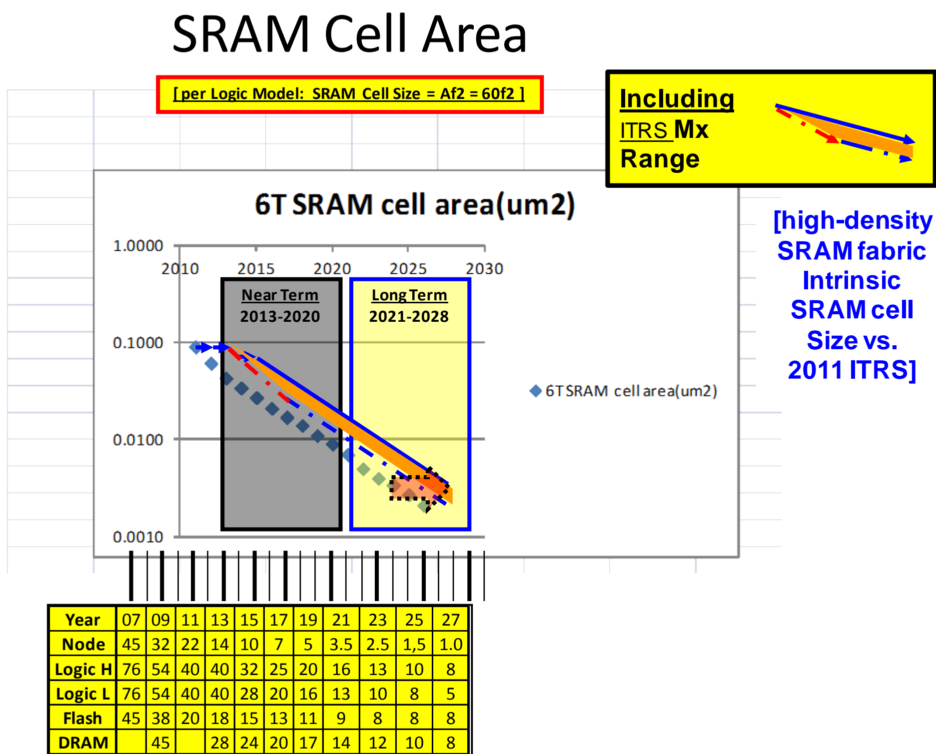
Figure ORTC2 2011 ITRS—MPU/ASIC Half Pitch and Gate Length Trends

To reflect the diversity of product technology cycle needs and to continue close monitoring of future Roadmap trend shifts, it was agreed by the IRC to continue the practice of publishing annual technology requirements in the 2013 ITRS Renewal Work from 2013 through 2020, called the “Near-term Years,” and also annual requirements from 2021 through 2028, called the “Long-term years.” As seen above in Figures ORTC1 and ORTC2, the long-term years of the 2013 ITRS are now somewhat aligned with the timing of the especially-challenging sub-1× nm technology era (2019/13–14 nm M1 to 2026/6.3–6 nm M1).

In the spirit of continued productivity and simplification of the roadmap, the 2013 ITRS now includes a “simplified” version of the Table ORTC1, with fewer columns and line items (see below). Included also is the link to the more detailed annualized table.

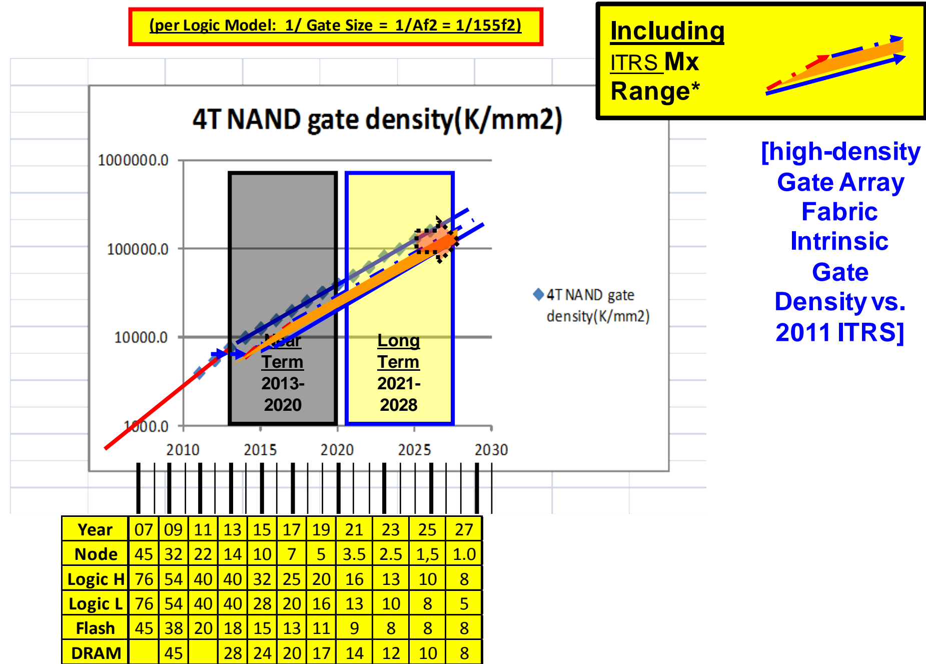
ORTC “Moore’s Law” and Power/Performance Drivers

As part of the 2013 ITRS Renewal work, the IRC agreed among their regional members to examine other options for ORTC technology trend drivers in the near term years which are typical of available industry data and expectations of the chip IDM and foundry/fabless design communities. Specifically, it was agreed that the ORTC Table 1 would add line items which track and target: Logic SRAM (6-transistor) Cell Area (μm^2) [see ORTC3 below]; and also Logic (4-transistor) NAND Gate Density ($Gates/mm^2$) [see ORTC4 below]—trends established by Design TWG and ORTC models. This work aligned also with recommendations for simplification of the tables around PIDS high performance and low power drivers of the 2013 ITRS ITWG work.



Year	07	09	11	13	15	17	19	21	23	25	27
Node	45	32	22	14	10	7	5	3.5	2.5	1,5	1.0
Logic H	76	54	40	40	32	25	20	16	13	10	8
Logic L	76	54	40	40	28	20	16	13	10	8	5
Flash	45	38	20	18	15	13	11	9	8	8	8
DRAM		45		28	24	20	17	14	12	10	8

Figure ORTC3 2013 ITRS—Logic SRAM Cell Area Trends



Year	07	09	11	13	15	17	19	21	23	25	27
Node	45	32	22	14	10	7	5	3.5	2.5	1,5	1.0
Logic H	76	54	40	40	32	25	20	16	13	10	8
Logic L	76	54	40	40	28	20	16	13	10	8	5
Flash	45	38	20	18	15	13	11	9	8	8	8
DRAM		45		28	24	20	17	14	12	10	8

Figure ORTC4 2013 ITRS—Logic Gate Density Trends

In their 2013 work, the IRC and the Cross-TWG study groups and subteams acted on the IRC recommendations and made proposals that would be suitable for the 2013 ITRS roadmap development work. This work addressed the need to be current to the latest status of industry needs and plans. The near term range industry technology status validation and alignment activities addressed the main priorities of the ITRS mission to create the Grand Challenges and Potential Solutions for pre-competitive research by academic and consortia and government laboratories.

The resulting consensus line item drivers are now included in a single table, Table ORTC1, of which a summary is presented below. The previous Tables ORTC2-7 are now referred to the appropriate TWG Chapter, per the matrix below. *Follow this link for the detailed Table ORTC1.*

ORTC [PREVIOUS ITRS VERSIONS] TABLE TWG CHAPTER REFERENCE MATRIX:

- Table ORTC2a,b DRAM and Flash Model Characteristics – See PIDS
- Table ORTC2c,d MPU/ASIC Model Characteristics – See Design
- Table ORTC3 Lithography and Wafer Size Trends – See Litho and Factory Integration
- Table ORTC4 Performance of Packaged Chips – See Assembly and Packaging
- Table ORTC5 Lithography Mask Counts and Defect Densities – See Lithography and Yield Enhancement
- Table ORTC6 Power Supply and Power Dissipation – See PIDS and Design
- Table ORTC7 Cost – Industry needs continuous -29% Cost/Function reduction; and Wafer Generation Productivity Improvements needed to compensate for increasing technology insertion costs – see Factory Integration

Table ORTC1 Summary of 2013 ORTC Technology Trend Targets–2013-2020

Year of Production	2013	2014	2015	2016	2017	2018	2019	2020
Logic Industry "Node Name" Label	"16/14"		"10"		"7"		"5"	
Logic ½ Pitch (nm)	40	32	32	28	25	23	20	18
Flash ½ Pitch [2D] (nm)	18	17	15	14	13	12	11	10
DRAM ½ Pitch (nm)	28	26	24	22	20	18	17	15
FinFET Fin Half-pitch (new) (nm)	30	24	24	21	19	17	15	13
FinFET Fin Width (new) (nm)	7.6	7.4	7.2	7.0	6.8	6.6	6.4	6.2
6-t SRAM Cell Size(um2) [@60f2]	0.096	0.061	0.061	0.048	0.038	0.030	0.024	0.019
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	0.248	0.157	0.157	0.125	0.099	0.078	0.062	0.049
4-input NAND Gate Density (Kgates/mm) [@155f2]	4.03E+03	6.37E+03	6.37E+03	8.03E+03	1.01E+04	1.27E+04	1.61E+04	2.02E+04
Flash Generations Label (bits per chip) (SLC/MLC)	64G /128G	128G /256G	128G /256G	256G /512G	256G / 512G	256G / 512G	512G / 1T	512G / 1T
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	16-32	16-32	16-32	16-32	16-32	32-64	32-64	48-96
Flash 3D Layer half-pitch targets (nm)	64nm	54nm	54nm	45nm	45nm	32nm	30nm	29nm
DRAM Generations Label (bits per chip)	4G	8G	8G	8G	8G	16G	16G	16G
450mm Production Risk Starts (1Kwspm)				2016				
450mm Production High Volume Manufacturing Begins (100Kwspm)							2018	
Vdd (High Performance, high Vdd transistors)[**]	0.86	0.85	0.83	0.81	0.80	0.78	0.77	0.75
1/(CV/I) (1/psec) [**]	1.13	1.23	1.53	1.63	1.75	1.84	1.97	2.00
On-chip local clock MPU HP [at 4% CAGR]	5.50	5.72	5.95	6.19	6.44	6.69	6.96	7.24
Maximum number wiring levels [unchanged	13	13	13	13	14	14	14	14
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	28	25	22	20	18	16	14	12
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	20	18	17	15	14	13	12	11
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	23	21	19	17	16	15	13	12

Table ORTC1 Summary of 2013 ORTC Technology Trend Targets–2020-2028

Year of Production	2021	2022	2023	2025	2028
Logic Industry "Node Name" Label	"3.5"		"2.5"	"1.8"	
Logic ½ Pitch (nm)	16	14	13	10	7
Flash ½ Pitch [2D] (nm)	9	8	8	8	8
DRAM ½ Pitch (nm)	14	13	12	10	7.7
FinFET Fin Half-pitch (new) (nm)	12	11	9.5	7.5	5.3
FinFET Fin Width (new) (nm)	6.1	5.9	5.7	5.4	5.0
6-t SRAM Cell Size(um2) [@60f2]	0.015	0.012	0.010	0.0060	0.0030
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	0.039	0.031	0.025	0.018	0.009
4-input NAND Gate Density (Kgates/mm) [@155f2]	2.55E+04	3.21E+04	4.05E+04	6.42E+04	1.28E+05
Flash Generations Label (bits per chip) (SLC/MLC)	512G / 1T	1T / 2T	1T / 2T	2T / 4T	4T / 8T
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	48-96	64-128	64-128	96-192	192-384
Flash 3D Layer half-pitch targets (nm)	28nm	27nm	27nm	25nm	22nm
DRAM Generations Label (bits per chip)	32G	32G	32G	32G	32G
Vdd (High Performance, high Vdd transistors)[**]	0.74	0.72	0.71	0.68	0.64
1/(CV/I) (1/psec) [**]	2.10	2.16	2.29	2.52	3.17
On-chip local clock MPU HP [at 4% CAGR]	7.53	7.83	8.14	8.8	9.9
Maximum number wiring levels [unchanged	15	15	15	16	17
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	11	10	9	7	5
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	10	9	8	7	5
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	11	10	9	8	6

*** Note: from the PIDS working group data; however, the calibration of Vdd, GLph, and I/CV is ongoing for improved targets in 2014 ITRS work*

WORKING GROUP SUMMARIES

Throughout 2013, all the working groups reviewed their previous assessments and adjusted their chapter reports and tables as determined by their world-wide teams. Most work resulted in significant revision. For this edition of the roadmap, several teams impacted most by recent developments in the industry and the prospect of new drivers and technologies continue to explore/assess technology needs and possible solutions. In some cases, this work continues into 2014.

We have summarized the 2013 work at this link: *http://www.itrs.net/Links/2013ITRS/Summary2013.htm*. The full version of the 2013 edition of the ITRS is found at *http://www.itrs.net/Links/2013ITRS/Home2013.htm.*