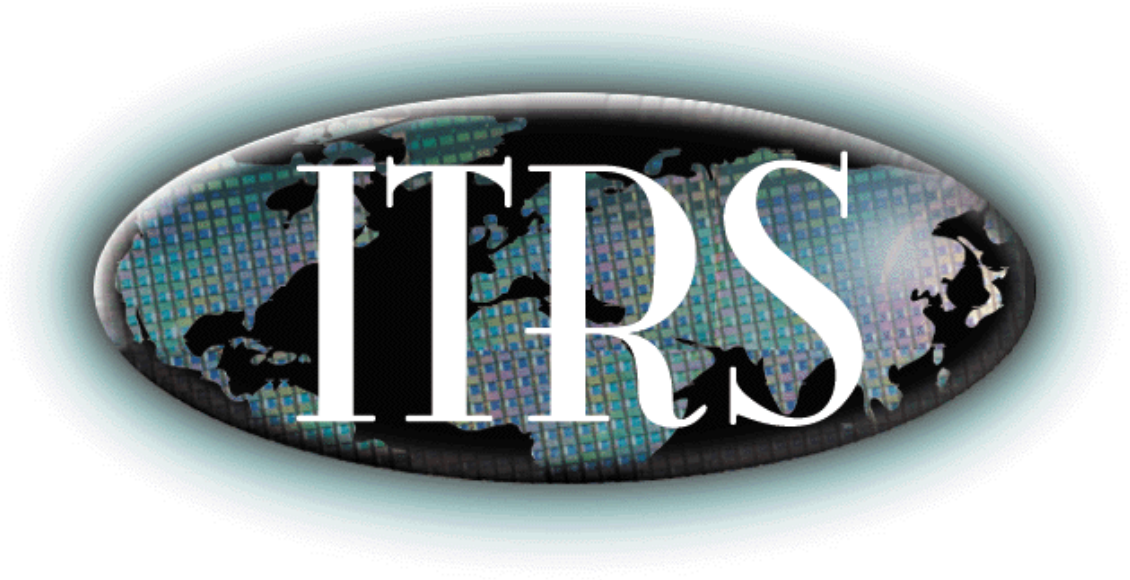

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES

1.0 SCOPE

Radio frequency (RF) and analog/mixed-signal (AMS) technologies serve the rapidly growing advanced communications and *"More-than-Moore (MtM)"* markets and represent essential and critical technologies for the success of many semiconductor manufacturers and the ultimate success of the future Internet of Things (IoT). Communications products and emerging products that support applications such as radar imaging, defense, and homeland security all have functionalities enabled by *MtM*, RF, and AMS technologies. These technologies are becoming key drivers for high-volume manufacturing. Consumer products account for over half of the demand for semiconductors. Fourth generation (4G) cellular phones and tablets now have a much higher RF and AMS semiconductor content and now are a very large fraction of the mobile market compared to only 5 % of the market a few years ago. The iPAD for example has more than 19 RF and AMS front-end components [1]. The consumer portions of the RF and AMS markets are very sensitive to cost. With different technologies capable of meeting similar technical requirements, time to market and overall system cost will govern technology selection.

The four major RF and AMS technology-device sub-groups that comprise many RF and AMS technologies are:
1) RF Complementary Metal Oxides Semiconductor (CMOS)
2) Group IV Silicon Bipolar and BiCMOS
3) Group III-V Compound Semiconductor
4) Passive On-Chip Devices

Unlike RF CMOS, some of the technologies considered in this RF and AMS Chapter currently lag technology and processing capabilities needed for reliable manufacturing, For those technologies, this RF and AMS roadmap pertains more to prototype capabilities rather than the usual CMOS volume production associated with most of the other ITRS Chapters.

Figures of merit (FOMs) for device technologies that relate to those circuit-level FOMs needed to support the performance requirements of systems drive the development of RF and AMS technologies. The FOMs are usually those FoMs for low-noise amplifiers (LNA), voltage-controlled oscillators (VCO), power amplifiers (PA), analog-to-digital converters (ADC), and serializer-deserializers (SerDes).

The technologies presented herein depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe and others of which have not traditionally been compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table. Compound semiconductors become more significant as today's emerging research devices, especially as those devices based on the More-than-Moore (MtM) technologies that are described elsewhere in this 2013 edition of the ITRS are deployed in the marketplace.

The purposes of this 2013 ITRS RF and AMS chapter are as follows:

1. Present the challenges that RF and AMS technologies have in meeting the demands of exemplary applications shown in Figure RFAMS1. Application frequency bands from RF (0 to 0.4 GHz), microwave (0.4 GHz to 30 GHz), and millimeter wave (30 GHz to 300 GHz) generally drive different technology requirements and this is reflected in the chapter. In future years, we will be addressing applications beyond 300 GHz as they emerge in the marketplace.

2. Present the challenges and requirements of Si RF CMOS, Si Bipolar, including SiGe heterojunction bipolar transistors (HBTs), Si/SiGe BiCMOS (bipolar + CMOS), III-V compound semiconductor devices, and passive on-chip device device technologies to meet the needs of these applications.

We base the Technology Requirements Tables (RFAMS2 and RFAMS3) for the group IV bipolar and group III-V compound semiconductor devices on a consistent set of refererence input data that are not necessarily consistent with the

Technology Requirements Tables for CMOS presented in the other Chapters of this 2013 Edition of the ITRS. ITRS members expect to have a uniform and consistent set of input data for all device techonlogies in the 2014 ITRS Update.

The following RF CMOS Sections numbered 1.1, 2.1, 3.1, 4.1, and 7.1 are copied from the 2011 ITRS RF and AMS Chapter and have not been updated for 2013. Also, the RF CMOS Table RFAMS1 is copied from the 2012 ITRS Update.

Analog - Carrier Frequency Bands			
LF Analog (0.0 GHz-0.4 GHz)	**RF (0.4 GHz-30 GHz)**	**Millimeter-Wave (30 GHz-300 GHz)**	**THz (> 300 GHz)**
Example applications			
Automotive controls	Cellular	60 GHz point-to-point	No products yet
On-chip regulators	WLAN	Imaging	
Power management	SerDes	Automotive radar	
	ADC,DAC	Wireless backhaul	

Figure RFAMS1 Analog and Carrier Frequency Bands and Example Applications considered in formulating this Roadmap

1.1 RF CMOS

As in previous years, the application drivers for the CMOS section are mobile transceivers in the 0.4 GHz – 30 GHz frequency range and various commercial applications in the 30 – 300 GHz frequency range. In addition, this year, the ITRS is putting additional effort to cover CMOS for mixed-signal analog applications. Therefore, we also consider the impact of CMOS device parameters on analog circuits that are not commonly used with RF application. A DC to high frequency wide-band amplifier is a typical building block seen in wire-line receivers with bandwidth reaching many GHz or higher. In optical communication with CMOS photonics, the data rate is already above 10 Gbps and is well on its way to top 40 Gbps and likely will reach 100 Gbps in the not too distant future. Wide-band trans-impedance amplifiers (TIA) are often used to convert photo-diode (PD) output to voltage levels suitable for CMOS digital signal processing.

The technology bases of this section are the CMOS devices of the *Process Integration, Devices, and Structures (PIDS)* chapter utilizing the low standby power (LSTP) roadmap for microwave applications and the high performance (HP) roadmap for millimeter-wave applications. The LSTP roadmap was selected as the basis for mobile microwave applications because portable applications require lower standby power and higher bias voltages than afforded by HP CMOS. The HP roadmap was selected for millimeter-wave applications because of the added device performance. The devices in the RF and AMS roadmaps are assumed to be identical to those in the PIDS roadmaps, but modifications may prove necessary if key analog properties cannot be realized. Contrary to previous editions of the RF and AMS roadmaps, the devices are now placed into production concurrently with the PIDS roadmap to reflect the System-on-a-Chip (SoC) nature of some applications requiring RF and AMS functions on mainly digital chips. The quality of high-frequency models and other tools to support RF and AMS design may improve over the first few years of production. The roadmap treats a performance-RF/analog device modeled after the LSTP or HP device. Such devices are used in circuits for transceivers; frequency synthesizers, frequency converters and amplifiers. Supporting analog-specific applications

requires device characteristics that are difficult to achieve with scaled MOS. Driving RF signals off-chip also requires higher voltage devices. Requirements for such devices include analog precision MOS device scaling and relatively high voltage compatibility to achieve high signal-to-noise ratios and low signal distortion. Such devices are typically available in CMOS technology offerings to support interfacing to higher-voltage input/output (I/O) ports. The performance of these devices can be found technical requirements sections of prior years of the ITRS RF and AMS chapter. Furthermore, many foundries also are including optional analog-friendly FETs in their CMOS offering. For such devices, the DC voltage gain would increase with increasing gate length in contrast to digital FETs where the halo implant causes the gain to effectively saturate and remain constant with increasing gate length. [2]

1.2 GROUP IV SILICON BIPOLAR AND BICMOS

For the first time with this 2013 edition, the roadmaps for Silicon Bipolar and BiCMOS and for III-V Compound Semiconductors are consistent with same reference input data. But, this consistency is not necessarily with the CMOS tables elsewhere in the 2013 ITRS.

1.2.1 DEVICES COVERED BY THE ROADMAP AND THEIR APPLICATIONS

The aim of this roadmap is to cover the bipolar transistors, and more specifically Si/SiGe heterojunction bipolar transistors (HBTs), for which performance increases are driven by RF/AMS applications and several players exist. Consequently, not all types of Si/SiGe HBTs available in today's technologies are covered in the roadmap.

High-voltage NPN and PNP bipolar transistors are used and are the topic of research for applications operating at frequencies below 5 GHz such as cellular and WLAN power amplifiers (PA), operational amplifiers, etc. These developments are tied to specific applications for which the performance of the bipolar transistors may no longer be the key driver. As an example, performance and cost of cellular and WiFi PAs are now dominated by the integration choices (passives, packages …). The roadmapping exercise of these devices is complicated because establishing the link between device and product performance may not be clear. For this reason the PA-NPN transistor is no longer part of the roadmap.

High-speed PNP (HS-PNP) development is driven by the applications of complementary bipolar and BiCMOS technologies (C-BiCMOS). Complementary bipolar circuits are attractive for (operational) amplifiers with low quiescent power consumption and high linearity across a large frequency range that often includes DC. These circuits greatly benefit from complementary technologies that offer NPN and PNP transistors with matched performance. Complementary BiCMOS (C-BiCMOS) technology seeks to maximize tradeoff between linearity and power consumption for applications that require very large bandwidth (e.g. A-D conversion, operational amplifiers and cable drivers). Overall performance is usually limited by the PNP. This device is vastly improved by introduction of silicon germanium technology. However, the HS-PNP transistor has been removed from the roadmap table because there are too few commercial sources of SiGe-based C-BiCMOS for reliable benchmarking.

Therefore, the roadmap covers the high-speed Si/SiGe NPN (HS-NPN) transistors only, and the scope of this section is then to provide requirements for this transistor. Improvements in the performance of the HS-NPN device are driven by the requirements of millimeter-wave products. These include circuits for wireless (~60 GHz WLAN) and wireline communications (40 Gb/s, 100 Gb/s, 400 Gb/s Ethernet and beyond), automotive radar (~77 GHz) and emerging applications up to ~170 GHz for industrial, medical, security, space, radio-astronomy, and other technologies [3,4]. The goal of extending the performance of the Si/SiGe HBTs is twofold. First, it is to allow the robust design of systems forecasted to operate at frequencies up to ~500 GHz by the end of the roadmap (which corresponds to ~ f_{MAX} / 3). Secondly it is to improve the performance (gain, noise figure, power consumption, etc.) of circuits operating at lower frequencies for existing applications; those already addressed or targeted by present bipolar / BiCMOS technologies.

The HS-NPN roadmap was generated from TCAD and compact model based predictions. TCAD tools included Boltzmann and hydrodynamic carrier transport, which were calibrated on the most recently obtained experimental results for an industrial prototyping technology ([5], designated as node N1 in Table RFAMS2). Results from the technology presented in [6] also contributed to calibrate the tools. The node N1 doping profile was scaled and properly modified towards the presently known ultimate physical limit (node N5 [7]) to yield the profiles of three more intermediate nodes N2, N3, and N4. The interface and contact resistances were assumed to reduce moderately from one node to the next compared to the CMOS roadmap. By varying the emitter width (representative for the critical dimension), a balanced vertical and lateral device design was found with respect to f_T and f_{MAX} for each major node. The five resulting nodes are considered as the major subsequent technology generations and were assigned to specific years of production release. The corresponding High Current Model L2 (HICUM/L2) parameters were extracted from the electrical results of these major nodes. These one-dimensional structure related model parameters were then augmented by parasitic elements resulting from realistic three-dimensional (3D) device structures, using e.g., a 3D Poisson solver for determining various parasitic

capacitances and a 3D thermal solver for obtaining the self-heating elements. A complete set of model parameters was then generated by a geometry scaling tool. The corresponding final 3D model was employed for generating the device and circuit related figures of merit of the major nodes listed in the ITRS tables.

1.2.2 BIPOLAR / BICMOS TECHNOLOGIES SPECIFICITIES

The years indicated in the bipolar roadmap are not the start of production year but rather the start of prototyping year. The life span of BiCMOS technologies (defined by length of time at a significant production volume) is much longer (~10 years) than that of CMOS technologies. This is because, for a given application, they may not benefit appreciably from simple (critical dimension) scaling. The end result is that BiCMOS technologies are not available for each CMOS node and several years separate two BiCMOS generations (a 4-year plateau is assumed in the roadmap). For these reasons, the roadmap provided here does not attempt to tie bipolar performance to a given CMOS node. CMOS node choice depends on many factors, some of which are company specific: bipolar performance requirements, gate density requirements, process integration compatibility, development time, and cost.

Today, the production-qualified BiCMOS technologies utilizing the HS-NPN offer 180 nm and 130 nm CMOS. This represents a four to five generation technology-node gap between CMOS and BiCMOS technologies. This is explained by the lack of product drivers requiring dense digital functions, the cost advantages of integration on mature CMOS nodes, and the ability to achieve excellent HS-NPN performance at these CMOS nodes. However, 90 nm and 55 nm BiCMOS technologies are under development to address mm-wave SOC applications that cannot be covered by pure CMOS technologies. For comparison, HV-BiCMOS technologies, which include C-BiCMOS, usually lag behind HS-BiCMOS technologies with CMOS nodes ranging between 350 nm and 180 nm today. They tend to cover applications for which large gate densities are usually not required and for which cost is of primary importance.

1.3 GROUP III-V COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

For RF, microwave, millimeter wave and mixed-signal applications, if the performance requirements can be satisfied by silicon and SiGe they will be, primarily for cost and integration density reasons. Therefore, the drivers for continued development of III-V devices are based on applications that require higher frequency, wider bandwidth, higher power, higher gain, higher dynamic range, higher efficiency or lower noise performance than can be achieved with silicon based devices. III-V devices will continue to serve niche or performance driven applications where silicon performance is not adequate. In addition, continued advances in the heterogeneous integration of III-V devices with Si CMOS on silicon substrates will enable the realization of RF and mixed-signal circuits that take advantage of the superior performance of III-V devices and the high integration density of Si CMOS.

1.3.1 MICROWAVE DRIVERS

Wireless communications require both portable and fixed transmitters and receivers to form a connected network. The public is most familiar with portable devices that take the form of cellular telephones and wireless personal digital appliances (PDAs). The III-V devices required to implement these portable devices are InGaP HBTs in power amplifier (PA) modules. GaN HEMT power amplifiers have the potential to enhance the performance of base station transmitters. However, GaN HEMT PAs will have to displace the incumbent mature, low cost Si technology. With the continued advancement in Si power amplifiers and the evolution of cellular networks into micro- and pico-cells, III-V technology has not made the expected inroads into these applications. The key driving forces for these two devices are integration of components and cost.

For portable applications, the PA module is a multichip assembly that contains a Si power management chip, RF matching networks, RF switches, filters, and PA chips capable of supplying 1 - 4 watts of RF power to the antenna. While silicon technology is typically used for power control circuitry and the switch functions, InGaP HBTs are typically used for the power amplifier chips. The trend is to combine several components/functions on the same semiconductor chip. For example, the PA controller function is being combined with the switch function or the PA controller could be integrated with the PA. Even some linear PAs are starting to include a CMOS-assist bias circuit to meet stringent current consumption vs. output power requirements. Combining several different PA module functions on a single chip reduces component count and wire bonding complexity and may lead to lower cost modules. These technology combination approaches will become more prevalent as PA modules are required to service an increased number of frequencies and modulation formats in years to come. The choice of which technology to use for each function depends on the RF performance specifications, die size, availability, and most importantly, total product cost.

Similar drivers exist for microwave transceivers for point-to-point communications systems like LMDS and radar and multifunction systems used for military applications. Microwave transceivers are typically multichip assemblies similar to the PA module in portable devices, and, in the case of radar and multifunction systems used for military applications, multiple transceivers are assembled into a phased array for electronic beam steering. Control functions are realized in silicon, whereas the power and low noise amplifiers have been traditionally realized in GaAs pHEMT, with some systems using either GaAs MHEMT or InP HEMT in the receive chain due to superior noise performance. In recent years the trend has been to higher levels of integration and for some applications with less stringent power or noise requirements the entire transceiver is being realized in SiGe BiCMOS. As GaN HEMT technology matures, GaN HEMTs are providing enhanced system power, bandwidth, and efficiency and thereby are beginning to replace the GaAs pHEMT PAs in these applcations. Because of its good noise performance coupled with its robustness and high dynamic range, GaN may also begin to replace GaAs and/or InP in the receiver chain.

Note: In the tables and chapter, less emphasis has been placed on III-V devices for RF and microwave frequencies. This decision is based on the fact that III-V devices for RF and microwave applications (< 30 GHz) are mature, production devices available at multiple foundries. The main drivers for device improvements for RF and microwave applications are not device performance or scaling, but rather cost, linearity/dynamic range/efficiency, and integration density. Cost and integration density are a function of manufacturing maturity, whereas linearity/dynamic range/efficiency depend on circuit design techniques.

1.3.2 MILLIMETER WAVE DRIVERS

Commercial interest in the mm-wave spectrum has grown steadily over the past decade. Unlike most of the lower frequency spectrum, where silicon based technologies dominate, III-V devices still provide a distinct performance advantage at millimeter wave frequencies and a number of III-V materials and device technologies compete in the applications marketplace. However, recent advancements in Silicon On Insulator (SOI) CMOS technologies have allowed silicon based technologies to enter mm-wave markets e.g. RF switches.

Each of the III-V technologies offers unique tradeoffs in cost, performance, and availability. Currently, III-V devices and integrated circuits are manufactured on three substrate materials: GaAs, InP, and SiC. In the future III-Vs fabricated on large diameter Si wafers may provide more cost effective solutions.

For performance driven applications in which high levels of integration are needed, we expect a continued drive towards heterogeneous integration of III-V and silicon technologies. Such an approach would enable designers to take advantage of the high-frequency performance of the III-Vs and the high-density integration and processing capabilities of silicon. In the future, we may see other III-V compound semiconductors, and even carbon-based semiconductors, including diamond and graphene, being developed for this spectrum.

In this section we present III-V transistor technologies, which are, or are forecast to be, in commercial production. Because this field is rapidly expanding, and because performance is not tied so tightly to lithographic dimensions as are digital integrated circuits, we have purposely omitted projections into the long-term years. III-V semiconductors do not enjoy the long-term heritage of silicon-based devices, nor do they follow Moore's Law. As the mm-wave spectrum markets and products develop and become more of a technology driver, it may be more plausible to carry the roadmap for mm-waves into the long term for future ITRS editions.

The scope of this section includes low noise and power transistors that are based on the following materials and device technologies: GaAs PHEMT, GaAs MHEMT /InP HEMT, GaN HEMT and InP HBT. All device types employ epitaxial layers that are composed of binary, ternary or quaternary compounds derived from column III and V of the periodic chart. There is great diversity in the nature and performance of these devices because device properties are critically dependent on the selection of materials, thickness, and doping in the epitaxial layers that are proprietary to the manufacturer. Trade-offs exist among power, efficiency, breakdown, noise figure *(NF)*, linearity, and other performance parameters. One consequence of these trade-offs is that the "lithography roadmap" is not the only driver for III-V performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit, such as maximum transit or cutoff frequency (f_T) and maximum frequency of oscillation *(f_{MAX})*. Performance trends are driven primarily by a combination of desirable trade-offs and "bandgap engineering" of the epitaxial layers in concert with shrinking lithography.

1.4 PASSIVE ON-CHIP DEVICES

Passive elements are indispensable in analog and RF systems and are used for matching networks, LC tank circuits, attenuators, filters, decoupling capacitors, loads, and more recently, on-die antennas or antenna reflectors. Passive elements can be simply classified into distributed elements including transmission lines, waveguides and antennas, and lumped elements including inductors, transformers, linear and variable capacitors (varactors), and resistors. The distributed circuits take into account the phase shift occurring when the signal wave propagates along circuits. As the operating frequency moves into the microwave and millimeter wave spectrum, distributed passives are used more frequently because they have higher quality factors (Q). On the other hand, lumped elements have physical dimensions which are deemed to be insignificant with respect to the wavelength, typically less than $\lambda/20$, so that phase effects may be ignored. They are typically used at frequencies lower than ~ 30 GHz, but also at microwave and mm-wave frequencies when their physical dimensions are small. The scope of this section focuses primarily on lumped-element passives as on-chip (SoC) components such as:

1) linear capacitors,

2) resistors,

3) inductors, and

4) varactors.

The on-chip lumped passives are used pervasively in applications in the Low Frequency (LF) analog (from direct current (DC) to 0.4 GHz) and Radio Frequency (RF) (from 0.4 GHz to 30 GHz). However, they are sometimes used through the mm-wave and higher frequencies as well. Therefore, some discussion is also given for passives employed in the higher frequency ranges of mm-waves from 30 GHz to 300 GHz.

Because the low frequency analog and mixed-signal applications require uniform and stable linear capacitors and resistors, the roadmap addresses voltage and temperature coefficients and matching as their key parameters. RF and microwave applications (0.4 GHz to 30 GHz) impose the additional requirement for high Q, specifically for inductor and capacitor (L/C) components. The Q limitations of L/C passives integrated on-chip originate primarily from the resistive losses in series connections (metal loss) and the parasitic capacitors in parallel connections (substrate loss). These losses and parasitics are significantly affected by the silicon substrate and, increasingly, by the processing features associated with interconnects, vias, and metal fills and slotting. Further interdependency on properties of interconnects is prominent at the highest frequency range of 30-300 GHz addressed in this section. This high frequency range makes use of distributed passive components, *e.g.* transmission lines. The figure of merits for transmission lines include the loss per unit length and per unit area and are determined mainly by the basic interconnects R-L-C characteristics.

The ITRS Chapters on *Assembly and Packaging* and on *Interconnects* contain sections on passive off-chip devices. This section focuses exclusively on passive on-chip devices and primarily on lumped elements.

2.0 DIFFICULT CHALLENGES

2.1 RF CMOS

It is easy to assume that the steady improvement in the digital performance of the basic devices in the HP and LSTP roadmaps derived from scaling will also result in continuous improvement in RF and analog performance. But in fact, many of the dimensional, materials-oriented, and structural changes being invoked in the digital roadmap degrade or at least alter RF and analog device behavior. For example, it is well know that the halo or pocket implant degrades transistor gain even at long channel lengths. As dimensions shrink, new tradeoffs in physical design optimization for RF performance will be necessary as different mechanisms emerge as limiting factors determining parasitic impedances in local interconnects to the device.

The gate resistance, for the most part ignored in considering the performance of digital circuits, becomes a critical limiter of RF FOMs. Consider the expression for the minimum noise factor of a FET. [8]

RFAMS-EQ (2.1.1) $$F_{MIN} \approx 1 + \frac{2f}{f_{Teff}} \sqrt{k_1} \sqrt{g_m (R_g + R_s) + 1}.$$

Also consider the following expression for maximum frequency of oscillation,[9]

RFAMS-EQ (2.1.2) $$f_{MAX} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g)g_o + 2\pi f_T R_g C_{gd}}}.$$

The conventional definitions of the variables apply; R_i is the intrinsic channel resistance, R_s in the series resistance, R_g is the gate resistance, g_o is the output conductance, g_m in the transconductance, C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitance. High gate resistance reduces f_{MAX} and raises F_{MIN}. For a given device, gate resistance depends on the specific details of the device geometry. For example, assume a gate contacted from two-sides as shown below. Furthermore, assume that the gate is composed of a stack of material(s) that can be characterized by a horizontal sheet resistance, R_{SH}. Then, one can find an optimal channel width, minimizing gate resistance, as follows.

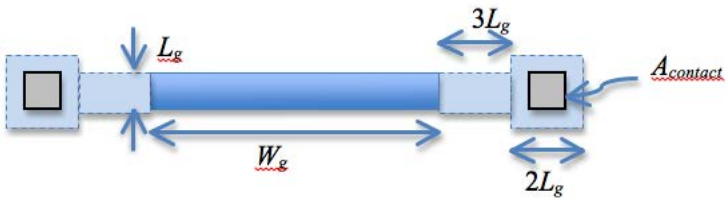

Figure RFAMS2 An Illustration of the Physical Layout of One Gate Finger of a MOSFET

The gate resistance is modeled to have 3 additive components: 1) contact resistance (two in parallel for the structure shown), 2) horizontal resistance of the link between the contact and active gate, and 3) the active gate resistance) as

RFAMS-EQ (2.1.3) $R_{GATE} = R_{CONT} + R_{LINK} + R_{ACTIVE}$.

The contact contribution is given by the via resistivity divided by the contact area. To this is added the resistance of two horizontal links between the contacts and the active gate. The horizontal contribution of the active device is given by the well-known expression for distributed gate resistance contacted on both sides.[10] Here the link regions are assumed to be three gate lengths. This gives the expression,

RFAMS-EQ (2.1.4) $$R_G = \frac{\rho_{via}}{2A_{contact}} + \frac{3}{2}R_{SH} + \frac{R_{SH}W_g}{12L_g}$$

Optimum gate width is generally found empirically, considering effects of parasitic capacitances of a given layout, the FOM one is trying to optimize, and resistances intrinsic to the transistor. For example, considering the term (R_s + R_g) in the expression for F_{MIN}, one could find the optimum gate width as;

RFAMS-EQ (2.1.5) $$W_{g,opt.} = \sqrt{\frac{12L_g R_s'}{R_{SH}}}$$

where R'$_s$ is the source resistance expressed in Ω-m. For estimating the figures of merit (FOMs) presented in the Technology Requirements we used an empirical value of device width based on recent publications and the authors' experience and scaled this in time proportionally with gate length.

Consider next the gate-to-drain and gate-to-source capacitances found in the expressions for f_{MAX} above or for the cutoff frequency,[11]

RFAMS-EQ (2.1.6) $$\frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} + C_{gd}(R_s + R_d) + (C_{gs} + C_{gd})(R_s + R_d)\frac{g_{out}}{g_m}$$

Typical device models capture only the intrinsic transistor capacitances, or in the common practice for high-frequency models, they will capture wiring capacitances of the first or second level of wiring for a specified device layout. This permits a single model to represent the behavior of the device in many wiring configurations but requires that parasitic impedances of the wiring be extracted and included in circuit simulations. This presents a challenge especially for mm-wave designs, which typically wire individual transistors to transmission lines formed on the top metal level.

As reflected in the HP and LSTP roadmaps, fundamental changes in device structures such as the introduction of multiple-gates and/or fully depleted SOI will be required to sustain continued performance and density improvement. These structures prohibit a contact to the device body. Thus, the electrical characteristics of these devices are fundamentally different from those of conventional CMOS. Potential benefits include higher voltage-gain and lower coupling between the drain and body. But these differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries. Thus, the fabrication of conventional precision analog / RF driver devices to be integrated alongside the scaled CMOS devices may require separate process steps. Even now, the impetus to enable system-on-chip (SOC) applications is encouraging the incorporation of optional analog or high-voltage devices and thereby expands the menu of potential devices albeit with the attendant cost increases.

2.2 GROUP IV SILICON BIPOLAR AND BICMOS

The primary challenge for the HS-NPN is increasing the unity current gain cut-off frequency f_T by more aggressive vertical profiles while still maintaining $f_{MAX} > f_T$ i.e. low base resistance (R_B) and low base-collector capacitance (C_{BC}). A number of novel device architectures have been proposed with new self-alignment schemes to improve the $R_B \times C_{BC}$ trade-off. Beyond node N1 in Table RFAMS2, a change to one of these new device architectures is expected in order to meet the f_T/f_{MAX} performance requirements. In addition, BiCMOS compatibility for these structures needs to be proven, as digital content requirements for the highest frequency applications will likely increase over time. The second major challenge facing bipolar devices, in general (including III-V), is the reduction of the emitter width in order to mitigate the increase of peak f_T operating current. With decreasing collector thickness and increased collector doping the peak f_T current density (J_C) is ultimately expected to increase up to 120 mA/μm² in N5. It serves to increase the base-collector junction switching speed (C_{CB}/I_C) but handling this current from both a wiring and a self-heating perspective is increasingly challenging. One way of reducing the total current and power is to reduce the emitter width, which is lithographically not challenging given that current emitter widths are around 0.13 μm, but the obstacle lies in the emitter resistance. Key portions of the emitter resistance are the interface resistances formed at the via-silicide-poly interface and at the emitter poly to mono region, which scales as the inverse emitter area. More generally, the HS-NPN roadmap assumes that all interface and contact resistances could be reduced by half at the end of the roadmap although solutions to meet this objective do not exist yet.

2.3 GROUP III-V COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

III-V compound semiconductor technologies have a number of similarities with silicon technologies and yet in many ways are distinctly different. Among the unique challenges faced by III-V devices are yield (manufacturability), substrate size, thermal management, integration density, DC/RF dispersion (gate/drain lag), dielectric loading, and reliability under high fields. Among the challenges common with Si based circuits are the need to improve efficiency and linearity/dynamic range, particularly for power amplifiers for communications applications.

Unlike silicon based circuits technology, III-V microwave and millimeter wave circuits are typically built on high resistivity or semi-insulating substrates. Semi-insulating GaAs wafers that are 150 mm in diameter are routinely available and are becoming the *de facto* standard, although many foundries still manufacture GaAs ICs on 100 mm diameter wafers. The move to larger diameter substrates will be driven not only by economies of scale and chip cost but also by equipment availability. GaAs tends to be two or more generations behind Si in wafer size, with InP and SiC one generation behind GaAs. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from the advances in processing equipment. Alternately, this can be addressed by fabrication of III-V devices on large diameter silicon wafers. While significant progress has been made in the development of conducting GaN substrates for LED applications, today there is no production source of semi-insulating GaN substrates. For most microwave/millimeter wave (high power) applications GaN device epitaxy relies on SiC for a host substrate and several firms now supply GaN epitaxial layers, tailored to customer specifications, on SiC substrates. Device quality, 100 mm diameter, high resistivity SiC substrates are available from multiple suppliers, with plans to scale to 150 mm diameter substrates based on industry demand. Recently, significant progress has been made on the growth of GaN on Si and device quality GaN epi on 200 mm diameter wafers has been demonstrated. However, this development is being driven by the power conditioning/converter circuit market whose circuits operates in the MHz frequencies and do not require high resistivity substrates. The growth of GaN on Si opens up the possibility of fabricating GaN circuits in a silicon foundry as well as the heterogeneous integration of GaN amplifiers with Si CMOS control circuitry.

Power amplifiers are among the largest uses of III-V devices. Improving amplifier efficiency is a major challenge for III-V power amplifiers for all applications including commercial (e.g, handset and base stations), military (e.g, radar) and

millimeter wave. This is primarily being addressed by exploring more efficient amplifier architectures: Doherty, drain modulation, and higher efficiency classes of operation (Class D, Class F, and Class S). However, the successful design and implementation of these amplifier architecutres does require further improvement in frequency response, gain and efficiency of the basic transistor building block without compromising breakdown or operating voltage. Achieving these improvements are both an advantage and challenge of III-V devices. These high efficiency architectures must also continue to meet the stringent linearity performance requirements and cannot substantially increase system cost. Adaptive digital pre-distortion (DPD) designs where the input signal is pre-distorted in the digital domain to compensate for device non-linearities will help meet the linearity requirements. The adaptive behavior of the pre-distorter also mitigates issues with thermal time constants and device performance drift over time. For example, for base stations, GaN may offer advantages over LDMOS in certain classes of high efficiency architectures. Today, the above linearization techniques are realized in multichip assemblies. Higher levels of integration and/or the heterogeneous integration of III-V devices with Si CMOS control circuitry could offer compact, higher performance, lower cost solutions.

High efficiency architecture deployment represents an opportunity to design devices with attributes that are compatible with the architecture and can further enhance efficiency. For example, a Doherty-friendly device will have peak power and peak efficiency impedances designed to achieve maximum benefit from the load modulation that this architecture relies upon to improve efficiency without sacrificing peak power. The figures-of-merit that drive device development are a function of the PA architecture. Improving such figures of merit may potentially lead to devices that are designed for a specific PA architecture. That is, a device designed for use with a Doherty amplifier may not perform well in an input signal envelope tracking architecture. Understanding these figures-of-merit will enable device manufacturers to further enhance PA efficiency.

Another major challenge facing power amplifier devices and modules for communication and radar is the need to increase their functionality in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity requirements at the same or lower cost. For example, the consumer expects increasing portable device functionality without a substantial increase in portable device cost. Meeting these conflicting requirements is the biggest challenge facing the development of future PA modules. Some examples of recent customer requirements that impact technology choices are listed below.

With the emergence of GSM-EDGE, High Speed Packet Access (HSPA), Long Term Evolution (LTE), and other communications standards, there there will be some convergence of the needs of linear PA and saturated PAs as PA designers must now provide linear operation as well. The proliferation of communications standards has resulted in the increased market share of Multi-Mode, Multi-Band (mm-MB) which may contain GSM-EDGE, LTE, HSPA, additional switching functions, and possibly built-in load-tunability to minimize the number of required amplifiers. With the decrease in average RF transmit power, there is an increasing focus on mid-power (16 dBm) efficiency. One solution includes on-chip switching to by-pass one or all of the PA stages. This on-chip switching drives the integration of RF FETs and HBTs on the same die. More recently, such integration is being extended to have the efficiency measured at multiple power points that increases the complexity of the bias control and switching operations.

PA users are requesting increasingly sophisticated bias circuits. Load matching is a challenge shared by the PA and the antenna. There has beern significant work on adaptive antenna matching that needs to be considered also. Some examples of user requests include: 1) enable pins/mode control, 2) temperature compensation circuitry, 3) automatic bias control in which the PA senses power and resets bias based on the power it senses, and 4) circuits that do not require a reference supply voltage. The above request 3 may require integration of the power detector/coupler into the PA module. Also, using only npn transistors to meet the above request 4 is challenging. In general, meeting the above requests or demands is the driver for BiFET integration where the FET is required to be a high quality analog FET. Continued emphasis on this area also makes BiCMOS, although it has RF shortcomings, an attractive alternative to GaAs HBT. Also, load matching is another challenge that is influenced considerably by the PA and the antenna. Adaptive antenna matching offers additional options for designers.

Another challenge that is presented to all portable applications is the migration of battery technology. The likely near-term decrease in the end-of-life battery voltage presents a major technology and design challenge to PA vendors. This has huge implications for what has to happen at a system level. The PA will still need to work on a 4 V to 5 V charger, but also operate at lower voltages such as 2.4 V. Thereby, the operating range of the PA will increase. If the required output power remains unchanged, then some form of load-line switching will needed. Whether or not the phone manufacturer supplies this or the PA supplier will impact the choice of technology used. Another consequence will be that the transistors used in the power amplifier will be required to operate at a much higher current density to meet the same requirements and this will also have ramifications for which technologies can be used.

The incredible cost sensitivity and the fact that PAs tend to use a system-in-a-package (SIP) approach make the technology trends difficult to forecast.

The challenge facing the adoption of GaN FETs for base station applications is continual product price pressure even though the technology has the potential to offer outstanding advantages compared to Si technology. If GaN can begin to displace Si in base station infractrucutes then production volumes will drive the cost reduction curve will be relatively dramatic just as happened with GaAs and SiGe technologies for handsets.

Additional III-V device challenges include:

1. Reliability of scaled devices, particularly for power applications
2. Techniques for heat removal including wafer thinning and site specific cooling for high power density devices such as GaN;
3. High breakdown voltages for power devices and associated passive components, such as capacitors and thin film resistors;
4. Non-native oxide passivation and dielectric materials for mixed-signal, enhancement/depletion (E/D) mode devices and scaled devices.
5. Reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
6. High yield multilayer interconnects for mixed-signal and increased functionality of PA and transceiver modules including understanding and mitigating impact of dielectric loading on FETs due to multi-layer interconnects/dielectrics
7. Overall yield and uniformity improvements to drive cost
8. Process compatibility with different device and materials technologies integrated in dense multi-chip modules, (particularly, those based on emerging packaging/integration technologies such as Freescales Redistributed Chip Package (RCP) and DRAPER Laboratories integrated Ultra High Desinity (iUHD) technology) and emerging chip-on-chip heterogeneous integration technologies. For example, a 4 mm by 4 mm power amplifier may have a dozen surface mounts, 2 GaAs HBT die, a CMOS controller-bias chip, SAW/BAW filter, and s switch.

2.4 PASSIVE ON-CHIP DEVICES INCLUDING RESISTORS, INDUCTORS, CAPACITORS, AND VARACTORS

The implementation of on-chip passive components required for RF and AMS circuits poses serious challenges to SoC integration of these functions. The processes to form the active transistor devices and the interconnects can be utilized to form passive elements but frequently, dedicated masks and processing steps are required to implement these devices with desirable properties. Thus, the co-integration of active and passive devices introduces process complexity and can lead to manufacturing control challenges.

The parasitic impedances such as capacitance, resistance, and self- or mutual-inductance of interconnects, resistances of the films used to form devices, substrate resistance and losses, and dielectric leakage all limit the performance of passive devices. The impact of these parasitic impedances on the performance of the passive on-chip devices will be captured in the Technology Requirements section.

A key challenge for any semiconductor technology, whether CMOS, BiCMOS, III-V or HVMOS is to implement passive devices required for the intended application at the lowest costs possible. With the exception of the metal-insulator-metal (MIM) capacitor, passive on-chip components can be formed using readily available base layers in the semiconductor process for resistors, MOS capacitors and varactors, and in the interconnect layers for inductors and inter-metal (*a.k.a.* metal-oxide-metal, or MOM) capacitors. If the properties of such devices are not adequate, it may be necessary to introduce added masks and processing to form high-performance passive devices.

There are challenges to providing low-cost and high-quality passive devices that are imposed directly by the scaling of interconnect dimensions. The decreasing thickness of individual metals, as well as the overall stack height, results in increasing resistive losses and vertical parasitic capacitances. This limits the Q of the on-chip integrated inductors, transformers, MIM and inter-metal (MOM) capacitors.

3.0 TECHNOLOGY REQUIREMENTS

We first discuss in this section on technology requirements those figures of merit (FOM) that are common to many RF and AMS technologies.

Extracting reliable FOMs from high-frequency measurements becomes more difficult as device performance levels increase while their resistances increase and capacitances must decrease. For these reasons a sufficient device area is recommended to measure capacitances exceeding 20 fF, which is a lower limit for reliable data. Measurement, de-embedding, and parameter extraction methodologies may have a significant impact on high frequency FOMs. Although some companies use complex procedures to obtain the accuracy required for compact modeling of silicon and SiGe devices, most companies use rather basic techniques to measure and monitor device cut-off frequencies [12,13].

The most common method used both for silicon bipolar and field-effect transistors is a two-dummy (Open + Short) de-embedding technique following a standard [short-open-load-through (SOLT) or line-reflect-reflect-match (LRRM)] impedance substrate standard (ISS) calibration. Even though the layout of these de-embedding structures and the precise de-embedding methodology may vary from one company to the other, the de-embedded device generally must keep the metal lines required to connect its electrodes, i.e., Metal 1 or Metal 1 + Metal 2 levels. This usually yields very repeatable results for the unity current gain *(h21)* cut-off frequency, f_T. For lower performance devices, like high-voltage and p-type devices, single-dummy (Open) de-embedding may be sufficient. In real circuits top metal lines are used to connect the transistors to matching networks and de-embedding the higher level metal wiring stack on top of the transistor, or not using it at all, in RF test structures may lead to an overestimation of device performance in the final circuits. This is especially true for MOS transistors [14], while the impact of de-embedding on bipolar transistor performance is negligible [15]. This highlights the importance of transistor layout optimization for MOS devices for VCOs and power transistors for which largest f_{MAX} and *MAG* values are desired [16]. As a consequence, the direct comparison of HF performance between MOS and bipolar transistors, including using the ITRS tables, must be done with caution since it does not account for the degradation due to the metal wiring stack. The latter strongly depends on the back-end-of-line of the technologies. Circuit designers usually prefer to compare the performance without de-embedding the metal wiring on top of the transistors, as discussed in [13] and [17].

The calibration and de-embedding approach described in the previous paragraph is in general not used for mm-wave III-V devices. For III-V device measurements, a single TRL (thru-reflect-line) calibration using on-wafer calibration standards is preferred. One of the main benefits of this approach is that the pad and interconnect parasitics to the edge of the device under test (DUT) are de-embedded automatically in the calibration step. TRL with on-wafer calibration standards has recently been used by several groups to measure and de-embed silicon devices above 100 GHz [18,19].

The unity power gain maximum frequency of oscillation, f_{MAX}, is extracted and reported from Mason's gain (U) at a given frequency. However, the accuracy of this approach is the subject of much debate as this FOM is highly dependent on the cleanliness of the 20 dB/dec roll-off of U as a function of frequency. A conventional approach to verify f_{MAX} is plotting $f_{MAX} = \text{freq} \times \sqrt{U}$ across a range of frequencies. This allows a reasonable estimate of f_{MAX} if a constant value is obtained over a wide frequency range, while at the same time providing information on measurement error for f_{MAX}.

The accurate extraction of the minimum noise factor, F_{MIN}, (or minimum noise figure, NF_{MIN}, in dB) of a transistor is even more challenging than f_{MAX}. At frequencies through W-band where commercial equipment is available, a source-pull technique is employed whereby the noise figure of the transistor is measured for several carefully selected source impedance states along with the S-parameters of the transistor. After de-embedding, the minimum noise figure and the IEEE noise parameters of the transistor are extrapolated using a least squares fitting algorithm. Since source pull measurements above 50 GHz can be difficult to make and reliably de-embed above 50 GHz, the minimum noise figure of the transistor is usually estimated from the noise figure of a low-noise amplifier or receiver measured for 50-Ohm signal source impedance. Other approaches above 100 GHz include the integration of a source-pull setup on the die. In the case of bipolar transistors, it is possible to extract all IEEE noise parameters only from either S-parameter or Y-parameter measurements [20]. Unfortunately, this much simpler technique is not applicable to FETs [21]. However, we report for III-V devices NFmin at 60 GHz and 94 GHz (from source pull for discrete devices). We report for 94 GHz and above LNA noise figure since source pull is difficult as discussed above.

Another important FOM extracted from the measured and de-embedded S-parameters, and road-mapped at 60 GHz, 94 GHz, 140 GHz and/or 220 GHz for bipolar devices, is the maximum available power gain (*MAG*) of a common-emitter or common-source stage. At frequencies where the transistor is not unconditionally stable, *MAG* reduces to the maximum stable gain (*MSG*). More complex circuit figures of merit such as that of power amplifiers are linked to *MAG*. However, we include for III-V devices large signal gain (at 1dB compression) for PAs and associated gain for low noise.

3.1 RF CMOS

We continue to use the HP and LSTP technologies from the *PIDS* chapter as the basis for millimeter-wave and microwave applications respectively. But, with the 2011 edition, we specifically reflect the three different technology options reflected in the PIDS chapter; Bulk CMOS, Fully-depleted SOI, and multi-gate allowing the user to more readily assess the differences in RF and analog performance resulting from these technology options. Furthermore, using device parameters from the PIDS chapter and film properties reflected in the *Front-end Process (FEP)* and *Integration* chapters, we attempt to reflect the performance limitations resulting from the parasitic impedances of the device structure.

These changes are evident in the roadmap for cutoff frequency (f_T) for the LSTP transistor where closer linkage to the device parameters in the PIDS tables resulted in a significant uplift in the tabulated values in the far term years. The roadmap for maximum frequency of oscillation (f_{MAX}) for both technologies now better reflects the impact of device parameters and parasitic impedances. Its near term value has dropped but it increases over time in a similar fashion compared to the 2009 edition.

In order to reflect requirements for narrow-band and broadband applications discussed in the System Drivers chapter, we provide roadmaps for analog gain at low frequency and maximum stable gain (MSG) and minimum noise figure NF_{MIN} for example application frequencies of 24 GHz for the LSTP technology and 60 GHz for the HP technology. We also tabulate the analog gain for an analog-friendly transistor that is provided as an option by some foundries.

Table RFAMS1 RF CMOS Technology Requirements

3.2 GROUP IV SILICON BIPOLAR AND BICMOS

We discuss in this section FOMs specific to the HS-NPN and the related circuits simulated with the model cards extracted for each node. The peak value of the frequency of unity current gain, f_T, the maximum oscillation frequency, f_{MAX}, and the *MAG* values are indeed common to all bipolar (Si, SiGe and III-V) devices covered by the ITRS RF/AMS chapter.

3.2.1 DEVICE FOM

The bipolar-specific FOMs presented in the table are the emitter-to-collector breakdown voltage BV_{CEO}, the collector-base breakdown voltage BV_{CBO} and the slew rate *SLi*. The effective emitter width W_E is not a FOM but a key feature size of the transistors. The emitter width W_E and the collector current density at peak f_T (J_C), provided for the HS-NPN, determine the current flowing through the transistor, which must be considered to avoid any electromigration issues.

It is important to mention that the extraction of reliable breakdown voltages from simulations is difficult. More specifically, BV_{CBO} values given for the last nodes are optimistic since they are based on the Boltzmann transport equation that does not take into account tunneling currents. Adding band-to-band and trap-assisted tunneling is expected to provide more reliable collector breakdown related information but only if the corresponding tunneling parameters were accurately known. Research effort is required to improve the prediction of breakdown voltages.

The intrinsic slew rate, *SLi* (V/s), is defined as the ratio of the collector current and the output capacitance ($SLi = I_C / (C_{BC} + C_{CS})$; C_{CS} being the collector – substrate capacitance) at peak f_T and is an indicator of the ultimate switching speed of the transistor in high-speed DACs, large-swing 50-Ohm output drivers, and in laser- or optical-modulator drivers. The intrinsic slew rate is related to the delay τ of a chain of identical CML HBT inverters.

Low-frequency (1/*f*) noise and matching numbers are no longer in the table since circuits' requirements are expected to remain constant. Maximum values of 1 µV².µm²/Hz and 2 %.µm are targeted for 1/*f* noise and collector current matching ($\sigma(\Delta I_C/I_C)$), respectively. While meeting this 1/*f* noise target should not be a concern, a degradation of the matching with the reduction of the emitter width is expected. This degradation will likely depend on the choice of the transistor architecture, which is not presumed in the roadmap. Indeed, the ITRS requirements for bipolar transistors could potentially be reached by different transistor architectures just like it is today for the BiCMOS technologies on the market.

The minimum noise figure, NF_{MIN}, is no longer reported for the transistor either since NF_{MIN} values are provided for Low Noise Amplifiers at different operating frequencies.

3.2.2 CIRCUITS FOM

Four different circuits were designed and simulated in each technology node (N1 through N5in Table RFAMS2) using the HICUM Level 2 SiGe HBT model described earlier.

A 31-stage CML Ring Oscillator was simulated using CBEBC HBTs with the emitter widths and lengths presented in the table (L_E / W_E = 10) and an ideal current source for the tail current. The interstage load has been set to 0.1 fF which results in somewhat too optimistic performance, especially for the lower nodes. The minimum values of the delay time τ_{CML} track reasonably well with the inverse of peak f_{MAX}.

Results from three representative circuits for mm-wave applications, a single-transistor LNA, a single-transistor class AB PA and a single-transistor Colpitts oscillator are presented too. A minimal set of ideal (lossless) passive components was included in each type of circuit. The circuits were designed and optimized at representative frequencies for present and future applications: 60 GHz, 94 GHz, 140 GHz and 220 GHz.

For the LNA, the NF_{MIN} and associated gain of a 10× common-emitter HBT, with an emitter length 10 times larger than the minimum emitter width, were determined at the optimal noise figure current density of each node and at each representative frequency. The collector emitter voltage of the HBT was 1.2 V in all cases. Noise correlation was included in the compact model [22]. No matching network was considered. Therefore these values represent best possible LNA performance. In a real circuit, the expected noise figure and gain will be degraded by the finite quality factor of the passive matching networks.

The size of the transistor employed in the power amplifier was 300×, where 30 10× SiGe HBT's were connected in parallel. The composite transistor was biased in class AB at V_{CE} = 1.5 V. This resulted in output power levels in the 11-16 dBm range, depending on the technology node and operation frequency. The ideal input and output matching networks were optimized using the load-pull technique in each technology node and at each application frequency such that the maximum power added efficiency (PAE) was obtained. The corresponding power gain and ouput power per emitter length at maximum PAE are reported in the table.

A single-ended Colpitts topology with ideal capacitors and tank inductor was chosen as the representative oscillator circuit. The circuit was loaded by a 50-Ohm port and a pad capacitance of 20 fF, to capture a realistic application scenario and to allow direct estimation of the output power per emitter length and of the oscillator efficiency (defined as generated output power divided by total DC power). The transistor was biased at a V_{CE} of 1.5 V with a DC emitter voltage of 0.3-0.4 V to allow for suitable Accumulation-Mode MOS (AMOS) varactor control voltage range in VCOs. For each technology node and at each application frequency, the value of the ideal passive components, the total emitter length of the transistor, and the bias current density of the transistor were optimized for the lowest possible phase noise. The output power per emitter length and the oscillator efficiency are reported at the minimum phase noise bias. Since noise correlation was not included in the oscillator simulations, the reported oscillator phase noise performance is rather pessimistic. As the HICUM Level 2 model with noise correlation becomes available in commercial simulators, noise correlation will be included in future editions of the ITRS table for oscillators.

Changes in the 2013 Technology Requirements Tables for bipolar devices are as follows:

1. Dropped the HS-PNP transistor from the table
2. Moved to a HS-NPN roadmap based on simulations
3. Updated the list of HS-NPN FOM (NF_{MIN} removed, *MAG* added at 140 GHz and 220 GHz)
4. Added circuits (RO, LNA, PA, VCO) FOM for HS-NPN
5. Eliminated the year by year scaling of f_T/f_{MAX} ; Inserted 5 performance plateaus corresponding to SiGe HBT performance nodes N1, N2, N3, N4, N5.

Table RFAMS2 RF and Analog Mixed-Signal Bipolar Technology Requirements

3.3 GROUP III-V COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

The changes in the tables are:

1. GaAs pHEMT scaling now stops at 100 nm gate length. In the future GaAs pHEMT technology will be overcome by InP HEMT/GaAs MHEMT and GaN HEMT technologies for millimeter wave noise and power, respectively.
2. InP HEMT and GaAs MHEMT roadmaps have been merged since the technologies provide essentially identical millimeter wave performance and follow the InP HEMT roadmap from 2012.

3. Power MHEMT based on reducing channel In contect has been eliminate for microwave and millimeter wave applications. Power MHEMT will be overcome by rapidly maturing GaN HEMT technology which offers significantly higher power densities for comparable gain and efficiency.
4. Significant updates/modifications were made to the GaN tables for millimeter wave applications, in part to correct for overstatement of performance found in the 2012 tables. GaN metrics are also extended to the 20 nm node.
5. InP HBT and SiGe FOMs were better aligned to facilitate technology trade-off comparisons. This includes addition of MSG at 60 GHz and 94 GHz, NFmin at 60 GHz, and slew rate (SLi – same definition as in section 3.2.1 Silicon Bipolar and BiCMOS Device FOM) for the InP HBT. High speed Si (SiGe) NPN bipolar and InP HBTs gain and noise metrics are quoted for an RF reference plane set at the first global interconnect level which is sufficient to ensure reliable device operation. InGaP HBTs for cell phone power amplifiers were added to the table. Metric are similar to the InP HBT metrics with MSG reported at frequencies of interest to the cell phone industry.

III-V devices are produced at relatively low volumes when compared silicon devices. This is especially true for scaled III-V devices (gate length < 100 nm) where wafer volumes can be quite small due to limited or highly specialized applications. In this regard, the values in the ITRS tables represent device/fabrication processes that demonstrate the capability to produce components (devices/circuits) in a production representative environment that includes availability of production 'released' fabrication processes, a design kit with robust device models, and device reliability data.

In addition to f_T and f_{MAX}, the III-V tables show a projection of key parameters intrinsic to the device, such as breakdown voltage, maximum current, and transconductance, as well as performance factors for low noise and power transistors at fixed frequencies, namely, noise, power, gain, and efficiency. We present predicted performance data at five frequencies of interest across the 10 GHz to 300 GHz frequency spectrum: 24 GHz, 60 GHz, 94 GHz, 140 GHz and 220 GHz. For low noise devices we use F_{min} and Associated Gain, both in dB, as the figures of merits below 100 GHz. For frequencies above 100 GHz in the table (i.e., 140 GHz and 220 GHz), device F_{min} measurements are not readily available as it is difficult to provide the optimum impedance ("Gamma opt") in a source pull measurement as input impedances become low. The noise figure *(NF*), in dB, of a single stage low noise amplifier MMIC (with 50 ohm matching at the input of the MMIC) is used in the table as a substitute for device F_{min}. (FET gate periphery at these frequencies is 2 x 25 micrometers). We note that when the small signal gain of a technology is high at a given frequency, the noise figure of a single stage MMIC will be similar to the noise figure of a multi-stage MMIC. Both device F_{min} and single stage MMIC *NF* are provided at 94 GHz to provide the reader with the expected relationship between the two parameters. For power devices simultaneous Output Power, Large Signal Gain (at 1dB compression), and Efficiency of a single stage power amplifier at each frequency are used as the FOM.

In comparison to Si CMOS, scaling of III-V devices, particularly for RF applications, presents a challenge. For example, in addition to improving transistor speed, gain (or frequency), the device engineer must simultaneously optimize the device for higher breakdown or operating voltages which are requisite for power and high dynamic range applications. In addition to geometry scaling, the device designer has an additional degree of freedom in device optimization, epi engineering – tailoring of device layers to support high breakdown fields and high mobility/saturation velocity. The III-V devices in this chapter are all formed with epitaxial layers (and not ion implantation). This has numerous advantages as well as challenges. Advantages include quantum well structures to enhance channel transport properties, barriers layers for channel confinement and heavily doped cap layers to minimize sources and drain parasitics. Challenges include: non-planar device structures and the use of recess technology to tailor electric fields in the vicinity of the gate electrode. In addition III-V FETs typically use T or mushroom shaped gates to reduce gate resistance.

Breakdown voltage is determined by a combination of material properties and gate recess geometry and, in general, material systems with better channel transport properties sacrifice breakdown voltage. For example InP HEMTs offer better high frequency performance (due to high In content InGaAs channels), where as GaAs pHEMTs offer better breakdown characteristics (lower In content). The GaN HEMT system offers superior breakdown characteristics with transport properties comparable to GaAs pHEMTs. For a given material system there is a tradeoff between high frequency and high voltage performance.

To first order the Johnson Figure of Merit (JFOM = v_{sat} * breakdown field) is independent of gate length for a given material system varying only slightly with gate length/device scaling. GaAs pHEMT, GaAs MHEMT, InP HEMT have similar values (related to the tradeoff of breakdown voltage and channel In content or saturation velocity) whereas GaN HEMTs JFOM is 10X higher due primarily to the larger breakdown field.

To first order f_T scales with channel composition and gate length, predominately due to the increase in transconductance. Gate-source capacitance, C_{GS}, the other parameter that directly impacts f_T, to first order, is invariant with gate length, primarily due to the fact that the reduction in capacitance due to shorter gate lengths is offset by the smaller gate-channel spacing required to eliminate short channel effects and the higher channel charge used to increase transconductance.

F_{max} exhibits a more complex behavior with scaling due to the additional R and C terms that provide multiple additional variables for device optimization. For example, the same gate recess that is used to tailor the electric field at the gate edge optimizes gate-drain capacitance, C_{GD}. Both C_{GD} and breakdown voltage increase with increasing drain side recess dimension. Thus f_{max} decreases with increasing breakdown voltage resulting in a compromise between high frequency performance and high voltage operation. While R_G is expected to increase with decreasing gate length, this increase is offset by the use of T-shaped gates, however, at the expense of increased C_{GD} due to the gate T-top overhang as well as the added fabrication process complexity. The same holds true for field plates, commonly used in GaN HEMTs to tailor the electric field on the drain side of the gate. In addition to enhancing breakdown voltage, the field plate structures also surpresses DC/RF dispersion (or current collapse). The challenge, particularly for millimetwr wave GaN devices, is to optimize the field plate structure without significantly degrading the high frequency performance due to the increased parasitic gate-drain capacitance. Regardless, compared to Si based devices, III-V devices collectively provide superior high frequency performance due to superior material transport properties.

Due to the multiple degrees of freedom in the optimization of III-V devices the FOM values for a given material system and gate length will vary from foundry to foundry. Therefore, the values in the tables are meant as trends and not as absolutes and where chosen to be consistent between different device types.

The 24 GHz spectrum is being positioned for wireless LAN applications. The 60 GHz frequencies, long used by the military for secure satellite cross links, falls in a region where atmospheric absorption is high, and as a consequence is ideal for short range, "last mile" connectivity in congested areas, where the short range facilitates frequency re-use. Within the scope of this roadmap, we expect to see applications opening at 94 GHz, 140 GHz and 220 GHz, such as point to point communication, concealed weapons detection and imaging all weather aircraft landing systems. The spectrum from 100 GHz to 1000 GHz holds promise for many applications in the areas of medical imaging, spectroscopy, and security. The III-V Technology Requirements Section summarizes the diverse technology choices for the frequencies, 24 GHz, 60 GHz, 94 GHz, 140 GHz and 220 GHz.

While in past years, a review of the tables used to show that no one material or device technology had the monopoly at any frequency (the user had many choices), this trend may no longer be true. Even though InP and GaAs technology will continue to play a role, especially for applications that require ultra low noise (InP HEMT or GaAs MHEMT) or low power consumption (InGaP HBTs for portable electronics) or ultra high frequency (InP HBTs), GaN technology will become more dominant as it matures, especially for power amplifiers even at millimeter wave frequencies. GaN is also attractive for robust, high dynamic range low noise amplifers Ultimately the technology choice for a given application will be driven by many factors, not the least of which is cost. Other factors are integration level, reliability heritage, operating voltage, and of course, performance, which is the focus of the roadmap. We have, however, made implicit predictions regarding the obsolescence and preferences for certain technologies. These predictions are implied by the "white space" (absence of parameters) in the out years for a particular technology. The general trends are summarized below:

- All FET technology metrics are based on depletion mode transistors. While enhancement mode transistor development is under way it is either for integration with depletion mode devices to create E/D mode logic for digital applications or for power electronics applications, both of which are beyond the current scope of this chapter.
- III-V power devices fall into two regions: low power (a few to tens of watts) provided by GaAs PHEMT and InP HEMT/GaAs MHEMT, and high power (tens to hundreds of watts) dominated by GaN.
- III-V MESFETs are not included in the tables. Although GaAs MESFETs may stil play a role in applications under 10 GHz, there is no development work in this technology nor do we see new designs forthcoming due to superior performance along with cost and reliability parity of GaAs PHEMT technologies.
- GaAs pHEMTs will slowly be retired from the table as the technology will not be scaled beyond 100nm and there are no known plans to use GaAs pHEMTs at or above 94 GHz. While GaAs pHEMTs are currently offered as foundry processes (L_G = 500, 250, 150, and 100 nm) and will continue to be used into the foreseeable future, GaAs PHEMTs will eventually be replaced by InP HEMTs/GaAs MHEMTs for emerging high frequency applications and more importantly by GaN for power and high frequency applications due its superior power performance.
- InP HEMT and GaAs Metamorphic technologies (MHEMT devices) offer essentially the same RF performance and were combined into a single roadmap. Low noise InP HEMT/GaAs MHEMT technology continues to scale towards

shorter gate lengths for mm-wave applications, and we see this trend continuing to the 25 nm node. The use of pseudomorphic, composite InGaAs/InAs channels in InP HEMTs has been shown to offer electron mobility enhancement relative to an equivalent random alloy channel.[23] The table for InP HEMT / GaAs MHEMT shows increasing indium mole fraction in the channel as gate lengths scale to 70nm, 50nm, 35nm, and 25nm in future years. The listed indium mole fraction values should be viewed as equivalent alloy compositions for composite InGaAs/InAs channels.

- While we have included continued scaling of Power InP HEMT/GaAs MHEMT technology applications will be limited and we expect that scaling may actually stop at 50 nm. Since breakdown voltages are compromised at shorter gate lengths and higher In-mole fractions, the power InP HEMT/GaAs MHEMT will give way to GaN HEMTs by the end of the decade.
- The III-V device community has continued to focus significant effort on the performance and maturation of GaN HEMT devices, particularly for millimeter-wave transmitters. Device operating frequencies have increased significantly, with f_T and f_{MAX} from highly scaled devices reaching frequencies above 350 GHz and 500 GHz, respectively. The Johnson figure of merit for these devices (~f_T * breakdown voltage) is in the 5 THz-V range for existing millimeter-wave device technologies. Recent device research features have included regrown ohmic contacts enabling 0.1 ohm-mm source and drain contact resistances, enhancement and depletion mode operation on the same wafer, self-aligned gate processes, incorporation of InAlN barrier layers, and gate lengths below 50nm. W-band (94 GHz) GaN MMICs have been demonstrated by multiple organizations with power output levels roughly 5x greater than InP HEMT and GaAs pHEMT MMICs at in this frequency range.
- Microwave GaN is in production at multiple foundries and is not included in the tables. The main performance driver for GaN for microwave frequencies is cost, efficiency and linearity. In addition, for both commercial and military applications linearity and efficiency is driven by circuit design. For 10GHz – 50 GHz applications, users will adopt 150 nm GaN technology to provide gain at the harmonics required for high efficiency switching mode operation. 150 nm GaN is now in production in multiple foundries.
- GaN is emerging as a leading technology for millimeter wave solid state applications. In the tables, formula-based projections are made for the next anticipated 4 generations of GaN HFET gate length scaling from 120 to 20 nm. Continued geometry (gate length) scaling is projected to provide increased gain and efficiency reguired for millimeter wave applications extending to 220 GHz and beyond. However, as with all semiconductor technologies, improved high frequency performance or gain comes at the expense of breakdown (and operating) voltage and as a result output power density decreases. Nevertheless, GaN still provides >5X the outpower density of competing III-V and Si technologies and will become the dominate power amplifer technology in this frequency range. Note: GaN HEMTs, like all FETs are surface sensitivie devices and suffer from DC/RF dispersion. The projected power performance improvements within each node or gate length are based on reduction in DC/RF dispersion as the node matures.
- GaN may also have a niche in the low noise area for applications requiring high robustness and linearity. GaN noise measure is comparable to GaAs PHEMT, and because limiters can be eliminated from the front end of receivers, GaN devices will offer distinct advantages in system noise figure. Low noise amplifiers in GaN HEMT technology have demonstrated wide bandwidth, high linearity, and competitive noise figure at frequencies ranging from 1 to 24 GHz and with scaling will prove to be viable as low noise devices well into the millimeter wave range. RF Receivers using GaN HEMT LNAs are under development for applications requiring high dynamic range or co-location with high power transmitters. Improved device operating frequencies have led to improved gain over wide bandwidths and reduced noise figure
- While InP HBTs offer superior high frequency performance, they will compete with SiGe HBTs for mixed-signal applications. For large volume applications SiGe BiCMOS offers clear cost and integration level advantages, while for equivalent lithography, InP may offer up to 4X improvement in performance. Alternatively, InP HBTs offer 3-4X higher breakdown voltage for the same cut-off frequency and may be a good solution for analog and power circuits at the upper end of the mmWave frequencies and the emerging sub-mmWave frequencies. For low to moderate volume low noise, mmW power and mixed-signal applications III-V solutions will beat SiGe HBT (BiCMOS) due to high BiCMOS NREs.
- For the InP HBT perfromance metrics the RF reference plane set at the first global interconnect level which is sufficient to ensure reliable device operation. F_{MAX} and maximum available gain values derived from the envelope of MAG and MSG. The MAG/MSG values were taken at peak Je for a device with a 3um long emitter length. BV_{CEO} is specified at the maximum VCE for an IC leakage of 10 uA/um2. NF_{MIN} is specified at the optimal DC bias and source impedance. In the future, may want to weight NF higher in our scaling studies (beta, RB/CBC balance).

- InGaP HBTs are included in the table. Development is primarily focused on driving cost, increasing integration density and improving efficiency and linearity (which are circuit driven), and less on scaling the emitter width.

Table RFAMS3 Group III-V Compound Semiconductor FET and Bipolar Transistors Technology Requirements

3.4 PASSIVE ON-CHIP DEVICES

Passive on-chip devices Technology Requirements tables have been reviewed and updated for MOS capacitors, polysilicon resistors, metal-insulator-metal (MIM) capacitors and inter-metal (MOM) capacitors. Other entries in the table remain the same as the 2011 table. These updates reflect the pace at which the requirements for passives are evolving and the limited participation of subject-area experts in this committee (3 committee members in 2013). Future work will attempt to more closely tie the performance of relevant passive devices to the *Interconnect* roadmap and to define application requirements that passive devices formed in any technology must meet.

3.4.1 INDUCTOR

The inductor is one of the most critical elements in RF and microwave circuits for high-frequency wireless applications. If the Q is too low, the lumped circuit will not reach the desired performance targets. Spiral inductors providing a high Q and inductance value are commonly in demand for wireless SoCs/RFICs. The important characteristics of an inductor are its inductance value and its parasitic capacitance and resistance that determine its Q and self-resonant frequency (SRF). The inductance value is determined, in the first order approximation, by the average diameter of the spiral loop and does not scale with conventional interconnect scaling. The losses in a SoC inductor are given by the sum of three components: 1) the DC resistance of the inductor, 2) the resistance due to skin effect in the conductive trace, and 3) the resistance due to eddy current excitation in the substrate and dielectric losses. Achieving a predetermined inductance at a small resistance *R* contributes to an increase in the Q. The DC resistance tends to increase with the scaling of interconnects. Even though the better conductors allow somewhat lower DC resistance, the AC resistance becomes higher. Typically, SoC inductors make use of the thick top metal layer(s) and/or a dedicated ultra-thick metal layer provided for this purpose, and potentially aluminum thick layer, to circumvent the trend of local interconnects scaling in resistance-critical applications.

When self-resonance occurs, the inductive reactance and the parasitic capacitive reactance become equal. For frequencies greater than the self-resonant frequency, the inductor becomes capacitive and loses its inductive property. The SRF of an inductor should be much higher than its operating frequency. To increase the SRF, the parasitic capacitance C of an inductor to the silicon substrate has to be suppressed. Parasitic capacitance of an inductor is determined by its area that gets smaller for smaller value inductors required for higher frequencies, and by the dielectric/semiconductor stack below the inductor. The dielectric portion of the parasitic capacitance increases with the interconnect scaling due to lower stack height, which is one more reason to provide an additional metal layer higher in the stack (with a thicker separation from the conductor layers below).
The maximum diameter of an inductor should be less than $\lambda/30$ in order to avoid distributed effects. Higher frequency applications require smaller size and higher self-resonant frequency inductors. As a result, the inductance density also becomes more and more important. Therefore, a major design goal for inductor components is to increase the Q by minimizing series resistive losses, increasing the density of inductance and increasing the self-resonant frequency by minimizing parasitic parallel capacitance. All three of these are in contradiction with interconnect scaling. Such a situation is typically resolved by additional (dedicated) thick metal layer(s) that remains largely independent of the interconnect scaling rules. Another popular method is post-integration of microelectromechanical system (MEMS) inductors, which offer higher Qs, but incur additional costs.

3.4.2 CAPACITOR

There are two types of linear capacitors generally used in SoC RF and microwave circuits: 1) interdigitated/inter-metal (*a.k.a.* metal-oxide-metal or MOM) and 2) metal-insulator-metal (MIM). The choice between the inter-metal and MIM capacitors depends mainly on the capacitance. Traditionally, interdigitated capacitors were only used to realize capacitance values up to a few pico Farads (pF), and for larger capacitance values MIM structures were generally used to minimize the overall physical size and avoid the distributed effects. However, this trend is changing, as explained later, because of the constant increase in the MOM capacitance density in scaled CMOS technology nodes. For capacitance values greater than 200 pF or so, die area becomes prohibitive and therefore MOS capacitors or off-chip capacitors are necessary. Nonetheless, MOS capacitors are nonlinear and also have high-frequency limitations due to their higher equivalent series resistance (ESR).

Capacitor performance is strongly associated with the Q and parasitic equivalent series resistance (ESR) and parasitic quivalent series inductance (ESL) of the capacitor. Resistive losses and the parasitic ESR and ESL are caused by the connections to the capacitor electrodes. To achieve a high Q, it is essential to reduce the conducting loss in the wiring and electrodes and to use dielectric materials with small loss-tangents.

To increase high-frequency performance and the passive circuit density and reduce the cost, a large capacitance density is highly desirable. Silicon oxide and nitride are commonly used in conventional MIM capacitors. They can provide good voltage linearity and low-temperature coefficients. But, their capacitance density will be limited by their low dielectric permittivity. Attempts to increase the capacitance density by reducing the dielectric thickness usually cause an undesired high leakage current and poor loss-tangent. Therefore, high-k dielectric materials are used to provide good electrical performances and increase the circuit density.

MIM capacitor is a vertical device created by two special metal plates with thin high-k dielectric insulator layer in between; hence, the capacitance density does not scale with the technology feature size. On the other hand, the technology scaling trend in deep sub-micron CMOS (<< 100 nm) indicates that due to increasingly smaller metal pitch and hence smaller horizontal spacing between interdigitated metal fingers, the inter-metal (MOM) capacitance density increases as the technology node shrinks, and as such the MOM density has already surpassed the MIM capacitance density. The MOM capacitance density is expected to triple in about 10 years. Also unlike their MIM counterparts, the inter-metal capacitors do not require any special dielectric or extra processing steps. Therefore, going forward higher Q remains the main niche area for the paid MIM option in special analog or RF applications. It should be noted that some foundries have started to offer high-density MIM capacitor options to catch up with the MOM alternative.

3.4.3 VARACTOR

A varactor is a variable capacitor for which the capacitance varies as a function of the control voltage applied between its terminals. It is employed to realize tunable oscillators, filters, phase shifters, and the like. The figures of merit that describe the performance of a varactor at high frequency are:

1) Capacitance tuning range or ratio C_{MAX}/C_{MIN},
2) Q over the entire range of control voltages, and
3) Linearity of the tuning characteristics: dC/dV.

It is always desirable to have a high Q, a capacitance ratio that is typically greater than 2, and very linear tuning characteristics. The variable capacitance is usually obtained by modulating the depletion region width of a reverse-biased pn junction or of a MOS capacitor.

Three types of varactor structures are typically encountered in silicon integrated circuits:

1) pn junctions implemented in the base-collector (BC) region of an HBT or in the source/drain-substrate junction of a MOSFET,
2) Accumulation-mode n-well MOS (AMOS) varactors formed using an n-channel MOS device placed in an n-well (rather than in a p-well) to benefit from reduced channel resistance in accumulation mode (as opposed to the inversion mode channel resistance in a MOS transistor) and maximize the quality factor, especially at mm-wave frequencies,
3) Hyper-abrupt pn or Schottky varactors, which require a special implant and exhibit the highest capacitance ratio but are only available in specialized processes.

During the last decade, due to the proliferation of nanoscale CMOS technologies, the AMOS varactor has become the most popular variable capacitance device. Note that the AMOS varactor comes for free in a conventional CMOS process. Typical varactor capacitance values range from a few fF to tens of pF. The varactor Q is inversely proportional to frequency, and is determined by the series resistance loss and the reactance of the variable capacitor.

3.4.4 RESISTOR

Integrated resistors can be produced either by using thin films of lossy metal on a dielectric substrate (such as inter-metal dielectrics (IMD) in the interconnects), or by reusing the transistor gate such as poly or metal in the high-k integation schemes. Nichrome (typically is NiCr but may also contain iron Fe) and tantalum nitride (TaN) are the most popular film materials for thin-film resistors. SiCr and poly-silicon thin films are also used for thin-film resistors. TaN is preferred to NiCr for RF applications because the presence of undesirable magnetic material, i.e., nickel, in NiCr, may introduce unwanted intermodulation products in multi-carrier wireless systems. In addition, TaN is relatively readily available in Cu-based interconnects. NiCr and TaN are commonly used in III-Vs as well. A common problem with planar film resistors is the parasitic capacitance arising from the underlying dielectric region and the distributed inductance. These parasitics have frequency dependence at high frequencies. Shortening the resistor length by introducing films with larger sheet resistivities is helpful for suppressing these parasitics. Desirable characteristics of resistors can be summarized as:

1) Resistance values that do not change with time,
2) Low temperature coefficient of resistance (*TCR*),
3) Large sheet resistivity (kΩ/square or higher) to minimize the parasitics and to guarantee that the resistor length is less than 0.1 λ so that distributed effects may be ignored, and
4) Adequate power dissipation capability

The required tolerances for passive components are roughly summarized in Figure RFAMS3. Analog and RF applications typically necessitate small tolerances of less than ±5%, as well as good matching between the passive elements, and high performance characteristics such as high Q factors and high self-resonance frequency.

Application / Element / Values / Typical Required Tolerance

Damping/ Resistor / (10-50 Ω)/ ±30%
Bypass/ Capacitor/ (20 pF-1 μF)/ ±30%
Pull-up, Pull-down/ Resistor/ (500-1 MΩ)/ ±10%
Integral calculus circuit/ Capacitor / (100 pF-1 μF)/ ±15%
Differential circuit/ Capacitor (10 pF-10 μF)/ ±5%
Oscillator circuit/ Capacitor (1 pF-10 μF)/ ±5%
Bias circuit/ Resistor/ (1 k-10 MΩ)/ ±1%
IC controlling/ Resistor/ (>10 kΩ)/ ±1%
Filter Capacitor/ (< 1 μF) and Inductor (< 100 nH)/ both ±5%
Impedance matching/ Resistor/ (50-100 Ω)/ Capacitor/ (< 10 nF)/ and Inductor/ (< 100 nH)/ all ±5%

Figure RFAMS3 Required Tolerances depending on the application

3.4.5 MILLIMETER-WAVE PASSIVE ON-CHIP DEVICES

The mm-wave passive on-chip devices include capacitors, resistors, inductors, varactors, transmission lines, antennas and antenna resonators. As in the RF range discussed previously, lumped inductors, transformers, MIM/MOM capacitors, pn junction and AMOS n-well varactors continue to play significant roles in minimizing the area occupied by LNAs, PAs, phase shifters, VCOs, and mixers in emerging silicon SoCs. Successful applications of all these components have been demonstrated in CMOS and SiGe BiCMOS circuits operating up to at least 170 GHz in both "RF" and "standard digital" backends, as well as III-V circuits. However, a concerted effort is needed from foundries to provide mm-wave friendly inductor/transformer and capacitor values in 10 pH to 100 pH and 5 fF to 100 fF ranges, respectively. For transformers, close lateral and vertical spacings (fine pitch) between the top two metal layers are needed to achieve large coupling coefficients (k) in 0.8 to 0.9 range. A thick-metal, thick-dielectric "RF" back-end also benefits high-quality passives in the mm-wave regime. Because the skin depth (δ) decreases with increasing frequencies ($\delta \approx 1/\sqrt{f}$,) one-micrometer thick metals are often sufficient for many applications at 60 GHz and above. In contrast, thick dielectrics are even more important at mm-wave than at RF frequencies in reducing parasitic capacitance and substrate losses. Special to mm-wave circuits is the much more common use of transmission lines as matching elements because of reduced wavelengths. Transmission lines are typically implemented in silicon circuits as microstrip lines in the top metal, with the ground plane placed above the silicon substrate and formed in the first 2-5 lower-level metals, often shunted together to reduce loss. Grounded coplanar waveguides with the ground plane above the silicon substrate and coplanar waveguides directly over the silicon substrate have also been employed. Sometimes, especially in "standard" backends, "slow-wave" transmission lines, employing lower-level metal floating bars perpendicular to the signal flow have been employed to increase inductance per area and minimize loss and the area occupied by matching elements. Increasingly, at frequencies above 100 GHz and in thick-metal back-ends, it has become feasible to integrate antennas or antenna resonators with the overall antenna efficiencies now exceeding 50% [24-26]. Note that transmission lines and antennas are not covered in the present On-Chip Passives table and should be considered in future updates.

Table RFAMS4 Passive on-Chip Technology Requirements

4.0 POTENTIAL SOLUTIONS

4.1 RF CMOS

We propose potential solutions for reducing gate resistance, reducing parasitic capacitances, improved high frequency models, and cite the need for reducing device series resistances and output conductance.

The gate resistance is a significant limiter of f_{MAX} and NF_{MIN}. Reducing the interfacial resistivity between the various films composing the gate will help reduce the overall gate resistance. Forming the gate from a single metal layer would

eliminate interfaces. Structural solutions like strapping the gate with overlying metal or forming a T-gate structure employed in III-V technologies would provide significant reduction in gate resistance.

The parasitic capacitances associated with connecting a multi-fingered device to transmission lines formed in the upper layers of the wiring stack, are a significant limiter to f_{MAX} and MSG. Increasing the size of the device and thereby increasing the spacing between wires will decrease the wiring capacitance, but this must be optimized with the increased resistances and junction capacitance that would result.

It is a typical foundry practice to provide device models that reflect the device behavior of the transistor plus wiring up to the first or second metal level leaving the connections to higher metal levels to the designers' discretion. While this allows for flexibility in design it requires the designer to extract the parasitic impedance of the full wiring stack in order to get an accurate simulation of circuit performance. A model reflecting a complete wiring stack or a method for locally extracting parasitic impedances would improve the accuracy of circuit simulations early in the design phase.

Device series resistances and transistor output conductance also limit transistor performance. Innovation in the digital device structure would be necessary to reduce these.

4.2 GROUP IV SILICON BIPOLAR AND BiCMOS

Potential solutions for continuing to improve the f_{MAX} of HS-NPN include lithography advancements that help drive lateral device scaling to reduce parasitic device resistances and capacitances. This enables narrower emitter widths for reduced base resistance (R_B), as well as reduces the unit length current at peak f_T. The improved f_{MAX} and reduced unit length current at peak f_T can be traded-off for more aggressive vertical profiles (thinner base width and higher collector doping concentration) to drive increase of f_T while remaining within reliability limits for current handling in the metal interconnects. The improved f_T and f_{MAX} will also improve the noise figure at high frequency to address mm-wave requirements.

Control of the vertical profile may limit this approach. The Chemical Vapor Deposition (CVD) technique does not appear as a showstopper since the control of the doping profile, including the collector, is today not limited by the control of the deposited thickness but by the dopants diffusion due to the subsequent thermal budget. Continuous improvements are therefore expected both in CVD concerning process uniformity and repeatability, and in metrology for the in-line control of the deposited layers (thicknesses and dopant concentrations). The associated challenges are bigger for selective epitaxial growth (SEG) than for non-selective epitaxial growth (NSEG). Potential solutions to better control the vertical profile include the reduction of the process thermal budget by leveraging advanced CMOS solutions, such as spike or flash anneals, laser annealing, and reduced thermal budget silicide modules [27].

Parasitic losses can significantly limit performance gains. Scaling of the intrinsic collector doping and extrinsic base doping profiles to drive f_T and R_B (f_{MAX}) improvements leads to continued pressure on the R_B–C_{BC} trade-off. Research and development of more advanced structures, which transition from emitter-base self-alignment to emitter-base and base-collector self-alignment has led to the reporting of several innovative architectures. These structures further minimize the interaction between the extrinsic and intrinsic regions of devices, helping to reduce the B-C junction area [28]. It is expected that continued development and improvement of these (and potentially other) architectures will enable scaling of f_{MAX} in accordance with the roadmap.

Concerning the issue of the emitter resistance increase with the reduction of the emitter width (W_E), no breakthrough is foreseen today. Continuous improvements to reduce the specific emitter resistance are required both on emitter deposition process and on transistor architecture. BiCMOS technologies will also benefit from improvements in CMOS technologies such as the expected reduction in silicide and contact resistances [29], which remains a major challenge.

W_E reduction is also driven by the requirements to reduce power consumption and to maintain a $W_E \times J_C$ (J_C being the collector current density at peak f_T) compatible with the electromigration capability of the metallization (including contact). Although BiCMOS technologies will have to deal with the improvements foreseen in CMOS technologies to this respect, special care to the wiring of the transistors will be required. To some extent metallization design rules, coming from core CMOS, could be adapted to the bipolar transistors.

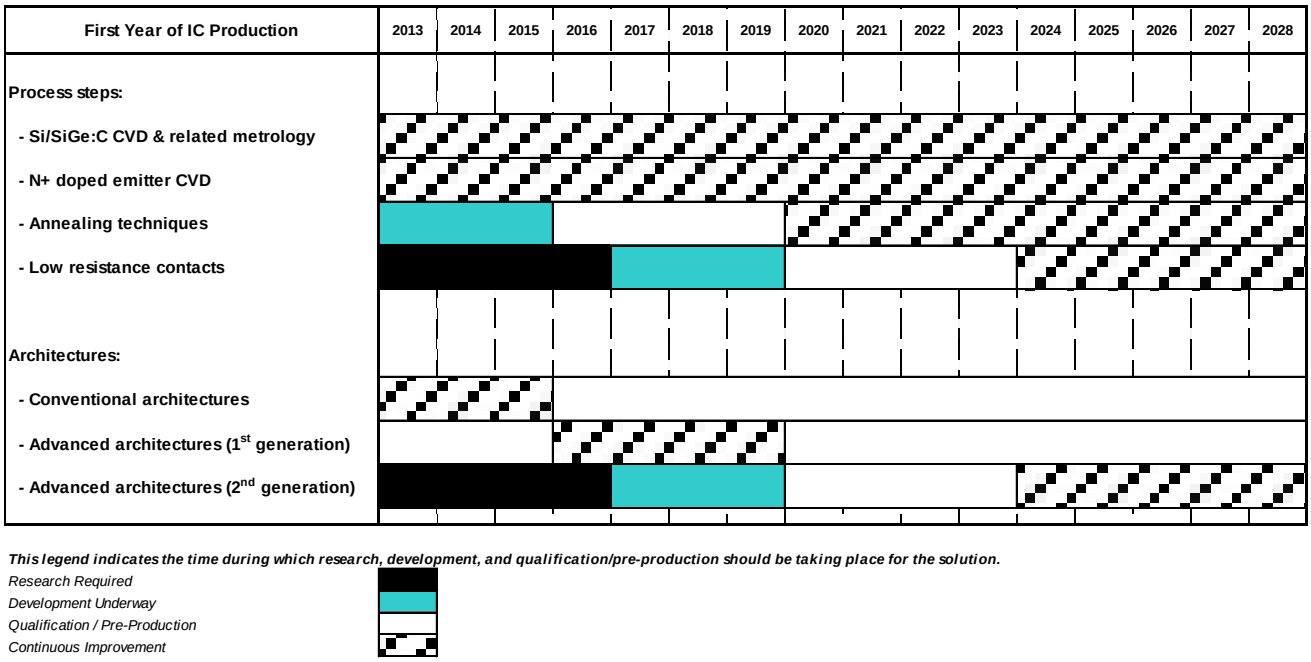

Figure RFAMS4 High-Speed SiGe BiCMOS Potential Solutions

4.3 GROUP III-V COMPOUND SEMICONDUCTORS CONSISTING OF ELEMENTS FROM GROUPS III AND V [BOTH BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]

In the past, compound semiconductors have taken advantage of the advances in lithography and processing equipment that are available in the silicon industry. In order to continue to accomplish this, wafer diameters need to be within one or two generations of the silicon industry. However, the lower volumes/demand for III-V devices does not always justify the investment required to scale III-V substrates. Today, 150 mm diameter, semi-insulating GaAs substrates are in production (although many III-V foundries still operate at 100 mm). InP substrates are available at 100 mm with 150 mm emerging based on demand. Silicon carbide semi-insulating substrates, the basis for GaN HEMTs for RF applications, are also at 100 mm with plans to scale to 150 mm, pending demand. Therefore III-V technology appears to be 2 – 3 generations behind Si that is pushing towards 450 mm diameter substrates for future nodes. Thus, the gap between III-V and Si fab infrastructures may actually be widening.

A potential solution may lie in fabricating III-V devices on silicon substrates and ultimately fabricating III-V devices in silicon foundries. For example, recent advances in the epitaxial growth of GaN on silicon has shown that the growth of device quality GaN HEMTs epitaxy on 200 mm diameter substrates is feasible,[30] opening up the possibility of fabricating GaN HEMTs in an existing 200 mm Si foundry for a more cost effective solution. It should be noted that the GaN on Si development is being driven by the power conversion/conditioning industry (i.e., switching transistors) whose circuits operate at 10's of MHz rather than the 10's of GHz of the RF industry and, as a result, substrate resistivity/loss is less important. Nonetheless, with continued advancements in epitaxial growth technology, GaN on Si will make inroads into the RF market and provide a significant cost advantage.

The fact that the silicon industry is exploring InGaAs channels for use in CMOS beyond the 8 nm node, also creates the opportunity for fabricating other III-V devices on large diameter Si substrates in a silicon fab. However, significant development is required to create Si fab compatible III-V process modules.

Uniformity, reproducibility, and yield for compound semiconductors still lag behind Si-based technologies. This is not surprising, given the much higher investment in infrastructure and research for silicon, as well as the extremely large disparity in production volume between the two. For example, III-V fabrication tend to still use 'evaporation and liftoff' and electroplating techniques (particularly for backend interconnects) which are inherently 'dirtier', and hence lower yield, fabrication processes when compared to the deposition/subtractive patterning/CMP processes perfected for Si. Again, transitioning III-V device fabrication into a silicon foundry to take advantage of the Si infrastructure and high yield processing techniques provides a potential solution to the uniformity, reproducibility, and yield challenge.

Nevertheless, as production volume in a particular compound technology rises, unit costs are found to decrease on a learning curve not unlike that of silicon.

Another potential solution for the substrate scaling challenge, as well as the integration density challenge, is the heterogeneous integration of III-V devices with Si CMOS on a silicon substrate. This integration approach is analogous to the SiGe BiCMOS process in which the SiGe HBT is replaced by a III-V transistor. This integration approach marries high-density digital circuitry with high performance III-V transistors to create 'mostly digital' RF and mixed-signal circuits whose performance cannot be achieved with either Si or III-V technology alone. Recent advances under DARPA's COSMOS program (integration of InP HBTs with Si CMOS) have demonstrated the feasibility of this integration approach.[31] GaN HEMTs have been also successfully integrated on a silicon substrate with Si CMOS [32]. Again, to realize the true cost and performance advantage of the heterogeneous integration approach, the entire fabrication processes needs to reside in a silicon foundry. Significant development is required to create Si fab compatible III-V process modules.

While significant advances are being made in optical lithography tools, the cost of these tools along with the cost of masks to define sub 0.25 μm features is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beam is a solution to the mask cost, but wafer through-put, which is measured in hours per III-V wafer as compared to wafers per hour, needs to be increased with high current electron sources and fast alignment systems. Since the III-V market for process tools is small, tool vendors have no incentive to develop tools for III-V foundries. Fortunately, high throughput, high-resolution e-beam lithography tools are under development for the silicon industry, however, the tools may be cost prohibitive for III-V foundries. Access to these tools may require fabrication of III-V devices in Si foundries on large diameter wafers.

While silicon carbide substrates are the defacto standard for GaN RF (power) devices due to their high resistivity and thermal conductivity, substrate (and epi) quality still has room for improvement. The use of GaN substrates provides a path to the growth of higher quality GaN HEMT epitaxy though homoepitaxy, however, while research on GaN substrates is continuing, GaN substrate maturity lags significantly behind SiC substrates in both quality and diameter, not to mention GaN substrates exhibit poorer thermal conductivity compared to SiC. Improved power densities in III-V devices made possible by advanced materials and device structures place an increased burden on thermal management. For example, while SiC substrates have significantly higher thermal conductance values compared to GaAs, InP and Si, the 5× to 10× higher power densities typically present in GaN transistors somewhat offsets the advantage in higher thermal conductance. Typical solutions to date have relied on substrate thinning to remove heat from the backside of the device and into a passive or active heat spreader in the ground plane. While this approach has been effective for GaAs and InP microwave devices, the trend toward high power density GaN technologies as well as power applications into the mm-wave spectrum pose additional issues related to the high thermal resistance of ternary and quaternary epitaxial layers in bandgap engineered devices as well as the much smaller size of mm-wave devices. As substrates are thinned, the contribution of the high thermal resistance epitaxial layers and the die attach medium increases disproportionally, particularly for small gate geometries, due to the thermal spreading resistance factor. While thermal management will include substrate thinning, the substrate thickness will also be dictated by RF considerations, particularly for microstrip transmission lines.

In addition to substrate thinning, solutions to device thermal management may include such techniques as thermal vias, topside heat removal structures, and site specific cooling. Thermal vias, in which a high thermal conductivity plug of material in placed beneath the power dissipation site in a transistor, have been explored using gold as a plug. However, mechanical stress due to thermal mismatch is a problem. Engineered nano materials, in which high conductivity materials which match the substrate thermal coefficient of expansion (CTE), are a possible solution. Topside gold shunts have also been demonstrated, but can interfere with the electric field distribution in the circuits. More recently GaN HEMTs on diamond substrates is beginning to emerge as a potential solution to the thermal challenge. Several companies are developing techniques to transfer device quality GaN HEMT epitaxy onto relatively low cost polycrystalline diamond substrates thus providing a very low thermal resistance path to the heat sink. Significant development is required to mature this approach and scale it to usable substrate diameters. A Defense Advanced Research Projects Agency (DARPA) program to address site specific cooling ("Near Junction Thermal Transport - NJTT)) is one of a portfolio of programs addressing high conductivity heat spreaders, micro-air cooling and high conductivity die attach materials. Solutions to thermal management will include all components in the thermal path from the junction outward. Other forms of carbon, such as graphene thermal spreaders and graphitic thermal interface materials,may also provide viable thermal solutions.

In contrast to Si CMOS which uses planar, self aligned gates and implanted or epitaxially regrown contact layers to engineer the device, gate recessing is typically used to engineer GaAs and InP based FETs to achieve high frequency

performance and higher breakdown voltages. The recess process utilizes epitaxially grown etch stop layers and high etch selectivity to create high yield processes. This approach is also being used to scale GaN HEMTs to millimeter wave frequencies, although significant development is still required to achieve high yield selective recess process. Other approaches for engineering of III-V FETS is the use of field plates to tailor the electric field on the drain side of the gate to achieve high breakdown voltages, although the use of filed plates compromise high frequency performance. Due to the high fields present in III-V power devices, continued improvement of passivation and hot carrier effects is also needed. The creation of high density, nano-composite/laminate dielectric layers by ALD (dielectric engineering) is a potential solution that leverages recent developments in Si technology.

It is highly desirable in mixed-signal electronics to have transistors capable of accommodating voltage swings of 10 V or more. As transistor speed is scaled for many mixed-signal or analog applications, it comes at the cost of low breakdown voltage values that greatly restrict the dynamic range of the circuits and represent a severe limitation. In this regard, InP HBTs that exhibit higher breakdown voltage for a give emitter geometry or transistor speed offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe is orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs. Gallium nitride HEMTs offer even higher promise due to the potential for a 10x increase in the Johnson figure of merit.

The performance of other RF circuit elements, such as mixers, can be also directly related to the dynamic range of the device. Therefore, it is necessary to scale the dimensions of a transistor to achieve the desired frequency performance while maintaining desirable breakdown voltage to allow large voltage swing for high dynamic range.

Currently, the GaN technology is primarily driven by microwave frequency power amplifier applications due to its ultra high breakdown field. The cut-off frequencies of GaN field effect transistors are now well over 100 GHz and existing monolithic microwave integrated circuits (MMICs) only consist of no more than ten transistors with air-bridge interconnect system. Both the transistor performance and integration level of circuits are too low to enable high-performance mixed-signal circuits. To fully exploit the potential of GaN devices for desired wide dynamic range circuits, a next-generation nitride electronic technology is being developed to achieve high transistor speed (~ 500 GHz) and high integration level (> 1000 transistors) by scaling the transistors, reducing parasitic resistances and capacitances, and utilizing multi-level interconnects as has been done in silicon technology. In addition, the development of a stable enhancement mode (E-mode) operation is critical. This will offer many important practical advantages in circuit applications, including greater simplicity in mixed-signal and RF circuits and the ability to implement enhancement/depletion (E/D) logic capability (direct-coupled FET logic). Further, large scale integration of hundreds to thousands of transistors demands a manufacturing technology that can achieve high yield.

Uniformity of transistors is particularly important for mixed-signal electronics and further underscores the need to develop a robust, manufacturable device process. The impact of the future GaN technology will be profound and will, lead to dramatic improvements in the performance of RF and mixed-signal electronic circuits, which include high-speed high power amplifiers, ultra-linear mixers, and high-output-power digital-to-analog converters.

High-frequency performance in III-Vs, and now even in CMOS, is driven as much by epitaxy, bandgap and strain engineering (vertical scaling), as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by properly engineering the epitaxial layer stack, the source and drain regions, the substrate orientation, and/or the dielectric stack above the device. We expect continued improvements by bandgap and strain engineering in all of the III-Vs.

Simultaneously achieving high power added efficiency, high linearity, and high output power is a significant challenge for III-V power amplifiers used in RF and mm-wave transmitters. In most narrowband applications, a switched-mode amplifier (Class D, E, or F) is a potential solution to meet these simultaneous requirements. For example, a Class-F architecture uses a pinched-off transistor (high negative V_{GS}) and allows the input power to turn the device on and off, generating an RF square-wave voltage waveform that is out of phase with the half sinusoidal current waveform. This design approach minimizes power dissipation (I-V product) during amplifier operation. For Class F amplifier operation to be highly efficient, all harmonics generated due to the non-linear voltage waveform have to be suppressed using even and odd harmonic resonant matching networks. This type of amplifier can theoretically achieve > 95% PAE for an ideal narrowband case. Transistor device requirements for this level of efficiency are extremely low on-resistance and low drain-source capacitance. These device requirements are commensurate with devices with unity gain cutoff frequencies (f_T) 10x greater than the desired amplifier operating frequency. Therefore, devices with f_T in the submillimeter wave range (> 300 GHz) are needed for efficient, Class F amplifier operation of mmW amplifiers (30-100 GHz).

Circuit design solutions have shown utility for improving the combination of efficiency and linearity from an amplifier. The Doherty amplifier enables improved efficiency relative to conventional architectures. Doherty amplifiers are typically

used in applications requiring high linearity, such as communications rather than those requiring wide bandwidth, such as electronic warfare. The Doherty amplifier power-combines two amplifiers that are biased differently – one is at Class AB while the other is at Class C that only conducts at half of the cycle. The benefit of the Doherty amplifier is improved power-added efficiency, at power levels well below saturation. Adaptive digital pre-distortion (DPD) designs, where the input signal is pre-distorted in the digital domain to compensate for device non-linearities, have also been used to improve linearity.

For receiver applications requiring wide bandwidth, in addition to high linearity and power added efficiency, recent circuit design innovations in feedback linearization, similar to classical operational amplifier techniques, offer potential solutions. In these approaches, excess gain-bandwidth product (such as that available in InP HBT amplifiers operating at 2 GHz) is traded for linearity without increasing DC power dissipation. Wideband microwave operation amplifiers have recently demonstrated a 5x improvement in the ratio of output third-order intercept point (OIP3) to DC power.

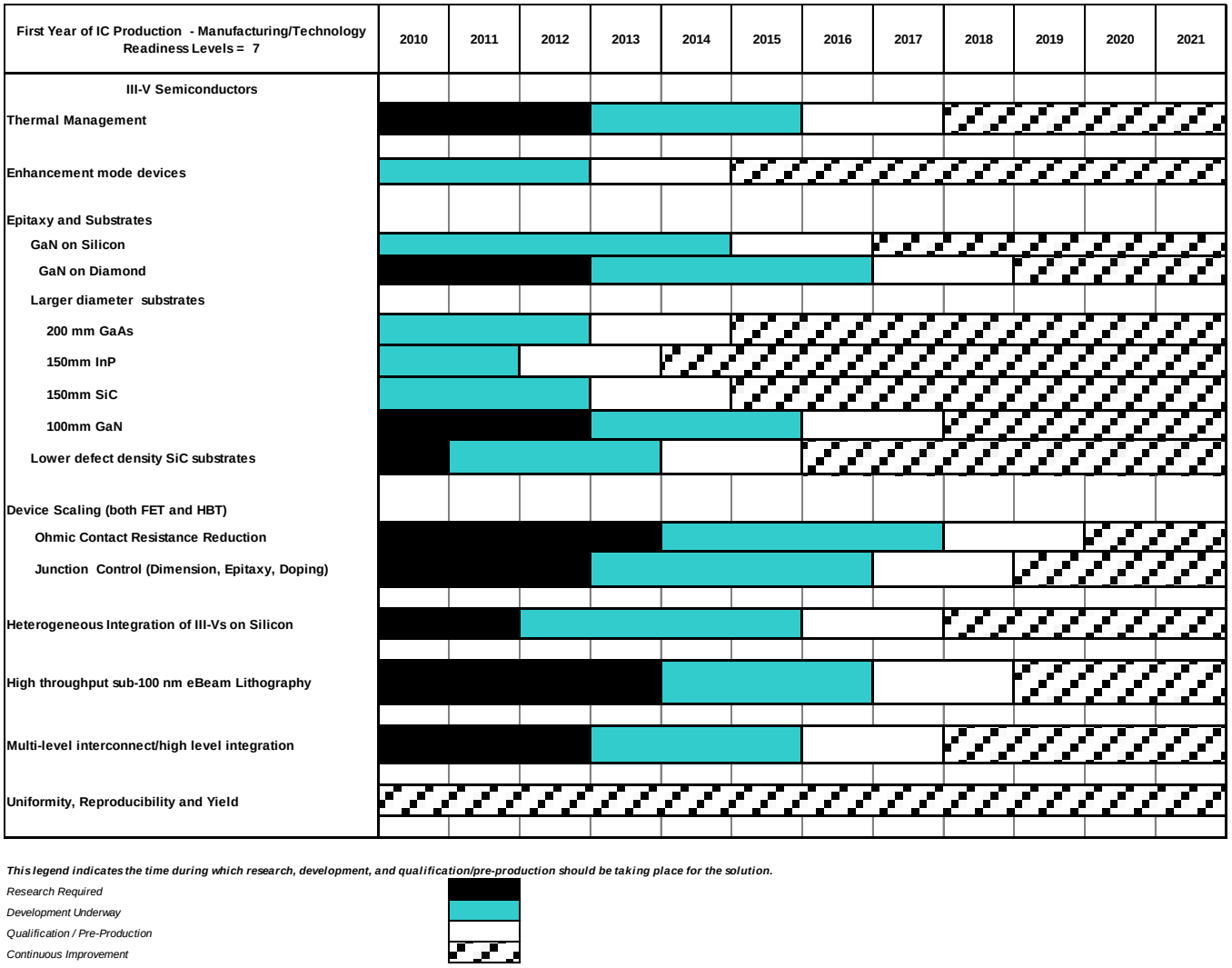

Figure RFAMS5 Group III-V Compound Semiconductors Potential Solutions

4.4 PASSIVE ON-CHIP DEVICES

Passive devices are challenged by cost-performance trade-offs. A low-cost device implemented on-chip with adequate performance is the preferred solution. The advent of small-pitch through-silicon vias enabling stacking of different technologies will be used to integrate high-performance transistors with high-performance passive devices on different substrates with low-loss connections at device-level geometries. This ultimately pushes passive devices off-chip and mainly into the package substrate. There is already a growing trend towards System-in-Package (SiP), MEMS passives [33], and Embedded Passives. These passive elements (*e.g.* capacitors and resistors) are placed/formed between interconnecting substrates of a printed wiring board. They represent a promising solution in terms of reduction in size and assembly costs of SiP.

5.0 CROSS-CUT ISSUES

5.1 ESH, METROLOGY, YIELD ENHANCEMENT, MODELING AND SIMULATION

In coming years the RF and AMS TWG needs to expand its interaction with both the Metrology and the Modeling and Simulation TWGs. The measurement of device parameters and FOMs at frequencies in the mm-wave bands is becoming necessary both in understanding the physical mechanisms limiting device performance and in being able to accurately simulate this performance. Commercial equipment capable of performing these measurements has recently become available for frequencies up to 750 GHz. But, such equipment has not been in use long enough to establish standardized methodologies for de-embedding devices parameters from the parasitics. There is a need for building a consensus and establishing standardized methodologies. Even below 50 GHz a consensus is at best limited and a standard methodology does not exist. Production measurements above 50 GHz are practically non-existent.

Some of the most important measurement and standards needs include:

1) Improve dynamic ranges in small-signal measurements, equipment, and methodology.
2) Better measurements and instrumentation in the mm-wave range for noise performance characterization. Noise sources above 200 GHz are not currently readily available.
2) Pushing large-signal network analysis up to millimeter-wave frequencies. This would let designers see the voltages and currents inside their nonlinear devices as they operate, and develop large-signal models that they can use to optimize efficiency and linearity at the same time.
3) Better signal measurement tools to allow modulation formats to be standardized.

5.2 OTHER CROSS-TWG DISCUSSIONS

This year we have expanded our interactions with the Assembly and Packaging TWG as we defined better the treatment of passive device and helped inaugurate the MEMS TWG. We also had very fruitful interaction with the System Drivers TWG in re-writing the Mixed Signal Driver section of that chapter. This allowed us, for the first time, to make some comments on the suitability of a given technology for a given application.

5.3 IMPACT OF FUTURE EMERGING RESEARCH DEVICES AND MATERIALS

The Emerging Research Devices and Emerging Research Materials Groups use the concept of the future RF transceiver as the context in which to consider selected new devices and materials for RF applications that are within the ITRS domain called “More than Moore” (MtM). At the 2011 ITRS Summer meetings, they presented the following three emerging technologies as future candidates for RF transceiver functions of transistors, mixers, local oscillators, and resonators:

1) Sub-100 nm graphene RF FET transistors fabricated using nanowire gates have the possibility of THz cut-off frequencies. The high Fermi velocity of the carriers in grapheme results in a high drift velocity of about 4×10^7 cm/s in the channel. For example, a 70 nm channel length graphene RF FET is likely to have a cut-off frequency f_T of about 1 THz. Such transistors have possible applications as low noise amplifiers and mixers.
2) Nanometer-sized spin-torque oscillators (STOs) are likely to have low phase noise and be tuned from 0.1 GHz to more than 40 GHz by external magnetic fields, spin-torque currents, and magnetic materials and structures.
3) Resonators made from NEMS devices (nano-resonators) will be used for RF filters that are expected to have high Q values and ultimately be tunable. Materials of interest for this application include silicon nanowires, III-V-compound semiconductor nanowire, carbon nanotubes, and graphene.

5.4 ANALOG CHALLENGES/TOPICS

This year, the ITRS took up a challenge from the Semiconductor Industry Association (SIA) to increase its treatment of analog technologies. In response, we expanded the scope of the application drivers considered when defining technology requirement. These applications span the range of frequencies from 0 to 300 GHz and are described in Figure RFAMS1. The chapter was re-organized by technology and each section addresses those applications generally produced in that given technology. We consider 5 circuit types as reflected in the Mixed Signal Drivers section of the *System Drivers* chapter. In addition, we consider general analog circuits such as voltage regulators, operation amplifiers and current sources. New members with subject-area expertise drove the expansion into these new areas. Conversely, the extent of our treatment of the available analog technologies was limited by the participation of subject area expert. Readers wishing to see the treatment of additional analog technologies are encourage to volunteer their efforts.

5.5 RF MEMS STRUCTURES

The new MEMS ITRS Chapter includes section on difficult challenges and technology requirements for RF MEMS resonators, capacitive switches, and varactors and a more complete discussion of cross-cut issues with RF and AMS technologies for communications. RF MEMS metal contact switches are not included.

RF MEMS devices not only include thin-film bulk-acoustic wave resonators (FBAR), surface acoustic wave resonators (SAW), capacitive switches, and metal contact switches, but also other MEMS devices types such as sensors (e.g., accelerometers and gyroscopes), microphones, and displays that add functionality to RF products. These MEMS accelerometers, gyroscopes, microphones, and displays devices are discussed in the 2010 iNEMI MEMS Chapter and except for display, are not discussed in this MEMS ITRS Chapter. For these reasons, they are not discussed in the RF and AMS Chapter. In general, the above four device types have found or will find use in wireless communication products as discrete devices, e.g., a FBAR filter mounted to a board or mother chip, or a Si MEMS oscillator replacing a quartz part in an existing socket. The time at which the RF MEMS devices are produced in high-volumes often occurs when the MEMS function is integrated with the CMOS, BiCMOS, or bipolar semiconductor die. The timing for this integration will be primarily driven by cost. Until that time, initial introductions will occur in the following order: 1) favor discrete die (e.g. FBAR devices), 2) above or below IC implementations (e.g. variable capacitors), and 3) monolithic integrations with semiconductor die, which will potentially reduce the bill of materials by removing customized MEMS packaging from some devices and enable new applications due to integration and cost reduction.

6.0 OTHER CONSIDERATIONS

6.1 INTERNATIONAL STANDARDS AND ASSOCIATED MEASUREMENTS

The global competition to manufacture high-volume innovative RF and AMS products with enhanced functions and performance, such as those enabled by nano-electrotechnologies, e.g., MEMS/NEMS, is intense because nations want to strengthen their economies and create new jobs for their citizens and companies want to grow market share and profits by being the first to introduce higher value devices using the newest technologies. International standards and their associated metrologies are significant enablers for success at all stages of RF and AMS innovation - from research, development, initial deployment, high-volume commercialization, end of initial useful life, to recycling and disposal. Standards can be the catalysts for more efficient innovation and successful commercialization of technologies, provided they incorporate the best available engineering and science in which contributors to ITRS roadmapping activities excel. Standards can insure interoperability and reduce the number of times different designs are implemented, thereby freeing engineering resources to innovate where it will be a true differentiator. Equally important, standards greatly affect business models and outcomes. Those who contribute to ITRS roadmapping also excel in the skills essential for contributing to international standards and supporting measurements. By so doing, they increase the likelihood that international standards and supporting measurements will be better aligned with future ITRS goals and roadmaps.

Collaborations that involve many diverse organizations such as semiconductor companies, trade associations, R and D laboratories, national measurement institutes, and international standards and technology roadmapping bodies are required to ensure that the essential standards, associated measurements infrastructure, and scientific/engineering-knowledge base are all adequate to overcome technology barriers, especially barriers associated with nano-electrotechnologies identified in the ITRS. Such collaborations enable the successful development and subsequent manufacture of next generation materials (ERM) and devices (ERD) and appropriate packaging and assembly. For example, the Technical Committee 113 on nano-electrotechnologies, a technical committee of the International Electrotechnical Commission, has as one of its major goals that IEC's standards for nano-electrotechnnologies occur through collaborations with other organizations whenever such collaboration is in the best interests of the international

standards community. The complete title for TC 113 is *Nanotechnology standardization for electrical and electronic products and systems.* TC 113 is developing standards for nano-electrotechnologies that includes nanoelectronics. More information about IEC TC 113 is available at http://www.iec.ch.

"Standards enable innovative products and new markets."
– Patrick Gallagher, NIST Director, November 2009

7.0 CONCLUSIONS

We list here some trends common to many of the RF and AMS technologies. These trends offer a framework in which to develop future editions of the RF and AMS Chapter and its updates.

Mesh-networks using mobile millimeter-wave communications are very promising solutions for addressing the spectrum crunch. Because of this, there is a lot of exploratory work on mobile devices at millimeter wavelengths. We expect to include more of the technologies that support mesh-networks in future editions of this RF and AMS Chapter. This potential application is considered by many to be the holy grail of RFICs, especially silicon RFICs that would bring down cost and bring commercial applications closer. Even though we are still a long way from this goal, there are several innovations that will assist in attaining this goal such as the following:

1) Stacked devices to improve output power, more efficient amplifier configurations than the traditional, combining InP or GaN with silicon to get the best of both worlds.
2) Using silicon digital processing power to linearize inherently nonlinear but efficient transmitters.
3) MIMO to get the connectivity in channels that are characterized by high multipath and fading, and to make the most of the silicon processing power and small antenna size.

7.1 RF CMOS

The CMOS roadmap this year attempts to more accurately reflect the RF and Analog performance of the transistors of the high-performance and low standby-power technologies presented in the PIDS chapter. Where PIDS presents three CMOS transistor architecture options, overlapping in time, we reflect the same options.

It is instructive to consider two of the circuit level FOMs, presented in the *System Drivers* chapter, the values of which we can estimate using transistor-level FOMs. First, the upper-limit of LNA FOM allows us to compare the performance potential of CMOS, SiGe HS-NPN and the InP HEMT. Figure RFAMS6 shows that CMOS is roughly equally suited for implementing a 60 GHz LNA when compared to the SiGe and III-V transistors.

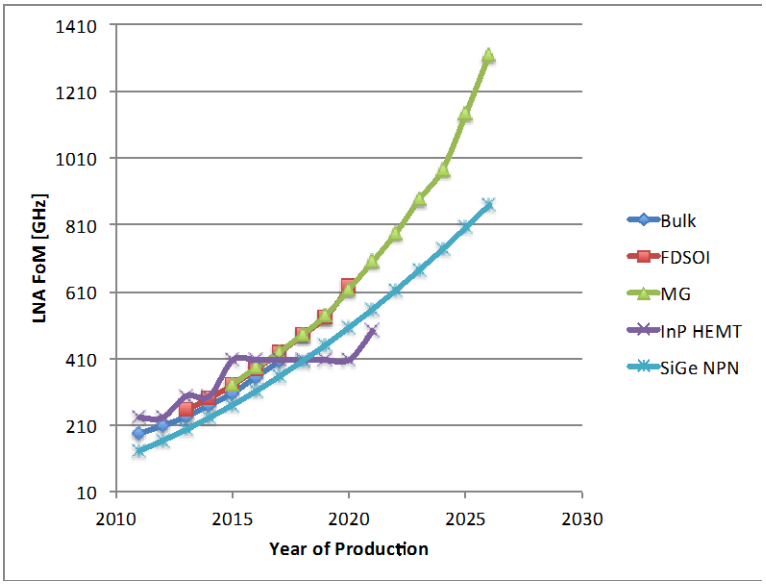

Figure RFAMS6 LNA Performance comparing CMOS, SiGe and InP Transistor Roadmaps

The result is different if we consider power amplifiers. The FOM for power amplifiers can be estimated from device FOMs as described in the System Drivers Chapter. The technology comparison in Figure RFAMS7 now shows a clear advantage of InP and especially GaN HEMTs over CMOS. Furthermore, SiGe NPNs are shown to perform equally well to GaN HEMTs. One must note that these FOMs do not provide the whole picture. For example, they ignore the fact that the load resistance needed to achieve the assumed output power will be extremely low for Si devices and essentially illustrate an unrealistic design point.

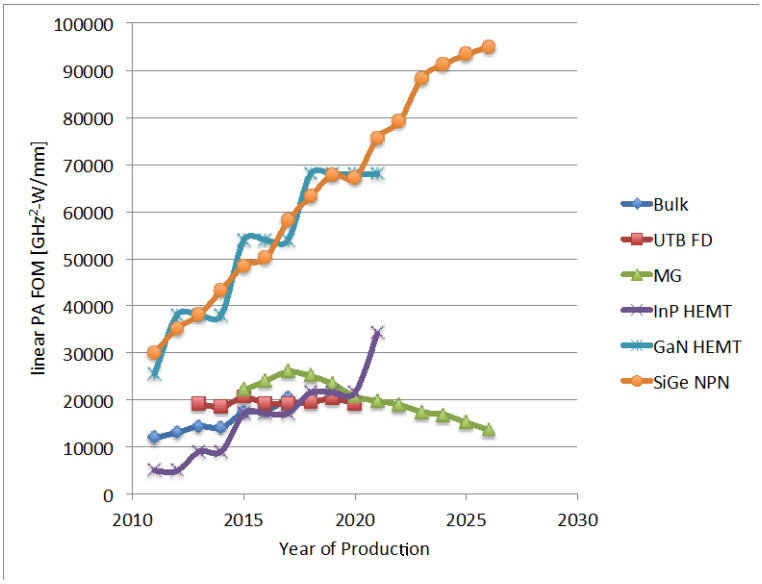

Figure RFAMS7 PA Performance comparing CMOS, with InP and GaN HEMT Transistor Roadmaps

CMOS technology performance for the PA application is projected to roll-off dramatically with technology scaling. This highlights the fact that while bandwidth may be high, the transistor gain is limited by its low-frequency value. The suitability of CMOS relative to other device technologies to implement a given application will depend on performance but also on other factors including cost and integration level.

7.2 Group IV Bipolar and BiCMOS Devices

The HS-NPN roadmap moved a step further with the use of simulation to generate the transistor table, which also allows providing consistent values for the circuits FOM. This roadmap is driven by the performance increase that is required to move from one BiCMOS node to the next, but the pace of this improvement is weighted by the technical challenges, as estimated today. These technical challenges facing the Si/SiGe bipolar and BiCMOS roadmap are multiple and involve the development of new architectures, vertical profile control, reduction of resistances, and integration with advanced CMOS nodes. But these challenges are probably not the only show-stoppers today. Indeed, the pace of the roadmap is also driven by the market, as it should be. In this respect, the development of high-speed NPN BiCMOS technologies is presently driven by optical communications, although emerging millimeter-wave markets are expected to drive more volumes in the future. These volumes are difficult to estimate today, because they deal with new applications (the development of which depends on marketing success) and because some of these markets may also be covered by CMOS and III/V technologies.

7.3 Group III-V Compound Semiconductors consisting of elements from groups III and V [both bipolar and field effect transistors (FET)]

Because of their superior transport properties and higher breakdown fields, devices based on III-V compound semiconductors will continue to serve niche markets, in applications 1) that are driven more by performance and less by cost and 2) where silicon technology can not meet the performance requirements such as high dynamic range or low noise figure. Examples include InGaP HBTs for cell phone PAs, GaN HEMTs for commercial and military microwave and millimeter wave high power PAs and tube replacements, and InP HEMTs and HBTs for millimeter wave and submillimeter wave transceivers. Compound semiconductors will continue to advance through a combination of gate

length (emitter width) scaling and more importantly epi or bandgap engineering and over time III-V devices will merge with Si technologies (through heterogeneous integration) resulting SoCs with the 'best junction for the function'.

7.4 PASSIVE ON-CHIP DEVICES

We address the challenges and requirements of passive on-chip devices only. The *Assembly and Packaging* Chapter treats passive off-chip and embedded devices. We address lumped device, i.e.; capacitors, resistors, inductors, and varactors, primarily for applications operating at frequencies less than 30GHz. We also begin to treat passive distributed devices, based on transmission lines, primarily for applications operating at frequencies above 30 GHz.

8.0 REFERENCES

[1] http://www.bizjournals.com/prnewswire/press_releases/2012/05/28/SP14461 , October 30, 2013.

[2] Hook, T.B.; Brown, J.S.; Breitwisch, M.; Hoyniak, D.; Mann, R.; , "High-performance logic and high-gain analog CMOS transistors formed by a shadow-mask technique with a single implant step," IEEE Transactions on Electron Devices, vol.49, no.9, pp. 1623- 1627, September 2002

[3] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, N. Kinayman, N. Jain, R. Anderson, F. Kolak, R. Wohlert, S.P. Bawell, J. Bennett, J.-P. Lanteri, "Ultra-wideband radar sensors for short-range vehicular applications," IEEE Transactions on Microwave Theory and Techniques, Vol. 52, No. 9, pp. 2105 – 2122, September 2004.

[4] U.R. Pfeiffer, E. Ojefors, A. Lisauskas, H.G. Roskos, "Opportunities for silicon at mmWave and Terahertz frequencies," in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, pp. 149 - 156, 2008.

[5] P. Chevalier, T. Lacave, E. Canderle, A. Pottrain, Y. Carminati, J. Rosa, F. Pourchon, N. Derrier, G. Avenier, A. Montagné, A. Balteanu, E. Dacquay, I. Sarkas, D. Celi, D. Gloria, C. Gaquiere, S.P. Voinigescu, and A. Chantre "Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz", in Compound Semiconductor IC Symposium Technical Digest, 2012

[6] B. Heinemann, R. Barth, D. Bolze, J. Drews, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, S. Marschmeyer, H. Rücker, D. Schmidt, M. A. Schubert, B. Tillack, C. Wipf, D. Wolansky, Y. Yamamoto, "SiGe HBT technology with fT/fMAX of 300GHz / 500 GHz and 2.0 ps CML gate delay", in IEDM Technical Digest, pp. 688-691, 2010.

[7] M. Schroter, G. Wedel, B. Heinemann, C. Jungemann, J. Krause, P. Chevalier, A. Chantre, "Physical and electrical performance limits of high-speed SiGeC HBTs - Part I: Vertical scaling", IEEE Trans. Electron Dev., Vol. 58, No. 11, pp. 3687-3696, 2011, and M. Schroter, J. Krause, N. Rinaldi, G. Wedel, B. Heinemann, P. Chevalier, A. Chantre, "Physical and electrical performance limits of high-speed SiGeC HBTs - Part II: Lateral scaling", IEEE Trans. Electron Dev., Vol. 58, No. 11, pp. 3697-3706, 2011.

[8] R. A. Pucel, H. A. Haus, and H. Statz, " Signal and Noise Properties of Gallium Arsenide Microwave Field Effect Transistors, " Advances in Electronics and Electron Physics, Vol. 38, New York: Academic Press, 1975, pp156-163

[9] P.H. Ladbrooke, "MMIC Design: GaAs FETs and HEMTs," Chapter 6, Artech House Inc., Boston, 1989.

[10] Razavi, B.; Ran-Hong Yan; Lee, K.F.; , "Impact of distributed gate resistance on the performance of MOS devices," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol.41, no.11, pp.750-754, November 1994.

[11] P.J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum fT of millimeter-wave MODFETs," IEEE Electron Device Lett., vol.10, No.7, pp.291-293, July 1989.

[12] R. Groves, J. Wang, L. Wagner, A. Wan, "Quantitative Analysis of Errors in On-Wafer S-Parameter De-embedding Techniques for High Frequency Device Modeling", in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2006, pp. 92 - 95.

[13] F. Pourchon, C. Raya, N. Derrier, P. Chevalier, D. Gloria, S. Pruvost, D. Céli, "From Measurement to Intrinsic Device Characteristics: Test Structures and Parasitic Determination", in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2008, pp. 232-239.

[14] O. Inac, B. Cetinoneri, M. Uzunkol, Y. A. Atesal, G. M. Rebeiz, "Millimeter-Wave and THz Circuits in 45-nm SOI CMOS", in Compound Semiconductor IC Symposium Technical Digest, 2011

[15] S. P. Voinigescu, E. Dacquay, V. Adinolfi, I. Sarkas, A. Balteanu, A. Tomkins, D. Celi, P. Chevalier, "Characterization and Modeling of an SiGe HBT Technology for Transceiver Applications in the 100–300-GHz Range", IEEE Transactions on Microwave Theory and Techniques, Vol. 60, No. 12, December 2012, pp. 4024-4034

[16] A. Balteanu, I. Sarkas, E. Dacquay, A. Tomkins, G. M. Rebeiz, P. M. Asbeck, S. P. Voinigescu, "A 2-Bit, 24 dBm, Millimeter-Wave SOI CMOS Power-DAC Cell for Watt-Level High-Efficiency,Fully Digital m-ary QAM Transmitters", IEEE Journal of Solid-State Circuits, Vol. 48, No. 5, May 2013, pp. 1126-1137

[17] S. P. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre, B. Sautreuil, "A Study of SiGe HBT Signal Sources in the 220–330-GHz Range", IEEE Journal of Solid-State Circuits, Vol. 48, No. 9, Sept. 2013, in press.

[18] M. Seo et al, "A 1.1V 150GHz amplifier with Passive Imaging Receiver with 8dB gain and +6dBm saturated output power in standard digital 65nm CMOS using dummy pre-filled microstrip lines," in 2009 IEEE ISSCC Technical Digest., pp. 484-485, February 2009.

[19] K.H.K. Yau, I. Sarkas, A. Tomkins, P. Chevalier, and S.P. Voinigescu, "On-wafer S-parameter De-embedding of Silicon Active and Passive Devices up to 170-GHz," in IEEE IMS Technical Digest, pp.600- 603, May 2010.

[20] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design", IEEE Journal of Solid-State Circuits, Vol. 32, No. 9, pp. 1430-1438, September 1997.

[21] K.H.K Yau, P. Chevalier, A. Chantre, and S.P. Voinigescu,"Characterization of the Noise Parameters of SiGe HBTs in the 70-170 GHz Range," IEEE Transactions on Microwave Theory and Techniques, Vol. 59, No. 8, pp. 1983-2000, August 2011.

[22] J. Herricht, P. Sakalas, M. Ramonas, M. Schroter, C. Jungemann, A. Mukherjee, K.-E. Moebus, "Systematic method for usage of correlated noise sources in compact models for high frequency transistors", IEEE Trans. Microw. Theory Techn., Vol. 60, No. 11, pp. 3403-3412, 2012.

[23] Lai, R.; Mei, X.B.; Deal, W.R.; Yoshida, W.; Kim, Y.M.; Liu, P.H.; Lee, J.; Uyeda, J.; Radisic, V.; Lange, M.; Gaier, T.; Samoska, L.; Fung, A.; "Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz", in Technical Digest of the IEEE International Electron Devices Meeting, 2007, pp 609 – 611].

[24] J. Hasch, U. Wostradowski, S. Gaier, and T. Hansen, "77 GHz Radar Transceiver with Dual Integrated Antenna Elements," in Proceedings of the 5th German Microwave Conference (GeMiC 2010), March 2010, pp. 280–283.

[25] Y. Atesal, B. Cetinoneri, M. Chang, R. Alhalabi, and G. Rebeiz, "Millimeter-Wave Wafer-Scale Silicon BiCMOS Power Amplifiers Using Free-Space Power Combining," IEEE Trans. Microw. Theory Tech.,vol. 59, no. 4, pp. 954–965, April 2011.

[26] Y. C. Ou and G. M. Rebeiz, "On-Chip Slot-Ring and High-Gain Horn Antennas for Millimeter-Wave Wafer-Scale Silicon Systems," IEEE Transactions on Microwave Theory and Techniques, Vol. 59, No. 8, pp. 1963 - 1972, August 2011

[27] D. Bolze, B. Heinemann, J. Gelpey, S. McCoy, W. Lerch, "Millisecond Annealing of High-Performance SiGe HBTs", in Proceedings of the 17th International Conference on Advanced Thermal Processing of Semiconductors, 2011, in press.

[28] P. Chevalier, T.F. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, A. Chantre, " Towards THz SiGe HBTs", in Proceedings of the Bipolar/BiCMOS Technology Meeting, 2011, pp. 57-65.

[29] K. Schuegraf, M. C. Abraham, A. Brand, M. Naik, R. Thakur, "Semiconductor Logic Technology Innovation to Achieve Sub-10 nm Manufacturing", IEEE Journal of the Electron Devices Society, Vol. 1, No. 3, pp. 66-74, March 2013

[30] A. R. Boyd; S. Degroote; M. Leys; F. Schulte; O. Rockenfeller; M. Luenenbuerger; M. Germain; J. Kaeppeler; M. Heuken, "Growth of GaN/AlGaN on 200 mm diameter silicon (111) wafers by MOCVD," Phys. Status Solidi C 6, 2009, pp. S1045-S1048.

[31] Raman S, Chang T-H, Dohrman CL, Rosker MJ. 2010 The DARPA COSMOS Program: The Convergence of InP and silicon CMOS Technologies for High-Performance Mixed-Signal. 2010 International Conference on Indium Phosphide and Related Materials (IPRM), 1-5 (doi: 10.1109/ICIPRM.2010.5516241)

[32] Kazior TE, Chelakara R, Hoke W, JBettencourt J, T. Palacios, H.S. Lee, "High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate", 2011 IEEE Compound Semiconductor IC Symposium (CSICS) Technical Digest, (doi: 10.1109/CSICS.2011.6062443)

[33] M. Rais-Zadeh, J. Laskar, and F. Ayazi, "High performance inductors on CMOS-grade trenched silicon substrate," IEEE Transactions on Components and Packaging Technologies, vol. 31, no.1, pp.126-134, 2008.

9.0 Acknowledgments

We thank our many colleagues with whom we have consulted to prepare the technology requirements tables and text for this 2013 RF and AMS Chapter. We also acknowledge the support provided by our respective host institutions. Without their support and funding this 2013 RF and AMS Chapter would not be possible.