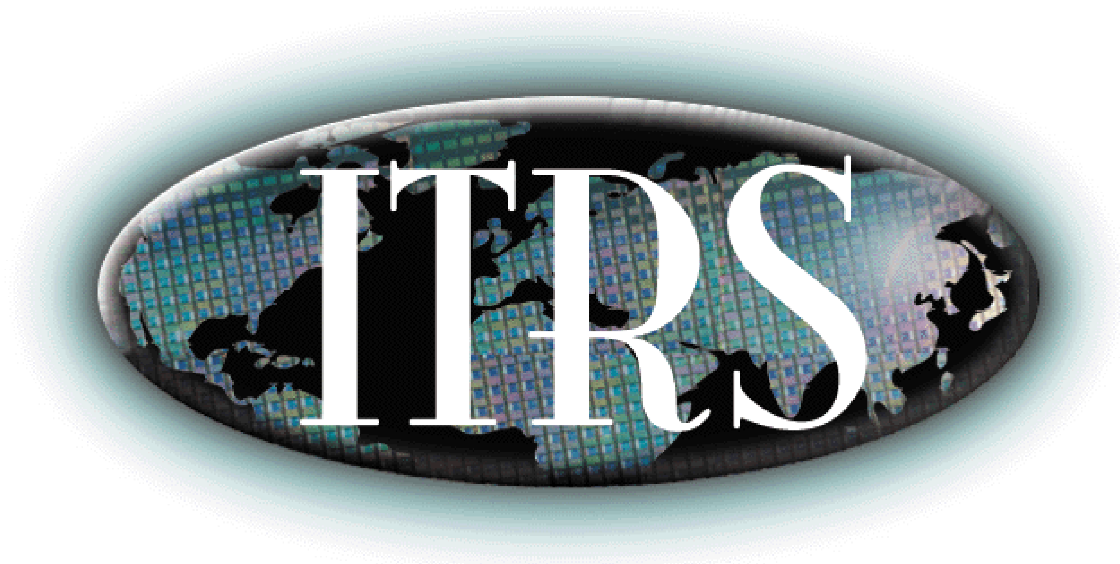

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

YIELD ENHANCEMENT

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Table of Contents

Yield Enhancement 1
1. Scope 1
2. Difficult Challenges 2
   2.1. Wafer Environmental Contamination Control 4
   2.2. Characterization, Inspection and Analysis 16
3. Potential Solutions 17
   3.1. Wafer Environmental Contamination Control 17
   3.2. Characterization, Inspection and Analysis 22
4. Yield Enhancement Supplemental Links (for team authors to check) 23
5. References 23

List of Figures

Figure YE1 Yield Enhancement Scope 1
Figure YE2 General Test Methodology for Ultrapure Water 11
Figure YE3 Wafer Environment and Reticle Environment Contamination Measurement and Control Potential Solutions 19
Figure YE4 Wafer Environmental Contamination Control Potential Solutions-UPW 20
Figure YE4 Wafer Environmental Contamination Control Potential Solutions-Liquid Chemicals 21
Figure YE5 Characterization, Inspection, and Analysis Potential Solutions 22

List of Tables

Table YE1 Definitions for the Different Interface Points 2
Table YE2 Yield Enhancement Difficult Challenges 3
Table YE3 Technology Requirements for Wafer Environmental Contamination Control 4
Table YE4 AMC Monitoring Methods 5
Table YE4a Supporting Table for On-line Methods 5
Table YE5 Defect Inspection on Pattern Wafer Technology Requirements 17
Table YE6 Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements 17
Table YE7 Defect Review and Automated Defect Classification Technology Requirements 17

YIELD ENHANCEMENT

1. SCOPE

Yield in most industries has been defined as the number of products that can be sold divided by the number of products that can be potentially made. In the semiconductor industry, yield is represented by the functionality and reliability of integrated circuits produced on the wafer surfaces. The scope of this chapter is currently limited to the yield of front end processing. The YE chapter does not discuss manufacture line yield, assembly/packaging yield, and final test yield. Yield Enhancement (YE) for manufacturing of integrated devices addresses the improvement from research and development yield to mature yield. The YE chapter displays the current and future requirements for high yielding manufacturing of DRAM, MPU, and Flash. Furthermore, it has the objective to identify the red brick wall for manufacturing, and to discuss potential solutions.

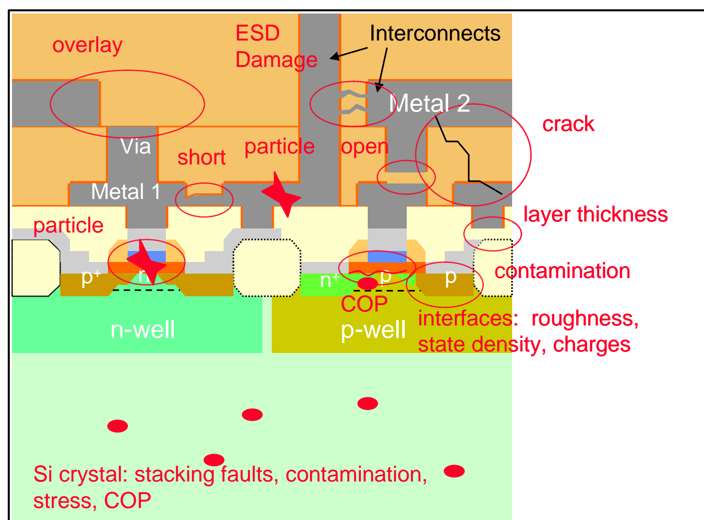

Figure YE1 Yield Enhancement Scope

During the manufacturing of integrated circuits yield loss is caused for example by defects, faults, process variations, and design. During processes such as implantation, etching, deposition, planarization, cleaning, lithography, etc. failures responsible for yield loss are occuring. Several examples of contaminations and mechanisms responsible for yield loss are listed in the following: a) airborne molecular contamination (AMC) or particles of organic or inorganic matter caused by the environment or by the tools; b) process induced defects as scratches, cracks, and particles, overlay faults, and stress; c) process variations resulting, *e.g.*, in differing doping profiles or layer thicknesses; d) the deviation from design, due to pattern transfer from the mask to the wafer, results in deviations and variations of layout and critical dimensions; and e) diffusion of atoms through layers and in the semiconductor bulk material.

The determination of defects and yield, and an appropriate yield to defect correlation are essential for yield enhancement. This correlation is of major importance, because not all defects change device properties or cause failure of devices or integrated circuits. Therefore, the yield enhancement chapter addresses not only the identification of tolerable contamination limits for processes and media, but also the tolerable budgets for particulate contamination of tools. The specification of tools for defect detection and classification of defects for root cause analysis addresses the technology requirements for detection and characterization of faults and failures.

The YE chapter has two focus topics: "Wafer Environment Contamination Control" and "Characterization, Inspection and Analysis." These two topics crosscut front end process technology, interconnect processes, lithography, metrology, design, process integration, test, and facility infrastructures.

Wafer Environment Contamination Control—Order-of-magnitude improvements in process critical fluid and gas impurity levels are not considered to be necessary in the foreseeable future. New materials and their precursors, however, introduce

challenges that require continuous study. Clarification of potential contamination from point-of-supply to point-of-process will define control systems necessary for delivered purity. There are several locations in the pathway from the original delivery package, *i.e*., the Point of Supply (POS) of a liquid or gas to the location where that material contacts the wafer, *i.e*., the Point of Process (POP), for ascertaining purity. This has led to a considerable amount of confusion and ambiguity in discussing the quality of process fluids, including the data found in Table YE3. Table YE1 summarizes the major fluid handling and/or measurement nodes found along the typical systems supplying process fluid. This table is an effort to create a common language for the discussion of attributes and requirements at these different node points. Further information regarding pathway nodes can be found in the supplementary materials and references, such as the Semiconductor Equipment and Materials International (SEMI) Standards.

Table YE1 Definitions for the Different Interface Points

	POS *Delivery Point of Gas/Chemical Supplier*	*POD* *Outlet of Central Facility System*	*POC* *Submain or VMB/VMP Take off Valve*	*POE* *Entry to Equipment or Sub Equipment*	*POU* *Entry to the Process Chamber*	*POP* *Contact with Wafer*
Interfaces	*SEMI Standards Focus Area*	*ITRS Factory Integration Facilities Group Focus Area*		*ITRS Factory Integration Equipment Group Focus Area*		*ITRS Front End Processes, Lithography, Interconnect TWG Focus Area*
Ultrapure water	Raw water	Outlet of final filtration in UPW plant	Outlet of submain take off valve	Inlet of wet bench or subequipment	Inlet of wet bench bath, spray nozzle, or connection point to piping, which is also used for other chemicals	Wafer in production
Process chemicals	Chemical drum/tote/bulk supply	Outlet of final filtration of chemical distribution unit	Outlet of VMB valve	Inlet of wet bench or intermediate tank	Inlet of wet bench bath or spray nozzle	Wafer in production
Specialty gases	Gas cylinder or bulk specialty gas systems	Outlet of final filtration of gas cabinet	Outlet of VMB valve	Inlet of equipment	Inlet of chamber (outlet of MFC)	Wafer in production
Bulk gases	Bulk gas delivered on site or gas generator	Outlet of final filtration/purification	Outlet of submain take off valve or VMB valve	Inlet of equipment/ subequipment	Inlet of chamber (outlet of MFC)	Wafer in production
Cleanroom and AMC	Outside air	Outlet of make-up air handling unit	Outlet of filters in cleanroom ceiling	Inlet to mini-environment or sub equipment for AMC, outlet of the tool filter for particles	Gas/air in vicinity to wafer/substrate	Wafer/substrate in production (AMC/ SMC)

POD—point of delivery POC—point of connection POE—point of entry POP—point of process POU—point of use VMB— valve manifold box VMP—valve manifold post UPW—ultra pure water MFC—mass flow controller AMC—airborne molecular contamination SMC—surface molecular contamination

Characterization, Inspection and Analysis—Physical device dimensions and corresponding defect dimensions continue shrinking, posing new challenges to detection as well as tolerable contamination. The wafer edges and backside were identified to show significant impact on yield as well as process variations and design. Development of defect detection, defect review, and classification technologies showing highest sensitivity at high throughput is crucial for cost efficient manufacturing. Furthermore for efficient manufacturing the monitoring of contamination in the environment and on the wafer surface requires appropriate analytic capabilities. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, electrical and virtual metrology results and their correlation to yield, test and work-in-progress data, will have to be developed to enhance root cause analysis and therefore enable rapid yield learning.

2. Difficult Challenges

The difficult challenges for the Yield Enhancement chapter are summarized in Table YE2. Currently, the most important key challenge will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is difficult to identify yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority the requirement for 3D inspection was identified. This necessitates for inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-

surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains, especially in the area of 3D inspection as the importance of 3D defect types increases. In 2011 and also with the change of the scope of the subchapter to *Characterization, Inspection and Analysis a new key challenge was identified: Detection of organic contamination on surfaces* – The detection and speciation of non-volatile organics on surfaces is currently not possible in the fab. There is no laboratory or fab scale instrumentation available or implemented.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- Process Stability versus Absolute Contamination Level
- Wafer Edge, Backside and Bevel Monitoring and Contamination Control
- Development of sub 10 nm water and chemical liquid particle counter
- Correlation Yield and Contamination Levels

In 2011 the identification of Non-Visual Defects and Process Variations was set to the most important key challenge in the future. Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

Furthermore, in the long term the following key challenges were identified:

- In-line Defect Characterization and Analysis
- Next generation lithography

Table YE2 Yield Enhancement Difficult Challenges

Difficult Challenges 2013-2020	*Summary of Issues*
It is a challenge to detect multiple killer defect types and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects.	• Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. • Reduction of inspection costs and increase of throughput is crucial in view of CoO. • Detection of line roughness due to process variation. • Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. • Reduction of background noise from detection units and samples to improve the sensitivity of systems. • Improvement of signal to noise ratio to delineate defect from process variation. • Where does process variation stop and defect start?

Table YE2 Yield Enhancement Difficult Challenges

Difficult Challenges 2013-2020	*Summary of Issues*
Process Stability vs. Absolute Contamination Level – This includes the correlation to yield test structures, methods and data that are needed for correlating defects caused by wafer environment and handling to yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	• Systematic Mechanisms Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and the manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the numbers of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. • Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic loss, and has to improve their coverage. • Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product. • Relative importance of different contaminants to wafer yield. • Define a standard test for yield/parametric effect. • A possible work around is the use of NEXAF at a synchrotron radiation facility.
Difficult Challenges Beyond 2020	***Summary of Issues***
Next Generation Inspection – As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This assessment should include each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.	• Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.
In-line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	• Data volume + quality: strong increase of data volume due to miniaturization • The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. • It will be recommended to supply information on chemical state and bonding especially of organics. • Small volume technique adapted to the scales of technology generations. • Capability to distinguish between the particle and the substrate signal.
Next generation lithography – Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.	

2.1. Wafer Environmental Contamination Control

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table YE3.

Table YE3 Technology Requirements for Wafer Environmental Contamination Control

Wafer environment control—The wafer environment control includes the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in PODs/FOUPs. As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, high capture rate, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport

and store wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. All carriers and enclosure materials must meet factory one specifications. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to an effective wafer and reticle isolation deployment.

Airborne molecular contamination (AMC)—Outgassing from materials of construction in the cleanroom, wafer processing equipment, post processed wafers, and wafer environmental enclosures as well as inadequate exhaust and fugitive emissions from chemicals used in wafer processing are the main sources of AMC. Only in some highly congested areas, makeup air is a significant yet temporarily important source for AMC. Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO, O3) can also be considered as part of the AMC burden. Acid vapors in the air have been linked to corrosion, as well as with the release of boron from HEPA filters. The impact of amines on deep ultraviolet (DUV) photoresists are well known examples of AMC affecting wafer processing. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front-end processes. Other areas of concerns for AMC are IPA from semiconductor cleaning equipment and corrosion when Cu is exposed. The impact of AMC on wafer processing can only be expected to become more deleterious. This is not only driven by device dimensions decreasing but also by the introduction of new chemistry and recipes for future technical nodes that exhibit new defect schemes. Besides AMC creating defects to the wafer surface or bulk material Yield Enhancement group engages on defects or shortfalls in productivity that originate from the impact of AMC to production tools as reticles, metrology or exposure tools. AMC is in many cases - as for excursions - a highly dynamic phenomenon. AMC control deals mainly with prevention of AMC release for which a tight source control is mandatory. There is clearly a need for better AMC monitoring instrumentation in the clean room to measure AMC at the part per trillion level (by volume) in real time. Surface acoustic wave (SAW) devices and atmospheric pressure ionized mass spectroscopy (APIMS) have been used to measure low level AMC, but a larger variety of on-line methods and instrumentation is needed and expected to be available in the future, see also the link for *AMC monitoring programs.* Table YE4 and YE4a provide more detail for AMC monitoring and on-line methods.

Table YE4 AMC Monitoring Methods

Table YE4a Supporting Table for On-line Methods

Numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures. Beyond proper material choice the need for pumping and nitrogen purging of wafer environment enclosures is further investigated for critical process steps to diminish cross-over of contamination from different process steps by FOUPs. The potential for AMC to impact new processes should be considered in all process integration studies.

While not specifically mentioned, charged defects are also an area of concern where ion control is critical in areas such as Lithography particularly EUV. Wafer charging must also be managed to avoid attracting charged particles to the wafer.

This is specifically true where disruptive, revolutionary techniques are introduced into the manufacturing chain. For example, future lithography systems require vacuum processing and are not expected to impose new AMC control requirements in the clean room environment. However new challenge compounds are identified for the tool interior that may require novel air and purge gas treatments.

A detailed definition of critical impurities is provided at this link: *AMC definitions.*

Temperature and humidity specifications have been added to Table YE3 this year for the most critical applications, *e.g.*, lithography for several reasons.

1) The strictest requirements are driven by the lithography process, which is protected by an environmental chamber. The specifications in the Table YE3 reflect the inlet condition to each individual environmental chamber. Here especially, the maximum variation over time is important, which the environmental chamber must be able to compensate. At the POP lower specifications down to ± 0.03° K are maintained.

2) But also in the coater/developer track temperature and humidity specifications must be guaranteed to maintain stable conditions for the resist.
3) The temperature variation is also important for the stepper itself, since minor temperature variations can result due to different thermal extension coefficients in misalignments between the stepper foundation/wafer stage and the lens column. Steppers need up to a week to stabilize after a temperature change.
4) Another critical requirement is driven by metrology equipment which depend either on laser beams (the air density depend on temperature and humidity) and by measurements where misalignments are important.

The temperature and humidity stability over different locations within critical areas is less important. Also in other areas temperature and humidity variations shall be controlled to less strict limits since it may have an impact on the surface (native oxide formation) or alignments. Some companies choose not to have different specifications for critical and non-critical areas to allow flexibility in the cleanroom use as well as simplify the temperature and humidity control and the associated segregation.

These specifications are variational specifications and set points can be chosen in a wide range. A recent benchmarking study between fabs has shown values between 19.5 and 24°C for temperature and values between 35% and 48% for the relative humidity. There are different drivers for establishing environmental conditions. The temperature set point is normally chosen based on comfort level and climatic conditions and the resulting energy consumption. The set point for relative humidity takes into consideration higher electrostatic charges at lower humidity and higher corrosion/native oxide formation at higher relative humidity. Capacity of AMC filters also depends on the humidity.

Another process area with temperature/humidity control as well as AMC control requirements is the location of the lithography excimer lasers, if they are installed in the subfab and not in the main cleanroom.

2.1.1. TABLE YE3 STRUCTURAL CHANGES FOR 2013

The revision of Table YE3 is taking into account the immediate wafer and masks environment and enclosures (FOUPs, reticle Pods). The revision aligns the table structure and content with actual manufacturing concepts involving clean room control, high purity storage environments as (bare) wafer and mask stockers and enclosures. Each process segment listed is split into information that is referring to the clean room ambient conditions and limits that are referring to the interior environment and atmosphere of FOUPs, reticle Pods or bare material storage environment. Clean room ambient conditions are regarded as POE conditions to critical process steps that may involve further tool related measures of AMC protection and reduction, yet require controlled entry conditions to achieve proper process control. FOUP and reticle Pods interior limits are not only influenced by clean room environmental contamination but are depending heavily on remaining active material outgassing or re-evaporation of AMC attached to the containment walls. Other structure changes are as follows:

- For reasons of transparency and comparability process limits for clean room environment and containments (FOUPs and reticle Pods) are posted side-by-side per process.
- The revision of AMC limits in Table YE3 performed in 2011 has been based on a structured investigation and inquiry process that involved front-end manufacturing companies, institutes and academia, and included their published information on defects and yield.
- The deduced tabulated recommendations for AMC limits consider integrated concepts of clean room limits and wafer/reticle environment limits at actual standard sit times or operation and service times for materials and tools that are regarded as acceptable under yield requirements and factory integration processes.

Example of Tabulated Values in Table YE3:

Gate/Furnace Area Wafer Environment (Cleanroom FOUP Ambient/Tool Ambient)	
Total Metals [A] (E+10)	< 10 atm/cm^2/week
Dopants [B] (E+10, front end of line only)	< 10 atm/cm^2/week
Volatile Organics (w/ CGMS retention times ≥ benzene, calibrated to hexadecane) [C]	20,000
Gate/Furnace Area Wafer Environment (FOUP Inside)	
Total Metals [A] (E+10)	< 0.5 atm/cm^2
Dopants [B] (E+10, front end of line only)	< 0.5 atm/cm^2
Volatile Organics (w/ CGMS retention times ≥ benzene, calibrated to hexadecane) [C]	20,000
SMC organics on wafers, ng/cm^2/day [D]	NA
Total SM on wafer, E+10 atoms/cm^2/day	< 0.5 atm/cm^2

SMC--surface molecular condensable, SM--surface metals

[A] Detection of metals at the levels indicated will be dependent on sampling time and flow rate. Sticking Coefficients vary widely for metals. It is generally believed that Cu has a sticking coefficient 10x of other metals, and therefore the guideline for Cu could be lower.

[B] Includes P, B, As, Sb

[C] Ideally, continuous monitoring using online instrumentation would be preferred when practical since this can give both long term averages and catch excursions. When online monitoring is not available, an average grab sample for at least 4 hours, and not more than 24 hours is recommended, to get an average, increase sensitivity of the analysis, and avoid short term transient effects

[D] SMC Organics: Single wafer shall be oxidized to make organic-free, then wafer shall be exposed for 24 hours and top side analyzed by TD-GC-MS with 400°C thermal desorption, and quantitation based on hexadecane external standard. TIC response factor per SEMI MF 1982-1103 (formerly ASTM 1982-99).[4] Limits determined by above method are a guideline for many organics. Note higher limits can be used for process wafers oxidized or cleaned prior to subsequent process step. Processes such as gate oxide formation, or polysilicon deposition, may be more sensitive to organics, especially high boilers such as DOP. Silicon nitride nucleation may also be more sensitive than above for some processes. Please note dopants requirement is covered in earlier section. Contamination levels are time based, and samples should be exposed for a weeks time for better sensitivity; ng/cm2/week. Total contamination level on reticles that cause problems also vary with energy exposure. These guidelines subject to change with new data currently being generated.

The structure and tabulated values in Table YE3 (process segment Furnace/thermal treatment): AMC limits for clean room ambient environmental control are listed side-by-side with AMC limits recommended for the wafer environment inside FOUPs. Tabulated values are derived from front-end manufacturing defect analysis and scientific work of academia.

New line item in Table YE3: Moisture: In order to reflect the impact of moisture to the wafer- and reticle environment, moisture has been introduced as additional line item to Table YE3, starting with “exposed copper”.

2.1.2. New AMC Topics Related to Factory Integration (AMC Integrated Concept)

The FOUP is a plastic container that stores and carry 25 wafers from tool to tool. During storage, wafers may outgas chemicals and by-products of previous processes inside the FOUPs. As a consequence, the concentration of some critical AMC inside FOUPs may be higher than inside the cleanroom by several orders of magnitude.

The FOUP itself may be a source of contamination because of residues from its own manufacturing process, and also because it can trap AMC coming from contaminated wafers which will then be further outgassed. The defects due to AMC are a result of a combination of critical contamination inside the FOUP, type of substrate and storage time. Some defects are also linked with humidity and temperature conditions. As a result, the measurement and control of the contamination inside FOUPs are key challenges for the IDMs and foundries.

Witness wafers have been used to link surface molecular contaminant (SMC) concentrations to specific defects. The surface concentrations are usually expressed in a maximum allowable number of molecules/cm^2. Sticking coefficients (s) for different molecules are found in the literature and help us to relate SMC to AMC concentrations in the air. AMC concentrations which will generate surface defects on the wafer are also depending on time of exposure at a given humidity and temperature. The general formula relating SMC to AMC is as follows: $C = N / (s \times V \times t)$, where C is the AMC concentration in the air, N the SMC concentration on the wafer, s the sticking coefficient, V the mean speed of the AMC and t the exposure time. The YE3 table is reporting recommended AMC concentrations in ppt(v) for 24 hours exposure time inside FOUPs. For lower exposure times, new AMC values can be calculated using the formula above. A simple consequence is that the allowable concentrations in air are higher for shorter exposures (linear relationship

according to this equation). Sticking coefficient are not strictly constant for different exposure times and the approach above only represent a simplified version of a more advanced theory using the kinetic laws of contamination (more details can be found in the literature).

The Yield Enhancement group has been working on the different issues related to FOUP contamination and therefore proposes a new table describing the potential solutions. Factory Integration is dealing with the whole process flow including: cycle time, q-time constraints, layout and consumption. As a consequence the integration of the measurement and control of contamination inside FOUPs was handled as a common project between YE and FI. In the frame of this common work, Factory Integration has the role to evaluate the validity of each solution in regards to cycle time and throughput. FOUP cleaning is increasingly more important to mitigate the FOUP contamination particularly from pores due to outgassing from the wafers. This can be mitigated by using a FOUP with lower porosity and more frequent FOUP swap and subsequently cleaning the FOUP before reintroduction into production.

In 2011, YE defined the potential solutions for the following 3 main topics:

- - Outgassing of new FOUP
- - Outgassing of “in production“ FOUP
- - Cross-contamination on wafers inside FOUP

2.1.3. NEW AMC TOPICS RELATED TO 450 MM

There are several considerations for critical contamination control specifications (CCCS) for the clean room environment and wafer environment in 450 mm wafer sub 1× nm technical node high volume manufacturing.

A transition in production from 300 mm wafer substrate to 450 mm diameter substrates is driven by output per wafer and time and therefore by cost. Yield loss would affect the overall output of the 450 mm production line which is subjected to be more productive than current 300 mm lines. Consequently this would affect the return on investment (ROI) on 450 mm investments which are right now assumed to be wafer diameter specific and therefore comparatively massive.

Critical contamination control specifications for the wafer level have to be put forward as projections for 450 mm wafer size together with the sub 1× nm node. Current know-how and information on wafer processing speed, wafer defect budget, handling modes and foreseeable fab space structure have to be taken into account. From this information CCCS for the clean room environment and the wafer environment need to be derived.

Contamination control specifications for the production of sub 1× nm structured chips products on 450 mm wafers experience in some parts influences that come with the technical node and materials used. Other parts are influenced by the projected influences from wafer size and possible countermeasures.

Based on know-how from current 300 mm high volume manufacturing (HVM) at 28 nm node in some segments, conservative, steady projections of the requirements can be proposed for specification. Such steady specification for the clean room environmental level can often only be maintained due to permanent technical improvements and active contamination control (counter) measures on the tool level. Such examples for foreseeable unchanged specifications on the clean room level are the specifications for the following:

Vibration—The mere increase in wafer size would pose significant challenges with regard to wafer handling due to higher masses of tool structures, lower stiffness and an unwanted reduction in resonance frequency. This shift – if not actively addressed – could increase the risk of coupling of natural background into the tool operation. Yet the actual perspective is that 450 mm production could further be possible in clean rooms respecting vibration class VC-D supported by active vibration control on tool-level

Particle cleanliness—Despites the model-related shrinking of the critical particle diameter together the shrinking of the line structures there is little evidence that significant tighter requirements for particle cleanliness in the clean room environment (class 4 or class 5 to ISO 14644-1) or mini-environments (class 1 to ISO 14644-1) would come along with the introduction of 450 mm wafers. Uncertainties exist based on the expected broad implementation of FOUP purge with XCDA or dry nitrogen that could enhance ESA (electrostatic attraction) based on increased surface charges.

For two contamination categories tighter specifications are foreseeable which are mainly due to the technological node expected on the onset of 450 mm production

ESD—The requirements to prevent ESD (Electrostatic discharge) induced defects will get more stringent with reduced line width but are supported by active countermeasures on the tool side

EMI—It can be expected that EMI (Electromagnetic interference) will gain more attention and may need enhanced preventive action. This is mainly related to the expectation that for sub 1x nm node both e-beam and TEMS may become production relevant tools thus requiring that standard production floor space may be capable to accommodate such EMI-sensitive tools

AMC—In the case of AMC (Airborne molecular Contamination) an alignment of requirements for various tools sharing the same fab space and experiencing the same threat to wafer yield should result in a simplification of the contamination control model and a higher ability to achieve yield safely. Currently AMC control strategies for the different processes vary widely based on the preparedness or unpreparedness of the tools for non-ideal contamination situations of the clean room environment. This leads to relaxed clean room environmental standards in case tools come with a well-defined AMC protective interface and stringent requirements if the tools arrives unprepared creating either a demand to adapt the clean room condition or the minienvironments conditions.

Considering that AMC effects to wafers do generally not originate from concentrations but form doses related to sit-times the migration to 450 mm wafers can have an impact on the contamination burden if processing speed would not scale up proportional to wafer size. Currently the WECC group would expect this effect to be most pronounced for metrology tools. The progress on processing speed needs to be monitored to decide whether AMC control limits for WECC would need scaling in the coming years due to the wafer size effect.

2.1.4. NEW AMC TOPICS RELATED TO INTERACTIONS OF AIR IONIZERS WITH AMC

Air ionizers may be used to neutralize charge to prevent electrostatic discharge damage and electrostatic particle attraction to wafer or masks.

The hot tip and ions formed can interact with AMC that have Si, S, P, B, Cl, Sn or other selected elements to make nm particles such as oxides, and larger deposits on the tips, that can throw the ionizer out of balance or lead to ionizer faults. While presumably rare, if this happens, the deposits calls attention to the unusual presence of specific AMC's that can react with excess energy to not only deposit onto ionizer tips, but possibly onto other surfaces, due to interaction with excess energy such as 193nm lithography, lasers and inspection tools or hot surfaces. The compounds might degrade optics, masks, scanners, or other surfaces. Analysis of the ionizer tip deposits can indicate what elements are present in air, aiding selection of methods to look for possible sources of a limited number of contaminants, instead of large sections of the periodic table. This method can be used to more rapidly find some AMC issues for which no other test are currently available, such as sub-ppbv leaks of some hydrides, silicones, silanols, halogens, organometallics, OCS, TEOS, organophosphates, etc.

Process critical materials—Additional experimental investigation is required to support our understanding of impurity specifications in novel materials, such as Cu plating solutions, CMP slurries, or chemical vapor deposition (CVD) precursors to high/low-κ dielectrics and other thin film materials. For many years the critical particle size concept was used to judge whether particles will have an impact on yield or not. This concept has to be rethought since particles do not impact the process yield alone by their physical size but also by their chemical composition. The allowable particle concentration thereby depend also on product parameters such as cell size and have therefore been aligned with the particle concentration on the surface as derived by the Front End Processes (FEP) TWG surface preparation group calculation model.

Ultrapure water—UPW is purified water with most of the quality parameters below or near their detection limits of the most advanced metrology. Specific definitions of the water quality requirements to enable future technology are presented in the Table YE3. Particle levels are reduced using the best available ultra-filtration technology, but today's particle counting technology is not capable of measuring particles at the critical node size**.**

It is important to remind that the roadmap is focused on technology enabling, identifying the parameters that require new technologies for monitoring and control. For the practical purposes, SEMI F063 provides a guide that can be used as a reference specification for the UPW quality in design and operation of advanced semiconductor processes, considering feasibility of the existing technologies. More stringent criteria beyond 2013 are only projected where there is evidence that manufacturing process requirements demand improvements. UPW is generally the cleanest fluid available in the manufacturing process. As such there is not much data to suggest that it is has a significant negative impact on process yields. For this reason the UPW Roadmap is relatively stable over time. Over the past several years the UPW and Chemical groups have worked closely together to develop a failure mode and effect analysis to evaluate the risk of known contaminants of the wafer. *A discussion of the UPW requirements can be found in the UPW supplemental material online.*

The UPW section of Table YE3 considers some parameters as process variables rather than contaminants. It is clear that the stability of the wafer environment can be as important as the level of contaminants present for some parameters. Some semiconductor manufactures treat dissolved oxygen (DO) in this way, while others consider it a contaminant Stability of temperature and pressure continue to be important, the former being critically important for immersion lithography.

For 2013 some non-critical parameters such as resistivity and bacteria are to be removed from the table, as they are only used for operational functionality of the UPW system but do not affect future technology device yield or defects. These parameters are critical for the water quality, but non-critical for the technology enabling. Bacteria can be controlled down to zero level and the resistivity became non-sensitive to the water quality variation within the ranges allowed for the ionic species in UPW.

The focus will turn more to critical parameters such as particles, metals, and organic compounds. Particles remain a high risk and critical for future technology enabling. On-line metrology for particles in liquid does not address killer particle size, and therefore, filtration efficiency for killer particles is not completely known.

The 2013 edition includes specifically a category for the particles in EUV mask operation. This is to emphasize the particular importance of the particle control in this area. Electrically active particles (mostly metallic) are considered more critical than electrically non-active particles, therefore the UPW team will work closely with FEP to define the risks and potential solutions. It is expected that electrically active particles will have smaller critical size than electrically non-active, which will remain ½ node. Colloidal silica particles may carry metal atoms and as such become more critical. As a work around to the particle metrology gap, the UPW forum has worked with SEMI to develop a filter performance validation standard (SEMI C079) as a risk mitigation measure. We are continuing to investigate selective defect density in the critical areas that require better understanding. This includes particle deposition modeling based on a thorough literature review. Literature survey information on the particle deposition is available in additional information documents.

2.1.5. METAL CONTAMINATION IN UPW

The UPW team is currently reviewing previous the definition of critical metal concentration of 1ppt and non-critical metals as 10 ppt). This is based on the fact the concentration of metal on the wafer is function of UPW concentration and deposition ability' Instead we are considering defining the UPW spec based on device impact (XE+Y at/cm2) and deposition as a function of metal concentration in the bulk liquid. We propose to define the spec based on the device impact as related to the deposition efficiency. We plan to consider detection risk for FMEA in terms of troubleshooting only. The FMEA will remain unchanged and will be included in *supplementary materials*.

2.1.6. ORGANIC CONTAMINATION IN UPW

There has been an increased interest in the past few years to understand how organic contamination of UPW may affect semiconductor devices. In the past organic contamination was measured in terms of its total organic carbon content or TOC. This measurement of the organic content does not account for the type of organic and how it may react with various wafer surfaces or how the reaction may impact device yield. As a result of this, the ITRS UPW team removed TOC from the table in the 2012 publication. In place of TOC we are now categorizing organic compounds in UPW based on the ability to form polar bonds with the various wafer surfaces. Immersion lithography lens hazing was previously a driver of UPW TOC<1.0ppb.

The 2013 Yield roadmap has added a separate line for immersion litho TOC (<1.0 ppb), implying that this may be required as POU definition, while the rest of the water quality spec was relaxed to 3 ppb of non-critical organics. We continue working on a new definition of critical organics, based polar strength as quantified using boiling point. The definition of the critical organics was included in the table notes, which recommend end users to consider characterization of the UPW organics in their own specs. New metrology is needed for on-line detection of the critical organics.

- Critical Organics – non-volatile polar organic compounds with boiling point > 200C
    - Critical organic compounds should be controlled to < 1 ppb
    - Organic compounds are categorized as critical with respect to its ability to form a hydrogen bond with any oxide surfaces including gate, tunnel, or native oxide
    - Total organic compounds should be controlled to < 3 ppb
    - Non- Polar Organics - have very little attractive strength to have any direct device impact. Non-polar organics may adhere to a hydrophobic wafer surface as foreign material (FM) via VanderWaals forces which are relatively weak and are easily removed in chemical cleans.
- Critical carbon atoms on wafer related to TOC in bulk fluid

- Defined by FEP as 1xE-^{12} atoms/cm^2 for Si-C defect in furnace
- Critical boiling point of organic compounds defined by FEP as 200°C
- We are looking at compounds with boiling points lower than 200°C that may be related to other defects such as deposition

There is evidence that oxide layers in semiconductor devices such as native oxide, gate oxide, and tunnel oxide can be affected by the presence of polar organic compounds in UPW which contain hydroxyl (-OH) groups forming hydrogen bonds with the oxide layer. The presence of organics on the oxide layers can lead to poor adhesion of the resist and can cause undercutting during the wet etching process. This can create oversized vias which can cause adjacent metal lines to become short-circuited.

We continue to use failure mode effects analysis (FMEA) approach to determine the overall risk of each subgroup to the wafer manufacturing process. In 2013 the UPW team completed an organic speciation benchmarking study which used LC-OCD analysis to speciate organic compounds in UPW used at 10 manufacturing sites. This information is available as *supporting documents* and will give us baseline data to identify typical organic compounds in semiconductor UPW systems and can be used for occurrence risk factor in the FMEA review.

It is critical that further experimental analysis is completed in the next few years to determine the correlation between failures in the semiconductor devices and level/type of organic contaminant. Research will continue in 2014 to investigate this further.

UPW measurement methodologies—General test methodologies for monitoring contaminants in UPW are indicated in the Figure YE2 below. Over the past few years the ITRS UPW team has benchmarked many advanced UPW systems to determine water quality. Past benchmark efforts have identified the inadequacy of some measurement methodologies to quantify contaminants in UPW. The following analytical methods are not sensitive to present levels of contamination in UPW: resistivity, total organic carbon, inorganic anions, and organic ions, as well as some organic species. Speciation of organics has been limited by these methods. Sensitivity of the following methods is presently adequate: viable bacteria, dissolved gasses, and metals. While particle measurement is not adequately sensitive to validate quality at the critical dimension it continues to be a valuable tool to detect filtration failures.

Parameter	*Measured (POD/POC)*	*Test Method*
TOC	*Online*	*Conductivity/CO_2*
Organic ions	*Lab*	*Ion chromatography*
Other organics	*Lab*	*LC-MS, GC-MS, LC-OCD*
Total silica	*Lab*	*ICP-MS or GFAAS*
Particle monitoring	*Online*	*Light scatter*
Particle count	*Lab*	*SEM—capture filter at various pore sizes*
Cations, anions, metals	*Lab*	*Ion chromatography, ICP-MS*
Dissolved O_2	*Online*	*Electric cell*
Dissolved N_2	*Online*	*Electric cell*

ES TOF—Electro spray time of flight
ICP-MS—inductively coupled plasma mass spectrometry
GFAAS—graphite furnace atomic absorption spectrometry

Figure YE2 General Test Methodology for Ultrapure Water

UPW and liquid chemicals particle measurement—Problem Definition and Goals: The sensitivity limit of particle counters for UPW and liquid chemicals has not kept pace with decreases in the critical particle size (the size of particles which are thought to be detrimental to wafer yield). Although this concept needs to be discussed again since particles not only impact yield because of their physical dimensions, but even more by the chemical composition, e.g., as spot Fe contamination, the fact remains the same. It is important to measure even smaller particles than we can do today. Measurements of these nanoparticles are made difficult by the low scattering efficiency of them. Low particle concentrations and small sample volumes of current particle monitors can result in large sample-to-sample variability. More sensitive particle measurement methodology with adequate measurement statistics is needed to meet projected purity goals.

2.1.7. The Sensitivity Problem

As of 2013, the highest sensitivity particles counter commercially available for both UPW and liquid chemicals is 0.03 microns. Experiments have shown that small particles may even deposit preferentially [M. Knotter] and therefore the impact is increased even further. Past improvements in particle counter sensitivity for UPW have been accomplished by increases in laser power. While improvements in sensitivity for liquid chemical particle counters are viable, further sensitivity improvements for UPW using this approach are unlikely, due to the significant cost implications. In addition, high-cost solutions do not necessarily guarantee a production-worthy metrology tool. High initial expense coupled with increased cost of ownership impact the viability of higher sensitivity instruments. To estimate the concentration of smaller particles currently an extrapolation assumes a $1/d^3$ relationship between particle counts and particle size in liquid chemicals. The further away the particle size of interest gets from actual measurement capabilities, the higher the potential for error-error being defined as the difference in the projected value to the true value. Moreover, the power law coefficient may be significantly affected by the actual filtration capability of the final filters used upstream to the particle measurement, making projections impossible. Therefore, it is important for the industry to develop a more sensitive method that can measure particle concentrations at greater sensitivity to validate the particle count versus particle size relationship so that the relationship can continue to be reliably used. Further discussion is needed on validity of the power law extrapolation, e.g., effect of filtration on extrapolation (filter rating/detection size).

2.1.8. The Measurement Precision Problem:

Statistical process control is increasingly being used to monitor the consistency of process parameters. Process variation of fluid purity can be as critical to wafer yield as the absolute purity of the fluids. Therefore, it is important that measurement methods detect sufficient number of events to ensure confidence in measured particle concentrations. Development of other statistically significant particle counting methods or a higher sample volume particle counter is needed to improve confidence in reported particle counts. The sample volume (volume of fluid measured) will determine the number of particle counts that are detected during the sample interval. Follow this link for *more details on particle monitoring*.

Although the gas/liquid chemical section of Table YE3 shows an essentially flat purity trend, there is likelihood that specific process steps may require higher purity. In some cases, yield improvements may be achieved more by reducing variations in purity than by reduction of average contamination levels. Hence, there is a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials, In 2008, Semi .released the results of a comprehensive effort to create a standard set of guidelines for defining “in control” specialty gases [1]. A coincident effort by several large semiconductor manufacturers began for the purchase of selected specialty gases. Although the number of companies that have started utilizing in control guidelines for the purchase of consumable raw materials has increased, along with the breadth of the offering for in control materials, however, the industry has not yet settled on one standard set of criteria.

Overview for gases and liquid chemicals—The recommended contaminant values for gases and chemicals in Table YE3 represent typical gas/liquid chemical quality requirements at the point of entry to the process tool (POE) for the more demanding manufacturing processes in the roadmap. In many applications, the requirements for the contaminants in these gases and/or liquid chemicals may be relaxed as dictated by the specific process requirements. On the other hand, some manufacturers have claimed benefits from lower contaminant levels. Considering that a given process can be run successfully within a “window” defined by a range of material purity and also by ranges in other parameters (purging time, etc.), it follows that, in practice, trade-offs exist between imposed purity requirements, process throughput, etc. Pushing a process to the upper limit of its “purity window” may require significant investment of time and effort in optimizing other parameters, and the economics of pursuing that effort will depend on the environment. It may also be that benefits attributed to low contaminant levels are more attributable to the reduction in contaminant variations achieved with high-purity process gases and chemicals. This topic is addressed in more detail below regarding the push for the adoption of statistical process control, SPC, for specifying process fluid purity.

There are three primary sources of process environment contamination: One is the impurities in the process materials as supplied. The second is the delivery system or the process itself. The third is decomposition, which may be caused thermally or by reaction with adventitious contaminants e.g., moisture. These contamination sources are found throughout the pathway from the delivered gas or chemical to the wafer surface. Table YE1 describes the several interfacial points of process materials with equipment found along these paths and associates them with the various TWGs within the ITRS and other organizations such as SEMI that focuses on them. This helps to clarify the relationship of these organizations with the WECC while also removing ambiguity about the definition of various points along the process path.

While purity measurements at the Point of Process, POP (that is, in the processing chamber itself), would provide the most direct correlation between gas or liquid quality and process performance, these measurements are often very difficult to obtain with the exception of certain fluid properties in wafer immersion baths. Examples include both particulate generation during plasma processes and wafer out gassing. The latter is the most important source of water vapor contamination in many processes, often obscuring moisture contributions from the process fluid. Measurements at the POU provide the most direct information of the quality of process fluids going directly into the process chamber, but these are also not available for many of the common processes.

Because of these difficulties, the values in Table YE3 are intended to represent those at the Point of Entry, POE, defined as the inlet to the process tool as described in Table YE1. There are sufficient measurement data on bulk gases and aqueous fluids to provide guidance with regard to POE impurity levels for many applications, although measurements on these fluids are often performed at the POS, POD, or POC. For these materials, which are relatively unreactive and delivered in large volume, the extrapolation to POE is generally very reasonable. In the case of Specialty Gases and other reactive process fluids, such extrapolation is more delicate because delivered volumes are smaller, increasing sensitivity to contamination effects, and degradation in the distribution system related to materials of construction, atmospheric contamination, thermal degradation, etc. is more likely. These factors are minimized with normal best construction and operations practices, and therefore the best guidance available is often regarding POS specification and to a lesser extent POD or POC measurements, which are interpreted as equivalent to POE. In summary, while the intention is to recommend POE purity levels for all gases and liquids, in practice, the supporting data has more often been collected at POS, POD, or POC.

The targeted levels can be reached either by bulk delivery of a fluid with requisite purity or through use of a local purification/filtration. Care should be taken, at a minimum, to maintain the quality of the gas coming from the source, ensuring that contamination is not added downstream of the POS, as may occur due to particle generation at components, moisture out gassing, byproduct generation due to incompatible materials, etc. Particle filtration as close to the POU as possible is generally advisable for gases. For the most critical applications a local purifier may be used to enhance or ensure ultimate purity at the POU. In those cases, the prevailing approach is to seek POC levels that are adequate for the process and to view the purifier as “insurance.” The challenge to the purifier is minimal, and long purifier lifetimes can normally be expected.

An important exception to this guidance is for some specialty materials that undergo a variation in composition as they are distilled from the cylinder or other delivery vessel in a bulk vapor delivery set up. Anhydrous HCl for example is known to form very stable hydrates with water that results in concentration in the water content in the cylinder as the original specified contents are removed [2]. In this case a combination of rigid specifications on how much of the contents can be used before moisture becomes unacceptable and the application of moisture gettering purification devices somewhere in the vapor transport path. Liquid anhydrous ammonia are another specialty gas with this potential issue [3], Within the realm of relatively volatile liquids that are delivered in bulk, i.e., not by direct liquid injection, volatilization,, aqueous hydrogen peroxide, aqueous ammonia and likely many of the amide based CVD/ALD precursors are expected to undergo similar distillative variation and/or thermal degradation under delivery conditions [4], Depending upon the process sensitivity this might be a source of poor film quality or process variability that can be addressed by attention to the delivery method or the application of POUP .

Point of use purifiers and filtration units are finding application in newer atomic layer deposition techniques, ALD, for example where the films are deposited by the monolayer and incorporated impurities can be especially destructive. A near/medium term challenge is filtration of the precursor vapor. The sources can be sublimable solids or readily condensable vapors of low volatility liquids. These can resolidify or reliquify causing plugging and instability in fluid transfer to the substrate surface.   In addition, these vapor delivery systems are typically low pressure (< 100 Torr) which can change the fluid dynamics and hence filtration efficiency dramatically. One additional limitation with the POUP systems in particular is endpoint monitoring to determine when the purifier matrix is exhausted. Practically this is handled by routine change out of the purifier units at a frequency that typically results in no problems.

Specific purity challenges will be discussed below, but generally there is little objective evidence to suggest that the purity levels listed in Table YE3 are not suitable for multiple generations of semiconductor manufacturing. Yield improvements are expected to be achieved by reducing variations in purity. Statistical process control (SPC) on incoming materials will reduce variation at the POS. Inconsistencies at the POU may remain due to variations in downstream contributions, e.g., when the flow in a distribution system is decreased, moisture contamination due to out gassing tends to increase. Elimination of these variations may again require purification at the appropriate point (e.g., POU purification, POUP).

Bulk and Specialty Gases—The major bulk gases are listed separately in Table YE3. The 2007 roadmap had indicated an increase in purity requirements post 45 nm. This type of improvement might be anticipated, based upon historical trends as design rules tightened, but there is again little objective evidence to support the need for improvements across the range of bulk gases. Informal poling of several large semiconductor manufacturing organizations suggests that an increase above current purity requirements for the majority of bulk gases is not necessary to meet post 45 nm design rule manufacturing. For very special applications where extraordinarily higher purities are critical, special purity grades or additional purification will be required. As exemplified above, downstream POUP might also be utilized as an additional means of removing variability in POS gases. Therefore, Table YE3 has been modified from 2005 to remove many of the step improvements scheduled for future manufacturing nodes except where specific information has been identified to justify the change.

The situation is similar for many of the Specialty Gases, although several additional categories of applications have been added to better identify needs for specific processes, *e.g.*, etch, deposition, doping and laser applications. Like the Bulk gases, the values in Table YE3 have been left at current levels, unless an objective justification for increased purity can be identified. Although changes to the current Table YE3 values for gases are small, the introduction of so many new materials and the process innovations required to meet future design rules, *e.g.*, atomic layer deposition, will require close monitoring. More details with regard to bulk and specialty gases are provided in the gas supplemental documents.

The 2005 roadmap identified the growing need for statistical process control for process gases and liquids. Several companies have begun requesting materials with specifications related to the statistical control of variability of the materials, but there are no standards accepted across the industry that define the SPC process. Currently there is a Semi sponsored task force, composed of representatives from the end user and supplier communities that is creating a common set of characteristics for defining "in control" specifications for gases and liquids.

The promise of providing "in control" process fluids is anticipated to improve process yields by either minimizing the overall variability of the manufacturing process or in simply reducing the likelihood of a process crash resulting from large variations in material quality that would still nominally have met a more standard specification.

An informal survey of several large semiconductor manufacturing companies on their implementation of statistical process control requirements for their bulk and specialty gas purchases indicates that SPC processes are already being applied to many of the materials utilized in manufacturing, or will be shortly. However, the criteria that form the basis of "in control" varies substantially. Survey responses suggest that customer expectation is that the application of process control for the preparation of POS materials will improve their semiconductor manufacturing process stability and are critical for high yield manufacturing. Initial implementation, will likely focus on specialty gases that exhibit the greatest potential for causing semiconductor process variability, *e.g.*, anhydrous HCl but will be used on new and existing products for both memory and microprocessors.

Liquid chemicals—Table YE3 summarizes the purity requirements for liquid chemicals delivered to process tools. Pre-diffusion cleaning and EUV mask blank cleaning requirements drive the most aggressive impurity levels. Liquid particle level targets are shown to become purer each technology generation. These target values are derived from the purity requirements on a wafer as calculated by the FEP surface preparation group assuming a linear relationship between the concentration in the liquid and on the wafer. Particle counters currently are capable of measuring only to 40 nm for liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes, but this will be influenced by the level of filtration utilized. Another measurement challenge for several chemicals is the differentiation between particles and bubbles, which is currently not possible.

The ability to accurately analyze organic, anion, and cation contamination in process chemicals is becoming more critical to successful wafer processing. In the supplementary links an ion table and a mixing calculation are provided that show for which chemicals which ions are important and in which chemicals they could actually occur/have been observed. With the increased use of CMP and plating chemicals, there must be a better understanding of purity requirements for the delivered chemicals.

ALD/CVD Precursors: Table YE3 contains information only for very few CVD/ALD precursors. The variety of layers and the respective contaminants is enormous.

Therefore, a link to the *precursor table* is provided. The precursor table provides information by application as to which precursors are potential candidates at different technology generations, and the nature of contamination that can be expected. A major challenge is the development of accelerated yield learning for critical processes that introduce new precursors that will only be used for one or two generations.

Bulk/specialty gases—There were only a few changes to the bulk gas purity requirements. The measurement of organic refractory components at <0.1 ppb is a detect ability challenge for both nitrogen and helium used in lithography applications. The roadmap indicates these areas as orange from 2007 to 2010 because this is at the limit of detection for current analytical methods.

In addition, changes were made to better delineate the need to control Ar as an impurity. The N_2 specification was changed to eliminate Ar as a critical impurity, although it was left in the O_2 specification. Even so, the 50 ppbv limit given in 2005 was raised to an Ar limit of <1000 ppbv. The ongoing requirement in O_2 derives from the potential for uncontrolled Ar impurities to impact plasma etching processes, although typical Ar specifications for O_2 used for etching is more consistent with the <1000 ppbv level.

For some processes, such as advanced lithography, very small quantities of "high molecular weight/high boiling point" (*e.g.*, C_6-C_{30}) hydrocarbons are detrimental because of increased adherence to the exposed surfaces, and potential for photochemical degradation to leave non-volatile residues on lenses, masks, mirrors, etc. However, any organics, even ones with retention times less than C_6 are considered detrimental if they can result in refractory deposits. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities. In order to detect such species with ultimate sensitivity, it is necessary to directly detect the relevant species and calibrate the analyzer with the appropriate standard. The methods used are analogous to those for AMC, such as TD gas chromatography (GC)/mass spectroscopy (MS) (TD = thermal desorption) or TD GC/FID, or ion mobility spectroscopy (IMS). Even these approaches may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks. For methods using adsorbent traps, it is very important to determine the trap efficiency. Using APIMS to provide real time measurement of individual hydrocarbons is possible, in principle, but calibration is difficult, because larger hydrocarbons are collisionally dissociated in the ionization process.

A compromise approach that has gained some acceptance is to use TD GC/MS and sum all peaks corresponding to C_6 and higher. The instrument is usually calibrated with a multi-component standard and results are reported "hexadecane". While the quantization provided by this method is approximate, and some species may be overlooked, it does at least emphasize the heavier hydrocarbons while providing a straightforward calibration.

Applications for both O_2 and H_2 generally tolerate higher levels of N_2 contamination than other contaminants and the table reflects this observation. Requirements for critical clean dry air (CDA), lithography purge gases, and supercritical CO_2 supply are included. Whereas critical CDA may not always be conveniently or cheaply available, there is no technological barrier to its production. Analytical methods are usually the same as used for airborne molecular contamination in clean room air, such as bubbling through ultra pure water (for metals, sulfates, amines, etc.) or trapping on an adsorbent trap for organics. In each case, the sampler concentrates impurities so that requisite sensitivities are achieved when the sample is introduced to the analyzer (ICP-MS or ion chromatography for aqueous samples, GC-MS for desorption of organics). Such methods are time consuming by nature, and direct methods would be preferred if available. However, there is no apparent pressing need for real-time analysis. For SO_2 there are convenient on line methods, *e.g.*, UV fluorescence.

For specialty gases, contaminant values in etchants, dopants, and deposition gases have been expanded in Table YE3 to reflect the increase number of different materials in use, and to better delineate the processes they are used for. Particulate contamination is omitted, since online monitoring of particle concentrations is not commonly practiced and the efficacy of POU particle filters is well established. Whereas there is evidence that the most demanding applications, such as low temperature epi and its cleaning gases, will continue to benefit from improvements in purity as deposition temperatures are lowered, this is expected to be reflected in wider use of the best available purity rather than substantial improvements of those levels.

Tighter control over the variation in purity in both bulk and specialty gases is anticipated to be more important than improvement in absolute purity levels. However, the often more chemically reactive specialty gases present a more formidal challenge for maintaining of POS purity levels throughout the delivery to the point of process. Selected specialty gases, *e.g.*, HCl are also expected to be among the first targeted for statistical process control at the POS.

Novel materials—More detailed consideration of the impurity levels found in the growing number of novel materials used in processing will be increasingly important. Requisite purity levels for critical materials such as novel metal oxides, CMP slurries, low/high k dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied, and many of these materials have not been called out in Table YE3. An early attempt to start to catalogue and characterize the properties of the thin film precursors utilized in semiconductor processing is found in the supplementary material for this chapter.

Deposition precursors for thin film materials are often sensitive to moisture, air and high temperatures. Control over the delivery process from the POS to the reaction chamber is critical to high yielding performance. The use of very high purity carrier and purge gases in these systems are often required to prevent decomposition that can contribute detrimental molecular and particulate impurities. Traditionally bulk purifiers were used in the bulk gas delivery systems to remove particles and other homogeneous chemical contaminations like oxygen, or moisture present in the supply gases. However, with the development and commercial availability of point-of-use (POU) purifiers, there is a strong interest from end users to utilize point-of-use (POU) purifiers particularly for specialty gases needed for critical process steps with very critical level of contamination control. These point-of-use purifiers (POU) are highly effective to remove chemical contaminants to extreme low level (~ ppt), easy to use, easy to replace, with low cost-of-ownership. The capability of placing those point-of-use (POU) purifiers very close to inlet of process chamber, assures least travel path (less contamination) for process gases after chemical purification and filtration.

Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements. Additional detail on the variety of thin film precursors under consideration can be found in Liquid Chemicals section of Table YE3 and the supplementary *precursor table.*

2.2. Characterization, Inspection and Analysis

In 2011 the subchapter was defined to be extended to characterization, inspection and analysis. During the previous years the sub chapter was limited to inspection capabilities. This is facing the demands of nowadays yield enhancement in a broad application as *e.g.* ‘More than Moore’ technologies but also power electronics and mechatronics and MEMS applications. Furthermore, the characterization, inspection and analysis demands of *e.g.* packaging and assembly could be taken into account.

The ability to detect in-line yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production-process research and development, yield ramp, and volume production — broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabrication facilities begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the integrated device manufacturers just in time for each phase of the process cycle. Tools that meet the requirements for process research and development are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate yield ramp must be available several months before production begins. Finally, the ability to monitor excursions at a technology generation is needed when the product hits high yield levels.

Technology requirements are presented by three tables covering the needs for: a) patterned wafer - and e-beam inspection; b) unpatterned wafer inspection, macro and bevel inspection and defect review; and c) Defect Review and Automated Defect Classification (ADC). The complexity of processes and integration schemes for manufacturing of integrated devices requires intense defect inspection for process and tool monitoring. Unpatterned wafer inspection is extensively used for tool qualification. Both defect inspections use subsequent defect review for root cause analysis, posing challenging requirements to the accuracy of defect coordinates. Furthermore, the cleanliness of inspection tools is of increasing importance. Due to the observed impact of defects on wafer bevel and edge on yield, backside and bevel wafer inspection needs a defect review possibility in order to be used to the full extent. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is inspected on e-beam tools which find their application also in detection of small defects.

One of the major challenges is to get to the defect of interest. Therefore, the signal-to-noise ratio is an important criterion for all inspection tools. The more nuisance defects are captured the less valuable the results are as defects of interest might not be recognized even after intense review. Furthermore, an efficient separation of DOI from noise will enable an increased throughput of the subsequent review.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside inspection requirements are based on the Lithography chapter technology requirements table, and also ask for specification of tool cleanliness of the inspection tools themselves, this was introduced

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers, defects that cannot be detected with conventional optical technologies, is emerging with the increased usage of e-beam based

technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and the back end of the process. Macro defects impacting large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved matching the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology generation.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The cost of the investment, fab space occupied, and the throughput of defect detection tools are major contributors to their cost of ownership (CoO). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Tables YE5, YE6, and YE7 have been stipulated on the basis of detecting accurately sized PolyStyrene Latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pits pattern flaws, surface roughness, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

Table YE5 Defect Inspection on Pattern Wafer Technology Requirements

Table YE6 Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements

Table YE7 Defect Review and Automated Defect Classification Technology Requirements

3. Potential Solutions

3.1. Wafer Environmental Contamination Control

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and continue to enable cost-effective high volume manufacturing for device dimensions below 90 nm. Refer to Figures YE3 and YE4. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and

equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Process critical materials—Figure YE4 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities.

In order to accelerate yield enhancement for processes that incorporate new materials, it is very desirable that development studies include purity data as much as is practical. Studies of new materials (*e.g.*, for gate dielectrics) are initially concerned with basic process performance, and later with integration issues. During those stages of development contamination is a relatively minor concern. However, if no information is collected, later yield enhancement efforts proceed with inadequate technical basis. Collecting and reporting both environmental and material contamination data whenever practical will lead to long-term benefits.

UPW—UPW systems meeting specifications do not appear to be large defect drivers for current device geometries. Based on this the Roadmap does not predict that significant changes are required for future geometries. As a Roadmap priority, specific defect mechanisms related to UPW are required to drive significant changes. The current focus is to understand the impact of the tool upon water quality, specifically particles, bacteria, and dissolved gasses, as well as to identify species that are suspected to be in UPW but are below the detection limit of available measurement methods. Improved measurement methodologies are required for organics, and organic ions to specify low-level contaminants in UPW. Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water.

Chemicals—Figure YE4 also shows various technological areas that may be required to enhance and measure the purity of delivered chemicals to the wafer manufacturing process. Technology areas:

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low outgassing, and non-absorbing materials development are key to effective wafer isolation deployment.

First Year of IC Production DRAM 1/2 Pitch	SUBSTRATE WAFER	 RETICLE	SUBSTRATE LOCATION STORAGE	 PROCESS	 TRANSPORT	2013 32nm	2014 28nm	2015 25nm	2016 22nm	2017 20nm	2018 18nm	2019 16nm	2020 14nm
New FOUP Outgassing / Contamination													
Off line AMC measurement in laboratory	X	0	X	0	0								
Inline AMC measurement inside FOUP in fab	X	0	X	X	X								
Inline AMC measurement inside 450mm FOUP and MAC in fab	X	0	X	X	X								
Used FOUP Outgassing / Contamination (no wafer inside)													
Off line AMC measurement in laboratory	X	0	X	0	0								
Inline AMC measurement inside FOUP in fab	X	0	X	X	X								
Inline AMC measurement inside 450mm FOUP and MAC in fab	X	0	X	X	X								
Vacuum purge and heating	X	0	X	0	0								
Wafer Cross Contamination Inside FOUP (e.g acids after dry etch, oxygen or humidity before EPI clean)													
Inline AMC measurement inside FOUP in fab	X	0	X	X	X								
Integrated AMC measurement inside load port	X	0	0	X	0								
Vacuum purge : outgass the FOUP with wafers under vacuum and fill it with N2	X	0	X	0	X								
N2 purge station : injection of N2 inside FOUP with wafer	X	0	X	0	X								
N2 purge station integrated in stocker : injection of N2 inside FOUP with wafers	X	0	X	0	0								
FOUP change : wafer transfer in a clean FOUP during q-time	X	0	X	0	X								
Purgeable load port : injection of N2 when the FOUP is connected to the EFEM	X	0	0	X	0								
Outgassing chamber integrated in process equipement	X	0	0	X	0								
Wafer tranfer under vacuum	X	0	0	X	X								

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Note for Figure YE3: The introduction of a new line item as potential solution to overcome cross contamination during wafer transportation: Wafer transfer under vacuum

Figure YE3 Wafer Environment and Reticle Environment Contamination Measurement and Control Potential Solutions

First Year of IC Production (e.g. DRAM 1/2 Pitch)	2013 32nm	2014 28nm	2015 25nm	2016 22.5nm	2017 20nm	2018 17.9nm	2019 15.9nm	2020 14.2nm	2021 12.6nm	2022 11.3nm	2023 10nm	2024 8.9nm	2025	2026
GENERAL														
Fluid purity impact on device yield / performance														
Contaminant based process control														
Ultra Pure Water														
Particle online metrology 15 nm [A]														
Particle online metrology 10 nm [A]														
Particle online metrology 5 nm [A]														
Effect of electrically active particles (as opposed to electrically non active particles) needs to be understood- modeling and characterization ongoing [B]														
Particle characterization to identify the source [B]														
Effective Filtration at 10nm particle size [A]														
Effective Filtration at 5nm particle size [A]														
Improved components to reduce particle generation (IX resin, coated pumps, etc.) [C]														
Off-line test for particle filtration performance validation [A]														
Correlation of specifc organic functional groups to wafer defects via Failure Mode and Effect Analysis [D]														
On-line detection of the critical organics (non-volatile) needs development [D]														
Need to develop organic deposition model (sticking, removable, etc.) [D]														
Use on-line TOC as way to control total organics (assuming that all is critical) [D]														

Drivers:
[A] killer particle control
[B] critical particle effect
[C] critical particles and organics
[D] critical organics

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Figure YE4 Wafer Environmental Contamination Control Potential Solutions-UPW

First Year of IC Production (e.g. DRAM 1/2 Pitch)	2013 32nm	2014 28nm	2015 25nm	2016 22.5nm	2017 20nm	2018 17.9nm	2019 15.9nm	2020 14.2nm
GENERAL								
Fluid purity impact on device yield / performance								
Contaminant based process control								
CHEMICALS - Metrology								
Development of 40 nm particle counter [A]								
Development of 20 nm particle counter [A]								
Development of 10 nm particle counter [A]								
Particle characterization to identify source of contamination [A], (for components and systems)								
Bubble discrimination of reactive chemistries [A]								
Improved metrology for concentration measurements[B]								
Surfactant concentration measurement and control [B]								
Anion & cation measurement in process chemicals, e.g. cleaning chemicals [A]								
Organic measurement (TOC and speciation) in process chemicals, e.g. H2O2, IPA [A]								
Contaminant characterization in CMP slurries, e.g. zeta potential, large particle size [A]*								
Contaminant characterization in CMP slurries, e.g. H2O2 concentration [B]								
Characterization of CMP slurries, e.g. Particle size distribution [B]								
On-line contaminant and constituent measurement in plating chemicals, e.g. copper sulfate, organic additives [A],[B]								
Improved blend accuracy taking into account incoming chemical concentration changes (closed loop control capability) [B]								
Closed loop point of use blending improvements [B]								
CHEMICALS - Components and Systems								
Filtration 0.02/0.04 µm with high flux (1 gpm/0.5 psi/10"/1cP) [A]								
Filtration sub 0.02 µm with high flux (1 gpm/0.5 psi/10"/1cP) [A]								
Filtration sub 0.01 µm with high flux (1 gpm/0.5 psi/10"/1cP) [A]								
Ionic POU purifiers (<1 ppt metals) [A]								
Inline End point detection for Ionic POU purifiers [A]								
Improved components to reduce particle generation, e.g. valves, pumps, fittings, etc. [A]								
Improved system startup & flushing methodology to more quickly reach particle target and reduce chemical usage [A]								
Improved flow capacity and increased pressure for pumps [C]								
Improved flow capacity increased pressure and temperature for piping components [C]								
Reduced pressure fluctuations by improved BCD system performance and by better pressure and flow control [A], [B]								
Improved connection technology (reduce leakages and increase reliabilitiy) [A], [D]								
Decrease permeation of piping components (eg HCl permeation) [A], [D]								
Higher purity resins and components (metals, organics, anions, cations, surface smoothness, permeability) [A]								
Elimination of particle sources in chemical distribution system including POU (particle prevention in chemical conditions) [A], (for EUV mask cleaning)								

**Slurries are also looked at in terms of changes in active components (e.g., H2O2)*

Driver:
[A] Purity
[A] Purity - components and systems
[B] Process control
[C] Capacity
[D] Maintenance

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification/Pre-Production
Continuous Improvement

Figure YE4 Wafer Environmental Contamination Control Potential Solutions-Liquid Chemicals

3.2. CHARACTERIZATION, INSPECTION AND ANALYSIS

For pattern wafer inspection the requirements the next years will be to overcome issues of detection of the defects within the nuisance signal. This is correlated to the issue to obtain high sensitivity at high throughput. Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. The high aspect ratio inspection is still requiring for high yield at high throughput due to the high cost of ownership of the inspection tools. This requires also a good separation of the defect signals from the noise. The introduction of advanced lithography process using high energies has a potential to initiate chemical reactions and layer modification on the surface. Therefore the detection of volatile and non-volatile organics is crucial. Currently, only synchrotron radiation based facilities have the potential to analyze traces of non – volatile organic surface contamination. This is with respect to qualification and quantification. Figure YE5 indicates potential solutions for Characterization, Inspection and Analysis.

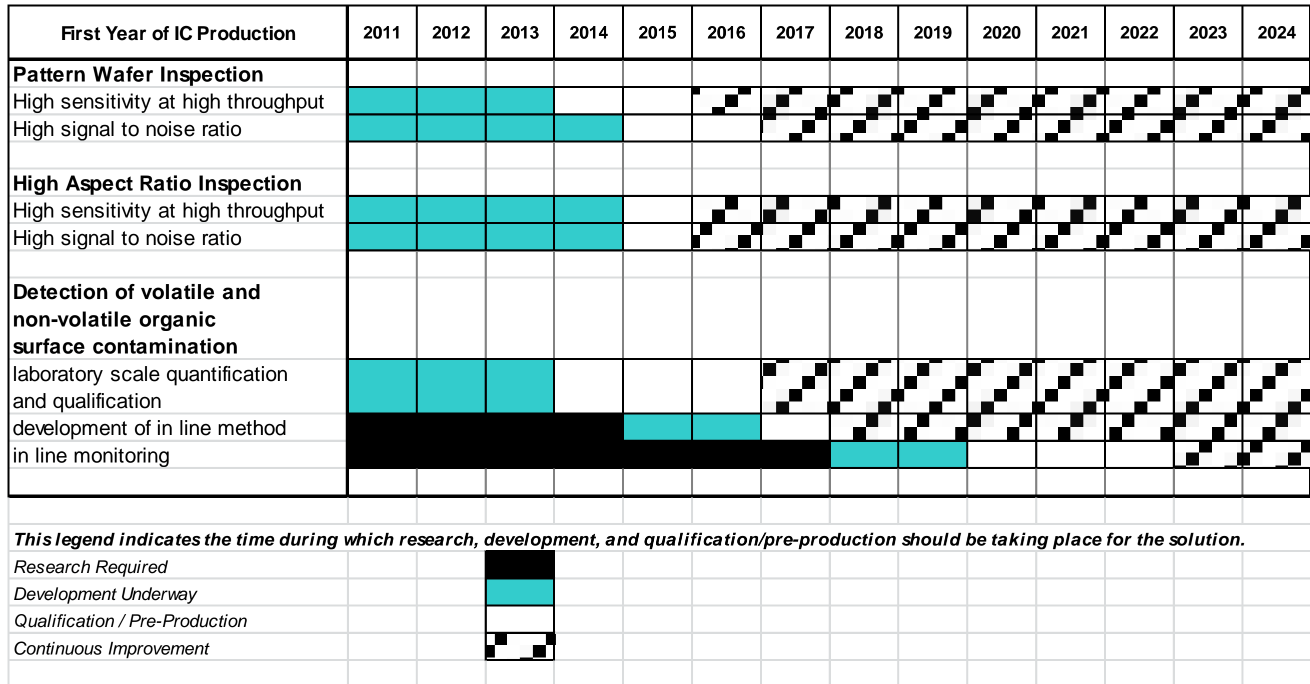

Figure YE5 Characterization, Inspection, and Analysis Potential Solutions

4. YIELD ENHANCEMENT SUPPLEMENTAL LINKS (FOR TEAM AUTHORS TO CHECK)

- AMC monitoring programs - AMC_MonitoringProgram_090730_NBR.xls
- AMC definitions - AMC_ITRS_Definitions_090724_AN.xls
- UPW supplemental materials - 2009 UPW Supplemental Material_100207.doc
- Industry Goals for Particle Measurements In Liquid Chemicals (updated February 2013) - Set LPC goals for the future Feb2013 Liquid Chems.doc
- Bulk and Specialty Gases - ITRS_SG_ContList_070913_NBR.xls
- Ion Table - ITRS IonList FEP UPW FINAL 2011.xlsx
- Mixing Calculation - ITRS_MixingCalc_HPM_100207.xls
- Precursor Table – 1403-14 rev 2 master precursor table 2013.doc
- Precursors in production - 1403-14 precursors in prodn 2013.doc
-

5. REFERENCES

[1] Semi, Standard Practices for the development of Ship To Control Process Limits. 2008.

[2] Funke, H. H.; Grissom, B. L.; McGrew, C. E.; Raynor, M. W., Techniques for the measurement of trace moisture in high-purity electronic specialty gases. Review of scientific instruments 2003, 74 (9), 3909-3933.

[3] Alvarez Jr, D.; Spiegelman, J.; Heinlein, E.; Ramos, C.; Holmes, R. J.; Shamsi, Z., New Chemical Vapor Delivery Systems for Surface Cleaning. Solid State Phenomena 2013, 195, 25-29.

[4] Norton, E. T.; Amato-Wierda, C., Kinetic and Mechanistic Studies of the Thermal Decomposition of Ti (N (CH3) 2) 4 during Chemical Vapor Deposition by in Situ Molecular Beam Mass Spectrometry. Chemistry of materials 2001, 13 (12), 4655-4660.