INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

ASSEMBLY AND PACKAGING

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ASSEMBLY AND PACKAGING

SCOPE

There is an increased awareness in the industry that assembly and packaging is an essential and integral part of the semiconductor product. In many market segments packaging technology is now a critical competitive factor, as it affects operating frequency, power, complexity, reliability, and cost. New emerging device technologies and applications are driving the requirements and innovation for assembly and packaging. As a result the technology boundaries between semiconductor technology, packaging technology, and system technologies in electronics are blurring.

Package designs no longer can be developed independently of the chip and system; they must be considered concurrently as part of the overall system design. As a result, a broad range of complex design parameters must be analyzed to optimize the complete system, and trade-offs among chip, package, and system are required. Package design, to effectively address higher performance while reducing cost on a more diversified base of technology, is driving increasing complexity in design process, tools, and the need for more accurate materials information.

To address these shifts in the industry needs, this year's Assembly and Packaging chapter has been expanded and additional focus has been placed on cross-chapter reviews. Many of the most difficult challenges have also been changed to address the needed shifts in research focus. Since the *2002 ITRS Update* publication, the scope of the Assembly and Packaging chapter has been expanded to include the following:

- Updates on requirements
  - Design
  - Materials
  - System-in-a-package (SiP)
  - Flip chip
- Updates on potential solutions
  - Chip-to-next-level interconnect
  - Single chip packaging
  - BGA and CSP packaging

Many of the Assembly and Packaging roadmap attributes are driven by the electronics products and board/substrate industries, and many of the challenges have system solutions. As a result, the solutions to certain packaging challenges are outside of the scope of this roadmap. To ensure that the needs of the semiconductor community are met, and to better understand system needs, the Assembly and Packaging International Technical Working Group (ITWG) continues to strive for:

- Membership of the TWG to include representatives from electronic systems and board/substrate industries
- Partnerships with organizations developing roadmaps for systems with the National Electronics Manufacturers Initiative (NEMI) and board/substrate industries with the Institute for Interconnecting and Packaging Electronic Circuits (IPC). The scope of these respective roadmaps has been identified and broadened.
- Synchronization of the systems, board/substrate, and packaging roadmaps

The packaging requirements are grouped by four new product categories that were developed based on the changing packaging market. These application areas encompass the majority of the product stream of the semiconductor industry. The technology addressed in the roadmap provides at least 80% of the revenue in each application area (in other words, the revenue center of gravity). The low-cost and hand-held segments have been combined into a single category this year based on the realization that there will not be a significant difference in the cost or major performance requirements in these segments any longer. The memory packaging category has also been eliminated as a separate category. These changes in product sectors will be reviewed with NEMI to develop a revised set of product categories that are common between the roadmaps where possible. These applications areas are:

Low-cost/Hand-held	<$500 consumer products, wireless products, disk drives, and displays
Cost-performance	<$3000 notebooks, desktop personal computers, telecommunications
High-performance	>$3000 high-end workstations, servers, avionics, supercomputers, most demanding requirements
Harsh	Under-the-hood and other hostile environments

DIFFICULT CHALLENGES

The most difficult challenges facing the assembly and packaging industry are presented in Table 92. These challenges are intended to provide a mechanism to allow the research community to focus resources in the areas of greatest need.

Table 92a Assembly and Packaging Difficult Challenges—Near-term

Difficult Challenges ≥ 45 nm/Through 2010	*Summary of Issues*
Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability
Improved Underfills for Flip Chip on Organic Substrates	Thermal performance and thermal coupling between parts Materials which enable integration of SMT, varying semiconductors, and substrate types reliably Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process Narrowing gaps Higher bump densities
Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal integrity associated with higher frequency/current and lower voltage switching) Commercial EDA supplier support System level co-design is needed now. EDA support for “native” area array is required to meet the Roadmap projections. Educational programs required to train engineers in these technologies/requirements.
Impact of Cu/low κ on Packaging	Direct wirebond and bump to Cu Bump and underfill technology to assure low-κ dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
High Current Density Packages	Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. Whisker growth Thermal dissipation

Table 92b Assembly and Packaging Difficult Challenges—Long-term

Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
Package Cost does not follow the Die Cost Reduction Curve	Margin in packaging inadequate to support investment required to reduce cost
Small Die with High Pad Count, High Power Density, and/or High Frequency	Current density, operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
High Frequency Die	Substrate wiring density to support >20 lines/mm Lower loss dielectrics—skin effect above 10 GHz "Hot spot" thermal management needs to be addressed before 2007. There is a "brick wall" at five-micron lines and spaces. Design TWG would like to have an upper bound on thermal management capability of future packages.
Close Gaps between Substrate Technology and the Chip	Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology Production techniques will require silicon-like production and process technologies after 2005.
System-level Design Capability to Integrated Chips, Passives, and Substrates	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Hardware only This is also an issue before 2007.Embedded passives may be integrated into the "bumps" as well as the substrates.
New Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	Organic device packaging requirements not yet define (will chips grow their own packages) Biological interfaces will require new interface types
Bumpless area array technologies will be needed during this period. Face to face packages and other 3D packages are examples. High frequency, low power and low profile are driving forces	

TECHNOLOGY REQUIREMENTS

Packaging technology continues to change rapidly. Assembly and packaging needs are driven as much by market application requirements as by silicon technology. Cost will drive technology trade-offs for all market segments. The key single chip package technology requirements have been updated by the domestic and international TWGs as shown in Tables 93a and b.

Although assembly and packaging costs are expected to decrease over time on a cost-per-pin basis, the chip and package pincount is increasing more rapidly than cost-per-pin is decreasing. This explosion in pin count is increasing not only the absolute cost of assembly and packaging on a per-chip basis, but also the substrate and system-level packaging costs. In the low-cost product and cost performance markets, the cost per pin decreases are also expected to flatten out over the next several years. This will drive a faster rate of package cost increase in these segments. To satisfy the requirements for the increasing numbers of pins needed to leverage silicon productivity more fully, the industry must implement affordable new assembly and packaging technologies that will be more independent of pincount.

Pin count will continue to increase in all segments while die sizes are expected to remain constant. This will drive a continuing need for finer off-chip and off-package pitch. The off-chip digital frequency has been increased to match on-chip in some high-speed communications applications, which will drive the need for improved package signal integrity. The need for very high-speed digital pins and high frequency RF I/O requirements have also been added to the requirement tables.

Packaging technology that addresses very high-power density has already been developed for high-end applications, but will need to be cost-reduced to enable broader applications.

Table 93a Single-chip Packaging Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)							
Low-cost, hand-held and memory	**0.30–0.56**	**0.29–.53**	**.27–.50**	**.26–.48**	**.25–.45**	**.23–.43**	**.22–.41**
Cost-performance	**.75–1.30**	**.71–1.24**	**.67–1.17**	**.64–1.11**	**.61–1.05**	**.58–1.00**	**.55–.96**
High-performance	**1.98**	**1.88**	**1.78**	**1.69**	**1.61**	**1.52**	**1.45**
Harsh	**0.36–3.20**	**0.32–2.88**	**0.29–2.60**	**0.26–2.33**	**0.23–2.11**	**0.21–2.00**	**0.20–1.90**
Chip Size (mm^2) [3]							
Low-cost	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Cost-performance	**140**	**140**	**140**	**140**	**140**	**140**	**140**
High-performance	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Harsh	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Maximum Power (Watts/mm^2) [4]							
Low-cost (Watts) [1]	**2.5**	**2.7**	**2.8**	**3**	**3**	**3**	**3**
Cost-performance	**0.57**	**0.6**	**0.65**	**0.7**	**0.74**	**0.79**	**0.83**
High-performance	**0.48**	**0.51**	**0.54**	**0.58**	**0.61**	**0.64**	**0.64**
Harsh	**0.14**	**0.16**	**0.16**	**0.18**	**0.18**	**0.2**	**0.2**
Core Voltage (Volts)							
Low-cost	**1.2**	**1.2**	**1**	**0.9**	**0.9**	**0.8**	**0.8**
Cost-performance	**1.2**	**1.2**	**1**	**0.9**	**0.9**	**0.8**	**0.8**
High-performance	**1.2**	**1.2**	**1**	**0.9**	**0.9**	**0.8**	**0.8**
Harsh	**2.5**	**2.5**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

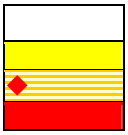

Table 93a Single-chip Packaging Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Package Pincount Maximum [5][6]							
Low-cost	**112–408**	**122–500**	**134–550**	**144–600**	**160–660**	**180–720**	**180–800**
Cost-performance	**500–1452**	**500–1600**	**550–1760**	**550–1936**	**600–2140**	**600–2400**	**660–2800**
High-performance	**2400**	**3000**	**3400**	**3800**	**4000**	**4400**	**4600**
Harsh	**450**	**500**	**550**	**600**	**660**	**720**	**780**
Minimum Overall Package Profile (mm)							
Low-cost	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**1**	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**
High-performance	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Harsh	**1**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**
Performance: On-Chip (MHz)[7]							
Low-cost	**502/3194**	**552/3514**	**607/3865**	**668/4251**	**735/4676**	**800/5000**	**830/5150**
Cost-performance	**3090**	**3990**	**5170**	**5630**	**6740**	**—**	**—**
High-performance	**3090**	**3990**	**5170**	**5630**	**6740**	**—**	**—**
Harsh	**72**	**80**	**88**	**96**	**106**	**116.6**	**128.26**
Performance: Chip-to-Board for Peripheral Buses (MHz) [7]							
Low-cost	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Cost-performance (for multi-drop nets)	**400**	**533**	**600**	**667**	**733**	**800**	**800**
High-performance (for differential-pair point-to-point nets)	**2000**	**2500**	**3125**	**3906**	**4883**	**6103**	**7629**
Harsh	**72**	**80**	**88**	**96**	**106**	**106**	**115**
Maximum Junction Temperature							
Cost-performance	**90**	**90**	**85**	**85**	**85**	**85**	**85**
High-performance	**90**	**90**	**85**	**85**	**85**	**85**	**85**
Harsh-complex ICs	**150**	**150**	**150**	**150**	**150**	**150**	**150**
Operating Temperature Extreme: Ambient (°C)							
Low-cost	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**
High-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**
Harsh-complex ICs	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
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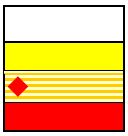

Notes for Tables 93a and 93b:

[1] Cost reduction will slow down as technology matures and economy of scale benefits are reduced.

[2] Cost refers to the average contract assembly cost per pin for each category.

[3] Die sizes for high performance will not increase beyond 310 mm and cost performance die sizes will flatten out as die size approaches 310 mm).

[4] Power will be limited more by system level cooling and test constraints than packaging.

[5] Pin counts will be limited for some applications by system level PWB cost impact.

[6] The pin counts assume the signal to reference pin ratios will vary from 1:4 to 2:1 across different markets segments.

[7] Maximum off-chip frequency will be limited to a small number of pins in many cases combined with a large number of lower frequency pins

Table 93b Single-chip Packages Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Cost (Cents/Pin) [1] [2]						
Low-cost	.22–.41	0.22–0.36	0.22–0.35	0.22–0.31	0.22–0.29	0.22–0.27
Cost-performance scale at 5%	0.52–0.94	0.5–.86	0.5–.77	0.5–0.69	0.5–0.65	0.5–0.59
High-performance scale at 5%	1.37	1.23	1.17	1.05	100	0.9
Harsh scale at 5%	0.27–1.54	0.24–1.38	0.22–1.31	.22–1.17	0.22–1.12	0.22–1.00
Chip Size (mm^2)[3]						
Low-cost	100	100	100	100	100	100
Cost-performance	140	140	140	140	140	140
High-performance	310	310	310	310	310	310
Harsh	100	100	100	100	100	100
Power Density (Watts/mm^2) [4]						
Low-cost (Watts)	3	3	3	3	3	3
Cost-performance	0.85	0.89	0.98	—	1.08	—
High-performance	1.55	1.71	1.78	—	2.05	—
Harsh	0.22	0.24	0.25	0.27	0.28	0.29
Core Voltage (Volts)						
Low-cost	0.6	0.6	0.5	0.4	0.4	0.4
Hand-held	0.5	0.5	0.4	0.4	0.4	0.4
Cost-performance	0.6	0.6	0.6	0.5	0.5	0.5
High-performance	0.6	0.6	0.6	0.5	0.5	0.5
Harsh	1.2	1	0.9	0.9	0.9	0.6
Package Pincount [5] [6]						
Low-cost scale	208–777	249–932	270–1011	325–1213	351–1314	421–1576
Cost-performance	780–2782	936–3338	1014–3616	1216–4339	1318–4702	1581–5642
High-performance	4009	4810	5335	6402	7042	8450
Harsh	642	706.2	812.13	933.9495	1074.041925	1235.148214
Overall Package Profile (mm)						
Low-cost	0.3	0.3	0.3	0.3	0.3	0.3
High-performance	N/A	N/A	N/A	N/A	N/A	N/A
Harsh	0.8	0.5	0.5	0.8	0.5	0.5
Performance: On-Chip (MHz) [7]						
Low-cost	956–6079	—	1243–7903	—	1616–10274	—
Cost-performance	12000	—	19000	—	29000	—
High-performance	12000	—	19000	—	29000	—
Harsh	138	—	179	—	234	—

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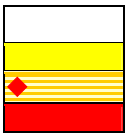

Table 93b Single Chip Packages Technology Requirements—Long-term (continued)

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Performance: Chip-to-Board for Peripheral Buses (MHz)[7]						
Low-cost	**125**	**—**	**125**	**—**	**150**	**—**
Cost-performance (multi-drop nets)	**—**	**800**	**—**	**800**	**—**	**800**
High-performance (differential-pair point-to-point nets)	**—**	**14901**	**—**	**29103**	**—**	**56843**
Harsh	**125**	**125**	**125**	**150**	**150**	**150**
Junction Temperature Maximum (°C) for Cost- performance						
Low-cost	**125**	**125**	**125**	**125**	**125**	**125**
Cost-performance	**85**	**85**	**85**	**85**	**85**	**85**
High-performance	**85**	**85**	**85**	**85**	**85**	**85**
Harsh	**150**	**150**	**150**	**150**	**150**	**150**
Harsh-complex ICs	**150**	**150**	**150**	**150**	**150**	**150**
Operating Temperature Extreme: Ambient (°C)						
Low-cost	**55**	**55**	**55**	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**	**45**	**45**	**45**
High-performance	**45**	**45**	**45**	**45**	**45**	**45**
Harsh	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**	**-40 to 125**
Harsh-complex ICs	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**

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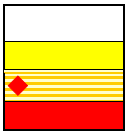

PACKAGE DESIGN REQUIREMENTS

Package design complexity (chip-to-module and chip/module-to-board) and scope are continuously increasing while the market intensifies the demand for design cycle time reduction and high design confidence. Physical, electrical, thermal, mechanical, assembly, and manufacturability considerations, in addition to cost and availability, confront the package designer. The package design process requires continuous improvements in design and analysis tools. The tools for layout, wiring, electrical, mechanical, and thermal design tasks must enhance usability and minimize interface incompatibilities if design cycle reductions are to be realized. The goal is an integrated design system. The scope of this integrated design system must include or be coordinated with chip design so that efficient chip/package co-design is feasible. Ideally, it should be linked to the system design so as to incorporate those requirements and trade-offs.

Differential-pair point-to-point wiring nets are required for high speed, broadband data communications. Data rate and number of such high speed ports will see significant increase in the foreseeable future. The driver-to-receiver power ratio will increase to afford improved attenuation budget, requiring excellent isolation between transmitting and receiving paths.

THERMAL MANAGEMENT

The task of dissipating the heat from integrated circuits while maintaining acceptable junction temperatures has been a significant challenge for semiconductor and system manufacturers. Power and junction temperature requirements are shown by market segment in Tables 93a and b. These ITRS projections indicate that the thermal management challenge will significantly increase in the future due to increasing power, decreasing junction temperatures, and a continuing need to have cost-effective solutions.

In the hand-held market segment, power availability is limited by battery power. The power dissipation is currently limited by the user (the heat sink is the hand or lap), and cooling is usually accomplished without forced air. Challenges increase from the desire to use higher power devices with the increasing convergence of computing with communication (driving higher performance and power in this market); and with an increasing need for system level cooling (more than one hot device). Solutions could include use of higher thermal conductivity materials, reduction in internal thermal resistance, and potentially in more novel approaches to manage cooling while not discomforting the user. Cooling needs to be an integral part of the product design.

Desktop processors for the cost-performance market have required forced air cooling for the system, and have represented a wide spectrum of electronic products. With area array flip chip, the backside of the chip provides a direct heat path for cooling. The packaging challenge has been to create an interface with the chip that provides very low thermal resistance, is cost effective, reliable, and also enables system level solutions. System cooling design must also be acceptable in this market, with implications to cost, acoustic noise, reliability, and high volume manufacturing. As Tables 93a and b show, power is expected to continue to increase while target junction temperatures decrease. In 2002 this equates to a ΔT of 45° (and shrinking over time) with the ambient. At an expected power of 75 Watts (and growing over time), this becomes a significant challenge for acceptable solutions in the cost-performance market, and further highlights the need for complete, integrated, chip-to-system solutions. Some of the key developments and innovations are: more advanced/efficient air-cooling, boundary layer control, engineered surfaces, and cost-effective alternative cooling systems.

Notebook computing products are also in the cost-performance market segment. Although they may not push the highest power levels while on battery operation, they do pose significant cooling requirements based on form factor, weight, and ergonomic issues (maintaining comfortable outer case temperatures for the user). Additional developmental areas would include redirection of internal thermal resistance, engineered surfaces, new novel cooling systems, and solutions that allow multiple and different power levels for the product.

The high-performance market sector has experienced a dramatic increase in power over the different generations. Air-cooling has been the preferred option to keep costs within bounds. In addition to managing total chip power requirements in excess of 100 Watts, solutions to manage power density and internal hot spots are necessary. Assuming identical junction and ambient temperatures, the higher power levels in this sector will demand a 40%–50% reduction in junction to ambient thermal resistance compared with the cost-performance segment. Current solutions are already focused on complete integration from the chip through the system, and this approach will need to continue. Significant engineering development will be needed for power increases at each technology generation, with capabilities needed equivalent to closed-loop cooled systems. Solutions must of course also be acceptable to the end-use customers. A major additional challenge will be to ensure that thermal management does not impede the migration path of products from this sector into the cost-performance market.

PACKAGING MATERIALS REQUIREMENTS

Assembly and Packaging involves the package physical design, and the design of materials and manufacturing processes to realize the physical design goals in performance and reliability. Dramatic improvements in materials properties will be required to support the projected technology nodes driven by projected semiconductor requirements in power, frequency and I/O, as well as market requirements in cost, size, weight, and environments. The rapid reduction in wirebond pitch will call for reduction in wire size, capillary, and solutions for wire sweep, electrical signal integrity and bond pad design, all of which will require significant materials improvement, and materials process innovation beyond what are available today.

The projected reduction of flip chip bump pitch from the current 150 µm to 100 µm in 2009 and thence to 70 µm will result in significant reduction in UBM via size as well as bump size and bump height. Materials innovation in solder-UBM structure as well as underfill materials and dispense process will be required to provide high volume manufacturing process and reliable package structure. One important area of concern will be electrical-thermal migration in the solder UBM structure associated with the expected current density increase with small UBM openings. Underfill void and adhesion in the reduced solder bumps gap and spacing between the bumps will pose additional difficult materials challenge.

With the introduction of Cu/low-κ materials the on-die dielectric stiffness will be approaching in stiffness to the materials on the package side such as the molding compound or underfill materials. Thermomechanical stresses will be transmitted to the die across the die-package interface. The IC and package is one single physical structure, and it will be necessary to

provide the process knowledge, materials database and the design methodology to assure that the materials on both sides of the interface, particularly the chip dielectric and copper interconnect, will be robust under thermal mechanical stress. For example, low modulus underfill materials and molding compound materials may become necessary. With the growing importance of die stacking to the main stream of consumer/handle applications, very thin die from continued reduction of wafer thickness will be called for, providing significant challenge and opportunities to the packaging materials engineer.

Major efforts have been underway to address environmental concerns such as materials and surface finishes for lead free solder assembly and for halogen free materials development and implementation, and they are expected to continue in the coming years. Materials properties like dielectric constant, dielectric loss, and thermal conductivity will be very significant to meet higher frequency and higher power demands. Materials research and development will be needed to meet thermal management challenges such as for thermal interface materials, heat spreaders, and external solutions. Knowledge of packaging materials properties are critically needed for modeling and simulation of electrical, thermal, and reliability performance for package design release and new package development. Methods for accurate characterization of materials properties and materials interface properties for packaging materials in their use environment will be needed. Establishment of materials database to make the materials information available to the community will be very important.

Table 94 Materials Challenges

Materials Challenges	*Issues*
Wirebond and Capillary	Materials that enable 20 micron pitch without wire sweep and provide good signal integrity
Solder Materials	Solder and UBM the supports 100 micron pitch and high current density
Underfills	Ability to support 100 pitch on large die
Thermal Interfaces	Increased power density
Materials Properties	Methodology and characterization database for frequencies above 10 GHz,
Molding Compound	Low modulas materials that reduce stress on low-κ wafer structures

RELIABILITY REQUIREMENTS

With the introduction of many new package formats, copper chip interconnect, low-κ chip dielectrics, direct chip attach, and area array interconnect there are many new requirements to packaged device reliability. Many of these new materials and package configurations require extensive characterization given the lack of historical reliability data. Extensive use of simulation to help validate and understand reliability performance is also required to assure these technologies are deployed with reasonable risk factors.

Some new package designs, materials, and technologies will not be capable of reliable performance in all market applications. More in-depth knowledge of the relevant failure mechanisms coupled with knowledge of the market use conditions will be required to bring new package technologies to the marketplace. Better definition of environmental requirements for each market segment would facilitate package development tailored to the market needs and help ensure consistent reliability performance among suppliers as well as between suppliers and customers. More research emphasis on physical and thermo-mechanical models of failure mechanisms is needed to support this trend.

Conception and development of tools for rapid electrical and physical fault isolation of package and interconnect technologies is critical. Faster techniques are needed to execute statistically significant studies of material bulk and interface properties. Developing extensions of current fault isolation and package analytical technologies (such as X-ray, acoustic, and Moire) needs to be balanced with development of new technologies for small defect visualization (such as X-ray tomography). Organic chemical interface analysis techniques are growing in importance with the introduction of new organic materials. Low alpha materials need to be considered during the timeframe of the ITRS to reduce errors induced by alpha radiation. Measurement techniques and standards for alpha radiation effects are not adequate to support the increased alpha sensitivity anticipated for advanced technology processes.

Interfacial delamination will continue to be a critical reliability hazard that is worsened by the trend to larger chips and new materials. Standard methods and acceptance criteria for interfacial adhesion are lacking. Fundamental work is needed

to establish adhesion strength and degradation rate versus environmental factors (temperature, relative humidity) as well as a function of interfacial physical (such as roughness, composition) and chemical (van der Waals, dipole, covalent) properties. The CTE mismatch between the chip and the substrate should be reduced to mitigate large chip packaging-related reliability issues.

New electrostatic discharge (ESD) test methods and equipment are required to comprehend increasing pincount and shrinking interconnect pitch. Improved handling solutions for bare chip and packaged devices will help ESD related reliability issues.

MEMS REQUIREMENTS

MEMS technology has broadly expanded in the last decade to become the standard for many automotive, medical, telecommunications, and consumer electronics applications and the predicted market growth for MEMS technology is very high. One of the major bottlenecks for the continued growth of MEMS products has been packaging technology.

Like standard semiconductor devices, MEMS devices need environment protection, electrical signal integrity, mechanical support, and thermal management. However, in addition, MEMS may require packaging that provides access to chemical or biological environments they interact with. Many of the MEMS applications also demand inert/vacuum inside the package. For example: pressure sensors “media compatible” for the disposable blood pressure application are not “media compatible” for a ten-year automotive application. As a result, even though the functionality of two MEMS could be the same, the differences in environment drive quite different package requirements. To effectively reduce cost, improved manufacturability, and improve reliability standardized technologies need to be develop that can handle this broad range of requirements. MEMS do not require high pin counts, or very fine pad pitches for interconnect.

Some single-chip ceramic, molded, chip scale, and wafer-level packaging technologies have been used successfully to address some of these applications requirements. However, MEMS multichip packages and 3D packaging solutions are still under development.

To meet product performance requirements MEMS devices and packaging designers must consider the interface of structural elements, signal processing and power elements, signal and energy changing elements, material technology, harsh media compatibility, test equipment process and standards, packaging techniques, and processes. While many of these issues are common with semiconductor packaging some are unique to MEMS. CADs systems package design standards and methodologies, packaging assembly attributes, reliability standards and assessment, and interfaces of micro and macro packaging attributes need to be developed to handle these unique design requirements.

0PTOELECTRONICS REQUIREMENTS

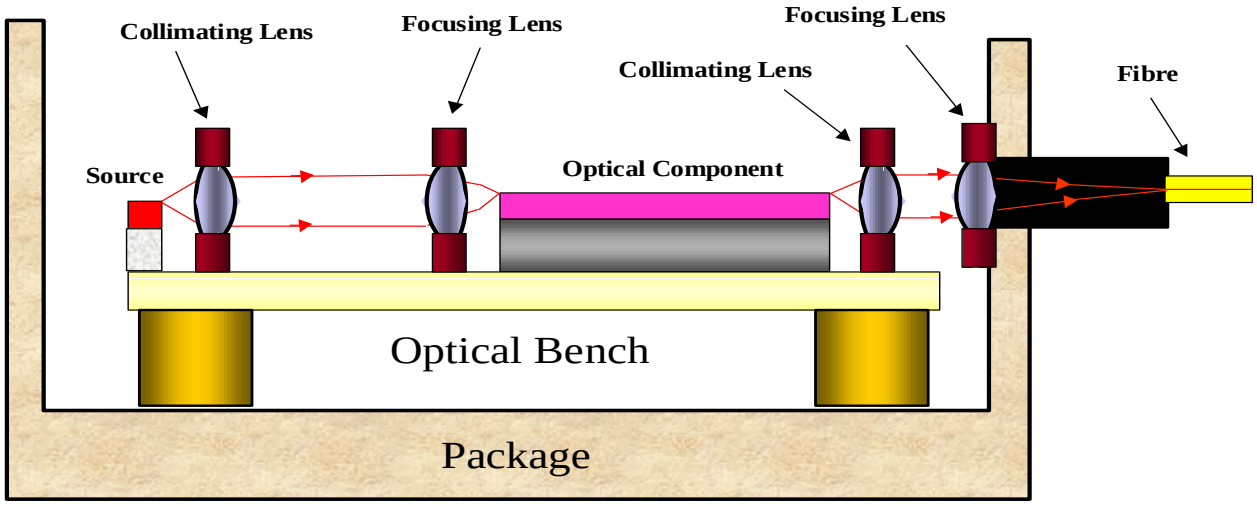

Figure 72 Optoelectronics Package Design Illustration

Optoelectronics packaging brings together two realms of component packaging—the traditional electronic packaging with its associated issues (covered elsewhere in this chapter) and the integration of optical components into the optoelectronics package. Figure 72 is an illustration of an optoelectronic design. The electronic packaging issues may be viewed as a special case of multi-chip packaging. I/O counts are typically lower and die sizes are smaller than standard multi-chip modules. The main issue is the high data rates and low signal levels of the converted optical signal. Another challenge is integration of optical functionality into the optoelectronics package. Optical functionality includes passive devices such as array waveguide gratings (AWG), filters, splitters, etc., and active devices including lasers, modulators, detectors, amplifiers, switches, and attenuators. An integral part of the optical-to-electrical and electrical-to-optical conversion is the high data rate, broadband electrical signals. It is desirable to integrate the serializer-deserializer (Serdes) in the optoelectronics package.

The key mechanical issues with optoelectronics packaging is aligning the optical path and maintaining this alignment under all service conditions. Typical systems for higher data rates utilize a 9.3 µm diameter fiber core that needs to be aligned to a narrow active device. For example, a detector for 10 Gbps use may have an active area on the order of 25 µm. The transmitter (laser) alignment tolerances are even more stringent with the mode size of the order of 10 µm and a mode shape that would need to be converted to match the fiber mode. This may require additional optics (lenses) between the laser diode and the fiber. Each added optic adds to the alignment complexity and increases the loss. These interfaces can be a large source of attenuation greatly impacting the system loss budget. Hermetic packaging is used to keep the optical pathway clear of contamination. Contamination in the pathway leads to additional loss and can damage the optical surfaces through absorption-generated heat or focusing of the optical beam. Cost reduction, especially for Metro applications, including broadband services delivery to small businesses, schools and homes, is driving the need to develop a non-hermetic approach. Fiber feed-throughs in the hermetic package add a great deal of complexity and cost. Care needs to be taken in mounting the optical components due to strain-induced birefringence. This effect can cause wavefront distortion and scattering.

The main issue in assembly is how to automate the alignment process, including automatic fiber handling and placement, to reduce costs. A self-aligning structure, which can be assembled without concern regarding changing alignments, is needed. A standardized approach to packaging and alignment would ease the development of automation equipment. Currently, only a few high-volume manufacturers are automating their processes. Simple issues such as how to handle fiber pigtails through an automation process need to be addressed as well as standardized carriers and systems.

A better understanding of the materials properties and careful selection of assembly materials are necessary to successfully engineer optoelectronics packages. The optoelectronics package may contain substrates as diverse as silicon, AlGaAs, InP, Polymer, or SiGe in various combinations in one package. An understanding of the thermomechanical effects and material interactions will be necessary for the fabrication of reliable packages. Viscoelastic properties of the mounting adhesives will be necessary to understand the environmental stressing behavior of fiber alignment mountings.

Integrated design capabilities will need to be developed for optoelectronics packaging. Design systems that encompass the optical, electrical, thermal, and mechanical requirements of these packaged systems are needed.

Thermal management requirements in optoelectronic packaging are more stringent than in their electronic counterparts. Whereas thermal management in standard electronics is primarily for reliability concerns, in optoelectronics many devices have temperature sensitivity to their operating parameters, such as wavelength. Indeed, it is common to use temperature tuning of the optical devices in order to operate on a specific wavelength on the ITU grid. This leads to a need for integration of thermo-electric (Peltier) coolers into the package and an adequate method for dissipating the waste heat. Future devices will be densely packed and operate at very high rates (10 Gbps, 40 Gbps—160 Gbps), which will only further exacerbate the thermal issues. Additionally, thermal drift will impact fiber alignment through differential expansion of the different components of the package. The optoelectronic packages may include optical devices such as laser diodes, photo diodes, light guides, and fibers. Since the characteristics of many of these components are temperature sensitive, the efficient control of the operating temperatures of the packages is required.

Optoelectronics packaging materials comprised of conventional electronic packaging materials, light guiding materials, optical positioning adhesives, and white light producing phosphor coatings. The challenge arises out of the fact that apart from meeting the requirements for electronic devices, the needs such as thermal stability, refractive index and assembly tolerance of optical devices/materials must also be met during assembly. Light guiding materials should exhibit very low loss of optical signals, high thermal stability to allow reflow processing, low birefringence, easy control of refractive index, and ease of processing.

SYSTEM-IN-A-PACKAGE REQUIREMENTS

Beginning in 2000, driven by mobile phone applications, a shift is occurring in multi-chip packaging where the System-in-a-Package (SiP) is becoming the fastest growing area of packaging due to its associated system integration benefits. SiP enables OEMs to continue their size/weight reduction trends while integrating more features and functions through system package integration. This integration challenge may be best realized through cooperation between OEMs, their semiconductor device suppliers and microelectronic manufacturing service suppliers. The OEMs in the mobile phone applications face shorter product life cycles. They have come to the realization that designing new products is easier and more cost effective when they can employ SiP using available ICs and do not have to reinvent some new ICs from scratch.

The definition of SiP has not been well established across industry. The ITRS AP-TWG has defined SiP as any combination of semiconductors, passives, and interconnects integrated into a single package. This definition does not limit SiP to any one technology or integration approach. There are, however, a number of distinct types of SiP approaches for different market sectors that have emerged. These include stacked-die, SMD mixed with bare die assemblies, and build-up approaches. In trying to define technology requirements for SiP we have not broken the requirements for each of these approaches and expect the requirements to be applied for each approach as noted.

The SiP can be manufactured using ceramic, leadframe, organic laminate, or even tape-based substrates. The passive components can be either embedded as part of the substrate construction or soldered or epoxy attached on the substrate surface.

Die interconnect can be accomplished by either wire bonding, flip chip (soldered or epoxy), and/or TAB to the SiP substrate or die-to-die. The final package configuration can take the shape of a conventional ceramic style package, ball grid arrays, land grid arrays, and leadframe-based packages or custom modules. The resulting SiP utilizes die-to-die interconnection and high density substrate technologies to handle the higher wiring density requirements at the package level, thereby reducing the cost, wiring, and I/O densities required at the mother board and system level.

Stacked-die approaches are being driven by the need to increase density in many hand-held applications, combined with the needs to reduce package cost. The technology has now been well established for logic and memory die applications that benefit from the common I/O interfaces plus die-to-die bonding. SMT combined with bare die in a single package is being utilized to provide integration of analog and digital systems components.

This approach has emerged as an alternative to SoC. The prime benefits of SiP are ability to integrate different semiconductor technologies and passive component types. SiP has faster design and prototype cycle time than SoC has. It also has lower development cost and improved functional density. For systems that require both analog and digital ICs, e.g., wireless systems, SiP has become the packaging technology of choice based on these benefits.

Since SiPs were first adopted in high-volume, hand-held and wireless applications, their resulting low-cost infrastructure, accomplished through the utilization of proven packaging platform technologies in high volume manufacturing lines, enables new SiP configurations to be customized for a broad range of new applications. Any application that utilizes chip sets, embedded, or large memory blocks with high interconnect density requirements should evaluate SiP for their cost/performance optimization needs.

However, the technology is still very immature and as a result there is a broad base of technology development requirements. These include development of well-defined technology standards, which will help drive the required design tool, materials, manufacturing process, equipment, and reliability improvements.

The SiP packaging concept is here to stay for the following reasons and can be considered as the fourth wave of packaging innovation:

- Different IC technologies such as GaAs, SiGe, and/or Si, and die functions such as logic, memory, RF, and/or analog can be assembled in the same package to achieve specific thermal, electrical and mechanical performance requirements.
- Dissimilar die geometries from 90 nm to 250 nm can be integrated in the same package cost effectively. The use of commodity, high volume ICs reduces final cost. The latest die technology can be used for each die function when necessary, therefore increasing performance.
- Other technologies such as MEMS, optical, or vision components may be included in the same SiP.

- Different interconnection technologies can be used—wire bond, flip-chip, or TAB—to connect to the package as well as each other.
- Other than passive R-, L- & C-components, antennas, baluns, filters, resonators, connectors, shields and heat shrinks can be included in the same package.
- Revisions or upgrades to OEMs products are easily accomplished by using the latest die functions, therefore reducing the cycle time for those changes.

As the ability of the semiconductor sector increases to build true SoC, not all the different components that need to complete a system can be cost effectively integrated on silicon. The SiP would then take on the responsibility to package the other non-silicon components into the package with the SoC device. The SiP will continue to become more complex and cost effective as new applications emerge. The final factor in favor of the SiP is the short cycle time it takes to create a new SiP or a modification of a present design. From design, characterization to manufacturing could be as short as 3–4 months while a SoC would take much longer. This cycle time reduction is why the SiP will continue to play a critical role in component packaging and system integration.

The SiP category does require new metrics for measuring cost-effectiveness. The cost-per-pin paradigm does not apply well to SiP and multi-chip package applications since the SiP greatly reduces the number of second-level connections through die-to-die interconnection within the package. Also the area and wiring density reductions in motherboard provide system cost reductions while enhancing reliability and performance. Both cost per area and total cost of ownership perspectives are required to fully appreciate the system integration cost and performance benefits delivered by SiP solutions. For instance, silicon efficiency is a new metric to measure the area effectiveness of flip-chip bare die and wafer level packaging (WLP) versus multi-chip and 3D packaging solutions. Bare die or WLP achieve 100 % Si efficiency (where the die size and package sizes are equal) whereas emerging 3D (stacked-die) packages are delivering over 250% Si efficiency using the previous measurement methods.

The SiP infrastructure faces the following challenges as it continues to grow:

- Design tools for the package
- Modeling tools for thermal, thermomechanical and electrical performance
- Factors compounding the increase in cooperation between the manufacturer, semiconductor device suppliers and the OEMs
- Functional test and build-in self test (BIST) at both the IC and package levels to facilitate the fault diagnosis and the assurance of die quality and reliability for the final system products

Table 95 provides a summary of some of the SiP technology requirements through 2018 with a focus on chip count, total component count, and reliability levels for mainstream products. The SiP table does not include information on substrate technology and related technology for embedded passives. These requirements are discussed in the substrate technology requirements and embedded passives sections. The assumption is that these SiP requirements can be addressed by either organic or ceramic-based substrate technologies, and that the industry will continue to use both these technology for SIP over the entire projection period.

SiP cost is also not addressed in the requirements table since a clear metric could not be defined. However, cost is expected to be the most critical factor in technology selection and implementation across industry. A key cost trade-off is the use of embedded passives in substrate that require addition layers and specialized materials versus surface mounting discrete components that provide the same functionality but require additional board area and add complexity to the assembly process.

Table 95 System-in-a-Package Requirements

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node		*hp90*			*hp65*			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
Number of terminals—maximum digital	**800**	**1000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**	**2000**
Number of terminals—maximum RF	**100**	**150**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**	**200**
Maximum body size (L × W) (mm)	**40**	**50**	**52**	**52**	**52**	**52**	**52**	**52**	**52**	**52**	**52**	**52**	**52**
Minimum terminal pitch BGA	**1.27**	**1.00**	**0.80**	**0.80**	**0.80**	**0.80**	**0.65**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**
Minimum terminal pitch leadless	**0.65**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.5**	**0.50**	**0.40**	**0.40**	**0.40**	**0.40**	**0.40**
Number of stack die maximum	**4**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Number of die in SiP maximum	**8**	**10**	**10**	**10**	**10**	**8**	**8**	**8**	**6**	**6**	**6**	**6**	**6**
Minimum component size (in.)	**0201**	**0201**	**0201**	**0105**	**0105**	**0105**	**0105**	**0105**	**0105**	**0105**	**0105**	**0105**	**0105**
Embedded passives	**Few**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**
MSL level	**3**	**2A**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Maximum reflow temperature (°C)	**250**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**	**260**

FLIP CHIP REQUIREMENTS

Flip Chip has been the standard interconnect technology for microprocessors and logic chips for high-performance main frame servers. To be widely adopted outside of these two specific areas, the industry requires cost competitive and readily accessible flip chip infrastructure, including wafer bumping, wafer probe, package substrate, and assembly. Flip chip packages assembled with eutectic solder bump, or high lead solder with low temperature solder finish, represent the target with which solutions in materials, surface finish and process technologies should be benchmarked. The semiconductor roadmap has projected higher thermal dissipation, higher frequency, and higher I/O, and compatibility with Cu/low-κ materials, in the next set of technology nodes. Potential solutions include decrease in bump pitch from 150 µm today to 70 µm by the end of the period for high I/O and high power chips. Reduction in bump pitch results in corresponding decreases in UBM size and UBM via opening, as well as in bump size, bump height, and underfill flow. Potential package design and process solutions will require understanding of how materials and process requirements will be met, as well as their impact on thermal-mechanical reliability and electro-migration behavior. Reduction in bump pitch and increase in bump I/O will increase local and global wireability requirements on the substrate. For hand-held portable applications, features such as thinning of bumped wafers, stacked and 3D package, and flip chip on lead frame will be required to compete with corresponding wire bond packages.

Automotive application includes high temperature and high power application. The next technology nodes will herald new designs and materials driven by broadened industry applications and technology advances including Cu/low κ in the die, high wireability substrates, smaller bump pitch and green package movement. Extensive reliability database and basic knowledge will be necessary for success in the market place. Flip chip and wafer level packaging will share infrastructure facilities such as bumping, re-passivation and redistribution, and technical issues. Wafer probing will continue to be a very important element for flip chip and wafer level packaging implementation. Finally, industry must perceive flip chip to be cost effective for their applications in order for it to succeed.

EMBEDDED PASSIVES REQUIREMENTS

The needs for embedded passives on packages have been variously described to be 1) saving on package real estate, 2) improving performance through shortened path, and 3) saving in cost of component and assembly. The alternate is discrete passives on package or implementation on chip. Embedded passives will be implemented only when there are competitive advantages in cost, performance, or functionality as compared to discrete passives or on-chip passives. With the cost and size of the discrete passives continue decrease, the embedded passives will likely find first implementations in specific areas where discrete or on-chip solutions are not suitable. While research in materials and manufacturing

processes for embedded resistors, capacitors, and inductors are proceeding, there would be a need for integrated package design tools that would include embedded passives in the design processes.

Discrete resistors can achieve the tight tolerance by sorting, and have extremely low cost and small size. Embedded resistors are used not because of size or materials cost benefit. Instead, a designer may use embedded resistors when discrete resistors are not sufficient to meet the performance need due to its parasitic inductance and capacitance. The most important issue for embedded resistor is their tolerance in the performance-oriented applications.

The printed wiring board could use a large number of terminating resistors. The savings from the piece parts and their assembly cost of a large number of discrete resistors may be sufficient to trade-off the additional cost associated with the embedded resistor layer and the required laser trimming. However, the materials resistance range, stability of sheet resistivity in long-term usage, and the temperature coefficient of resistivity still need improvement, particularly when used in package substrate applications.

The optoelectronic applications are pushing for broadband applications. These applications need high precision resistors as close to the ICs as possible. Customers are willing to pay for the additional cost of laser trimming on embedded resistors on the packages.

For those applications, where 15% tolerance is sufficient, on-chip resistors will be used. Resistors must also have very high density to meet the high I/O lead count requirements. There is no benefit to use the embedded resistors on the package, unless the high precision is achieved using laser trimming. The density constraint will limit it to medium I/O applications. The broadband opto-electronic module manufacturers often depend on the third party library services offered by the semiconductor foundries for I/O interface circuits, which may not include the required on-chip terminating resistors.

At the present time, the chipset users encounter the need to get different ICs from different sources. The terminating resistors may or may not be on the chipset ICs. The graphic DRAM ICs connected to the chipset ICs may or may not have the terminating resistors. There is a desire to have embedded terminating resistors on the packages. Such package may be used in the differential-pair point-to-point wiring nets. For multi-drop wiring net, a terminating resistor is need at the end of a long transmission line. It is usually placed on the PWB, not on the packages. In other words, it is desirable to have embedded resistors on the package for the point-to-point wiring net.

However, the additional cost should be very little, because the IC cost will remain the same when the terminating resistors are eventually integrated on the IC. Furthermore, the on-chip terminating resistors are more flexible. They may be connected or disconnected under IC control. That is, they may be used for point-to-point as well as the multi-drop wiring nets.

If implementation of embedded resistors requires an additional layer on the package substrate, the additional layer cost would have to be amortized over the cost of all the resistor components. However, if they can be implemented over unused real estate on the package and require little additional process steps in substrate processing, the economic justification will be more compelling.

For RF applications, resistors in the range of 20 to 100 Ohm are used for load and termination. Discrete resistors may be sorted to get the precision required. Embedded resistors will need trimming to get the required precision. Those in the range of 100 Ohm to 250K Ohm are used for biasing and circuit stability purpose. The cost of a chip resistor and its assembly on PWB is about one cent or less per resistor. This is the cost target for the trimmable, embedded on-package resistors.

De-coupling capacitors are needed as reservoirs of electrical charges to minimize switching noise in the electronic system. The rise/fall switching transition is very short in the IC, has a medium duration in the package, and is longest on the printed wiring board. Therefore, designers want high-frequency de-coupling capacitors on the IC, or very close to it to minimize the series inductance and resistance; mid-frequency de-coupling capacitors on the package; and low-frequency/high-capacitance de-coupling capacitors on the PWB.

For RF applications, capacitors in the range of 1 to 100 pF with 10% tolerance are used for RF tuning circuits. Those in the range of 10 to 1000 pF with 10 to 15% tolerance are used for IF tuning circuits. Those in the range of 100 pF to 100 nF with 15 to 25% tolerance are used RF bypass applications. The embedded capacitors may achieve the 15% tolerance, and may be used for IF tuning, DC blocking, and RF bypass.

The discrete capacitors may be sorted to meet the required precision. The cost of a chip capacitor and its assembly on the PWB is about one to two cents per capacitor. The challenges are the minimization of the series resistance and inductance of the lead wires. The on-chip capacitor array may have a total value of 100 pF per array. They may be personalized

through on-chip logic circuits to meet the value for the specific circuit requirement, which is not possible with on-package capacitors.

There are a few parameters affecting the quality value (Q) of a on-chip inductor, as follows:

- The semiconductor substrate is not an insulating material. The distributed capacitance between the inductor coil and the non-insulating substrate reduces the effective inductance.
- The high series resistance of the fine metal lines on IC.
- The on-chip inductors have been used by RF circuit designers. For examples: impedance matching, filtering, and the LC-tank circuit in the oscillators. Oscillators without inductors have also been implemented.

The clock generation in the microprocessor IC may use one or more on-chip phase-lock-loops (PLL). Some PLLs may use LC-tank circuit in the oscillators. The highest frequency PLL may use the on-chip inductor. The additional on-chip PLLs may use on-package, either discrete or embedded, inductors in the tank circuits. Of course, there are PLLs free of any inductor element. The on-chip analog power supply to the on-chip PLLs may use on-chip series regulator, which uses on-chip de-coupling capacitors to remove noise from the digital sections.

The on-package inductor minimizes both constraints encountered by the on-chip inductors. The designers need to follow a few rules in laying out the desired inductors. They also have to pay close attention on magnetic flux linkage among adjacent inductors, which cause coupled noise. Note that the inductive coupling reaches a much farther distance than the capacitive coupling does. The designers have to be very careful about coupled noise concern when pushing for a high number of inductors on the package. The use of high permeability material will increase the inductance value.

There are several functions, which are implemented by passive components, and are too large to be integrated on the ICs. Some examples are antennas, baluns, filters, resonators, and RF shields. These structures required improved dimensional control in substrates and low-loss dielectrics in low-cost substrates. The broad range applications of system-in-a-package (SiP) have called for the implementation of embedded passives in the package substrate as discussed in the SiP and RF sections.

RF AND MIXED-SIGNAL REQUIREMENTS

The packaging challenges in the RF and mixed-signal realm will become increasingly important as low-cost mobile and high bandwidth products expand across all market segments. The increasing performance of silicon, SiGe, and GaAs devices, coupled with dramatic device cost reductions, has established the need for very low-cost, high-performance packaging. The primary approach to date has been to focus on extending performance of established low-cost, wirebond packages through careful design optimization. However, this approach will not support continued cost reductions and performance improvements on the long term. In the RF product area, frequency shifts up to the 5 GHz range that will require improved dielectric loss, tighter control of parasitic variability due to process variations, and more precise electrical simulation capability, including near-field and far-field effects.

Flip chip attachment to package and embedded passives on the package minimize connection length. They will be key enabling technologies to package level performance. Low inductance and high-density packages like FBGA/CSP will enable designers to use lower cost partitioning solutions than the traditional ceramic modules.

Integrated modeling and simulation tools are required to drive down design cycle time to acceptable levels. Performance, physical size, and cost driven integration will continue to arrive at a single chip radio that combines memory, processor and mixed-signal functions, when economically feasible. In the mean time, system-in-a-package (SiP) will serve the broad range wireless applications as discussed in an earlier section.

Fast design cycle time and accurate simulation at both the chip and package levels are enablers of this integration. High-speed test and higher level of functional test at the package level also become development challenges. Microelectromechanical systems (MEMS) will be used in the fabrication of filter, switch, oscillator and other components. They offer the benefit of small size, low insertion loss, low power consumption, integration with ICs, and the potential of low cost with batch fabrication. Reliability, potential temperature sensitivity, and hermetic/vacuum packaging of MEMS devices are key development challenges.

POTENTIAL SOLUTIONS

WAFER LEVEL PACKAGING

The wafer level packaging process (WLP) is a technology in which all of the IC packaging is performed at the wafer level. A WLP technology can, for the first time, maintain the cost of the IC packaging as a constant percentage of the total wafer cost. This is possible because WLP reduces the cost of packaging the individual chips. A WLP technology requires that when the chip size shrinks in later years, all of the package interconnects will continuously be located within the chip outline (it must be a fan-in design, known as the real chip size package). From a systems perspective, the limitation on WLP is how many I/O can be placed under the chip and still have a board design that can be routed.

The primary application market for WLP technology is projected to be low to moderate I/O density applications, as typified by high yield DRAM, Flash, Analog, EEPROM, RF and other ICs with ≤ 100 total I/O and adequate silicon area.

FBGA packages from WLP technology reached the level of practical use in 2000. Its use will expand in the field of portable devices and other small-size devices that require high-density mounting. A key enabling technology to take full advantage of a WLP will be the development of wafer level test and burn-in. Most WLPs with I/O pitch equal to or greater than 0.5 mm do not require the use of underfill and can therefore be directly implemented into a standard surface mount technology (SMT) process flow.

WLP technology can solve or eliminate the problems and restrictions involved in bare chip mounting, therefore packages from WLP will be an alternative to bare chip EEPROM.

CHIP-TO-NEXT-LEVEL INTERCONNECT

Table 96 illustrates the chip-to-next-level interconnect potential solutions. The values for wire bond in this table are for inline pad pitches. Staggered and multi-tiered bond pad configuration can achieve an effective pitch denser than the value shown for inline pitch. The combination of decreasing pitch and multi-tier pad design provides effective potential solution to the high I/O requirements. The flip chip connection requires fan-out wiring on the package substrate. Signal leads are usually placed on the outer several rows together with many of the voltage and ground leads for easy fan-out and minimum package inductance. The inner regions of the area array may be used for voltage and ground connection to minimize the on-chip resistive voltage drop across the IC chip. The area array pad pitch is 150 μm now, and reduces to 130 μm for the 80 nm technology generation and beyond for applications in the cost performance and high performance market segments where there is growing need for increasing signal I/O and high chip power. This interconnect approach will require compatible wafer bumping, wafer probing, assembly, underfill and substrate technologies being available at the necessary performance and cost. Users will likely minimize change of the pad pitch in their product line to reduce the cost of the test probe head. The trade-off is with length of fan-out wires where crosstalk noise between parallel signal wires would be a consideration. For some of the hand-held applications where the chip size and power are small, one may utilize area array pad pitch smaller than that used for the cost-performance and high-performance market segments. Smaller bump pitch on the chip requires corresponding pitch on the substrate and assembly process capability including underfill. The trade-off between design advantage from small bump pitch and the higher cost of substrate and flip chip assembly will determine the directions for the technology. For the applications with low supply current, the anisotropic conductive adhesives may be used for the area array connections

Table 96 Chip-to-next-level Potential Solutions

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node		*hp90*			*hp65*			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
Chip Interconnect Pitch (µm)													
Wire bond—ball	**40**	**35**	**30**	**25**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Wire bond—wedge	**30**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
TAB*	**35**	**35**	**30**	**30**	**25**	**25**	**25**	**20**	**20**	**20**	**15**	**15**	**15**
Flip chip area array*	**150**	**150**	**130**	**130**	**120**	**110**	**100**		**90**		**80**		**70**
Peripheral flip chip	**60**	**60**	**40**	**40**	**30**	**30**	**20**	**20**	**20**	**20**	**15**	**15**	**15**

*Note: *This is for solder bump flip chip. For extremely high current applications, solder bump pad pitch may be larger to allow bigger via opening to UBM. Conductive adhesive flip chip is not addressed separately but may have smaller pitches for small die applications, provided high density substrate with competitive cost is available.*

BALL GRID ARRAY PACKAGES

For many applications in the 200+ pincount range, BGA packages will provide potential solutions. Many BGAs will utilize a wire bond interconnect on the periphery of the ICs. Area array flip chip connections to BGAs will be needed for high I/O or high power chips. Laminate based ball grid arrays will require the use of underfills to reduce the shear stress load on the flip chip interconnections for large die, due to the large difference in the CTE between the silicon IC and the substrate. The bending of the encapsulated flip chip on BGAs may become excessive for large chip sizes and could impact the thermal cooling path. The space transformation between the tight pad pitch on the IC chip and the relatively large pitch between the plated through hole (PTH) on the substrate is totally contained in the BGA package. The area array solder balls beneath the BGA package have the same pitch as that of the PTH or PTH pad on the substrate. To minimize the number of signal layers on the wiring board, the signal leads underneath the BGA can be confined to the outer several rows. The inner rows are taken by the IC chip and wire bond interconnections for the cavity-down BGA. For the cavity-up BGA, the inner rows are either not used or are restricted for voltage and ground connections. Table 97 shows the maximum possible pincount for potential BGA package solutions with respect to the solder ball array pitch.

Table 97 BGA Potential Solutions

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
DRAM ½ Pitch (nm)	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*32*	*28*	*22*	*20*	*16*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
BGA Solder Ball Pitch (mm)													
Low-cost and hand-held	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
High-performance	**1**	**1**	**1**	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**
Harsh	**1**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**	**0.65**	**0.65**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**

Note: Body sizes rounded to nearest JEDEC size

FINE PITCH BGA /CHIP SCALE PACKAGES

Fine pitch BGA/chip scale packages (FBGA/CSP) provide a potential solution where low weight and small size are requirements. These packages are only slightly larger than the chip itself, and are available in a variety of configurations and materials combinations. The size may range from 4 to 21 mm as shown in Table 98. The 21 mm FBGA/CSP is for the high lead count applications. Underneath the FBGA/CSP packages, the depopulated area array solder balls are placed with a given pitch, which is a fraction of the PTH pitch on the printed wiring board (PWB). Fan-out wiring connections

are required on the PWB for each solder ball underneath the FBGA/CSP to reach a PTH in the PWB. To minimize the fan-out requirements, only a few of the outer rows of the area array connections are used. For example, with solder ball pads at 0.4 mm pitch in 2003, two 48 µm lines may be placed between two adjacent solder ball pads to access three outer rows. The detail will be given in the next section. When the number of rows accessed is four or higher, a build-up layer on the PWB will be needed, unless the line width is reduced further to 34.2 µm or less. The FBGA/CSP packages provide potential advantages of higher performance, higher density, and chip shrink transparency.

Table 98 Single Chip Packages Potential Solutions

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node		*hp90*			*hp65*			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
FBGA/CSP area array pitch (mm)	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.15**	**0.15**	**0.1**	**0.1**
FBGA/CSP size (mm/side)	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**	**4–21**

HIGH DENSITY PACKAGE SUBSTRATES AND PRINTED WIRING BOARDS (PWBS)

To accommodate FBGA/CSP solutions in 2003, the metal wiring on the top layer of the PWB needs to access the three outer rows. This means that the PWB should be capable of placing two 48 µm signal lines between the two adjacent solder ball pads at 0.4 mm pitch as indicated in Table 99. Build-up layers may be used to access the fourth and higher rows.

Table 99 BGA and FBGA/CSP Package Potential PWB Solutions

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2012*	*2015*	*2018*
Technology Node		*hp90*			*hp65*					
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*20*	*14*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*14*	*10*	*7*
FBGA/CSP solder ball pad pitch (mm)	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.15**	**0.15**	**0.1**
Pad size (µm)	**160**	**160**	**120**	**120**	**80**	**80**	**80**	**60**	**60**	**40**
Line width (µm)	**48**	**48**	**36**	**36**	**24**	**24**	**24**	**18**	**18**	**12**
Line spacing (µm)	**48**	**48**	**36**	**36**	**24**	**24**	**24**	**18**	**18**	**12**
Number of rows accessed	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

For BGA substrate, the most stringent line width/spacing needs are for the adhesive flip chip solutions suitable for small die in the low-cost applications, using pad pitch shown in Table 96. On the other hand, the assembly of adhesive flip chip is accomplished at a relatively low temperature, presenting less a concern in the substrate materials.

For the high current cost-performance and high-performance applications, solder bump flip chip solutions are needed. Due to the electromigration concern associated with high current density in the underbump metallurgy (UBM) as discussed in the materials section, the solder bump pitch should be adjusted accordingly. Table 100 uses the solder bump pitch shown in Table 96 and illustrates key substrate features expressed as a function of the flip chip pad pitch, pad size, and line width/spacing. When the outermost rows of chip pads are de-populated by 50%, one may place three lines between the pads at a two-pitch distance. For example, in 2003, one may place three 32.1 µm lines between the two pads at the 300 µm center-to-center distance. This gives four lines per two pitches, resulting in the equivalence of accessing 2.0 rows per fan-out layer, or four rows per two fan-out layers for the cost-performance applications. Similarly, one may place five 20.5 µm lines between these two pads, and achieve the equivalence of accessing 3.0 rows per fan-out layer as shown in Table 100.

All of the signal I/O pads and some of the voltage and ground pads are assumed to locate on a few of the outer rows, as shown in the Table 100. Each of these outer row pads requires a fan-out redistribution wire on the topside of the package substrate to reach a through via or PTH on the substrate. The via or PTH then connects to the global wiring in a system-

in-a-package (SiP) substrate, or it is connected to a solder ball underneath, constituting a BGA package. The numbers of leads are very often less than the pad count on the IC. These additional voltage and ground pads needed for the IC are located in the inner rows, and connected to voltage and ground pads in the outer rows. When the IC chip size is shrunk to optimize wafer productivity, flip-chip substrate redesign is usually necessary to accommodate chip shrink. A designer may place all flip-chip pads away from the chip edges, which are reserved for future chip shrink, so that a redesign of the flip-chip package substrate may be avoided after the chip shrink. This may or may not impact the number of pads needed for the targeted IC. For intermediate I/O, an IC designer may choose wire bond package so that the same package substrate may be used after chip shrink.

Global wiring solutions are addressed in the *National Technology Roadmap for Electronic Interconnections* (available from the IPC)[1] and in the *National Electronics Manufacturing Technology Roadmap* (available from NEMI)[2]. These wiring geometries are not sufficiently dense to support moving on-chip wiring onto the substrate. Substrate costs should not exceed 30–50% of the total assembly and packaging cost (cents/pin) shown in Tables 93a and 93b. A high Tg material is needed to meet the multiple cycles of high temperature Pb-free solder reflow during the chip-to-package assembly. It is important for the large chip to approach CTE matching between chip and package, and desirable between large packages and PWB. A low dielectric constant material in the substrate will reduce the capacitance load to meet the electrical performance needs. A low dielectric loss material is needed for the RF applications. And the low moisture absorption will improve the package reliability. Tables 99 and 100 illustrate the BGA, fine pitch BGA/CSP, and flip chip interconnect compatible high-density substrate solutions as a function of pitch, line width, and line spacing.

Table 100 Flip Chip Substrate Top-side Fan-out Potential Solutions

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2012*	*2015*	*2018*
Technology Node		*hp90*			*hp65*					
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*20*	*14*	*10*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*14*	*10*	*7*
Flip chip pad pitch (µm)	**150**	**150**	**130**	**130**	**120**	**110**	**100**	**90**	**80**	**70**
Pad size (µm)*	**75**	**75**	**65**	**65**	**60**	**55**	**50**	**45**	**40**	**35**
Chip Size (mm/size)										
Cost-performance	**12**	**12**	**12**	**12**	**12**	**12**	**12**	**12**	**12**	**12**
High-performance	**17**	**17**	**17**	**17**	**17**	**17**	**17**	**17**	**17**	**17**
Array Size = # pads along chip edge										
Cost-performance (maximum)	**79**	**79**	**91**	**91**	**99**	**108**	**119**	**132**	**149**	**170**
High-performance (maximum)	**112**	**112**	**129**	**129**	**140**	**153**	**169**	**187**	**211**	**241**
Wiring Substrate (Three lines replacing one depopulated pad-accessing 2.0 rows per fan-out layer)										
Line width (µm)	**32.1**	**32.1**	**27.8**	**27.8**	**25.7**	**23.5**	**21.4**	**19.2**	**17.1**	**15**
Line spacing (µm)	**32.1**	**32.1**	**27.9**	**27.9**	**25.7**	**23.6**	**21.4**	**19.3**	**17.1**	**15**
Wiring Substrate (Five lines replacing one depopulated pad-accessing 3.0 rows per fan-out layer)										
Line width (µm)	**20.4**	**20.4**	**17.7**	**17.7**	**16.3**	**15**	**13.6**	**12.2**	**10.9**	**9.5**
Line spacing (µm)	**20.5**	**20.5**	**17.7**	**17.7**	**16.4**	**15**	**13.6**	**12.3**	**10.9**	**9.5**
Wiring Substrate (Three lines between adjacent pads-accessing 4.0 rows per fan-out layer)										
Line width (µm)	**10.7**	**10.7**	**9.2**	**9.2**	**8.5**	**7.8**	**7.1**	**6.4**	**5.7**	**5**
Line spacing (µm)	**10.7**	**10.7**	**9.2**	**9.3**	**8.6**	**7.9**	**7.1**	**6.4**	**5.7**	**5**

** The pad size is assumed as 50% of pad pitch. It is usually different at different fan-out layers, e.g. from 30% to 60%*

[1] *The Institute for Interconnecting and Packaging Electronic Circuits (IPC). "National Technology Roadmap for Electronic Interconnections." Northbrook, Illinois:IPC, 1997.*
[2] *National Electronic Manufacturing Initiative, Inc. (NEMI). "National Electronic Manufacturing Technology Roadmaps." Herndon, VA:NEMI, 1998.*

CROSS-CUT ITWG ISSUES

DESIGN

With the rapid increase in device complexity and performance there has been a parallel increase in package design complexity. As a result, the need for chip and package co-design has evolved that requires integration of the design process. In the near term the ability to exchange electrical, thermal, mechanical, and geometric data between chip and package design environments is required. This data can then be used to evaluate performance and reliability. As device structures become more sensitive to small changes in electrical environment, mechanical stress, and thermal transients below the 90 nm node higher precision real time simulation of package and chip designs will be required. Packaging is also driving the pin count and power trends that the chip design TWGs have utilized to establish device complexity and performance trends.

ENVIRONMENT, SAFETY, AND HEALTH

Assembly and Packaging must consider potential risks or challenges that may be passed onto the interim buyer and the final consumer. Materials used should allow for hazard-free handling and eventual disposal or recycling. Because the majority of assembly and packaging is located offshore, multiple jurisdictions and regulatory bodies must be considered.

In general requirements for elimination of Pb-based solders in electronics and halogen-free PCB materials has been delayed several years due to the cost and complexity of implementation. However the industry is now moving aggressively to support first product roll-outs during 2002. To a large degree the packaging industry is driving this roll-out. A link to the *Environment, Safety, and Health* chapter is provided, which provides comprehensive information and a link to a new chemical screening tool (Chemical Restrictions Table).

MODELING AND SIMULATION

The cross-cut needs from Assembly and Packaging to Modeling and Simulation consist of co-design in two respects: Between chip and package, and including as well mechanical, electrical and thermal simulation. They are closely related to the requirements on Modeling and Simulation raised from the Interconnect chapter. Additionally, lower voltages and higher currents have significantly increased the need for chip-package co-design to minimize the effects of high-current transients on very low-level signal lines.

Assembly and Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Advanced modeling tools covering the related electrical, thermal and mechanical aspects are needed to support the development and optimization of these technologies. Especially important is that these effects can no longer be treated separately and must, in turn, also simultaneously be simulated. Whereas the requirements in terms of processes, materials and effects to be included in Modeling and Simulation are similar to those raised by the Interconnect chapter, the key additional requirement is the need to manage the large complexity and configurations of chip-package co-designs. This requests memory and CPU efficient hierarchical simulation capabilities to be able to deal with the high clock frequencies and high densities occurring. Reduction techniques in time-domain or frequency-domain are needed as well as computationally efficient full-wave simulation tools. Thermal and mechanical models used must be based on realistic material data, including air flow, stress predictions in accelerated test, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. These models need also to include manufacturing and assembly processes such as adhesive/undersell flow or BGA rework.

It is anticipated that near-term Modeling and Simulation needs of Assembly and Packaging will be addressed by non-optimally combining available capabilities, or by evolutionary extension of these capabilities. In the longer term it is desired that a more complete system approach will be provided.

METROLOGY

Package technology development to support the roadmap requires understanding of materials interfaces and the ability to characterize, control, and strengthen them drives assembly and packaging thermal performance, reliability yield, and cost. The ability to accurately qualify, and perhaps design and control the interface performance, will remain crucial to future cost-effective development and manufacturing. The key is to fully characterize the basic mechanisms (physical, chemical,

mechanical) for interface bond strength (adhesion) between metal/polymer, polymer/polymer, and metal/inorganic dielectric materials, as well as to quantitatively qualify the very low levels of complex organics present at these interfaces through manufacturing processes. This understanding will be crucial to improve the interface integrity.

TEST

As indicated in the packaging pin count, pad pitch, and pin pitch roadmaps there will continue to be aggressive packaging technology development to support increasing counts and finer pitches. However these developments may not be supportable from a test standpoint at acceptable cost levels. One solution to this problem is increased utilization of DFT technology that enables very high pin count products to be tested using lower pin count test systems. As noted in the packaging requirements tables the highest pin count products are also expected to have high reference to signal pin ratio's that will reduce the effective test pin counts. Pin and pad pitches, particularly for area array based interconnect will also present very significant challenges for cost effective test and new technology developments are required particularly to support the sub .5 mm ball pitches in BGA and sub-70 μm bump pitches in flip chip die.