INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

INTERCONNECT

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INTERCONNECT

SCOPE

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap emphasized a continued change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low-κ dielectric introduction for MPUs and ASICs is one of the central issues for the 2003 ITRS Interconnect area. The technical product driver for the smallest feature size remains the dynamic memory chip, however an emerging classification of chips, system-on-a-chip, or SoC, will challenge microprocessors for increased complexity and decreased design rules. Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration, combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant predicted by the ITRS has been problematic. The reliability and yield issues associated with integration of these materials with dual-Damascene copper processing proved to be more challenging than predicted. Fluorine doped silicon dioxide ($\kappa = 3.7$) was introduced at the 180 nm technology node, however insulating materials with $\kappa = 2.6–3.0$ were not widely used at the 130 nm node. These materials are expected to be in use for the 90 nm technology node. The integration of $\kappa > 2.6$ porous, low−κ materials is expected to be even more challenging. Since the development and integration of these new low-κ materials is rather time invariant, κ values will translate to lower technology nodes with any roadmap acceleration. The κ values of the bulk dielectric materials are defined in the dielectric potential solutions figure and the range of effective κ values for the integrated dielectric stack is listed in the technology requirements tables. (For a more thorough explanation, access the link to the *calculation of the effective . for various integration schemes* .) The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge.

The conductor, barrier, and nucleation potential solutions have been grouped into sections for local, Metal 1 and intermediate wiring levels, global wiring levels, as well as passive devices. Cu resistivity due to electron scattering effects will become an important factor in the long term, and is also an area of focus. Atomic layer deposition (ALD), characterized by excellent conformality and thickness control, is still receiving attention for applications in the deposition of conductors, barriers, nucleation layers and high-κ dielectric materials. Links to *expanded references to ALD* are included as supplemental material.

Figure 63 covers etch and Figure 64 addresses strip and clean potential solutions, acknowledging the increased integration challenges of these steps. For example, the etch solution for a dual-Damascene structure with and without an embedded trench etch stop are different. Requirements for pre-etch and post-etch clean, which might utilize novel approaches such as super critical CO_2, have been expanded.

Planarization potential solutions has now been split into sections for planarization of conductors and insulators. One of the primary integration challenges with low-κ materials is adhesion failure between barrier or capping materials and the dielectric during planarization. Porous low-κ materials are even more problematic and are therefore one of the key focus areas for planarization development efforts. A more detailed *schematic on the dishing/erosion/thinning metrics* shown in the technology requirements tables is found in the supplemental material link.

DIFFICULT CHALLENGES

Table 80 highlights and differentiates the five key challenges in the near term (≥ 45 nm) and long term (< 45 nm). In the near term, the most difficult challenge for interconnect is the introduction of new materials that meet conductivity requirements and reduce the dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be migrated.

Table 80 Interconnect Difficult Challenges

Five Difficult Challenges ≥45 nm/Through 2009	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control (3D CD) of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Five Difficult Challenges <45 nm/Beyond 2009	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity
Three-dimensional control (3D CD) of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual-Damascene metal structures and DRAM at nano dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

** Top three challenges*

Dimensional control is a key challenge for present and future interconnect technology generations. The dominant architecture, Damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect-ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and other micro structures, mechanical properties, ultra thin barriers and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques.

Dimensional control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and CVD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels. At the 45 nm node, feature size effects, such as electron surface scattering, will increase the effective resistivity and new conductor technologies may be required. Cu and low κ will continue to find applications in future chip generations, but

for global wiring, new interconnect solutions incorporating RF or optical propagation will be required, bringing even more material and process integration challenges.

TECHNOLOGY REQUIREMENTS

To adequately describe the wiring needs of interconnect, near term (2003–2009) and long term (2010–2018) technology requirements and potential solutions are addressed for two specific classes of products: high-performance microprocessors (HP MPU) and dynamic memory (DRAM [Tables 81–82]. For MPUs, Metal 1, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a hierarchical scaling methodology that has been broadly adopted.

Implementation of copper and low-κ materials allows scaling of the intermediate wiring levels and minimizes the impact on wiring delay. Metal 1 wiring levels are relatively unaffected by traditional scaling. RC delay, however, is dominated by global interconnect and the benefit of materials changes alone is insufficient to meet overall performance requirements long-term. Figure 54 shows the delay of Metal 1 and global wiring in future generations. Repeaters can be incorporated to mitigate the delay in global wiring but consume power and chip area.

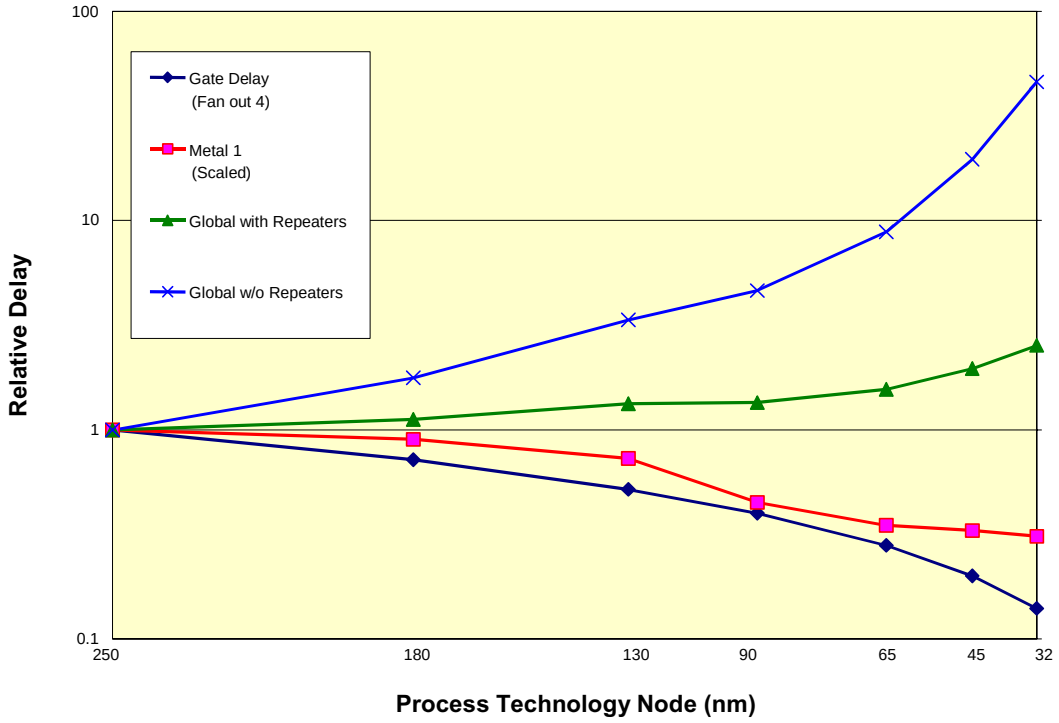


Figure 54 Delay for Metal 1 and Global Wiring versus Feature Size

As supply voltage is scaled and signal levels reduced, crosstalk has become an issue for all clock and signal wiring levels; the near term solution adopted by the industry is the use of thinner metallization to lower line-to-line capacitance. This approach is more effective for the lower resistivity copper metallization, where reduced aspect ratios can be achieved with less sacrifice in resistance as compared with aluminum metallization. The latter change expands the development timeframe to address the difficulty in integrating low-κ dielectrics into a Damascene architecture. The 2003 Roadmap continues to reflect the design trend featuring reduced aspect ratios (as an alternative means of reducing capacitance) and less aggressive scaling of dielectric.

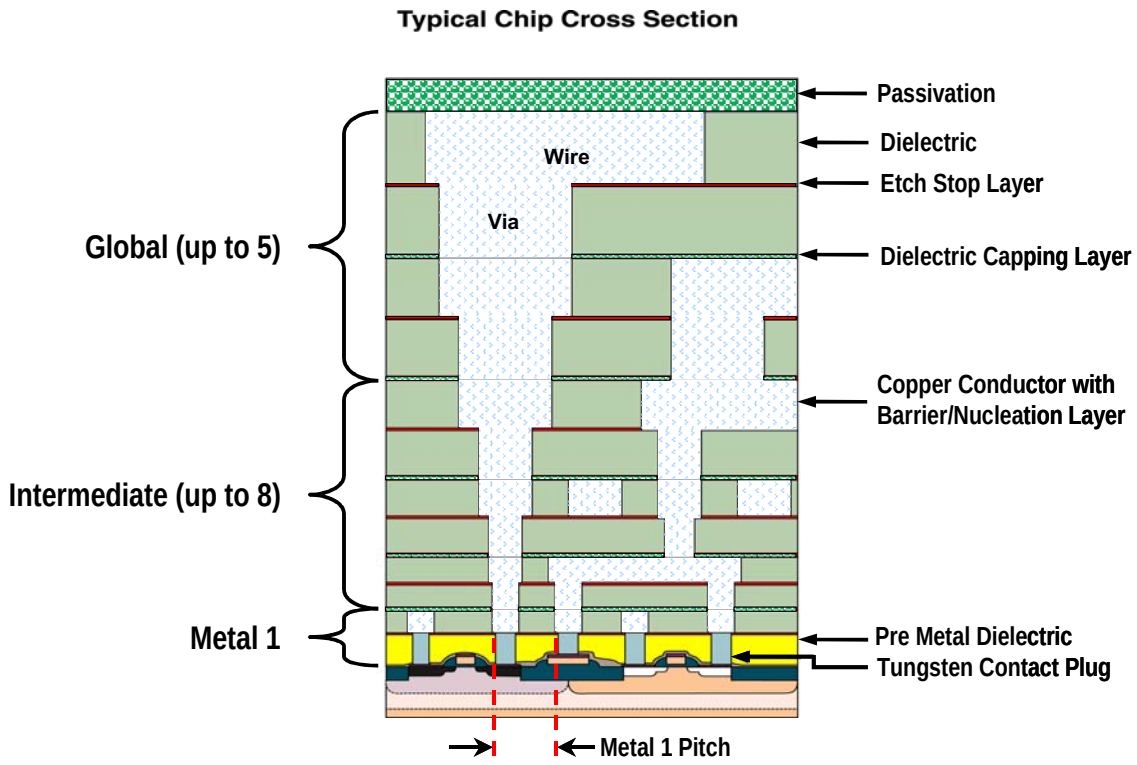


Figure 55 Cross-section of Hierarchical Scaling

Inductive effects will soon become increasingly important as frequency of operation increases, and additional metal patterns or ground planes may be required for inductive shielding.

To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified solely to meet performance requirements. Refer to Tables 81a and b. More information regarding *optional levels* is provided through a link to supplemental files.

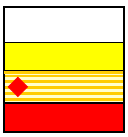
In the long term, new design or technology solutions (such as co-planar waveguides, free space RF, optical interconnect) will be needed to overcome the performance limitations of traditional interconnect.

Table 81a MPU Interconnect Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Number of metal levels	**9**	**10**	**11**	**11**	**11**	**12**	**12**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	**579**	**688**	**907**	**1002**	**1117**	**1401**	**1559**
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	**8.6**	**7.3**	**5.5**	**5.0**	**4.5**	**3.6**	**3.3**
Jmax (A/cm^2) – intermediate wire (at 105°C)	**3.7E05**	**5.0E05**	**6.8E05**	**7.8E05**	**1.0E06**	**1.4E06**	**2.5E06**
Metal 1 wiring pitch (nm) *	**240**	**214**	**190**	**170**	**152**	**134**	**120**
Metal 1 A/R (for Cu)	**1.6**	**1.7**	**1.7**	**1.7**	**1.7**	**1.8**	**1.8**
Interconnect RC delay (ps) for 1 mm Metal 1 line	**191**	**224**	**284**	**355**	**384**	**477**	**595**
Line length (mm) where τ = RC delay (Metal 1 wire)	**79**	**65**	**55**	**46**	**41**	**34**	**28**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**19**	**18**	**16**	**14**	**13**	**12**	**11**
Intermediate wiring pitch (nm)	**320**	**275**	**240**	**215**	**195**	**174**	**156**
Intermediate wiring dual Damascene A/R (Cu wire/via)	**1.7/1.5**	**1.7/1.5**	**1.7/1.5**	**1.7/1.6**	**1.8/1.6**	**1.8/1.6**	**1.8/1.6**
Interconnect RC delay (ps) for 1 mm intermediate line	**105**	**139**	**182**	**224**	**229**	**288**	**358**
Line length (mm) where τ = RC delay (intermediate wire)	**107**	**83**	**69**	**58**	**53**	**43**	**37**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**27**	**23**	**20**	**18**	**18**	**15**	**10**
Minimum global wiring pitch (nm)	**475**	**410**	**360**	**320**	**290**	**260**	**234**
Ratio range (global wiring pitches/intermediate wiring pitch)	**1.5–5.0**	**1.5–6.7**	**1.5–6.7**	**1.5–6.7**	**1.5–8.0**	**1.5–8.0**	**1.5–8.0**
Global wiring dual Damascene A/R (Cu wire/via)	**2.1/1.9**	**2.1/1.9**	**2.2/2.0**	**2.2/2.0**	**2.2/2.0**	**2.3/2.0**	**2.3/2.0**
Interconnect RC delay (ps) for 1 mm global line at minimum pitch	**42**	**55**	**69**	**87**	**92**	**112**	**139**
Line length (mm) where τ = RC delay (global wire at minimum pitch)	**169**	**132**	**112**	**93**	**83**	**69**	**59**
Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	**168**	**193**	**176**	**158**	**172**	**160**	**144**
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	**30**	**29**	**24**	**21**	**19**	**17**	**15**
Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	**12**	**10**	**9**	**8**	**7**	**6**	**6**
Interlevel metal insulator (minimum expected) – effective dielectric constant (κ)	**3.3–3.6**	**3.1–3.6**	**3.1–3.6**	**3.1–3.6**	**2.7–3.0**	**2.7–3.0**	**2.7–3.0**
Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	**<3.0**	**<2.7**	**<2.7**	**<2.7**	**<2.4**	**<2.4**	**<2.4**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



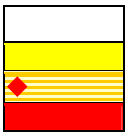
Notes for Tables 81a and 81b:
[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semi-global wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.
[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.
[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity.

Table 81b MPU Interconnect Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*54*	*42*	*38*	*30*	*27*	*21*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Number of metal levels	12	12	12	13	14	14
Number of optional levels – ground planes/capacitors	4	4	4	4	4	4
Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	1784	2214	2544	3544	4208	5035
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	2.8	2.3	2.0	1.4	1.2	1.0
Jmax (A/cm^2) – intermediate wire (at 105°C)	3.0E06	3.7E06	4.3E06	5.1E06	5.8E06	6.9E06
Metal 1 wiring pitch (nm) *	108	84	76	60	54	42
Metal 1 A/R (for Cu)	1.8	1.8	1.9	1.9	2	2
Interconnect RC delay (ps) for 1 mm Metal 1 line	616	963	970	1510	2008	2679
Line length (mm) where τ = RC delay (Metal 1 wire)	25	18	15	11	9	6
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	10	8	7	6	5	4
Intermediate wiring pitch (nm)	135	110	95	78	65	55
Intermediate wiring dual Damascene A/R (Cu wire/via)	1.8/1.6	1.9/1.7	1.9/1.7	1.9/1.7	2.0/1.8	2.0/1.8
Interconnect RC delay (ps) for 1 mm intermediate line	380	552	614	908	1203	1582
Line length (mm) where τ = RC delay (intermediate wire)	32	23	19	14	11	8
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% ' height, 50% areal density, 500 µm square array	12	10	9	7	7	6
Minimum global wiring pitch (nm)	205	165	140	117	100	83
Ratio range (global wiring pitches/intermediate wiring pitch)	1.5–10	1.5–10	1.5–13	1.5–13	1.5–16	1.5–16
Global wiring dual-Damascene A/R (Cu wire/via)	2.3/2.1	2.3/2.1	2.4/2.2	2.4/2.2	2.5/2.3	2.5/2.3
Interconnect RC delay (ps) for 1 mm global line at minimum pitch	143	220	248	354	452	618
Line length (mm) where τ = RC delay (global wire at minimum pitch)	52	37	30	23	19	13
Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	155	127	148	122	130	130
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	14	13	10	9	8	7
Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	5	4	3.5	3	2.5	2
Interlevel metal insulator – effective dielectric constant (κ)	2.3-2.6	2.3-2.6	2.0-2.4	2.0-2.4	<2.0	<2.0
Interlevel metal insulator (minimum expected) – bulk dielectric constant (κ)	<2.1	<2.1	<1.9	<1.9	<1.7	<1.7

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 81a and 81b:
[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semi-global wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.
[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.
[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity.

Table 82a DRAM Interconnect Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Number of metal layers	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Contact A/R – stacked capacitor	**13**	**15**	**15**	**16**	**16**	**17**	**17**
Metal 1 wiring pitch (nm) *	**180**	**160**	**140**	**130**	**114**	**100**	**90**
Specific contact resistance (Ω-cm^2)	**1.00E-07**	**8.50E-08**	**7.00E-08**	**5.00E-08**	**4.00E-08**	**3.50E-08**	**3.00E-08**
Specific via resistance (Ω-cm^2)	**1.10E-09**	**9.00E-10**	**7.50E-10**	**5.80E-10**	**5.00E-10**	**4.00E-10**	**3.50E-10**
Conductor effective resistivity (μΩ-cm)	**3.3**	**3.3**	**3.3**	**3.3**	**2.2**	**2.2**	**2.2**
Interlevel metal insulator – effective dielectric constant (κ)	**3.6–4.1**	**3.6–4.1**	**3.6–4.1**	**3.6–4.1**	**3.1–3.6**	**3.1–3.6**	**3.1–3.6**

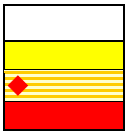
**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Table 82b DRAM Interconnect Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Number of metal levels	**4**	**4**	**4**	**4**	**4**	**4**
Contact A/R – stacked capacitor	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**
Metal 1 wiring pitch (nm) *	**80**	**64**	**57**	**44**	**40**	**32**
Specific contact resistance (Ω-cm^2)	**2.30E-08**	**1.60E-08**	**1.20E-08**	**7.70E-09**	**5.50E-09**	**3.90E-09**
Specific via resistance (Ω-cm^2)	**3.20E-10**	**2.20E-10**	**1.60E-10**	**1.00E-10**	**7.60E-11**	**5.00E-11**
Conductor effective resistivity (μΩ-cm)	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Interlevel metal insulator – effective dielectric constant (κ)	**2.7–3.1**	**2.7–3.1**	**2.7–3.1**	**2.7–3.1**	**2.0–2.4**	**2.0–2.4**

**Refer to Executive Summary Figure 4 for definition of Metal 1 pitch*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



DRAM interconnect technology reflects the most aggressive metal pitch and highest aspect ratio contacts and will continue to provide the most significant challenges in dimensional control and defect management (refer to Table 82). The introduction of low-κ dielectric materials (FSG) is underway and copper at the 65 nm ½ pitch is required to meet the performance of high-speed memory products. However, the pricing sensitivity of the marketplace may delay introduction if cost savings associated with copper are not realized. This suggests that capability for aluminum processing must be continuously improved and extended.

Damascene processing flows dominate MPU/ASIC fabrication methodologies and usage in DRAM is expected to broaden. Figure 56 illustrates several typical interlevel dielectric (ILD) architectures. While current copper Damascene

processes utilize physical vapor deposited (PVD) Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to the 22 nm generation but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of Damascene features. Surface segregated, CVD, ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required.

Near-term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for decoupling and metal insulator metal (MIM) capacitors and materials with high remanent polarization for ferroelectric memories. The thermal, mechanical, and electrical properties of these new materials present a formidable challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials will be required that have sufficient optical contrast to serve as low-loss waveguides.

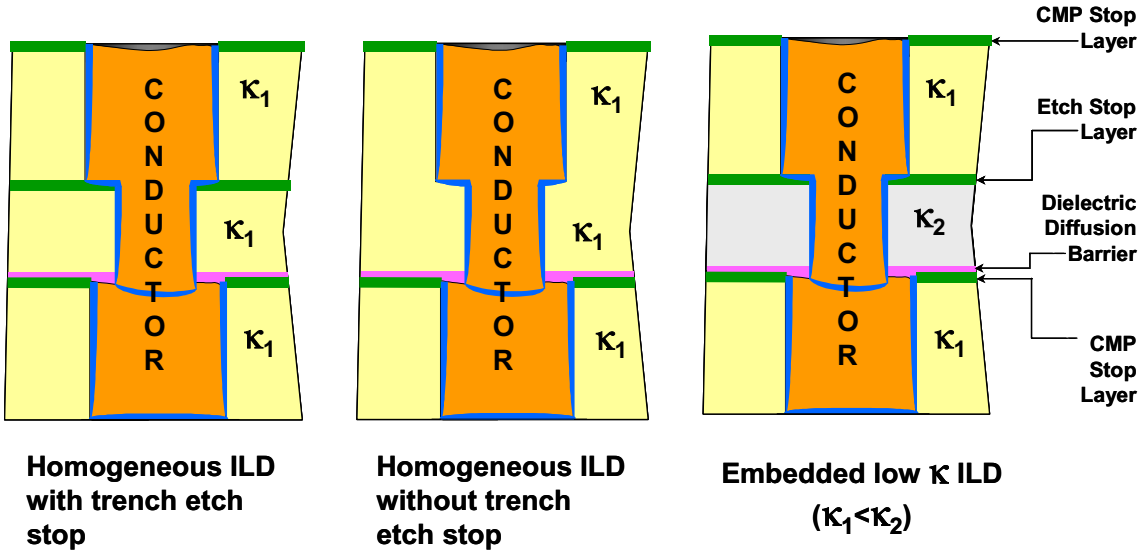


Figure 56 Typical ILD Architectures

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long-term solution. For copper CMP, minimization of erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Planarization processes (with associated end-point) that are compatible with low-κ dielectrics that may have low density and poor mechanical strength must be developed. Improvements in post-CMP clean will be critical in achieving the low defect densities required for future devices. Etch, resist strip, and post-etch cleans must be developed which maintain the desired selectivity to etch stop layers and diffusion barriers, but which do not degrade low-κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

POTENTIAL SOLUTIONS

DIELECTRIC POTENTIAL SOLUTIONS

The previous ITRS documents have indicated a growing concern that the changes in the dielectric materials used through the 130 nm technology node are minor compared to the future technology needs and far more revolutionary in nature than the evolutionary path followed to date. This range of new dielectric material requirements encompasses both conventional and novel device architectures as well as almost every existing end use. Some dielectric materials are finding additional uses in alternate locations of the BEOL structure with new emphasis on required electrical, mechanical and processing properties. Even with new ever more stringent requirements for future technology nodes, the lifetime of the existing class of dielectric materials has been extended because of problems with the properties or integration of the new materials. The two most obvious and often cited examples are the delay in implementation of high-κ materials for DRAM capacitor structures and the failure to achieve integration of true low-κ (κ<3.0) interlayer dielectric (ILD) materials in large volume manufacturing.

The following three overall BEOL dielectric challenges remain valid throughout the 15-year scope of this roadmap:

- Development of true low-κ materials and manufacturing processes capable of achieving the minimum effective permittivity (κ_{eff}) possible, for maximum device performance at a viable performance/price ratio, for Cu dual-Damascene technology
- Development of moderate (κ>20) to high (κ>100) permittivity materials and manufacturing processes capable of achieving continually higher bit density at a viable bit/price ratio for stand-alone memory applications, decoupling and (MIM) capacitors for MPU/ASICs and system-on-a-chip (SoC).
- Sufficient development activity focused on invention and integration of new materials for emerging technologies to replace conventional wiring based electronics with alternatives, such as RF, optical and bio-based interconnect.

To address the range of dielectric material requirements and add focus to each specific application within the BEOL, which will encompass the dielectric requirements for Pre-Metal Dielectric (PMD) for the first time, the Dielectric Potential Solutions figure has been divided into applications instead of arbitrary groupings by dielectric permittivity.

PRE-METAL DIELECTRIC (PMD)

Improvements or changes in the technology used to deposit pre-metal dielectric (PMD) layers will be required. These changes will be driven by the move to NiSi, increases in the aspect ratios of spaces between adjacent gates in DRAMs and the simultaneous requirement for high phosphorous doping concentrations and low thermal budgets in NOR-type flash memories.

The increasing use of NiSi doped junctions and gate conductors in logic circuits will challenge those deposition technologies that require anneals above 450°C to 490°C. Thermal budget restrictions should also accompany the introduction of metal gates, however, these are likely to fall within the same range dictated by NiSi. This problem is intensified when high phosphorous doping concentrations are also required. Some NOR-type flash memories already incorporate NiSi while requiring PMD phosphorous concentrations as high as 10% to meet charge retention requirements. This could prove to be an insurmountable challenge for purely thermal deposition processes.

The aspect ratios of the spaces between adjacent gates in DRAMs are expected to reach 16:1 by 2005 and continue to increase thereafter. As a result, DRAM PMD deposition by plasma-based processes could become increasingly problematic. Plasma induced damage (PID) of thin gate dielectrics by plasma based PMD deposition processes has not proven to be a significant issue to date. However, it will continue to be an area of concern as gate dielectrics become thinner and/or are replaced by new high-κ materials.

Finally, low-κ dielectrics will be required for DRAMs for the layer incorporating bitlines in order to reduce capacitance. For example, κ_{eff} values ranging from 2.7 to 3.1 will be required by 2010, decreasing to 2.0 to 2.4 by 2018. It is conceivable that future PMD deposition processes will incorporate multiple steps, and possibly multiple process types, in order to satisfy the requirements of gap fill, thermal budget and doping concentration.

INTRA-METAL DIELECTRIC (IMD)

The introduction of FSG (κ=3.7) at the 180 nm technology node in conjunction with Cu dual-Damascene process integration represented the first major break in the historical extension of silicon dioxide (κ=4.1) and aluminum in the IC

industry. Although relatively minor in variation from silicon dioxide, issues of fluorine mobility, reactivity with refractory metal based barrier layers, adhesion and moisture sensitivity required the expenditure of significant engineering resource over a number of years to develop a truly robust manufacturing process.

The daunting task of implementing low-κ interlayer dielectric materials (κ<3.0) has magnified these integration challenges by at least one or two orders of magnitude. Concurrent with this low-κ materials introduction is a migration of metal barrier deposition technologies (PVD→CVD→ALD) as well as the continued reduction in barrier thickness to maintain the targeted Cu resistivity. The combination of these integration challenges, coupled with design improvements to alternately address projected cross-talk and RC delay problems, has resulted in an extension in the industry wide implementation of low-κ ILD material past that proposed in the last three ITRS documents.

The preferred integration scheme for silicon-based dielectric materials continues to be the original "full-via-first" process implemented with silicon dioxide at the 250 nm node. Organic-based dielectric materials have usually adopted a dual inorganic hardmask scheme. In an effort to optimize performance and minimize integration complexity, organic/inorganic hybrid dielectrics have been discussed.

Many electrical simulation models exist to extrapolate these values from well-controlled test structures within a die. In the *supplemental file* simulation extraction results for representative low-κ integration schemes are presented for several technology nodes. The model inputs are specific to the ITRS targets for layer thickness, aspect ratios and dielectric materials projected to be commercially available concurrent with proposed manufacturing ramp timings.

Several integration challenges associated with etch selectivity/damage, 193 nm photoresist, Cu CMP and packaging process compatibility are still areas of significant effort across almost all low-κ dielectric materials. Historically derived material property relationships of physical, mechanical and electrical properties have not reliably predicted integration success. Therefore a steep learning (reinventing) curve is in progress throughout the industry. Fortunately, no new electrical or electromigration failure modes have been identified and attributed directly to any low-κ dielectric material. The technical community still maintains a healthy debate about microstructure requirements for porous dielectric materials with respect to pore size, pore shape, aspect ratio and degree of interconnectivity (open *versus* closed).

HARDMASK

This is a generic term used to describe the dielectric film deposited on top of the trench level intra-metal dielectric. It has two main functions—1) to assist in patterning of the dual-Damascene structure for subsequent metal fill and 2) as a highly selective CMP stop layer. In addition, this layer is called upon to prevent fast diffusion of acid or base moieties that could interact detrimentally with the traditional acid catalyzed photoresist systems employed at 248 nm and 193 nm. Depending on the efficiency of CMP and acid/base moiety inhibition, this layer could be inconsequential to the over all κ_{eff} or a significant contributor. For most integration schemes, the composition of this layer can be chosen independently of most other dielectric layer choices. However, in the case of the hybrid integration scheme it is best to have the hardmask dielectric material and the via layer dielectric material similar to simplify the etch sequence. There are currently both spin-on and CVD deposited solutions available with dielectric constant values down to at least 3.0. Some spin-on offerings are available down to a dielectric constant value of 2.2.

ETCH STOP—VIA

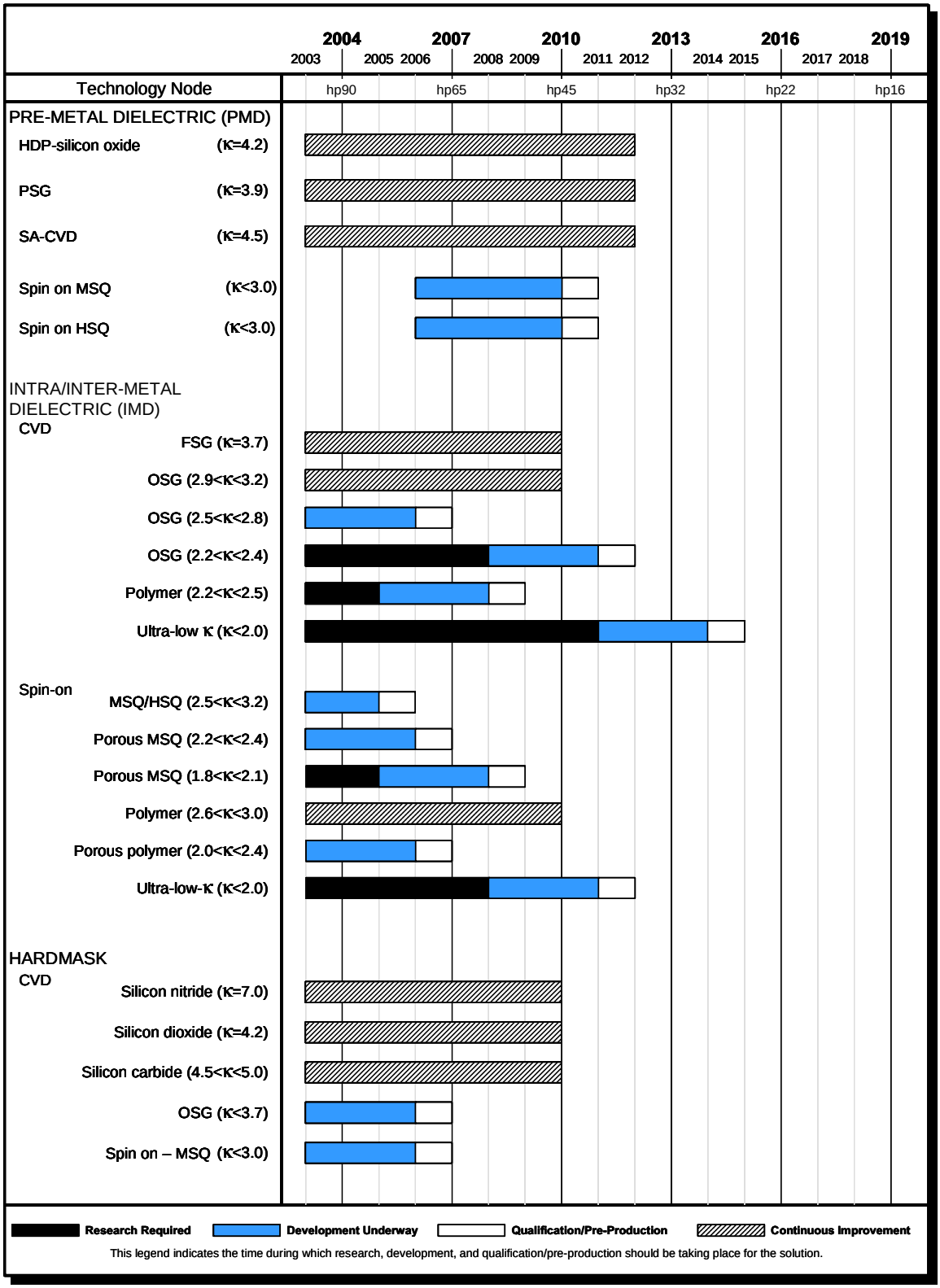
The via etch stop layer also has two main functions. It must have significant enough etch selectivity with respect to the via dielectric layer so that etching of the underlying IMD adjacent to non-landed vias is avoided. This via etch stop also serves as the capping layer for the underlying Cu wiring layer. It must be a Cu diffusion barrier and have acceptable adhesion and interface properties so that Cu electromigration requirements are met. The via etch stop layer can also be a significant contributor to overall κ_{eff} so its thickness and κ value should both be minimized.

ETCH STOP—TRENCH

The primary function of this dielectric layer is to provide enough etch selectivity, as compared to the trench level dielectric, to form a smooth, well-defined trench bottom. Significant trench bottom roughness can be a reliability issue if it affects metal barrier coverage. Variability in trench depth can be a significant contributor to variation in metal line resistance. Alternate integration schemes, like a hybrid ILD structure, have eliminated the need for a discrete trench etch stop layer by incorporating these requirements in the via level dielectric.

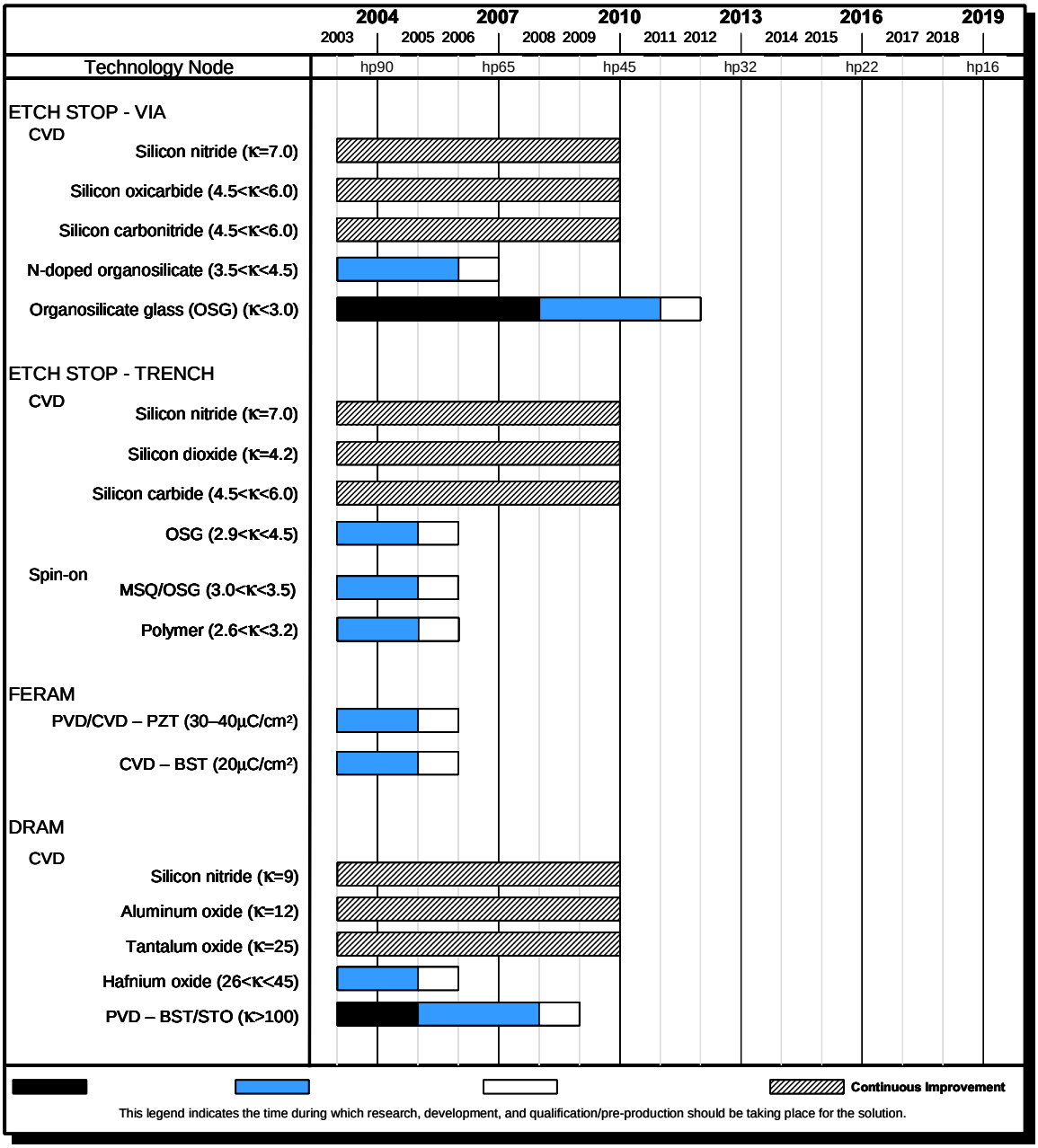
DRAM

DRAM technology has just begun the arduous process of implementing the assortment of medium dielectric constant materials ($5<\kappa<40$) in stacked capacitor structures. The trench defined DRAM technology could possibly delay the implementation of these medium dielectric materials for an additional technology node because of the enhanced active area available. Both DRAM technologies will develop an understanding of these medium dielectric constant materials as a stepping-stone to the higher κ (> 40) alternatives. These high dielectric constant materials, again, are most likely to be implemented in stacked capacitor structures (DRAM) initially, followed by trench capacitor structures, before they are considered as replacements for silicon dioxide gates.



HDP—high density plasma SA-CVD—sub atmospheric CVD PSG—phospho-silicate glass MSQ—methyl silsesquioxane HSQ—hydrogen silsesquioxane FSG—fluorinated silicate glass OSG—organosilicate glass

Figure 57 Dielectric Potential Solutions



PVD—physical vapor deposition PZT—Pb(Zr,Ti)O4 BST—barium strontium titanate STO—strontium titanate

Figure 57 Dielectric Potential Solutions (continued)

CONDUCTOR POTENTIAL SOLUTIONS

Local wiring, which is sometimes called M0, is limited to very short lengths for contacts and adjacent transistors. Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, ASICs and DRAMs. ALD, in conjunction with CVD techniques, is being utilized first in the W deposition area to accomplish a seamless W fill. The absence of seams at the local wiring or contact level is especially important when the subsequent wiring level is ECD copper in order to avoid defect issues associated with retained plating solution.

Continued development of ALD tungsten deposition will be needed to accomplish W fill of high aspect ratio (17:1 in 2009) contacts for stacked capacitor DRAM designs. Alternate materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts, which are projected to have aspect ratios greater than 20:1 by 2012. Aluminum may continue to be used for local wiring and enhanced CVD/PVD flow techniques will continue to be improved for Damascene architectures.

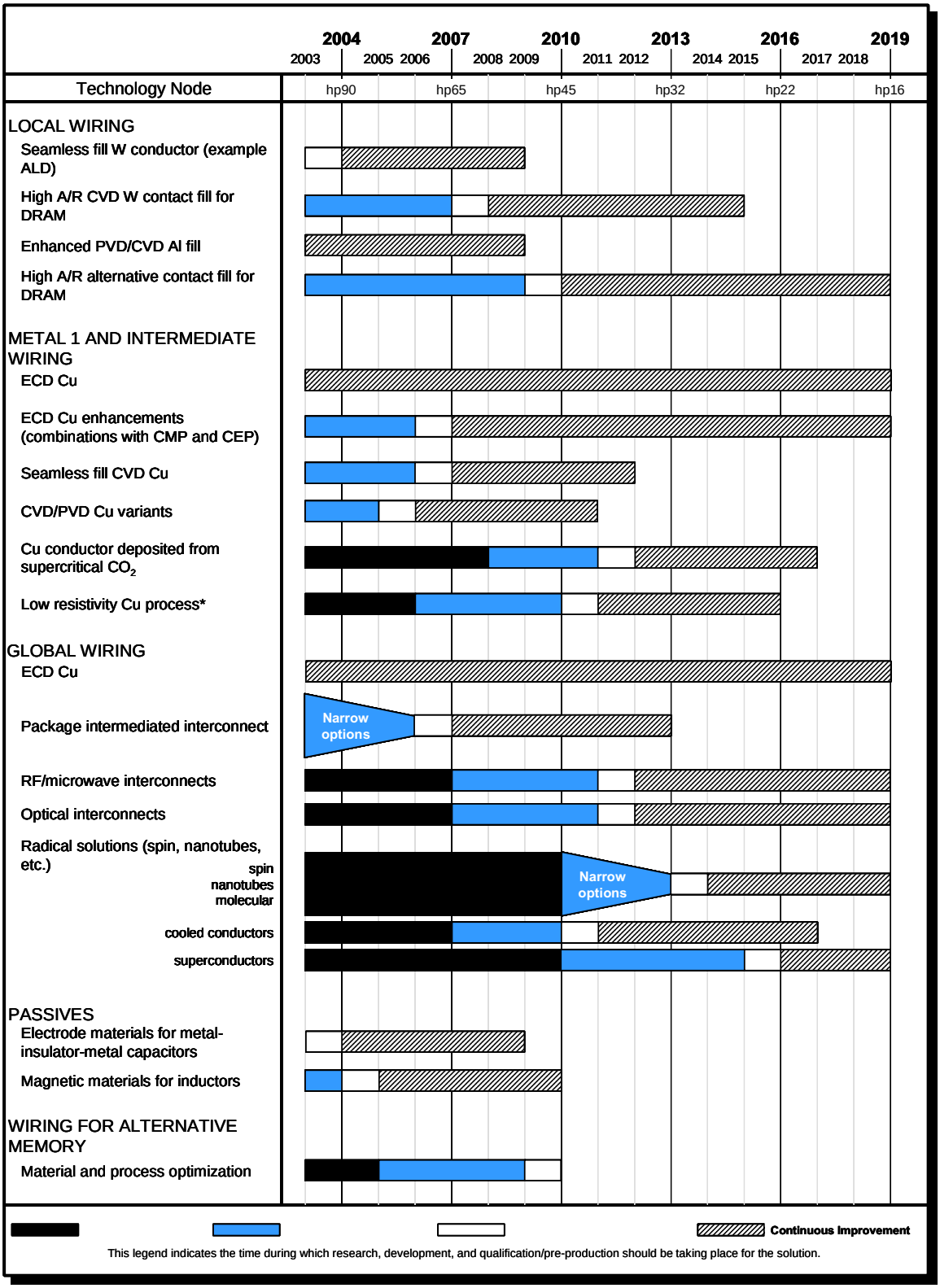
Cu will be the preferred solution for the Metal 1 and intermediate wiring levels in microprocessors and ASICs and electrochemical deposition will continue to dominate the market in the near term. There will be continuous improvement in the plating chemistry and ECD tool design to allow seamless fill of smaller geometry higher aspect ratio structures. Development is also underway to accomplish both deposition and planarization in a single tool by combining ECD with CMP or CEP.

CVD Cu fill may become competitive as a fill technology if the same "superfilling" behavior and microstructure characteristic of ECD can be achieved. Alternatively combinations of CVD and PVD Cu may be employed to accomplish seamless fill at smaller geometries. Deposition of Cu and other conductors from supercritical CO_2 solutions is still in the research phase but is also a promising technology.

Metal 1 Cu wiring will be the first to be impacted by the size effects that will increase Cu resistivity toward the end of this decade. Soon thereafter, size effects will also increase Cu resistivity for the intermediate wiring levels. This is much more problematic since intermediate wiring traverses longer lengths and is more likely to impact performance than Metal 1 wiring. Cu interfaces, microstructure and impurity levels will need to be engineered to alleviate the impact of this resistivity rise for a few additional technology generations.

Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. However, scaling at each technology generation has the largest impact on global wiring levels that nominally traverse lengths on the order of the die size. This problem is currently being addressed by the intelligent use of repeaters, or by oversized drivers, but they impact both chip size and power. The most likely near term solutions are appropriate use of design and signaling options, packaging or 3D interconnects to minimize the effect of these resistive global wires. A great deal of research is also underway on the use of either RF or optical techniques to resolve this issue. More radical solutions include cooled conductors, superconductors, nanotubes etc. All of the above global wiring alternatives are discussed in greater detail in the new concepts section of the Interconnect roadmap.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of metal-insulator-metal (MIM) capacitors to improve yield and reliability. Both Al and Cu are currently in use for standard spiral inductors, but in the future various magnetic materials may emerge with different inductor designs to reduce the area of these devices.



ALD—atomic layer deposition ECD—electrochemical deposition CMP—chemical mechanical planarization
CEP—chemically enhanced planarization
**Cu process with optimized interfaces, microstructures, and impurities to alleviate resistivity rise at small critical dimensions*

Figure 58 Conductor Potential Solutions

BARRIER POTENTIAL SOLUTIONS

Barriers for tungsten local wiring and contact fill will continue to utilize Ti/TiN films. There will be continuous improvement on established deposition techniques such as long throw and ionized PVD and CVD to improve compatibility with the new seamless W technology. CVD Ti/TiN barriers will continue to be improved for high aspect ratio contacts (e.g., DRAM stacked capacitors) filled with W conductor. Development of ALD Ti/TiN along with ALD W is underway and is likely to improve the overall seamless W fill process by eliminating the "pinch off" of the contact hole characteristic of other deposition techniques.

Conventional PVD and CVD barrier technologies will be continuously improved to allow Al fill to be extended to higher aspect ratio structures, however it is likely that ALD barriers will also replace these techniques in the future. Research is also underway to explore alternate materials and fill techniques for high aspect ratio contact structures that would allow simplification of the current contact/barrier/conductor film stack.

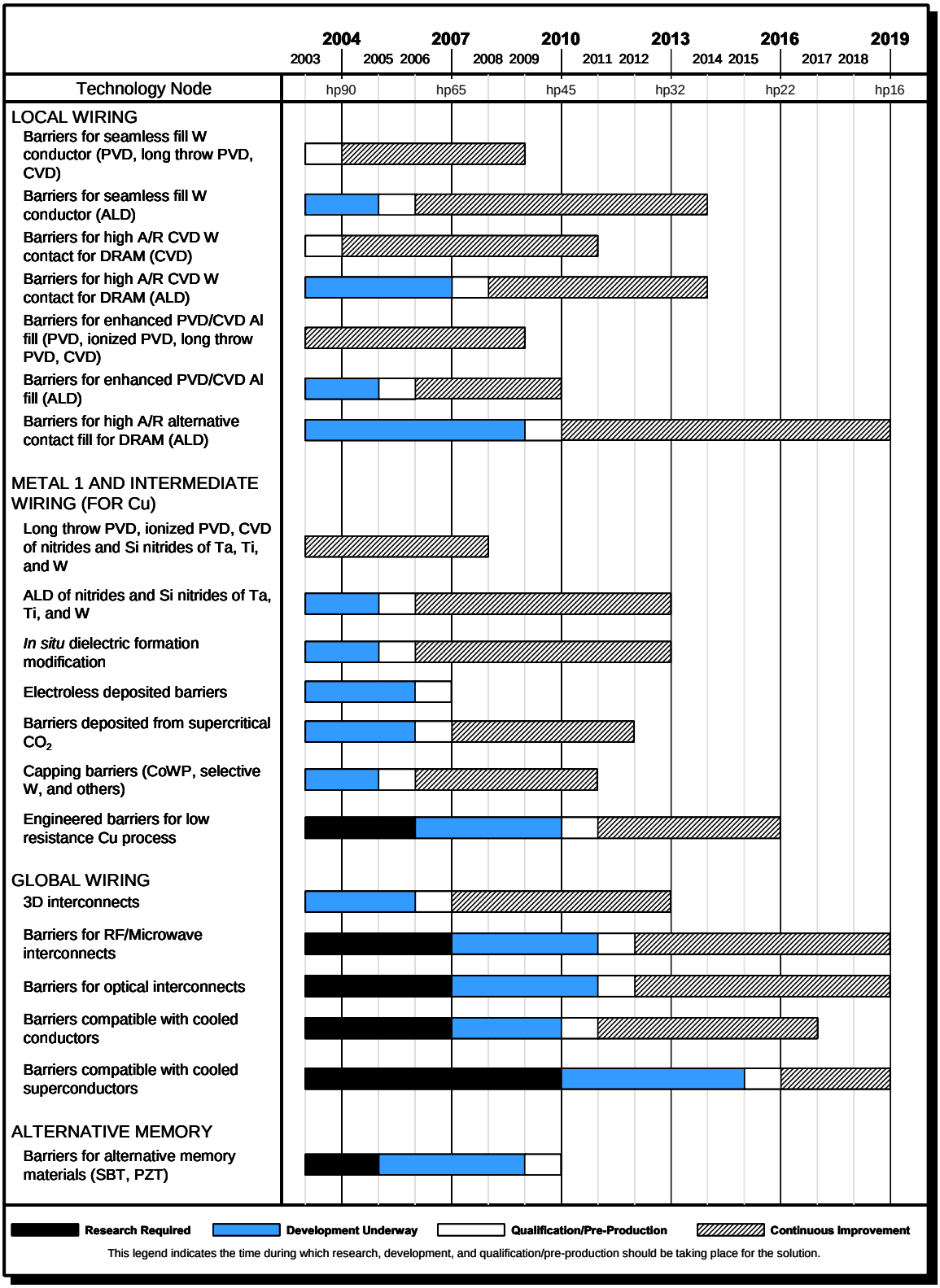
Barrier materials used for Cu wiring must prevent Cu diffusion into the adjacent dielectric and must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta has become the predominant industry solution but other nitrides and silicon nitrides of Ta, Ti, and W have also shown promise.

Long throw, ionized PVD, and CVD depositions will continue to be improved to meet the very challenging sidewall coverage requirements of future dual-Damascene structures. However, even the most advanced of these deposition techniques tend to narrow the upper part of the dual-Damascene trench and limit the fill capability of the ECD Cu process. A great deal of effort is underway to develop ALD barriers that are expected to become the predominant future solution for copper.

One major obstacle to the adoption of ALD for barriers is penetration of the precursor materials into the porous low-κ dielectrics targeted for future technology nodes. *In situ* modification of the etched low-κ sidewalls may be used either with ALD or as a standalone barrier solution to resolve this issue. Development is also underway to explore deposition of barriers by electroless techniques and from supercritical CO_2.

Another focus area for metal barriers is the top surface of the Cu dual-Damascene structure. Dielectric Cu barriers such as Si_3N_4, SiCN and SiC currently predominate for this application, however they are not the preferred solution because their higher κ values increase the overall κ_{eff} of the structure. Selective metal capping barriers such as W or CoWP are being explored for this application.

Finally, a great deal of research and development in the area of advanced barrier materials and deposition techniques will be needed. Engineering the smoothness and other properties of the Cu barrier interface will be key to ameliorating the expected Cu resistivity increase due to electron scattering effects.



SBT—strontium barium titanate

Figure 59 Barrier Potential Solutions

NUCLEATION POTENTIAL SOLUTIONS

The conformality and coverage of the nucleation layer is often the critical factor in determining whether the subsequent conductor deposition will be seamless or free of voids. For local wiring and contact fill, there will be continued improvement in ALD W nucleation layers that have been used to enable seamless or high aspect ratio W fill. In the area of Al fill, the CVD Al nucleation layer may be extended to ALD to allow continuous improvement in the fill characteristics of this technology.

Development is still underway for alternative materials and processes for high aspect ratio DRAM contacts but ALD nucleation layers will likely be needed for this technology.

For Metal 1, Intermediate and Global wiring, enhanced PVD Cu, deposited through either long throw or various ionized techniques, continues to be the dominant nucleation layer for ECD Cu. There will be improvement of these enhanced PVD techniques and they will continue to be used, especially on the global wiring levels with larger critical dimensions. However, these enhanced PVD techniques have marginal extendibility to next generation dual Damascene structures and various Cu nucleation layer alternatives are being explored.

There continues to be research for both electroless and CVD Cu nucleation layers and development is already well underway on deposition of Cu nucleation layers using either ALD or supercritical CO_2. Another potential solution to the problem of marginal PVD Cu sidewall coverage is repair of the nucleation layer through ECD techniques. A more elegant solution to the problem involves modification of the ECD process and/or barrier to be self-nucleating thereby eliminating the need for a Cu nucleation layer.

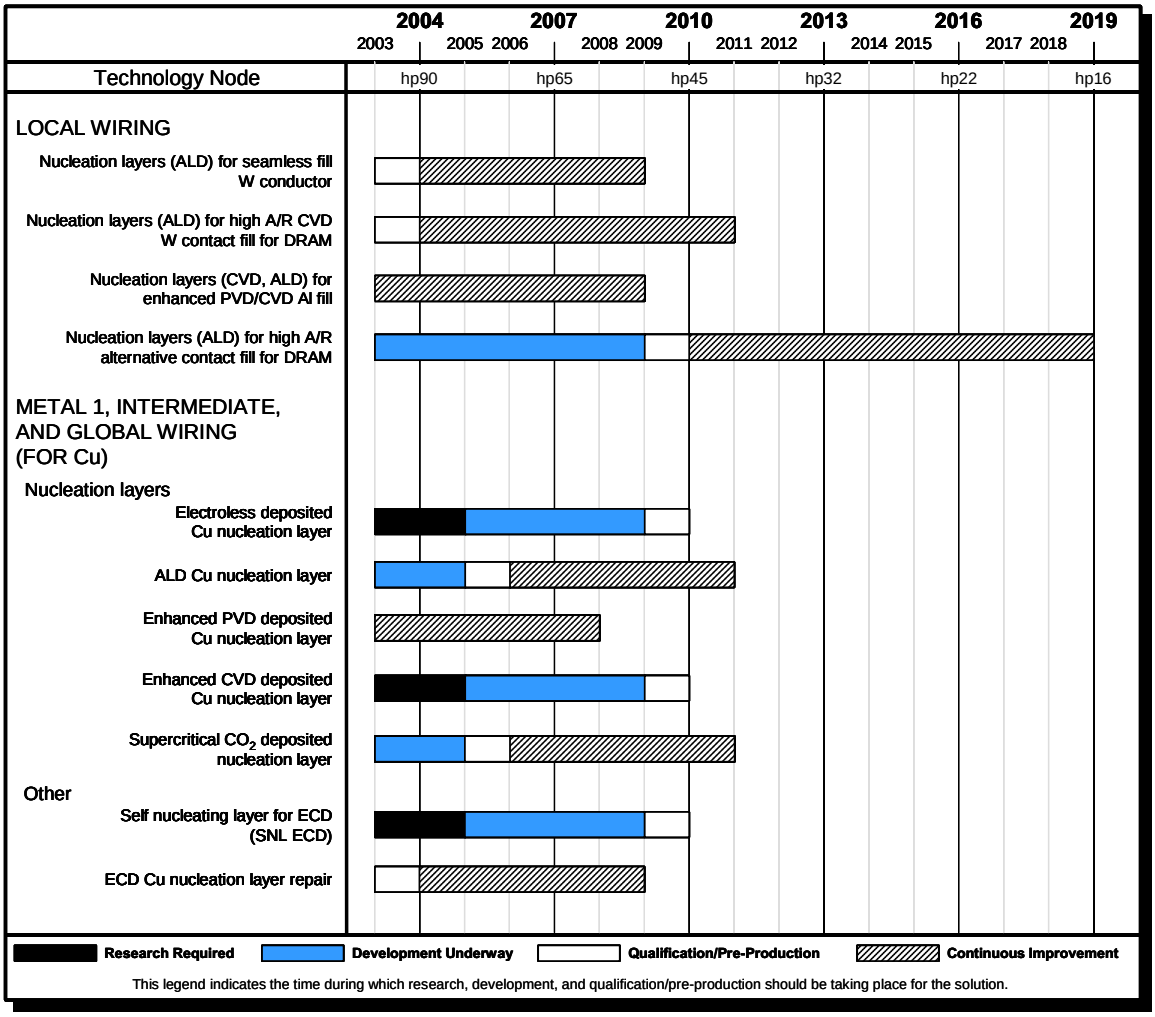


Figure 60 Nucleation Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Increasingly, planarization has become an enabling step for interconnect technology. As materials and structures become less conventional and demands on planarization tolerances become more exacting, planarization processes themselves become more closely coupled to the choice of integration scheme. Chemical-mechanical polishing (CMP) and near alternatives remain the leading planarization technologies for current and future manufacturing. The combinations of materials and structures that define a CMP application continue to grow. Each application has unique needs and may dictate unique solutions.

The CMP of doped silicon dioxide for pre-metal dielectrics (PMD) and CMP of tungsten for local interconnect and contacts will remain a requirement for the foreseeable future. PMD is an example of where multiple applications can exist with similar materials. Target PMD CMP stops at a target thickness within a film, similar to interlevel dielectric (ILD) CMP. Selective PMD stops on or in an underlying film with selectivity to optimize topography. Polysilicon CMP is utilized today in making memory devices.

ILD CMP and tungsten via CMP are slowly being reduced. They are being replaced with Cu dual-Damascene CMP with the adoption of copper damascene processes.

Copper and barrier CMP are standard processes for leading edge logic devices and adoption for memory devices and other logic devices will follow. The dielectric materials into which copper damascene features are built are on a path of decreasing κ values over time. Each change in dielectric materials brings new metal planarization challenges. Among these is the need to reduce the mechanical forces applied to the wafer during CMP, in order to prevent adhesive/cohesive failures in the dielectric, due to the reduced mechanical strength of ULK dielectrics. Although this problem can be alleviated through integration choices, including the use of capping layers, an effective dielectric constant performance penalty is likely. Integration can also include hardmask films that need to be removed to avoid the penalty.

As minimum wire dimensions scale with each new technology node, the primary influence that planarization has on control of wire thickness becomes increasingly important. Thickness variation of Metal 1 and intermediate Cu wiring at minimum pitch is a result of pattern erosion during CMP. Thickness variation of the global wiring results from both pattern erosion and dishing of the individual wires. With the projected scaling of wire thickness, it is likely that Cu variation due to CMP must be limited to less than 10% of the nominal thickness for any interconnect level.

Topography after Cu and barrier CMP leads to conductive defects at subsequent interconnect layers. Topography needs are also driven by depth of focus in lithography, and these will continue to become tighter with each technology node, especially at 32 nm and beyond. Tighter control of metal planarization will be addressed by improvements in all facets of CMP, including tools (end point, removal non-uniformity, process parameters), slurries (selectivity, recess), and pads (planarization lengths). Techniques for more planar depositions may also contribute.

Related *links* are provided for thinning of the Metal 1 and intermediate Cu wiring at minimum pitch; thinning of the global wiring from both pattern erosion and dishing of the individual wires, and wide global features and Cu dishing from CMP.

Development will continue in alternative metal planarization techniques. These include Chemically Enhanced Planarization (CEP), electropolishing, and Electro-chemical-mechanical polishing (ECMP). These alternatives may offer advantages for productivity or erosion, but especially for low stress compatibility with weak/porous dielectrics if the issues with each are solved. Implementation may hinge around the adoption of ultra low κ dielectrics.

Planarization tools for metal CMP must evolve so that Cu can be polished in advanced dielectrics. The current breed of tools all control relative speed and distributed force to the wafer surface, with techniques to enhance cross-wafer slurry transport. Various polish endpoint detection techniques are used, with inline dielectric thickness metrology as an available option. Integrated wafer cleaning has become standard for metal planarization tools.

It is important that future tools be designed for processing Cu in low-κ and ultra low-κ dielectrics in a low-shear-force region of the CMP process space. In addition to the above features, the next generation tool for manufacturing may include tribological metrology to measure frictional forces, and *in situ* (or inline) metrology for dielectric and metal thickness, planarity, defects/residuals, and reliable full-wafer endpoint detection for both Cu and barrier films. These features will enable a machine-tunable, radially-uniform, polish and allow an improved implementation of automatic

process control (APC). The polisher may have fully integrated slurry metrology and incorporate a number of "green tool" features. These needs may require novel tool designs.

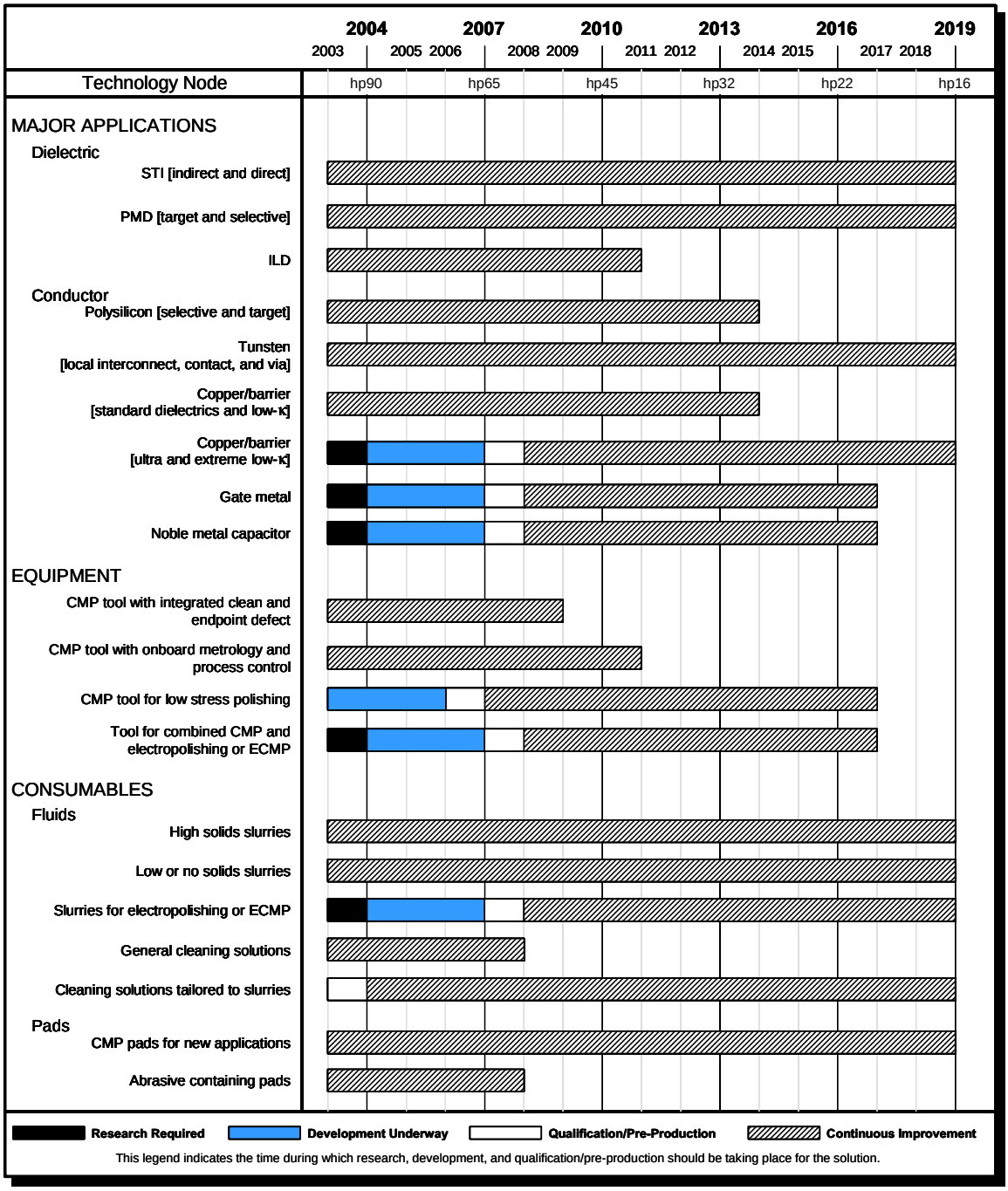
Tribological metrology may be fully integrated for active force control. Metrology and active control of the wafer surface temperature will become increasingly important to control the polishing chemical reaction. Tools may have the capability of precision "point-of-use" slurry mixing, and a green tool design should be well established.

Advances in CMP consumables will share equal importance with tools in enabling future metal planarization. The attention focused on polishing slurries has resulted in significant improvements in the mean and variation of their performance. Producing slurries with controlled selectivities for Cu/barrier/dielectric has allowed the user to engineer the polish sequence for minimal Cu thinning. At the same time, attention must be paid to the slurry's role in creating scratch and residual defects on the Cu wires and dielectric surfaces, and corrosion of the Cu wires. The RMS roughness of the polished Cu surface will become important, as interface scattering effects start to influence the conductivity of small wires.

The advent of low or no solids CMP chemistries for Cu may improve manufacturing margin through improved selectivity and dishing control, two areas that may also be addressed by improved pads. Development of new abrasive materials with engineered chemical-physical properties and engineered pad materials both may lead to enhanced precision and defect performance in metal polishing processes. A materials pathway to a low shear force metal polish is a potential solution.

For CMP consumables, it is expected that a path of continuous improvement will be taken on existing applications. The introduction of new CMP applications for new circuit materials will continue and will drive development of consumables beyond the introduction of lower κ materials. Examples of this may include moving away from polysilicon for both gate conductors and for metal capacitors. For the metal gate case, the choice of integration scheme will dictate whether CMP is needed. Beyond the 45 nm node, it is very likely that new applications will continue to be created with new materials and device structures.

Post-CMP wafer cleaning will likely become more closely integrated with the metal planarization process. With respect to tools, the combined polisher/cleaner for Cu CMP is common in manufacturing. The brush scrubber, in combination with megasonic and chemical treatments, is currently favored. The chemistries employed for cleaning are now formulated for metal applications, and in the future may need to be tailored for the specific slurry and CMP process with which they are used. Since the chemical characteristics of the cleanable defects are more and more determined by the slurry used and the polishing byproducts, closer collaboration between the slurry providers, chemical providers, and end user will be required. Metal corrosion remains a concern, as it is often tied to the specifics of the metals deposition. Development will continue on alternative cleaning technologies.



STI—shallow trench isolation ECMP—Electro-chemical-mechanical polishing

Figure 61 Planarization Potential Solutions

ETCH POTENTIAL SOLUTIONS

Future etch technology development, in support of future projected BEOL requirements, will include both dielectric and conductor classes of materials. Within the class of dielectric materials requiring etch development for logic designs, compositions as diverse as inorganic, hybrid inorganic/organic and wholly organic are anticipated to be driven by the dielectric roadmap contained within the Dielectric Potential Challenges section in this ITRS document. Continual optimization of existing capacitively coupled based source technology is envisioned to adequately address the progression of shrinking line/space dimensions and associated via/contact diameters while overall aspect ratios maintain parity with current technology. Future memory technology development will require the introduction of progressively higher dielectric materials to partially offset cell area reductions. These materials as a class exhibit very low volatility by-

products. The high aspect ratio contact etch is expected to be continually challenged based on ever increasing aspect ratios for each new technology node. It is anticipated that current inductively coupled source equipment will continue to address future needs.

Conductor etch requirements include the continuation of the stalwart Al etch, to at least the 90 nm technology node using existing inductively coupled plasma source technology. The introduction of progressively higher dielectric materials in support of future memory technology development are also anticipated to require new top and bottom metal electrode materials like noble and refractory metals. Currently, etch of these metal electrode materials are being addressed with existing capacitively coupled source equipment.

New interconnect and/or package technologies (e.g., 3D IC discussed in a later section) are moving into manufacturing. One of the key technology challenges of this technology is the need to etch 100 micron vias from the interconnect layers, through the entire wafer providing for electrical (or sometimes thermal) connections on the back of the die. The use of Xenon containing gas mixtures will be critical.

Etch process technology development, in support of the dielectric etch of dual-Damascene structures, has highlighted the importance of the etch mask stack configuration. Integration engineers continue to optimize the discrete number of individual layers, within the etch mask stack (one, two, three), the compositional makeup of the individual layers within the etch mask stack, as well as the sequence of etch (and strip) operations as shown in Figure 62. The function of the etch mask stack is a combination of high etch selectivity (>20:1) during etch of the underlying dual-Damascene configuration (usually via definition) and etch parity to enable discrete layer removal or simultaneous pattern definition and etch of some underlying structure. Existing examples of inorganic, organic, hybrid inorganic/organic and metal are documented in the technical literature and it is foreseeable that all of these classes of materials will be used in combination for the foreseeable future.

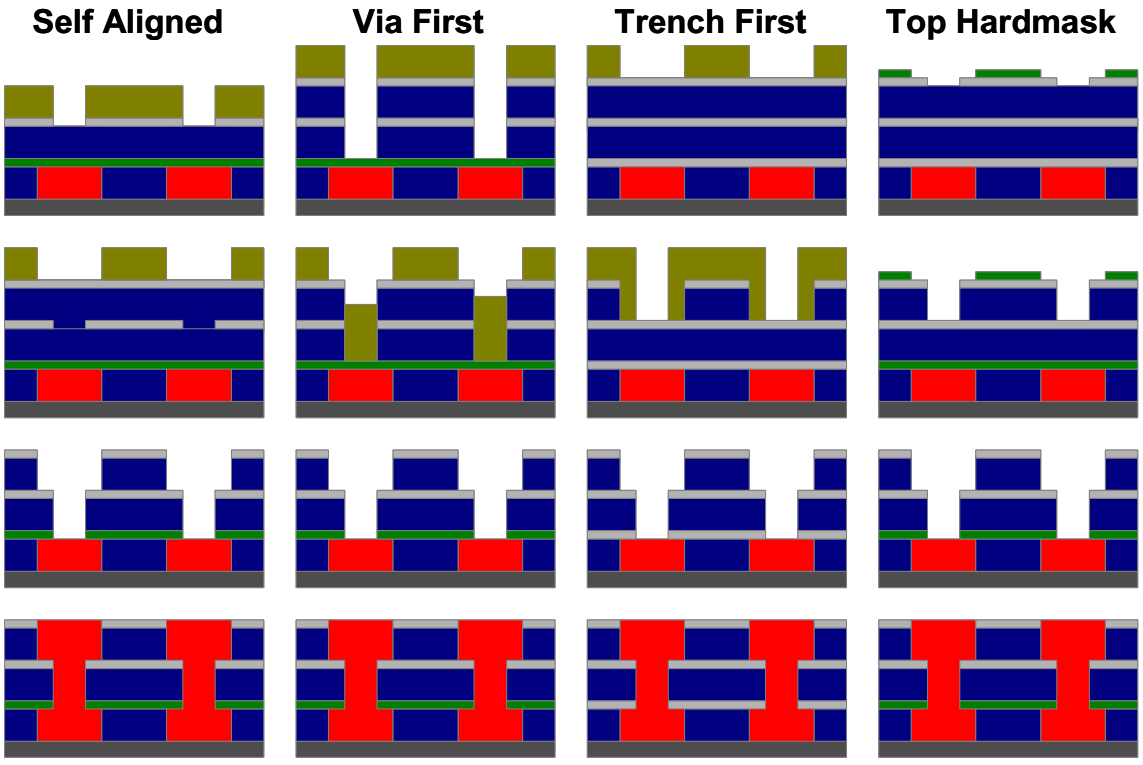


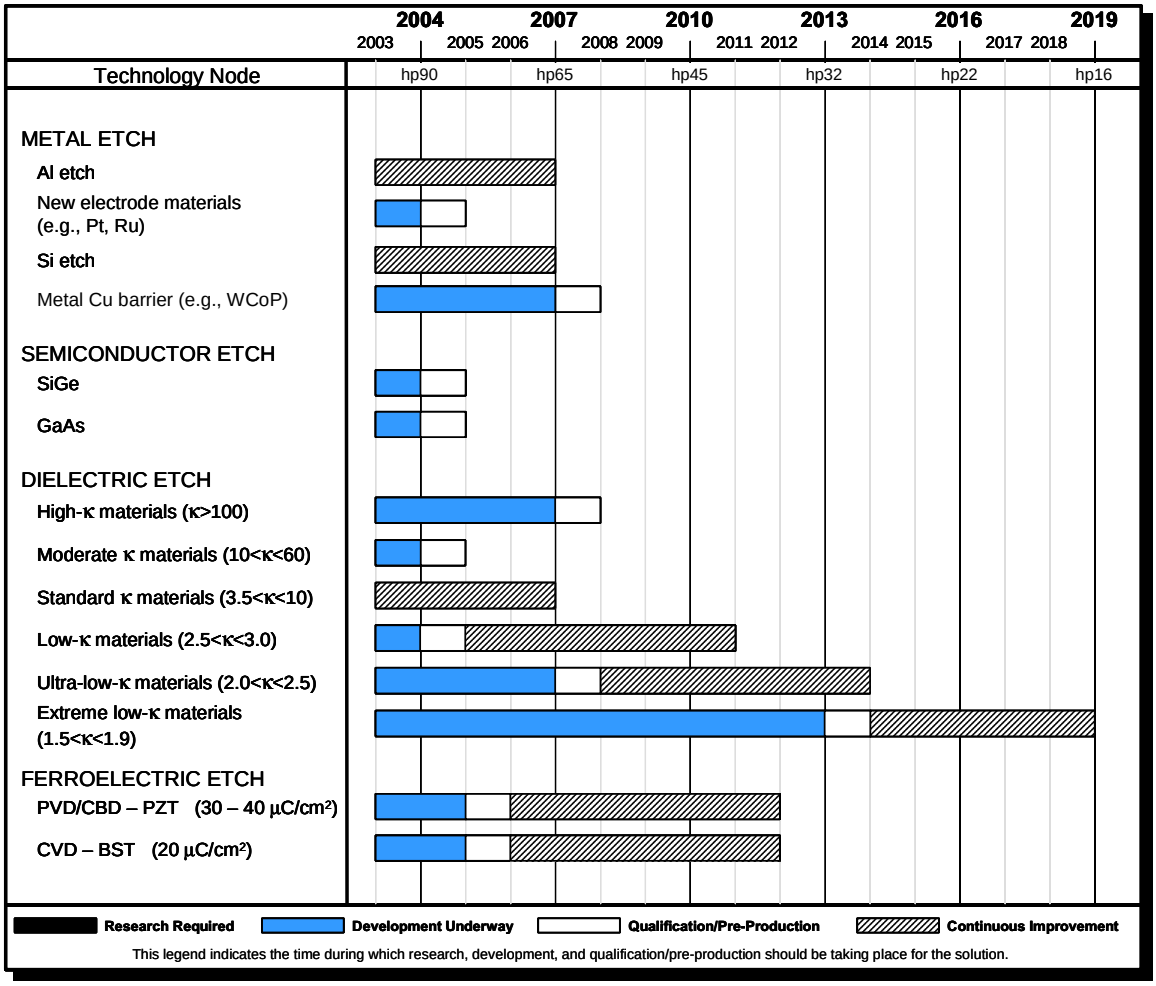
Figure 62 Etch Schemes for Dual Damascene

The etch cluster tool is expanding the number of modules or unit operations addressed within the cluster from a historical number of one to two and potentially three. The continued importance of clustering etch with *in situ* photoresist strip, clean, etch damage removal, etch damage repair and degas may potentially enlarge the scope of the etch tool to a cluster platform analogous to the current metal PVD cluster (degas, sputter etch, barrier 1, barrier 2, seed, seed geometry optimization).

Photoresist strip technology for metal etch will be a continuation of existing technology where emphasis will remain on total removal of all exposed organic material and the passivation of exposed metal. With respect to dielectric etch, if the entire ILD structure is composed of dense inorganic materials, classic ashing technology will continue with evolutionary advancements. Organic ILD material integration will challenge the need for high selectivities between PR / etch residue and the exposed organic ILD material. The greatest challenge will continue to be photoresist strip technology development for hybrid inorganic/organic ILD materials.

As the combination of exposed materials continues to expand to include, simultaneously, metals, inorganics, organics, and hybrid inorganic/organic layers, clean technology will evolve from a single wet clean process step to a sequence approach. This could potentially include a sequence for clean 1, protect 1, clean 2, de-protect, dielectric fix, surface treatment for barrier deposition process.

Through wafer via etch has already been demonstrated and in some cases is in limited production. In general it can be accomplished with RIE and/or bias-able parallel plate reactors. A new etch tool technology is not required. Relatively large amounts of material per wafer must be removed, so higher molecular weight inert gases are being investigated as a means to increase the efficiency of the etch. Again since so much material is being removed an increased burden of reactor clean time may arise affecting tool availability. Once the etch chemistry and process issues are solved, more effective means of reducing reactor downtime may need to be investigated.



WCoP—tungsten cobalt phosphide CBD—chemical bath deposition

Figure 63 Etch Potential Solutions

INTERCONNECT SURFACE PREPARATION

Interconnect structures based on copper and ultra-low-κ materials create unique surface conditioning challenges that were not encountered in previous technology nodes. Additionally, high aspect ratio structures for contacts and capacitors

increase the cleaning and surface conditioning challenges. Interconnect Surface Preparation includes post-etch photoresist stripping, post-strip residue removal, post-CMP cleaning for dielectrics and metals, pre-deposition cleaning for dielectrics and metals and post-deposition cleaning for dielectrics and metals. The main focus in these tables is dual-Damascene processing involving copper metal and low dielectric constant insulators. Interconnect necessarily involves several other metallic films as barriers and seed layers as well as silicon oxide and silicon nitride dielectric films as etch stops and hard masks.

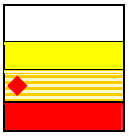
Wet cleaning, plasma cleaning, and other dry cleaning methods, such as supercritical fluids and cryogenic aerosols are all considered conditioning area. No one technique or technology has solved all the technical challenges for surface conditioning. For example, plasma stripping is cost effective for removing photoresist and residue, but is unable to remove metallic contamination. Wet cleaning is effective for removing metallic contamination but drying of high aspect ratio features has proven challenging.

Although surface conditioning is generally considered as a separate, stand-alone process, it has been incorporated into other process tools where a technical advantage is achieved, such as CMP. The combination of various surface-conditioning methods has proven successful for cleaning the wafer surface. For example, a typical post-etch cleaning sequence for the trench step of dual Damascene and then the subsequent barrier and copper PVD step includes an *in situ* post-etch photoresist strip and clean, a wet post-strip and clean, a wet pre-deposition clean, and finally an *in situ* pre-deposition sputter clean. Post-etch stripping and residue removal can now be performed *in situ* on the dual-Damascene dielectric etching tools.

Both logic and DRAM devices have cleaning challenges. As DRAM manufacturing migrates to copper interconnect, the same surface conditioning issues that logic faces need to be addressed. Additionally, high aspect ratio features such as contacts and cylindrical capacitors are difficult to clean and to dry. The front surface, back surface, and edge of the wafer must be effectively cleaned of particles, metallic and organic contamination. The surface must not be roughened and the materials must not be affected.

Table 83a Interconnect Surface Preparation Technology Requirements—Near-term*

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*D ½*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*M*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*M*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particles								
Killer defect density, D_pR_p (#/cm^2) [A]	**0.0172**	**0.0217**	**0.0283**	**0.0185**	**0.0233**	**0.0158**	**0.0199**	*D ½*
Critical particle diameter, d_c (nm) [B]	**50**	**45**	**40**	**35**	**32.5**	**27.5**	**25**	*D ½*
Critical particle density, D_{pw} (#/wafer) [C]	**59**	**75**	**97**	**64**	**80**	**54**	**68**	*D ½*
Back surface particles								
Back surface critical particle diameter (nm) [D]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Back surface critical particle density (#/wafer) [E]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Edge bevel particles								
Edge bevel critical particle diameter (nm) [F]	**200**	**180**	**160**	**140**	**130**	**114**	**100**	*D ½, M*
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Metallic Contamination								
Critical front surface metals (10^9 atoms/cm^2) (H)	**50**	**50**	**10**	**10**	**10**	**10**	**10**	*M*
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**1000**	**1000**	**1000**	**1000**	**500**	**500**	**500**	*M*
Mobile ions (10^{10} atoms/cm^2) [J]	**5**	**5**	**5**	**5**	**2.5**	**2.5**	**2.5**	*D ½*
Organic contamination (10^{13} C at/cm^2) [K]	**1.8**	**1.6**	**1.4**	**1.3**	**1.2**	**1.0**	**0.9**	*M*
Cleaning Effects on Dielectric Material								
Maximum dielectric constant increase due to Strip + Clean [L]	**4.00%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*
Maximum dielectric constant increase due to rework [L]	**4.00%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 83a and 83b:

[A] Killer defect density is calculated from the formula for 99% yield, $Y=0.99=\exp[-D_pR_pA_{eff}]$. A_{eff} is the effective chip area, D_p is the defect density, and R_p is a defect kill factor indicating the probability that a given defect will kill the device. The product DpRp is the density of device-killing defects on the wafer. R_p is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, R_p was assumed to be 0.2 for any particle > the critical particle size, d_c. A_{eff} is assumed to be the same as for Front End Surface Preparation. For DRAM, $A_{eff}=2.5F^2T+(1-aF^2T/A_{chip})\times 0.6A_{chip}$. where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and A_{chip} is the DRAM chip size. For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length. Because A_{eff} can increase or decrease with each successive technology node, DpRp does not always decrease over time.

[B] Critical particle diameter, d_c, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.

[C] An example is provided which assumes that the kill factor, R_p, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is

calculated using [Rp×3.14159× (wafer radius-edge exclusion)^2]. To convert from particles/wafer at the critical particle size to particles/wafer at an alterative size, a suggested conversion formula is: $D_{alternate}=D_{critical}\times(d_{critical}/ d_{alternate})^2$.

[D] and [E] Metrics for critical back surface particle size and back surface particle count are not being listed in 2003. While it is recognized that back surface particles are important to control and are assessed during equipment qualification, there is no clear empirical or theoretical model which links back surface particles to device yield. In the past, arguments have been made that back surface particles affect device yield mainly at the lithographic steps by causing the front surface of the wafer to move out of the focal plane leading to critical dimension variations. However, it is not clear how the limited back surface contact achievable with pin chucks interacts with back surface particle density to cause front surface flatness variations. In addition, it is also not clear how lithographic depth-of-focus (DOF) will change from year to year as this is not specified in the lithography roadmap. In general, it is felt that a good rule is to control back surface particles at a critical diameter equal to one-half of the DOF for critical lithographic steps. In 2003, DOF is about 0.4 micron, so the critical back surface particle diameter is generally considered to be 0.2 micron. It is not possible to measure absolute levels of back surface particles on in-process wafers due to large variations in back surface finish and films. A generally accepted practice is to process wafers with the polished front surface down in order to assess back surface particle adders for a particular process or operation. Current best practice indicates that back surface particle adders for any particular process step in 2003 should be less than 400 at 0.2 micron.

[F] and [G] Edge bevel critical particle size is taken as 2×DRAM ½ pitch. The size was determined to be particles that could be shed and then distributed onto the wafer surface causing detrimental yield reduction. Few references exist correlating edge defects with yield, however, minimization of the number of particles and density is important. The levels are still under evaluation, however, and no values are presented here, although current practices indicate edge bevel particle adders for any interconnect process step, in particular CMP, should be less than 4 defects per quadrant of the wafer. Again, this value should be treated as guidance, not a specification.

[H] Front surface metallic contamination levels are based on degradation of yield from metallic diffusion into the transistor or leakage of the device from metal migration. Data shows that Cu levels <1E13 can cause interconnect leakage and <1E10 can cause transistor degradation. The ability of the Cu to diffuse into the dielectric and then through the silicon to the transistors is questionable as many references site Cu cannot diffuse though thick silicon, nevertheless, the lower the Cu contamination the better. The levels are still under evaluations, however, and the values presented here should be treated as guidance, not a specification.

[I] Back surface Cu contamination level are based on degradation of electrical parameters of the transistor caused by Cu diffusion through the silicon. Many studies have been undertaken that evaluates the effects of backside Cu contamination on the transistors. The most profound affect is TDDB due to electric field drift. Oxygen on the back surface prevents the diffusion into the silicon. However, once in the silicon the Cu will diffuse and precipitate, dependent on thermal treatments. Various references quote a concentration as high as 1E15 and other quote as low as 1E11 as degrading device performance, dependent on test device structures and film thicknesses. Again, the levels are still under evaluation and the values presented here should be treated as guidance, not a specification.[1]

[J] Mobile ions for interconnect is less stringent than the front end line metrics. Although the mobile ions can lead to the same electrical degradation and do the same damage from migration though the dielectric, the oxide does getter some of the sodium. For backside contamination levels, use the front end values. For interconnect, the cause shown here are guidance as to allowable levels, approximately twice the value of the front end metrics.

[K] Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean. Leaving this film may result in undesirable delamination of subsequently deposited layers. Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, D_c at the 180 nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm^2). D_c for subsequent nodes was scaled linearly with the ratio of CD to 180 nm.
D_c = (CD/180)(7.3E+13).

[L] Stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant.

[M] Stripping and cleaning processes generally involve some removal of the insulator. In particular the carbon can be leaked from the CDO films, leaving a thin layer of SiO_x. This must be minimized in order to maintain critical dimensions. These values are guidance for allowable degradation of the dielectric constant.

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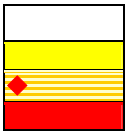
1 A. A. Isrtatov and E. R. Weber, J. Electrochem. Soc. 149(1) G21(2002).

Table 83b Interconnect Surface Preparation Technology Requirements—Long-term*

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*Driver*
Technology Node	*hp45*		*hp32*		*hp22*		
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	*D ½*
MPU / ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	*M*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*	*M*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*	*M*
Wafer diameter (mm)	**300**	**300**	**300**	**450**	**450**	**450**	*D ½, M*
Wafer edge exclusion (mm)	**2**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particles							
Killer defect density, D_pR_p (#/cm^2) [A]	**0.0250**	**0.0199**	**0.0250**	**0.0199**	**0.0136**	**0.0215**	*D ½*
Critical particle diameter, d_c (nm) [B]	**22.5**	**17.5**	**16**	**12.5**	**11**	**9**	*D ½*
Critical particle density, D_{pw} (#/wafer) [C]	**86**	**155**	**195**	**155**	**106**	**168**	*D ½*
Back surface particles							
Back surface critical particle diameter (nm) [D]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Back surface critical particle density (#/wafer) [E]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*D ½, M*
Edge bevel particles							
Edge bevel critical particle diameter (nm) [F]	**90**	**70**	**64**	**50**	**44**	**36**	*D ½, M*
Particles (cm^{-2}) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Particles (#/wafer) (G)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	*M*
Metallic Contamination							
Critical front surface metals (10^9 atoms/cm^2) (H)	**10**	**10**	**10**	**10**	**10**	**10**	*M*
Critical back surface metals (Cu) (10^9 atoms/cm^2) (I)	**250**	**250**	**100**	**100**	**100**	**100**	*M*
Mobile ions (10^{10} atoms/cm^2) [J]	**2.5**	**2.5**	**2.4**	**2.4**	**2.3**	**2.3**	*D ½*
Organic contamination (10^{13} C at/cm^2) [K]	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	*M*
Cleaning Effects on Dielectric Material							
Maximum dielectric constant increase due to Strip + Clean [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**0.00%**	**0.00%**	*M*
Maximum dielectric constant increase due to rework [L]	**2.00%**	**2.00%**	**2.00%**	**2.00%**	**0.00%**	**0.00%**	*M*
Maximum effect on dielectric critical dimension due to Strip + Clean [M]	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	**2.50%**	*M*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Challenges and potential solutions for interconnect surface preparation are primarily based on copper and low-κ integration schemes. The surface conditioning challenges for 90 and 65 nm are: cleaning and drying copper and sensitive low-κ dielectric films without damaging the surface or leaving residue. The high aspect ratio features, for example contacts, vias, stacked capacitors, and other storage devices, must be effectively cleaned and the water removed from the deep features. Moisture must not be incorporated into the porous low-κ dielectric structure, the carbon must not be extracted, and the dielectric constant must not change. The stacked features must not have voiding at the interfaces. Copper films must be cleaned without corrosion, especially around the barrier-copper interface, and the final surface must assure electrical contact by being free of thick oxide layers. Copper from the edges and backside of the wafer must be cleaned to prevent undesirable migration of the copper to the transistor.

The 45 nm surface conditioning challenges are extensions of the issues faced at 65 nm. Porous, carbon-containing ultra low-κ dielectrics integration may prove especially difficult. Surface preparation and cleaning techniques being looked at for this node extend beyond wet and plasma cleaning. Supercritical fluids, cryogenic aerosols, and laser cleaning are some of the new technologies being investigated. Advanced wet and plasma techniques are still on the roadmap, as improvements to these techniques will extend the use of these processes.

Wet cleaning will continue to be the method of choice for post-CMP, post-strip, and pre-deposition cleaning for the 90 and 65 nm nodes. Cleaning of copper and low-κ dielectric materials can be accomplished by wet methods. Dilute acid-based formulations with the additions of fluorine-based chemicals, surfactants, chelating agents, and/or corrosion-inhibiting agents will be used for cleaning at the 90 and 65 nm nodes and are extendible to 45 nm. Other advanced wet cleaning techniques, such as the use of dilute solutions of ozone, or other unique chemistries are still in the research stage for the 45 nm node and beyond.

Carbon-containing low-κ dielectric films present the problem of a hydrophobic surface, which is difficult to rinse and dry without creating watermarks or leaving undesirable surfactant residue. This challenge might be addressed with Front End surface preparation techniques such as surface tension drying or may drive the introduction of new processes such as super critical CO_2 or the introduction of new chemicals that can replace isopropyl alcohol (IPA). In addition, shrinking critical dimensions are creating more fragile structures and cleaning processes will be required which do not damage these structures.

Particle removal is becoming more important as geometries continue to shrink. Backside, edge, and front side particle removal must be accomplished to successfully clean a wafer. New methods being investigated include the extension of megasonics, brush, and other physical methods that minimize wafer damage. Edge and backside particles are known to cause yield degradation, however, quantification is difficult. New tools are being developed that can measure the particles on the edge and backside, allowing correlation to yield, that is not currently available.

Cleaning processes and chemical formulations will address environmental, health, and safety issues by using less concentrated chemistries to clean, less hazardous chemicals, and more environmentally friendly chemicals. Fluorine-based chemicals and chelating agents in particular have disposal issues. Reducing the use of water is also a goal.

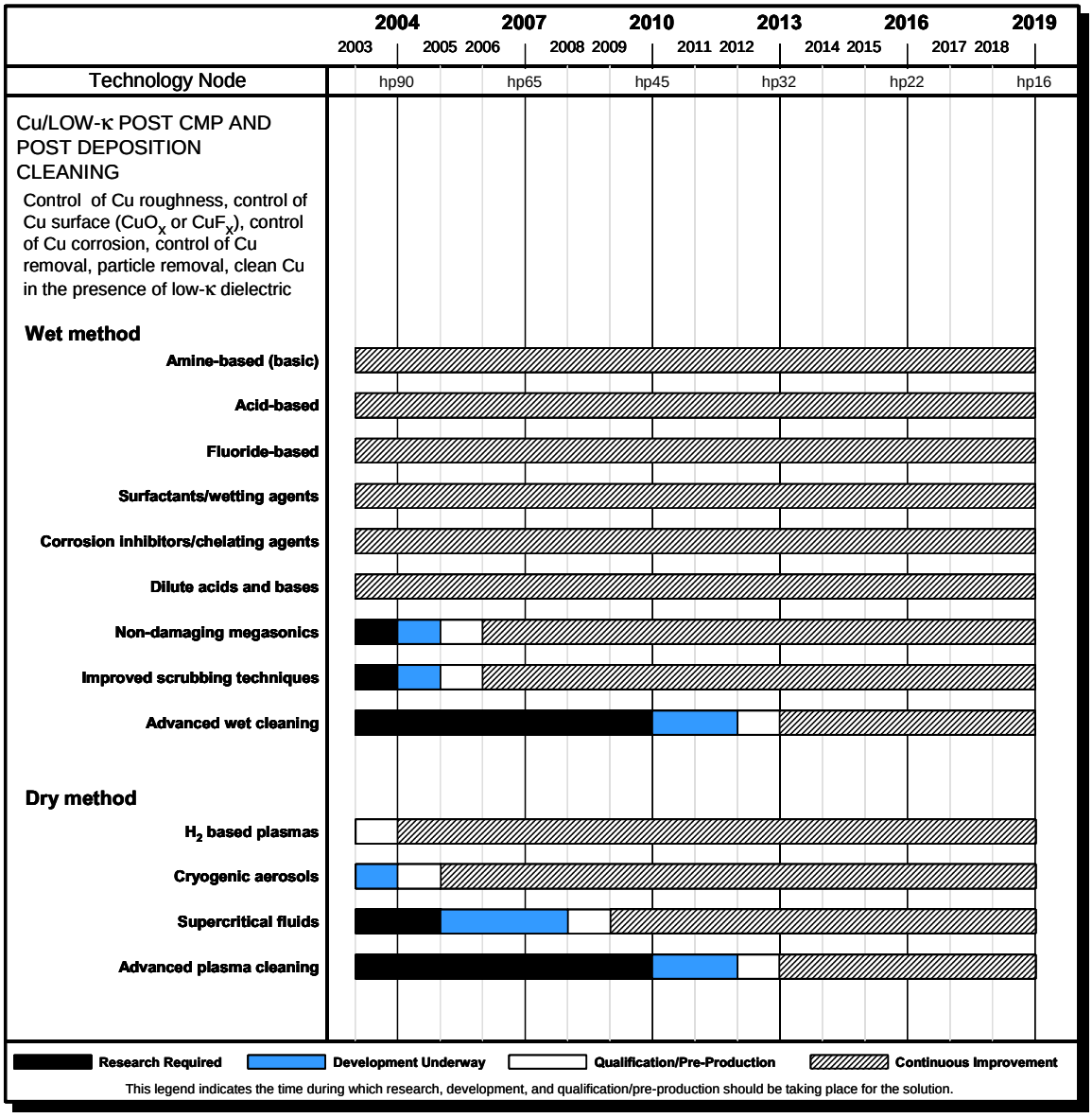
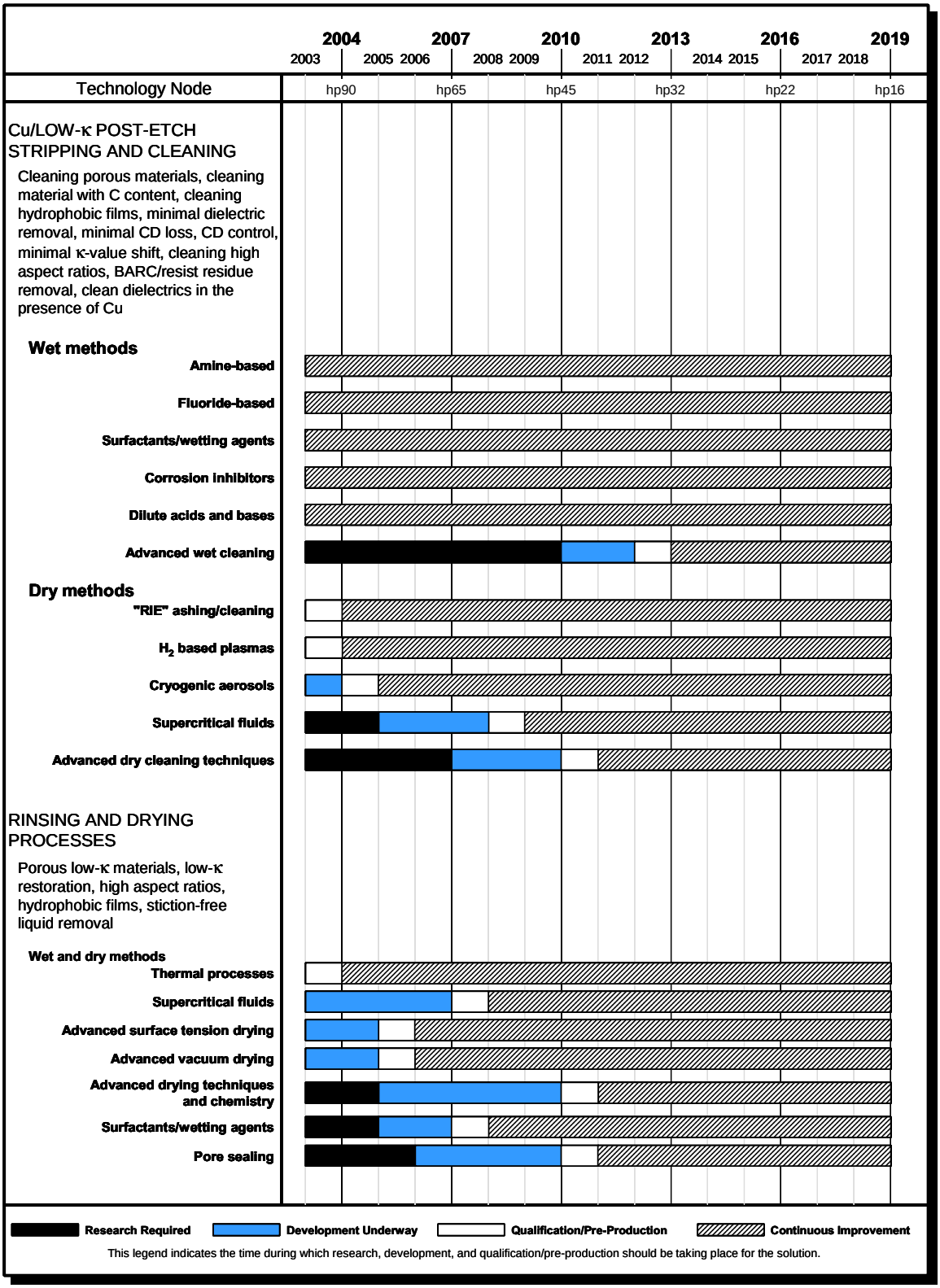


Figure 64 Interconnect Surface Preparation Potential Solutions



BARC—bottom anti-reflective coating

Figure 64 Interconnect Surface Preparation Potential Solutions (continued)

PASSIVE DEVICES

INTRODUCTION

The inclusion of precision on-chip passive devices is a new challenge for current and future interconnect architectures. This request for high quality capacitors, inductors and resistors is mainly driven by advanced mixed-signal, high frequency (RF) and system-on-a-chip (SoC) applications. Reduction and control of substrate coupling noise and other parasitics for mixed signal and RF CMOS applications is one of the most important tasks. From an application point of view the most important requirements for passives are listed in Tables 53a and 53b of the RF and Analog/Mixed-signal Technologies for Wireless Communications section of the Process Integration, Devices, and Structures (PIDS) chapter. In the past the traditional way to realize passive circuit elements (e.g., capacitors, resistors) on ICs was integration during front end processing. In this case doped monocrystalline Si substrate, polycrystalline Si and Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during front end processing suffer increased performance degradation especially when used at high RF frequencies. Therefore there is an increasing demand for low loss, low parasitics, but high quality passive devices in the interconnect levels.

For interconnect integration the key challenge is to achieve this goal in a modular and cost effective way, without sacrificing the overall interconnect performance and reliability. Currently the favored approach is the introduction of optional levels and new materials to accomplish the necessary functions and attributes.

MIM CAPACITORS

High quality metal-insulator-metal (MIM) capacitors are seeing increased use in CMOS, BICMOS, and bipolar chips. Typical applications are filter and analog capacitors (e.g., in A/D or D/A converters), RF coupling and RF bypass capacitors in RF oscillators, resonator circuits and matching networks. Key attributes of MIM capacitors are high linearity over broad voltage ranges (low voltage coefficients), low series resistance, good matching properties, small temperature coefficient of capacitance, low leakage currents, high breakdown voltage and sufficient dielectric reliability.

The economic demand for small chip area consumption leads directly to the request for higher MIM charge storage densities. Above a capacitance density of 1.5–2 $fF/\mu m^2$ a further thinning of the traditionally used Si-oxide or nitride dielectrics is no longer useful because of increased leakage currents and reduced dielectric reliability. Therefore new high-κ dielectric materials need to come into play.

As always the introduction of new materials leads to new challenges in material processing and integration. High quality films with excellent thickness uniformity, low defect densities and high dielectric constants need to be deposited below 450°C in order to be compatible with the overall interconnect architecture. In order to reduce parasitic substrate coupling and allow for high quality factors of the MIM capacitors the integration into the upper metallization levels is preferred.

Low resistive capacitor electrodes and perfectly engineered electrode-dielectric interfaces are necessary to achieve high MIM quality factors and reliability. Some promising integrations of high-κ materials in MIM capacitors have been demonstrated in the literature (see appendix: Optional levels – passive devices). However, improvements are still necessary in order to come to a cost effective and manufacturable solution with a minimum of additional process steps.

INDUCTORS

High quality on-chip inductors are critical components in analog/mixed signal and high frequency RF applications. Currently they are widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers and low noise amplifiers. Key attributes are high quality factors, Q, at high inductance, high self-resonance frequency, low Ohmic losses, low eddy currents and low capacitive substrate losses.

Today, spiral inductors in the upper thick Al- or Cu-metallization levels are most widely used in order to fabricate low resistive coils with sufficient spacing from the Si-substrate to achieve optimized quality factors. These simple spiral inductors can be fabricated relatively easily using standard interconnect processes. But they may not in every case be good enough to fulfill all future RF requirements. Therefore, some more advanced constructions and approaches are being pursued.

Examples such as shunted coils, realized in several metallization levels, the use of metallic or even magnetic ground planes, suspended spiral inductors in air-gaps, post passivation add-on modules with coils in fat redistribution metal layers (several µm metal thickness) or solenoidal inductors with and without ferro-magnetic core fillings have been successfully demonstrated (see appendix: Optional levels – passive devices). However, not all of these alternative fabrication schemes are suitable for manufacturing, because of integration and process complexity issues. These approaches are an expression of the constant struggle for improved performance with higher inductance at higher frequencies or improvements in quality factor by reducing the Ohmic losses in the coil and/or the parasitic substrate. Another possibility for reducing the substrate losses is the use of high Ohmic Si substrates, however, this last approach is not always compatible with the respective device and product requirements.

RESISTORS

Precision thin film resistors are widely used in analog and mixed signal circuits and specific SoC applications. Key attributes are precise resistance control, excellent matching properties, high voltage linearity, low temperature coefficients (TCR), low 1/f noise and low parasitics resulting in high Q values. Today the most widely used Si-substrate-, poly-Si- or silicide- resistors fabricated during front end processing suffer mainly from poor 1/f noise performance and substrate losses.

Thin film resistors in the metallization levels can significantly improve the 1/f noise performance and other substrate losses. Key challenges for resistors in the interconnect are finding materials with moderate and tunable sheet resistance compatible with the standard interconnect materials and integration schemes, excellent thickness control and good etch selectivity to dielectrics with a modular integration scheme. Especially for Cu-metallization schemes TaN has been found to be a promising candidate. However, other materials may be coming up in the near future (see appendix: Optional levels – passive devices).

RELIABILITY

INTRODUCTION

The rapid changes in interconnect materials and structures that has occurred in the last technology generation have resulted in significant new challenges to the interconnect reliability community. The anticipated move to radical forms of interconnect in future generations will provide even more challenges and require new understanding of interconnect reliability. This section presents a short description of the reliability concerns that have been identified with Cu/low κ metallization, and comments on the need to place reliability as a major concern for future technology directions.

CU/LOW-κ ISSUES

The semiconductor industry move to copper metallization promises significant improvements in interconnect current carrying capacity and high temperature operation, but has resulted in numerous new material integration and reliability challenges. The problems are further exacerbated by continued increases in the interconnect density, the number of layers, and power consumption. Aluminum metallization reliability was established over several years, and was found to be able to be characterized by a few parameters that could be used as design constraints, such as Jmax and "critical length." No such characterization has yet been established for copper metallization. Parameters that establish a relationship between fundamental material properties and design requirements are critically needed for the continued expansion of the use of copper metallization in ICs.

INTERFACES

Copper, unlike aluminum, has no self-passivation layer. Therefore, surface diffusion is expected to dominate electromigration behavior, and material interfaces will play a key role in determining overall reliability. Since copper readily diffuses into silicon and most dielectrics, it must be encapsulated with metallic (such as Ta, TaN) or dielectric (such as SiN, SiC) diffusion barriers to prevent electrical leakage between metal wires and degradation of transistor performance. Cu diffusion is also greatly enhanced by electric fields imposed between adjacent wires during device operation, and absolute barrier integrity is crucial to long-term device reliability. As barrier thickness scales with metal width to meet conductor effective resistivity goals, copper containment becomes increasing more problematic, and eventually new copper passivation techniques and/or diffusion-resistant dielectrics are needed to provide essentially "zero thickness" solutions.

The effects of surface scattering on Cu resistivity, basically an interface effect, have been shown in Cu lines as large as 90 nm. Even if these effects are reduced to acceptable levels by surface passivation treatments during device fabrication, they will still need to be proved stable for long-term reliability considerations.

RELIABILITY IMPLICATIONS OF CU/LOW-κ MATERIALS AND PROCESSES

Damascene structures may change the approach to photoresist stripping and subsequent cleaning for interconnect layers. The use of hard mask materials and oxygen-based chemistries for etching organic low-κ dielectrics enables *in situ* stripping of the photoresist during the trench, contact or via etch steps. Dry stripping alone may be insufficient to remove residues and particles from structures with high aspect ratios without attacking the low-κ dielectrics or copper and its barriers. The implementation of porous silicon oxide or similar low-κ materials may or may not allow the continued use of traditional oxygen-based stripping processes, but the detailed reliability implications of any combination of processes and materials used will need to be understood. All of these unit processes bring their own specific yield loss mechanisms as well as susceptibility to longer-term reliability problems.

The integration of new low-κ dielectrics needed for performance enhancement bring numerous reliability concerns that include thermally or mechanically-induced cracking or adhesion loss, poor mechanical strength, moisture absorption, time-dependent behavior, texture effects, and poor thermal conductivity. The typical thermal conductivity of low-κ dielectrics is less than one third that of oxide, leading to higher metal wire temperatures and enhanced electromigration. Bi-layer or embedded oxide/ low-κ dielectric schemes may be required to enhance the mechanical strength and heat dissipation of future low-κ dielectric systems.

The lessened mechanical strength of low-κ dielectrics and anticipated higher temperature operation of some of the copper interconnects will drive the need for novel packaging techniques and structures. These, combined with the move to higher packaging process temperatures needed to accommodate lead-free solders, will provide new reliability challenges for the research and development community to resolve. Expanding use of advanced technology in assembly, such as area-array bumps, need to be considered and integrated with circuit, material, and process selections in order to maintain product reliability in the future. This is especially important to encompass low-κ dielectrics and assembly-related process steps, such as under-bump fill, which may be performed on the wafer.

MODELING AND SIMULATION

Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- Wire length
- Current densities expected for the currents required by the circuit
- Calculated local operating temperature, which includes the effects of Joule heating in the circuit and elsewhere

These tools will need to become an integral part of the circuit designer's tool set to help predict product reliability before processing begins and to develop solutions that anticipate technology and thereby accelerate their introduction.

FUTURE RELIABILITY DIRECTIONS

The sections above discuss only reliability concerns that have been identified thus far for the Cu/low-κ system. Continuing research is needed to fully understand the multi-variable nature of copper and low-κ interconnect reliability and provide accurate models for designed-in reliability. It is expected that many of the problems that result in Cu reliability issues will be more severe as feature sizes scale, as surface area to volume ratio of the metallization increases, and as geometries scale to feature sizes where electron surface scattering effects become a significant contributor to resistivity. The fundamental reliability limits of copper/low-κ metallization must be identified to assess technology extendibility in these ranges, and to identify any unique failure modes that may arise.

It is expected that one or more alternate interconnect approaches, such as optical interconnects, package intermediated interconnects, 3D interconnects, or microwave interconnects, will begin to be used within the next five years. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

SYSTEMS AND PERFORMANCE ISSUES

INTERCONNECT PERFORMANCE

The adequacy of near-term interconnect technologies (copper wires and low-κ dielectrics) to continue meeting the performance requirements for ICs fabricated for succeeding technology nodes varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. Calculations show that using the existing roadmap values for technology generations from 180 nm down to 15 nm, the delay of scaled wires increases by approximately 10× while the delay of fixed length wires increases by approximately 2000×. If these wires are modified with repeating inverters, these delays reduce to approximately 3× for scaled wires and 40× for fixed length wires. In some designs these increases with repeaters can be handled by modifications such as modular architectures to reduce the need for fixed length lines. However, such significant modifications to circuit architecture suffer from the disadvantages of needing new design tools and not being generally applicable to all designs. While delay is a major factor for many digital applications, crosstalk and noise associated with decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits. These trends are a strong function of design strategy, and should be considered in that context.

In addition to the problems with scaled wires for clock and signaling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to the decreasing V_{dd}, causes an increased voltage drop between the power supply and the bias point for fixed length wires. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires. At the present time this need is being partially addressed by the introduction of ball-grid-array packaging technology that distributes power feeds across the area of the chip, eliminating much of the on-chip lateral power feeds through relatively high-resistance global wires. More novel solutions using other packaging intermediated power and ground solutions will be required for future scaled interconnect systems.

SYSTEM LEVEL INTEGRATION

System level integration encompasses the physical and functional assembly of a system's macro functions to achieve its desired operating characteristics. Assembly of individual functional components (such as bare chip or block functions on a single chip) into the system must encompass all the performance and reliability requirements imposed on the system. For interconnect, the requirements are currently met through the distinctly separate functions of on-chip interconnect, package, and board-level technologies.

It is now widely conceded that technology alone cannot solve the on-chip global interconnect problem with current design methodologies. Rather, the current view is that design, process technology, packaging, and board construction will all need to come together to provide an optimized integrated system level solution for interconnect requirements.

The current projection for evolution of interconnect is that in the short term interconnect delay problems in new ICs will be met by circuit design within the constraints of planar technology with special attention to minimizing the lengths of critical paths. This will be done in concert with a substantial push in Cu/low-κ technology, as well as more innovative packaging and board approaches, to minimize the changes needed in design architectures while still meeting the continued advances in performance projected by the ITRS.

In the intermediate term, Cu/low κ will be pushed to its limits, and new design architectures as well as chip-package co-design will be achieved with new CAD tools to significantly facilitate needed performance advances. Beyond these extrapolations of current practices, radically new design, packaging, and interconnect technology options will be needed.

Many changes are envisioned to meet the needs for advanced interconnect. Among the design options being considered are items such as non-synchronous clocking, interconnect-centric architectures and design tools, and interconnect-aware verification and analysis. The packaging community is expected to impact the global interconnect problem in the near term with optimized co-design of the chip and package interconnects. This approach will lead naturally to the total optimized system in a single package (SIP). The SIP approach can provide many unique capabilities for interconnect,

including transfer of high-speed clocks and signals to thick package leads to minimize RC delay and use of specialized chips for interconnect functions. Subsequently, innovations such as wafer-scale packaging and package intermediated intra- and inter-chip interconnects will be needed to assist in alleviating the interconnect problem.

Many new technology options are currently envisioned beyond the immediate Cu/low-κ and IC/package redesign. These may include microwave interconnects, package-mediated interconnects (such as multi-chip packages, active substrate packages, etc.), RF package coupled interconnects, 3D ICs, optical interconnects, and nanotubes. Other futuristic approaches such as self-assembled interconnects and quantum communications via spin are intriguing concepts, but will require major innovations to be useful in circuit applications.

Each of the higher system level approaches listed above has the potential to minimize the problems associated with global interconnect. Research and development in all of these areas is needed to ensure timely availability of these future options while accelerated efforts in design and packaging will deliver the solution.

NEW INTERCONNECT CONCEPTS

INTRODUCTION

The need for new interconnect concepts, *beyond the traditional metal/dielectric system*, was pointed out dramatically during the 1997 roadmap development. It was realized that the continued push to smaller geometries, higher frequencies, and larger chip sizes rapidly resulted in an incompatibility between interconnect needs and projected interconnect performance. Further analysis has shown that the problem is primarily with global interconnects (although the problems may extend to lower levels in some designs), and for this case the traditional metal/dielectric interconnect systems will not meet advanced roadmap requirements using even the most optimistic estimates of resistance and dielectric constants. This recognition has led to investigations into new interconnect concepts to continue IC technology along the Moore's law curve.

The totality of new concepts that have been identified as possible resolutions to global interconnect issues is extensive. These options range from expanded use of design changes that minimize the need for long interconnects, to much more speculative approaches using new physical principles such as electron spin and quantum entanglement. In between these extremes are approaches using geometry, such as 3D; new materials like nanotubes and molecular conductors; and use of other IC disciplines such as package-intermediated interconnects.

During the past few years several of the proposed possibilities have proceeded from the research stage to development, but as of this writing none of the technology options have been identified as the clear choice for future generations of global interconnect. Much work needs to be done to determine if these options are feasible, manufacturable, and provide any cost effective, extendable solution to interconnect or integrated circuit performance challenges. It is probable that unlike Al, W, or Cu and SiO_2 or low κ, no single one of these solutions will be used universally over nearly all of the IC product types.

A selection of some of the more promising technology directions being pursued to continue to meet the advancing roadmap requirements, and some of their critical issues, are described below. These options are listed on Conductor Potential Solutions, Figure 58, as Global Interconnect options.

PACKAGING INTERMEDIATED INTERCONNECTS

One option for reducing the global interconnect problem is to move some of the interconnects from the primary chip to thicker metallization and higher performance levels on the package, or on a supplementary chip designed to carry only interconnects. These signals would then be transferred back to the primary chip at an appropriate point. In some cases, a "sea of leads" approach might be used to provide major density increases in I/O to benefit not only global interconnect, but at the same time, power and ground connections. The basic components of most of the package intermediated approaches have been demonstrated at the laboratory level. Creative development is now needed to provide implementations of this approach that will circumvent the inherent cost and reliability limitations introduced by added elements and connections.

CRITICAL CHALLENGES

- Cost and reliability of additional interconnects between chip and package
- Cost of supplemental chip (if used)
- Design issues associated with division of interconnects between chip and package
- Probing and testing

3D INTERCONNECTS

3D interconnects comprise multiple levels of active devices stacked on top of one another to minimize the distance required for interconnects. The stacked layers may be separate chips that are connected through the package by conventional bond pads, may be separate chips bonded with innovative "through wafer" contacts, or multiple stacks of active devices in the interconnect layers on a single chip. The separate chip approach contacted through the package is used today, but does not provide the minimum interconnect lengths that could be available by through wafer contacts or 3D integration on a single chip. It also does not provide the advantage that integrated repeaters within the 3D layers would achieve to facilitate high-speed signal transmission. Today however, the main driver for 3D integration seems to be the product and system perspective and not so much the improvement of interconnect performance.

In this SoC (System-on-a-Chip) versus SiP (System-in-a-Package) debate, the 3D integration allows one to realize heterogeneous stacks of different ICs, such as combinations of digital CMOS with memory (DRAM, non-volatile, etc.), mixed signal, bipolar (RF) or compound semiconductors (III-V). The 3D approach takes many forms and opens many new and unique areas of research. Among these areas are critical alignment tolerances, material performance and compatibility issues, and heat management issues.

CRITICAL CHALLENGES

- Thermal management capability compatible with high heat load of 3D interconnect
- Capabilities for thinning and bonding wafers
- Capabilities for patterning, etching, aligning and filling dense, narrow inter-chip vias
- Where active devices are to be built on top of interconnects, a means to build "transistor" grade electronic materials on top of the interconnects at low temperature
- Models of manufacturing cost and yields for 3D integration that allow intelligent selection among the options for specific product applications

RF AND MICROWAVE INTERCONNECTS

A relatively radical alternative to the usual metal/dielectric interconnects is to use transmission of signals from one part of a chip to another via RF or microwaves. This option essentially takes the form of a LAN on a chip, with transmitters and receivers combining antennas and appropriate signal generation and signal detection circuitry. Transmission in this case has been proposed to be a "free-space transmission" through the package and IC structures. Another possibility is that the RF signal be capacitively coupled through a waveguide in the package lid. The transmission has been proposed as a sinusoidal signal or as a coded digital signal, depending on the specific system concept employed. Each option has its own particular advantages and disadvantages, as well as its own unique requirements. The basic concepts of this approach to global interconnects have been demonstrated.

CRITICAL CHALLENGES

- Complete characterization of total system concept for cost and performance comparison with alternative solutions
- Full design rules for the electrical and electromagnetic portions of RF and microwave interconnects

OPTICAL INTERCONNECTS

Optical interconnects are considered a possible option for replacing the conductor/dielectric system for global interconnects. The optical approach has many variants, the simplest perhaps having emitters off-chip and only free space waveguides and detectors in top layers on-chip. Progressively more complex options culminate in monolithic emitters, waveguides, and detectors. The optical interconnect option has many advantages, but also has several clear areas requiring significant research. The decisions on which signals to include in optical communications and which remain in conventional metal dielectric, and the choice of on-chip optical emitters, are significant. In the case of optical

interconnects, it is easy to assume that this solution will meet speed requirements because the signal travels at "the speed of light." However, to define the total interconnect system for this approach it is necessary to consider the delays associated with rise and fall times of optical emitters and detectors, the speed of light in the transmitting medium, losses in the optical waveguides (if used), the signal noise due to coupling between waveguides, and a myriad of other details.

CRITICAL CHALLENGES

- A high efficiency, high switching rate laser source, monolithically integratable into Si CMOS, (at low cost) needs to be developed
- A low power modulator, monolithically integratable into Si CMOS, (at low cost) to be used in conjunction with an off chip continuous laser
- Low power, high efficiency, small size optical detectors monolithically integratable into Si CMOS (at low cost)

GUIDED TERAHERTZ WAVE INTERCONNECTS

Guided terahertz waves are a hybrid of RF and optical signaling, using transmission of frequencies around 10^{12} Hz. These are propagated through microstripline waveguides possibly built with Cu/low κ or SiO_2. This approach is attractive because it provides the opportunity to significantly extend the bandwidth of interconnect systems without changing the material set. This technology may lend itself to smaller feature sizes than optical or RF and may be usable in "intermediate" interconnect layers.

CRITICAL CHALLENGES

- High efficiency terahertz sources capable of monolithic integration into Si CMOS (at low cost)
- Low power terahertz modulator that can be monolithically integrated into Si CMOS (at low cost)
- Low power, monolithically integratable into Si, CMOS (at low cost) terahertz detectors of small feature size need to be developed. (The "small" detectors that are currently available are largely bolometric, and do not afford the bandwidth promised by the terahertz carrier.)
- A study of microstripline scalability to determine such parameters as; impedance, losses, dispersion, mode stability, power handling capability, electrical reliability, "microstrip-to-microstrip crosstalk" and others needs to be performed with a resulting set of design rules

RADICAL SOLUTIONS

In addition to the aforementioned options for global interconnect solutions, there are several more radical options that may offer unique advantages. These radical alternatives include such areas as nanotube interconnects, spin coupling, and molecular interconnects. These options are in their early stages of development, and have a common critical need for a total system concept that demonstrates their utility in the interconnect function as well as a manufacturing methodology for their fabrication. Although many important features of radical solutions to the interconnect problem have been realized, there is still a critical need for additional creative approaches that will provide the defined roadmap capabilities while meeting the difficult challenges of cost and manufacturability.

The discussions above have described several *new concepts* for providing interconnect solutions compatible with the increasing requirements needed to continue the progression of IC technology. Although several independent approaches are described, it is expected that the solutions used will be different for different applications, and that the ultimate solutions may require a combination of several of the approaches described above. This realization makes it imperative that cross-functional research is emphasized to ensure that the best approaches using all of the possible techniques are fully evaluated.

Interconnect technology has been following an evolutionary path ever since it's inception by Robert Noyce in his 1959 patent. Even the difficult transitions to Cu/low-κ are relatively minor technology transitions in comparison to the disruptive technologies proposed above. There are many technology issues to be dealt with but before the industry will embrace a large investment to arrive at solutions, some strategic questions need to be addressed:

1. How does the approach fit in the solution of the overall interconnect problem?
2. How much of the problem does it solve? (for which products?)
3. When will the technology be ready for implementation?

4. How does the capability of this technology match needs at the projected time of implementation?
5. How extendable, or for how many generations will it provide benefit?
6. What other technologies will need to be developed to effectively implement the solution?
7. What changes in software, hardware, manufacturing, applications, or business will need to be in place to effectively implement the solution?
8. What technical problems need to be solved before implementation? and what is their current state?
9. What needs to be done/added to provide the implementation on time?
10. How will the technology be transferred into the mainstream?

CROSSCUT ISSUES

In response to the magnitude and difficulty of solving the global interconnect problem, the interconnect community has begun, not only a significant effort to push Cu/low κ to its limits, but also to explore radical alternatives that may require fundamental changes in design and packaging methodologies. At the same time, the design, packaging, and modeling and simulation communities have started significant efforts to alter their approaches to address the global interconnect problem. Possible solutions range from relatively minor modifications of existing technology, to radical alternatives to existing methodologies. In this case it is critical that the entries in the ITRS technology requirements tables comprehend needs generated by advances in all areas. It is also critical that the design, packaging, and modeling and simulation communities are appraised of common needs envisioned by the interconnect community. The following paragraphs discuss some of these needs.

DESIGN, MODELING AND SIMULATION

Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Further, the models are largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and chose the correct interconnect routing, (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to effectively utilize both the near term and far term proposed interconnect systems. The upcoming new interconnect challenges specifically;

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1 cm). This capability will also be needed for systems using RF or terahertz wave interconnections
2. A means to optimally place function blocks will be needed for the “3D” integrated circuits not only on an individual die but also now on a stack of die.
3. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
4. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurrences of critical “hot spots” within the die. Predictive thermal models, that can accommodate thermal impacts of RF standing waves, the multiple heat generating layers embedded in the 3D IC, and heat generated by, as well as thermal performance of, optical devices and quantum well devices will be needed

Modeling and Simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to the prediction of resistivity increase of further shrinking copper interconnects (due to grain structures) and the physical structure and properties of new low-κ dielectrics and other more exotic interconnect materials.

In all of these cases Modeling and Simulation should provide predictions accurate enough to reduce as much as possible the need for and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for Modeling and Simulation is ever increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical and electrical modeling (which in this issue of the roadmap has newly become one of the short-term challenges for Modeling and Simulation).

Specific interconnect needs for modeling and simulation include: performance prediction (including high frequency effects and reliability) for complex (e.g., 3-D) structures fabricated with real non-idealized processes (including etching, PVD, CMP), with hierarchical capability to choose the appropriate tradeoff between speed and accuracy for the application in question; tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; and materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier and dielectric). Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, and copper thinning and dishing in CMP. See the *Modeling and Simulation* chapter.

ASSEMBLY AND PACKAGING

The most acute near-term challenge is the package to die interface of ICs using the increasingly more fragile low-κ materials. These materials are more than an order of magnitude weaker than SiO_2 and as the dielectric constant is lowered their strength will diminish further. Means to package the materials with low-to-zero applied stress, both during fabrication and use in the field need to be explored. Alternatively, a means to reinforce the interconnect structure, using the metal layers or some form of "supported passivation" (but without increasing capacitive effects) need to be developed.

An industry wide approach for the fabrication of 3D ICs has not been determined. A few possible impacts are:

- Development of means to pick, accurately place die on top of other die, then subsequently electrically and mechanically join them
- Development of means to electrically connect to the top, bottom and even the sides of the die stacks
- Development of packages that provide means to extract heat from the die stacks, either passively or by active "fluid" cooling

The departure technologies, optical, RF will require new package types that will accommodate free space or guided wave communication from the die through the package to the outside world.

METROLOGY

Although copper Damascene process technology is now well established, research and development continues as the first low-κ materials move into production. It is useful to note that although the goal of metrology is measurement of patterned wafers, most available methods are used on blanket wafers or test structures. Measurement of voids in copper continues to be a critical challenge. Determination of pore size distribution in low κ has been demonstrated. The issue is finding voids and killer pores that result in yield and reliability loss. Automated control of copper plating baths has been introduced. Several of the key Metrology Technology Challenges are due to Interconnect Technology, and they are listed below. The Interconnect Metrology section of the Metrology Roadmap describes the critical metrology challenges in more detail.

- Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are void detection in copper lines and killer pore detection in patterned low κ
- Measurement of complex material stacks and interfacial properties including physical and electrical properties
- Determination of manufacturing Metrology when device and interconnect technology remain undefined

YIELD ENHANCEMENT

Driven by metal line size reduction, interconnect will continue to battle it's historical yield challenges, metal integrity and reliability. The shift to damascene gave significant improvement in line shorts performance over etched aluminum, but the incidence of via opens increased dramatically. This problem is the essential "governor" of metal shrink capability. Cu offers higher EM reliability than Al but the advantage has now been consumed with higher current densities in the smaller lines. A fast means to detect these opens without resorting to electrical probing would be highly desirable.

New metrics have been introduced into the roadmap tables for backside particles. The primary source for these today is from CMP and as the number of metal layers increase so will the number of CMP operations. A new means of removing the particles beyond the brush scrub, sonic scrub, and surfactant cleans used today should be developed.

Identifying and separating known good die will be key to the successful execution of 3D IC. Some technologies stack whole wafers, wherein the yield losses multiply. Other technologies stack dies and unless the die are pre-tested and functionally known to be good, yield losses will again multiply.

ENVIRONMENT, SAFETY, AND HEALTH

Interconnect technologies carry unique environmental, safety, and health (ESH) challenges. The performance-driven need for new materials (low-κ dielectrics, high-κ dielectrics, copper conductors and barriers, and others) and processes (electrochemical deposition, CVD metal/dielectric deposition, Cu/barrier CMP, low κ/high κ etch/clean, and others) brings numerous ESH concerns, especially considering the rapid pace of insertion. Continuous improvement is needed in methods for treating and recycling CMP slurries and copper electrochemical deposition baths. Both wet and dry processes will continue and require appropriate abatement; the introduction of new metal and dielectric materials adds to these ESH challenges. Closed-loop control and replenishment are potential solutions for wet processes. The new materials, precursors, and processes that will be required for future low-κ dielectrics and CVD conductor/barrier depositions must also be carefully screened for ESH issues during the early phase of development. Reaction product emissions, health and safety properties, materials compatibility with equipment and other chemical components, flammability and reactivity must be predetermined to ameliorate ESH impact. The industry must also strive to reduce chemical emissions and waste (copper plating solutions, CMP slurries, acids/solvents, PFCs, water use) through process optimization, use of alternative chemistries, recycling, and/or abatement. (Refer to the *Environment, Safety, and Health chapter* for comprehensive information and to a new chemical screening tool (Chemical Restrictions Table).)

The insertion of low–κ materials is having only a minor impact on ESH. The materials themselves are relatively benign. The CVD precursors are in many respects much less dangerous than the SiH_4 predecessors. Solvent systems for spin-on low κ are being designed which are are environmentally acceptable when handled using normal manufacturing procedures. The etch chemistries for forming the damascene relief structures also use gases that the industry has experience in handling and abating.

The transition to Cu metalization has eliminated the need for the halogenated etch chemistries used in Al etch, but has created a waste stream of aqueous and suspended copper metal and ions. These waste streams are the result of the electroplating chemicals used for the deposition and "residues" that result from the following Cu CMP process. The Cu in these waste streams can be highly dilute; either at the source (*e.g.*, plating, CMP rinse water), or as a result of combining them with other "acid waste" at the facility level. In the case of CMP, the slurry abrasive particles are a large proportion of the waste stream with relatively small amounts of Cu metal and ion included. Solutions do exist to remove the copper from these waste streams such as electrophoresis, electrowinning, or ion exchange resins. However the industry must determine if these remedies will be applied at point of use (tool or bay) or at the facility level.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

Cu and low-κ interconnects will probably represent the final "conventional" interconnect technology. There are no metals with significantly lower resistivity than Cu. The industry will push the dielectric constant as close to the theoretical ideal of 1 as possible. Therefore any new device that will require a high speed-power-performance interconnect will use the Cu and low-κ system.

Modern multilevel interconnect systems are essentially complex mechanical structures; civil engineering executed at the micro-to-nano scale. The tools that are used to design these structures; the processes to fabricate them, and the methods used to characterize them will be extendable to other micro-to-nano structures.

CONCLUSION

Managing the rapid rate of materials introduction and the concomitant complexity represents the overall interconnect challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. The delay associated with global wiring and the management of crosstalk and noise must be addressed with increased development activity. System-on-a-chip may alter the picture or technology timing because chip functionality can be traded for scaled density in the marketplace. Ultimately, interconnect innovation with optical, RF, or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.