INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

LITHOGRAPHY

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LITHOGRAPHY

SCOPE

In 2003 and beyond, lithographers are confronted with two sets of challenges. The first is a consequence of the difficulties inherent in extending optical methods of patterning to physical limits, while the second follows from the need to develop entirely new, post-optical lithographic technologies capable of being implemented into manufacturing. Not only is it necessary to invent technical solutions to very challenging problems, it is critical that die costs not be increased because of the new methods. Each new generation of lithographic technology requires advances in all of the key elements of the following lithography infrastructure:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask making equipment, and materials
- Metrology equipment for critical dimension (CD) measurement, overlay control, and defect inspection

This chapter provides a 15-year roadmap defining lithography's difficult challenges, technology requirements, and potential solutions. Additionally, this chapter defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for Environment, Safety, and Health (ESH); Yield Enhancement; Metrology; and Modeling and Simulation.

Since the earliest days of the microelectronics industry, optical lithography has been the mainstream technology for volume manufacturing, and it is expected to continue as such through the 45 nm node, through the application of resolution enhancement techniques such as off-axis illumination (OAI), phase shifting masks (PSM), optical proximity corrections (OPC), and possibly liquid immersion. In addition to resolution enhancement techniques, lenses with increasing numerical apertures and decreasing aberrations will be required to extend the life of optical lithography, and liquid immersion is also being considered as a means of extending optical lithography. It should be noted that it becomes much more difficult to implement OPC and resolution enhancement at the 65 nm node and beyond, compared to preceding nodes.

The requirements of the 32 nm node and beyond are viewed as beyond the capabilities of optical lithography. Extension of the Roadmap will require the development of next-generation lithography (NGL) technologies, such as extreme ultraviolet lithography (EUV), electron projection lithography (EPL), and imprint lithography. Because next generation lithographies will require the development of substantially new infrastructure, the costs of these technologies will put great pressure on manufacturing costs.

DIFFICULT CHALLENGES

The ten most difficult challenges to the continued shrinking of minimum feature sizes are shown in Table 76. Mask-making capability and cost escalation continue to be critical to future progress in lithography and will require continued focus. As a consequence of prior aggressive Roadmap acceleration—particularly the MPU gate linewidth (post etch), and increased mask error factors (MEFs) associated with low k_1 lithography—mask linewidth control appears as a particularly significant challenge going forward. For example, in the 1997 roadmap the 70 nm node requirements showed 4× masks needing 9 nm of CD control for isolated lines and 14 nm for contacts. The 2003 requirements are 6.4 nm for isolated lines and 5.5 nm for contacts assuming mask error factor (MEF) values of 1.0 (assuming alt-PSM masks) and 3.0, respectively. MPU gate CD control requirements will stress many other aspects of lithography process control, including lenses, resist processing equipment, resist materials, and metrology.

Mask equipment and process capabilities are in place for manufacturing masks with complex OPC and PSM, while mask processes for post-193 nm technologies are in research and development. Mask damage from electrostatic discharge (ESD) has long been a concern, and it is expected to be even more problematic as mask feature sizes shrink. Furthermore, masks for 157 nm lithography will be kept in ambient atmospheres nearly free of water, so the risk of ESD damage to masks will increase. A cost-effective pellicle solution has not yet been fully developed for 157 nm masks, further complicating mask handling for lithography at that wavelength.

While lithography has long contributed significantly to over-all semiconductor manufacturing costs, there is even greater concern going forward regarding cost control and return-on-investment (ROI). These issues of masks and lithography costs are relevant to optical, as well as next-generation lithography. To be extended further, optical lithography will require new resists that will provide both good pattern fidelity when exposed with short wavelengths (193 nm, possibly under immersion, and 157 nm), and improved performance during etch. Inadequacies in resist performance and CaF_2 quality and supply have already led to a slowdown in the pace of advances in lithography.

Process control, particularly for overlay and linewidths, also represents a major challenge. It is unclear whether metrology, which is fundamental to process control, will be adequate to meet future requirements as needed for both development and volume manufacturing. Resist line edge roughness (LER) is becoming significant, as gate linewidth control becomes comparable to the size of a polymer unit. Next-generation lithography will require careful attention to details as the exposure tools are based upon approaches that have never been used before in manufacturing. These tools must be developed and proven to be capable of meeting the reliability and utilization requirements of cost-effective manufacturing.

Table 76 Lithography Difficult Challenges

Five Difficult Challenges/ ≥ 50 nm Through 2009	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD control, defectivity, and 157 nm pellicles; defect free multi-layer EUV substrates or EPL membrane masks Equipment infrastructure (writers, inspection, repair)
Cost Control and Return on Investment (ROI)	Achieving constant/improved ratio of tool cost to throughput over time Cost-effective resolution enhanced optical masks and post-optical masks Sufficient lifetimes for the technologies Resources for developing multiple technologies at the same time High output, cost-effective, EUV light source
Process Control	Processes to control gate CDs to less than 1.8 nm (3 sigma) New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay Accuracy of OPC
Resists for ArF, Immersion Lithography and F_2	Outgassing, LER, SEM-induced CD changes, defects ≥ 30 nm.
CaF_2	Yield, cost, quality
Five Difficult Challenges/ < 45 nm Beyond 2010	
Mask Fabrication and Process Control	Defect-free NGL masks Equipment infrastructure (writers, inspection, repair) Mask process control methods
Metrology and Defect Inspection	Capability for critical dimensions down to 7 nm and metrology for overlay down to 7.2 nm, and patterned wafer defect inspection for defects < 30 nm
Cost Control and ROI	Achieving constant/improved ratio of tool cost to throughput Development of cost-effective post-optical masks Achieving ROI for industry with sufficient lifetimes for the technologies
Gate CD Control Improvements, Process Control, Resist Materials	Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay
Tools for Mass Production	Post optical exposure tools capable of meeting requirements of the Roadmap

SEM—scanning electron microscope

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Tables 77a and b)
- Resist Requirements (Tables 78a, b, and c)
- Mask Requirements (Tables 79a, b, and c)

Because of the particular challenges associated with imaging contact holes, contact hole size after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gates. This is important to comprehend in the Roadmap, because contacts have very small process windows and large mask error factors, and minor changes in the contact size have large implications for mask CD control requirements. Small MPU gates after etch are pursued aggressively and create significant challenges for metrology and process control.

Photoresists need to be developed that provide good pattern fidelity, good linewidth control (including roughness), and low defects. As feature sizes get smaller, defects and polymers will have comparable dimensions with implications for the filtering of resists.

The masks for all next-generation lithographies are radically different from optical masks, and no NGL technology can support a pellicle. Because the requirements for NGL masks are substantially different than those for optical lithography, separate tables have been included for Optical, EUV, and EPL masks (Tables 79a, b, and c, respectively). These masks have tight requirements for linewidth control and registration, because they will be applied at the 45 nm and beyond. EUV masks must also have very tight flatness control, and there are additional requirements for various parameters associated with reflectivity of EUV masks. EPL masks are comprised of thin membranes, and have special requirements. NGL masks, being different in form from optical masks, will also require the development of new defect inspection capabilities. Solutions for protecting the masks from defects added during storage, handling and use in the exposure tool need to be developed and tested, because there are no known pellicle options for NGL masks. These very different NGL mask requirements can be expected to exacerbate, rather than relieve, the high costs associated with masks that are already being encountered with optical masks.

Table 77a Lithography Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM							
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Contact in resist (nm)	130	110	100	90	80	70	60
Contact after etch (nm)	115	100	90	80	70	65	55
Overlay	35	32	28	25	23	21	19
CD control (3 sigma) (nm)	12.2	11.0	9.8	8.6	8.0	7.0	6.1
MPU							
MPU/ASCI Metal 1 (M1) ½ pitch (nm)	120	107	95	85	76	67	60
MPU ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
MPU gate in resist (nm)	◆ 65	53	45	40	35	32	28
MPU gate length after etch (nm)	45	37	32	28	25	22	20
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
Gate CD control (3 sigma) (nm)	◆ 4.0	3.3	2.9	2.5	2.2	2.0	1.8
ASIC/LP							
ASIC ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
ASIC/LP gate in resist (nm)	90	75	65	53	45	40	36
ASIC/LP gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
CD control (3 sigma) (nm)	5.8	4.7	4.0	3.3	2.9	2.5	2.2
Chip size (mm^2)							
DRAM, introduction	485	383	568	419	662	449	356
DRAM, production	139	110	82	122	97	131	104
MPU, high volume at introduction	280	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310	310
ASIC	704	704	704	704	704	704	704
Minimum field area	704	704	704	704	704	704	704
Wafer size (diameter, mm)	300	300	300	300	300	300	300

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

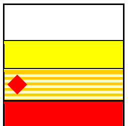
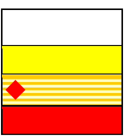


Table 77b Lithography Technology Requirements—Long-term

Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM						
DRAM ½ Pitch (nm)	45	35	32	25	22	18
Contact in resist (nm)	55	45	40	35	30	25
Contact after etch (m)	50	35	30	25	21	18
Overlay	18	14	12.8	10	8.8	7.2
CD control (3 sigma) (nm)	5.5	4.3	3.9	3.1	2.7	2.2
MPU						
MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54	42	38	30	27	21
MPU ½ Pitch (nm) (uncontacted gate)	45	35	32	25	22	18
MPU gate in resist (nm)	25	20	18	15	13	10
MPU gate length after etch (nm)	18	14	13	10	9	7
Contact in resist (nm)	59	46	42	33	30	23
Contact after etch (nm)	54	42	38	30	27	21
CD control (3 sigma) (nm)	1.6	1.3	1.2	0.9	0.8	0.6
ASIC/LP						
ASIC ½ Pitch (nm) (uncontacted gate)	45	35	32	25	22	16
ASIC/LP gate in resist (nm)	32	27	22	19	16	13
ASIC/LP gate length after etch (nm)	22	19	16	14	11	9
Contact in resist (nm)	59	46	42	33	30	23
Contact after etch (nm)	54	42	38	30	27	21
CD control (3 sigma) (nm)	2.0	1.7	1.4	1.3	1.0	0.8
Chip size (mm^2)						
DRAM, introduction	563	353	*560*	*351*	*464*	*292*
DRAM, production	83	104	83	104	138	87
MPU, high volume at introduction	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310
ASIC	704	704	704	704	704	704
Minimum field area	704	704	704	704	704	704
Wafer size (diameter, mm)	300	450	450	450	450	450

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 77a and 77b:
[1] The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists, and masks for manufacturing must be available one year earlier. Development capability must be available two–three years earlier.
[2] Linewidth variations are based on linewidth deviations from target dimensions for all critical features for a given product. For example, for microprocessors these would be the gate features critical to circuit performance. This total linewidth variation includes contributions from errors within each exposure field for features of various orientations and with varying pitch. Variations also include contributions from linewidth changes across individual wafers and from wafer-to-wafer. The variances of the final dimensions after etch are assumed to result 2/3 from variance of the linewidths in resist and 1/3 from the etch process for all processes except MPU gates, where it is assumed that 80% of the variance of the linewidths comes from resist and 20% from the etch process. It is assumed that the allowable variations in linewidth are ±15% of the final, etch feature size for DRAMs and ASICS and ±10% for MPUs

Table 78a Resist Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (un-contacted gate)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Gate in resist Length (nm)	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Gate Length after etch (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
*Resist Characteristics **							
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) ***	◆ **4.0**	**3.3**	**2.9**	**2.5**	**2.2**	**2.0**	**1.8**
*Resist thickness (nm, imaging layer) ****	**250–400**	**220–360**	**200–320**	**170–250**	**160–220**	**140–200**	**130–180**
*Ultra thin resist thickness (nm)*****	**120–150**	**120–150**	**120–150**	**100–150**	**100–130**	**100–130**	**80-120**
PEB temperature sensitivity (nm/C)	**2.5**	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**
Backside particles (particles/m^2 at critical size, nm)	**2000 @ 150**	**2000 @ 150**	**1500 @ 100**	**1500 @ 100**	**1500 @ 100**	**1500 @ 100**	**1000 @ 50**
Defects in spin-coated resist films† #/cm^2	**0.02**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
(size in nm)	**60**	**55**	**50**	**45**	**40**	**35**	**30**
Defects in patterned resist films, gates, contacts, etc. #/cm^2	**0.07**	**0.06**	**0.05**	**0.04**	**0.04**	**0.03**	**0.03**
(size in nm)	**60**	**55**	**50**	**45**	**40**	**35**	**30**
*Line Width Roughness (nm, 3 sigma) <8% of CD *******	◆ **3.6**	**3.0**	**2.6**	**2.2**	**2.0**	**1.8**	**1.6**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

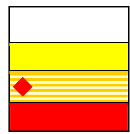


Table 78b Resist Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**	**42**	**38**	**30**	**27**	**21**
MPU/ASIC ½ Pitch (nm)	**45**	**35**	**32**	**25**	**22**	**18**
MPU Printed Gate Length (nm)	**25**	**20**	**18**	**15**	**13**	**10**
MPU Physical Gate Length (nm)	**18**	**14**	**13**	**10**	**9**	**7**
*Resist Characteristics **						
*Resist meets requirements for resolution and gate CD Control (nm, 3 sigma) ***	**1.6**	**1.3**	**1.2**	**0.9**	**0.8**	**0.6**
*Resist thickness (nm, imaging layer) ****	**120–160**	**80–140**	**80–140**	**60–100**	**50–80**	**40–70**
*Ultra thin resist thickness (nm)****	**80–120**	**60–100**	**60–100**	**40–80**	**40–60**	**40–60**
PEB temperature sensitivity (nm/C)	**1.5**	**1.5**	**1**	**1**	**1**	**1**
Backside particles (particles/m^2 at critical size, nm)	**1000 @ 50**	**1000 @ 50**	**1000 @ 50**	**1000 @ 50**	**500 @ 50**	**500 @ 50**
Defects in spin-coated resist films #/cm^2	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
(size in nm)	**30**	**20**	**20**	**10**	**10**	**10**
Defects in patterned resist films for gates, contacts, etc. #/cm^2	**0.03**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
(size in nm)	**30**	**20**	**20**	**10**	**10**	**10**
*Line Width Roughness (nm, 3 sigma) <8% of CD *******	**1.4**	**1.1**	**1.0**	**0.8**	**0.7**	**0.6**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 78c Resist Sensitivities

Exposure Technology	*Sensitivity*
248 nm	**20–50 mJ/ cm^2**
193 nm	**10–30 mJ/ cm^2**
157 nm	**5–15 mJ/ cm^2**
Extreme Ultraviolet at 13.5 nm	**2–15 mJ/ cm^2**
*Electron Beam Projection at 100 kV ******	**2–10 uC/ cm^2**
*E-beam Direct Write at 50 kV ******	**5–10 uC/ cm^2**

****** Linked with resolution*

Notes for Tables 78a and 78b:
Exposure Dependent Requirements
* Resist sensitivity is treated separately in the second resist sensitivities table (separate sheet).
** Indicates whether the resist has sufficient resolution, CD control, and profile to meet the resolution and gate CD control values.
*** Resist thickness is determined by the aspect ratio range of 2.5:1 to 4:1, limited by pattern collapse.
**** Resist thickness of top imaging layer of a multi-layer resist determined by opacity to the exposure source.
***** Linked with resolution.

****** *LWR is 3σ of the linewidth over a range of spatial frequencies given by* $\frac{1}{P} \le \text{spatial frequences} \le \frac{1}{0.5X_j}$ *, where P is the pitch and* X_j *is the low-end-of-range of the drain extension found in the Thermal and Thin Film, Doping and Etching Technology Requirements Table.*
*LWR=SQRT(2)*LER.*
† Defects in coated films are those detectable as physical objects, such as pinholes, that may be distinguished from the resist film by optical detection methods.
Other requirements:
[A] Need for a positive tone resist and a negative tone resist will depend upon critical feature type and density.
[B] Feature wall profile should be 90 ± 2 degrees.
[C] Thermal stability should be ≥ 130°C.
[D] Etching selectivity should be > that of poly hydroxystyrene (PHOST).
[E] Upon removal by stripping there should be no detectible residues.
[F] Sensitive to basic airborne compounds such as amines and amides. Clean handling space should have <1000 pptM of these materials.
[G] Metal contaminants < 5 ppb.
[H] Organic material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e12. Value for EUV lithography tool is <5e13. Values for electron projection are being determined.
[I] Si containing material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 157 nm lithography tool is <1e8. Value for EUV lithography tool is <5e13. Values for electron projection are being determined.

Table 79a Optical Mask Requirements

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Wafer minimum half pitch (nm)	100	90	80	70	65	57	50
Wafer minimum line (nm, in resist) [A]	◆ 65	53	45	40	35	32	30
Wafer minimum line (nm, post etch)	45	37	32	28	25	22	20
Overlay	35	32	28	25	23	21	19
Wafer minimum contact hole (nm, post etch)	115	100	90	80	70	65	55
Magnification [B]	4	4	4	4	4	4	4
Mask nominal image size (nm) [C]	260	212	180	160	140	128	112
Mask minimum primary feature size [D]	182	148.4	126	112	98	89.6	78.4
Mask OPC feature size (nm) clear	200	180	160	140	130	114	100
Mask sub-resolution feature size (nm) opaque [E]	130	106	90	80	70	64	56
Image placement (nm, multi-point) [F]	21	19	17	15	14	13	12
CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
MEF isolated lines, binary [G]	1.4	1.4	1.4	1.4	1.6	1.6	1.6
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask [H]	◆ 4.6	3.8	3.3	2.9	2.2	2.0	1.8
MEF isolated lines, alternating phase shift [G]	1	1	1	1	1	1	1
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), alternating phase shift mask [I]	6.4	5.3	4.6	4.0	3.6	3.1	2.9
MEF dense lines [G]	2	2	2	2	2.5	3	3
CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	9.8	8.8	7.8	6.9	5.1	3.7	3.3
MEF contacts [G]	3	3	3	3	3.5	4	4
CD uniformity (nm, 3 sigma), contact/vias [K]	◆ 5.0	4.4	3.9	3.5	2.6	2.1	1.8
Linearity (nm) [L]	15.2	13.7	12.2	10.6	9.9	8.7	7.6
CD mean to target (nm) [M]	8.0	7.2	6.4	5.6	5.2	4.6	4.0
Defect size (nm) [N] *	80	72	64	56	52	45.6	40
Substrate form factor	152 × 152 × 6.35						
Blank flatness (nm, peak-valley) [O]	480	410	365	320	298	252	192
Transmission uniformity to mask (pellicle and clear feature) (±% 3 sigma)	1	1	1	1	1	1	1
Data volume (GB) [P]	144	216	324	486	729	1094	1640
Mask design grid (nm) [Q]	4	4	4	2	2	2	2

The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.

180 degree phase defects are 70% of number shown.

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

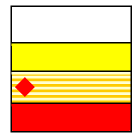
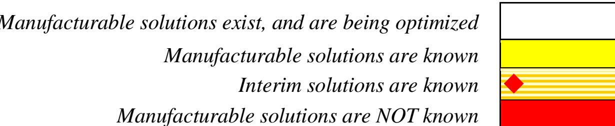


Table 79a Optical Mask Requirements (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm)	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Attenuated PSM transmission mean deviation from target (± % of target) [R]	**5**	**5**	**5**	**4**	**4**	**4**	**4**
Attenuated PSM transmission uniformity (±% of target) [R]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Attenuated PSM phase mean deviation from 180º (± degree) [S]	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Alternating PSM phase mean deviation from nominal phase angle target 180º degrees (± degree) [S]	**2**	**2**	**2**	**1**	**1**	**1**	**1**
Alternating PSM phase uniformity (± degree) [T]	**2**	**◆ 2**	**◆ 2**	**1**	**1**	**1**	**1**
Nominal reflectivity (%) [U]	**20%**	**20%**	**15%**	**15%**	**15%**	**10%**	**10%**
Mask materials and substrates	**Absorber on fused silica, except for 157 nm optical that will be absorber on fluorine doped, low OH fused silica substrate.**						
Strategy for protecting mask from defects	**Pellicle for optical masks down to 193 nm.**				**Modified fused silica pellicles have demonstrated feasibility for 157- nm scanners, and removable pellicles might be useful for small lot production. Research continues on organic membrane pellicles materials in a search for viable solutions.**		
(Exposure tool dependent)	**Primary PSM choices are attenuated shifter and alternating aperture**						

The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.
180 degree phase defects are 70% of number shown



Notes for Table 79a—Optical Mask requirements:
[A] Wafer Minimum Line Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
[B] Magnification—Lithography tool reduction ratio, N:1.
[C] Mask Nominal Image Size— Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio which equals 4×.
[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.
[E] Mask Sub-Resolution Feature Size—The minimum width of isolated non-printing features on the mask such as sub-resolution assist features.
[F] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error post pellicle mount. These values do not comprehend additional image placement error induced by pellicle mount and mask clamping in the exposure tool.
[G] The CD error on the wafer is directly proportional to the CD error on the mask where mask error factor (MEF) is the constant of proportionality. An MEF value greater than unity therefore imposes a more stringent CD uniformity requirement on the mask to maintain the CD uniformity budget on the wafer.
[H] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and isolated features on a binary mask.
[I] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a quartz shifter phase mask.
[J] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a binary or attenuated phase shift mask.
[K] CD Uniformity—The three-sigma deviation of square root of contact area on a mask through multiple pitches.

[L] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are equal to the smallest sub-resolution assist mask feature and up to three times the minimum wafer half pitch multiplied by the magnification.
[M] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.
[N] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[O] Blank Flatness—Flatness is nanometers, peak-to-valley across the 110 mm × 110 mm central area image field on a 6-inch ×6-inch square mask blank. Flatness is derived from wafer lithography DOF requirements for each node.
[P] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
[Q] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[R] Transmission—Ratio, expressed in percent, of the fraction of light passing through an attenuated PSM layer relative to the mask blank with no opaque films.
[S] Phase—Change in optical path length between two regions on the mask expressed in degrees.
[T] Alt PSM phase uniformity is a range specification equal to the maximum phase error deviation of any point from the target.
[U] Optimization of mask reflectivity for wavelengths used for optical (laser) mask patterning versus optical inspection versus wafer exposure is a recognized issue to be addressed in the future.

Table 79b EUVL Mask Requirements

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
Wafer minimum half pitch (nm)	**57**	**50**	**45**	**35**	**32**	**25**	**22**	**18**
Wafer minimum line (nm, in resist) [A]	**32**	**30**	**25**	**20**	**18**	**15**	**13**	**10**
Wafer minimum line (nm, post etch)	**22**	**20**	**18**	**14**	**13**	**10**	**9**	**7**
Overlay	**21**	**19**	**18**	**14**	**12.8**	**10**	**8.8**	**7.2**
Wafer minimum contact hole (nm, after etch)	**65**	**55**	**50**	**35**	**30**	**25**	**21**	**18**
Generic Mask Requirements								
Magnification [B]	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Mask nominal image size (nm) [C]	**128**	**120**	**100**	**80**	**72**	**60**	**52**	**40**
Mask minimum primary feature size [D]	**114**	**100**	**90**	**70**	**64**	**50**	**44**	**36**
Image placement (nm, multi-point) [E]	**13**	**11.5**	**11**	**9**	**8**	**6**	**6**	**5**
CD Uniformity (nm, 3 sigma) [F]								
Isolated lines (MPU gates)	**3.0**	**2.5**	**2.0**	**1.5**	**1.3**	**0.7**	**0.5**	**0.4**
Dense lines DRAM (half pitch)	**12.5**	**11**	**9**	**6.5**	**5.5**	**2.0**	**1.5**	**1.0**
Contact/vias	**8**	**7**	**6.5**	**4.5**	**3.5**	**2.5**	**2.0**	**1.5**
Linearity (nm) [G]	**8**	**7**	**6.5**	**5**	**4.5**	**3.5**	**3.5**	**2.5**
CD mean to target (nm) [H]	**4**	**3.5**	**3**	**2.5**	**2**	**1.5**	**1.5**	**1**
Defect size (nm) [I]	**40**	**36**	**32**	**26**	**23**	**18**	**16**	**13**
Data volume (GB) [J]	**730**	**1096**	**1644**	**2466**	**3700**	**5550**	**8326**	**12490**
Mask design grid (nm) [K]	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 79b EUVL Mask Requirements (continued)

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
EUVL-specific Mask Requirements								
Substrate defect size (nm) [L]	30	29	27	24	23	19	18	14
Mean peak reflectivity	65%	66%	66%	67%	67%	67%	67%	67%
Peak reflectivity uniformity (% 3 sigma absolute)	0.58%	0.56%	0.54%	0.48%	0.42%	0.36%	0.30%	0.24%
Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.06	0.06	0.06	0.05	0.05	0.05	0.04	0.04
Minimum absorber sidewall angle (degrees)	85	85	85	85	85	85	85	85
Absorber sidewall angle tolerance (± degrees)	1	1	0.75	0.62	0.5	0.5	0.5	0.5
Absorber LER (3 sigma nm) [N]	4	4	3	2.5	90	3	2	2
Mask substrate flatness (nm peak-to-valley) [O]	◆ 65	◆ 60	55	45	40	30	25	20
Maximum aspect ratio of absorber stack	1	1.1	1.3	1.4	1.5	1.6	1.7	1.7

Legend	
Manufacturable solutions exist, and are being optimized	(white)
Manufacturable solutions are known	(yellow)
Interim solutions are known	◆
Manufacturable solutions are NOT known	(red)

Notes for Table 79b—EUV Mask requirements:
EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.
[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
[B] Magnification—Lithography tool reduction ratio, N:1.
[C] Mask Nominal Image Size— Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD, placement, and defects.
[E] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.
[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).
[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.
[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.
[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[L] Substrate Defect Size—the minimum diameter spherical defect (in polystyrene latex sphere equivalent dimensions) on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.
[M] Includes variation in median wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.
[N] Line edge roughness (LER)—is defined a roughness 3 sigma one-sided for spatial period <mask primary feature size.
[O] Mask Substrate Flatness—Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge, which may be compensated by the mask mounting and leveling method in the exposure tool. The flatness error is defined as the deviation of the surface from the plane that minimizes the maximum deviation. This flatness requirement applies to each of the front and backsides individually.

Table 79c EPL Mask Requirements

Year of Production	*2008*		*2009*		*2010*		*2012*		*2013*		*2015*		*2016*		*2018*	
Technology Node					*hp45*				*hp32*				*hp22*			
DRAM ½ Pitch (nm)	***57***		***50***													
Wafer minimum half pitch (nm) [A]	**57**		**50**		**45**		**35**		**32**		**25**		**22**		**18**	
Wafer minimum line (nm, in resist)	**32**		**30**		**25**		**20**		**18**		**15**		**13**		**10**	
Wafer minimum line (nm, post etch)	**22**		**20**		**18**		**14**		**13**		**10**		**9**		**7**	
Overlay	**21**		**19**		**18**		**14**		**12.8**		**10**		**8.8**		**7.2**	
Wafer minimum contact hole (nm, post etch)	**65**		**55**		**50**		**35**		**30**		**25**		**21**		**18**	
Generic mask requirements																
Magnification [B]	**4**		**4**		**4**		**4**		**4**		**4**		**4**		**4**	
Mask minimum image size (nm) [C]	**89**		**84**		**70**		**56**		**50**		**42**		**36**		**28**	
Image placement error in sub-field (nm, multi-point) [D]	**9**		**8.5**		**8**		**6**		**5.5**		**4.5**		**4**		**3.5**	
Sub-field placement error on mask (nm, 3 sigma, non-linear term) [E]	**9**		**8.5**		**8**		**6**		**5.5**		**4.5**		**4**		**3.5**	
CD Uniformity (nm, 3 sigma) [F]																
Isolated lines (MPU gates)	**3**		**2.8**		**2.5**		**2**		**1.8**		**1.4**		**1.2**		**1**	
Dense lines (DRAM half pitch)	**13**		**12**		**9**		**7**		**6.5**		**5.0**		**4.5**		**4.0**	
Contact/vias	**8.0**		**7**		**6.5**		**3.5**		**2.5**		**3.5**		**3.0**		**2.5**	
Linearity (nm) [G]	**9**		**8**		**7**		**5.5**		**5**		**4**		**3.5**		**3**	
CD mean to target (nm) [H]	**4.5**		**4**		**3.5**		**2.5**		**2.5**		**2**		**1.5**		**1**	
Pattern corner rounding (nm)	**35**		**31**		**28**		**22**		**20**		**16**		**14**		**11**	
Defect size (nm) [I]	**45**		**40**		**35**		**25**		**25**		**20**		**15**		**10**	
Data volume (GB) [J]	**730**		**1096**		**1644**		**2466**		**3700**		**5550**		**8326**		**12490**	
Mask design grid (nm) [K]	**4**		**4**		**4**		**4**		**4**		**4**		**4**		**4**	
EPL-specific Mask Requirements																
Mask type	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**	**Mem-brane [T]**	**Stencil [U]**
Clear area transmission factor [L]	**50%**	**100%**	**50%**	**100%**	**50%**	**100%**	**70%**	**100%**	**70%**	**100%**	**70%**	**100%**	**70%**	**100%**	**70%**	**100%**
Membrane thickness uniformity (3 sigma %) [M]	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**	**2%**	**N/A**
Membrane thickness uniformity in sub-field (3 sigma %) [N]	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**	**1%**	**N/A**
Membrane mean thickness error (%) [O]	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**	**10%**	**N/A**
Scatterer thickness uniformity in mask (3 sigma %) [P]	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
Scatterer mean thickness error (%) [Q]	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
Pattern sidewall angle (degrees)	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

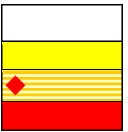


Table 79c EPL Mask Requirements (continued)

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	***57***	***50***						
Pattern sidewall angle tolerance (+ degrees) [R]	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**	**0.3**
Scatterer/stencil LER (3 sigma nm) [S]	**4.5**	**4**	**3.5**	**3**	**3**	**3**	**3**	**3**
Mask substrate flatness (micron peak-to-valley)	**10**	**5**	**5**	**5**	**5**	**4**	**4**	**3**
Mask flatness within a sub-field (micron peak-to-valley)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Table 79c—EPL Mask requirements
EPL masks have hundreds of sub-fields (~1 by 1 mm), and each sub-field corresponds to a membrane surrounded by Si struts
[A] Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity).
[B] Magnification—Lithography tool reduction ratio, N:1.
[C] Mask Minimum Image Size—The nominal mask size of the smallest primary feature to be transferred to the wafer (Includes biasing for proximity effect correction).
[D] Image Placement Error in Sub-field—The three sigma deviation (X or Y) of the images in a sub-field relative to a defined reference grid. Please note that a sub-field is 1 mm × 1 mm on the mask. These values do not comprehend additional image placement error induced by mask clamping in the exposure tool.
[E] Sub-field Placement in Mask—The three sigma non-linear deviation (X or Y) of the position of sub-fields on mask relative to a defined reference grid. The position of each sub-field can be represented by a mark on the strut adjacent to the sub-field. Note that the EPL exposure tool can correct sub-field positions on wafer in accordance with the measurement results of sub-field positions on mask. These values do not comprehend additional image placement error induced by mask clamping in the exposure tool.
[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature.
[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and less than three times the minimum wafer half pitch multiplied by the magnification.
[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed upon feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.
[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[L] Clear Area Transmission Factor—Percentage of current incident on a clear area on the mask relative to that arriving at wafer through the axial back focal plane aperture of the projection optics of the exposure tool (for NA of 6–8 mrad).
[M] Membrane Thickness Uniformity in Mask—The three sigma variation of membrane thickness over a mask.
[N] Membrane Thickness Uniformity in Sub-field—The three sigma variation of membrane thickness over a sub-field. Note that a sub-field is a 1×1 mm area.
[O] Membrane Mean Thickness Error—Maximum deviation of mean membrane thickness from designed value.
[P] Scatterer Thickness Uniformity in Mask—The three sigma variation of scatterer thickness over a mask.
[Q] Scatterer Mean Thickness Error—Maximum deviation of scatterer thickness from designed value.
[R] Pattern Sidewall Angle—Sidewall angle must be 90 degrees with respect to the plane of the membrane surface. The sidewall may only be slightly retrograde, so the angle must be 90 degrees plus the tolerance.
[S] Scatterer/stencil LER—Line edge roughness (LER) is defined as roughness 3 sigma one-sided for spatial period < minimum linewidth.
[T] Membrane masks have patterned scattering layers on each membrane.
[U] Stencil masks have patterns etched through the membranes in each sub-field.

POTENTIAL SOLUTIONS

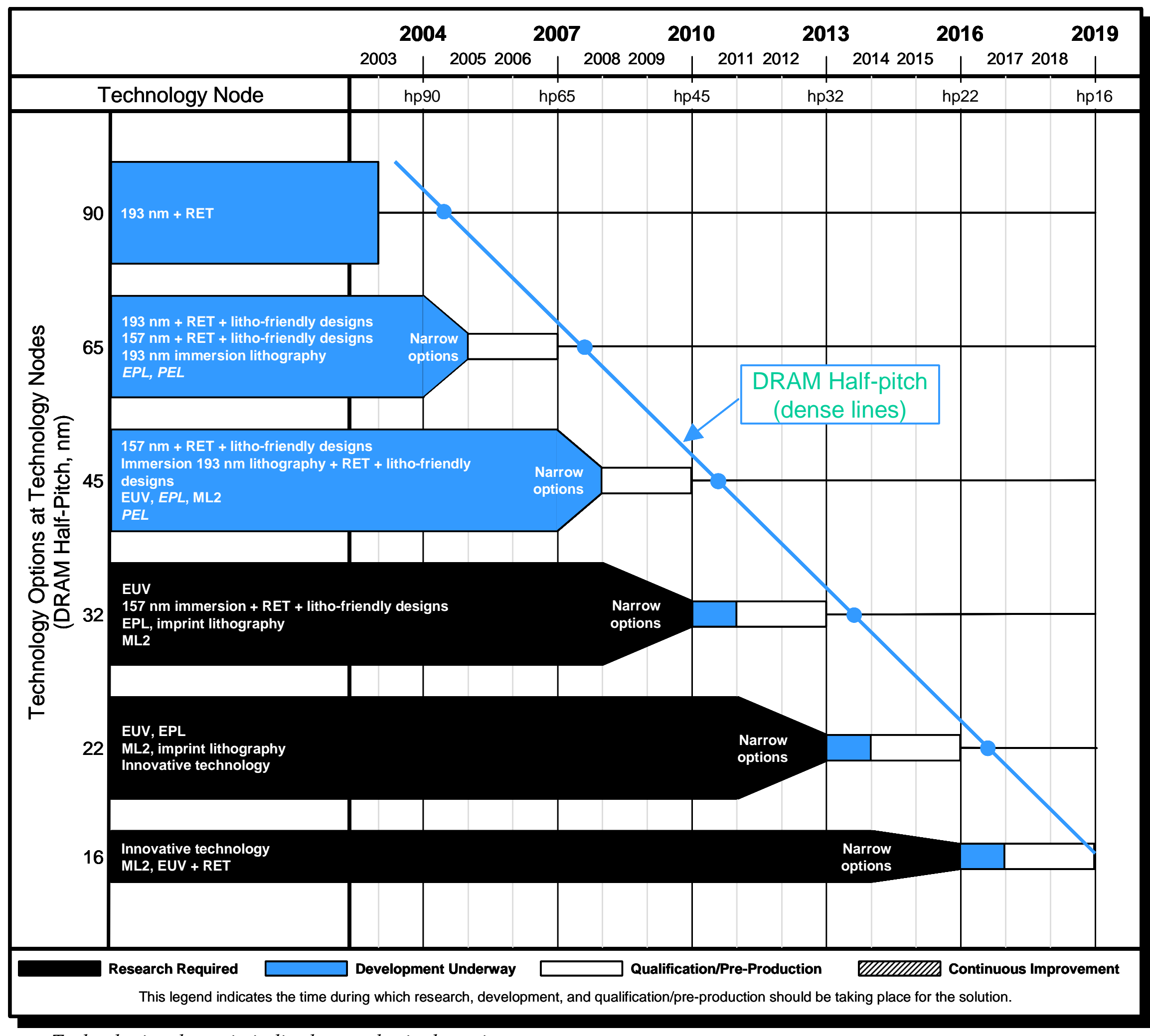
The potential solutions for lithography are presented in Figure 53. Optical lithography is expected to be the dominant approach through the 65 nm node, with NGL possibly appearing at the 45 nm node, although more likely later. For leading-edge semiconductor manufacturing, 193 nm lithography has replaced 248 nm lithography as the wavelength for critical layer patterning. Significant improvements in 193 nm resists and CaF_2 are still needed for future applications of 193 nm lithography, and 157 nm lithography is still in early development. Perhaps the most significant decision to be made regarding potential solutions involves immersion lithography. If this technology proves viable, it has the potential to extend 193 nm imaging to the 45 nm node, thus delaying or obviating the introduction of 157 nm lithography. Immersion lithography could extend optical lithography close to the 32 nm node if it can be implemented using 157 nm light. Thus, immersion lithography has an impact on the possible implementation of 157 nm lithography, and then later on the timing for the insertion of next-generation lithographies.

The post-optical or next-generation lithography (NGL) alternatives are all candidates at and below 45 nm. Of the possible NGL technologies, multiple regions consider EUV, EPL, maskless (ML2), and imprint lithography as potential successors to optical lithography. There are activities taking place in other lithographic technologies, such as proximity electron lithography (PEL), but these activities are confined largely to single regions. Proximity x-ray lithography and ion projection lithography are currently not considered as potential solutions, but imprint lithography has been added. Imprint lithography has the potential to be a cost-effective solution, but there are a number of problems that need to be solved for this to happen, including the difficulties associated with 1× masks, defects and overlay. It is unclear whether any technology currently identified as a potential solution will indeed be capable of meeting the requirements of the 18 nm node.

Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. The elimination of proximity x-ray and ion projection lithography has not reduced the number of technologies that require simultaneous development, because of the recent emergence of immersion lithography and imprint lithography. Closely coordinated global interactions within industry and the universities are absolutely necessary to narrow the options for these future generations.

The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities that are necessary for continued adherence to Moore's Law at the 32 nm node and beyond. This shift will drive major changes throughout the lithography infrastructure and will require significant resources for commercialization. These development costs must necessarily be recovered in the costs of exposure tools, masks, and materials.

Direct write lithography has been applied to niche applications in development and low volume ASIC production, but its role could be expanded. Breakthroughs in direct-write technologies that achieve high throughput will be a significant paradigm shift. It will eliminate the need for masks, offering inherent cost and cycle-time reduction. Other technologies that eliminate the need for masks and resist would likewise constitute a paradigm shift. Maskless lithography (ML2) is currently in the research phase, and many significant technological hurdles will need to be overcome for ML2 to be viable for cost-effective semiconductor manufacturing.



Technologies shown in italics have only single region support.
RET—resolution enhancement technology EUV—extreme ultraviolet EPL—electron projection lithography
ML2—maskless lithography PEL—proximity electron lithography

Figure 53 Lithography Exposure Tool Potential Solutions

CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions involving Lithography, ESH, Yield Enhancement, Metrology, and Modeling and Simulation are outlined in this section.

ENVIRONMENT, SAFETY, AND HEALTH

The recent discussion over the continued use of perfluorooctyl sulfonates (PFOS) in photochemicals has shown that long- and commonly-used materials can have safety issues that are being understood only recently. The introduction of new technologies necessarily means the use of materials and chemicals whose safety and environmental implications are even less well known. Practices for use and disposal of the chemicals utilized in lithography must continue with careful regard for the safety of workers and their environment. Refer to the *Environment, Safety, and Health* chapter for comprehensive information and link to a new chemical screening tool (Chemical Restrictions Table).

YIELD ENHANCEMENT

Yield enhancement is expected to become a major challenge, as critical defect sizes become smaller than the limits of optical detection. Non-optical methods of defect detection have yet been demonstrated to have the acquisition rates required for controlling defects in semiconductor manufacturing.

METROLOGY

The rapid advancement of lithography technology and resultant decrease in feature dimensions continues to challenge wafer and mask metrology capability. The existing precision of critical dimension measurement tools does not meet the somewhat relaxed 20% measurement precision-to-process tolerance metric at the most advanced technology nodes. Precision includes measurement tool variation from short- and long-term tool variation as well as tool-to-tool matching. Wafer and mask CD technology is evolving to meet the need for 3D measurements. Potential solutions for near-term CD measurements include CD-scanning electron microscopy, scatterometry, and scanned probe microscopy. A key requirement is measurement of line edge roughness (LER). Measurement precision for LER must be smaller (better) than that needed for linewidth.

Overlay metrology is also challenged by future technology generations. Traditional overlay test structures do not capture all possible overlay errors that can occur during use of phase shift and optical proximity correction masks.

The complete discussion of Lithography Metrology is located in the Lithography Metrology and Microscopy sections of the *Metrology* chapter. The Lithography Metrology Technology Requirements and Potential Solutions is also presented in that chapter.

MODELING AND SIMULATION

Support from Modeling and Simulation is strongly needed both for the efforts to push the limits of traditional optical lithography and for the assessment of new Next Generation Lithography technologies. The application of simulation tools in lithography largely benefits from the well-known physical basis of Maxwell's equations, which, however, need a problem-specific and efficient implementation in simulation tools. On the other hand side the physical/chemical understanding of resist processes, particularly for chemically amplified resists, is far less advanced, requiring additional calibration and model development work.

Concerning the simulation of optical imaging, the key requirements for applications in lithography are accuracy, speed of computation, and the capability to deal with the complex systems which occur, including non-ideal masks, optical system imperfections, multilayer resists and non-planar substrates. Problem-specific algorithms and implementations are needed to deal with the enhancements used when pushing optical lithography to the limits, such as immersion, polarization, off-axis illumination, complicated mask geometries including phase-shifting, and optical proximity correction. Non-linearities of the optical systems used are getting more critical and must be appropriately addressed in simulation. The influence of defects on the mask and on the wafer is becoming more important and requires appropriate simulation capabilities, especially for the identification of "printable defects." New techniques used in future next generation lithography, such as replacement of refractive lenses by multilayer mirrors or the use of reflecting masks, must be appropriately modeled and included in the simulation programs.

A specific challenge for lithography modeling and simulation is state-of-the-art photoresists. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as line-edge roughness (LER). Better calibration techniques are required both for model development and for customizing models implemented in commercial tools to appropriately describe the photoresists in question. Intimate links with etching simulation must be established to predict the geometry of non-ideal mask edges that are frequently result of the complete lithography step.

A specific requirement for lithography modeling and simulation is the need for very efficient simulation tools that allow the simulation of large areas and/or the conduction of simulation studies for a multitude of variations of physical parameters or layouts. Details on developments needed to satisfy these requirements are given in the *Modeling and Simulation* chapter.

INTER-FOCUS ITWG DISCUSSION

Gate CD control capability has impacts on devices (process integration, devices, and structures [PIDS]), front-end processes (FEP), metrology and design. Depending upon the level of CD control that is possible, there will be more or less stringent requirements on the other processes that affect transistor performance, such as implant, diffusion and etch. Tight CD control will require metrology that is capability of supporting the control requirements. Design will need to take into account the collective capabilities of all processes that affect transistor performance.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

Emerging devices are expected to have impacts on lithography primarily in two areas. First, a number of devices that have been considered require critical layer patterning over non-planar substrates, which will require lithographic solutions that can provide tight CD control over the topography. For example, bilayer resists represent a possible solution to this problem. Large depth-of-focus may become a compelling advantage for certain lithographic technologies, such as electron projection lithography. Second, emerging devices could provide relief for the control of gate CDs. This will have an impact on all aspects of lithographic technology, including masks, resists, exposure tools, and metrology.