INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

METROLOGY

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METROLOGY

Metrology, including materials characterization, continues to enable the introduction and manufacture of new materials, processes, and structures. The pace of feature size reduction challenges traditional measurement technology, and the uncertain nature of device design adds to the challenge. Long-term research into nano-devices may provide both new measurement methods and potential test vehicles for metrology. Although most metrology done inside new manufacturing facilities uses in-line equipment, the evolution to *in situ* continues. All metrology is connected to factory-wide automation that include database and intelligent information from data capability. Off-line materials characterization is also evolving toward compatibility with factory-wide automation. Although thorough materials characterization is a critical part of materials and process development, predicting the necessary metrology for manufacturing remains an elusive goal. Issues resolved by process improvements leave open the question of what to measure during manufacturing to ensure reliability.

The relationship between metrology and process technology development needs fundamental restructuring. In the past the challenge has been to develop metrology ahead of target process technology. Today we face major uncertainty from unresolved choices of fundamentally new materials and radically different device designs. *Understanding the interaction between metrology data and information and optimum feed forward and real-time process control are key to restructuring the relationship between metrology and process technology.* A new section has been added to the Metrology Roadmap that covers metrology needs for emerging technology paradigms such as spintronics and molecular electronics.

Research and development of new as well as evolutionary metrology technology must keep pace with the three-year schedule for introduction of new technology generations. The roadmap for feature size reduction drives the timeline for metrology solutions for new materials, process, and structures. New substrate materials such as silicon on insulator and strained silicon channels add to the complexity of measurements. Metrology development must be done in the context of these issues. Metrology enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The increasing diversity of chip types will spread already limited metrology resources over a wider range of challenges. The metrology community including suppliers, chip manufacturers, consortia, and research institutions must provide cooperative research, development, and prototyping in order to meet the ITRS timeline. *The forefront developments in measurement technology must be commercialized in a timely manner.* The feature sizes and materials a decade away in the 2003 Roadmap already greatly challenge the measurements used in process and materials development.

The near term challenges for metrology revolve around the need for controlling scaling as well as new materials and processes used for gate stack, ultra-shallow junctions, and copper/low-κ interconnect. The large number of candidate materials being considered for each node require characterization in evaluation and control in development and process. Moreover, it is entirely possible that different materials will be used by different manufacturers at a given node, potentially requiring different metrologies. Advances in electrical and physical metrology for high- and low-κ dielectric films must continue, and new metrology for pore size distribution and voids in copper lines are being evaluated. The increasing emphasis on active area measurements instead of test structures in scribe (kerf) lines places new demands on metrology. Long-term needs are difficult to address due to the lack of clarity of device design and interconnect technology. The selection of a replacement for copper interconnect remains a research challenge. Although materials characterization and some existing in-line metrology apply to new device and interconnect structures, development of manufacturing capable metrology requires a more certain knowledge of materials, devices, and interconnect structures.

All areas of measurement technology (especially those covered in the *Yield Enhancement chapter*) are being combined with computer integrated manufacturing (CIM) and data management systems for information-based process control. Although Integrated Metrology still needs a universal definition, it has become the term associated with the slow migration from offline to inline and *in situ* measurements. The proper combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

Metrology tool development requires access to new materials and structures if it is to be successful. It requires the availability of state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of production. This requires a greater attention to expanding close ties between metrology development and process development. When the metrology is well matched to the process tools and

processes, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

SCOPE

The metrology topics covered in the 2003 *Metrology* roadmap are microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; *in situ* sensors and cluster stations for process control; reference materials; correlation of physical and electrical measurements; and packaging. These topics are reported in the following sections: *Measurements for Processes Facing Statistical Limits and Physical Structures Reaching Atomic Dimensions*; *Microscopy*; *Lithography Metrology*; *Front End Processes Metrology*; *Interconnect Metrology*; *Materials and Contamination Characterization*; *Integrated Metrology*; *Reference Measurement Systems*, *Reference Materials*; *and Characterization and Metrology for Emerging Devices.*

International cooperation in the development of new metrology technology and standards will be required. Both metrology and process research and development organizations must work together with the industry including both the supplier and IC manufacturer. Earlier cooperation between IC manufacturers and metrology suppliers will provide technology roadmaps that maximize the effectiveness of measurement equipment. Metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. Despite the existence of standardized definitions and procedures for metrics, individualized implementation of metrics such as measurement precision to tolerance (P/T) ratio is typical.[1] The P/T ratio for evaluation of automated measurement capability for use in statistical process control relates the measurement variation (precision) of the metrology tool to the product specification limits. Determination of measurement tool variations is sometimes carried out using reference materials that are not representative of the product or process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. It is also possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a need for metrics that accurately describe the resolution capability of metrology tools for use in statistical process control. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio. However, because the type of resolution depends on the process (e.g., thickness and width require spatial resolution while levels of metallics on the surface require resolution of atomic percent differences), topic-specific metrics may be required. A new need is for standardized approach to determination of precision when the metrology tool provides discrete instead of continuous data. This situation occurs, for example, when significant differences are smaller than the instrument resolution.

The principles of Integrated Metrology can be applied to stand-alone and sensor based metrology itself. Factors that impact tool calibration and measurement precision such as small changes in ambient temperature and humidity could be monitored and used to improve metrology tool performance and thus improve statistical process control.

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for metrology should decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS based metrology and nano-technology are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales.

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[1] *For example, refer to SEMI E89-0999 "Guide For Measurement System Capability Analysis."*

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 45 nm node. Metrology needs after 2009 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect materials will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 115 presents the ten major challenges for metrology.

Table 115 Metrology Difficult Challenges

Five Difficult Challenges ≥45 nm/Through 2009	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species /energy /dosage (current), and wafer temperature during RTA.
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low-κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new, low-κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new, high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. High frequency dielectric constant measurements have shown a constant frequency response and are no longer a pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Five Difficult Challenges < 45 nm/Beyond 2009	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for Damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in die properties is becoming more difficult as device shrinks.
Statistical limits of sub-45 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions.	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

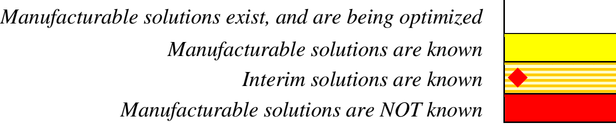
** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

METROLOGY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

Selected measurement requirements for metrology tools are listed in Tables 116–120. The microscopy resolution refers to the ability of a CD measurement tool to distinguish between lines that differ in width. The spatial resolution requirements for 2- and 3-dimensional (2D and 3D) dopant profiling are based on the requirements of Modeling & Simulation. Meeting 2D dopant profiling requirements will be difficult, and methods with slightly less spatial resolution may provide useful information. Measurement accuracy for all metrology requires appropriate reference materials.

Table 116a Metrology Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*	*MPU/ASIC*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	
Microscopy								
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	**0.40**	**0.33**	**0.29**	**0.25**	**0.22**	**0.20**	**0.18**	*MPU Gate*
Microscopy capable of measurement of patterned wafers having maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	**13**	**15**	**15**	**16**	**16**	**17**	**17**	*D1/2*
	120	**107!**	**95**	**85**	**76**	**67**	**60**	
Materials and Contamination Characterization								
Real particle detection limit (nm) [B]	**45**	**37**	**32**	**28**	**25**	**22**	**20**	*MPU*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**33**	**30**	**27**	**23**	**22**	**19**	**17**	*D1/2*
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	*MPU Gate*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	*MPU Gate*



Notes for Tables 116a and 116b:
[A] Metal and via aspect ratios are additive for dual-Damascene process flow.
[B] This value depends on surface microroughness and layer composition.
[C] The requirements for metal contamination have been changed based on less stringent requirements found in Front End Processes chapter Surface Preparation Technology Requirements table, Note F.

Table 116b Metrology Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*Driver*
Technology Node	*hp45*		*hp32*		*hp22*		
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*54*	*42*	*38*	*30*	*27*	*21*	
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*	
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*	
Microscopy							
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	**0.16**	**0.13**	**0.12**	**0.09**	**0.08**	**0.06**	
Microscopy capable of measurement of patterned wafers having maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	**>20** **50**	**>20** **35**	**>20** **30**	**>20** **25**	**>20** **21**	**>20** **18**	
Materials and Contamination Characterization							
Real particle detection limit (nm) [B]	**18**	**14**	**13**	**10**	**9**	**7**	
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**15**	**12**	**11**	**8**	**7**	**6**	
Specification limit of total surface contamination for critical COI surface materials (atoms/cm^2) [C]	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

MEASUREMENTS FOR PROCESSES FACING STATISTICAL LIMITS AND PHYSICAL STRUCTURES REACHING ATOMIC DIMENSIONS

As the dimensions of integrated circuit devices continue to shrink, the finite dimensions of the atoms within the structures will lead to statistical variations in critical dimensions and thus device properties. Furthermore, as dimensions of structures continue to shrink, the physical properties will deviate from the bulk properties because of quantum mechanical and mean free path effects. For instance, the lattice spacing of silicon atoms in a 35 nm gate represents about 1% of the gate length. The effects of statistical variations may be even more pronounced in gate dielectric structures composed of multi-layers of different components, each only several atoms thick. The engineering of such structures must take these statistical variations of dopant atoms and intrinsic defects and the quantum mechanical effects of confined structures into account to obtain sufficiently uniform device and circuit performance for large-scale integration.

Advances in interconnect technology are introducing conductor materials such as copper that must be excluded from the semiconductor itself and low-κ interconnect structures. Process and process modeling advances are required to deposit barrier layers of the order of only a few atomic layers that are pin hole-free. Metrology must be developed to ensure the integrity of barrier layers. As the conductor cross-section shrinks to the order of the mean free path of electrons, the bulk conductivity model no longer applies.

Several issues challenge measurement of transistor structures. Metrology of gate dielectric structures requires a practical standardized model of the quantum mechanical effects at the silicon—dielectric interface and gate—dielectric interface. Stochastic modeling strategies will be required to supplement deterministic (continuum) modeling techniques that have been used thus far. Significant advances in two- and three-dimensional dopant profiling metrology will be required to validate modeling. Mechanical stress changes the transport properties of transistors, and this can be either advantageous or detrimental. Metrology and modeling needs to be developed to manage stress effects.

These and other statistical variations in real materials and structures are independent of measurement uncertainties, and will add quadratically to the total uncertainty to the total uncertainty of the values of measured quantities. In addition, they must be taken into account in circuit and process design in ways that are not yet envisioned. It appears that the measurement uncertainties of a number of parameters specified for future device generations elsewhere in the Roadmap cannot be met for fundamental physical reasons having little to do with metrology *per se*.

MICROSCOPY

Microscopy is used in most of the core technology processes where two-dimensional distributions, i.e., digital images of the shape and appearance of integrated circuit (IC) features reveal important information. Usually, imaging is the first, but many times the only one step in the "being able to see it, measure it, and control it" chain. Microscopes typically employ light, electron beam, or scanned probe methods. Beyond imaging, online microscopy applications include critical dimension (CD) and overlay measurements along with detection, review and automatic classification of defects and particles. Because of the high value and quantity of wafers, the need for rapid, non-destructive, inline imaging and measurement is growing. Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies. Microscopy techniques and measurements based on them must serve the technologists better giving fast, detailed, adequate information on the processes in ways that help to establish process control in a more automated manner. Refer to the *supplemental material for more details on Microscopy*.

Electron Microscopy—There are many different microscopy methods that use electron beams as sources of illumination. These include scanning electron microscopy, transmission electron microscopy, scanning transmission electron microscopy, electron holography, and low-energy electron microscopy. Scanning electron microscopy and electron holography are discussed below, and transmission electron microscopy, scanning transmission electron microscopy, and low-energy electron microscopy are discussed in the section on Materials and Contamination Characterization.

Scanning Electron Microscopy (SEM)—continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 65 nm generation.[1] New inline SEM technology, such as the use of ultra-low-energy electron beams (< 250 eV) and high energy SEM may be required for overcoming image degradation due to charging, contamination, and radiation damage of the sample surface, while maintaining adequate resolution. Improving the resolution of the SEM by the reduction of spherical aberration leads to an unacceptably small depth of field and SEM imaging with several focus steps and/or use of algorithms that take the beam shape into account might be needed. Aberration correction lens technology has migrated from transmission electron microscopy to SEM providing a significant increase in capability. Other non-traditional SEM imaging techniques such as the implementation of nano-tips, and electron holography need to be developed, if they can prove to be production-worthy methodologies. A new alternative path could be high-pressure or environmental microscopy, which opens the possibility for higher accelerating voltage high-resolution imaging and metrology. Binary and phase-shifting chromium-on-quartz optical photomasks have been successfully investigated with this mode of high-resolution scanning electron microscopy. It has been found that the gaseous sample environment minimizes sample charging and contamination. This methodology also holds good potentials for the inspection, imaging and metrology of wafers.

To be able to make statistically sound SEM measurements it is essential to collect the right kind and right amount of information. The collection of more then needed information leads to loss of throughput, not enough or wrong type to loss of control. It is important to develop metrology methods that reveal and express the needed information with the indication of the validity of the measurements. Data analysis methods that adhere to the physics of the measurement and do use all information collected were demonstrated to be better than arbitrary methods. Measured and modeled image and fast and accurate comparative techniques are likely to gain importance in SEM dimensional metrology.

A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and the deposition of charge in gate structures, may set fundamental limits to the utility of all microscopies relying on charged particle beams.

Determination of the real 3D shape for sub-90 nm contacts/vias, transistor gates, interconnect lines or damascene trenches will require continuing advances in existing microscopy and sample preparation methods. Cross sectioning by FIB and lift-out for imaging in a TEM or a STEM has been successfully demonstrated.

Scanning probe microscopy (SPM)—may be used to calibrate CD-SEM measurements. Stylus microscopes offer 3D measurements that are insensitive to the material scanned. Flexing of the stylus degrades measurements, when the probe is too slender. The stylus shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High stiffness probe materials, such as short carbon nano-tubes, may alleviate this problem.

Far-field optical microscopy—is limited by the wavelength of light. Deep ultra-violet sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of defects is needed. Optical microscopes will continue to have application in the inspection of large features, such as solder bump arrays for multi-chip modules.

For *defect detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes. High-speed scanning has been demonstrated with arrayed SPMs, (that might be faster than SEMs) but issues associated with stylus lifetime, uniformity, characterization, and wear need to be addressed. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput and operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs.

LITHOGRAPHY METROLOGY

Lithography metrology continues to be challenged by rapid advancement of patterning technology. New materials in all process areas add to the challenges faced by Lithography Metrology. A proper control of the variation in transistor gate length starts with mask metrology. Although the overall features on a mask are four times larger than as printed, phase shift and optical proximity correction features are roughly half the size of the printed structures. Indeed, larger values for Mask Error Factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology have to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension (CD) and overlay are also becoming more challenging. CD control for transistor gate length continues to be a critical part of manufacturing IC's with increasing clock speeds. Acceleration of research and development activities for CD and overlay are essential if we are to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability.

Although a number of potential solutions for CD measurement exist, there is no unique technique that matches every measurement requirement. Often, special test structures are measured during manufacturing. When this is the case, active device dimension are not measured. CD-SEM continues to be used for wafer and mask measurement of lines and via/contact. A considerable effort has been aimed at overcoming electron beam damage to photoresist used by 193 nm exposures and that will continue when 157 nm exposure tools are introduced. Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects unless they are accurately modeled and corrected increase measurement variation and, therefore, total uncertainty of CD SEM measurements. Developments in electron beam source technology that improve resolution and precision are being tested. CD-SEM is facing an issue with poor depth of field unless a new approach to SEM based CD measurement is found. High-voltage CD-SEM and low loss detectors have been proposed as means of extending CD-SEM.[2] Scatterometry has moved into manufacturing, and does provide line shape metrology. Here, scatterometry refers to both single wavelength - multi angle optical scattering and to multi-wavelength - single angle methods. Recent advances have resulted in the ability to determine CD and line shape without the aid of a library of simulated results. Scatterometry has already been shown to provide a tighter distribution of key transistor electrical properties when used in an Advanced Process Control mode. The next step is the development of scatterometry for contact and via structures. Scatterometry models assume uniform optical property of line and background materials. Surface anomalies and non-uniform dopant distribution may affect scatterometry results. Therefore, scatterometry models need calibration and periodic verification. Litho and etch microloading effects may noticeably affect line CD. Since scatterometry makes measurements on special test structures, other CD metrology techniques (such as SEM or AFM) need to be employed to establish correlation between CD of the scatterometry structure and CDs of the circuit. Scatterometry needs to be capable of measuring smaller

[2] *A.C. Diebold and D. Joy. CD measurements for Future Technology Generations. Solid State Technology, June 2003.*

test structures while improving measurement precision. The use of "feed forward" control concepts must be extended to lithography metrology taking data from resist measurements and controlling subsequent processing, such as etch, to improve product performance. The use of overlay measurement equipment for CD control has also been reported. This method is based on the fact that the change in line width also affects the length of the photoresist lines that can then be measured using the optical microscope of the overlay system. A special test structure with arrays of line and arrays of spaces is required. CD-AFM measurements are an excellent means of verifying line shape and calibrating CD measurements. New probe tip technology and 3-D tiltable cantilever is required if CD-AFM is to be applied to dense line measurement below 90 nm node. Focus - Exposure correlation studies (especially for contact/via) can be done using all of the above methods as well as by the dual beam FIB (SEM plus focused ion beam) where there is an immediate correlation with line shape. Electron holography has been proposed as a long term CD measurement technology.

Line edge roughness (LER) is an important part of lithography process control. Line width roughness (LWR) is an important part of etch process control. The Lithography Roadmap provides metrics for both LER and LWR. In 2001, LWR requirements were listed as LER. LWR was included in the 2001 ITRS because it was correlated to an increase in transistor leakage current but not to changes in drive current.[3] It is important to note that the precision requirement for LER are several years ahead of those required for CD as indicated below. Although CD-SEM and lithography process simulation systems have software that determines LER, there is no standard method of determining line edge roughness. Thus standardized assessment of the status of LEW and LWR versus roadmap requirements is not possible.

Critical dimension measurement capability does not meet precision requirements that comprehend measurement variation from individual tool reproducibility, tool to tool matching and sample-to-sample measurement bias variation. Precision is defined by SEMI as a multiple of reproducibility. As indicated in the introduction, reproducibility includes repeatability, variation from reloading the wafer, and long-term drift. In practice, reproducibility is determined by repeated measurements on the same sample over an extended period of time. Although the precision requirements for CD measurement in the ITRS have always included the effects of line shape and materials variation, repeated measurements on the same sample would never detect measurement uncertainty related to sample-to-sample bias variation. Therefore, with the current methodology the uncertainty of measurement associated with variation of line shape, material, layout or any other parameter will not be included in the precision. Typically, reference materials for CD process control are specially selected optimum or "golden" wafers from each process level. Thus, industry practice is to determine measurement precision as a reproducibility of the measurement for each process level. The measurement bias is not detected. This approach misses measurement bias variation component of measurement uncertainty. In light of this, a new metric, total measurement uncertainty, (TMU), has been proposed. The components of total uncertainty need to be properly assessed for every metrology tool. This would allow meaningful comparisons and improved tool matching. Total measurement variation defines a new precision-like variable P(TMU). P(TMU) would be determined using a technology representative set of samples that accounts for variations in measurement bias associated with each process level. One way to reduce TMU is to correct CD measurement bias at each process level.

Calibration of in-line CD metrology equipment requires careful implementation of the calibration measurement equipment. For example, laboratory based, cross-sectional SEM or CD-AFM must have precision that matches or exceeds in-line CD and have to be frequently calibrated. Reference materials used during manufacturing must be representative to the actual process level and structure. Due to the importance of maintaining control of transistor gate length as well as other structures, different metrology systems may be selected for transistor gate control. Reports of this approach already exist.

CD measurement has been extended to line shape control. Tilt beam CD-SEM, comparison of line scan intensity variation versus line scans from a golden wafer, scatterometry, CD-AFM, and the dual beam FIB (electron and ion beam systems) have all been applied to line shape measurement. Sidewall angle has been proposed as the key process variable. Already, photoresist lines have shapes that are not well described by a single planar description of the sidewall. Line edge and line width roughness along a line, vertical line edge roughness, and rounded top shapes are important considerations in process control. As mentioned above, precision values change with each process level. This adds to the difficulty in determination of etch bias (the difference in CD before and after etch). Electrical CD measurements provide a monitoring of gate and interconnect line width, but only after the point where reworking the wafers is no longer possible and does not allow a real-time correction of process parameter.

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[3] *K. Patterson, J.L. Sturtevant, J. Alvis, N. Benavides, D. Bonser, N. Cave, C. Nelson-Thomas, B. Taylor, K. Turnquest, Experimental Determination of the Impact of Polysilicon LER on sub-100 nm Transistor Performance, In Metrology, Inspection, and Process Control for Microlithography XV, SPIE Vol 4344, 2001, pp 809–814.*

Mask Metrology is moving beyond the present optical technology. Binary and phase-shifting chromium on quartz optical photomasks have been successfully investigated with high-pressure/environmental scanning electron microscopy. The successful application of this methodology to semiconductor photomask metrology is new because of the recent availability of a high-pressure SEM instrumentation equipped with high-resolution, high-signal, field emission technology in conjunction with large chamber and sample transfer capabilities. The high-pressure SEM methodology employs a gaseous environment to help to compensate for the charge build-up that occurs under irradiation with the electron beam. Although potentially very desirable for the charge neutralization, this methodology has not been seriously employed in photomask or wafer metrology until now. This is a new application of this technology to this area, and it shows great promise in the inspection, imaging and metrology of photomasks in a charge-free operational mode. This methodology also holds the potential of similar implications for wafer metrology. For accurate metrology, high-pressure SEM methodology also affords a path that minimizes, if not eliminates, the need for charge modeling.

Lithography metrology consists not only of overlay and CD metrology (essentially microscopy to measure width, depth, and shape of printed features after completion of the lithography step), but also includes the process control and characterization of materials needed for lithography process, especially photoresists, phase shifters, and antireflective coatings (ARCs). As these lithography materials become more complex, the materials characterization associated with them also increases in difficulty. Additionally, most (non-lithography) materials used in the wafer fabrication process (gate oxides, metals, low-κ dielectrics, SOI substrates, etc) enter the lithography process indirectly, since their optical properties affect the reflection of light at a given wavelength. Even a small variation in process conditions for a layer not normally considered critical to the lithography process (e.g. the thickness of the buried oxide in SOI wafers) can change the dimensions or shapes of the printed feature, if this process change affected the optical response of the layer.

As a minimum, the complex refractive index (refractive index n and extinction coefficient κ) of all layers needs to be known at the lithography wavelength. Literature data for such properties are usually not available or obsolete and not reliable (derived from obsolete reflectance measurements on materials of unknown quality followed by Kramers-Kronig transform). In ideal cases, n and κ can be measured inline using spectroscopic ellipsometry at the exposure wavelength. Especially below 157 nm, such measurements are very difficult and usually performed outside of the fab by engineering personnel. EUV optical properties can only be determined using specialized light sources (such as a synchrotron). Therefore, materials composition is often used as a figure of merit, when direct measurement of the optical properties is not practical. But even two materials with the same composition can have different optical properties (take amorphous and crystalline Si as an example).

Additional complications in the determination of the optical properties of a material arise from surface roughness, interfacial layers, birefringence or optical anisotropy (often seen in photoresists or other organic layers responding to stress), or depth-dependent composition. For some materials for a wafer fab, it is impossible to determine the optical properties of such material, since the inverse problem of fitting the optical constants from the ellipsometric angles is underdetermined. Therefore, physical materials characterization must accompany the determination of optical properties, since physical characteristics, materials properties, and optical constants are all inter-related.

Overlay measurements are challenged by phase shift and optical proximity correction masks, and the use of different exposure tools for metal trench and via will compound the difficulty.

Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with scanning probe microscopy (SPM). The need for new target structures has been suggested as a means of overcoming the issues associated with phase shift mask and optical proximity mask alignment errors not detectable with traditional targets. Overlay for on-chip interconnect will continue to be challenging. The use of chemical mechanical polishing for planarization degrades target structures. Thus as requirements for tighter overlay control are introduced, the line edge of overlay targets in interconnect are roughened. The low-κ materials used as insulators will continue to make overlay more difficult especially as porous low κ move into manufacturing.

The Lithography Metrology Requirements Tables are divided into wafer and mask requirements. The mask metrology requirements are further divided into the needs for each type of exposure technology: optical, EUV, and electron projection .

Table 117a Lithography Wafer Metrology Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Printed gate CD control (nm) Uniformity (variance) is 10% of CD Allowed lithography variance = 4/5 total variance of physical gate length [A]*	◆ 4.0	3.3	2.9	2.5	2.2	2.0	1.8
Wafer dense line CD control (nm) * Uniformity is 15% of CD Allowed lithography variance = 2/3 total variance	12.2	11.0	9.8	8.6	8.0	7.0	6.1
Wafer minimum contact hole (nm, post etch) from lithography tables	115	100	90	80	70	65	55
Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	14.1	12.2	11.0	9.8	8.6	8.0	6.7
Line width roughness (nm, 3 σ) <8% of CD ***	◆ 3.6	3.0	2.6	2.2	2.0	1.8	1.6
Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.8	◆ 0.7	0.6	0.5	0.4	0.4	0.4
Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	2.4	2.2	2.0	1.7	1.6	1.4	1.2
Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)	2.8	2.4	2.2	2.0	1.7	1.6	1.3
Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.72	0.592	0.512	0.4	0.4	0.352	0.32
Maximum CD measurement bias (%) [B]	10	10	10	10	10	10	10
Wafer overlay control (nm)	35	32	28	25	23	21	19
Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	3.5	3.2	2.8	2.5	2.3	2.1	1.9

** All precision values are 3 Sigma in nm and include metrology tool-to-tool matching.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology node. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

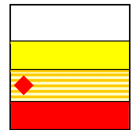
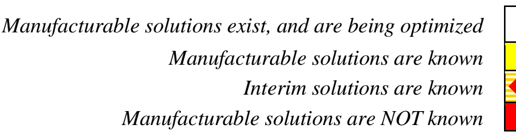


Table 117b Lithography Metrology Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*54*	*42*	*38*	*30*	*27*	*21*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Printed gate CD control (nm) Uniformity (variance) is 10% of CD Allowed lithography variance = 4/5 total variance of physical gate length [A] *	1.6	1.3	1.2	0.9	0.8	0.6
Wafer dense line CD control (nm) * Uniformity is 15% of CD Allowed lithography variance = 2/3 total variance	5.5	4.3	3.9	3.1	2.7	2.2
Wafer minimum contact hole (nm, post etch) from lithography tables	50	35	30	25	21	18
Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	6.1	4.3	3.7	3.1	2.6	2.2
Line width roughness (nm, 3 σ) <8% of CD ***	1.4	1.1	1.0	0.8	0.7	0.6
Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.3	0.3	0.2	0.2	0.2	0.1
Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	1.1	0.9	0.8	0.6	0.5	0.4
Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)	1.2	0.9	0.7	0.6	0.5	0.4
Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.288	0.224	0.208	0.16	0.144	0.112
Maximum CD measurement bias (%) [B]	10	10	10	10	10	10
Wafer overlay control (nm)	18	14	12.8	10	8.8	7.2
Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	1.8	1.4	1.3	1.0	0.9	0.7

** All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology node. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.



Notes for Tables 117a and 117b:
[A] The orange designation for CD measurement for isolated lines in the near term is a result of roadmap process range and need for tool matching in the precision requirement also makes this requirement very difficult to achieve. A work around for isolated line CD measurement is to use a single tool and avoid tool matching. Long term, CD measurement for 25 nm linewidths requires a technology breakthrough because extension of known methods may not be possible.

Table 118a Lithography Metrology (Mask) Technology Requirements: Optical—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Printed gate CD control (nm) allowed lithography variance = 4/5 total variance of physical gate length [A] *	◆ 4.0	3.3	2.9	2.5	2.2	2.0	1.8
Wafer overlay control (nm)	35	32	28	25	23	21	19
Wafer minimum contact hole (nm, post etch) from lithography tables	115	100	90	80	70	65	55
Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	14.1	12.2	11.0	9.8	8.6	8.0	6.7
Mask nominal image size (nm) [B]	260	212	180	160	140	128	112
Mask minimum primary feature size [C]	182	148.4	126	112	98	89.6	78.4
Optical Section							
Minimum OPC size (opaque at 4×, nm) [D]	130	106	90	80	70	64	56
Image placement (multipoint at 4×, nm)	21	19	17	15	14	13	12
CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Mask error factor (MEF) from lithography tables isolated lines, binary	1.4	1.4	1.4	1.4	1.6	1.6	1.6
MEF isolated lines, alternating phase shift [G]	1	1	1	1	1	1	1
MEF dense lines [G]	2	2	2	2	2.5	3	3
MEF contacts [G]	3	3	3	3	3.5	4	4
CD Uniformity (3 Sigma at 4×, nm) Refer to Lithography Chapter Table for Optical Mask Requirements							
Isolated lines (MPU gates), binary Uniformity is 10% of CD [E], [F]	4.6	3.8	3.3	2.9	2.2	2.0	1.8
Isolated lines (MPU gates), alternated Uniformity is 10% of CD [E], [G]	6.4	5.3	4.6	4.0	3.6	3.1	2.9
Dense lines (DRAM half-pitch) Uniformity is 15% of CD [E], [H]	9.8	8.8	7.8	6.9	5.1	3.7	3.3
Wafer minimum contact hole (nm, post etch) from lithography tables	115	100	90	80	70	65	55
Mask contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	5.0	4.4	3.9	3.5	2.6	2.1	1.8
Mask image placement metrology (precision, P/T=0.1)	2.1	1.9	1.7	1.5	1.4	1.3	1.2
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, binary**)	◆ 0.9	0.8	0.7	0.6	0.4	0.4	0.4
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, alternated**)	◆ 1.3	◆ 1.1	0.9	0.8	0.7	0.6	0.6
Mask CD metrology tool precision* (P/T=0.2 for dense lines**)	◆ 2.0	◆ 1.8	◆ 1.6	◆ 1.4	1.0	0.7	0.7
Mask CD metrology tool precision* (P/T=0.2 for contact/vias**)	◆ 1.0	◆ 0.9	0.8	0.7	0.5	0.4	0.4
Specific Requirements							
Alternated PSM phase mean deviation	2	2	2	1	1	1	1
Phase metrology precision, P/T=0.2	0.4	0.4	0.4	0.2	0.2	0.2	0.2
Alternated PSM phase uniformity (±degrees)	2	2	2	1	1	1	1
Phase uniformity metrology precision, P/T=0.2	0.4	0.4	0.4	0.2	0.2	0.2	0.2

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

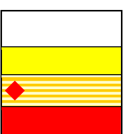


Table 118b Lithography Metrology (Mask) Technology Requirements: EUV—Near and Long-term

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*67*	*60*	*54*	*42*	*38*	*30*	*27*	*21*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
EUV								
Image placement error (nm, multipoint)	13	12	11	9	8	7	6	6
CD Uniformity (3 sigma at 4×, nm)								
Isolated lines (MPU gates) Uniformity is 10% of CD Mask error factor varies with year	3.0	2.5	2.0	1.5	1.3	0.7	0.5	0.4
Dense lines (DRAM half-pitch) Uniformity is 15% of CD Mask error factor varies with year	12.5	11.0	9.0	6.5	5.5	2.0	1.5	1.0
Wafer minimum contact hole (nm, post etch) from lithography tables	65	55	50	35	30	25	21	18
Contact/Vias Uniformity is 10% of CD mask error factor varies with year	8	7	6.5	4.5	3.5	2.5	2	1.5
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**	0.6	0.5	0.4	0.3	0.3	0.1	0.1	0.1
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**	2.5	2.2	1.8	1.3	1.1	0.4	0.3	0.2
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**	1.6	1.4	1.3	0.9	0.7	0.5	0.4	0.3
Specific Requirements								
Mean peak reflectivity	65%	66%	66%	67%	67%	67%	67%	67%
Peak reflectivity uniformity (3 sigma %)	0.58%	0.56%	0.54%	0.48%	0.42%	0.36%	0.30%	0.24%
Absorber sidewall angle tolerance (degrees)	1	1	0.75	0.62	0.5	0.5	0.5	0.5
Absorber LER (3 sigma, nm)	4.5	4	3.5	3	3	3	2	2
Mask substrate flatness (peak-to-valley, nm)	◆ 60	◆ 55	50	40	35	25	25	20
Metrology mean peak reflectivity precision (P/T=0.2, %)	1.30%	1.30%	1.30%	1.30%	1.30%	1.30%	1.30%	1.30%
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)	0.12%	0.11%	0.11%	0.10%	0.08%	0.07%	0.06%	0.05%
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)	0.2	0.2	0.15	0.124	0.1	0.1	0.1	0.1
Absorber LER metrology precision (3 sigma, P/T=0.2)	0.9	0.8	0.7	0.6	0.6	0.6	0.4	0.4
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)	12	11	10	8	7	5	5	4

**All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
***Measurement tool performance needs to be independent of target shape, material, and density.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Notes for Table 118 a, 118b, and 118c:

[A] The designation for CD measurement for isolated lines in the near term is a result of roadmap process range and the need for tool matching in the precision requirement makes this requirement very difficult to achieve. A work-around for isolated line CD measurement is to use a single tool and avoid tool matching. Long term, CD measurement for 25 nm linewidths requires a technology breakthrough because extension of known methods may not be possible.

[B] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio that equals 4×.

[C] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.

[D] Mask OPC Feature size—Minimum width of the smallest non-printing features on the mask.

[E] The CD process range for isolated gate lithography is 4/5 of the total CD process range of 1/10 the CD at 3σ.

The CD process range is 4/5 of the 15% of CD for dense lines and 2/3 the 15% for contact/via. Process ranges are variances. It is important to note that the mask part of the lithography process range is allowed 40% of the total lithography process range. The mask error factor (MEF) reduces the CD process range, and its effect is calculated by dividing the process range by the MEF.

[F] The mask error factor for isolated lines on a binary mask changes from 1.4 to 1.6 at the 65 nm node.

[G] The mask error factor for alternating phase shift masks is 1.

[H] The mask error factor for dense lines is 2 from the 100 to the 70 nm node. It is 2.5 at the 65 nm node, and is 3 for the 57 and 50 nm node.

[I] The mask error factor for contact and via lines is 3 from the 100 to the 70 nm node. It is 3.5 at the 65 nm node, and is 4 for the 57 and 50 nm node.

Table 118c Lithography Metrology (Mask) Technology Requirements: EPL—Near and long-term

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*67*	*60*	*54*	*42*	*38*	*30*	*27*	*21*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
Wafer gate CD control*	**2.0**	**1.8**	**1.6**	**1.3**	**1.2**	**0.9**	**0.8**	**0.6**
Wafer overlay control*	**22**	**20**	**16**		**11**		**10**	
EPL								
Minimum stitching feature size (nm)	**TBD**	**TBD**	**56**	**TBD**	**40**	**TBD**	**30**	**TBD**
Image placement error in sub-field (nm, multipoint)	**8**	**7.5**	**6.5**	**5.5**	**5.4**	**4**	**3.5**	**3**
Complementary mask pair placement error (nm, multipoint) for stencil mask	**TBD**	**TBD**	**10**	**TBD**	**7**	**TBD**	**5**	**TBD**
Metrology stitching precision (3 sigma, P/T=0.1)	**TBD**	**TBD**	**5.6**	**TBD**	**4**	**TBD**	**3**	**TBD**
Mask image placement metrology precision (3 sigma, P/T = 0.1)	**TBD**	**TBD**	**1.1**	**TBD**	**0.8**	**TBD**	**0.6**	**TBD**
Complementary mask pair metrology precision (3 sigma, P/T = 0.1)	**TBD**	**TBD**	**1**	**TBD**	**0.7**	**TBD**	**0.5**	**TBD**
CD Uniformity (3 sigma at 4× nm)								
Isolated lines (MPU gates) Uniformity is 10% of CD	**3.1**	**2.9**	**2.6**	**2.0**	**1.9**	**1.4**	**1.3**	**1.0**
Dense lines (DRAM half-pitch) Uniformity is 15% of CD	**11.2**	**9.8**	**8.8**	**6.9**	**6.3**	**4.9**	**4.3**	**3.5**
Wafer minimum contact hole (nm, post etch) from lithography tables	**65**	**55**	**50**	**35**	**30**	**25**	**21**	**18**
Contact/Vias Uniformity is 15% of CD mask error factor is 1	**12.7**	**10.8**	**9.8**	**6.9**	**5.9**	**4.9**	**4.1**	**3.5**
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**	**0.6**	**0.6**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.2**
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**	**2.2**	**2.0**	**1.8**	**1.4**	**1.3**	**1.0**	**0.9**	**0.7**
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**	**2.2**	**2.0**	**1.8**	**1.4**	**1.3**	**1.0**	**0.9**	**0.7**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

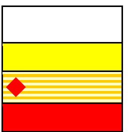
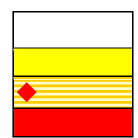


Table 118c Lithography Metrology (Mask) Technology Requirements: EPL—Near and long-term (continued)

Year of Production	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node			*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*67*	*60*	*54*	*42*	*38*	*30*	*27*	*21*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*57*	*50*	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*32*	*28*	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*22*	*20*	*18*	*14*	*13*	*10*	*9*	*7*
Specific requirements								
Clear area transmission uniformity (3 sigma %) for membrane	**TBD**	**TBD**	**0.70%**	**TBD**	**0.60%**	**TBD**	**0.05%**	**TBD**
Energy loss (delta E/E) (%) for membrane	**TBD**	**TBD**	**0.07%**	**TBD**	**0.05%**	**TBD**	**0.04%**	**TBD**
Scatterer sidewall angle tolerance (degrees)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Scatterer/stencil LER (3 sigma, nm)	**TBD**	**TBD**	**3**	**TBD**	**2**	**TBD**	**1.5**	**TBD**
Metrology transmission uniformity precision (P/T=0.2, %)	**TBD**	**TBD**	**0.07%**	**TBD**	**0.06%**	**TBD**	**0.05%**	**TBD**
Energy loss metrology precision (3 sigma, P/T = 0.1)	**TBD**	**TBD**	**0.01%**	**TBD**	**0.01%**	**TBD**	**0.00%**	**TBD**
Sidewall angle metrology precision (3 sigma, P/T = 0.2)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
LER metrology precision (3 sigma, P/T=0.2)	**TBD**	**TBD**	**0.6**	**TBD**	**0.4**	**TBD**	**0.3**	**TBD**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



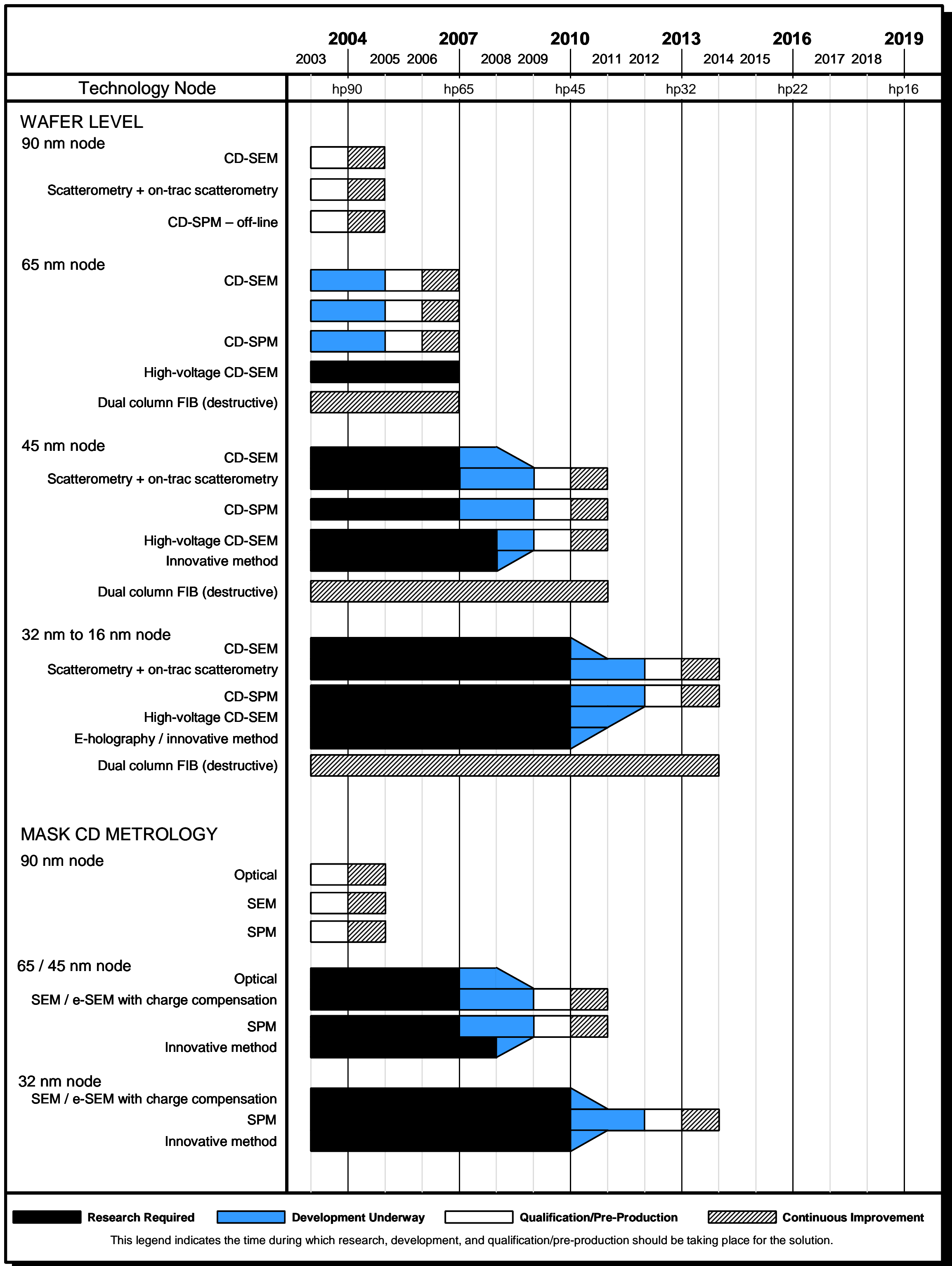


Figure 81 Lithography Metrology—CD Measurement Potential Solutions

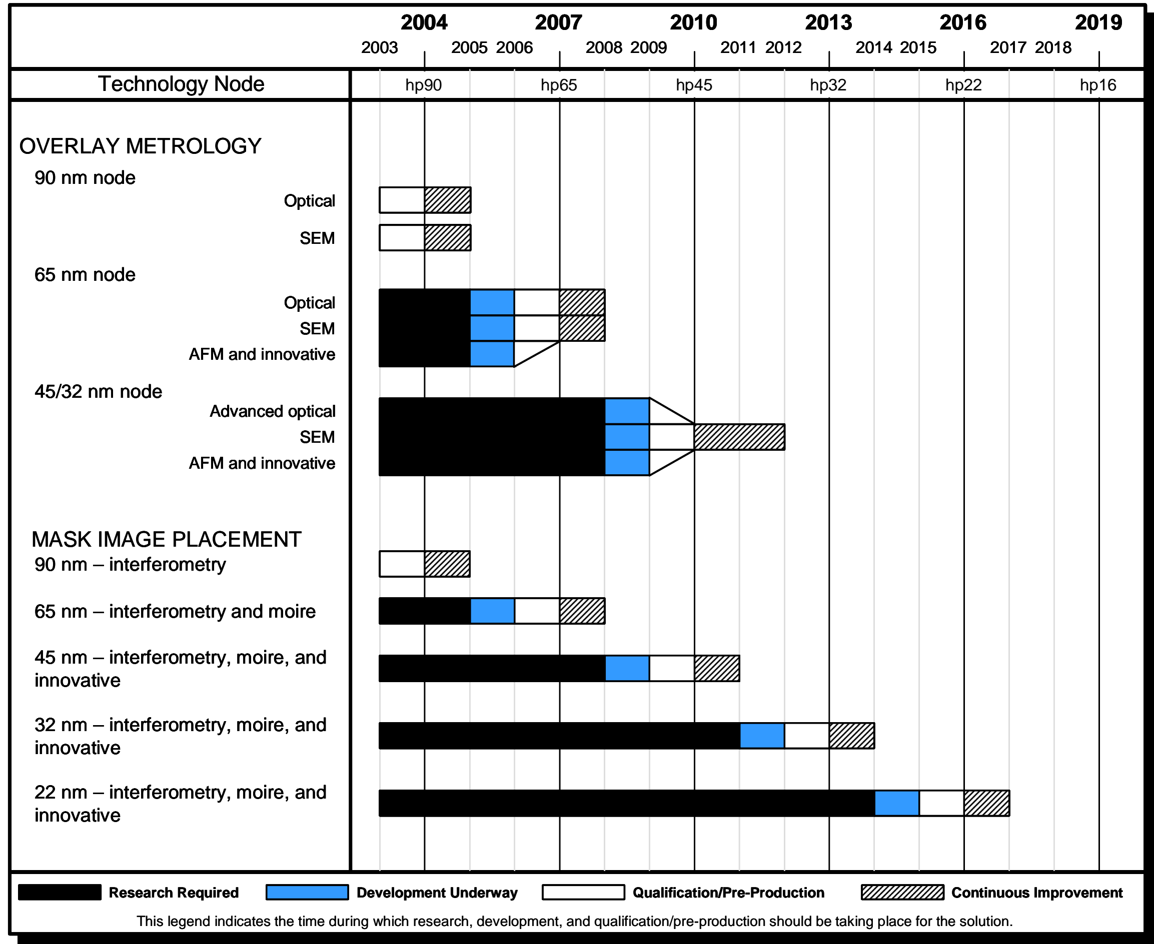


Figure 82 Lithography Metrology—Overlay Potential Solutions

FRONT END PROCESSES METROLOGY

The accelerated introduction of new technology generations requires accelerated advancements of metrology for transistor development and fabrication. In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front-end plasma etch technologies are covered. Process integration issues such as the need to control leakage current and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Metrology requirements for Front End Processes are shown in Table 119, and the Potential Solutions are shown in Figure 83

Table 119a Front End Processes Metrology Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*	
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	$<1\times10^{10}$	$<1\times10^{10}$	$<1\times10^{10}$	$<1\times10^{10}$	$<1\times10^{10}$	$<1\times10^{10}$	$<1\times10^{10}$	
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	$<1\times10^{9}$	$<1\times10^{9}$	$<1\times10^{9}$	$<1\times10^{9}$	$<1\times10^{9}$	$<1\times10^{9}$	$<1\times10^{9}$	
High-performance logic EOT equivalent oxide thickness (EOT) nm	**1.3**	**1.2**	**1.1**	**1**	**0.9**	**0.8**	**0.7**	
Low-operating power logic EOT	**2.2**	**2.1**	**2**	**1.9**	**1.8**	**1.7**	**1.6**	
± 3σ dielectric process range (EOT) (nm)	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	
EOT measurement precision 3σ (nm) [B]	**0.0052**	**0.0048**	**0.0044**	**0.004**	**0.0036**	**0.0032**	**0.0028**	*MPU high-performance*
DRAM stacked capacitor structure	**Cylinder**	**Cylinder**	**Cylinder/ Pedestal**	**Cylinder/ Pedestal**	**Pedestal**	**Pedestal**	**Pedestal**	
DRAM stacked capacitor electrodes	**MIS**	**MIS/MIM**	**MIM**	**MIM**	**MIM**	**MIM**	**MIM**	
DRAM stacked capacitor dielectric material	Ta_2O_5/ Al_2O_5	Ta_2O_5/ Al_2O_5	Ta_2O_5/ Al_2O_5	Ta_2O_5/ Al_2O_5 others	Ta_2O_5/ Al_2O_5 others	Ta_2O_5/ Al_2O_5 others	Ta_2O_5/ Al_2O_5 others	
DRAM stacked capacitor dielectric constant	**22**	**22**	**40**	**50**	**50**	**50**	**50**	

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

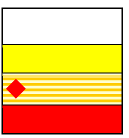
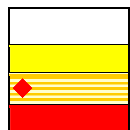


Table 119a Front End Processes Metrology Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*	
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	
Equivalent oxide thickness (EOT) (nm) for stacked capacitor	**3.5**	**2.3**	**1.8**	**1.4**	**0.8**	**0.8**	**0.8**	
DRAM stacked capacitor dielectric physical thickness (nm)	**19.3**	**12.7**	**18.0**	**17.5**	**10**	**10**	**10**	
± 3 σ process range	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	**±4%**	
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	**0.077**	**0.051**	**0.072**	**0.070**	**0.040**	**0.040**	**0.040**	
Dopant concentration [channel maximum] (atoms/cm³) for V_t = 0.4	**1.5–2.5E18**	**1.5–2.5E18**	**1.5–2.5E18**	**2.0–4.0E18**	**2.5–5.0E18**	**NA New Device on FD SOI**	**NA New Device on FD SOI**	
Dopant atom	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	**P, As, B**	
Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008	**19**	**15**	**13**	**12**	**10**	**22**	**20**	
Lateral steepness of dopant profile (nm/decade)	**5**	**4.1**	**3.5**	**3.1**	**2.8**	**na**	**na**	
Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	**5**	**4.1**	**3.5**	**3.1**	**2.8**	**2.8**	**2.8**	
At-line dopant concentration precision (across concentration range) [D]	**4%**	**4%**	**4%**	**4%**	**4%**	**4%**	**4%**	

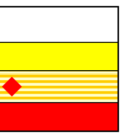


Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 119b Front End Processes Metrology Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	<1×10^{10}	<1×10^{10}	<1×10^{10}	<1×10^{10}	<1×10^{10}	<1×10^{10}
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	<1×10^9	<1×10^9	<1×10^9	<1×10^9	<1×10^9	<1×10^9
High- performance logic EOT [A] equivalent oxide thickness (EOT) nm	TBD	0.7	TBD	0.6	TBD	0.5
Low-operating power logic EOT	TBD	TBD	TBD	TBD	TBD	TBD
± 3σ process range (EOT) (nm)	±4%	±4%	±4%	±4%	±4%	±4%
Logic dielectric measurement precision 3σ (nm) [B]	0	0.0028	0	0.0024	0	0.002
DRAM stacked capacitor structure dielectric material process control requirements	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
(Dielectric constant)	50	60	60	80	80	100
Equivalent oxide thickness (nm) stacked capacitor	0.7	0.6	0.5	0.4	0.4	0.25
DRAM stacked capacitor dielectric physical thickness (nm) ±3σ process range [C]	8.8	9.0	7.5	8.0	8.0	6.3
	±4%	±4%	±4%	±4%	±4%	±4%
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.035	0.036	0.03	0.032	0.032	0.025
Dopant concentration [channel maximum] (atoms/cm^3)	NA New Device on FD SOI	NA New Device on FD SOI	NA New Device on FD SOI	NA New Device on FD SOI	NA New Device on FD SOI	NA New Device on FD SOI
Dopant atom	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B
Metrology for junction depth [based on drain extension] (nm)	18	14	13	10	9	7
Lateral Steepness of dopant profile (nm/decade)	TBD	TBD	TBD	TBD	TBD	TBD
Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	2.8	2.8	2.8	2.8	2.8	2.8
At-line dopant profile concentration precision (across concentration range) [E]	2%	2%	2%	2%	2%	2%

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 119a and 119 b:

[A] The use of SOI wafers requires metrology development.

[B] Precision calculated from P/T=0.1=6× precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as Ta_2O_5 will be used at and after the 70 nm logic node and possibly at the 100 nm node. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\varepsilon_{high-\kappa}/\varepsilon_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick Ta_2O_5 (κ= ~25) layer has a 1 nm equivalent oxide (κ=3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.

[C] In the case of MIS structure, physical thickness, t_{diel} , is calculated using the equation of $t_{diel}=(t_{eq.ox}-1\ nm)_{diel}\ \varepsilon_{high-\kappa}/3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, t_{diel} is calculated using the equation of $t_{diel}= t_{eq.ox}\ \varepsilon_{high-\kappa}/3.9$. Here $t_{eq.ox}$ is equivalent oxide thickness, and t_{diel} is dielectric constant of the dielectric material.
[D] High- precision measurements with low systematic error are required.

Starting materials —Many of the metrology challenges related to starting materials involve the emerging class of layered materials such as SOI, Strained Silicon and combinations of these technologies. The trend toward thinner layers, along with multiple layer interfaces pose a challenge to most material metrology techniques.

Areas of concern include the following:

- Bulk Ni and Cu measurement on p+, SOI, SSi and SSOI wafers
- Measurement of 10^9–10^{10} cm^{-3} Fe (and other bulk metals) in the top Si of thin SOI wafers
- Measurement variability of nitrogen concentrations < 1×10^{14} cm^{-3} in nitrogen-doped epi and annealed wafers
- Thickness and uniformity of very thin SOI layers (<20 nm)
- Defectivity of thin layers (e.g., threading dislocations, "HF defects")
- Particle detection (<100 nm) on layered surfaces

Metrology requirements for Nanotopography (nanometer-scale surface height variation over a 2–20 mm length scale) are still emerging. Small particle detection (<50 nm) continues to be of concern for the future. Note that the silicon starting materials particle requirements below 90 nm size will not use sub-90 nm metrology but will model the sub-90 nm particle requirement based upon 90 nm particle detection. More information can be found in the Starting Materials section of the FEP Roadmap.

Silicon-On-Insulator (SOI) is entering the mainstream of IC device applications, and this is expected to grow further along the Roadmap. An expectation has been that the materials specifications for polished silicon substrates would be transferred to SOI specifications. However, the underlying insulator structure in SOI negatively affects many of the metrology capabilities used for polished silicon substrates. Thus, there is an inability to measure and control SOI material properties at the level desired. This leads to a major challenge for SOI metrology, one that the metrology community must address soon. For more details on these metrology challenges see the FEP section on Starting Materials.

The use of strained silicon without SOI has emerged as potential solution for channel mobility enhancement at an early date than foreseen in the 2001 roadmap. Metrology issues for strained silicon are discussed in the Materials Characterization Section of the Metrology chapter.

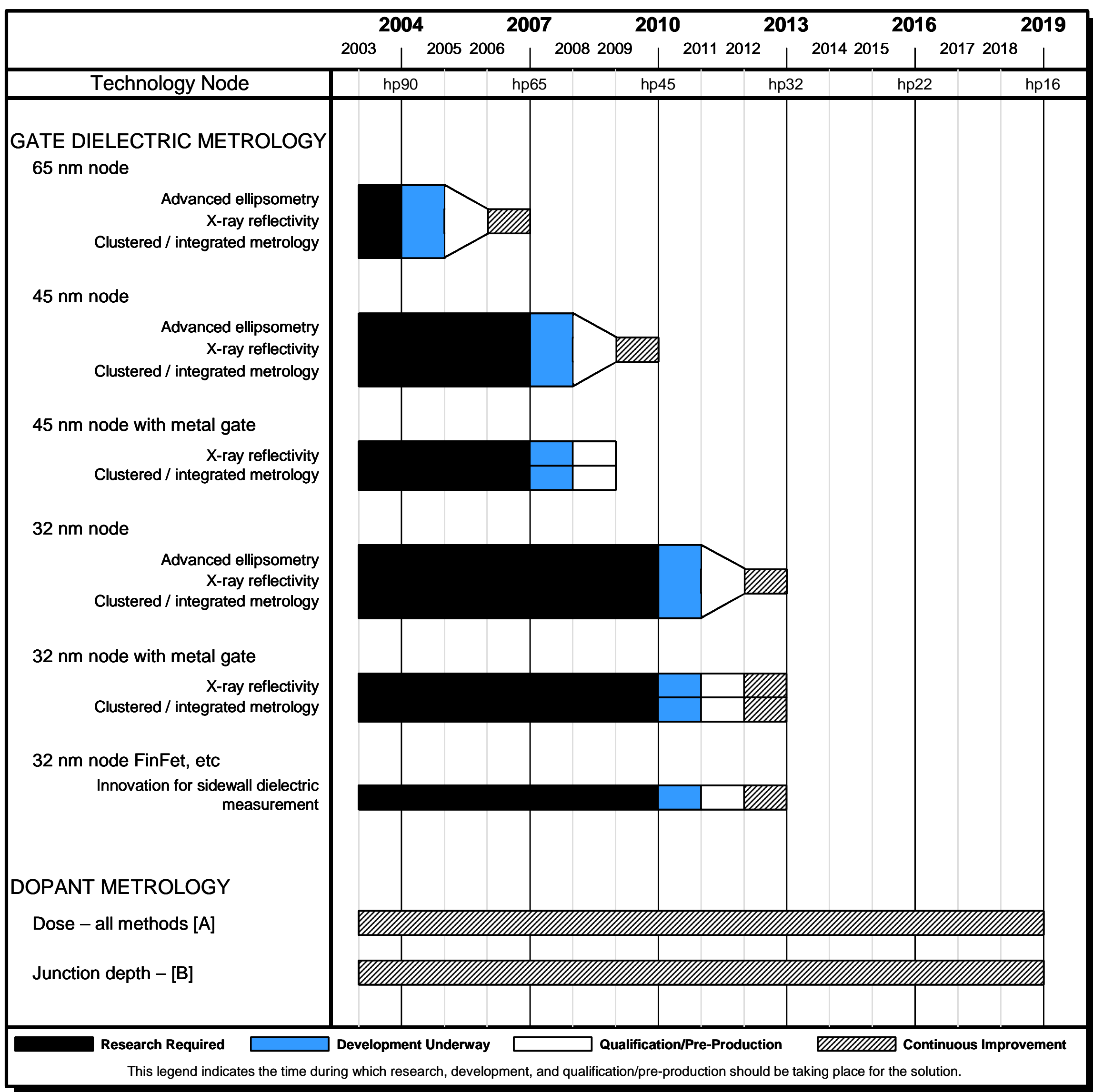
Surface preparation—*In situ* sensors for particles, chemical composition, and possibly for trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Yield Enhancement* chapter. Particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter. The role of impurities in high-κ gate dielectrics, and therefore their measurement requirements, is a future research topic.

Thermal/thin films—The transition from silicon oxynitride to alternate materials with higher dielectric constants remains a key metrology challenge. Development of metrology for high-κ materials needs to continue and metrology for the interface layer remains a difficult challenge. The FEP roadmap shows the first use of high κ in both low-power and high-performance devices in 2005. Potential solutions that enable interfacial control include in-line optical metrology that extends either into the infra-red and/or the ultra-violet wavelength range. Continued development and standardization of electrical testing at high frequencies and new methods for dielectric reliability testing are required. Higher κ electrical testing by traditional capacitor and transistor structures, Hg-probe type capacitor testing, and non-contact, corona discharge methods are all under development. There is considerable evidence that the dielectric properties of transistor and capacitor dielectric films after deposition are different from those subsequent to thermal processing, and this complicates comparison of electrical and physical methods. Correlation must improve. Application of materials characterization methods such as scanning transmission electron microscopy and X-ray reflectivity to higher κ materials as well as methods for controlling Ge in SiGe channels are discussed in the *Materials and Contamination Characterization section* of this Metrology chapter.

Metrology must be further developed for controlling gate electrode processes. Examples of new gate electrode processes and thickness include multiple thickness for poly silicon gate. The control of the thickness and work function of metal gate electrodes is a new metrology need.

FERAM—Although the thickness of the dielectric films are 100 to 200 nm, optical models for in-line film thickness measurement of the metal oxides must be developed when a new materials set is used. The main metrology need is for fatigue testing of the capacitor structures at 10^{16} read write cycles and above.

Doping technology—Improved inline process measurements to control active dopant implants is required beyond 90 nm. Presently, 4-point probe measurement is used for high dose implant and thermally modulated optical reflectance is used for low-dose implant process control. Both methods require improvement, and a new technique that provides direct *in situ* measurement of dose, dopant profile, and dose uniformity would allow real-time control. New methods for control of B, P, and As implants are also needed, and an in-line electron microprobe system optimized for B, P, and As X-ray fluorescence based dose measurement has recently been introduced. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of new, non-destructive measurement methods such as carrier illumination (an optical technology) are under evaluation. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology.



[A] in-line: four-point probe, TMOR, e-beam+XRF, carrier illumination; off-line: SIMS, and innovative methods
[B] carrier illumination, off-line SIMS, and innovative methods

Figure 83 Front End Processes Metrology Potential Solution

INTERCONNECT METROLOGY

The industry now has experience manufacturing Cu/low-κ Damascene interconnects. This experience provides important guidance on what process parameters to control as well as an indication of which measurements are mainly used in research and development instead of during volume manufacturing. We now know that the reliability of copper metal connection is degraded by the effects of electro and stress migration. Initial experience with the change from 180 nm to 130 nm technology showed that reliability issues with metal vias and copper lines could be solved by altering process conditions to change film stress and other parameters. Voids in metal lines and vias can either be present after deposition / CMP / anneal or form from agglomeration of micro-voids due to electro or stress migration. Recent efforts to understand electro and stress migration point to the impact of the shape of metal structures and the stress of the low-κ films.

Advances in measurement technology have enabled *in situ* control of Chemical Mechanical Polishing (CMP) and determination of the thickness of buried barrier films on horizontal surfaces. The pose size distribution of porous low κ can be measured using small angle X-ray scattering or ellipsometric porisimetry. Although voids can be detected in fields of copper lines, most methods determine a change in the volume of copper lines. Thus, process induced changes such as those that occur across the wafer from CMP can mask the presence of voids. Metrology for in-line control of bath chemistry is being implemented.

Some measurements remain elusive. For example, measurement of barrier and seed copper film thickness on sidewalls is not yet possible. Recently crystallographic texture measurements on sidewalls have been reported. Adhesion strength measurements are still done using destructive methods. End point detection for etch must be developed for new etch stop materials for porous low κ. Detection of killer pores and voids is not yet possible.

The accelerated reduction in feature size makes development of metrology for high aspect ratio features a greater challenge for on-chip interconnect development and manufacture. Critical dimension measurements are also a key enabler for development of interconnect processes. CD metrology must be extended to very high aspect ratio structures made from porous dielectric materials and requires 3D information for trench and via/contact sidewalls. These measurements will be further complicated by the underlying multi film complexity.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline measurements for interconnect structures are made on simplified structures or monitor wafers and are often destructive. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Metrology requirements for Interconnect are shown in Table 120 and the potential solutions are shown in Figure 84 below. The new measurement requirements for void detection in copper lines and killer pores in low κ appears to be difficult or impossible to meet. The need is to have a rapid, in-line observation of very small number of voids/larger pores. The main challenge is the requirement that the information be a statistically significant determination at the percentage specified in Table 120.

Table 120a Interconnect Metrology Technology Requirements—Near Term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	500	500	500	500	500	500	500
Measurement of deposited barrier layer at thickness (nm) /	12	10	9	8	7	6	6
Process range (±3σ)	10%	10%	10%	10%	10%	10%	10%
Precision 1s (nm) for P/T=0.1 [B]	0.12	0.1	0.09	0.08	0.07	0.06	0.06
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	27	23	20	18	18	15	10
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1% or more of total metal level conductor volume of copper lines and vias.	10.7	9	8	7	6.5	5.7	5
Detection of killer pore in ILD at (nm) size	10.7	9	8	7	6.5	5.7	5
Measure interlevel metal insulator bulk/effective dielectric constant (κ) and anisotropy on patterned structures [C]	<2.7	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4
	3.0–3.6	3.0–3.6	3.0–3.6	3.0–3.6	2.6–3.1	2.6–3.1	2.6–3.1

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 120a and 120b:

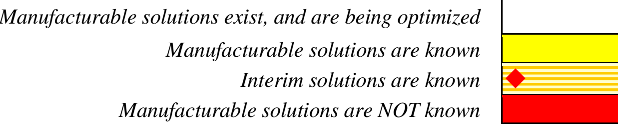
[A] Planarity control is mainly required for the first layer of interconnect dielectric that contains the transistor contacts. The planarity established by CMP sets the planarity for the subsequent process levels. Planarity after CMP of electrodeposited copper lines is largely established by using the hard mask at the top of the dielectric layer for the metal level as etch stop markers.

[B] The Roadmap now predicts that a deposited barrier will be used beyond the 65 nm node. These measurements are listed as Yellow (Manufacturable Solutions are Known) because barrier thickness should be measured on sidewall and bottom of contact/via instead of on horizontal areas. Precision metrics can be met for horizontal areas for barrier layers up to the 45 nm node.

[C] Minimum effective dielectric constant is listed. Due to divergence of DRAM and logic requirements, minimum listed number is associated with logic requirements. The development of a measurement technique for low-κ dielectric constant and anisotropy is complete up to 40 GHz.

Table 120b Interconnect Metrology Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*Driver*
Technology Node	*hp45*		*hp32*		*hp22*		
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	
MPU/ASIC Un-contacted Poly ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*	
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*	
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	**500**	**500**	**500**	**500**	**500**	**500**	*MPU*
Measurement of deposited barrier layer at thickness (nm)/ *Process range (±3σ)* *Precision 1σ(nm) for P/T=0.1 [B]*	**5** **10%** **0.5**	**4** **10%** **0.4**	**3.5** **10%** **0.35**	**3** **10%** **0.3**	**2.5** **10%** **0.25**	**2** **10%** **0.2**	*MPU*
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% ×height, 50% areal density, 500 μm square array	**10**	**8**	**7**	**6**	**5**	**4**	*MPU*
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1 % or more of total metal level conductor volume of copper line and 5% of vias.	**4.5**	**3.5**	**3.2**	**2.5**	**2.2**	**1.8**	*MPU*
Detection of killer pore in ILD at (nm) size	**2**	**1.6**	**1.4**	**1.1**	**1**	**0.8**	*MPU*
Measure interlevel metal insulator bulk / effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× clock frequency (GHz) [C]	**<1.9** **2.1**	**<2.1** **2.3**	**<1.7** **1.9**	**<1.7** **1.9**	**<1.6** **1.8**	**<1.5** **1.7**	*MPU*



Low-κ Metrology Needs

In-line metrology for non-porous low-κ processes is accomplished using measurements of film thickness and post CMP flatness. *In situ* sensors are widely used to control CMP. Metrology continues to be a critical part of research and development of porous low-κ materials. The need for transition of some of the measurements used during process development into volume manufacturing is a topic of debate. Examples include pore size distribution measurement. Pore size distribution has been characterized off-line by small angle neutron scattering, positron annihilation, a combination of gas absorption and ellipsometry (ellipsometric poresimetry), and small angle X-ray scattering (SAXS). SAXS and ellipsometric poresimetry can be used next to (at-line) a manufacturing line. The need for moving these methods into the fab is under evaluation. Detection of large, "killer, pores in patterned low κ has been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap.

High-frequency measurement of low-κ materials and test structures has been developed up to 40 GHz. As a result of extensive evaluation, the interconnect community no longer considers this measurement a critical need. Low-κ materials seem to have constant dielectric functions over the frequency range of interest (from 1 GHz to 10 GHz).

Thinning of porous low κ during chemical mechanical polishing technology must be controlled, and available flatness metrology further developed to for patterned porous low-κ wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations have developed (continue to develop) flatness tests that provide the information required for statistical process control that is useful for lithographic processing.

Interconnect specific CD measurement procedures must be further developed for control of etch processes. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capabilities of current in-line CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels.

Furthermore, scatterometry must be extended to contact and via structures. Electrical test structures continue to be an important means of evaluating the R-C properties of patterned low-κ films.

Conductor Metrology

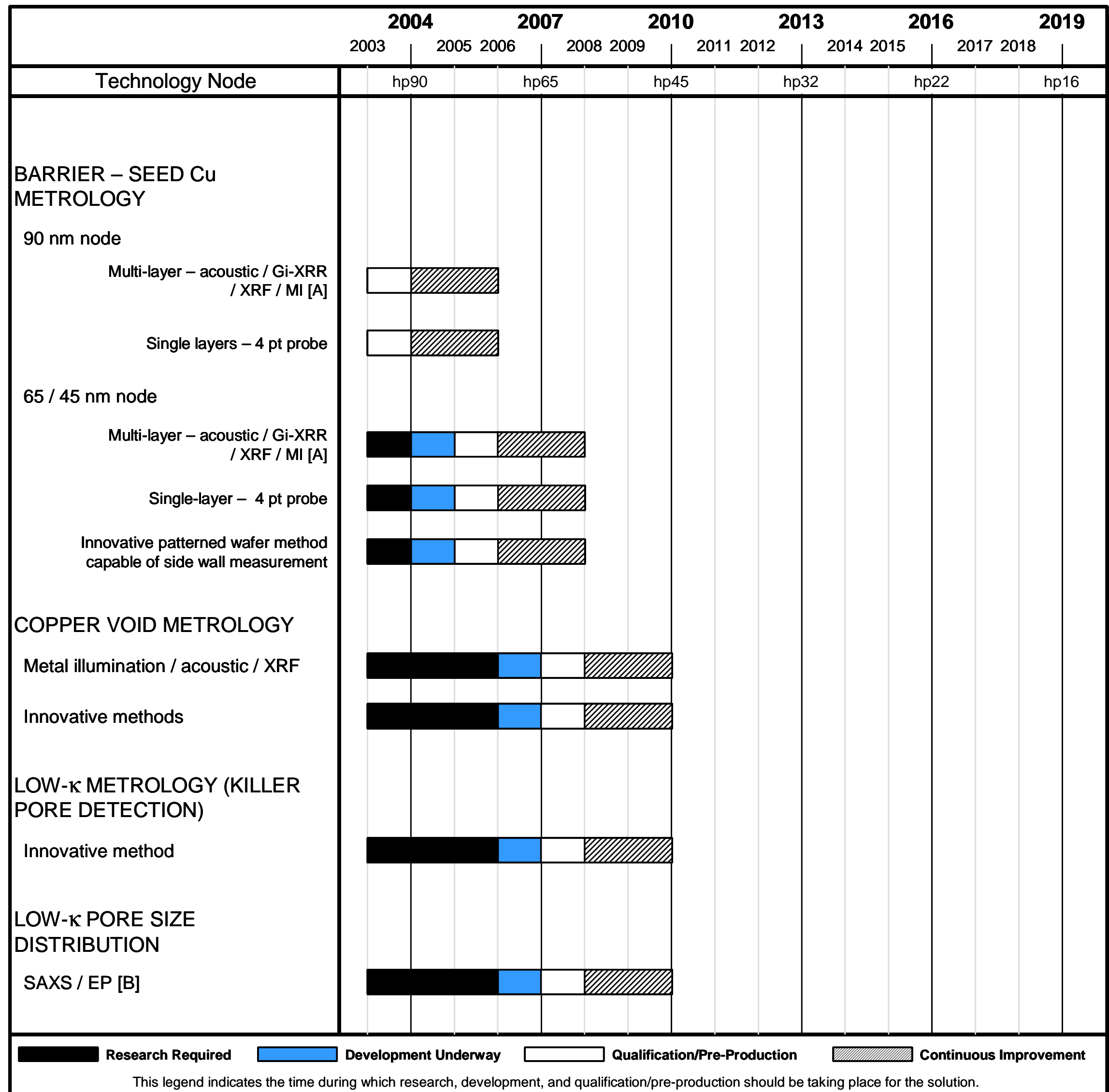
Copper electroplating systems need quantitative determination of the additives, byproducts and inorganic contents in the bath to maintain the desired properties in the electroplated copper film. Process monitoring requires *in situ* measurements of additives, byproducts and inorganic content that result from bath aging. A mass spectrometry based method of real-time sampling of bath contents provides a new potential solution. Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid Chromatography can be used to quantitative measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for the monitoring of inorganics.

There is some concern about the application of statistical process control to very thin barrier layers. Interconnect technical requirements indicate that barrier layers for future technology will be <5 nm thick. The 2001 ITRS specified a process window of 20% total thickness variation. The measurement precision (6σ) for a 6 nm film must be ≤0.12 nm, which is beyond current capabilities. It may be possible to use existing metrology capability to determine the presence or absence of these very thin films without using traditional SPC. Presently, a number of measurement methods are capable of measuring a barrier layer under seed copper when the films are horizontal. These methods include acoustic methods, X-ray reflectivity, and X-ray fluorescence. Some of these methods can be used on patterned wafers. At-line determination of the crystallographic texture (grain orientation) has been demonstrated using grazing X-ray diffraction. Detection of voids in copper lines is most useful after CMP and anneal processes. A metric for copper void content has been proposed in the Interconnect Roadmap and in line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Many of the methods are based on detection of changes in the total volume of the copper lines. The typical across-chip variation in the thickness of copper lines will mask the amount of voiding that these methods can observe. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, spatially resolved (for product wafers) multi-layer thickness measurements.

In-line measurement of crystallographic phase and crystallographic texture (grain orientation) of copper/barrier films is now possible using X-ray diffraction based methods. This technology is under evaluation for process monitoring, and the connection to electrical properties and process yield is being investigated.

Post CMP processes for interconnect structures require measurement of dishing and erosion in the copper lines. Current optical and acoustic techniques have been explored, but need to address the statistical sampling requirements for the accurate detection of dishing and erosion on a manufacturing environment.

Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.



MI—metal illumination, GI-XRR—grazing incidence X-ray reflectivity, XRF—X-ray fluorescence, SAXS—small angle X-ray scattering, EP—ellipsometric poresimetry

Figure 84 Interconnect Metrology Potential Solutions

Materials and Contamination Characterization

The rapid introduction of new materials, reduced feature size, new device structures, and low-temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility.

Often, offline methods provide information that inline methods cannot. For example, transmission electron microscopy (TEM) and scanning TEM, especially those capable of annular dark field (ADF) imaging, provide the highest spatial or cross-sectional characterization of ultra thin films and interfacial layers. ADF-STEM systems equipped with X-ray detection and electron energy loss instrumentation have provided new information about interface chemical bonding. High-performance secondary ion mass spectrometry (SIMS), and its variant time-of-flight (TOF) SIMS, provide contamination analysis of surfaces and thin film stacks. Grazing incidence X-ray reflectivity provides measurement of thin film thickness and density, while grazing incidence X-ray diffraction provides information about the crystalline

texture of thin films. The importance of using diffuse scattering in addition to specular scattering during XRR seems to be critical to building interfacial models from XRR that can be compared to interfacial models from other methods such as TEM/STEM, SIMS, and ion backscattering. Field emission Auger electron spectroscopy (FE-AES) provide composition analysis of particulate contamination down to less than 20 nm in size. Offline characterization of physical properties such as void content and size in porous low-κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials. Many of these tools are now available for full wafers up to 300 mm in diameter.

Continued development of TEM and STEM imaging capability is required. Several technologies are being applied to materials and process development for critical areas such as high- and low κ. Interfacial imaging has been greatly improved by the ADF detector for STEM imaging. The key to the STEM mode is the ability to do materials characterization in an area close to the size of the finest focus of the electron beam. ELS can be done in an area with a diameter of approximately 0.2 nm. With this greatly improved spatial localization, electron energy loss (ELS) characterization can be used to characterize interfacial regions such as the interface between high κ and silicon substrate. STEM with ADF imaging and ELS is just beginning to move into manufacturing support. Advances in image reconstruction software have also improved image resolution and thus interfacial imaging. Several improvements in TEM/STEM technology are now commercially available. These include lens aberration correction and monochromators for the electron beam.

Promising new technology such as high-energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. Beta site systems are now being tested.

A new approach to contamination control is being developed for *in-line* measurement. Real-time sampling of wet chemical baths has been added to a mass spectrometry based detection system for measurement of trace contamination in the bath solutions. While these and other offline characterization tools provide critical information for implementing the Roadmap, there are still many challenges. Characterization of the high-κ gate stacks to be used will be very difficult due to for example the layer-layer chemical intermixing and structure, interface roughness, and matrix-induced effects on some analytical probes and signals. In addition, as the device feature size continues to shrink, the applicability of characterizing planar structures as representative of the device feature becomes more questionable. Furthermore, the ongoing scaling makes the analysis of contamination in high aspect ratio structures even more difficult.

The introduction of new materials will raise new challenges in contamination analysis, such as happened with copper metallization where the very real possibility of cross contamination has led to the need to measure bulk copper contamination down to the order of 10^{10} atoms/cm^3 and surface copper contamination even in the edge exclusion and bevel regions, all because of the high diffusivity properties of this deleterious metal. The device shrinks are also tending to lower the thermal budgets of the process, so that the behavior of metal contamination and how to reduce its negative effects are changing the characterization needs. For example, low-temperature processing is changing which surface contamination elements, and at what levels, need to be controlled, and therefore measured. A key example is the role of surface calcium on very thin gate oxide integrity, and the difficult challenge of measuring this surface element at the 10^8 atoms/cm^3 level. Traditional methods such as vapor phase decomposition ICPMS can have day-to-day BLANK limitations at this level. In addition, the low-temperature processing is changing how the gettering of metal contamination is achieved. This change leads to challenges on how to characterize material properties to insure proper gettering.

The unexpected acceleration of the use of strained silicon without SOI has resulted in new metrology and characterization requirements earlier than expected in the 2001 Roadmap. These are under evaluation and development. Gate oxide metrology becomes even more complex, if strained Si channel structures are used as the starting material instead of bulk Si or SOI wafers. Strained Si is either grown on thick relaxed SiGe buffer layers on bulk Si or on compliant substrates consisting of thin SiGe layers on SOI. In both cases, the metrology of the starting material is crucial with a large number of parameters to be controlled: 1) Thickness and Ge profile of the SiGe buffer, 2) thickness of the strained Si channel, 3) roughness of the Si/SiGe interface and the Si surface, 4) magnitude and local variation of stress in the Si channel, 5) threading dislocation density in the Si channel (high sensitivity of the measurement is needed, since the desirable dislocation density is very low, $<10^3 10^4$ cm^{-2}), 6) density of other defects, such as twins, dislocation pile-ups, or misfit dislocations, particularly at the SiGe/Si channel interface, 7) distribution of dopants in channel and buffer (particularly after thermal annealing).

Transmission electron microscopy is readily available to determine thicknesses and interface/surface roughness of strained silicon on a microscopic scale. Both threading and misfit dislocations can be seen in TEM images, but TEM sensitivity to dislocations is poor because of the limited field of view. Atomic force microscopy determines the surface

roughness of the Si channel. Etch pit density (EPD) measurements determine the density of threading dislocations near the surface. Clear prescriptions for EPD are needed to select the etch depth. The meaning of lines and points in the EPD optical images need to be explained. Computer-controlled data analysis of EPD images is desirable, but not feasible at the moment. X-ray topography is another technique offering promise for defect detection. The Ge and dopant profiles can easily be measured with SIMS. A high sputtering rate is needed for thick SiGe buffers, while high depth resolution (possibly with a low-energy floating ion gun) enables the analysis of the thin Si channel and of the channel/buffer interface. Optical carrier excitation using a red photodiode directed at the sputtering crater avoids SIMS charging artifacts. This is particularly important for strained Si over SOI and for undoped layers.

Stress of the Si channel is the crucial parameter that determines the mobility enhancement of electrons and holes. Measuring this biaxial stress is possible using Raman spectrometry, since the energy of the Si-Si vibration in the Si channel depends on stress. However, the phonon deformation potential (describing the variation of the Si-Si phonon energy with stress) is not firmly established for thin Si channels. Such Raman measurements need to be performed using a UV laser to avoid penetration of the laser into the Si substrate. At 325 nm wavelength, the entire Raman signal stems from the thin Si channel, which makes data analysis simple. For longer wavelengths, the Si-Si vibration in the SiGe buffer appears also. The energy of this vibration depends on alloy composition and stress, which provides additional information. Raman mapping yields the stress distribution across the wafer with a maximum resolution of about 0.5 m, thus predicting transistor-to-transistor variations in mobility enhancements. It would be desirable to improve this resolution, possibly using solid or liquid immersion techniques.

Analysis of ellipsometry data for such strained Si channels is complicated, since the dielectric function of Si depends on the stress. This relationship (described by the piezo-optical or elasto-optical tensors) is qualitatively understood, but we lack sufficiently accurate quantitative data for fitting ellipsometry data of strained Si channels to extract the Si channel thickness. When only considering the UV portion of the ellipsometry spectra, there is some hope that we may be able to determine the gate oxide thickness, at least for sufficiently smooth surfaces. For rougher surfaces, there is an additional source of error, since the surface roughness enters the ellipsometry data analysis in a similar fashion as the native or gate oxide. For accurate gate oxide metrology, the Si surface roughness should be an order of magnitude less than the gate oxide thickness. This is satisfied for bulk Si starting materials, but may cause concerns for measurements on strained Si channels. Confinement effects in the thin Si channel are not yet an issue in the visible and UV portions of the ellipsometry spectra. In principle, ellipsometry should not only be able to determine the Si channel thickness, but also the Ge content of the SiGe buffer underneath. In practice, however, the Ge content determined from the data is much too low, possibly due to ignoring the strain effects on the Si dielectric function. (On pseudomorphic Si/SiGe heterostructures, ellipsometry is much more successful.)

X-ray reflectivity is an attractive alternative to spectroscopic ellipsometry to determine the strained Si channel thickness, since the refractive index for X-rays is very close to 1 and does not depend on the stress. Indeed, for Si channel thicknesses of the order of 10–20 nm, a clear series of interference fringes (sometimes accompanied by an additional large-angle peak of unknown origin) is obtained. However, determining the Si channel thickness using commercial software fitting packages does not always yield the correct value (in comparison to TEM). Possibly, this is related to the surface roughness, which is more difficult to handle for X-ray reflectivity experiments than for spectroscopic ellipsometry because of the smaller wavelength. Experimental concerns about X-ray instrument reliability and alignment are similar to described above for measurements on high-k gate dielectrics. High-resolution triple-axis X-ray diffraction has been used successfully (using lab and synchrotron X-ray sources) to determine the vertical Si lattice constant in the channel, another measure for the stress in the structures.

A number of microscopy methods are in the research and development phase. These include the point projection microscope (electron holography) and low-energy electron microscopy. Low-energy electron microscopy has been used to study surface science for several years. The application of this method to materials characterization and possibly to in-line metrology needs to be studied. A discussion of these methods is provided in the Microscopy Section of the Metrology Roadmap.

One of the five long-term difficult challenges for metrology is structural and elemental analysis at device dimensions. Fulfilling this need will require developing materials characterization methods that provide atomic maps. Local Electrode Atom Probe and similar methods hold promise of providing atom-by-atom maps for conductive samples. This technology needs further development of the method and its application. One challenge will be obtaining near 100% detection of each element during data acquisition.

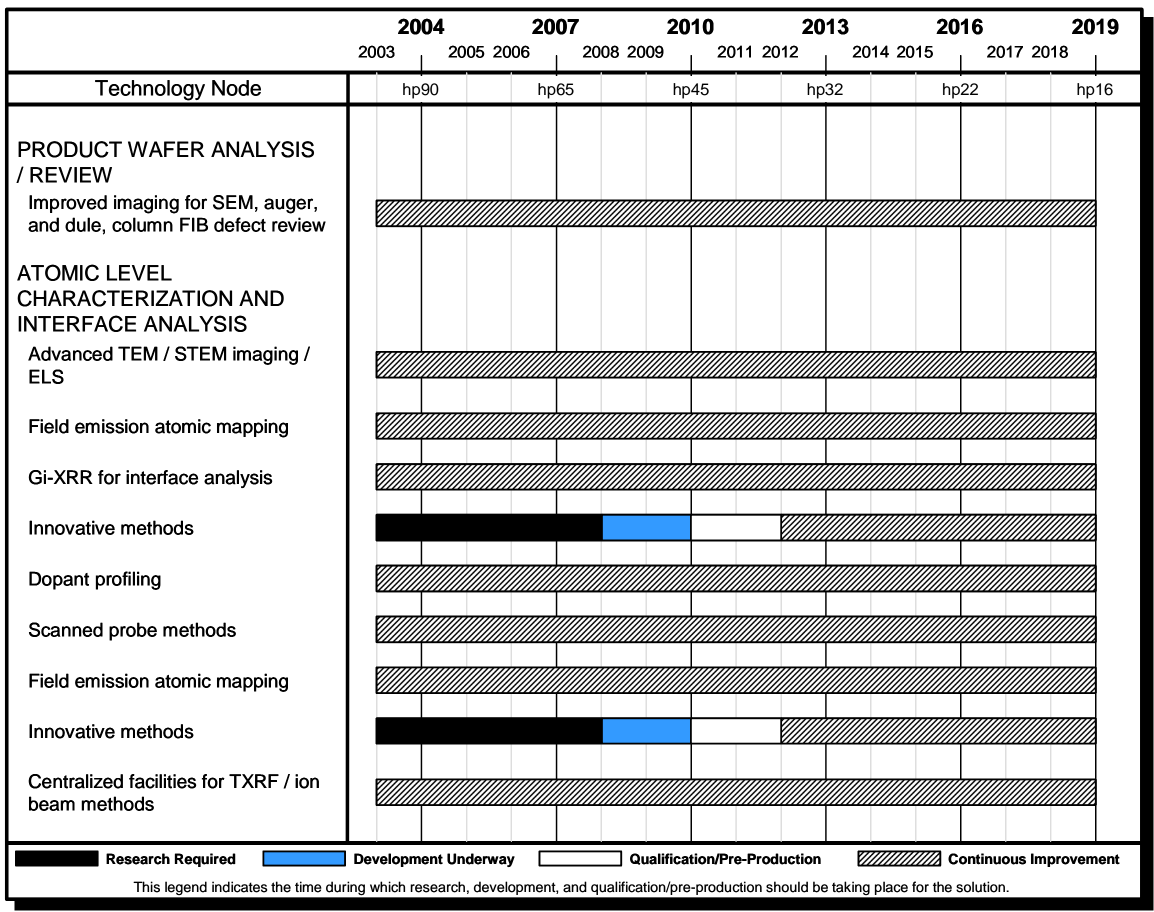


Figure 85 Materials and Contamination Potential Solutions

INTEGRATED METROLOGY AND ADVANCED PROCESS CONTROL

Metrology plays a key role in productivity gains made through *advanced process control* (APC), particularly as the trend toward integrated metrology—from offline to inline to *in situ* techniques—enables a richer, more powerful spectrum of process control strategies. At this point, advances in APC have been driven primarily by successes in run-to-run (R2R) control and in fault detection and classification (FDC). These advances in integrated metrology and APC have been substantial though in some ways serendipitous. At this point in time, it is clear that: 1) APC has demonstrated major value to the industry, and has been adopted by most manufacturers, to some extent, since its introduction into the Roadmap in 1994; 2) APC capabilities and associated sensors and metrology to support APC are available today for key process areas such as CMP and lithography, but 3) a truly comprehensive APC manufacturing strategy is not yet reality, nor is a portfolio of sensors and metrology tools to support complete factory-wide deployment, particularly given the profound changes in materials, processes, and device structures expected for future technology nodes. The benefits already realized from APC are driving the development of new sensor technologies and associated control software, which will allow factory-wide comprehensive solutions to be realized in the near future.

APC comprises two different thrusts as follows: 1) *Course correction* is aimed at adjustment of process parameters in order to compensate for systematic drift in equipment and process behavior. Here, R2R control has been the dominant driver, in which inline metrology is employed for feedback or feed-forward control, either on a wafer-to-wafer or batch-to-batch basis to maintain product quality in the presence of process variations, and to reduce non-product wafers. Real-time control, based on *in situ* and real-time sensors for during-process course correction, generally requires further development of more process-specific sensors with sufficient metrological precision. 2) *Fault management* is directed at rapid identification and response to equipment problems. The primary driver has been fault detection and classification (FDC), in which *in situ* and real-time sensors are used to identify common equipment faults, initiate repair actions, and reduce product scrap. Additional benefit is envisioned as sensor and metrology data are combined with informatics approaches to enable more sophisticated classification of more subtle fault sources, along with fault prognosis and maintenance rescheduling consistent with overall tool and factory efficiency. Building on the increasing confidence which

R2R and FDC successes have provided, the challenges for these two APC components are to add real-time control to R2R control for course correction, and to expand FDC to broader fault management.

Inline metrology tools now underpin broad implementations of R2R control, involving both feedback and multi-step feed-forward univariate or multivariate control capabilities. While *in situ* real-time sensors can in principle drive run-to-run control, they have been primarily exploited for real-time fault detection, with a few examples (e.g., interferometric etch end point control) in real-time course correction. The economic value of both run-to-run course correction and real-time fault detection have led to advances in equipment engineering capability (EEC), i.e., broad integration of APC hardware, models and algorithms with factory-level information distribution, scheduling, and operations. Despite these advances, availability of comprehensive APC systems requires further R&D in sensors, control strategies, new applications, and improved user interfaces to these APC systems to reduce the barriers to understanding and acceptance of APC.

Since R2R is primarily based on inline metrology, it delivers value primarily by compensating for longer-term process and equipment drifts, using feedback information to adjust process settings for the next wafer, and/or compensating for incoming product variability (wafer-to-wafer, lot-to-lot, etc.) by using feed-forward information to adjust the subsequent process(es) experienced by the same wafer. FDC delivers value by determining the health of the tool or process through evaluation of *in situ* information (process, equipment and wafer); this evaluation may occur in real-time, i.e., during processing, or as summary activity after processing has been completed. In the latter case, in-line wafer metrology represents a driver for FDC as well as R2R control. The increased availability and standardization of R2R control and FDC and their associated interfaces will also lead to control strategies and solutions that incorporate both capabilities in a complementary fashion. R2R control and FDC will be integrated as follows: 1) at the data storage level, thereby supporting data sharing and data mining between application types, 2) at the user interface level, thereby reducing the APC learning curve and allowing APC to be represented as a single entity in the factory, 3), at the logic interaction level, whereby control rules will allow FDC results to impact R2R control operation and vice-versa to support complementary utilization of these capabilities, and 4) eventually, at the algorithm level, where FDC and R2R models and modeling approaches would be integrated. Items 1) through 3) above will be critical to the realization of comprehensive factory-wide manufacturing strategies. The technology to support all of these items is incomplete. Other factors that will lead to factory-wide strategies include 1) hierarchical control solutions, 2) cascaded control between processes, and 3) coordination of control with yield management applications. Another key APC enabler is the development of standards that define the interaction of the APC applications with each other and with outside agents, and ensure access to wafer, process and equipment data as necessary to support these applications.

APC will benefit from the move to integrated metrology. Though a significant number of benefits from R2R control can be achieved with off-line metrology, e.g., with lithography overlay and CD control, integrated metrology will provide benefit by 1) shortening the control loop time, thereby improving control accuracy; 2) eliminating the human and associated wafer transport factors associated with non-integrated metrology; 3) allowing the metrology to be better tuned and optimized to the process; and 4) automating the matching process through recipe download to the tool and metrology. All of these factors lead to improved throughput and yield. Today integrated metrology is prevalent only in CMP (film thickness), but it is beginning to appear in etch (film thickness and CD) and lithography (CD) process types. Overlay metrology for lithography must evolve from off-line (stand-alone) to in-line for improved throughput and enabling of 100% sampling with minimal throughput penalty. In-line metrology, as a replacement for off-line metrology, will improve throughput, reduce cycle time, allow for increased sampling (number of wafers as well as points per wafer), and reduce control feed forward and feedback lag times.

Difficult challenges must be overcome before integrated metrology is accepted on a large scale. These challenges are in the areas of 1) performance and cost metrics for integrated metrology, which should be comparable to those for stand-alone metrology, 2) impact on tool throughput (which should approach zero), 3), integration, 4) data management, 5) setup (including calibration and training) and configuration time and management, 6) cost and difficulty of maintenance and impact on tool up-time, and 7) the understanding that the level of accuracy of integrated metrology is a function of the integration and control environment (unlike stand-alone metrology), and accuracy equivalence with stand-alone metrology may not be required to deliver significant benefit.

To the extent that real-time, *in situ* sensors can be made sufficiently quantitative and precise, they will add the capability for real-time course correction that compensates for short-term, random process variability. In turn, this will enable a true real-time APC, in which *in situ* sensors with real-time response drive both course correction and fault detection. The availability of real-time course correction will stimulate a new APC hierarchy, in which real-time course correction and fault detection operate at the tool (unit process) level much as regulatory control of equipment has long been practiced. Real-time course correction will tighten unit process variability as seen by inline metrology, but benefit from run-to-run

control will remain. This scenario suggests that a new control hierarchy should be developed which optimizes algorithms and responsibilities within the overall APC strategy, and which delivers metrology information upward in the hierarchy (e.g., *in situ* sensor data may enhance run-to-run control).

In-situ sensor technology remains far from complete. A reasonable group of sensors based on optical, chemical, and electrical signals from processes are available, but their development and demonstration as sufficiently quantitative metrology techniques for course correction has been limited. Note that the course correction demands substantially higher quantitative accuracy at this point than does fault management. *In situ* sensors that measure across-wafer uniformity and vertical profile are particularly needed, and if possible these should be accompanied by equipment designs that enable control actions that directly compensate for nonuniformities.

While *in situ*, real-time sensors are broadly deployed for detection and response to key equipment failure modes, *in situ* sensor and inline metrology have yet to be broadly coordinated and integrated to enable causal identification of more subtle failure modes and optimized maintenance/repair scheduling (i.e., fault .classification and prognosis). This is an important challenge given the economic consequences of downtime for preventive or emergency equipment maintenance.

In-situ sensors face additional challenge in the wealth of complex materials, processes, and device structures anticipated for future technology nodes. Measuring the composition, thickness, and uniformity of ultrathin gate dielectrics or metallic barrier layers presents a significant challenge, even with the adoption of atomic layer deposition (ALD): ALD chemistries, as well as materials, are complex, and their advantages must be compromised with the demands of manufacturing throughput. Nanoporous low-κ materials, and particularly their interfaces with barrier layers, present an equal challenge for *in situ* sensors. And *in situ* chemical identification is increasingly critical where surface chemistry plays a key role in product quality (e.g., in high-κ gate dielectrics, electroplating additives, CMP, and low-K dielectrics).

A key factor that will dictate not only the capability, but also acceptance, of all forms of APC and integrated metrology is *data quality*. Poor data quality can cause an APC system to reduce process performance rather than improve it. A prerequisite to APC deployment is thus acceptable levels of data quality provided by the tool, metrology and sensors. Data quality issues include availability, timeliness (of data capture and delivery), accuracy, resolution, freshness, and contextual richness (including time stamping). APC systems will benefit from the quantification of data quality by identifying minimum data quality required for effective APC deployment. Thus the roadmap must establish minimum data quality requirements, e.g. for each application and technology node, to support effective APC. A link is provided to show *key sensor technology requirements*.

CHARACTERIZATION AND METROLOGY FOR EMERGING DEVICE TECHNOLOGIES

Materials characterizations including electrical characterization are critical parts of the development of emerging devices. In this section, molecular electronics, nanowire devices, and spintronics are used to illustrate the state of materials characterization.[4] It is important to note that the some of these new technologies can be used to fabricate test structures for evaluating new or improved metrology methods. This section is not meant to be exhaustive, but rather it is meant to start the discussion between the metrology community and the emerging devices communities.

MOLECULAR ELECTRONICS

Molecular Electronics refers to the use of molecular components to replace either transistor or capacitor functions. One example of molecular electronics employs the use of crossed wires that are "tiled" in two dimensions. The molecular switches connect the upper and lower wires, and thus are two terminal switches. Electrical testing is a critical part of evaluation of molecular electronics. One type of two-terminal switch is the supramolecular complex made from catenanes or rotaxanes. Catenanes and rotaxanes are mechanically interlocking molecules that exhibit different positions relative to each other based on their oxidation state. Different physical conformations of these molecules have very different tunneling currents. The electrical properties of these new "molecular switches" require non-traditional electrical testing. Although the overlapping wires can be imaged using SEM, even a low-resolution view of molecular structure cannot be observed. Thus, microscopy is not presently capable of observing molecular conformations in these structures. However, molecular switches can be observed during switching under favorable conditions. Conductance switching was observed using scanning tunneling microscopy. Molecules appear as stick-like structures whose height changes. Materials

[4] *Metrology Requirements and the Limits of Measurement Technology for the Semiconductor Industry, A.C. Diebold, in Characterization and Metrology for ULSI Technology 2003, AIP, in press.*

characterization methods often provide other critical information. X-ray diffraction of crystal of molecular superstructures has been used to understand the atomic structure of these molecular superstructures. Electrical testing and chemical analysis have been used to understand the oxidation state and function of molecular electronics structures. Ultra-violet–visible wavelength absorption spectroscopy has been used to confirm the conformational state and redox potential of [2]-catenane.

NANOWIRES

Nanowire have a wide variety of shapes and thicknesses. Often, the nanowire dimensions are greater than those found in leading-edge copper interconnects. The thinnest nanowires are characterized for conduction and magnetic properties. Quantum confinement in two dimensions results in new properties for the thinnest nanowires. Transmission electron microscopy combined with scanned probe microscopy and electrical characterization has been used to characterize gold nanowires that were one to several atoms thick. These nanowires showed quantized conductance (G) based on the number of atoms in the diameter of the wire. Helical gold and silicon nanowire structures that are several atoms thick showed quantized conductance that was temperature dependant. Also, 4–5 nm-wide silicon nanowires have been grown using alkanethiol coated gold nanocrystals of 2.5 nm in diameter. The crystallographic orientation of these silicon nanowires was controlled by the reactant gas pressure. TEM and electron diffraction characterization required the use of chloroform to extract the nanowires onto a standard sample holder. These nanowires have small enough diameter to exhibit the effects of quantum confinement (and possibly new surface states) in photoluminescence and absorption spectra. The absorbtion edge was blue shifted from the indirect band edge of 1.1 eV of bulk Si and showed discrete absorbance features. *The fabrication methods used in the study of nanowires may provide the means of making reference and test materials for CD measurements before lithography methods used in volume manufacturing are available*. Transistor structures have also been fabricated using this technology. Again, TEM provided key materials characterization. If this technology is going to be used in volume manufacturing in the distant future, then new microscopy capabilities must be developed.

SPINTRONICS

A number of methods are used to characterize materials properties that are critical to devices that operate with selected electron spin states. One example is time resolved Faraday rotation that measures the change in polarization of light due to the magnetization of a material. Faraday rotation is determined using transmission measurements. The effect is greatly enhanced near quantum well resonances. In time resolved Faraday measurements, spin-up or spin-down excitons are selectively excited, and the spin scattering of these excitons impacts the magnetization of the sample. Manufacturing control will be another challenge because spin sensitive metrology is not used for any other application.

REFERENCE MEASUREMENT SYSTEM

A Reference Measurement System (RMS) is an instrument, or a set of several instruments, which complement each other in their ability to excel in various aspects of dimensional metrology. An RMS is well characterized using the best the science and technology of dimensional metrology can offer: applied physics, sound statistics and proper handling of all measurement error contributions. Because an RMS has been well characterized, it is more accurate, perhaps by an order of magnitude, and more precise than any instruments in a production fab.[5] An RMS must be sufficiently stable that other measurement systems can be related to it. An RMS can be used to track measurement discrepancies among the metrology instruments of a fab, and to control the performance and matching of production metrology instruments over time.

Due to the performance and reliability expected from this instrument, the RMS requires a significantly higher degree of care, scrutiny and testing than other fab instruments. Through its measurements this “golden” instrument can help production and reduce costs. However, this is an instrument that, by the nature of the semiconductor process, must reside within the clean environment of the fab so that wafers measured within this instrument can be allowed back into the process stream. Wafers from any other fab can come for measurements, and go back to serve as in-house references across the company or companies.

[5] *Lauchlan, L., Nyyssonen, D. and Sullivan, N. 1997. Metrology Methods in Photolithography in Handbook of Microlithography, Micromachining, and Microfabrication Vol 1. P. Rai-Choudhury, ed. SPIE Engineering Press, Bellingham, WA.*

REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties typically used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar instruments at different locations (internally or externally), or between the model and experiment. Reference materials are also extremely useful in testing and benchmarking instrumentation. Reference materials can be obtained from a variety of sources and come in a variety of forms and grades. Depending on the source, they may be called Certified Reference Materials (CRM), Consensus Reference Materials, NIST Traceable Reference Materials (NTRM®) or Standard Reference Materials (SRM®).[6]

NIST has maintained its position as one of the leading internationally accepted national authorities of measurement science in the semiconductor industry. NIST has also recognized the difficulty of keeping pace with the IC industry through the traditional method of need identification, instrumentation and technique development, and the development of SRMs. Several approaches allow the industry to supplement NIST's ability to supply reference materials. Commercial suppliers can submit potential calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark for the series of artifacts checked by NIST.[7] Another approach is the development of consensus reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM International. There are several technical requirements related to reference materials and certification, as follows:

- Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be much smaller than the desired calibration uncertainty.
- Reference materials may be difficult to manufacture with the desired attributes; frequently it is necessary to use specialized manufacturing techniques in short runs to obtain the samples to be measured and certified.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.
- The final measurement uncertainty in an industry measurement employing a reference material is a combination of uncertainty in the certified value of the reference material and additional uncertainties associated with comparing the reference material to the unknown. For this reason, the uncertainty in the reference material must be smaller than the desired uncertainty of the final measurement. An industry rule of thumb is that uncertainties in the certified value of the reference material be less than ¼ of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy (including both bias and variability) better than ¼ of the required final accuracy of the measurement for which it will be used.
- Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.
- It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process equipment development. Each type of reference material has its own set of difficult challenges, involving different combinations of the challenges described above.

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[6] *NTRM® and SRM® acronyms are registered trademarks of NIST.*
[7] *Use of the NTRM mark on a subsequent series of artifacts, even of the same type, requires additional verification testing by NIST.*