

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

MODELING AND SIMULATION

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MODELING AND SIMULATION

SCOPE

Technology Modeling and Simulation covers the region of the semiconductor modeling world called extended TCAD, and it is one of the few enabling methodologies that can reduce development cycle times and costs. Extended TCAD, within the scope of this document, covers the following topical areas: 1) *Front end process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding lithography; 2) *Lithography modeling*—modeling of the imaging of the mask by the lithography equipment, the photoresist characteristics and processing; 3) *Device modeling*—hierarchy of physically based models for the operational description of active devices; 4) *Interconnect and integrated passives modeling*—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 5) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 6) *Package simulation*—electrical, mechanical, and thermal modeling of chip packages; 7) *Materials modeling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 8) *Equipment/feature scale modeling*—hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point of the wafer, starting from the equipment geometry and settings; 9) *Numerical methods*—all algorithms needed to implement the models developed in any of the other sections, including grid generators, surface-advancement techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines. Here, items 7) to 9) are unique because they in fact cross-cut almost all other topics in Modeling and Simulation. Material and equipment issues are becoming more and more important in all processes as well as for active devices and interconnects. Numerical algorithms are shared by most of the areas in simulation.

Suppliers of Modeling and Simulation capability are mainly universities and research institutes funded by government and/or projects. TCAD vendors play an important role in the development of those capabilities, and are in most cases the interfaces between R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the development and optimization of technologies, devices and ICs.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs.

DIFFICULT CHALLENGES

The difficult challenges highlighted in Table 121 are those Modeling and Simulation requirements which on one hand must be met in time to support the high-level progress of the roadmap and on the other hand are most critical to fulfill due to their technical difficulty and the R&D resources needed. Additionally, it should be noted that a key difficult challenge present across all the modeling areas is that of experimental validation. This is especially difficult because for most processes many physical effects interact with each other and must be appropriately separated by well-selected experiments, in order to be able to develop predictive models and not simply fit experimental data. As devices shrink and new materials are introduced into the technology arena, new and enhanced analytical techniques are vital that can extract the necessary information for this model development and evaluation validation from the experiments. This critical need is mentioned as a cross-cut item with the Metrology ITWG.

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Table 121 Modeling and Simulation Difficult Challenges

<i>Difficult Challenges ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
High-frequency Circuit Modeling for 5–40 GHz Applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters High-frequency circuit models including non-quasi-static, substrate noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurements
Front-end Process Modeling for Nanometer Structures	Diffusion/activation/damage models and parameters including low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
Modeling of Equipment Influences on Features Generated in Deposition and Etching Processes	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms, and reduced models for complex chemistry Linked equipment/feature scale models CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, and ALD modeling Multi-generation equipment/wafer models
Lithography Simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models including line-edge roughness, etch resistance and mechanical stability Multi-generation lithography system models
Ultimate Nanoscale CMOS Simulation Capability	Methods and algorithms that contribute to prediction of CMOS limits Quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Phenomenological gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distributions
Thermal-mechanical-electrical Modeling for Interconnections and Packaging	Model thermal-mechanical and electronic properties of low κ , high κ , and conductors and the impact of processing on these properties Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion
<i>Difficult Challenges < 45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
Modeling of Processing and Electrical Properties of New Materials	Computational materials science tools to understand materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions
Compact Modeling including More Physical Models and Statistics	Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling
Nano-scale Modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes, quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
Optoelectronics Modeling	Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling Physical design tools for integrated electrical/optical systems

DIFFICULT CHALLENGES \geq 45 NM, THROUGH 2010

High-frequency circuit modeling for 5–40 GHz applications—Accurate and efficient modeling of interconnect parasitics and delays is of prime importance. 2D and 3D effects on interconnects must be considered with their statistical variations. Partitioning is needed for distributed R-C-L extractions. Efficient simulation techniques should handle multi-layer dielectrics. Compact models for active devices are needed for e.g. HBTs, CMOS and LDMOSTs. These include non-quasi-static effects and surrounding parasitics. Compact models for passive devices are needed for e.g. varactors, inductors, high-density capacitors, transformers and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. For these global effects accurate and efficient (layout) extraction techniques are needed. If possible, models should be physics-based to enable efficient modeling of statistics and variations. This challenge is primarily being addressed below in the subchapters on Circuit Component Modeling and on Interconnects and Integrated Passives Modeling.

Front-end process modeling for nanometer structures—This is the key challenge for the prediction of result from device fabrication. It overlaps to some extent with the challenge “Ultimate nanoscale CMOS simulation capability”, which however also includes materials and device simulation. Most important and challenging in the area of front-end process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants. Due to the strongly reduced thermal budgets needed for shallow junctions that process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of these two. Implantation damage, amorphization, re-crystallisation, and silicidation must be accurately simulated. In view of the need to increase carrier mobilities in the channel, the modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and for SOI structures. Model development, calibration and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects and stress, especially regarding two- and three-dimensional measurements. This challenge is being addressed below in the subchapter on Front-End Process Modeling.

Modeling of equipment influences on features generated in deposition and etching processes—Inhomogeneities of the results of a process step caused by the fabrication equipment used are key issues for manufacturability and yield of a technology. This refers especially to inhomogeneities across the wafer or between different wafers, and to drifts of process results between maintenance of equipment, e.g. due to coating of chamber walls. Processes where these effects are especially important are presently plasma deposition and etching, chemical vapor deposition, electroplating, and Chemical Mechanical Polishing (CMP). Generally, predictive simulation is still limited by lack of knowledge of the physical properties of materials and the chemical processes involved. The development of accurate models for reactions paths, the extraction of reliable values for the required parameters and also the development of reduced chemistry models which include only the primary mechanisms needed for practical applications is an important challenge. For better linking with feature-scale simulation, surface chemistry and plasma-surface interactions must be appropriately modeled. Beyond this in future also integrated equipment and feature scale simulation will be increasingly important for processes where a clear separation and interface between equipment- and feature-scale effects cannot be defined. This challenge is being addressed below in the subchapter on Equipment/Feature Scale Modeling.

Modeling of lithography technologies—This becomes increasingly important in the coming generations as the number of wavelengths and the number of available resolution enhancement techniques increases. Creation of improved modeling approaches for Optical Proximity Correction (OPC) and Phase Shifting Masks (PSM) synthesis is an important challenge. Developing predictive models for chemically amplified resists is a continuing challenge, but if developed, would greatly expand the application area of lithography modeling. This challenge is being addressed below in the subchapter on Lithography Modeling.

Ultimate nanoscale CMOS simulation capability—A fundamental question of the microelectronics industry continues to be what the ultimate limits of CMOS technology and devices are. Due to the progress made since the 2001 ITRS this issue has become even more important and urgent, and has therefore been pulled in from a long-term to a short-term challenge for Modeling and Simulation. The key requirement to deal with this challenge is predictive simulation of materials, processes, and device behavior including reliability. Material models are needed especially for gate-stacks including high- κ materials, for interconnects including size-dependent resistivity of copper and low- κ dielectrics, and for nonlinear photoresists. Due to the short-term need, such material models may in part still be phenomenological rather than

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derived from first principles. In addition, partly quantum based and non-equilibrium (ballistic) device simulation will be needed. Both atomistic and process-induced fluctuations critically affect the manufacturability of the ultimate CMOS devices and must therefore be dealt with in simulation. This challenge crosscuts most of the subchapters below.

Thermal-Mechanical-Electrical Modeling for interconnections and packaging—Performance and reliability of integrated circuits is ever more affected by interconnects and packaging. Electrical, thermal and mechanical properties highly interact with each other and must therefore be simulated together. Reliability issues requiring modeling include electromigration, stress voiding, integrity and adhesion of thin films, surface roughness, package fracture and corrosion. The capability to withstand the heat produced in the IC and to transport it off the chip is getting a top-level concern with further increasing densities. New materials such as low κ are being introduced to meet the targets of the roadmap. Thermal modeling of high- κ materials in gate stacks is also required. Due to their variety and lack of knowledge of their properties these two kinds of materials require large efforts on the development of models. Processing affects both material properties and the three-dimensional shape of interconnects. These non-idealities must be considered in the simulations. This challenge is being addressed below primarily in the subchapter on Interconnects and Integrated Passives Modeling.

DIFFICULT CHALLENGES < 45 NM, BEYOND 2010

Modeling of processing and electrical properties of new materials—Increasingly new materials need to be introduced in technology development due to physical limits which otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists. In consequence, equipment, process, device and circuit models must be extended to include these new materials. Furthermore, computational material science needs to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort. This challenge crosscuts most of the subchapters below.

Compact modeling including more physical models and statistics—Beyond the 45 nm node non-classical CMOS devices will be prominent. Possible device architectures are e.g. FD-SOI, FinFET or Dual Gate FET. In addition to the surface-potential-based models for conventional CMOS, this requires inclusion of e.g. quantum confinement and ballistic effects. Moreover, the computer-efficient inclusion of variability and statistics is crucial, even for non-mature processes. It enables fast ramp-up of mass production in new fabs. Modeling of nano-scale devices for their circuit behavior will be necessary. However, it is hard to predict in detail what new models will be needed for which devices. This challenge refers primarily to the subchapters on Circuits Component Modeling and on Device Modeling below.

Nano-Scale Modeling—Within the Emerging Research Devices section of PIDS new device structures such as nanowires, carbon nanotubes, quantum dots and molecular electronics are being discussed as good candidates to complement CMOS on the long-term run. For the assessment and optimization of such devices and their fabrication technologies suitable process and device simulation tools must be developed, including e.g. quantum transport, resonant tunneling, and spintronics. This challenge crosscuts most of the subchapters below.

Optoelectronics modeling—Further increasing frequencies and the upcoming limitations of metal interconnects make the link between electrical devices and optical interconnects an interesting option. Tools for the simulation of the fabrication of optical interconnects and of the performance of integrated electrical/optical systems must be developed. This challenge refers primarily to the subchapter on Interconnects and Integrated Passives Modeling below.

TECHNOLOGY REQUIREMENTS

In the following paragraphs the needs for each of the nine topical areas mentioned in the Scope are discussed in more detail. As mentioned above the areas “Materials Modeling,” “Equipment/Feature Scale Modeling,” and “Numerical Methods” are crosscutting all the other areas. Therefore, in addition to being discussed in their specific sections, they are also mentioned in many of the other paragraphs.

FRONT END PROCESS MODELING

Front-end process modeling includes the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding patterning activities. These areas are important for understanding and optimizing transistor fabrication, pushing the limits of scaling traditional planar devices, and evaluating process issues in alternative device architectures. The needs for modeling are driven by the reduction of feature size in scaling transistors and by the increasing number of new materials being considered to overcome scaling roadblocks. These not only cause

higher demands on model accuracy but also require models for effects considered as second order effects in the previous node, or models of new materials, material properties, and doping techniques.

Analytic models will continue to be needed for ion implantation and alternative doping techniques in the near term. Model data sets need to be extended to include damage and silicon-related materials, as well as very low (less than 1 KeV) and high-energy (some MeV) implantation. Channeling tails need to be modeled for the full range of tilt and rotation conditions and relevant layout stacks. With the reducing thermal budget, accurate lateral doping and damage distributions need to be modeled. Monte Carlo implant models are more and more required for application that cannot be adequately addressed by analytic models, e.g., doping of sidewalls of narrow trenches or in some cases S/D extensions. Model-based evaluation of alternative doping processes such as solid source and plasma immersion ion implantation (PIII) can also play a valuable role. As no technique has emerged as a clear winner so far, the modeling community needs to monitor the evolution of these techniques and track models for the most promising ones.

An optimum trade-off between minimized dopant diffusion and sufficient (maximized) dopant activation is the key for the formation of shallow junction and low device access resistance. Improved physical understanding of the related mechanisms is therefore directly important for technology development and also the prerequisite for any work on physical modeling. For doping diffusion and activation, continuum models will remain the mainstay of process simulators, and will need continued refinement to be able to adequately capture technologies with reduced thermal budgets and a wider range of impurity species including the effect of the pre-amorphization techniques. Point-defect based diffusion models will need to be considerably refined especially concerning the kinetics of dopants and defects in clustering and activation, in addition to capturing traditional transient enhanced diffusion effects. RTA ramp rates are an important factor, and their influence in diffusion/activation models needs to be improved. Models need to also consider experimental conditions different from traditional furnace or rapid thermal anneals, especially Spike Annealing and Laser Annealing. The effect of interfaces, especially non-SiO₂ interfaces, is becoming increasingly important. Here, the segregation and trapping of impurities needs to be modeled for all kinds of dielectrics, including high- κ material stacks, taking the influence of N, C, F, Ge, and metallic impurities and of knock-on oxygen into account.

Advanced process models will be needed for the modeling of metastable dopant activation (>solid solubility). These should include activation kinetics considering the reduced front-end thermal budget and deactivation kinetics during subsequent backend processing. Models for surface and interface diffusion will be needed. These include interactions with SiO₂ and new gate dielectric materials. Process models for diffusion/activation in alternative materials (such as SiGe or SiGe:C) need also to be improved as well as those for very thin body, including SOI, needed for alternative devices with or without any intrinsic mechanical stresses.

Atomistic process models are beginning to play an important role, both as direct simulation approaches for front-end processes and as a pathway to improved continuum model development and parameter extraction. Detailed insight into dopant-defect interactions using *ab initio* methods will be needed for understanding the kinetics of reduced thermal budget processes and the role of other impurities such as fluorine. Computational materials science will also allow atomistic studies of new processes, materials, and interfaces, such as high- κ dielectric deposition and interface properties. Hierarchical modeling from *ab initio* calculations to continuum needs to be developed and incorporated into mainstream TCAD flows.

As engineering of mechanical stress effects for device mobility improvement is becoming increasingly important, models for the effect of stress on reliability and dopant diffusion need to be developed. Stress resulting from all process steps must be considered over the full range of temperatures used in processing. Thin film growth needs to be better understood, including the reliability impact of stress in corners and small 3D structures.

For advanced gate stacks, modeling of high- κ dielectric film properties, interactions with substrates, and properties/interactions with metal gates is a critical need to enable continued EOT (Equivalent Oxide Thickness) scaling. Models should span from deposition conditions through geometrical shape of the gate stack to structural properties such as interface defect density for use in device simulation.

Feature-scale models for deposition and etching need to be linked to equipment simulation. This will allow determination of the influence of equipment settings on feature topography as well as on inhomogeneities on the wafer and from wafer to wafer. This should also result in more physical feature scale models in particular for the new deposition techniques such as MOCVD or ALD and for epitaxial growth of semiconductors and dielectrics. Modeling of these processes will become more critical as we move beyond planar MOS to more complex device structures and integration schemes.

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For each of these front-end modeling areas, approaches need to be developed to enable estimation of the performance impact of variation in critical front-end process steps. These includes random effects such as random dopant fluctuation and systematic effects such as within-wafer etch variation, and are tightly linked to modeling of lithography variations such as proximity effects and line edge roughness.

Inverse modeling techniques have to be widely introduced in order to anticipate definition of the next architecture nodes without any frozen process flow, based on the existing technologies.

Improved metrology and analytical techniques are essential for the determination of accurate process models, especially tools for these ultra shallow geometries, thin films and dopant levels. Novel materials/interface measurement techniques for these new materials systems are also required.

LITHOGRAPHY MODELING

Lithography modeling and simulation needs have been sub-divided into five areas as follows: image modeling, electromagnetic scattering analysis, resist modeling, integrated modeling systems, and coupling of metrology and modeling. These areas are discussed below.

- *Image modeling*—More accurate, flexible, and efficient imaging models are needed for the simulation support in the development of new process technology. The existing models and software implementations have to be critically evaluated with respect to their capability to describe polarization effects that occur at extreme numerical apertures, especially in immersion lithography. Advanced image models have to cover all types of polarization effects such as spatial variation of polarization inside source and projector pupils, birefringence of lenses, and polarization aberrations. Improved simulation approaches are required to describe flare effects resulting from physically rough surfaces in lithographic imaging systems.
- *Electromagnetic scattering analysis*—Electromagnetic scattering analysis will need to become part of the mainstream investigation capability. Scattering from phase shift masks, and scattering from wafer topography underlying the resist are two examples of applications requiring rigorous electromagnetic capability. The critical evaluation and optimization of reticle related optical enhancement techniques such as OPC and PSM requires more efficient and faster modeling approaches. More efficient modeling techniques are also needed for the description of light scattering from mask defects, especially in EUV lithography.
- *Resist modeling*—Predictive, quantitative resist modeling will continue to be the bottleneck in lithography simulation. Accurate models for chemically amplified resists that include post exposure bake, diffusion, line edge roughness, and surface interactions are needed, and must be capable of correctly predicting three-dimensional resist patterns. The performance of simplified resist models such as diffused aerial image approaches has to be evaluated in comparison to full resist models. Thin and multilayer resist models that link the lithography to the etch process are becoming important. Photoresist patterns have to be evaluated with respect to their etch resistance and mechanical stability. Because of the increasing importance of polymer-size effects there is a growing need for resist studies based on computational molecular modeling.
- *Integrated modeling systems*—For lithographic imaging close to the theoretical resolution limits, the interaction between different components of the lithographic system such as the illumination system, the mask, the projection system, and the resist becomes increasingly complex. With so many independent parameters, and an avalanche of data to understand, computer-based optimization systems are a requirement to fine-tune future technologies that will operate near the limit of diffraction optics. Specifically, this includes the optimization of mask and source parameters in optical resolution enhancement techniques. Integrated modeling systems are also required for extensive defect printability studies from the mask through the final product.
- *Coupling of metrology and modeling*—More predictive process simulation requires a stronger connection between models and metrology tools. Methods have to be developed that translate the output of metrology tools into appropriate simulation parameters. Experimental schemes for the measurement of resist parameters, especially for 157 nm and EUV, have to be devised. Methods that are developed for the simulation of lithographic processes can also be used for the evaluation of metrology tools. This includes mask inspection, modeling of alignment signals for overlay, aberration measurement, and the extraction of resist modeling parameters from appropriate measurements.

Simulation models have to be validated across multiple features, sizes and pitches for 2D and 3D profiles by appropriate experiments. Extensive benchmarking can help to evaluate the accuracy of models to identify the most efficient modeling approaches.

The massive application of optical enhancement techniques such as OPC, PSM and off-axis illumination will increase the importance of lithography simulation for process development and optimization. The combination of well planned experiments and predictive lithography simulation will help to reduce the rise of process development costs.

An important application of simulation for the next few technology nodes will be evaluation of the trade-offs for the various lithography options (such as 193 nm versus 157 nm versus immersion lithography at 193 nm and at 157 nm on specific critical layers). For next-generation lithography technologies, there is a need to have reliable simulation tools for extreme ultra violet (EUV), for direct e-beam, for electron projection lithography (EPL), and for maskless lithography (ML²) techniques.

DEVICE MODELING

Device modeling refers in general to a suite of models and methods describing carrier transport in materials. Models range from the simple Drift Diffusion, which solves Poisson and Continuity Equations, to more complex and CPU intensive ones as the Energy Balance, which solve some simplification of the Boltzmann Equations. The choice of the appropriate model depends on the problem and the level of details required and it is therefore left to the user. In addition, the complex physics of today's devices mandates at times the usage of Monte Carlo codes, which stochastically solve the Boltzmann equation, and the usage of Schrödinger solvers that account for quantum effects.

Despite the significant advances of recent years in both numerics and physics, continuing development is required to meet the increasingly challenging industry needs for device exploration and optimization. Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount. What follows is a list of the most outstanding limitations.

Gate stack—Gate dielectrics have become so thin that tunneling gate current is today an important design factor. Detailed quantum modeling of the entire gate stack (channel-dielectric-electrode) is needed to represent the behavior of oxides and nitrided-oxides that are only a few atomic layers thick. It must include details of tunneling and charge transport in the dielectric, effective dielectric constants of complex dielectric stacks, interface states and trap distribution in high- κ materials. Fundamental material modeling should be intensified to aid in the search for alternative, high- κ gate dielectrics and their evaluation. The focus has to be on their resulting flat-band shifting, threshold and capacitance characteristics, channel mobility and reliability.

Stress and strain—Stack of different material layers and process thermal budget result in stress and strain fields that increasingly determine the device characteristics. Comprehensive models, which include the effect of arbitrary full-tensor stress fields on band-structure (band-edges, effective density-of-states, effective masses, mobility, saturation velocity), are of paramount importance.

Contact resistance—With shrinking device dimensions, the contact resistance contribution to the total device resistance (channel, S/D, contact) will increase and thus will play a more important role in predictive simulation of the current-voltage characteristics and trans-conductance. A correct modeling of contact and sheet resistance (high doping activation and mobility) is prerequisite for a correct device description.

3D modeling—Realistic doping distributions enhance the coupling among the various spatial directions in a device, thus requiring a full three-dimensional modeling of the problem. Effects such as gate edge roughness or width dependence greatly impact devices output characteristics and they need to be taken into account during device optimization studies. This implies that 3D simulations are no longer reserved for occasional, limited use but are a real need for everyday tasks. Therefore, device editors, gridding algorithms and solvers have to be enhanced to the point that 3D tools have complexity and computational requirements similar to 2D.

Dopant fluctuations—The ever shrinking geometries have created a singular problem unlike any other: Because of the small volumes involved modest fluctuations of implanted dopants will give rise to considerable differences in doping concentration, which in turn will have tremendous impact on devices characteristics. Dopant fluctuation will broaden the device parameters distribution and will need therefore to be taken into account for any optimization or manufacturability study. In this regime, each single device will have to be represented by an entire distribution of devices with random doping concentration (generable for example via Monte Carlo methods) and preferably in 3D, which re-emphasize the need of fast 3D simulators.

RF—Development of bipolar specific models lags behind that of models aimed at conventional CMOS scaling despite being as much or possibly more necessary. Consequently, support of RF, analog and mixed-signal CMOS, BiCMOS and

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Bipolar circuit design requires enhancements, especially in the numerical treatment of small signal analysis (AC) and large signal behavior (transient). Efficient tools are needed to analyze device performance, to characterize non-quasi-static effects, to minimize the requirement for time- and cost intensive RF measurements and to provide predictive data in the downscaled regime. Device simulation integrated with RF circuit or mixed-mode simulation could ease optimization but will require efficient algorithms. When coupling circuit and device simulations, calculations for different devices will need to be run in parallel, thus requiring the necessary hardware and software support. The employed models will have to take into account surface-quantization and direct gate tunneling. Comprehensive internal noise modeling must cover all the important internal noise sources from the sub-KHz to the at least 100-GHz regime. Efficient models for substrate noise coupling have to be provided to couple comprehensive descriptions of external noise sources to the transport equations in a flexible way. Finally, self-heating of chips frequency dependency of physical parameters must be taken into account.

CMOS scaling—Novel device architectures and ultimate CMOS scaling require more rigorous modeling. Channel lengths or silicon films of a few nanometers cannot be accurately represented without (partially) ballistic transport models, which also include quantum effects. Several approaches have been suggested so far, but they lack rigorous justifications in their approximations and are prohibitively computational intensive. Simpler schemes propose self-consistent Poisson-Schrödinger equations, whereas more advanced methods try to use Green's or Wigner's functions to solve the Wigner transport equation, the Kadanoff-Baym equation, or the many-particle quantum Liouville equation.

Novel devices—In recent years, a large variety of CMOS compatible new device architectures has been proposed. A promising method to suppress the short-channel effect exploits thin films, therefore fully depleted SOI, FinFETs, and various forms of double-gate or all-around gate structures have been investigated. For these structures the quantum transport models discussed above are indispensable. Additional device features being explored include non-planar or elevated S/D structures, transport engineered devices with strained Si or SiGe, for which a correct and comprehensive description of stress and strain effects becomes an essential requirement. Emerging memory technologies employ magnetic, paramagnetic, and ferroelectrics materials, therefore they require the modeling of spin, magnetic interaction and electrical polarization phenomena.

Miscellaneous—Good progress was made in the last decade for the modeling of substrate current and hot carrier injection effects. Applications of microscopic simulators have allowed a detailed understanding of the generation and dynamics of hot carriers. However, scaled devices because of their thin dielectric layers require further development, especially concerning trapping and de-trapping mechanisms or transport in dielectrics. Furthermore, models of charge trapping and transport in dielectrics for non-volatile memories still need significant improvements.

Highly demanded degradation analysis relies on similar models. Prediction of reliability under steady state and transient conditions or ESD has become an important aspect of the technology scaling analysis and unfortunately, only post-processing or empiric models are available.

For low power devices, the junction leakage current due primarily to band-to-band generation seriously limits the process window. Therefore, existing models as well as their parameters will need to be revisited.

To address design for manufacturability issues some representation of devices variability (doping, gate line width etc.) has to be developed and interfaced to circuit design.

Simulation for large area devices also needs to be explored. Power amplifiers or optical devices are usually built from many transistor cells connected together through a huge interconnect system. The impact of distribution effects on device parameters is not well understood and modeled, especially when thermal and electromagnetic effects are at play. Large signal behavior would be required but traditional TCAD is prohibitive because of the number of grid points necessary to discretize the whole system.

INTERCONNECTS AND INTEGRATED PASSIVES MODELING

Interconnects play an increasingly important role as a limiting factor for staying in pace with Moore' law to double the maximum clock frequency every 1.5 years. This refers both to their electrical performance and to their reliability, and in turn requires coupled electrical, mechanical, and thermal simulation. Concerning reliability, electromigration, stress voiding and extrusion are most important aspects. Both electrical performance and reliability are critically influenced by process conditions, material properties including the microstructure of copper and (porous) low- κ materials. Performance and reliability critically depend on design, but with further shrinking distances and cross sections the deviations from ideal structures resulting from real fabrication processes is another important factor. Similar to front-end technology, both

the modeling of the fabrication and then the modeling of the performance and reliability of interconnects, based on the results of processing and/or its simulation, are required. Whereas other subchapters deal with the first aspect, the latter one is addressed in this section.

A series of physical effects are responsible for the limitation of the maximum allowed frequency. Besides aspects considered already at larger feature sizes, such as resistivity, capacitance and inductance, these are: The skin effect that forces the current to pass through the surface of the conductors, the proximity effect that acts as a “high-frequency” Lorentz force effect, i.e. the high-frequency currents that are flowing in parallel runners will attract or repel each other due to electromagnetic interaction. Current crowding effects (due to high-frequency) are known to occur in corners, bends and splits of runners. In the latter cases two-dimensional approximations based on transmission-line theory are invalid and a full wave analysis is required.

Besides the demand to understand in sufficient detail these high-frequency effects, an increasing need is felt to be able to simulate integrated passive elements. The integrated passives have high potential as cost-saving solutions in production. In order to characterize these passive elements it is needed to simulate these components in realistic circumstances. For example, in order to determine the quality factor of a spiral inductor it should be known how much energy is consumed by Ohmic losses due to induced currents in the substrate. In fact, one is dealing here with a generic trend in future IC design: the electromagnetic properties of the passive components and the presence of semiconducting layers that respond in a highly non-linear way to the electromagnetic stimulus poses high demands on the simulation capabilities.

Of high priority are the coupled thermal and mechanical performance properties of thin multi-layer films. Structural and compositional properties of thin films need to be obtained and related to reliability effects. The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling can trigger fractures that may not be foreseen. Simulation tools are needed to more effectively study these effects than by experiment alone. The interplay with equipment and feature scale simulation becomes an increasingly important factor for being successful. The change to low- κ dielectrics with low thermal conductivity has placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development.

As the operation speed of devices is increasing to the multiple GHz range and the complexity of interconnect systems continuously increases, software tools with higher accuracy and better efficiency become necessary. Accurate modeling of high-frequency electromagnetic properties like inductive coupling is key. The ability to predict the electrical and parasitic properties of complex interconnect structures continues to be a challenge. Software tools and methodologies that link process results to results at the IC level, that identify reliability issues or design deficiencies, that give the designer capabilities to explore alternative interconnects easily are needed.

Today there are some potential solutions, but all these solutions need further development for being suitable to a day-by-day use in the design flow. The potential for the advanced modeling of the electrical performance fall in two categories:

- First, if the semiconducting substrate is low Ohmic, then the electromagnetic response can be captured in linear dependencies. In that case the substrate can be treated as a low conductive medium that is characterized by its conductivity and permittivity. Numerous modeling approaches are available that are based on a full wave approach. The method-of-moments (MoM) and the partial-element-equivalent-circuit (PEEC) method are pursued as a valuable scheme to simulate the electromagnetic environment. Recently, the finite-difference-time-domain method is also pursued for characterized interconnects and integrated passives in the high-frequency regime.
- The second category deals with the situation that the substrate is fully taken into account as a semiconductor, thereby responding in a non-linear manner to electromagnetic fields. Moreover, a second non-linearity is induced by the fact that the field-source dependency needs to be addressed self-consistently. Recently an approach has been presented that considers the self-consistent coupling of the Maxwell equations to the semiconductor device equations. The feasibility of the solution is demonstrated, however in order to convert this solution into a practical tool, a series of developments are still required. Questions that need to be addressed are: How can one extract, preferably in a (semi-) automatic way the equivalent circuit representation, i.e. the net list and the SPICE parameters or S parameters from the full wave solution? Reduced-order modeling techniques have high potential and deserve to be further developed and explored.

All full wave solutions suffer from a severe computational burden. A typical simulation of the electromagnetic behavior requires an about ten-fold larger set of node variables to be solved as compared to a steady-state simulation. Due to the

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dynamic character, the vector potential for the magnetic field must be included. In order to deal with the frequency dependence both the phases and amplitudes of the variables need to be stored. Therefore, fast linear solvers play a key-role in implementing full wave solutions in the design flow.

Interconnect performance simulation is getting especially difficult because the problem widely spans in four respects, as follows:

1. An increased coupling of electrical and thermal-mechanical simulation is necessary.
2. The final target is performance and reliability at least at chip level. However, with shrinking dimensions and increasing aspect ratios this is more and more influenced by process details leading to deviations from ideal interconnect shapes—so the problem spans from few Angstroms to several mm.
3. In the end details on feature level as well as the physical effects discussed above more and more influence the performance of the actual design—in turn, the various levels of interconnect simulation need suitably to be coupled with design in a bi-directional manner.
4. Simultaneous simulation of interconnects and packaging gets more and more important.

To solve these issues hierarchical simulation methodologies and tools must be developed.

CIRCUIT ELEMENT MODELING

A strong increase of design productivity is needed for several reasons. Firstly, the mask cost increases dramatically (see *Lithography*). This makes the cost of a re-design more significant. Secondly, the construction of a new fab requires higher investments. This implies a faster ramp-up to timely generate revenues (see *Factory Integration*). Accurate modeling of circuit behavior, including parasitics, is crucial for first-time-right designs. It should take into account statistics and variations of the processing. Preferably, these statistical models should be available long before process qualification.

Circuit element models for circuit simulation are key to chip design productivity. Many challenges can be found in the *Design chapter*. Examples are the increase of clock frequency, the decrease of supply voltage, the increased importance of weak inversion and the exponential increase of the circuit complexity. Model accuracy and CPU efficiency are two opposing requirements. This dichotomy gives rise to a hierarchy of models. The most accurate models are used to simulate small circuits. Less accurate models are derived to simulate larger circuits, and so forth. Similarly, this dichotomy implies a hierarchy of models at several structural levels; device level, cell level, block level.

Historically analog simulation needs have driven the development of circuit element models. Both analog and digital designers then use these models. The increasing number of (analog and digital) devices per chip necessitates faster models and improved convergence in the simulation tools. Device models will include many more detailed effects. Quantum effects, leakage, noise, distortion and non-quasi-static effects gain in importance. A natural tendency is to add new parameters for each model improvement. Making the models more physics-based with less fit parameters can prevent this. Robust and accurate parameter extraction algorithms are essential for each model. An industry standard for circuit element models will assist exchange of IP blocks and fab-less business models.

For CMOS the trend is from threshold-based models towards surface-potential-based models. Presently the first models of this generation are available: HiSIM, MOS Model 11 and SP2001. The surface-potential-based models are valid over the full operation range. They avoid the mathematical gluing between a sub threshold model and a saturation model. These models have less but more physics-based parameters. This enables fast parameter extraction and easy inclusion of variability and statistics. This is important for digital circuits, e.g. static noise margin in SRAM. However, it is crucial for analog and RF applications. These operate often in weak inversion, where the threshold-based models rely on mathematical fitting, whereas surface-potential-based models are physics based. For some RF applications longer-channel devices are used, making non-quasi-static models essential. For analog and RF the modeling of noise and distortion will need more attention. RF (noise) measurements should preferably be avoided for parameter extraction.

Compact models for future CMOS generations should model new effects correctly. Examples are mobility-enhanced channels and high- κ gate leakage. Non-classical CMOS devices (see the *PIDS chapter*) will pose additional modeling challenges. Many devices have fully depleted channels, like FD SOI-CMOS, FinFET, Omega FET, Dual Gate FET, etc. This enables shorter channels, which means more ballistic effects. Moreover, two channels close (10 nm) to each other will have quantum mechanical interactions. This is important in multi-channel devices like FinFET and Dual Gate FET. Given the small dimensions, variability and statistics will be more prominent in this class of devices. For non-CMOS devices it is hard to define the modeling challenges. The number of options in the *PIDS chapter* is still very large. For

bipolars, models will be extended towards extreme HBTs, either in SiGe(C) or in III-V materials. For memories models are needed for new memory concepts like FRAM, MRAM, phase-change as mentioned in the *PIDS chapter*.

The circuit modeling of RF will extend to the 100 GHz range: Either extreme RF applications (77 GHz car radar) or 30-40 GHz applications where (third harmonic) distortion is important. Models for active devices, including their parasitic elements, are crucial for good RF circuit modeling. However, the correct description of passive circuit components will need significant more attention. Modeling of inductors, transmission lines and varicaps will include skin effects and other resistance increase at higher frequencies. The models for these (frequency dependent) effects should not contain any frequency dependent elements. This allows time-domain simulations in addition to frequency-domain simulations. For several larger (active or passive) elements the non-quasi-static effects will be significant and should be modeled accurately.

The importance of interconnect modeling increases with the stronger contribution to circuit delays and cross talk. The physics of interconnect modeling is not very complicated. However, the complexity and the size of the interconnect network poses serious challenges. Different application need models for different effects, like e.g. cross talk, matching, inductive coupling (also in 3D), skin effects and size effects (see the *Interconnect chapter*). A hierarchical interconnect simulation approach is necessary to keep simulation times reasonable. Taking into account the inductances is important for fast-clocked circuits. For RF applications it is an essential part of the circuit behavior. Full wave description of interconnect devices, like transmission lines and antennas, will be common for high speed or high frequencies. In case the full-wave description of interconnect gets important beyond the device level, serious efforts are needed on complexity reduction algorithms.

In more complicated circuits several long-range effects will gain in importance. Examples are the substrate-coupling effects for mixed-signal and RF applications. The digital clock signal will propagate to the analog and RF parts and disturb their specifications. Temperature effects will get more important for SOI-based and thin-film devices. Hence, self-heating and mutual heating effects should be modeled in more detail. For RF applications, large-scale electromagnetic field effects will gain in importance. This should be taken into account beyond the device level.

Predictive reliability simulation will be more important. More designs will be close to the hard reliability limits. ESD is getting one of the most serious reliability problems in future processes. Predictive circuit-level simulation, based on device level compact models, is essential to guarantee ESD-safe chip-design. In addition, the prediction of electromigration from interconnect layout needs improvements to avoid super-worst-case margins. Simulation of oxide reliability, hot-carrier effects and EMC compatibility might pose constraints in some cases.

PACKAGE SIMULATION

IC-package co-design is a key crosscut issue with system-level considerations becoming increasingly important. In the past a package designer might have been presented with the die footprint including the placement of the die I/O pads as well as the placement of the I/O connections to the PCB (printed circuit board). With ever increasing pin counts and overall size constraints, this practice often leads to packages that are unreasonably expensive or that cannot be manufactured. Beyond being routable and manufacturable a package must meet demanding requirements with respect to signal integrity, power, temperature and mechanical integrity. The required electrical, thermal and mechanical simulations must be performed with consideration of the die and the system, and this is possible only with communication enabled by co-design tools. A properly designed co-design tool will interact directly with both the package and die databases and have the capability of communicating results between the two.

The more common package models today are lumped discrete models such as IBIS, SPEF or SPICE. There will continue to be demand for such models due to their simplicity and speed of simulation. In the near term such simple modeling needs to be improved to better describe the package. SPEF models are appropriate for the IC when the self-inductance of small short connections is important, but the absence of large current loops renders mutual inductance negligible. In a package with relatively long traces, large current loops and bond wires, mutual inductance can be extremely important, and it is becoming more important in the IC. IBIS models describe the cross-coupling well, but all die pins on a given package net are generally shorted together significantly limiting the possibilities for simulation. Neither of these formats properly addresses power and ground issues. With SPICE one can build more complex models of the ground and power structures, but the models tend to be cumbersome and slow.

Modeling of power and ground structures in the package is extremely important. Current bottlenecks, noise and simultaneous switching issues are critically important with repercussions for thermal analysis. It is difficult to ascertain if

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enough decoupling capacitors have been placed in the correct places to guarantee performance, or perhaps too many have been added negatively impacting cost and package size.

There is a clear need to move beyond models based upon discrete elements to distributed and transmission line models. In simple packages there may be very limited power and ground structures, while in a typical BGA (ball grid array) package only half of a given trace may cross a ground plane. In a more complex flip-chip design there may be many ground and power planes on alternating layers. Especially with increasing initiatives for package re-use, models for these packages may be generated once, then passed to many consumers. Hence there is a need to form a consensus on packaging model formats that are generally useful and easily shared. Alternative modeling schemes such as reduced-order models should be investigated. To allow for the increasing complexity and interactions of the IC-package-PCB system, a modular approach that allows for different implementations of different component models may likely be required, especially when considering system-in-package or system-on-chip solutions. It may be necessary to simultaneously consider digital, analog, RF and even MEMS (micro-electro-mechanical systems) and optical components.

Generating models for simulation is creating new challenges with regard to Numerical Methods. The package geometries are such that there is no substitute for fully three-dimensional field-solver extraction. In a flip-chip package there are sometimes so many layers and power and ground structures that the extraction of a single signal net may be very costly. In an MCM (multi-chip module) there may be longer traces that couple many nets together requiring a very large minimal set for extraction. In either case, chopping the problem into smaller pieces introduces significant fictitious fringing spoiling the power/ground extraction. The development of scalable field-solver engines that can manage full-package extraction is essential; scalability will likely be achieved through implementation on a parallel cluster. At the same time efficiencies with regard to time and memory consumption need to be further improved.

The introduction of low- κ dielectrics with low thermal conductivity increases the need for thermal analysis. ICs generating increasing amounts of heat will transfer more of that heat to packages that will be challenged to dissipate it, and in turn the package will transfer heat to the system. This again requires co-design tools that facilitate simultaneous analysis. Furthermore, current flow through ground and power structures must be understood because current bottlenecks can lead to hot spots.

Inherent and thermally induced mechanical stresses throughout the layer stack must be identified and modeled. The low- κ dielectrics often have reduced mechanical integrity, while at the same time thermal stresses are more severe. The stresses are especially enhanced with non-uniform heating induced by the die, by current bottlenecks in the ground and power planes, and with reduced thermal conductivity. Predictive software tools for stress migration and voiding, fracture and fatigue in thin films are needed.

MATERIALS MODELING

The determination of the physical properties of thin film and bulk materials and the impact of these properties on the electrical, mechanical, and thermal properties of devices and integrated circuits is becoming more and more important across all aspects of semiconductor technology as new materials are being explored. The strong driving forces behind this are the physical limits of material systems used so far. Both empirical and fundamental materials modeling and simulation are needed to aid in this understanding. Whereas at short time scales, e.g. for the short-term challenge “Ultimate nanoscale CMOS simulation capability” insufficient availability of fundamental materials modeling capability will frequently still require the use phenomenological models, in the long-term run first principle simulations will be indispensable. Problems to be addressed include the following:

- Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases that contain both experimental and, where not available, material parameters calculated from first principles such as plasma cross sections, chemical reaction rates, the thermal and mechanical properties of package materials, and interdiffusion constants are needed.
- Materials models are needed for improved (especially chemically amplified) resists, for advanced mask making and for multilayer mirrors to be used in EUV lithography.
- With devices continuing to shrink to nearly atomistic dimensions, materials simulation and modeling tools that go from atomistic descriptions to continuum results will become more and more important.
- For processing, needs include codes with no adjustable parameters for ion implantation, diffusion and activation, interdiffusion in thin films, dielectric properties, and transport properties. A key problem here is the approximate

solution of Schrödinger's equation that leads currently to discrepancies between first-principle simulations and experiment, and requires readjustment of the approximations.

- Interconnect performance and reliability will be strongly affected by the microstructure of copper, which must be taken into account in the simulation. Another issue for materials modeling are low- κ dielectrics.
- Most models used in device simulation can be considered as material models, because they are based, for example, on the band structure of the semiconductor. Also here major progress is needed due to shrinking dimensions, higher local fields and especially due to the use of strained substrates, SiGe and other new materials. See the *Device Modeling* subchapter.
- Many alternate materials are being suggested as possible solutions for some of the critical semiconductor roadmap roadblocks. Materials simulation tools that give insight to inter-relationships between the physical properties of multi-layer thin films and the electrical, thermal, and reliability aspects of the device or integrated circuit would allow "what-ifs" without the need for many and complex experimental characterizations.

EQUIPMENT/FEATURE SCALE MODELING

CURRENT STATUS

Traditionally, equipment modeling has dealt with predicting macroscopic phenomena based on equipment settings and geometries supplemented, in a rather disjunctive manner, with so-called feature scale simulation addressing either in isolation or through some linkage with the equipment model general phenomena on the microscopic scale. These functions were addressed separately in the context of multi-scale length modeling. However, the mission of 'equipment modeling' is evolving in its scope and now includes unit process simulation (i.e., quantitative simulation of individual process steps) through to integration of hierarchical simulation levels and process steps. This will lead to virtual process integration in the computational realm of the actual manufacturing cycle. With a growing fidelity of the representation of physical and chemical mechanisms a predictive capability appears in future realizable. In this respect, the entire manufacturing life-cycle starting with the concept and feasibility and ending in continuous improvement will be increasingly impacted by equipment simulation that is based on fundamental phenomena and mechanisms. Many of these themes are being addressed concurrently within the various technical communities where there are logical interfaces. Examples include lithography where the resist development, resist trim, poly or dielectric etch are inherently interlocked, or metal silicidation where equipment simulation and TCAD process modeling are tightly coupled. This development is already reflected by the inclusion of some aspects of equipment simulation in the Front-End and Lithography Modeling subchapter.

Classical equipment simulation has been primarily applied within semiconductor IC manufacturers who have developed in-house models with significant functionality. The state-of-the-art equipment modeling includes models for thermal and plasma processes, electroplating, atomic layer deposition (ALD), models describing thermal and chemical transport and the mechanical components such as friction and abrasion in Chemical Mechanical Polishing (CMP). Feature scale simulation is presently at a less mature level in terms of physical and chemical models being combined with stable and flexible 3D computational algorithms but should be viewed never the less as having been applied fairly successfully to relevant process tasks. Feature scale simulation models commonly applied in industrial environment are either analytic (string, level-set) or particle-based (Monte Carlo) with some measure of calibration to account phenomenologically for complex mechanisms such as the physics and chemistry of plasma bulk and surface interactions.

Coupling between unit process models representing different physics and chemistries, such as between lithography and etching is a reality now. Examples include couplings between the output of aerial image simulations and full models for gate etch processes at the equipment and/or feature scale. Computational resources and physical process knowledge available to modelers may often be limited though resulting in systems treated wholly at the feature level, with reduced or compact models and combinations of approaches.

In view of skyrocketing cost of experiments, accounting for linked processes including equipment influences is critical for modeling and simulation to contribute to cycle time reduction and to realize cost savings in the 300mm and advanced substrates (e.g. SOI) technology platforms.

REQUIREMENTS FOR IMPROVEMENT

Traditional Equipment Simulation

With respect to thermal, plasma processes, CVD, ALD, CMP and to a lesser extent electroplating equipment, process equipment behavior may be described using commercial or mature in-house models. At a less mature stage are wave

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driven plasma sources, magnetized plasma sources and the interaction between slurry chemistry, pad mechanics, and heat conduction in CMP tools.

Specific areas of improvement for chamber models include the following:

- Characterization of transport in magnetized and/or capacitively-coupled plasmas,
- Electrical modeling that replicates the non-idealities of industrial electrical matches,
- Electrostatic chuck modeling,
- Thermal dependence of etch and deposition systems,
- Predicting the effect of consumables on CMP polish rates and uniformity, and
- Influence of additives on electroplating or electroless fill and the resulting film morphology.

Moving from “data-matching” to “predictive” modeling requires inputs that rely less on questionable phenomenological approximations but more fundamentally describe the studied physical systems including a seamless representation of process integration. Processes of growing importance extend beyond those traditionally examined by modelers and include photoresist etch processes, advanced patterning integrations, novel etch stop layers and new gate stack material.

Feature Scale Simulation

Certain problems with high technology impact require a high degree of fidelity in the coupling between equipment and feature scale to be quantitative. One example is that of RTP where prediction of heat coupling affects dopant diffusion and activation significantly. In these and other instances the scales are straddled (cm-equipment, sub micron-feature to nanoscale) and may drive heightened attention to be paid to different model interfaces. One-way coupling from equipment to feature scale may be sufficient in some cases like inert annealing, but needs to be replaced in other cases like oxidation by bidirectional integration. In part, achieving robust coupling will be dependent on sorting out the physical and computational robustness of both feature and equipment scale simulations.

Data Needs

Data needs are generally focused at the description of precursor (etch or deposition) generation and transport. In CVD and ALD, quantum chemistry tools exist to probe most reactive systems; however, streamlined computational approaches to speed up the rate of mechanism development especially for metal-organic precursors used to deposit the high- κ materials for gate stacks are needed. Hierarchies of models ranging from ab-initio through equipment simulations to spreadsheet-like models should address this.

In plasma processes, electron and heavy particle impact cross-section related data for radicals; dissociation fragments and excited states are of ongoing importance. Emphasis needs to be on the dissociation pathways. The speed required to generate the data is an issue and as such judicious approximations may be needed and the emphasis shifted away from resolving collision processes. Details regarding electronic and thermally excited state plasmas are an important part of the picture. Overall, cost and time may shift the burden for supplying data to bona fide theoretical calculations from experiment.

For the case of electroplating, the adsorption/desorption behavior of each additive in the presence of an electric field on the deposition surface is unknown, and decomposition in the bath over time is not understood. Extension of quantum chemistry calculations to liquid systems, especially in the presence of electric fields, is lacking and needed.

Plasma interactions with eroding photoresist, the evolution of line edge roughness and its mitigation, and the impact of photoresist on processes elsewhere on the wafer and chamber need to be much better understood. The development of more sophisticated photoresist plasma interaction chemistry models is needed. Qualitative representations of interactions of arbitrary species on arbitrarily prepared surfaces would be invaluable. As a first step, relative orders of recombination and reaction rates for radicals on ultra low- κ (ULK) material surfaces have high value. Eventually the relative surface rates for all pertinent radicals on all materials will need to be determined. Plasma surface interaction data needs extend to metal alloys deposition processes for advanced metallization in both the back and front end.

Model Validation and Empirical Model Development

Cost-effective verification of process chemistry, especially plasma models is needed. Traditional beam and experimental electron transport studies will have to defer to probes of phenomena at the substrate. Pinhole experiments that characterize the transport of species to the wafer and through a facsimile of a feature need to be proliferated. Standardization of test structures (e.g., overhang structures) and wafers dedicated to specific diagnostics such as

temperature measurement are also needed. Real-time process monitors employing Fourier-Transform Infrared Spectroscopy (FTIR) or interferometry, for example, can be coupled with advanced process control methodologies and models for the dual purpose of control and process model verification and development. The major effort required for better model validation is without doubt sensor development.

In CMP, basic process characterizations are poorly understood. Pad surface roughness data and thermal measurements are required to develop models. Data are also needed to understand the wear of pads and conditioners as a function of process conditions, and the impact on polish rates. In addition, the flow and agglomeration behavior of slurry under stress needs to be characterized. Clearly, more systematic and fundamental approaches to characterizing these systems are required.

Integrated Model Development

Models that probe process integration are reality but by no means standard simulation tools. These tools need to communicate with layout tools and at least, etch and deposition models should be able to model standard test structures that are employed in unit process development. Although coupling between different process steps can mostly be described by feature-scale or wafer-scale data, equipment influences are key for most process steps and therefore also for the simulation of their interaction. Specific opportunities exist in first-principles based tiling design and etch process cognizant mask design. Standard computational platforms, chemistry/plasma chemistry mechanisms, and standard surface property databases are needed. The barrier to creating universal mechanisms and databases will be intellectual property considerations.

LOOKING FORWARD

Non-traditional applications of modeling and simulation will be important as with the advent of ablative methods, electropolishing, neutral beam technology and plasma source ion implantation. Health and environmental impact will also be drivers. Synthetic (computationally derived) FTIR spectra will be important when the species are unknown to exist or “standards” do not exist to benchmark their measurement. Time and cost savings exigencies will drive the integration of aerial image simulators that describe the as developed image on a wafer to other unit process simulations for gate process definition. Novel device manufacturing models will not only require topography prediction but also sub-surface phenomena will need to be resolved for the prediction and mitigation of damage. Simulations that can predict the impact of process conditions on film morphology as well as interface characteristics will become increasingly important. It is also necessary to couple these results onto electrical transport models to come closer to achieving the holy grail of determining the impact of equipment scale process knobs on electrical device characteristics. Being able to model the direct relationship between equipment settings and back end and front-end microstructure, electrical reliability and mechanical integrity will strongly improve manufacturing’s ability to realize the roadmap.

NUMERICAL METHODS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena to be addressed by extended TCAD. For example, more accurate solutions of the Boltzmann transport equation in device simulation are required. To include the stress and several defect species and complexes in the simulation of dopant diffusion and activation requires dealing with an increasing number of coupled partial differential equations over the device grid. Moreover, physical processes with different intrinsic time- and/or length scales critically influence each other, and have to be simulated adequately in a coupled manner—point-defect diffusion occurs on an orders of magnitude faster time scale than macroscopic process time. The gas flow, depletion, and reaction in an oxidation furnace on a macroscopic scale are the basis for the chemical vapor deposition in a contact hole, there also critically affected by the local geometry on a deep sub-micrometer scale. More recently, an increasing demand has been put on the simulation of electromagnetic effects such as the skin effect in conductors, the proximity effect and the substrate coupling. These are just some examples how increased requirements on predictability and accuracy of models induce more complex models and, in turn, drive the discretization methods and linear solver technology.

Increasing accuracy requirements lead in many domains of modeling to the transition to a completely different level of approach, such as Monte-Carlo instead of analytical simulation of ion implantation, atomistic modeling instead of continuum diffusion equations, rigorous solutions of Maxwell equations instead of the traditional thin mask approximation to enable the simulation of advanced masks (phase shifting masks, optical proximity correction) in optical lithography. These advanced approaches frequently require the development of new problem-specific and efficient algorithms, as the application of standard algorithms would result in prohibitive time and memory requirements. Not only the linear solvers as stand-alone libraries demands continuous improvement, but also research is required on how the set of discretized equations are scheduled and organized before submission to the linear solvers is done. In consequence, the

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state-of-the-art of the numerical methods and algorithms available or being developed mainly in other domains of science must be permanently checked from the point of view of the application requirements of all domains of simulation, described in this roadmap, and be used to influence and kick-off developments required.

Meshing, although always important for the efficient and accurate solution of differential equations, has become a major issue because device architectures are now essentially three-dimensional. The increase of the numbers of steps to be included in process simulation, and especially the frequent use of automated simulation splits to investigate process options and the sensitivity of electrical device data on process details requires completely automated grid generation. This automated grid generation must be reliable for all kinds of device geometries and distributions of volume variables, with a failure rate at least two orders of magnitude below current tools. In addition, meshing tools must be capable of resolving all critical features of the device or equipment, like small geometry features or steep dopant gradients, without unacceptable drawbacks in terms of mesh nodes or computation time needed for mesh generation or adaptation in the refinement as well as the coarsening direction.

Mesh generation time is especially critical in case of simulation splits or simulation runs with a large number of process steps. Considerable problems are caused especially in three-dimensional simulations by moving gradients of volume variables and even more by moving geometries: These require parallel mesh refinement and unrefinement or the use of moving mesh nodes, in most cases with additional requirements on the shape or quality of the mesh elements to be met to enable an appropriate solution of the physical model equations to be solved.

Meshing algorithms must guarantee that discretization errors caused by the removal or by the movement of mesh nodes do not negatively affect the simulation results: Especially for applications in sensitivity analysis it must be guaranteed that changes of the results are due to physical reasons and not critically affected by changes of the meshes used in the different simulations.

A favorite solution to this problem is that a new mesh should use as many nodes and elements of the preceding mesh as possible and appropriate, such as during the simulation of oxidation. Stable and efficient algorithms are needed to trace the change of device geometries especially in the three-dimensional simulation of process steps like etching where multiple layers have to be considered. Such algorithms must reliably avoid artifacts in device topology and allow for appropriate volume meshing. Currently, none of the several approaches used (triangulated surfaces, cells, level set; delooping) has demonstrated to solve all relevant application problems.

These meshing requirements outlined above are further extended by the growing demand for equipment and material simulation. While in this case the problem of moving geometries hardly exists, adaptation to time-dependent volume variables is still critical. A major concern is to combine the very different scale in the simulation problem: the on-chip features are on the nanometer to micron scale whereas the equipment scale is in the centimeter range. Automatic mesh generation and adaptation is especially important to resolve critical features of equipment geometry and the wafers to be processed, while avoiding a too high number of mesh nodes. This problem gets severe when coupling equipment and feature scale simulation. Several current tools for Computational Fluid Dynamics (CFD) calculations suffer from a complicated procedure to define the geometry to be simulated and to provide necessary information for mesh generation.

Particle-based Monte-Carlo codes need an increase in raw CPU speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more GFLOPS will at least be partly met by improving hardware, provided current trends continue. Workstation speed has improved by 1.8x on average each year since 1990. Parallel solution strategies are also needed in order to address computationally intensive 3D simulation needs. This especially includes the use of distributed systems (e.g., workstation clusters or PC farms). These systems are currently standard in industry. However, it has to be critically investigated which kind of simulations will only be possible with large shared-memory computers, and whether and how sufficiently powerful systems will be accessible to industry and research.

The linear solvers are often the bottleneck in the computation. Many millions of algebraic equations need to be solved simultaneously, by a two-fold iterative scheme. For example, the unification of the drift-diffusion model and the Maxwell equations demands that ~10 variables are solved for each grid node. The outer loop that is needed to address the non-linear coupling can be substantially speeded up by intelligent forward guessing strategies. Further improving of these methods will drastically reduce the number of iterations. The inner loop that is required for obtaining the updates can be improved considerably by re-ordering strategies, optimal preconditioning, and partitioning of the equation set. All these methods need to be exploited and optimized for the TCAD applications.

Research is also needed on arriving at robust solution techniques: effectively this means that the iteration sequence avoids local minima and the flow gets trapped, techniques need to be developed how to escape from these traps without fully destroying the so far achieved result. It still is the case that the user needs a detailed knowledge of the operation of the

simulation tools in order to use them for explorative purposes. Improvements are desirable in terms of ease of use, i.e. built-in strategies should be available.

Research is also needed on developing robust and efficient parameter extraction algorithm. Without a well-calibrated parameter set, simulators lose their practical values. However, calibration work is frequently a time consuming and delicate issue, due to a large number of parameters and the so-called “local minimum problem.” Some algorithms, such as GA (genetic algorithm), may be good candidates to solve this problem, but only if remarkable improvements in its efficiency are realized.

A continuous challenge is inverse modeling, which has a potential capability of providing us with information of parameters that are difficult to measure such as two-dimensional dopant distribution, the dominant chemical-reaction-path, etc. From the mathematical point of view inverse modeling is a delicate issue because a limited set of data has to be correlated to a large collection of configurations that could reproduce the restricted data set. This means that in many cases, no satisfactory solution can be obtained, or in other cases, the obtained solution represents one example of millions of configurations. However, it has a potential of opening a new way of application for modeling and simulation. Preferring one configuration above another one should be guided by objective criteria. The latter may be found by entropy principles or information theoretical considerations.

POTENTIAL SOLUTIONS

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. This document presents above specific needs to increase this effectiveness and to provide impact on our industry in the future. Whereas the discussion on the requirements given above implicitly included the potential technical solutions to meet them, some general actions are needed to enable Modeling and Simulation to fulfill these needs and in this way to provide the forecasted benefits to the semiconductor industry:

- Increase cross-discipline efforts will be vital in order to leverage on expertise of fields that were originally not related and need now to work together to cope with the challenges outlined in this document.
- Adequate resources for research must be mobilized and directed to efficiently work towards the technical solutions for the challenges and requirements defined. In addition to the definition of the top-level requirements in the ITRS, interactions between industry and research institutes both at universities and at independent laboratories must continue to be enhanced and extended in order to guide the activities towards the industrial requirements detailed in this roadmap. Especially, this interaction must also include the promotion and enabling of mid- to long-term research actions needed in Modeling and Simulation, which is generally pre-competitive and therefore an excellent field for broad cooperation. Nevertheless, short-term needs and financial boundary conditions in industry have so far frequently led to strong cuts of such activities, with the consequence of endangering the mid- to long-term success of the roadmap.
- Software houses, research institutes and universities must be strongly encouraged to standardize and/or open up some of their universally used Modeling and Simulation modules in order to avoid multiple work in the pre-competitive area. In the ideal case there should be vendor-independent standard interfaces which allow for the combination of tools from different sources, or at least standardized model-interfaces which allow R&D institutes to focus on the development of added-value features, like new models, while being compatible with supported software environments from the beginning and in this way reduce time-to-application. Semiconductor industry can have a central role in this respect by requesting such standardization when deciding about their software investments.
- With equipment vendors playing an ever larger role in process development, the target should be that not only a basic process is sold with the equipment but also an appropriate simulation tool (or at least a model with well-established parameters) to describe this equipment and process. For a well-characterized and stabilized process sufficient data should be available to enable the development of these features with high added value. Cooperation of equipment vendors with university and independent research institutes is vital for this process. Compatibility with overall simulation environments generally offered by software houses should be achieved via the standardized or open interfaces mentioned above, or via direct cooperation with relevant software vendors. In order not to limit the semiconductor industries’ choice of equipment and software either the standardized interfaces or non-exclusive cooperation would be preferred. Related IPR problems need to be solved well in time.

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- In order to further optimize the industrial benefit from simulation, the methodologies for evaluating the impact of Modeling and Simulation must be improved. The target should be to identify more in detail in which way simulation can most efficiently support the industrial development (“value for money”), but also to get a more clear view of the overall cost benefit as already estimated in Table 122b. Making the cost benefit from Modeling and Simulation more transparent should also help to get sufficient resources for the required R&D work without which the cost benefit cannot be achieved.

The most important general technical development needed in the field of Modeling and Simulation is that of integration – between equipment and process, between different processes, process to device, device to circuit, layout and design – but also between different levels of description. In some cases the Modeling and Simulation software tools are linked together (such as traditional TCAD process and device simulators, design tools), while in many other areas the software tools are still separated. If one examines the cycle time for development of a new technology, much of that time and cost is not in the individual module development, but at the integration level. There is a continued strong need for Modeling and Simulation tools to be better linked for determining unforeseen interactions of one step on the next. This type of effort is needed for the following:

- The interfacing or integration of individual equipment/feature scale simulation tools. An example is the linking of a lithography simulation tool that predicts exposure characteristics in photoresist with a plasma-etching tool that predicts etch profiles for process latitude and sensitivities.
- The interfacing of materials structural simulation tools with software that predicts electronic properties. An example where these tools would be useful is in the development of high- κ dielectric thin films. Future software tools in this area then might treat the gate stack as a system rather than as individual components. Unforeseen materials interaction issues, better “what-if” analyses, and reliability effects could be studied.
- The integration of chip performance tools with package thermal, mechanical, and electrical simulation tools to create a co-design environment.
- Structured data sets that contain needed physical constants that facilitate parameter passing between tools.
- The integration of device simulators with robust methods for creating compact models and device files for design.
- Generally, a hierarchy of closely coupled simulation tools must be developed – from spreadsheet to *ab-initio*. This would allow the industry to select the most appropriate level of description for their simulation problem in question, along with appropriate and efficient data transfer when the application requires investigations at different levels (e.g. for influence of process variations on design).

CAPABILITIES AND ACCURACY/SPEED REQUIREMENTS

Modeling and simulation encompasses a variety of applications with widely varying requirements. For example, in applications closely associated with design, speed and accuracy of phenomenological models are the primary requirements, while predictability in uncalibrated regimes is secondary. Examples are circuit modeling and the lithography models built into OPC systems. In applications associated with technology development, the requirement may be considered to be a mixture of physically based models and calibrated/parameterized empirical models. Traditional TCAD applications, when used to optimize technology development (using highly calibrated simulators), fit this description. Finally, there are modeling areas in which the basic physics are being explored. Examples are Monte Carlo device simulators, or first principles calculations of diffusion parameters for dopant diffusion in silicon. To give useful guidance for all these application areas, the Technology Requirements tables for Modeling and Simulation have been divided into tables for simulation “Capabilities” and tables for “Accuracy and Speed.” Refer to Table 122a, b, and c. It should be stated, however, that there is an overall trend to require more predictive physical models that need less calibration. Moreover, integration between different process steps (which influence each other) and between feature- and equipment scale becomes more and more important and close and makes it increasingly difficult to specify single items without taking others into consideration simultaneously.

The “Capabilities” requirements tables (Table 122a and c) are meant to describe the technology requirements for Modeling and Simulation that demand new features of modeling to be developed, or describe where existing models and tools are still largely unsatisfactory. An example would be the capability to model chemically amplified photoresists. In this case, the basic ability to predictively simulate the performance of such a nonlinear resist needs to be developed. This

type of requirement is often tied either to the introduction of new technologies or to new regimes of physical phenomena at smaller dimension.

In contrast, the “Accuracy and Speed” requirements table (Table 122b) more properly describes the level of simulator accuracy needed for process/circuit design or optimization. For TCAD applications, this level of accuracy is needed to achieve the overall TCAD cost reduction goals listed in the first row of the table. The cost reduction goal should be interpreted more generally as a cost and development time reduction, as it is understood that TCAD should speed up the process development schedule. For ECAD and design applications, these are the accuracy levels needed for designers to effectively create new products. Note that accuracy requirements are specified only for the near-term technology requirements; for the long term, investigation of new technologies is the overall priority. It should be recognized that at a given point in time, several technology generations are being simulated in parallel, with differing accuracy requirements for each.

It should be noted that the accuracy requirements in Table 122b refer to accuracies obtained after calibration of the simulation tools to a particular technology node. It is generally understood that for TCAD simulation tools in particular, calibration is required for each technology node because new technologies, materials, dopant species, and process regimes are introduced in each node.

Cost saving figures given in Table 122b are estimates for the cost saving by use of extended TCAD during the development of new processes, devices and ICs. They are based on a questionnaire-based survey held in Japan in 2002, which gave estimates of 26% reduction in time during development, 30% in numbers of lots, and 34% in numbers of process options. These numbers are the averages across the most impressively successful cases, which were evaluated not by modeling engineers but by more than 70 integration/device-engineers and managers of about 10 semiconductor companies in Japan.

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Table 122a Modeling and Simulation Technology Requirements: Capabilities—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Lithography							
Exposure	Include realistic properties of masks, birefringence of lenses; non-planar topographies		Simulation of immersion, EUV, EPL, ML2 lithographic processes including CPU-efficient algorithms				
Resist models	193 nm/157 nm resist models including ultra-thin resists		Detailed chemically amplified resist model including LER and EUV resists			Finite polymer-size effects	
Front End Process Modeling							
Gate Stack*	◆ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier)		Model materials properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage)			Processing and properties of alternative materials	
Diffusion and activation models	Interfaces, ultra-shallow junctions and activation		Enhance calibrated phenomenological models by physically based ones for Si based materials, including stress/strain				
Topography Modeling							
Deposition	Homogeneity, topography dependence		Electrical properties, stress, incl. microstructure			Adhesion and reliability, including microstructure	
Planarization	Cell-level CMP		Chip-level including dummy placement optimization			CMP process models for circuit design	
Etching	(Surface) physics based feature scale models			Integration of feature-scale simulation with equipment (plasma) models			
Numerical Device Modeling							
Classical CMOS*	◆ Mobility models incl. stress, surface roughness and high-κ		Device models with relevant quantum effects included			Models/algorithms to the scaling limit	
Non-classical CMOS including transport-enhanced devices*	◆ Mobility models incl. stress, surface roughness and high-κ		Device models with relevant quantum effects included, especially for ultra-thin films			Ballistic transport	
RF Modeling	Parasitic devices		High-frequency noise				
Circuit Component Modeling							
Active devices*	◆ Non-classical CMOS compact models/ non-quasi-static models and series resistance		Circuit models for non-classical CMOS devices including influences of statistics			Include ballistic effects	
Interconnects and integrated passives	On-chip inductance effects + frequency dependent resistance		Hierarchical full chip RLC			Include reliability	
Package Modeling							
Electrical modeling*	◆ Unified RLC extraction for package/chips		Reduced order models			Full-wave analysis	
Thermal-mechanical modeling	◆ Thermo-mechanical-integrated models		Include non-bulk materials properties			Include reliability	
Numerical analysis							
Algorithms*	◆ Robust, reliable 3D grid generation especially for process simulation		Faster linear solvers			Exploit parallel computation	

*For 2003, interim solutions are known but research is still needed towards mature commercial solutions.

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known

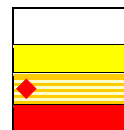


Table 122b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term

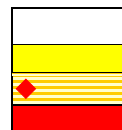
Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Technology-development cost reduction (due to TCAD)	35%	35%	35%	40%	40%	40%	40%
<i>Lithography Modeling</i>							
Resist profile prediction accuracy (5% of printed gate length)	3.3 nm	2.7 nm	2.3 nm	2.0 nm	1.8 nm	1.6 nm	1.4 nm
OPC model accuracy (about 3% of physical gate length)	1.5 nm	1.5 nm	1 nm	1 nm	1 nm	1 nm	1 nm
<i>Front End Process Modeling</i>							
Vertical junction depth simulation accuracy (% of physical gate length)	10% (4.5 nm)	10% (3.7 nm)	10% (3.2 nm)	10% (2.8 nm)	10% (2.5 nm)	10% (2.2 nm)	10% (2.0 nm)
Lateral junction depth (and abruptness) simulation accuracy (% of physical gate length)	5% (2.3 nm)	5% (1.9 nm)	5% (1.6 nm)	5% (1.4 nm)	5% (1.3 nm)	5% (1.1 nm)	5% (1.0 nm)
Total source/drain series resistance (accuracy)	10%	10%	10%	10%	10%	10%	10%
<i>Back-end process/Equipment/Topography Modeling</i>							
Etch/deposition cross wafer uniformity (% accuracy of the MPU physical gate length)	2.5%	2.5%	2.5%	2.5%	2.5%	2.5%	2.5%
2D/3D topography accuracy (% accuracy of MPU physical gate length)	5% (2.3 nm)	5% (1.9 nm)	5% (1.6 nm)	5% (1.4 nm)	5% (1.3 nm)	5% (1.1 nm)	5% (1.0 nm)
<i>Numerical Device Modeling</i>							
Accuracy of fit at given fit (% of maximum chip frequency)	10%	10%	10%	10%	10%	10%	10%
Gate leakage current accuracy (%) (I_g/I_{off})	25%	25%	25%	25%	25%	25%	25%
I_{on} accuracy	5%	5%	5%	3%	3%	3%	3%
I_{off} accuracy	30%	30%	30%	30%	30%	30%	30%
Long-channel V_t (accuracy)	3%	3%	3%	3%	3%	3%	3%
V_t rolloff accuracy (mV)	15mV	15mV	15mV	10mV	10mV	7mV	7mV
V_t 3F variation (%)	25%	25%	25%	25%	25%	25%	25%
<i>Circuit Element Modeling/ECAD</i>							
I-V error—compact model accuracy	5%	5%	5%	3%	3%	3%	3%
Sub-threshold current accuracy model accuracy	10%	10%	10%	10%	10%	10%	10%
Intrinsic MOS C-V accuracy	5%	5%	5%	5%	5%	5%	5%
Parasitic C-V accuracy	5%	5%	5%	5%	5%	5%	5%
Accuracy of G_m and r_0 at $V_t + 150mV$ versus L , V_{bs} , V_{ds} and T	10%	10%	10%	10%	10%	10%	10%
Circuit delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%
RLC delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%
<i>Package Modeling</i>							
Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	1%	1%	1%	1%
Temperature distribution for chip and package (accuracy)	1C	1C	1C	1C	1C	1C	1C
<i>Numerical Method</i>							
Speed-up of algorithms for 3D process/device (compared with year 2000)	4x	5.6x	8x	11.2x	16x	22.4x	32x

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



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Table 122c Modeling and Simulation Technology Requirements: Capabilities—Long-term

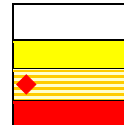
Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM 1/2 Pitch (nm)	45	35	32	25	22	18
Lithography Modeling						
Next generation lithography	NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)					
Resist technology	Finite polymer-size effects	Non-conventional photo-resist models				
Front End process Modeling						
Advanced process models	Atomistic process modeling					
Models for advanced doping techniques	New technology needed					
Topography Modeling						
Alternative material models	Calculation of thermal, mechanical and electronic properties	Atomistic material model				
Equipment impact on process results including material properties	Computer engineered materials and process recipes					
Numerical Device Modeling						
Emerging devices	Nanoscale simulation capability including accurate quantum effects					
Circuit Element Modeling/ECAD						
Advanced circuit models	Circuit models for nanoscale devices and interconnects					
Package Modeling						
Electrical/optical models	Mixed electrical-optical analysis	Reliability prediction in coupled modeling				
Numerics						
Numerical algorithms	Efficient atomistic/quantum methods	Multi-scale simulation (atomistic-continuum)				

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



REFERENCES

Most recent versions of other roadmaps including some future Modeling and Simulation topics for semiconductors are the NEMI Technology Roadmap produced by the National Electronics Manufacturing Initiative¹ in the USA, and the Technology Roadmap for Nanoelectronics² produced by the European Commission's IST programme (Future and Emerging Technologies). Simulation issues addressed in the NEMI roadmap are largely related to systems and products and therefore focus on reliability, electrical and thermal simulation, furthermore on optoelectronics, microelectromechanical systems, and nanoscale/spintronics. The EU Nanoelectronics Roadmap elaborates especially on emerging devices beyond CMOS and the nanofabrication techniques needed for them. Whereas this gives relevant information for simulation on the long-term scale, molecular modeling is described in some detail. The working group received contributions to its discussion from the European Industrial User Group "UPPER+,"³ funded by the European Commission within the IST programme. UPPER+ focuses on process and device modeling and simulation. These three external activities well complement each other.

INTER-ITWG ISSUES

Whereas cross-cut links between Modeling and Simulation and the focal ITWGs are summarized in the chapters of those ITWGs, strong links also exist to the other cross-cut ITWGs, as explained in the following sub-sections.

LINKS BETWEEN MODELING AND SIMULATION AND ENVIRONMENT, SAFETY AND HEALTH

For the optimization of ESH issues, the elementary chemical reactions in each relevant process must be understood as far as possible, and new measurement and evaluation methods must be implemented for developing processes with have the lowest ESH impact. Similarly, availability of these measurement methods and knowledge of the reactions is also a key requirement for the development of predictive models for those processes, which are dealt with in the Modeling and Simulation chapter. In turn, many enabling measurement techniques can be shared between ESH and the Modeling and Simulation community, although the final targets of the two areas are different: Assessment of material consumption and occurrence of dangerous species for ESH vs. the geometry, doping and morphology of layer stacks in Modeling and Simulation. Moreover, the implementation of such models in equipment simulation programs, especially for plasma processes, also offers the possibility to ESH to obtain quantitative data for the generation of dangerous species and in the ideal case also for optimization of equipment and process conditions to minimize already the generation of these species or their release from the process equipment. Moreover, simulation can frequently also contribute to characterization techniques by converting measured data (like spectra) into quantitative data (e.g., on gas composition), see the link between Modeling and Simulation and Metrology. In this way ESH and Modeling and Simulation have the potential to well support each other.

LINKS BETWEEN MODELING AND SIMULATION AND YIELD ENHANCEMENT

Links between Yield Enhancement on one side and Modeling and Simulation on the other side are twofold: First, Modeling and Simulation can contribute to the assessment of the influence of defects on the ICs. An obvious example is the question whether mask defects of a specific size, kind, and position are printed during an optical lithography step. This can well be studied by state-of-the-art simulation tools for optical lithography, which also allow to identify critical defect sizes above which the device or IC is destroyed e.g. because the defect will cause otherwise separate lines to be connected. Especially for the investigation of defect limits for patterning steps simulation offers very good prospects provided the simulation tools will be further developed accordingly. The propagation of defects in subsequent process steps through to devices and ICs and the mutual interactions of defects can be studied with various other Modeling and Simulation tools in order to monitor and minimize their impact.

Another important problem is the assessment of the impact of largely inevitable process fluctuations on the performance of devices and ICs. Many parameters in a fabrication line are distributed around their nominal values with some

¹ See <http://www.NEMI.org>.

² R. Compano, ed. *Technology Roadmap for Nanoelectronics. Second Edition. November 2000*, see <http://www.cordis.lu/ist/fet/nidqf.htm>.

³ See http://www.iisb.fraunhofer.de/en/arb_geb/upper_plus.htm.

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tolerances, like e.g. anneal temperatures, times, and ramp profiles, or have some drift in time. Coupled process and device simulation can be used to calculate the spread of critical product parameters resulting from such distributions of fabrication parameters, and in this way contribute to the assessment and optimization of the yield for a specific product and fabrication technology.

Obviously, these contributions from Modeling and Simulation to Yield Enhancement require sufficient generality, accuracy and speed of application of the simulation tools to be used, and are a challenge for the future development of Modeling and Simulation.

LINKS BETWEEN MODELING AND SIMULATION AND METROLOGY

Strong bi-directional links exist between Metrology on one hand side and Modeling and Simulation on the other hand side. A key issue in the development of physical models for semiconductor fabrication processes and equipment as well as devices is the availability of measurement techniques and methodologies which are capable of characterizing quantities such as geometry and chemical composition of layer stacks, dopant distributions, (point) defects, stress/strain, carrier concentrations, lifetime and mobility with the high accuracy and spatial resolution, and low detection limit required to enable model development and evaluation. Metrology is needed which gives sufficient information for true three-dimensional structures, and in many cases it must be applicable to real structures rather than test structures designed for that specific purpose. A further complication results from the required measurement and model accuracy approaching or even getting lower than the distance between individual (dopant) atoms. In these cases the interpretation of measurement results gets questionable, whereas in simulation the transition from continuum models based on partial differential equations to atomistic calculations is being made.

Apparently, the requirements of Modeling and Simulation contribute to driving the development of Metrology. However, simulation not only raises requirements but also can and must contribute to the development of metrology itself. The physical understanding of the processes occurring in the semiconductor and other materials considered is in many cases extremely valuable to interpret data collected in metrology and to convert them into quantitative information, to give realistic error estimates, and even to design or customize a measurement method. E.g. simulation can be used to relate variations of process parameters or atomic fluctuations to spreads of quantities that are measured, and in this way help to correctly interpret measurements. Frequently modeling groups directly contribute to the development and customization of measurement methodologies required to provide the data needed for model development. For example, with the increasing variety of new materials and processes in gate etch processes and complexity of gases and materials involved in dielectric etch and process cleans, simulation is called for making available a reliable means to characterize process emissions. In most cases, what evolves from surfaces or in the gas phase is unknown or difficult to synthesize outside of the particular process set-up and equipment. An emerging means of identifying species of potential environmental risk is through computational spectra generation. Synthetic reference spectra for materials can be generated with relative ease using computational chemistry approaches. For example, FTIR (Fourier-Transform Infrared Spectroscopy) spectra have been used to identify radicals of the RuO_x system in Ruthenium etch processes and to scan for noxious gases to ensure they are not produced in highly polymerizing dielectric etch gas chemistries. In both these cases, experimental reference spectra are difficult to generate or difficult to obtain.

Furthermore, it is frequently possible to verify simulation models and tools using measurement methods available (e.g. 2D measurement of cross sections), and then to use them beyond the domain directly accessible to measurement techniques (e.g., for 3D profiling) because in that cases the physics has not changed and the difference between the two situations can be reliably be handled by the algorithms in the simulator (e.g. solving partial differential equations in three instead of two dimensions). To conclude, Metrology and Modeling and Simulation must ever stronger cooperate to best take advantage from each other. Refer to the [Metrology chapter](#).

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

One fundamental question for the microelectronics industry is what the ultimate limits of CMOS are going to be, both in physical and also in economical respect. Another fundamental question is of course what will follow afterwards, or more and more complement CMOS for specific applications. Whereas the first of these two issues has in this version of the ITRS been shifted from the *Emerging Research Devices* subchapter to the overall [Process Integration, Devices, and Structures \(PIDS\) chapter](#), the latter issue is continued to be discussed within [Emerging Research Devices](#).

These fundamental questions are also being recognized within the Modeling and Simulation chapter: *Ultimate nanoscale CMOS simulation capability* is one of the six short-term challenges for Modeling and Simulation (See the beginning of this chapter.) Furthermore, in this roadmap *Nano-scale Modeling* has been newly introduced as a long-term challenge for Modeling and Simulation.

For both of these challenges Modeling and Simulation is called to contribute to the assessment of the options for device development being investigated by other ITWGs, especially by PIDS. In any case this request the availability of predictive physical models that must be developed in all areas covered by the Modeling and Simulation chapter. Besides sufficient and timely research, see the Potential Solutions section of this chapter, these challenges even more than in present request interdisciplinary cooperation, extending in future beyond electrical engineering, physics, chemistry, mathematics, computer science, material science to also include biology.