INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

TEST AND TEST EQUIPMENT

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SCOPE

The 2003 Test Roadmap has continued to expand scope from the 2001 edition. Increased focus has been placed on emerging difficult challenges to improve coverage of these topics, and this content of the test roadmap is expected to grow and mature with future roadmap revisions.

This revision cycle finds the test equipment industry at the beginning of a significant shift from traditional test architectures to "universal slot" architectures with high levels of test instrument encapsulation and modularity. This shift has been enabled by the continued evolution of technology and increased integration level of design components. In many cases a single Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC) is able to take the place of entire subsystems of electronics in older tester designs. Encapsulation and modularity has led to the concept of Open Architecture, the ability to mix and match test instruments from multiple suppliers into a single tester hardware and software environment. This concept raises significant business model challenges to the test equipment industry, an industry that is today based on full vertical integration and proprietary platforms. However, there are several potential advantages of an open architecture approach:

- Focus research and development investment, both dollars and effort, on the test instrument itself rather than test infrastructure
- Differentiation based on test capability rather than "platform"
- Suppliers focus on development of solutions within their particular core competency, reducing cost and speeding time to market
- Reduces the investment in re-engineering infrastructural elements
- Eliminates the need for each supplier to be everything to everyone—a very difficult position to achieve

In the end, the success of open architecture will be driven by the industry—both suppliers and customers, supply and demand—however it is indisputable that the next several years represent a turning point for many of the suppliers of test solutions. Regardless of the success of Open Architecture, emerging platforms offer a new level of capability flexibility and longevity that will have a significant impact on the industry and the deployment of test. It is quite possible that the next significant equipment selection decision may identify the test platform that will be deployed for all products for the next decade. This is an exciting time to be involved with test!

The organization of the chapter follows that of the 2001 roadmap revision. Test technology requirements are divided into sections by key market segments and design attributes, as these are the primary considerations that drive test decisions. In addition, several areas of difficult challenges are expanded to provide additional insight into the need for technology research and development.

This document represents significant contributions from a wide cross section of the industry as noted in the acknowledgements, however the Test Technical Working Group is always looking for additional participation—please contact the working group chair if you have interest in participating!

DIFFICULT CHALLENGES

Test process implementation decisions will continue to be driven by the constant trade-off between product test cost and test effectiveness. Cost pressure will continue for high performance digital and analog test equipment to manage leading edge design test requirements during the Design for Test (DFT) technology development phase or for designs that do not lend themselves to extensive DFT solutions. Use of DFT will continue to grow with the purpose of moving test complexity on-chip and thus reducing the capability requirements, and therefore cost, of manufacturing test equipment. Equipment cost and throughput continue to dominate product cost Paretos.

However, in the device debug and characterization world, at-speed functional and analog test will continue to serve as a primary vehicle for root cause of design and process errors and marginalities. Traditional test equipment based methodologies are required to correlate DFT-based results to end-use environment conditions. It is expected that this equipment will not proliferate into manufacturing, but rather be used to prove manufacturing capability on lower cost

high-volume testers. This represents a significant challenge to the industry, should this trend continue it would result in a reduction of the total available market for the most complex, development intensive test equipment and a void in research and development investment dollars. This void is manifesting itself today in the general hesitancy of suppliers to develop high-end solutions. New methodologies for design debug and characterization must be identified to avoid rising equipment costs.

Commodity memory bit density growth drives an associated increase in production test throughput to maintain cost parity for Flash and DRAM devices. Simple extensions to test parallelism will not be sufficient and may be limited by increasing DUT interface speed and accuracy requirements. Multi-bit testing, BIST, and Built-in Self Repair (BISR) will be essential to enable production throughput and yield. Breakthroughs in multi-die probe and parallel package handling capability will be required to sustain the cost per bit learning curve with each successive node.

Increasing device complexity in terms of transistor count, interface frequency, power consumption, and integration of diverse circuit types will drive significant challenges within the test community in the future. In the near term these challenges center on the abilities to provide test access through highly structured DFT methodologies and to deliver high performance signals to the device through the test equipment interface. Long-term challenges lie in test equipment-to-device interfaces, advanced test methodologies, and failure diagnosis. Further discussion of difficult challenges follows; Table 23 provides a summary of these challenges defined in priority order.

The following sections will expand on several of the most significant difficult challenges. This is followed by a summary table of the key concepts.

HIGH SPEED DIFFERENTIAL LINKS

High-speed serial interfaces have been used in the communications market segment for many years. While the communications market is expected to maintain a significant frequency lead, penetration of high-speed serial protocols into the Microprocessor, ASIC and System on Chip (SOC) markets in the form of multi-lane buses has accelerated dramatically. This trend brings a complex test problem, previously limited to the high-speed networking environment, into the mainstream. Key learnings from this market segment indicate the need to execute extensive jitter tolerance and jitter transfer testing, among others, on these interfaces. Such testing is done today in the analog domain through a rack and stack or mixed-signal tester approach. These solutions carry significant manufacturing cost considerations due to test time and equipment capital cost, and support a relatively limited number of high-speed serial ports on a single device. As these interfaces proliferate to many ports on a single device, the traditional analog test approach will fail due to the scalability of analog instrumentation. As the frequency of these interfaces continues to increase, alternative equipment solutions and test methods will need to be developed to enable engineering and manufacturing test.

HIGH INTEGRATION DESIGNS

Increasing pressure on consumer products for final product form factor and battery life is driving significant levels of single chip integration, blurring the lines between design types. The advent of SOC designs makes it difficult to determine whether analog circuits have been added to a fundamentally digital design (Big D/Little A) or logic circuits have been added to a fundamentally analog design (Big A/Little D). Test is no longer able to take advantage of the traditional design boundary conditions imposed by process technology to optimize equipment for particular circuit types. Future test platform designs must be flexible enough to effectively accommodate the mix and match of all circuit types on a single die or in a single package.

Analog complexity may vary from relatively low performance baseband up to and including multi-gigahertz radio frequency (RF) applications. In addition to logic and analog circuitry, a true SOC design may contain a significant amount of embedded volatile and/or non-volatile memory. The combination of these circuits on a single die compounds the test complexities and challenges for devices that fall in an increasingly commodity market. Fundamental innovation in DFT and test equipment architecture is needed to balance the long test time demands of memory test with the complexities of logic and analog circuit testing.

In addition, design throughput time for these devices will shrink dramatically. Large SOC designs will be constructed from reusable mixed technology design blocks, or Intellectual Property (IP) Cores, enabling designers to stitch together new designs with a great reduction in effort. Additionally, System-in-Package (SIP) techniques enable a step function increase in design density and diversity by combining multiple die in a single package. A highly structured, hierarchical DFT approach will be required to enable high-test coverage and test collateral reuse for embedded design blocks to prevent test from dominating time-to-market.

MULTI-DIE PACKAGING

Integration of customer defined "options" such as large memory arrays, while maintaining small product form factor and minimizing time to market is driving demand for multi-die packaging. Mixed technology multi-die packaging carries similar challenges as an SOC device with the added complication that the opportunities to reduce test complexity with DFT is at risk because individual die may come from different design teams or even different manufacturers. Additionally, devices with several unique test strategies each optimized for particular technologies and typically handled individually on specialized testers, could come together in one package. This represents a significant challenge to existing test methods and test equipment capability.

Multi-die package component yield is the product of the individual die yields and the packaging yield. To minimize the yield impact of multi-die packages, known-good die (KGD) from wafer probe will be required. KGD dramatically increases wafer probe defect detection requirements and challenges existing wafer probe and latent defect acceleration methodologies. Growing demand for multi-die packaging drives increased interest in enhanced wafer level test and burn-in capability and will likely lead to development of novel manufacturing process flows to maximize throughput and yield.

KNOWN GOOD DIE

The term Known Good Die (KGD) has been the subject of much debate in the industry since it was coined over a decade ago. The original definition offered was that a bare, bumped or TAB die should have the same quality and reliability metrics as its packaged brethren. Attempts to meet these criteria have met with mixed success.

As die products markets have evolved from a focus on the small volume, high performance, aerospace and military applications to high volume, low cost consumer products, the requirements for quality and reliability have changed. The term Known Good Die has also evolved from a focus on the product to a description of the test methods and reliability screens used to meet the application requirements. Today, rather than meet a nebulous criteria focused on an arbitrary judgment of customers needs, known good die processes are designed to meet the requirements for a particular market application as stated by the customer.

Definition and deployment of Known Good Die manufacturing test processes is a critical challenge for the industry over the near term. As the consumer product segment migrates to System in Package (SiP) technology to achieve density requirements, KGD becomes a fundamental requirement to achieve yield and cost metrics when multiple die are combined in a single package.

RELIABILITY SCREENS

The test process is responsible for screening of manufacturing defects that affect device functionality, performance, and reliability to reduce customer perceived Defects Per Million (DPM). A portion of the test flow is dedicated to the acceleration of latent defects that do not appear as test failures but would manifest as longer term reliability failures. Traditional techniques for screening of reliability failures include IDDQ, burn-in, and voltage stress.

The effectiveness of these methods is challenged by the continued device scaling with each successive process generation. Increases in device quiescent current in the off state is raising the level of background current in to the milliampere, and in some cases ampere range. These levels of background current increase the difficulty of identifying microampere to milliampere level IDDQ fault currents. Continued extension of techniques such as delta-IDDQ that have enabled extensions into current process generations is uncertain. At the same time, the effectiveness of voltage and temperature acceleration methodologies utilized by burn-in and voltage stress is declining due to reduced margin between operational and over-stress conditions. Costs associated with burn-in techniques continue to rise and in some cases have come to dominate manufacturing cost for high power products.

The increasing cost and declining effectiveness of current techniques for latent defect acceleration combine to create one of the most critical challenges facing the industry for future process generations. Extensions to current techniques may prove adequate for the next several years, but fundamental research in the development of new methodologies is required.

POTENTIAL YIELD LOSSES

Manufacturing yield loss occurs whenever any test or inspection process rejects as faulty a device that functions correctly. Causes of yield loss include:

- Tester inaccuracies (timing, voltage, current, temperature control, etc)

- Overtesting (e.g., delay faults on non-functional paths)
- Misprobing
- Mechanical damage during probing
- Handling issues
- Faulty BIST circuits
- Some IDDQ-only failures
- Faulty repairs of normally repairable circuits

The dominant yield loss from tester inaccuracy has recently become tester timing accuracy. Forecasts of off-chip pin speeds elsewhere in this document suggest that these increases will continue, putting pressure on the tester timing systems. These forecasts in the past have not taken into account the instability of the devices themselves (such as timing shifts due to temperature drift, V_{dd} noise, etc). Tester accuracy by itself cannot account for device instability.

Tester and device architectures must both adapt. Two basic issues must be addressed. First, in order to correct for drift from any source, high-speed buses are increasingly making use of forwarded clocks. Test systems must accommodate these forwarded clocks. Second, the highest data rates today are in self-timed data streams. Such data streams are expected to exhibit drift far in excess of a full bit time as the data rates continue to increase. Test systems that strobe device outputs based on synchronous timing calculations cannot track this drift. Tester architectures must accommodate the clocking process inherent in these self-timed data streams.

Tester designs capable of accommodating these device behaviors, along with the increased data rates they enable, may be even more expensive than the high-performance functional testers delivered today. At-speed functional test of complex devices with many such high-speed channels will apparently continue to be costly.

These potential yield losses and cost pressures may be mitigated by the use of alternative test methods to at-speed functional test. DFT methodologies must mature to provide coverage of the ”collateral” defects currently best identified by at-speed functional test vectors through advanced pattern application methods and novel fault models. Further work on appropriate fault models is required.

Similar yield loss issues have recently surfaced with inaccurate launch-capture delay tests. Delay path measurement errors of fifteen picoseconds have been observed in delay path measurements—this is 5% of recently announced internal clock periods, indicating a possibility of either yield loss or test escapes, as there is as yet no known way of adding margin testing to delay path measurement.

Delay path measurements also contribute to yield loss if inappropriate delay paths are measured. Tools must be developed to avoid yield loss due to measurement of false paths.

In a larger sense, however, the concept of yield loss may be understood to include discarding large numbers of properly fabricated devices or interconnect because a small number of properly fabricated devices are faulty. Yield loss of this sort is currently mitigated in high-density memories by providing redundant rows and columns; similar strategies have been used successfully at system levels using higher levels of reconfigurability.

Research and development regarding ways to incorporate on-line testing and repairs has a rich history in systems technology. Migrating the results of these efforts into ICs has the potential of reducing yield loss reckoned in this larger sense. More efforts in pursuit of on-line testing and repair technology are required.

MANUFACTURING TEST COST

Significant progress continues in the reduction of test equipment capital cost, however much work remains ahead of the industry. The equipment industry has benefited from the continuous trend toward availability of higher performance and higher integration components, enabling an increase in the test capability per dollar spent. Evidence of this trend is clear in the low performance logic test equipment that is available today. However, significant work remains to translate similar improvements to the broad market of logic, analog, RF, and memory applications.

The dramatic increase in SOC and System-in-Package (SiP) designs, largely targeted in commodity consumer applications, has consequently increased pressure to reduce the cost of test for mixed technology designs. These designs break the traditional barriers between digital, analog, RF, and mixed-signal test equipment capability requirements, resulting in a trend toward highly configurable, one-platform-fits-all test solutions. The first generation of this equipment has been a combination of leading edge technology from all segments with the consequence of increasing test cost due to

the high capital cost of this approach. Low cost equipment solutions targeting Design-for-Test enabled (DFT) devices do not scale into the mixed technology space today. The next logical step is to increase test system configurability and flexibility to achieve a more appropriate cost performance point—this is leading to a fundamental shift in test equipment architecture.

For many years the cost of the tester overwhelmed all of the other parameters in the device test cost equation (with the single exception of throughput). As the capital cost of the tester itself declines, the drivers of device test cost become less obvious and the analysis must look at all of the contributors to manufacturing test cost. The analysis must include the design non-recurrent engineering (NRE) associated with DFT, handler or prober equipment costs and many other factors.

The 1997 and 1999 roadmaps highlighted a potential trend showing microprocessor test cost approaching the total manufacturing cost. This assumed that cost per pin and pin-count trends would continue upwards for high-end microprocessor devices. Since the publication of the 1997 SIA roadmap, there has been a great deal of emphasis placed on ATE cost, cost of EDA tools, and test engineering cost at the manufacturing floor. This focus resulted in a better understanding of the cost of semiconductor test and has helped moderate the potential convergence forecast in costs. Looking forward, test cost per unit and test equipment capital cost considerations will continue to dominate manufacturing test methodology decisions.

The cost of manufacturing test consists of many cost positions; a high level overview follows:

1. Test Manufacturing
   - ATE capital cost
   - Handler cost
   - Probe-card cost
   - Spares and maintenance cost
   - Floor space cost
   - Electricity cost
   - Tester utilization
   - Operator cost
   - Other
2. Test Development
   - Test program
   - DFT
   - Tool depreciation
   - Time-to-market
   - Other
3. Product Related
   - DFT area overhead
   - Yield impact
   - Test quality
   - Other

Key parameters that describe the cell cost per unit are test cell efficiency and throughput (i.e., the test time and various index times). ATE capital cost has traditionally been measured using a simple cost-per-digital pin approach. Although this is a convenient metric, it is misleading because it ignores base system costs associated with equipment infrastructure and central instruments as well as the scaling that occurs with reducing pin-counts and number of sites. Moreover, it is not aligned with the trend toward ATE platforms, where the same base infrastructure can be used for very diverse sets of test channels. Therefore, it was suggested that using the following equation for each tester segment would be a more useful way to present and evaluate the ATE cost trends:

$$C_{ATE} = C_{BASE} + \sum_{i=0}^{x-1} C_{CHANNEL,i}$$

In this equation, CBASE equals the base cost of a test system with zero pins/channels (e.g., it includes the cost of the mechanical infrastructure, back-plane, central instruments, and resources required per site like power supplies). $C_{CHANNEL,i}$

equals the incremental cost for pin i, and x equals the number of pins. The summation addresses mixed configuration systems, which provide different test pin capabilities (e.g., digital, analog, RF, memory).

REDUCING COST OF TESTING

Looking forward, it is expected that the continuing focus on cost of test will result in a better understanding of trade-offs between test methodologies, fault models, and distributed test across multiple insertions among other considerations, resulting in overall test cost reduction. Also, it is expected that the critical value of test for yield learning (i.e., time-to-quality, time-to-yield, and time-to-market) will be considered in the cost of test equation. New yield attribution techniques, like statistical wafer map analysis, defect-based-test, yield attribution at core granularity, will support the yield-learning process.

Looking forward, test development time and cost will be reduced further by DFT techniques, test standards (i.e., to support test content reuse, test program inter-operability and manufacturing agility), automatic generation of test patterns (i.e., structural test approaches), and consideration of testability issues earlier in the design process. Structural test is becoming an industry wide practice, but will not replace functional test in most product segments in the near-term. DFT is mainstream in high-end digital logic designs and penetration into analog and SOC designs will commence in the near term.

DFT techniques will be used to increase throughput and/or utilization of tester resources, like digital test data compression techniques, bandwidth matching, and DFT that enables the testing of multiple cores concurrently (e.g., ADC, DAC, digital, and memory cores). ATE will have capabilities supporting EDA/DFT features, like for example capabilities to test multiple cores concurrently for a given site and straightforward communication between EDA and ATE environments (e.g., for data logging). The reduction in test time will partly be used to apply new deep sub-micron fault models as may be required to keep up test quality levels as technology progresses. DFT techniques will enable the use of lower cost lower capability equipment and reuse of existing equipment. For certain performance points and segments, dedicated low cost equipment is economically justified and will continue to be architected.

Packaging technologies like System-in-Package (SIP) (and stacked packaging) will push the need for Known Good Die (KGD), impacting wafer test time and cost. Moreover, the potential increase in package pin count may complicate final test requirements. For certain segments, new manufacturing process flows may become economically justified (e.g., extra wafer test insertions for embedded flash test and DRAMs).

The main focus of this section is on the cost of a test cell. A test cell is defined as a complete configuration consisting of automatic handler, tester and test fixture that is necessary to test a part. Note that test cost should not be minimized independently, but in the context of achieving the lowest overall manufacturing cost over a period of time. For example, increased test cost may be justifiable to accelerate yield ramp up if doing so it gives a lower overall manufacturing cost. In future updates of the roadmap, we intend to extend the scope of this section to also include forecasts that cover some of the other aspects of the cost of testing.

REDUCING BASE COST

The total base cost varies from $100,000 to $400,000 and is expected to decrease only slightly over time. Multi-site test increases throughput and distributes the base cost across multiple dice, thereby reducing the base cost per die. Multi-site test will become pervasive in segments beyond memory test, especially for applications where ATE base cost (and indexing costs) are dominating the cost equation. The increase in number of sites will be enabled by new probe card technologies with higher pin-counts and frequency capabilities. For extremely high number of sites, the probe-card cost and power supply costs may become a significant portion of the total cell cost. For certain product segments this may limit the economical justification for increasing the number of sites. Research and development will continue to bring to market cost-effective probe technologies directed at product offerings and test trends.

Product life cycles of system-on-chip (SOC) designs have shortened and SOC designs are breaking traditional barriers between digital, analog, RF, memory, and mixed signal test equipment. To leverage investment cost across multiple different products, to increase equipment utilization, to have flexibility to test a range of product segments, and to ensure availability of the latest ATE technologies, ATE must become modular and extendible – either by in-house platform strategies or by open-architecture initiatives. This trend will change the relationship between the different cost positions. For example, more functions traditionally in the chassis may now reside on the pin cards. An increase in number of test insertions may become economically justified only in specific product segments (e.g., extra wafer test insertions for embedded flash test and DRAMs).

REDUCING CHANNEL COST

The channel cost is expected to decrease through continued integration within the tester electronics, and also by widening DFT adoption that reduces ATE pin requirements.

The relative high cost of analog and RF test instruments and the long test times associated with testing of these circuits remains a key challenge. DFT methodologies for analog and mixed-signal test are in the early stages of development and represent a significant challenge for the industry. High-speed serial interfaces are penetrating ASIC and SOC markets. Jitter testing already today results in high test-times and equipment capital costs. As the number of interfaces increase, the cost problem will increase. Looking forward, new test methods need to be developed.

EXAMPLE PRODUCT SEGMENTS

The above trends in base cost and channel cost are analyzed for four different product segments, see the Table 21.

Table 21 Test Equipment Cost Trend per Product Segment

	Number of Channels					
	Functional (high-end)	*Functional (low-end)*	*Structural*	*Analog/RF*	*Memory*	*Base Cost*
Channel Cost	**$2.5K–$7K**	**$500–$2.5K**	**$500–$1K**	**$8K–$30K**	**$900–$1K**	
High-performance ASIC/MPU Product	**250**		**100**		**20**	**$250K–$550K**
Low-performance Microcontroller Product		**32**	**8**		**2**	**$150K–$350K**
Mixed-signal/RF SOC Product	**5**	**50**	**50**	**60**	**50**	**$150K–$400K**
Commodity Memory Product					**17**	**$30K–150K**

The increase in number of test channels per site per year is described in the corresponding rows. The channel cost trend is described in the corresponding columns.

Table 22 shows the expected trend in the number of sites. Note that there are multiple trajectories/approaches that achieve the test cost targets. The proposed trajectories are a typical situation for the different product segments. Also note that the optimum number of sites for a certain technology node is not necessarily the maximum number of sites possible. The used economic model will be made available.

Table 22a Multi-site Wafer Test (Package Test) for Product Segments—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	***107***	***90***	***80***	***70***	***65***	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
High Performance ASIC/MPU							
Number of sites (wafer test)	**1**	**4**	**8**	**8**	**8**	**8**	**16**
Number of sites (package test)	**2**	**2**	**4**	**4**	**4**	**4**	**8**
Low Performance Microcontroller							
Number of sites (wafer test)	**16**	**32**	**32**	**64**	**64**	**128**	**128**
Number of sites (package test)	**96**	**128**	**128**	**256**	**256**	**512**	**512**
Mixed-signal/RF							
Number of sites (wafer test)	**2**	**2**	**2**	**4**	**4**	**4**	**4**
Number of sites (package test)	**4**	**4**	**8**	**8**	**8**	**8**	**16**
Commodity Memory							
Number of sites (wafer test)	**128**	**128**	**128**	**128**	**256**	**256**	**256**
Number of sites (package test)	**64**	**128**	**128**	**128**	**256**	**256**	**256**

Table 22b Multi-site Wafer Test (Package Test) for Product Segments—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
High Performance ASIC/MPU						
Number of sites (wafer test)	**16**	**16**	**16**	**16**	**16**	**16**
Number of sites (package test)	**8**	**8**	**8**	**8**	**8**	**8**
Low Performance Microcontroller						
Number of sites (wafer test)	**128**	**128**	**128**	**256**	**256**	**512**
Number of sites (package test)	**512**	**512**	**512**	**768**	**768**	**1024**
Mixed-signal/RF						
Number of sites (wafer test)	**8**	**8**	**8**	**8**	**8**	**8**
Number of sites (package test)	**16**	**16**	**16**	**16**	**16**	**16**
Commodity Memory						
Number of sites (wafer test)	**512**	**512**	**512**	**512**	**512**	**512**
Number of sites (package test)	**512**	**512**	**512**	**512**	**512**	**512**

IMPORTANT AREAS OF CONCERN

1. Increases in the number of sites places severe demand on the ATE architectures and probe card technologies. Research and development will continue to bring to market cost-effective probe technologies directed at product offerings and multi-site test trends.

2. Once test compression becomes pervasive, it is expected that the digital test cost percentage of the overall cost of test will be reduced significantly. Therefore, the cost of test may become dominated by for example Analog/RF test.

3. The relative high cost of analog and RF test instruments and also the long test times associated with testing of these circuits remains a key challenge. To enable parallel test multiple instruments are required with fast parallel execution of DSP test algorithms like FFT. A secondary consideration for mixed signal multi-site test is the load board circuitry area for package test, especially for complex packages. The high number printed circuit board (PCB) layers make drilling through holes difficult. The number of ATE digital pins can also limits the number of sites, because many current generation mixed-signal designs generally don't use DFT/BIST and therefore require full functional test. This is expected to change with future designs due to cost pressure.

4. High-speed serial interfaces are penetrating ASIC and SOC markets. Jitter testing results in high test-times and equipment capital costs. As the number of interfaces increase, the cost problem will increase linearly. New test methods need to be developed to manage the cost scaling.

5. Increasing memory sizes result in increasing test times (i.e., reduced cell throughput), pushing towards new DFT techniques (e.g., BIST and BISR). Embedded memory technologies (Flash and DRAM) may economically justify extra test insertions. Fundamental research is required to develop methods to maintain the cost per bit learning curve.

6. In addition to massively parallel test, wafer-level burn-in may become an approach of reducing the cost of test for some device types.

TEST AND YIELD LEARNING

In addition to the normal sorting function, test provides the essential feedback loop for understanding the failure mechanisms inherent in deep submicron fabrication processes. Test is the main source of feedback regarding killer defects, unacceptable parametric variations and design-process interactions. Test must continue to support cost-effective defect isolation, process measurements and failure root cause determination.

PHYSICAL FAILURE ANALYSIS

The migration of CMOS technology towards smaller feature sizes and more complex devices will severely challenge the traditional Physical Failure Analysis (PFA) process. The traditional PFA process, comprising the steps of fault localization, deprocessing, and physical characterization/inspection, process will increasingly be too slow and difficult to be relied upon as a routine analysis procedure. Instead, with development in key areas such as software-based defect localization and signature analysis as described below, PFA will move into a sampling/verification role. Nevertheless PFA will remain an important process that needs improvements to existing tools and techniques to keep pace with process technology and, in some cases, requires new breakthrough techniques. Gaps in PFA capability generated by the progress in technology and device complexity are detailed in the following prioritized list.

1. *Circuit probing*—Characterization of circuit components within a failed device has historically been performed by contact probe. While Focused Ion Beam (FIB) probe pads are a possible solution, the ability to create probe pads without altering circuit characteristics is not clear. Contact probing without FIB pads is limited by the need for accurate placement and the required proximity of probes. In general the worst case can be characterized by the need to place four probes in a single SRAM cell.
2. *Metal stack failure isolation*—Physical isolation of failures in the metallization structure of a device is complicated by the growing number of levels of metal. Heating laser probe techniques, such as TIVA and OBIRCH, are the most common techniques for isolating metal stack defects. Such techniques are limited by the ability of the laser to penetrate the metal stack more than three to four levels and by the spreading of heating within the stack. These limitations can lead to a degradation of spatial resolution. While a strategy of accessing the chip from both topside and backside could improve the situation, such a strategy may not be practical, particularly for flip chip structures.

3. *FIB editing*—The ability to perform FIB edits of circuits to support prototypes and reduce the number of design revisions is limited by the required spatial resolution and aspect ratio of the holes. In addition, the ability to perform edits on emerging new materials is unproven.
4. *Vertical imaging resolution*—Vertical resolution in imaging defects is a growing concern as the number of metal layers increases. The combination of deprocessing and cross section analysis has historically provided access to defects. As "killer defects" become smaller and aspect ratio increases, more three-dimensional approaches to imaging areas of the integrated circuit are needed to improve resolution rates and reduce physical analysis time. Since the spatial resolution of defect localization and imaging technology are not scaling with the silicon technology, it is becoming increasingly difficult to match imaging technologies with the isolated defect efficiently.
5. *Handling new materials*—New materials pose a number of issues for failure analysis. These include sample preparation issues, FIB edits and cross sections, electron beam imaging and interactions with the various failure analysis tools. Each new material requires development across a broad spectrum of failure analysis capabilities.
6. *Waveform acquisition*—The applicability of device waveform acquisition technologies must be re-evaluated for each technology node. Single point PICA analysis is the leading candidate for future technology nodes but there remain concerns over the device physics of light generation at transitions and the range of possible photon detectors.

In addition to technology concerns, several additional concerns for failure analysis also exist. The development of new capabilities for failure analysis has become increasingly expensive and high-risk with each process generation. Typical tool costs are increasing and tend to be less globally deployed than in the past, which reduces the total accessible market for a given failure analysis tool and therefore makes investment in failure analysis tool development less attractive financially. There is a need for consortium inputs to the failure analysis tool manufacturers to help reduce the risk of unsuccessful failure analysis tool introductions. Further, as toolsets are less globally deployed and failure analysis becomes more expensive, reevaluation of the value proposition for failure analysis will be more scrutinized and the number of parts going through the process will likely decrease.

SOFTWARE-BASED DIAGNOSIS AND SIGNATURE ANALYSIS

As challenges to PFA become more severe, alternatives are needed. A key alternative/supplement to traditional hardware-based fault localization is software-based fault localization. Software-based fault localization methodologies and tools are needed to handle diagnostics for fails detected by all major test methodologies, including scan-based and BIST-based test; functional; IDDQ and, especially important, AC (delay) test. Localizing faults in embedded or stand-alone memories, a relatively easy task, is no longer sufficient given the lack of dense upper level metal and the fact that microprocessors have taken the place of RAMs as technology leaders. The tools must handle all realistic physical defects, including resistive bridges, resistive contacts/vias and opens. Methods to diagnose problems related to parametric (non-defect) and reliability failures, must also be developed. DFT techniques such as BIST must be designed with special consideration to support the necessary data gathering. IDDQ measurement devices need to support the accuracy levels required by diagnostics. Tester response data capture capabilities and data management systems must meet the demands of these methodologies. Specifically, ATE should allow for unlimited collecting of scan data at the model scan vector rates predicted in Table 23 for DFT testers. Diagnostic data collection allowing localization to a single or few failing net candidates should not add significantly to overall test time.

The tools and methodologies should support several levels of software-based diagnosis:

1. Production-worthy data collection, trading off resolution against test cost overhead. Concerns may include test data compression and BIST approaches. An absolute minimum requirement is failing core identification. Average test time overhead should be less than 1%.
2. Extensive data gathering on selected engineering or monitor wafers or lots. Granularity must be sufficient to build accurate fault type Paretos and support tool commonality analysis. Throughput time must be short enough to provide timely feedback to the fabrication process on sufficient volume and must support both time-zero and reliability failures. Tools should identify not just failing nets, but failing layers. Such analysis may involve integrating layout information and/or in-line test results into fault localization. Typical test time should be on the order of seconds.
3. Individual die analysis that identifies defects to a single transistor or section of conductor no longer than 10 µm and identifies the failing layer. Such analysis may involve special-purpose diagnostic-resolution-enhancing ATPG and fail data collection and/or analog re-simulation and may be followed-up by failure analysis. Analysis time may be considerably longer than in the previous two cases.

Hardware-based fault localization tools may be used to complement and supplement those above as appropriate. The spatial resolution of these techniques is predominantly fixed at about 0.5µm by the near infrared light used for imaging

and overlay (e.g., timing-resolved emission, emission microscopy, laser probing and Thermally-Induced Voltage Alteration [TIVA], etc.). Since no other method exists for backside imaging, this constraint must be dealt with by integrating hardware based fault isolation tools with improved computer aided design (CAD) capability for overlay and signal tracing. CAD navigation must be both spatial and time-based, i.e., linked to simulation waveforms.

Finally, signature analysis techniques are expected to be developed to significantly reduce or eliminate the need for physical failure analysis. Statistical methods are needed to select failing die of a particular class to accurately pre-sort and prioritize input to physical failure analysis. Data management strategies are required to collect consistent data across multiple products containing the same design cores. In the longer term, methods must be developed to identify root cause based on test information without resorting to physical failure analysis. A key enabling technology is characterization test methods that are capable of distinguishing individual defect types. Integration of electrical characterization with layout data and test-structure/in-line test results are also key capabilities.

DEFECTS AND FAILURE MECHANISMS

The industry faces new manufacturing-imperfection-related test and yield-learning challenges that result from changing processing technology, changing circuit sensitivities and modeling limitations.

1. Process technology advancements are changing the population of physical defects that affect circuit functionality. For example, smaller or higher aspect-ratio vias are more susceptible to incomplete etch, which may lead to a greater prevalence of resistive vias. Similarly, the change from subtractive aluminum processes to damascene Cu may cause a decrease in particle-related blocked-etch metal shorts in favor of an increase in particle-related blocked-deposition metal opens. In addition, the introduction with Cu interconnects of a liner metal that can remain intact when a line open occurs may increase the occurrence of resistive line opens. The introduction of low-κ dielectrics may lead to an increase in the occurrence of possibly latent, resistive bridges and smaller transistors may increase the importance of degradation mechanisms, such as Negative Bias Temperature Instability (NBTI).
2. Changing circuit sensitivities are likely to make defects that were benign in the past become killer defects in the future. For example, shorter clock cycles mean defects that cause 10's or 100's of picoseconds of delay are more likely to cause circuit failures. Furthermore power-optimized and/or synthesized designs will result in fewer paths with significant timing margin, which implies that random delay-causing defects will be more likely to cause failure. Similarly increasing noise effects, such as crosstalk and power/GND bounce decrease noise and timing margins and again increase circuit susceptibility to defects.
3. Finally, modeling complexity threatens the ability of EDA/design to ensure the circuit's functionality under all process conditions, which may result in circuits with subtle parametric failure modes reaching the test floor.

All aspects of the test process, including fault modeling, test generation, test coverage evaluation, DFT solutions, test application and diagnosis, must handle these realistic and changing populations of manufacturing imperfections. New classes of defects may not be detectable using traditional test methods for some products; for example, small delay defects for ASICs. Promising strategies include realistic defect-based fault modeling, out-of-spec testing such as low-VDD or temperature, defect-oriented test generation such as that based on inductive fault analysis, statistical methods, and techniques to allow continued use of IDDQ. To ensure these and other techniques are accurately targeted and effective, high-fidelity information about the occurrence and properties of the population of manufacturing imperfections will be needed, therefore methods for understanding and characterizing the defects must be developed.

AUTOMATED TEST PROGRAM GENERATION

Correct by construction test programs and patterns have long eluded test development teams. Increasing design complexity and demands on team productivity require significant improvement in test program generation automation to limit or reduce time to market impact. The Electronic Design Automation (EDA) industry has developed and deployed many tools that are intended to aid the entire process of test development, content creation, and equipment translation. However, device makers seldom have a homogeneous environment provided by a single EDA supplier and the general lack of interoperability standards among tools create significant challenges and effort by the device maker to enable automation. Cooperation among EDA and test equipment suppliers is increasing, a focus on tool interface and interoperability standards is growing—the challenges increase with every process generation and related growth in design integration.

To achieve full test program generation automation will require increased standardization of the test equipment software environment itself. Historically each equipment supplier has taken a holistic and proprietary approach to definition and

development of their specific software environment. Similar to EDA, most device makers do not have a homogeneous test environment of equipment provided by a single supplier. Increased standardization of the test equipment software environment (where appropriate) would lower the barrier of entry for suppliers as well as simplify the porting of test content between platforms as required by the device maker.

Today's environment of platform-unique supplier software solutions and home-grown tools for equipment programming, automation, and customization will drive unacceptable growth in test development engineering and factory integration effort. Automation of common tasks and decreasing test platform integration time demand a focus on standards to enable more efficient use of resources in line with shrinking product development lifecycles. New tool development must comprehend the end use to ensure that the resulting effort is indeed reduced over existing methods and that tool throughput gains are not eliminated by pre and post-processing of data.

MODELING AND SIMULATION

Time to market can define the success or failure of a product. Device debug can contribute significantly to the time required to deliver a product to a customer, making this a critical path item from a schedule perspective. Flawless execution throughout this effort requires thorough preparation pre-silicon to minimize surprises and ensure correctness of test content and interfaces. Pre-silicon electrical modeling of the device test environment is a fundamental requirement for high power and high interface speed devices.

Electrical models of the entire power and signal delivery paths must be available months ahead of first silicon availability to enable test interface board design and manufacture. High power devices require careful attention to power path layout and power supply performance to minimize parasitics and maximize response bandwidth. Devices with high frequency interfaces are extremely sensitive to losses due to loading, impedance discontinuities, and interconnect material properties making electrical modeling critical to the material selection and interconnect design. Complex simulation capability is needed to allow optimization of interface layout routing and geometries versus instrument location and path performance. Simulations require detailed models of the test equipment instrument, electrical delivery path, probe card or loadboard and contactor, and the DUT. Such simulations are needed to guarantee signal and power performance at the die.

Equipment suppliers must include electrical modeling and model validation in the fundamental requirements set for all future power supply and pin electronics development programs. In many cases it is necessary to deliver prototype electrical models ahead of actual test instrument availability to ensure compatibility with the test environment.

Table 23a Test and Test Equipment Difficult Challenges—Near-term

Five Difficult Challenges ≥45 nm/Through 2010	*Summary of Issues*
High-speed Device Interfaces	A major roadblock will be the need for high frequency, high pin count probes and test sockets; research and development is urgently required to enable cost-effective solutions with reduced parasitic impedance. High-speed serial interface speed and port count trends will continue to drive high-speed analog source/capture and jitter analysis instrument capability for characterization. DFT/DFM techniques must be developed for manufacturing. Device interface circuitry must not degrade equipment bandwidth and accuracy, or introduce noise, especially for high-frequency differential I/O and analog circuits.
Highly Integrated Designs	Highly structured DFT approaches are required to enable test access to embedded cores. Individual cores require special attention when using DFT and BIST to enable test. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever-increasing instrument capability trends. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits. DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Reliability Screens	Existing methodologies are limited (burn-in versus thermal runaway, IDDQ versus background current increases). Research is required to identify novel infant mortality defect acceleration stress conditions
Manufacturing Test Cost	Test cell throughput enhancements are needed to reduce manufacturing test cost. Opportunities include massively parallel test, wafer-level test, wafer-level burn-in, and others. Challenges include device interfacing/contacting, power and thermal management. Device test needs must be managed through DFT to enable low-cost manufacturing test solutions; including reduced pin count test, equipment reuse, and reduced test time. Automatic test program generators are needed to reduce test development time. Test standards are required to enable test content reuse and manufacturing agility.
Modeling and Simulation	Logic and timing accurate simulation of the ATE, device interface, and DUT is needed to enable pre-silicon test development and minimize costly post-silicon test content development/debug on expensive ATE. High-performance digital and analog I/O and power requirements require significant improvements to test environment simulation capability to ensure signal accuracy and power quality at the die. Equipment suppliers must provide accurate simulation models for pin electronics, power supplies, and device interfaces to enable interface design.

Table 23b Test and Test Equipment Difficult Challenges—Long-term

Five Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
DUT to ATE interface	Probing capability for optical and other disruptive technologies Support for massively parallel test—including full wafer contacting Decreasing die size and increasing circuit density are driving dramatic increases in die thermal density. This problem is further magnified by the desire to enable parallel test to maximize manufacturing throughput. New thermal control techniques will be needed for wafer probe and component test. DFT to enable test of device pins not contacted by the interface and test equipment.
Test Methodologies	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends Logic BIST techniques must evolve to support new fault models, failure analysis, and deterministic test. EDA tools for DFT insertion must support DFT selection with considerations for functionality, coverage, cost, circuit performance and ATPG performance.
Defect Analysis	Defect types and behavior will continue to evolve with advances in fabrication process technology. Fundamental research in existing and novel fault models to address emerging defects will be required. Significant advances in EDA tools for ATPG capacity and performance for advanced fault models and DFT insertion are required to improve efficiency and reduce design complexities associated with test.
Failure Analysis	Realtime analysis of defects in multi-layer metal processes is needed. Failure analysis methods for analog devices must be developed and automated. Transition from a destructive physical inspection process to a primarily non-destructive diagnostic capability. Characterization capabilities must identify, locate, and distinguish individual defect types.
Disruptive Device Technologies	Develop new test methods for MEMS and sensors. Develop new fault models for advanced/disruptive transistor structures.

TEST TECHNOLOGY REQUIREMENTS

SYSTEM ON CHIP

This section is intended to discuss the test challenges associated with integration of multiple technologies on a single System-on-Chip (SOC) device. The challenges of the particular technologies themselves are covered in subsequent sections.

A System on Chip (SOC) design consists of many individual design blocks, or cores. This implies a diversity of test requirements to manage the specific features of each embedded core and its related technology (logic, memory, analog). SOC test must include the appropriate combination of these test methods associated with individual cores, core access techniques, and full-chip testing methods.

SOC test is highly dependent on a highly structured DFT methodology to enable observability and controllability of individual cores. Increasingly, SOC design will rely on a database of pre-existing IP cores that encapsulate the design itself, interfaces to other blocks, and test.

A fundamental challenge of SOC test is the need to combine test requirements from multiple sources with differing testability approaches and methods. Opportunities exist to define standards for test to conform to a hierarchical methodology; these standards are most easily imposed on internally designed cores. However, when IP is purchased or licensed from a third party, it is typically the test methodology that must adapt. Many EDA tools already leverage a standard format for logic designs; this standard must be extended to other core types, such as analog circuits.

In addition to SRAM/DRAM BIST widely used today, BIST techniques for embedded non-volatile memory devices, such as Flash, MRAM and FeRAM, should be developed. With the increase in the size of embedded memories, Built-In Self-Repair (BISR) techniques will be essential.

Cost effective test of analog cores is a critical issue. Analog BIST techniques provide a potential solution but are not mature enough for general use. Failure analysis techniques for analog cores must be developed.

Structured use of IP core wrappers and test access mechanisms must be developed for testing of individual cores within a SOC. These should be developed carefully to enable functional, at-speed, parametric and interconnect testing. Furthermore these methods should be standardized with the interface language for interoperability of EDA tools. One such effort is the Core Test Language (CTL) development within the IEEE P1500 standard. The high complexity of SOC design creates design and test throughput and test quality challenges. EDA tools must be developed to aid management of this complexity.

Table 24a System on Chip Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100nm*	*90nm*	*80nm*	*70nm*	*65nm*	*57nm*	*50nm*
Embedded Cores							
Standardization of core test data [1]	Standard format on EDA/ATE	Standard format on EDA/ATE	Standard format on EDA/ATE	Extension to analog cores	Extension to analog cores	Extension to analog cores	Extension to analog cores
Embedded Cores: Logic							
Test logic insertion at RTL design	Partially	Partially	Fully	Fully	Fully	Fully	Fully
Testability analysis and overhead estimation at RTL design	Ad hoc	Fully	Fully	Fully	Fully	Fully	Fully
BIST for logic cores	Yes [2]	Yes [2]	Yes [2]	Yes [2]	Yes [2]	Yes [2]	Yes [2]
BISR for logic cores	Minimal	Minimal	Minimal	Some	Some	Some	Some
Embedded Cores: Memory							
Embedded non-volatile memory BIST	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Embedded memory BIST (redundant configuration, self hard repair) [3]	Partially BISR	Partially BISR	Partially BISR	Partially BISR	BISR	BISR	BISR
Embedded memory BIST (redundant configuration, self soft repair) [4]	Partially BISR	Partially BISR	BISR	BISR	BISR	BISR	BISR
Embedded Cores: Analog							
BIST for analog cores	Restricted use (PLL, ADC, etc.)	Limited use (PLL, ADC, etc.)	Limited use (PLL, ADC, etc.)	Full use	Full use	Full use	Full use
Failure analysis for analog cores	No	No	No	Yes	Yes	Yes	Yes
Core Access							
Standardization of test interface [5]	Standard interface on IP core	Standard interface on IP core/EDA [6]	Standard interface on IP core/EDA [6]	Standard interface on IP core/EDA [6]	Standard interface on IP core/EDA [6]	Standard interface on IP core/EDA [6]	Standard interface on IP core/ EDA [6]
Analog-mixed signal core access	Direct access	Analog wrapper [7]	Analog wrapper [7]	Standard analog wrapper [7]	Standard analog wrapper [7]	Standard analog wrapper [7]	Standard analog wrapper [7]
SoC Level Testing							
Test strategy for IP core-based design (test control integration, test scheduling for low power consumption, test time reduction and test pin reduction)	Partially automated	Partially automated	Fully automated	Fully automated	Fully automated	Fully automated	Fully automated
DFT selection for cores	DFT selection for cores	DFT selection for cores	DFT selection for cores/fully automated EDA tool	DFT selection for cores/fully automated EDA tool	DFT selection for cores/fully automated EDA tool	DFT selection for cores/fully automated EDA tool	DFT selection for cores/fully automated EDA tool
DFT at higher level design (behavior level, HW/SW co-design, high level synthesis with testability analysis)	No	No	Yes	Yes	Yes	Yes	Yes
Fault model for SoC level fault coverage [8]	Single stuck-at fault model/ transition	Standard fault models	Standard fault models	New standard fault model, its coverage	New standard fault model, its coverage	New standard fault model, its coverage	New standard fault model, its coverage
Manufacturing							
Diagnosis interface/data [9]	Standard format and methods on IP core	Standard format and methods on IP core	Standard format and methods on IP core	Standard format and methods on IP core	Automated SOC diagnosis	Automated SOC diagnosis	Automated SOC diagnosis

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

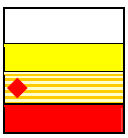
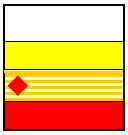


Table 24b System on Chip Test Requirements—Long-term

Year of Production	*2012 32nm*	*2015 22nm*	*2018 16nm*
Embedded Cores			
Standardization of core test data [1]	Extension to Analog Cores	Extension to Analog Cores	Extension to Analog Cores
Embedded Cores: Logic			
Test logic insertion at RTL design	Fully	Fully	Fully
Testability analysis and overhead estimation at RTL design	Fully	Fully	Fully
BIST for logic cores	Yes [2]	Yes [2]	Yes [2]
BISR for logic cores	Logic BISR	Logic BISR	Logic BISR
Embedded Cores: Memory			
Embedded non-volatile memory BIST	Yes	Yes	Yes
Embedded memory BIST (redundant configuration, self hard repair) [3]	Yes	Yes	Yes
Embedded memory BIST (redundant configuration, self soft repair) [4]	Yes	Yes	Yes
Embedded Cores: Analog			
BIST for analog cores	Full use	Full use	Full use
Failure analysis for analog circuits	Yes	Yes	Yes
Core Access			
Standardization of test interface [5]	Standard interface on IP core/ EDA [6]	Standard interface on IP core/ EDA [6]	Standard interface on IP core/ EDA [6]
Analog/mixed-signal core access	Standard analog wrapper [7]	Standard analog wrapper [7]	Standard analog wrapper [7]
SoC Level Testing			
Test strategy for IP core-based design (test control integration, test scheduling for low power consumption, test time reduction and test pin reduction)	Fully automated	Fully automated	Fully automated
DFT selection for cores	DFT selection for cores/ fully automated EDA tool	DFT selection for cores/ fully automated EDA tool	DFT selection for cores/ fully automated EDA tool
DFT at higher level design (behavior level, HW/SW co-design, high level synthesis with testability analysis)	Yes	Yes	Yes
Fault model for SoC level fault coverage [8]	New standard fault model, its coverage	New standard fault model, its coverage	New standard fault model, its coverage
Manufacturing			
Diagnosis interface/data [9]	Automated SOC diagnosis	Automated SOC diagnosis	Automated SOC diagnosis



Definitions for Tables 24a and 24b:
[1] The standardization of test data format needs to reduce turn-around-time of test program development
[2] High fault coverage, at-speed test on system operation, test time restraint, low power, low area overhead
[3] Electric fuse such as a kind of non-volatile memory would be used to store the repair code for BISR
[4] After BIST and BISA at power-on time, repair code would be stored in the register
[5] Standardization of core wrapper, test access mechanism, and the interface language, e.g., IEEE P1500 and 1450.6 CTL
[6] EDA tools handle the standard test interface to translate core test patterns to chip-level, assemble chip-level test logic, etc.
[7] Extended wrapper structure to access to embedded analog-MS cores, not chip-level analog boundary-scan
[8] The standardization of fault model and fault coverage needs to popularize IP Cores
[9] The standardization of diagnosis data format and interface needs to reduce turn-around-time of failure analysis

GIGAHERTZ HIGH FREQUENCY DIFFERENTIAL LINK

High frequency I/O technology continues to expand beyond the original transceiver applications for telecomm. Serial I/O interfaces are being widely adopted into back plane applications, short and long-haul communications, and chip-to-chip links for computing applications. New industrial standards emerging recently include new introductions from consortiums and further evolution of existing standards. For example, in telecom applications, SONET is going from 2.5Gbps to 10/40Gbps, fiber channel is going from 1.0625G/2.125Gbps to 4.25Gbps, and Ethernet going from 100 Mbps to 1Gbps and 10Gbps. In computing applications, Serial ATA is ramping quickly from the current 1.5Gbps definition to 3Gbps in 2004, and targeting 6Gbps in 2007. PCI Express is poised to increase from today's 2.5Gbps to 5Gbps in 2006. Even the traditional source-synchronous bus, which is approaching to its practical limit at 2–3Gbps, is now reinventing itself with new clocking schemes to reach 5–8Gbps and beyond. As frequency continues to increase, a convergence of classic parallel bus and classic serial bus clocking schemes will occur and differential signaling will replace single-ended signaling. All of these high-speed differential link present challenges for production test on ATE.

In the past two years, the test and measurement industry has made significant progress in providing high-speed serial link test solutions. Solutions have emerged to provide high-density high-speed test up to 3.2 Gbps. At the present time, testing in the 3.2 Gbps to 12 Gbps range remains in the arena of expensive, stand-alone pattern-generators and bit-error-rate detectors. In some hybrid solutions, such lab instruments are bundled with production testers to address the embedded high-speed serial links in SOC or ASIC designs. The excessive test time and cost of this approach unattractive for high volume production, but this hybrid approach provides leading edge test performance with short time to market, a valuable tool for new product introduction and debug. However this hybrid approach has fundamental limitations that become more obvious as the data-rate goes beyond 3Gbps and bandwidth restrictions for the long cable required to connect these external instruments begin to dominate instrument performance. Integrated instrumentation is physically much closer to the device, improving signal delivery, but requires a much higher integration level than an external instrument. It is likely that this hybrid approach will evolve to integrate the front-end interface to the device into the tester before the full instrument capability. This compromise should effectively alleviate this limitation.

In order to keep the overall system cost down, low cost PCB lamination materials such as FR4 will remain the material of choice for most of the telecomm backplane and computing applications. However, the preference of FR4 creates a bottleneck in spectral bandwidth. Several techniques are being developed to extend the transmission data-rate under this constraint, such as pre-emphasis/de-emphasis, transmit-side equalization/receiver-side adaptive equalization, simultaneous bi-directional signaling, multi-level encoding and phase encoding. All of these techniques, if deployed, would significantly complicate the test requirement for high-speed serial links.

Without proper test methodologies and equipment, many IC manufacturers are forced to use various innovative but limited testing techniques (such as loopback, golden device, and DUT board circuitry), which may compromise fault coverage. This is a potential risk for relatively new IO technologies that are often intentionally designed to push the envelope of the process technology.

In the near term there is an urgent need for ATE manufacturers to design multi-port, gigabit data rate instruments and integrate them into test systems, including control software, to keep up with the rapid progression in speed and port count. This must be done under the consideration that viable solutions need to be cost effective. In the long term, the existing DFT features need to be extended beyond the current traffic generation DFT to provide more performance related parametric coverage. We envision that the DFT/BIST on-chip instrument methodology will co-exist with off chip test instrument. An economically ideal distribution of on-chip and off-chip test coverage is yet to be determined. The goal is to minimize manufacturing test cost and efficiently test high port count devices.

IMPORTANT AREAS OF CONCERN

1. *Data Rate Increase*—In the computing industry, the current 400–1024 MHz source synchronous bus will soon evolve to 1600 MHz and beyond. Between 2003 and 2006, the classical source synchronous bus will gradually be replaced by embedded clock, clock forwarding, and simultaneous bi-directional architectures. These new architectures will break through the 2-3Gbps limit of the classic source synchronous architecture, and bring the maximum computing IO speed up to 1.5Gbps to 8Gbps. This trend seems to coincide with the data rate requirements in the telecom backplane applications of 2.5Gbps to 8Gbps. Because most telecom related backplanes would be limited to the use of low cost FR-4 as PCB lamination material, the data rate will stay below 10Gbps at least until 2010. On the other hand the telecom long haul and short haul transceivers will continue to lead serial link technology to higher data rates. The current 10Gbps long haul applications are moving to CMOS for lower cost and higher integration. Long-haul 40Gbps may not see appreciable market demand until 2010.

2. *Port Count Increase*—Low voltage CMOS technologies and low output voltage swings enable massive integration into large ASICs and SOCs. Currently in 2003, 20~80 pairs of 1~3Gbps backplane SerDes designs are being produced by many IC makers. This port-count will exceed 200 pairs by 2005, while the source synchronous bus will exceed 240 ports around 2005. With such a high port count, the traditional rack-and-stack approach with lab instruments becomes impractical. A multi port ATE solution is required to handle the increasing number of serial ports on a single device. Solutions are beginning to emerge, but significant work is needed to reduce cost and enhance functionality.
3. *Cost Factor*—Traditionally most multi-gigabit transceivers were designed as high-performance, high-priced, and high-margin devices with a low level of integration and relatively low production volume. With the introduction of low cost, low power CMOS macro cells, gigabit transceivers have become valued additions to many high-volume and low priced (even commodity) devices. In addition to high port count, a cost efficient test solution that can test all serial ports concurrently is essential for production. The constant trade-off between performance and integration level results in the separation of SerDes devices into two categories: high-performance-level serial transceivers, and high-integration-level gigahertz link macro-cells. The economics of high-performance long haul communication related products typically allow a more traditional, instrument based test approach or a hybrid tester as discussed earlier. Although reliable DFT features or other low cost test techniques are the ultimate solution for large port count SerDes, there is still a strong desire that the tester can provide at-speed stimulus and captures before a product becomes mature. With the accelerating technology improvements, the life cycles for most products are become much shorter, therefore it may become increasingly difficult to verify and optimize a DFT circuitry.
4. *Jitter Decomposition Measurement*—The jitter generated by a transmitter is the key parameter to guarantee transmitter quality. Currently, jitter measurement capability on ATE is in its infancy, there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth and test time requirements for high performance interfaces. More and more serial link standards adopt the concept of separating jitter into deterministic jitter (DJ) and random jitter (RJ). The old concept of histogram based peak-to-peak jitter has been replaced by the concept of total jitter (TJ) that is associated with a certain bit-error-rate for the serial link (typically 10-12). For the dominant 3.2Gbps data rate in 2003, it is normal for a 3.2Gbps SerDes to have a total jitter (TJ) lower than 30ps, which requires instruments to decompose it into RJ of less than 2ps-rms and DJ of less than 10ps-pk-pk. Because a digital signal of 3.2Gbps has a frequency spectrum up to 8~10GHz, associated jitter measurement instruments must provide this analog bandwidth to avoid adding erroneous data-dependent jitter to the measurement. Most existing instruments for jitter measurements take more than 20 seconds to capture jitter from a high-speed data stream. Although it is faster to measure jitter based on the device clock, many of these designs do not provide direct access to the internal clock. In that case, jitter can only be measured from the data stream. Although many jitter decomposition techniques have been introduced in the last two years by various companies, few are reliable beyond the 2.5~3.2Gbps range. Even between the few, correlation is hard to achieve.
5. *Jitter Tolerance Test*—Jitter Tolerance measures the level of jitter on the input signal that the receiver can tolerate before communication quality, in terms of bit-error-rate (BER), is degraded. This is a key specification for receiver (Rx) noise immunity. To conduct a jitter tolerance test, jitter must be deliberately injected into the data stream in a controlled fashion. Currently, there are few integrated ATE solutions that have this capability in the speed range required by today's high performance designs. The recent trend of separating jitter into deterministic jitter (DJ) and random jitter (RJ) also applies to the jitter tolerance test. Integrated instruments that can inject more than one type of jitter do not exist in either the ATE world nor the lab equipment world, although they are starting to appear on test equipment suppliers' roadmaps (however gaps remain between the standard definition and the instrument's capability). Today some indirect measurement techniques are more practical for cost effective manufacturing test until low cost and integrated instruments becomes available to test jitter to the specs as they are defined.
6. *Test Fixture Bandwidth*—The test fixture used to interface the device to the instruments/ATE includes a printed circuit board, cable, connectors, etc… With increasing frequency and port count, the ability to deliver the high frequency signals to the instrument without significant loss and distortion becomes a monumental task in the test environment. Once the signal goes beyond 10Gbps, the fixture bandwidth requirement reaches 20GHz. Although, it is possible to implement this for a few lines, it is an area of fundamental research to route several hundred such interconnect. Integration of the front-end DUT interface into the ATE test head will alleviate this problem. The socket and wafer probe are also considerable bandwidth bottlenecks for multi-gigahertz testing, where additional R&D is needed. Therefore, a DFT approach to measure the jitter on chip is preferred and must be developed for the multi-gigabit domain.
7. *Synchronization*—Most receivers in serial communication use clock and data recovery circuits (CDR) to extract the clock from a data stream. The phase of the recovered data is not necessarily fixed from device to device, or even from one reset to the next. Highly flexible timing and clocking schemes are required to accommodate this latency

variation by conducting phase alignment and frame alignment. In this area, there has been some progress made recently on ATE.

8. *Parametric DFT vs. logic DFT*—Classically only basic functional DFT circuits are implemented for SerDes modules. On-chip BIST mainly consists of a built-in Pseudo-Random-Bit-Sequence (PRBS) generator and a bit-error (BER) checker. These, however, only provide functional coverage, without parametric test capabilities (such as input and output jitter and voltage levels). BIST circuits for jitter and level tests are still in the research stage. Therefore instruments remain the only solution to test these parameters in the near future.
9. *Advanced signal shaping and encoding*—The adoption of more sophisticated analog techniques such as pre-emphasis, equalization, PAM-x multilevel encoding and phase encoding could potentially lead the test requirement to a somewhat traditional analog test solution, but much higher in frequency. Although pre-emphasis and equalization are now becoming more popular, it is still not clear when multi-level coding will replace the predominant binary coding in this area.

Table 25a Gigahertz High Frequency Differential Link Test Requirements—Near-Term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
High–performance-level Serial Transceivers							
Serial data rate (Gbits/s)	**10**	**10**	**10**	**10**	**40**	**40**	**40**
High-integration-level Backplane and Computer I/O							
Serial data rate (Gbits/s) at Production	**2.5**	**3.2**	**4.25**	**6**	**8**	**10**	**10**
Introduction	**3.2**	**4.25**	**6**	**8**	**10**	**10**	**10**
Maximum port count at Production frequencies	**80**	**200**	**200**	**200**	**200**	**200**	**200**
at Introduction frequencies	**80**	**20**	**20**	**20**	**20**	**20**	**20**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

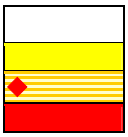
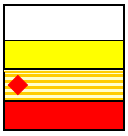


Table 25b Gigahertz High Frequency Differential Link Test Requirements—Long-Term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
High–performance-level Serial Transceivers						
Serial data rate (Gbits/s)	40	40	40	40	160	160
High-integration-level Backplane And Computer I/O						
Serial data rate (Gbits/s)	10	10	10	40	40	40
Maximum port count	200	200	200	50	100	200

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



HIGH-PERFORMANCE ASIC TEST REQUIREMENTS

High-performance ASIC test requirements, Tables 26a and b, illustrate the demands that automatic test equipment (ATE) manufacturers must meet in terms such as pin count and frequencies in order to test the digital portions of today's ASICs. It is unlikely that ATE will ever be required to meet all of these demands on all pins simultaneously. For example, the highest off-chip data frequencies will probably occur on a relatively small number of high frequency serial interfaces operating at 1.25, 2.5, 10, or 40 GHz rates, while the majority of device pins will operate at the lower frequencies shown in the tables. It is expected that integration of high-frequency serial differential I/O buffers will result in a slowing of the device pin count growth trend to approximately 3000 by the year 2016.

The off-chip frequencies shown in the tables are for signal pins other than the high-frequency serial interface pins. For example, data may enter the ASIC on a broad bus at 156 Mbps, and exit on a narrow bus at 2.5 Gbps.

The number of externally stored, non-scan test vectors has not been shown. This number is typically around 32 M in 2001, and could climb toward 1000 M in the future if not constrained. Since external high-speed memory for test vectors can greatly increase the cost of ATE and result in manufacturing cell throughput reduction due to long vector load times, there is an urgent need for DUT designs incorporating DFT and BIST in the near future. This has been incorporated in the DFT tester section. It is expected that vector compression and signature methodologies that have emerged over the past 2 years will place reasonable limit on the demand for vector memory for scan test.

High-frequency clocks are often generated on-chip using phase-locked-loop (PLL) oscillators. These are stimulated by clock signals from the ATE at much lower frequencies, but are required to have very low jitter. Typically a special tester clock pin is needed to provide jitter on the order of 10 ps RMS with an accuracy of ±20 ppm for SONET, and ±100 ppm for other serial communications systems.

Today's ASICs are rapidly transforming into SOC designs that incorporate intellectual property (IP) such as memories and analog circuits. Therefore the test requirements contained in Tables 26a and b should be combined with the mixed-signal and memory test and high frequency serial requirements when determining ATE requirements. This section outlines the logic test challenges while the SOC section above considers the non-logic and integration challenges of SOC.

Table 26a High-performance ASIC Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Off-chip data freq. MHz NRZ (see note).	**1000**	**1100**	**1200**	**1300**	**1400**	**1400**	**1500**
Overall timing accuracy (% period)	**±5**	**± 5**	**±5**	**±5**	**±5**	**±5**	**±5**
Special clock pin RMS jitter ps	**5**	**5**	**5**	**5**	**4**	**4**	**3**
Signal pk-pk range V	**0.9–3.3**	**0.9–2.5**	**0.8–2.5**	**0.7–2.5**	**0.6–2.4**	**0.6–2.4**	**0.6–2.4**
Power/device. DC with heat sink W	**150**	**160**	**170**	**170**	**170**	**170**	**180**
Maximum number of I/O signal pads. *Power and ground could double the number of pads for wafer test.*	**1700**	**1800**	**2000**	**2100**	**2200**	**2200**	**2300**

Table 26b High-performance ASIC Test Requirements—Long-term

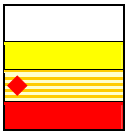
Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Off-chip data freq. MHz NRZ (see note).	**1500**	**1500**	**1800**	**1800**	**2000**	**2000**
Overall timing accuracy (% period)	**±5**	**±5**	**±5**	**±5**	**±5**	**±5**
Special clock pin. RMS jitter ps	**2**	**2**	**2**	**2**	**2**	**2**
Signal pk-pk range V	**0.6–2.5**	**0.6–2.5**	**0.6–2.6**	**0.6–2.6**	**0.6–2.7**	**0.6–2.7**
Power/device. DC with heat sink W	**180**	**180**	**190**	**190**	**200**	**200**
Maximum number of I/O signal pads. *Power and ground could double the number of pads for wafer test.*	**2400**	**2500**	**2700**	**2800**	**3000**	**3100**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



HIGH-PERFORMANCE MICROPROCESSOR TEST REQUIREMENTS

With the focus to shift microprocessor test content from a pure at-speed functional test approach to a more diverse test suite encompassing DFT and BIST techniques many of the traditional manufacturing test challenges are changing. Traditional challenges such as data rate and timing accuracy are being replaced by characteristics like test data volume and power and thermal management. This is not to say that the traditional challenges associated with scaling of at-speed functional test are going away, but rather that there is a shifting emphasis on these parameters to the post-silicon device debug and validation environment. DFT methods have begun to minimize the impact of key test limitations associated with tester data rate and accuracy scaling.

As a result, the microprocessor trends shown in Tables 27a and b more accurately reflect post-silicon efforts than manufacturing need. Manufacturing challenges associated with DFT methodologies are covered in the DFT tester section.

This basic shift in test methods will have a dramatic impact on the industry over the near term. It is not clear today how the leading-edge equipment required for post-silicon debug and validation will be economically viable provided increasing development resources and declining equipment demand. However, this segment continues to draft the leading edge I/O data rate requirements and will benefit from capability solutions developed for these challenges in the long haul communication market.

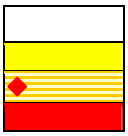
Over the near term it is expected that equipment capability will scale to match device parameters like data rate and power consumption. Timing accuracy requirements will demand new approaches to specification definition and calibration methodologies. It is unclear whether test equipment design innovation will find answers to the nagging issues of timing accuracy and adaptation to emerging interface protocols over the long term. However, it is clear that functional test will not be possible without the intervention of novel technologies as the available timing margin will be overtaken by timing inaccuracies.

Algorithmic Pattern Generator (APG) capabilities are still required for testing of embedded memory on a microprocessor. However with the advent of BIST for most large arrays, APG performance scaling has essentially frozen at 1999 levels even as the total number of embedded memory bits continues to increase.

Significant progress has been made within the last two years to address the growing concerns around power supply bandwidth and dynamic response to current demand transients. Continued research in this area and in alternative methods will be required to address future requirements.

Table 27a High Performance Microprocessor Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Pin count I/O signal channels (maximum pins) [1]	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Pin count power and ground (maximum pins)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**
Busses							
Clock input frequency (MHz) [2]	**1200**	**1200**	**1200**	**1200**	**1200**	**1200**	**1200**
Clock accuracy (ps) [3]	**42**	**42**	**42**	**42**	**42**	**42**	**42**
Off-chip bus data rate (Mbits/s)	**1600**	**2400**	**3200**	**4800**	**6400**	**8000**	**9600**
Accuracy OTA (ps)	**31**	**21**	**16**	**10**	**8**	**6**	**5**
Bi-directional I/O	**Yes**	**Yes**	**Yes**	**Yes**	**No**	**No**	**No**
Uni-directional I/O	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Source synchronous	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Differential	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Self clocked	**No**	**No**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Power Supplies							
High current power supply voltage range (volts) [4]	**0.9–2.0**	**0.9–2.0**	**0.9–2.0**	**0.7–1.8**	**0.7–1.8**	**0.5-1.2**	**0.5-1.2**
Low current power supply voltage range (volts)	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**	**0.7–3.3**	**0.7–3.3**	**0.5-3.3**	**0.5-3.3**
Power supply transient accuracy (% of programmed value AC+DC)	**10**	**10**	**10**	**10**	**10**	**10**	**10**
High current power supply maximum current (A)	**200**	**250**	**300**	**300**	**300**	**300**	**300**
Patterns							
Vector memory (Meg–vectors per pin)	**128**	**256**	**256**	**512**	**512**	**512**	**512**
Vector memory load time (minutes)	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Independent pattern management (# of patterns)	**>1000**	**>1000**	**>1000**	**>1000**	**>1000**	**>1000**	**>1000**



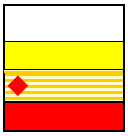
Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 27a and 27b:
[1] Maximum pin count is for debug tester purposes. Debug testers typically utilize the higher pin counts.
[2] Tester should be capable of handling RAMBUS type of date rates and protocols. Characterization testers need to meet full data rate requirements. Production tester accuracy of measurement of "output-to-output" will be critical.
[3] The tester needs to supply the clock as a bypass.
[4] The power supply should be capable of handling 6000 µF, and current switching of 2× maximum current. The circuit can wakeup between 1–20 cycles of the CPU clock.

Table 27b High Performance Microprocessor Test Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Pin count I/O signal channels (maximum pins) [1]	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Pin count power and ground (maximum pins)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**
Busses						
Clock input frequency (MHz) [2]	**1200**	**1200**	**1200**	**1200**	**1200**	**1200**
Clock accuracy (ps) [3]	**42**	**42**	**42**	**42**	**42**	**42**
Off-chip bus data rate (Mbits/s)	**9600**	**12800**	**14400**	**20000**	**21600**	**24800**
Accuracy OTA (ps)	**5**	**4**	**3**	**2**	**2**	**1**
Bi-directional I/O	**No**	**No**	**No**	**No**	**No**	**No**
Uni-directional I/O	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Source synchronous	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Differential	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Self clocked	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Power Supplies						
High current power supply voltage range (volts) [4]	**0.5–1.2**	**0.5–1.2**	**0.5–1.2**	**0.5–1.2**	**0.5–1.2**	**0.5–1.2**
Low current power supply voltage range (volts)	**0.5–3.3**	**0.5–3.3**	**0.5–3.3**	**0.5–3.3**	**0.5–3.3**	**0.5–3.3**
Power supply accuracy (% of programmed value AC+DC)	**10**	**10**	**10**	**10**	**10**	**10**
High current power supply maximum current (A)	**350**	**350**	**400**	**400**	**450**	**450**
Patterns						
Vector memory (meg–vectors per pin)	**1024**	**1024**	**4096**	**4096**	**4096**	**4096**
Vector memory load time (minutes)	**15**	**15**	**15**	**15**	**15**	**15**
Independent pattern management (number of patterns)	**>1000**	**>1000**	**>1000**	**>1000**	**>1000**	**>1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



LOW-END MICROCONTROLLER TEST REQUIREMENTS

Sales of 8-bit microcontrollers continue to thrive in today's market. The need for connectivity in both the wired and wireless arena are continuing to drive the development of many new building blocks for the microcontroller, including USB, TCP/IP, and RF interfaces. Lower flash memory costs are resulting in a move from the traditional mask ROM to integration of flash memory technology. Current applications utilizing microcontrollers include household appliances, entertainment devices, games, motor controllers, and security systems.

The difficult challenges for microcontroller testing continue to be in the area of test cost. The primary method to lower cost requires higher levels of parallelism, resulting in the need for higher pin count testers. Higher levels of parallelism are exposing tester parallel test inefficiencies and have resulted in new line item in the test requirements table, for "parallel test efficiency". Higher levels of parallelism have also accelerated the need for testers beyond the 1024 pin count. Tables 28a and b show only the test characteristics that are unique to testing of microcontrollers.

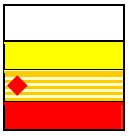
Table 28a Low-end Microcontroller Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Overall timing accuracy (% of period)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
RMS clock jitter (ps)	**75**	**50**	**50**	**50**	**40**	**40**	**40**
External test vectors (M) [1]	**12**	**12**	**12**	**12**	**16**	**16**	**16**
Reliability–MTBF (hrs)	**5000**	**6000**	**7000**	**8000**	**9000**	**9000**	**9000**
DPS maximum voltage (V)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Maximum DPS in tester	**128**	**192**	**192**	**320**	**320**	**768**	**768**
Maximum devices for parallel testing [2]	**96**	**128**	**128**	**256**	**256**	**512**	**512**
Maximum tester pins	**1536**	**2048**	**2048**	**2048**	**2048**	**4096**	**4096**
Parallel test efficiency	**97%**	**99%**	**99.50%**	**99.90%**	**99.90%**	**99.90%**	**99.90%**

Notes for Tables 28a and 28b:
[1] Without BIST or DFT. number will be smaller if acceptable BIST and/or DFT solutions are developed
[2] This category is for parallel testing of microcontrollers, and is not to be confused with parallel testing of memories

Table 28b Low-end Microcontroller Test Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Overall timing accuracy (% of period)	**4**	**4**	**4**	**4**	**3**	**3**
RMS clock jitter (ps)	**40**	**40**	**40**	**30**	**30**	**30**
External test vectors (M) [1]	**16**	**16**	**16**	**32**	**32**	**32**
Reliability–MTBF (hrs)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
DPS maximum voltage (V) [2]	**5**	**5**	**5**	**5**	**5**	**5**
Maximum DPS in tester	**768**	**768**	**768**	**768**	**1024**	**1024**
Maximum devices for parallel testing	**512**	**512**	**768**	**768**	**1024**	**1024**
Maximum tester pins	**4096**	**4096**	**4096**	**4096**	**4096**	**4096**
Parallel test efficiency	**99.9%**	**99.9%**	**99.9%**	**99.9%**	**99.9%**	**99.9%**



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

MIXED-SIGNAL TESTING

The trend toward more system functionality on a single piece of silicon will increasingly blur the lines between traditional digital, analog, RF/microwave and mixed-signal devices. This trend will drive test equipment toward a single platform solution that can test any device structure on a single piece of silicon. Consequently, ATE must be modular and expandable across the entire spectrum from digital-only to the full integration of high performance analog/RF/microwave instruments. The analog test issues and test technology limiters are higher bandwidth, higher arbitrary waveform generator sampling rates, higher dynamic range for RF applications, lower noise floors, and seamless integration of digital and analog instruments. The digital requirements for mixed-signal test equipment are equivalent to those for purely digital chips and are shown in the tables for the associated market segment.

The mixed-signal test equipment requirements in Tables 29a and b focuses on test instruments rather than specific IC device applications. Current Analog/RF/Microwave testing methodologies require performance-based measurements (i.e., using external outside-the-chip instruments); therefore, instrumentation needs reflect the increasing device performance predicted in the process and packaging technology roadmaps. Where appropriate, instrument requirements are linked to Microprocessor, ASIC and Data Communication requirements expressed in other roadmap tables.

The complexity and breadth of applications is also forcing specialized instrument designs focused on a particular device application. Often, more than one complex analog function is integrated in a single design. Instrument designs for ATE are chasing ever-increasing test requirements, especially for arbitrary waveform generators. This complexity increases the number of instruments in a given test system, which increases cost and creates significant configuration-management issues for equipment that must be shared across multiple products. This trend of increasing instrument numbers, complexity, and performance is expected to continue but cannot be allowed to drive up the cost of test.

Analog DFT and BIST techniques are lagging. No proven alternative to performance-based analog testing exists and more research in this area is needed. Analog BIST has been suggested as a possible solution and area for more research. Fundamental research is needed to identify techniques that enable reduction of test instrument complexity or elimination of the need for external instrumentation.

IMPORTANT AREAS OF CONCERN

1. The analog/RF/microwave signal environment seriously complicates load board design and test methodology. Noise, crosstalk, signal mixing, load board design, and ATE software issues will dominate the test development process and schedule.
2. Multi-site parallel test as well as concurrent test of all analog functions is needed to reduce test time, increase manufacturing cell throughput, and reduce test cost. This requires multiple instruments with fast parallel execution of DSP test algorithms (FFTs etc). Parallel test has been used for many years to test Memory and high volume Digital Devices but not to a large enough extent on mixed-signal devices.
3. Better software tools that apply to more than one test equipment vendor are needed. Tools are required for digital and mixed-signal vector generation, circuit simulation of the device's analog circuitry along with the load board and the test instruments, and rapid mixed-signal test program generation. Currently, mixed-signal test programs are manually generated; automatic test program generators are widely used for generating digital test.

Table 29a Mixed-signal Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
BW * (MHz)	**30**	**40**	**50**	**60**	**60**	**60**	**60**
Fs** (MS/s***)	**Moving from Nyquist sample rates to over/under sampling sources/digitizers**						
Resolution (bits)	**DSP computation to 24 bits—noise floor is more important**						
Noise floor (dB/RT Hz)	**-155**	**-155**	**-155**	**-160**	**-160**	**-160**	**-165**
High Frequency Waveform Source							
Level V (pk–pk)	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Accuracy (+/-)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (MHz)	**1250**	**1500**	**1500**	**1800**	**1800**	**2150**	**2150**
Fs (MS/s)	**5000**	**6000**	**6000**	**7200**	**7200**	**8600**	**8600**
Resolution (bits) AWG/Sine†	**8/10**	**8/10**	**8/10**	**8/10**	**8/10**	**8/10**	**8/10**
Noise floor (dB/RT Hz)	**-135**	**-135**	**-135**	**-140**	**-140**	**-140**	**-140**
High Frequency Waveform Digitizer							
Level V (pk–pk)	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Accuracy (+/-)	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (MHz) (undersampled)	**4000**	**5200**	**6400**	**8000**	**9200**	**10800**	**12500**
Fs (MS/s)	**Direct conversion remains at 400—move to under sampling**						
Resolution (bits)	**Minimum 12 bits—noise floor is more important**						
Noise floor (dB/RT Hz)	**-140**	**-140**	**-145**	**-145**	**-150**	**-150**	**-150**
Time Measurement							
Jitter measurement (ps RMS)	**Will be driven by high-speed serial communication ports**						
Frequency measurement (MHz)	**Will be driven by high-performance ASIC clock rates**						
Single shot time capability (ps)	**Will be driven by high-speed serial communication ports**						
RF/Microwave Instrumentation							
Source BW (GHz)	**14**	**14**	**18**	**18**	**18**	**18**	**18**
Accuracy (+/-dB)	**0.2**	**0.2**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
Source phase noise low frequency Close-In 1KHz (dBc/Hz)	**-130**	**-130**	**-136**	**-136**	**-136**	**-136**	**-136**
Source phase noise high frequency Wideband 10MHz (dBc/Hz)	**-160**	**-160**	**-166**	**-166**	**-166**	**-166**	**-166**
Receive BW (GHz)	**14**	**14**	**18**	**18**	**18**	**18**	**18**
Receive noise floor (dBm/Hz)	**-160**	**-166**	**-166**	**-166**	**-166**	**-166**	**-166**
Receive dynamic range SFDR (dBc) ‡	**140**	**140**	**140**	**160**	**160**	**160**	**160**
Special Digital Capabilities							
D/A and A/D digital data rate (MB/s)	**Same as high performance ASIC "off-chip data rate"**						
Sample clock jitter (< ps RMS)	**0.5**	**0.3**	**0.2**	**0.15**	**0.1**	**0.1**	**0.1**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

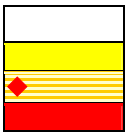


Table 29b Mixed-signal Test Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
BW * (MHz)	**60**	**60**	**60**	**60**	**60**	**60**
Fs** MS/s***	**Moving over/under sampling**					
Resolution (bits)	**Noise floor more important**					
Noise floor (dB/RT Hz)	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**
High Frequency Waveform Source						
Level V (pk–pk)	**4**	**4**	**4**	**4**	**4**	**4**
Accuracy	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (MHz)	**3000**	**3000**	**3000**	**3000**	**5000**	**5000**
Fs (MS/s)	**12000**	**12000**	**12000**	**12000**	**12000**	**15000**
Resolution (bits) AWG/Sine†	**10/14**	**10/14**	**10/14**	**10/14**	**10/14**	**10/14**
Noise floor (dB/RT Hz)	**-155**	**-155**	**-155**	**-155**	**-155**	**-155**
High Frequency Waveform Digitizer						
Level V (pk–pk)	**4**	**4**	**4**	**4**	**4**	**4**
Accuracy	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**	**0.50%**
BW (MHz) (undersampled)	**10000**	**10000**	**10000**	**10000**	**10000**	**10000**
Fs (MS/s)	**Moving to under sampling**					
Resolution (bits)	**14**	**14**	**14**	**14**	**14**	**14**
Noise floor (dB/RT Hz)	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**
Time Measurement						
Jitter measurement (ps RMS)	**Driven by high-speed serial ports**					
Frequency measurement (MHz)	**Driven by ASIC clock rates**					
Single shot time capability (ps)	**Driven by high-speed serial ports**					
RF/Microwave Instrumentation						
Source BW (GHz)	**36**	**36**	**36**	**36**	**36**	**36**
Source phase noise low frequency Close-In 1KHz (dBc/Hz)	**-140**	**-140**	**-140**	**-140**	**-140**	**-140**
Source phase noise high frequency Wideband 10MHz (dBc/Hz)	**-166**	**-166**	**-166**	**-166**	**-166**	**-166**
Receive BW (GHz)	**36**	**36**	**36**	**36**	**36**	**36**
Receive noise floor (dBm/Hz)	**-166**	**-166**	**-166**	**-166**	**-166**	**-166**
Receive dynamic range SFDR (dBc) ‡	**160**	**160**	**160**	**160**	**160**	**160**
Special Digital Capabilities						
D/A and A/D data rate (MB/s) §	**Follows ASIC "off chip data rate"**					
Sample clock jitter (< ps RMS)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**

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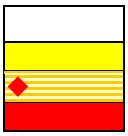

Definitions for Tables 29a and 29b:

Low Frequency Source And Digitizer—This is the basic, minimum, instrument set of any mixed-signal tester. Telecommunications, advanced audio and wireless baseband will drive these specifications. Differential inputs/outputs are needed.

High Frequency Waveform Source—Disk drive read channels (PRML) will drive sample rate and bandwidth. Local area network (LAN) devices will drive sample rate, bit resolution and amplitude accuracy. Differential outputs are needed.

High Frequency Waveform Digitizer—An undersampled (down conversion, track-and-hold, etc) bandwidth is shown. The sample rates and bit resolutions are for a direct conversion digitizer, which is usually preceded by the undersampler. PRML and LAN devices will drive digitizer specifications. Differential inputs are needed.

Time Measurement—Phase Lock Loops (PLLs), which are increasingly being embedded in new designs, will require jitter and frequency measurements. A specialized class of instruments will have to be developed to make these measurements efficiently and accurately.

RF/Microwave Instrumentation—Single chip RF/digital/baseband/audio devices will require RF instruments such as modulated carrier sources and low noise receivers or down converters.

Special Digital Capabilities—For converter testing, the ability to source a digital word to a D/A and capture a digital word from an A/D.

EQUIPMENT FOR TESTING DEVICES DESIGNED WITH DFT

The use of DFT is showing a rapid growth trend across the semiconductor industry. The reasons for this growth are many. DFT can greatly shorten test development cycle times, improve fault coverage, access multiple internal circuits in a SOC through a common subset of pins, test high performance circuits with medium performance interfaces, facilitate massively parallel testing, and more. Except for a few isolated point solutions, most structural (DFT) testing to-date has been performed on conventional digital ATE. This has the unfortunate consequences of exceeding the test requirements in some areas and being sub optimal in others. This means that many devices utilizing DFT are paying a higher cost of test than necessary. Therefore, a need has arisen for the development of specialized ATE, targeted at this "new" class of DFT savvy devices.

Table 30 indicates the industry trends over the next seven years. The data represented is a composite of the projected requirements from various semiconductor manufacturers. There are slightly divergent requirements across the semiconductor industry due to a number of different factors:

1. DFT is still a maturing technology and thus, not consistently implemented across the industry.
2. There are different deployment strategies dependent on device technologies and manufacturing flows.
3. There is a need to support various levels of "legacy" test methodologies for older product families.

Therefore it is important to note that these tables should not be construed as a "specification." It is not expected that any single configuration would satisfy all DFT applications.

Table 30 DFT-BIST Device Test Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009	Driver
Technology Node		hp90			hp65			
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	**57**	**50**	
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	
Number of parallel sites	**64**	**64**	**128**	**128**	**256**	**256**	**256**	Cost
Scan data volume (Giga-pin-vectors available per site)	**32**	**32**	**64**	**64**	**128**	**128**	**256**	Logic Density
Data capture volume (M bits-per-pin)	**64**	**64**	**128**	**128**	**256**	**256**	**256**	Scan/BIST debug
Scan pin (available per site/system)	**384/2K**	**384/2K**	**512/4K**	**512/4K**	**512/4K**	**512/4K**	**512/4K**	Logic Density
Scan vector rate (MT or MHz)	**100**	**200**	**200**	**300**	**300**	**400**	**400**	Test Time
"Full function" pin (available per site/system)	**128/512**	**128/512**	**128/512**	**128/512**	**128/512**	**128/512**	**128/512**	Test Time
Functional vector depth (M-Vectors)	**16**	**16**	**16**	**16**	**16**	**16**	**16**	Logic Density
Functional data rate (MHz)	**100**	**200**	**200**	**200**	**200**	**200**	**200**	Test Time
"Reduced function" pin (available per site/system)(DC only)	**3K/4K**	**4K/5K**	**4K/5K**	**5K/6K**	**5K/6K**	**5K/6K**	**5K/6K**	I/O Density
Clock pins (available per site/system)	**8/64**	**8/64**	**8/128**	**8/128**	**8/256**	**8/256**	**8/256**	Clock Domains
Clock frequency (MHz)	**400**	**600**	**600**	**800**	**800**	**800**	**1000**	On-chip Clock Rate
Scan launch/capture speed (MHz)	**100**	**150**	**200**	**200**	**200**	**250**	**250**	AC Scan
Power supplies (available per site/system)	**8/128**	**8/128**	**8/128**	**8/128**	**8/256**	**8/256**	**8/256**	Logic Density
Support for mixed signal and RF DFT	**LoFreq**	**LoFreq**	**HiFreq**	**HiFreq**	**RF**	**RF**	**RF**	SoC

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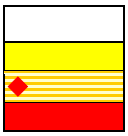


Notes for Table 30:

Parallel Sites—Parallel testing of devices is a common technique for reducing the effective cost of test per device by testing multiple devices with a single tester. The number of devices that can be tested in parallel will be necessarily limited by the tester's available physical resources, however there should be no "logical" limit imposed by the hardware or software architecture. A common concern with these tables in the past has been the total number of pins that seem to be indicated by multiplying all of the numbers together, however this is not the intent. The total number of pins available on a given tester should be consistent with the current state-of-the-art for pin densities.

Scan Data Volume—The total number of bits shifted into the scan input pins plus the total number of bits shifted out of scan output pins. It is the total number of scan-able elements in a device multiplied by the total number of scan-loads plus the scan-unloads. A single bit shifted into a single device pin or shifted out of a single device pin can be defined as pin-vector (a tester architecture neutral unit).

Scan Pin—The maximum number of scan input pins plus scan output pins. This number does not necessarily include the pins required for scan control.

Scan Vector Rate—The maximum shift rate for scan data input pins and scan data output pins (expressed in MegaTransfers per second (MT)).

"Full Function" Pin—Full Function pins are backed by drive and receive resources containing the full functionality of a traditional ATE system pin. These resources may include, but are not necessarily limited to, precision timing accuracy, flexible waveform capability, high vector rates, programmable drive/receive thresholds, parametric measurement capability, etc. These "Full Function" pins are used to test the DUT via a traditional ATE approach utilizing device primary I/O pins which may include, but are not limited to the following functions: clock, input, output, bi-directional, and reference level bias (fixed state controlled by ATE pin electronics). In addition, the full function pins should be capable of scan (either within the limits of "Full Function" pin memory depth or with access to the scan memory).

Functional Vector Depth—The total number of vectors required to test a particular device. In this context, it refers to the total number of individual states (e.g., "0," "1," "H," "L," "X," "Z," etc.) applied to or received from a single device pin.

Functional Data Rate—The maximum rate of application of vectors to the data pins of the device.

"Reduced Function" Pin—Reduced Function pins are backed by low-cost resources containing limited digital drive/receive capability (e.g., static vectors are vectors that remain static for the duration of a particular test or subtest), no waveform capability, very little vector depth, etc. These pins will typically have programmable drive/receive thresholds, and parametric measurement capability.

Clock Pin—These single-ended clock pins function at higher frequencies and higher accuracies than the scan and functional data pins. These clocks are used for functional testing at the functional data rate, as well as, AC scan (shift slow—sample fast) and BIST, to facilitate high performance testing on DFT testers.

Clock Frequency—The maximum frequency attainable from the standard clock source. The accuracy and skew for the clock pins should be maintained to less than or equal to 8% of the minimum clock period and the jitter should be less than or equal to 1.5% of the minimum clock period.

Power Supplies—ATE device power supplies provide programmable voltage (or current) levels during testing. The most typical application is to apply voltage and current to a device's primary power connections such as V_{cc} or V_{dd}. Other uses include reference voltage sources for device pins, termination voltages for external loads, and current sourcing during test. Device power supplies may be used in forcing either current or voltage while measuring the resulting voltage or current. Common feature include programmable clamps, measurement trigger/capture controlled by the tester's pattern generator, and switch-able output voltage ranges controlled by the pattern generator. Supplies should be gang-able for flexibility.

SEMICONDUCTOR MEMORIES TEST REQUIREMENTS

It is expected that memory density will continue to grow at an exponential rate. Semiconductor memories will continue to be the test vehicle for the development of new process technologies. DRAM has historically been the process technology development vehicle but there is some indication that Flash may also be used as the leading device to define the process technology, design and test. Refer to Tables 31 through 33.

COMMODITY DRAM TESTING

DRAM bit density will continue to quadruple every two years in the short-term; however, in the long-term this trend will slow and DRAM bit density will quadruple every three years. Increasing memory size will cause test to become a manufacturing bottleneck due to increasing device test time and decreasing manufacturing cell throughput. Redundancy is necessary for commodity DRAMs. To enhance test productivity, new test-oriented architectures will be required. Multi-bit testing, BIST, and built-in self-repair (BISR) will be essential to maintain the production throughput and yield.

Parallelism in test must continue to scale in both test equipment and wafer probe/component handler capabilities. The number of devices simultaneously tested refers to the packaged devices tested at-speed. Commodity DRAMs will lag the leading edge specialty DRAMs in I/O bit rates. Above 2Gbps, there are significant challenges in signal transmission methods, sockets, probing, and handling. Because of required timing accuracy and test/device interface components, exceeding 64 devices in parallel per test head is a challenge.

The primary fault models for DRAMs will continue to be cell stuck-at, multi-cell coupling, decoder open, and data retention faults. For 100nm feature size and below, in-line defect detection will be necessary for product development. With in-line defect monitoring, processing of defective wafers will be avoided and test time for wafer sort and package-level test will be maintained.

Table 31a Commodity DRAM Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU / ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
DRAM capacity (Gbits): R&D	**4**	**TBD**	**8**	**TBD**	**16**	**TBD**	**TBD**
Mass Production	**1**	**TBD**	**2**	**TBD**	**4**	**TBD**	**TBD**
DRAM data rate (GHz): R&D	**1.6**	**TBD**	**2**	**TBD**	**2.4**	**TBD**	**TBD**
Mass Production	**1.3**	**TBD**	**1.6**	**TBD**	**2**	**TBD**	**TBD**
DRAM access time (ns): R&D	**1**	**TBD**	**0.5**	**TBD**	**0.3**	**TBD**	**TBD**
Mass Production	**2.5**	**TBD**	**2**	**TBD**	**1**	**TBD**	**TBD**
DRAM bit width/device (Mass Production)	**16**	**TBD**	**16**	**TBD**	**16**	**TBD**	**TBD**
Tester data rate (GHz): R&D	**1.6**	**TBD**	**2**	**TBD**	**2.4**	**TBD**	**TBD**
Mass Production	**1.3**	**TBD**	**1.6**	**TBD**	**2**	**TBD**	**TBD**
Overall timing accuracy (ps): R&D	**50**	**TBD**	**40**	**TBD**	**30**	**TBD**	**TBD**
Mass Production	**60**	**TBD**	**50**	**TBD**	**40**	**TBD**	**TBD**
Simultaneous testing (devices/test head)	**64**	**TBD**	**64**	**TBD**	**128**	**TBD**	**TBD**
Test channels (Mass Production)	**1200***	**TBD**	**2300**	**TBD**	**2300**	**TBD**	**TBD**
	2300**					**TBD**	**TBD**

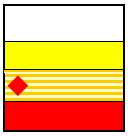
**Assuming SDRAM with 32 devices/station, Driver 800, I/O 640*
*** Assuming RAMBUS with 32 devices/station, Driver 480, I/O 640; 2 64 devices/station, Driver 960, I/O 1280*

Table 31b Commodity DRAM Test Requirements—Long-term

Year of Production		*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node		*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)		*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)		*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)		*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)		*18*	*14*	*13*	*10*	*9*	*7*
DRAM capacity (Gbits):	R&D	**64**	**TBD**	**256**	**TBD**	**1024**	**TBD**
	Mass Production	**16**	**TBD**	**64**	**TBD**	**256**	**TBD**
DRAM data rate (GHz):	R&D	**3**	**TBD**	**3.6**	**TBD**	**4.2**	**TBD**
	Mass Production	**2.4**	**TBD**	**3**	**TBD**	**3.6**	**TBD**
DRAM access time (ns):	R&D	**0.2**	**TBD**	**0.15**	**TBD**	**0.1**	**TBD**
	Mass Production	**0.8**	**TBD**	**0.5**	**TBD**	**0.3**	**TBD**
Tester data rate (GHz):	R&D	**3**	**TBD**	**3.6**	**TBD**	**4.2**	**TBD**
	Mass Production	**2.4**	**TBD**	**3**	**TBD**	**3.6**	**TBD**
Overall timing accuracy (ps):	R&D	**25**	**TBD**	**20**	**TBD**	**18**	**TBD**
	Mass Production	**30**	**TBD**	**25**	**TBD**	**20**	**TBD**
Simultaneous testing (Devices/test head)		**128**	**TBD**	**256**	**TBD**	**256**	**TBD**
Test channels (Mass Production)		**3500***	**TBD**	**3500***	**TBD**	**3500***	**TBD**

**Assuming RAMBUS with 64 devices/station, Driver 960, I/O 2560*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



COMMODITY FLASH TESTING

Flash will follow the DRAM trend of density doubling every year in the short term and slow to a doubling every 1.5 years. NOR Flash has been the volume driver, but NAND volumes have been rapidly increasing. NAND and NOR generally do not have the same test solution due to differences in bus definition. Further proliferation of bus types is expected due to the customization of flash for specific customer applications. Bus width is presently 8-bit and 16-bit but 32-bit widths are on the horizon.

Flash is commonly used in battery powered embedded applications thus test equipment must provide a means of measuring low levels of current or energy. Supply voltage requirements of Flash have been dropping slowly over time, but the need for internal test mode voltages that are 3–8 times the external supply requirements is expected to continue. Increased absolute accuracy of supply voltages will be required in the future due to the trend toward lower voltages, but is expected to remain constant as a relative percentage. I/O voltage decreases are pushing the operation limits of standard tester load circuits; new methods will be required in the future.

Wafer test generally does not require the performance of package test, but error detection, error analysis, and redundancy processing is required.

Stacking of various types of Flash and other memory or logic components in a single package has become standard and is expected to continue. Stacked packaging has complicated the package test requirements, increasing package pin counts and the number of DUT power supplies. Flash components contain an embedded controller for program/erase control, enabling additional features that require increased logic or analog test capability. Data and clock rates for flash will increase, but there is expected to be a wide variability in the requirements based upon the end application. Tables 32a and b reflect only the high-end requirement.

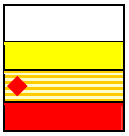
Table 32a Commodity Flash Memory Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU / ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Device Characteristics							
Density (megabits): volume production	**256**	**256**	**512**	**512**	**512**	**1024**	**1024**
Density (megabits): lead density	**512**	**1024**	**1024**	**2048**	**2048**	**2048**	**4096**
Data width (bits)	**16**	**32**	**32**	**32**	**32**	**32**	**32**
Simultaneously tested devices (wafer test)	**64**	**128**	**128**	**128**	**256**	**256**	**256**
Simultaneously tested devices (package test)	**128**	**128**	**128**	**256**	**256**	**256**	**256**
Power Supplies							
Power supply voltage range	**1.0–5.5**	**1.0–5.5**	**1.0–5.5**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**
Number of power supplies per device	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Maximum current (MA)	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Programming power supply voltage range (V)	**1.0–12.0**	**1.0–12.0**	**0.6–10.0**	**0.6–10.0**	**0.6–10.0**	**0.6–8.1**	**0.6–8.1**
Number of programming power supplies per device	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Pattern Generator							
Tester channels per test site [1]	**64**	**64**	**64**	**72**	**72**	**72**	**72**
Timing							
Maximum data rate (MHz)	**125**	**133**	**166**	**166**	**166**	**233**	**233**
Accuracy OTA (ns)	**0.6**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**

Table 32b Commodity Flash Memory Test Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU / ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Device Characteristics						
Density (megabits): volume production	**1024**	**2048**	**2048**	**4096**	**4096**	**8192**
Density (megabits): lead density	**4096**	**8196**	**8196**	**16384**	**16384**	**32768**
Data width (bits)	**32**	**32**	**32**	**32**	**32**	**64**
Simultaneously tested devices (wafer test)	**256**	**256**	**512**	**512**	**512**	**512**
Simultaneously tested devices (package test)	**256**	**256**	**256**	**256**	**256**	**256**
Power Supplies						
Power supply voltage range	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**	**0.6–3.3**
Number of power supplies per device	**2**	**2**	**2**	**2**	**2**	**2**
Maximum current (MA)	**300**	**300**	**300**	**300**	**300**	**300**
Programming power supply voltage range (V)	**0.6–8.0**	**0.6–8.0**	**0.6–8.0**	**0.6–8.0**	**0.6–8.0**	**0.6–8.0**
Number of programming power supplies per device	**2**	**2**	**2**	**2**	**2**	**2**
Pattern Generator						
Tester channels per test site [1]	**72**	**72**	**72**	**72**	**72**	**72**
Timing						
Maximum data rate (MHz)	**200**	**200**	**250**	**250**	**300**	**300**
Accuracy OTA (ns)	**0.3**	**0.3**	**0.2**	**0.2**	**0.1**	**0.1**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



EMBEDDED DRAM AND FLASH TESTING

In the near-term, the number of embedded DRAM bits will double in every two years; in the long-term this growth will slow to double every three years. The major concern in the merged logic-DRAM design in a dual-gate process will be array noise and sense-amp imbalance.

Embedded Flash memory bits will grow exponentially in the near term; however, in the long-term embedded flash memory bits will double every two years. It is expected that embedded flash memories will transition to use a multi-bit cell architecture. More and more ICs will include both DRAM and flash memories. Oxide reliability, sense-amp imbalance, and oxide-nitride-oxide (ONO) scaling will be the major concerns for flash memories. Refer to Tables 33a and b.

To enhance test productivity, new test-oriented architectures will be required. Built-in self-test and built-in self-repair will be essential to test embedded DRAM and embedded Flash memories and to maintain production throughput and yield. The primary test algorithms for Flash memories will continue to be Read-disturb, Program-disturb, and Erase-disturb while March tests with all data background will be essential for embedded DRAM.

Considerable parallelism in test will be required to maintain test throughput in the face of rising memory densities. It is expected that double insertion of devices will become more cost effective for some designs than testing both logic and embedded memories on the logic tester. In double insertion, embedded Flash and DRAMs will be tested and repaired on the memory tester, while the logic blocks will be tested on the logic tester.

Embedded SRAM test requirements are captured in the High Performance Microprocessor section of the roadmap.

Table 33a Embedded Memory (DRAM and Flash) Test Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Embedded DRAM							
Embedded DRAM size (Mbits)							
R&D	**128**	**128**	**256**	**256**	**512**	**512**	**1024**
Mass Production	**64**	**64**	**128**	**128**	**256**	**256**	**512**
Failure concerns	**Particle defects; array noise, data retention**		**Particle defects, array noise; sense-amp imbalance**				
Wafer level test	**Double insertion**						
Usage of on-chip test	**100% BIST 100% BISR**		**100% BIST 100% BISR**		**100% BIST 100% BISR**		**100% BIST 100% BISR**
Embedded Flash							
Embedded Flash size (Mbits)							
R&D	**64**	**64**	**128**	**128**	**256**	**256**	**512**
Mass Production	**32**	**32**	**64**	**64**	**128**	**128**	**256**
Embedded mixed memory size (Mbits)							
Flash	**16**	**16**	**32**	**32**	**64**	**64**	**128**
DRAM	**16**	**16**	**32**	**32**	**32**	**64**	**64**
Failure concerns	**Oxide defects; ONO scaling**		**Oxide defects; ONO scaling; over-erase**				
Wafer level test	**Double insertion**						
Usage of on-chip test	**BIST/BIST DAT**		**BIST/BIST DAT**		**BIST/BIST DAT**		**BIST/BIST DAT**

Table 33b Embedded Memory (DRAM and Flash) Test Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Embedded DRAM						
Embedded DRAM size (Gbits)						
R&D	**1**	**1**	**2**	**2**	**4**	**4**
Mass Production	**0.512**	**0.512**	**1**	**1**	**2**	**2**
Failure concerns	**Particle Defects, Array Noise, Sense-amp Imbalance**					
Wafer level test	**In-line Defect Detection, Double Insertion**					
Usage of on-chip test	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**	**100% BIST 100% BISR**
Embedded Flash						
Embedded Flash size (Mbits)						
R&D	**256**	**512**	**512**	**1024**	**1024**	**2048**
Mass production	**64**	**256**	**128**	**512**	**256**	**1024**
Embedded mixed memory size (Mbits)						
Flash	**64**	**128**	**128**	**256**	**256**	**512**
DRAM	**64**	**128**	**128**	**256**	**256**	**512**
Failure concerns	**Oxide Defects, ONO Scaling, Sense-amp Imbalance**					
Wafer level test	**In-line Defect Detection, Double Insertion**					
Usage of on-chip test	**100% BIST 100% BISR**	**BIST/BISR DAT**	**BIST/BISR DAT**	**BIST/BISR DAT**	**BIST/BISR DAT**	**BIST/BISR DAT**

Number of bits in mass production is approximately 50% of number of bits in R&D

RELIABILITY TECHNOLOGY REQUIREMENTS

Reliability solutions are an optimization of Reliability Defect Density (RDD) learning, Reliability Screens & Test Methods (RS&TM) applications, and Design For Reliability (DFR). The goal of the reliability solution optimization is to provide the best value for the reliability dollar spent, where value is defined as the ratio of customer satisfaction to customer cost. When talking reliability, customer satisfaction is measured by the field failure rate or Failures In Time (FITs). The cost of reliability has two components—manufacturing operations costs and yield. As such, these two components of the reliability cost equation are the primary challenges facing every reliability solution provider. Manufacturing Operations costs are driven by applying conditions outside of the application specs which most often demand providing solutions to leakage induced power (electrical power delivery and thermal/heat dissipation) and screens duration. The yield costs are severely biased towards elimination of "overkill"/"false rejects"—which in many ways are tied to derivatives of the power solution.

Of the three components of the reliability solution, this section will deal specifically with the RS&TM. Defect learning is addressed in the Defect Modeling and Physical Defects section, and although the 3rd rule of Reliability states "Reliability Learning follows Yield Learning—except when it doesn't", historical data overwhelmingly supports the premise that the component of defects that are "reliability unique" is very small.

Similarly, DFR has a cousin in the DFT section however the genetics are not as strongly matched as in the case of defect learning. DFR also has three key components: Technology Design, Chip Design (Logical and Physical), and System Design.

In each of the three, the DFR work must strive for Defect Tolerance. In the case of technology design, leakage induced power mitigation maintains an edge in importance over defect tolerance. Regarding chip design and DFR, power mitigation and fault tolerance are at par in design priority. Redundant element analysis and power dissipation analysis burn considerable design engineering horsepower. At the system level, defect tolerance in the forms of error

detection/correction remains the byword in reliability, but power mitigation is a strong second and quickly closing the gap.

In the arena of Reliability Screens & Test Methods, there is a kaleidoscope of techniques and methodologies each with it's own champions and supporting/compelling/biased data. Hence the battle rages and debates ebb and flow depending upon the technology node, chip/circuit type, design style, performance target, reliability requirements and defect *dujour*.

RS&TM are best categorized by separating them into Wafer Applications and Package (or Module) Applications and then further segregation into "Detection" and "Acceleration" techniques. This tiered structure will help to dilute the perennial argument between test and reliability regarding whether a field return is a test escape or an early life reliability failure.

Regardless of operational process step (i.e., Wafer or Package), acceleration techniques invariably must deal with potent power implications simply because acceleration requires temperature and/or voltage far in excess of application conditions—and leakage varies logarithmically with both. The same is not true for detection techniques. In many instances, detection techniques employ conditions that reduce leakage, and in instances where detection requires application conditions that exacerbate leakage those conditions typically do not approach the level of acceleration conditions.

BURN-IN REQUIREMENTS

Burn-in requirements, Tables 34a and b, show no significant changes from previous roadmaps. Increasing burn-in costs in certain market segments continue to drive efforts to reduce or eliminate burn-in. For high complexity devices, cost drivers are higher pin count, tighter pitch, and increased functionality. For high power devices, cost drivers are massive current at low voltages and tight thermal management. Burn-in cost reduction on these devices is being driven by implementation of DFT stressing techniques in burn-in, as well as continuing research into cost-effective thermal management techniques. In general, new devices are requiring more power supplies, tighter tolerances (both electrical and mechanical), more analog stimulus during burn-in, and increased functional stressing capabilities. One emerging trend is the increasing use of system level burn-in for high reliability applications as traditional burn-in approaches become more expensive and less effective.

Burn-in reduction/elimination is being adversely impacted by several factors. Voltage acceleration is eroding on newer technologies due to lower core voltage, the effect of higher stress voltages on leakage current and power dissipation, and decreasing headroom for voltage acceleration before triggering device wearout. Increased power requirements and the resulting heat generation are forcing reductions in burn-in temperature, resulting in less temperature acceleration. Examples of alternatives to burn-in include HVST (High Voltage Stress Test), IDDQ/Delta IDDQ, wafer level reliability testing, and package level reliability stress tests. Tools to reduce burn-in include Test In Burn-in capabilities, individual device thermal management, wafer mapping for burn-in candidates, and integrated feedback loops with the wafer fab. Mature technologies with well-understood fabrication processes are more successful at eliminating burn-in. More complex and higher reliability technologies, including leading edge VLSI, Microprocessors, and Memories, appear unlikely to eliminate burn-in for the foreseeable future.

Burn-in system technology is advancing to meet much higher device power and current requirements. The range of core voltage requirements is increasing significantly. Scan requires very deep vectors for large memories, while high power requires individual device thermal management. System frequency capabilities, with some exceptions, are incapable of meeting speeds of the newest technology devices. As a result, at-speed burn-in is typically accomplished through use of internal clocks. Devices with DFT are able to use skinny interfaces, while those without DFT are requiring increasing I/O.

Burn-in board technology is being driven by tighter socket pitches, higher current requirements, higher heat dissipation, both lower and higher voltage levels, and increasing clock and data rates. This results in higher board layer counts, smaller traces, less space for routing, more complex processes and materials, higher test costs (due to increasing test channels and more complex test probes) and a new set of board reliability issues. Solutions involve new printed circuit board materials, thicker burn-in boards, new socket interface techniques, more sophisticated layout tools, and increasing use of simulation.

Burn-in socket design is being driven by high current and power dissipation, higher frequencies and lower voltages, larger packages with smaller pitches and higher I/O count, ergonomics, increasing tooling expenses, shorter device life cycles, shorter customer lead-times, longer socket development times, burn-in board interfacing challenges, lack of standardization in the packaging industry, and device alignment challenges. Areas of research include new socket body

materials, new contact designs, alternatives for traditional contacting technology, and increasing use of electrical, mechanical, and thermal modeling.

Most requirements for Known Good Die (KGD) continue to rely on individual die carrier technology or non-burn-in methods of ensuring die reliability. Two product families that typically require the most intensive amounts of burn-in (DRAM and high-end microprocessors) are not well suited for wafer level burn-in (WLBI) due to high I/O and limited DFT (DRAM) or high power requirements (high-end microprocessors). New product introduction, which could best utilize WLBI capabilities, is also a poor candidate because of rapidly changing designs that make WLBI tooling costs unattractive. WLBI is most ideally suited for mid-range devices. WLBI may most benefit mature processes with high per-wafer die densities and devices requiring rapid feedback from the burn-in to the fab operation. Increasing use of bare die in various applications will continue to drive development of KGD and WLBI.

Overall costs for burn-in are going down for mature products, while increasing for the high power/high complexity applications. More mature socket prices are declining, while leading edge socket technology is becoming more expensive due to high pin count and small pitch. High power applications are typically much more expensive on a per device basis, although cost-competitive with traditional technologies on a per watt basis.

Table 34a Burn-in Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU / ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
High Performance ASIC							
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**50**	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–3.3**	**0.7–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**
Power dissipation (W per DUT)	**50**	**75**	**100**	**150**	**200**	**200**	**200**
Maximum number of signal I/O	**384**	**384**	**384**	**384**	**384**	**384**	**384**
High Performance Microprocessor							
Clock input frequency (MHz)	**200**	**250**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–3.4**	**0.5–3.4**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**
Power dissipation (W per DUT)	**200**	**250**	**600**	**600**	**600**	**600**	**600**
Maximum current (A)	**150**	**300**	**400**	**450**	**450**	**450**	**450**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Low-End Microcontroller							
Clock frequency (MHz)	**200**	**300**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**50**	**60**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–12.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**
Power dissipation (W per DUT)	**5**	**10**	**10**	**10**	**10**	**10**	**10**
Maximum number of signal I/O	**32**	**32**	**32**	**32**	**32**	**32**	**32**
Mixed-Signal							
Clock input frequency (MHz)	**200**	**250**	**250**	**250**	**250**	**250**	**250**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.7–100**	**0.7–100**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**
Power dissipation (W per DUT)	**75**	**75**	**150**	**150**	**150**	**150**	**150**
Maximum current (A)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Analog signal peak-to-peak voltage range (V)	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**
Commodity Memory							
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**30**	**50**	**50**	**50**	**50**	**50**	**50**
Power supply voltage range (V)	**0.6–6.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**	**0.6–4.0**
Programming power supply voltage range (V)	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–10**	**0.6–8**	**0.6–8**	**0.6–8**
Power dissipation (W per DUT)	**10**	**15**	**20**	**20**	**20**	**20**	**20**
Maximum number of signal I/O	**36**	**72**	**72**	**72**	**72**	**72**	**72**
DFT / BIST Requirements							
Scan pin count (per DUT)	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Scan vector memory depth (megavectors)	**256**	**256**	**256**	**256**	**256**	**256**	**256**
Scan vector frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**	**75**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

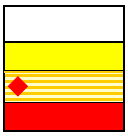


Table 34b Burn-in Requirements—Long-term

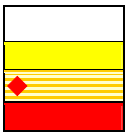
Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
High Performance ASIC						
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.4–2.5**
Power dissipation (W per DUT)	**200**	**200**	**200**	**225**	**225**	**250**
Maximum number of signal I/O	**384**	**384**	**384**	**384**	**384**	**384**
High Performance Microprocessor						
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**
Power dissipation (W per DUT)	**600**	**600**	**600**	**600**	**600**	**600**
Maximum current (A)	**450**	**450**	**450**	**450**	**450**	**450**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**
Low-End Microcontroller						
Clock frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**
Power dissipation (W per DUT)	**20**	**20**	**20**	**20**	**20**	**20**
Maximum number of signal I/O	**32**	**32**	**32**	**32**	**32**	**32**
Mixed-Signal						
Clock input frequency (MHz)	**250**	**250**	**250**	**250**	**250**	**250**
Clock input frequency (MHz)	**250**	**250**	**250**	**250**	**250**	**250**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**
Power supply voltage range (V)	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–1000**	**0.5–1000**	**0.5–1000**
Power dissipation (W per DUT)	**150**	**150**	**150**	**150**	**150**	**150**
Maximum current (A)	**30**	**30**	**30**	**30**	**30**	**30**
Maximum number of signal I/O	**128**	**128**	**128**	**128**	**128**	**128**
Analog signal peak-to-peak voltage range (V)	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**	**±10V**
Commodity Memory						
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**50**	**50**	**50**	**50**	**50**	**50**
Power supply voltage range (V)	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**	**0.5–4.0**
Programming power supply voltage range (V)	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**	**0.5–8.0**
Power dissipation (W per DUT)	**20**	**20**	**20**	**20**	**20**	**20**
Maximum number of signal I/O	**72**	**72**	**72**	**72**	**72**	**72**
DFT / BIST Requirements						
Scan pin count (per DUT)	**128**	**128**	**128**	**128**	**128**	**128**
Scan vector memory depth (megavectors)	**256**	**256**	**256**	**256**	**256**	**256**
Scan vector frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



IDDQ TESTING

Normal background leakages (both the amplitude and variability) are increasing to the point where IDDQ testing as it has historically been practiced will face difficulty in the future. IDDQ testing must change to continue to enable defect detection. Alternative solutions must be developed to provide the same benefits in the face of the rising background leakage currents of future technologies. IDDQ provides a rich source of information about a manufactured chip and in many cases today plays a vital role in both defect detection and characterization.

The Table 35 shows projected IDDQ values for performance-oriented products in future technologies. These values should not be precisely interpreted; instead they are meant to provide relative values as technology scales. These numbers may be significantly lower (e.g., three orders of magnitude) for low-power technologies. These ranges are derived from the maximum device I_{off} (from 2001 ITRS *Process Integration* chapter, Logic Technology Requirements Tables [high performance, low operating power, and low standby power tables]), transistor counts (from *ORTC, Table 1g-1h*), typical W/L ratios, and assuming a percentage of off transistors. It is assumed that the IC is designed appropriately to enable IDDQ testing.

Table 35 Projected Performance-oriented IC IDDQ Values

YEAR	MAXIMUM IDDQ
2001	**30–70 mA**
2003	**70–150 mA**
2005	**150–400 mA**
2008	**400 mA–1.6 A**
2011	**1.6–8 A**
2014	**8–20 A**

Note—all table values assume 25°C

Not only are IDDQ values projected to increase in magnitude, but also the variability of IDDQ (for a given technology and product) is expected to be high. For example, although the IDDQ values in Table 35 represent the maximum, typical values could be significantly lower. It is important to better understand the components of this variability and to develop new test techniques so that this variability can be tolerated.

Below is a list of potential opportunities (both test methods and design-for-test techniques) for continuous use of IDDQ testing.

- Use of "Delta IDDQ" or "IDDQ Ratios" test methods
- Substrate biasing to control V_t
- Processing changes to have higher V_t (either for all devices or selected ones) or lower V_t variance
- IDDQ testing at low temperature
- Power supply partitioning at chip level and use of multiple power sources
- Use of large "footer" devices that limit leakage currents in the transistor path
- IDDQ measurements for multiple V_{dd} voltages
- Transient and charged-based I_{dd} techniques
- IDDQ limits determined based on comparisons with neighboring die
- IDDQ limits determined as a function of other parametric measurements (e.g., speed)
- IDDQ measured simultaneously on a set of power supply pads
- Built-in IDDQ sensors (potentially self-calibrating) or other on-chip measurement aids

IDDQ has been an important failure analysis and characterization technique. Physical failure analysis relies on IDDQ for defect localization and defect type identification. In addition, there is important information about defective circuit behavior in the relationship between IDDQ and conditions such as temperature, voltage, and circuit state. As IDDQ goes up, however, some loss of diagnostic effectiveness using traditional techniques is possible.

There is also a need to improve the rate at which IDDQ measurements can be performed. Test equipment improvements or supported test fixture aids are preferred. Furthermore, IDDQ measurement resolution and accuracy at high currents must improve—particularly for emerging "signature-based" techniques.

TEST HANDLER AND PROBER TECHNOLOGY REQUIREMENTS

Wafer probe and component test handling equipment face significant technical challenges in each market segment. Common issues on both platforms include thermal management, higher parallelism and increasing capital equipment cost.

Specific to wafer probe the technical trends impacting this equipment include fab process technology, increasing probe count, decreasing probe pitch/diameter and evolving probe tip geometries. These trends translate into challenges in the areas of DUT thermal management, wafer placement accuracy under load, chuck electrical isolation, and probe to pad alignment (PTPA) complexity.

Memory test handling unique challenges include massive parallelism, ball to edge package gap and thin/stacked form factors which translate into requirements for new kit-less innovative handling technologies. Logic test handling unique challenges include thermal power dissipation, operational improvements, increase ESD sensitivity and advanced packaging technologies. These trends translate into requirements for active thermal control during test, lower cycle times and improved material flow characteristics, integrated ESD measurement and universal tooling. Communications and network product test handling unique challenges include very high and low temperature control, 10Gbps + testing, and stacked die packages. These trends translate into requirements for very low and high temperature tri-temperature handlers shielded for EMI and able to handle small, thin and stacked packages.

Ultimately these issues are increasing cost of wafer probers and component test handlers, while structural and functional test equipment costs continue to decrease. Over the next several years, test handling equipment solutions will be required to meet increasing product requirements under increasing cost pressures.

Table 36a Handler (Memory—Pick and Place) Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**32–64**	**32–64**	**64–128**	**64–128**	**64–128**	**128–256**	**128–256**
Index time (S)	**3–5**	**3–5**	**3–5**	**3–5**	**2–5**	**2–5**	**2–4**
Throughput (devices per hour)	**6–8K**	**6–8K**	**8–10K**	**8–10K**	**8–10K**	**8–12K**	**8–12K**
Sorting	**5–9**	**5–9**	**5–9**	**5–9**	**5–9**	**5–9**	**5–9**
Maximum set point (degrees C)	**135**	**135**	**135**	**135**	**135**	**135**	**135**
Minimum set point (degrees C)	**-55**	**-55**	**-55**	**-55**	**-55**	**-55**	**-55**
Temperature accuracy (degrees C)	**±2**	**±2**	**±2**	**±2**	**±2**	**±2**	**±1.5**
Foot print (ratio)	**1–1.3**	**1–1.3**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**
Number of pins/device	**40–80**	**40–250**	**40–250**	**40–250**	**40–250**	**40–400**	**40–400**
Pin pitch (mm)	**0.5–1.0**	**0.5–1.0**	**0.5–1.0**	**0.4–1.0**	**0.4–1.0**	**0.3–1.0**	**0.3–1.0**
Ball edge to package edge clearance (mm)	**0.6**	**0.6**	**0**	**0**	**0**	**0**	**0**
Minimum package thickness (mm)	**0.8–1.8**	**0.3–1.8**	**0.3–1.8**	**0.3–1.8**	**0.3–1.8**	**0.2–1.8**	**0.2–1.8**
Conversion time (minutes)	**40**	**40**	**40**	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**
Tester/handler communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

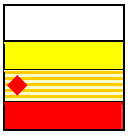
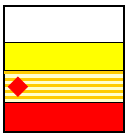


Table 36b Handler (Memory—Pick and Place) Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**128–256**	**128–256**	**128–256**	**128–256**	**128–256**	**128–256**
Index time (S)	**2–4**	**2–4**	**2–4**	**2–4**	**2–4**	**2–4**
Throughput (devices per hour)	**12–20K**	**12–20K**	**12–20K**	**12–20K**	**12–20K**	**12–20K**
Sorting	**5-9**	**5-9**	**5-9**	**5-9**	**5-9**	**5-9**
Maximum set point (degrees C)	**135**	**135**	**135**	**135**	**135**	**135**
Minimum set point (degrees C)	**-55**	**-55**	**-55**	**-55**	**-55**	**-55**
Temperature accuracy (degrees C)	**±1.5**	**±1.5**	**±1.5**	**±1.5**	**±1.5**	**±1.5**
Foot print (ratio)	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**
Number of pins/device	**40–400**	**40–400**	**40–400**	**40–400**	**40–400**	**40–400**
Pin pitch (mm)	**0.3-1.0**	**0.3-1.0**	**0.3-1.0**	**0.3-1.0**	**0.3-1.0**	**0.3–1.0**
Ball edge to package edge clearance (mm)	**0**	**0**	**0**	**0**	**0**	**0**
Minimum package thickness (mm)	**0.2–1.8**	**0.2–1.8**	**0.2–1.8**	**0.2–1.8**	**0.2–1.8**	**0.2-1.8**
Conversion time (minutes)	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**	**1 (kitless)**
Tester/handler communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 36a and 36b:

Index time was done from test end signal reception from tester to the test start signal transmission of handler.

UPH calculated with zero-second test time and no lot-size generated interruptions.

Sort is number of stackable JEDEC tray sleeves used for output of devices.

±assumes a normal distribution centered at the temperature with 3 standard deviations equal to the ±number.

Allowable temperature rise due to a step power pulse of the corresponding power density.

Asynchronous capability is defined as the capability of the handler to input, socket and output devices independently with multiple test sites-no gang socketing.

Uninterrupted tray flow requires the handler operation to not be halted when loading/unloading trays.

Auto-Retest requires units to be retested automatically without the need for operator intervention. This is different from a simple reprobe in that the part must be socketed on a different change kit head (if possible).

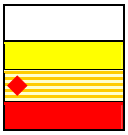
EMI event field is a measurement of electric emissions due to ESD events during normal handler operation.

MTBF is per SEMI E-10 [1]definitions.

[1] *SEMI E10-0699E—Standard for Definition and Measurement of Equipment Reliability, Availability, and Measurement (RAM).*

Table 37a Handler (Logic—Pick and Place) Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**4**	**8**	**8**	**8**	**8**	**8**	**16**
Index time (S)	**0.3–0.4**	**0.3–0.4**	**0.3–0.4**	**0.3–0.4**	**0.25–0.3**	**0.25–0.3**	**0.25**
Throughput (devices per hour)	**4–6K**	**8–12K**	**8–12K**	**8–12K**	**9–14K**	**9–14K**	**12–20K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
Maximum set point (degrees C)	**125**	**125**	**125**	**125**	**125**	**125**	**125**
Minimum set point (degrees C)	**-10**	**-10**	**-10**	**-10**	**-10**	**-10**	**-10**
Temperature accuracy (degrees C)	**±0.5**	**±0.5**	**±0.5**	**±0.3**	**±0.3**	**±0.1**	**±0.1**
Total thermal load (Watts) - MPU	**80**	**80**	**125**	**125**	**150**	**150**	**175**
Total thermal load (Watts) – Non-MPU	**25**	**25**	**25**	**25**	**35**	**35**	**35**
Thermal Watt density (Watts/cm^2) – MPU	**80**	**80**	**130**	**130**	**175**	**175**	**200**
Thermal Watt density (Watts/cm^2) – Non-MPU	**25**	**25**	**25**	**25**	**35**	**35**	**35**
Foot print (ratio)	**1**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.4**
Max socket load per unit (kg)	**16**	**20**	**24**	**27**	**30**	**30**	**35**
Asynchronous capability	**No**	**No**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**700**	**700**	**750**	**750**	**800**	**800**	**850**
Pin/land pitch (mm)	**1.2**	**1.2**	**1.1**	**1.1**	**1**	**1**	**0.8**
EMI event field (ESD measurements) (mV)	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**
Handler/tester communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**
Conversion time (minutes)	**30**	**30**	**30**	**30**	**15**	**15**	**15**
Uninterrupted tray loading/auto-2A	**No**	**No**	**No**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**80**	**100**	**100**	**168**	**168**	**500**	**500**



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 37b Handler (Logic—Pick and Place) Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**16**	**16**	**16**	**32**	**32**	**32**
Index time (S)	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**
Throughput (devices per hour)	**12–20K**	**12–20K**	**12–20K**	**20–28K**	**20–28K**	**20–28K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
Maximum set point (degrees C)	**125**	**125**	**125**	**125**	**125**	**125**
Minimum set point (degrees C)	**-10**	**-10**	**-10**	**-10**	**-10**	**-10**
Temperature accuracy (degrees C)	**±0.1**	**±0.1**	**±0.1**	**±0.1**	**±0.1**	**±0.1**
Total thermal load (Watts) – MPU	**200**	**200**	**200**	**250**	**250**	**300**
Total thermal load (Watts) – Non-MPU	**50**	**50**	**50**	**75**	**75**	**100**
Thermal Watt density (Watts/cm^2) – MPU	**225**	**225**	**225**	**250**	**250**	**250**
Thermal Watt density (Watts/cm^2) – Non-MPU	**75**	**75**	**75**	**100**	**100**	**125**
Foot print (ratio)	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**
Max socket load per unit (kg)	**35**	**35**	**35**	**35**	**35**	**35**
Asynchronous capability	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**850**	**850**	**850**	**900**	**900**	**1000**
Pin/land pitch (mm)	**0.6**	**0.6**	**0.6**	**0.4**	**0.4**	**0.4**
EMI event field (ESD measurements) (mV)	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**
Handler/tester communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**
Conversion time (minutes)	**5**	**5**	**5**	**5**	**5**	**5**
Uninterrupted tray loading/auto-2A	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

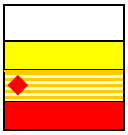


Table 38a Handler (Network and Communications—Pick and Place) Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**4**	**8**	**8**	**8**	**8**	**8**	**16**
Index time (S)	**0.3–0.4**	**0.3–0.4**	**0.3–0.4**	**0.3–0.4**	**0.25–0.3**	**0.25–0.3**	**0.25**
Throughput (devices per hour)	**4–6K**	**8–12K**	**8–12K**	**8–12K**	**9–14K**	**9–14K**	**12–20K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
Set point range (degrees C)	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**
Temperature accuracy (degrees C)	**-0.5**	**-0.5**	**-0.5**	**-0.5**	**-0.5**	**-0.5**	**-0.5**
Total thermal load (Watts)	**25**	**25**	**25**	**35**	**35**	**35**	**35**
Thermal Watt density (Watts/cm^2) – MPU	**25**	**25**	**25**	**50**	**50**	**50**	**50**
Allowable device temperature rise (degrees C)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Foot print (ratio)	**1**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.4**
Max socket load per unit (kg)	**16**	**20**	**24**	**27**	**30**	**30**	**35**
Asynchronous capability	**No**	**No**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**700**	**700**	**750**	**750**	**800**	**800**	**850**
Pin/land pitch (mm)	**1.2**	**1.2**	**1.1**	**1.1**	**1**	**1**	**0.8**
EMI event field (ESD measurements) (mV)	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**
Handler/tester communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**
Conversion time (minutes)	**30**	**30**	**30**	**30**	**15**	**15**	**15**
Uninterrupted tray loading/auto-2A	**No**	**No**	**No**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**80**	**100**	**100**	**168**	**168**	**500**	**500**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

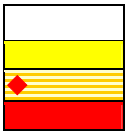


Table 38b Handler (Network and Communications—Pick and Place) Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	***2015***	*2016*	***2018***
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Conformity tray type	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**	**JEDEC**
Parallel testing	**16**	**16**	**16**	**32**	**32**	**32**
Index time (S)	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**
Throughput (devices per hour)	**12–20K**	**12–20K**	**12–20K**	**20–28K**	**20–28K**	**20–28K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
Set point range (degrees C)	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**	**-45 to +150**
Temperature accuracy (degrees C)	**-0.5**	**-0.5**	**-0.5**	**-0.5**	**-0.5**	**-0.5**
Total thermal load (Watts)	**50**	**50**	**50**	**50**	**50**	**50**
Thermal Watt density (Watts/cm^2) - MPU	**50**	**50**	**50**	**50**	**50**	**50**
Allowable device temperature rise (degrees C)	**20**	**20**	**20**	**20**	**20**	**20**
Foot print (ratio)	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**	**1.4**
Max socket load per unit (kg)	**35**	**35**	**35**	**35**	**35**	**35**
Asynchronous capability	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**850**	**850**	**850**	**900**	**900**	**1000**
Pin/land pitch (mm)	**0.6**	**0.6**	**0.6**	**0.4**	**0.4**	**0.4**
EMI event field (ESD measurements) (mV)	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**	**250 @ 6" or 150 @ 12"**
Handler/tester communications	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**	**SECS/GEM--HSEM**
Conversion time (minutes)	**5**	**5**	**5**	**5**	**5**	**5**
Uninterrupted tray loading/auto-2A	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

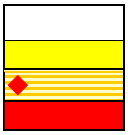


Table 39a Prober (Logic MPU—Pick and Place) Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	***57***	***50***
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Pad pitch							
Peripheral (mm)	**50–125**	**50–125**	**40–100**	**40–100**	**40–100**	**30–80**	**30–80**
Bump (mm)	**40**	**40**	**30**	**30**	**30**	**30**	**30**
Wafer thickness (mm)	**180–725**	**180–725**	**80–775**	**80–775**	**80–775**	**80–775**	**80–775**
Maximum I/O pads	**2200**	**2200**	**3000**	**3000**	**3000**	**400**	**4000**
Chuck positioning accuracy							
X & Y (µm)	**4**	**4**	**4**	**4**	**4**	**2**	**2**
Z (µm)	**4**	**4**	**2**	**2**	**1**	**1**	**1**
Co-planarity (µm)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Probe-to-pad alignment (µm)	**6.5**	**6.5**	**4.5**	**4.5**	**4.5**	**4.5**	**4.5**
Maximum chuck force (kg)	**50**	**50**	**50**	**100**	**100**	**100**	**100**
Parallel testing	**1X**	**1X**	**1X**	**2X**	**2X**	**2X**	**2X**
Set point range (degrees C)	**-10 to +25**	**-10 to +25**	**-30 to +85**	**-30 to +85**	**-30 to +85**	**-30 to +85**	**-30 to +85**
Temperature accuracy (degrees C)	**-1**	**-1**	**-1**	**-1**	**-1**	**-1**	**-1**
Total power (Watts)	**150**	**150**	**150**	**150**	**200**	**200**	**250**
Power density (Watt/cm^2)	**45**	**45**	**90**	**90**	**90**	**90**	**120**
Chuck leakage (picoampere)	**3**	**3**	**1**	**1**	**1**	**0.1**	**0.1**
Foot print (ratio)	**1–1.3**	**1–1.3**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

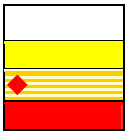


Table 39b Prober (Logic MPU—Pick and Place) Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*32*	*28*	*22*	*20*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Wafer diameter (mm)	**300**	**300**	**300**	**450**	**450**	**450**
Pad pitch						
Peripheral (mm)	**30–60**	**30–60**	**30–60**	**30–60**	**30–60**	**30–60**
Bump (mm)	**20**	**20**	**20**	**20**	**20**	**20**
Wafer thickness (mm)	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**
Maximum I/O pads	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**
Chuck positioning accuracy						
X & Y (µm)	**2**	**2**	**2**	**2**	**2**	**2**
Z (µm)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Co-planarity (µm)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Probe-to-pad alignment (µm)	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Maximum chuck force (kg)	**100**	**100**	**100**	**100**	**100**	**100**
Parallel testing	**2X**	**2X**	**2X**	**2X**	**2X**	**2X**
Set point range (degrees C)	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**
Temperature accuracy (degrees C)	**-1**	**-1**	**-1**	**-1**	**-1**	**-1**
Total power (Watts)	**250**	**250**	**250**	**300**	**300**	**300**
Power density (Watt/cm^2)	**120**	**120**	**120**	**120**	**120**	**120**
Chuck leakage (picoampere)	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**
Foot print (ratio)	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**	**1.3–1.5**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

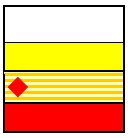


Table 40 Memory Test Handler Difficult Challenges

Challenge	***Issue/Goal***
Package Form Factors	Variety of sizes, thicknesses, and ball pitches requires kitless handlers with thin-die handling capability
Ball-to-package Edge Gap	As this decreases from 0.6 mm to 0 mm, new handling and socketing methods must be introduced
Massive Parallelism	Parallelism at x128 and up to x256 on roadmap, thermal, and alignment challenges

Table 41 Logic Test Handler Difficult Challenges

Challenge	***Issue/Goal***
Thermal Control	Improved temperature control and temperature rise control due to high power densities during test
Operations Improvements	Continuous lot processing (lot cascading), auto-retest, asynchronous device socketing, low-conversion times
ESD	Products more sensitive to ESD while on-die protection circuitry increases cost.
Packaging Technology	Lower stress socketing, low-cost change kits, higher I/O count, heat lids change thermal characteristics

Table 42 Network and Communications Test Handler Difficult Challenges

Challenge	***Issue/Goal***
New Packaging Technologies	Known good die solutions (KGD), stacked die packaging, thin die packaging
Temperature Control	Wide range tri-temperature soak requirements (-45ºC to 150ºC) increases system complexity
Operations Improvements	Continuous lot processing (lot cascading), auto-retest, low conversion times, asynchronous operation
EMI/RF up to 40 GHz	Shielding issues associated with high frequency testing (>10 GHz)

Table 43 Logic Test Prober Difficult Challenges

Challenge	***Issue/Goal***
Thermal contact resistance between wafer and chuck	The high thermal resistance and variation in contact resistance across chuck are required to improve temperature control and reduce temperature rise of device under test
Heat dissipation at elevated temperature	Heat dissipation of >100 Watts at >85ºC is a configuration gap in the prober industry
Probe card optical standardization	With advancement in probe card technology a new optical alignment methodology must be developed

DEVICE INTERFACE TECHNOLOGY REQUIREMENTS

As device analog and digital I/O bandwidth and power demands increase there is an associated requirements for high performance power and signal delivery. These requirements drive challenges for the assemblies used to interface the test equipment to the device-under-test. The highest performance interfaces require complete power and signal path modeling from the source instrument to the die, requiring accurate simulation models of the test instrument, path, probe or socket, and die. To further complicate matters, shrinking die and package geometries further complicate these interfaces with decreasing pitch and increasing pin count mechanical requirements.

PROBE CARDS

Wafer probe technologies face complex electrical and mechanical challenges driven by product specifications, test implementation requirements, test productivity goals, and reduced test cost demands. Across the device spectrum, these challenges include: higher frequency response (bandwidth), rising pin counts across tighter pitches and smaller pads/bumps, increasing switching currents (di/dt), alternative pad/bump metallurgies and increasing test parallelism. Research and development of new or improved probe technologies is required to meet these challenges to ensure that the basic probing requirement of ensuring reliable, sound and cost-effective electrical contact to the device(s) under test (DUT) is achieved.

The tables contained in this section derive trends based on product families similar to the layout of the Test Technology Requirements section above. In addition, tables that trend probe card requirements based on established probe

technologies are included in the *supplemental material*. This contribution represents a significant contribution from the Japan region.

TRENDS AFFECTING PROBE CARD TECHNOLOGIES

Along with addressing the key challenges listed below, research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment.

The continuing volume growth (share of market) of bumped devices, often with I/Os in area arrays, points to the escalating demand for "vertical" style probe card technologies, with a rising need in multi-DUT configurations as well.

Increasingly, manufacturing test of devices is moving to parallel test. For some product groups (e.g., memory), current wafer probe technologies handle parallel testing of 32, 64, and even 128 devices. Probe technologies capable of further increases in parallelism, including up to full wafer (up to 300 mm), are needed to drive test costs lower. For some high pin count products, e.g., ASICS, parallel probing requirements are emerging. To achieve full wafer probing, the number of probed I/Os per die may need to be restricted. DFT techniques must be considered to achieve full wafer probing of commodity Flash Memory.

Wafer probe electrical models that integrate models of other elements in the path from tester to DUT will be required of probe card suppliers. These models will be needed to conduct simulations of increasingly complex automated test equipment (ATE) to DUT interface networks to optimize performance at the DUT.

As new or advanced probe technologies are entering the marketplace, issues of single-sourcing, order to delivery time, probe lifetime, application support, and reparability are important and essential considerations in the selection of a probe card for use in volume production.

PROBE CARD TECHNOLOGY REQUIREMENTS

Many probe card technology types are available in the marketplace, each with suitability (technical and/or test operations driven) for probing certain device types and limitations that prevent more widespread use. There is no single probe technology capable of addressing the requirements across the entire device spectrum.

Table 44 Probe Card Difficult Challenges—Near-term

Challenge	*Issue / Goal*
High Frequency Probing	Traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz.
Geometry	Probe technologies to support peripheral fine pitch probe of 25 µm, peripheral staggered pad probes at effective pitches of 20/40, and fine pitch (45 µm) for dual row, non-staggered probing on all four die sides. Fine pitch vertical probe technologies to support 100 µm pitch solder bump and staggered pad devices Alternative probe technology for 75 µm on 100 µm pitch dense array (vertical probe; bumped device) Increasing probe array planarity requirements in combination with increasing array size.
Parallel Test	Need a probe technology to handle the complexity of System On Chip (SoC) devices while probing more than one device. Current probe technologies have I/O limitations for bumped device probes
Probing at Temperature	Reduce effects on probes for non-ambient testing -40 to 150°C; especially for fine-pitch devices For effects on Handlers and Probers, see that section.
Product	Probe technologies to direct probe on copper bond pads including various oxidation considerations Probe technologies for probing over active circuitry (including flip-chip) Reduction of probe force requirements to eliminate die damage, including interlayer dielectric damage with low-κ dielectrics
Probe Cleaning	Development of *in situ* cleaning mediums/methods, particularly for fine pitch, multi-DUT and non-traditional probes Reduction of cleaning requirements while maintaining electrical performance to increase lifetime
Cost and Delivery	Fine pitch or high pin count probe cards are too expensive and take too long to build. Time and cost to repair fine pitch or high pin count probe cards is very high. The time between chip design completion ("tape-out") and the availability of wafers to be probed is less than the time required to design and build a probe card in almost every probe technology except traditional cantilever. Space transformer lead-times are too long, thus causing some vertical probe technologies to have lengthy lead-times.
Probe Metrology	Tools are required that support fine pitch probe characterization and pad damage measurements Metrology correlation is needed—repair versus on-floor usage

This section explores the challenges that are required of probe technologies independent of those driven by the devices being probed. These include the resulting behavior of the probe when/after contacting the wafer, the design of the probe card to realize the productivity benefits of probing multiple die at the same time and the environment that the probe card is expected to operate within.

PITCH AND INTERCONNECT DEFORMATION

I/O density requirements are driving pad/bump sizes to ever-smaller sizes. It is well known that on the leading edge, wirebond pad pitches are under 50 µm (with resulting pad sizes naturally less than that). It is a formidable challenge for traditional probe technologies to continually scale down when with this scaling comes a parallel scaling-down of the permissible probe mark.

The use of cantilever probe cards for probing wirebond technologies, though still today's leading solution, is seen to be reaching practical limits in pitch and scrub within the nearer term horizon. Thus the newer emerging technologies, many using “semiconductor-like” processes may offer solutions for reduced pitch scrub requirements.

Area array solder bumps are seeing growing application and the commensurate need/demand for vertical probing technologies. Though pitch reductions are foreseen, reductions may be delayed until 2nd level packaging constraints are resolved. As the pitch/bump dimensions get smaller, current vertical technologies, typically an array of guided wires, may also see their practical limit, thus requiring development of newer technologies.

MULTI-DUT

Productivity gains are often realized when testing (probing) more than one device in parallel. Memory testing has been a leader in this area, with leading edge approaching 200 devices in parallel. As the table below indicates virtually all memory testing is done in multi-DUT fashion. The move to multiple DUT testing within other product categories is already underway and is accelerating: with the use of DFT and “smart test” techniques, 16, 32, and even 64 DUTs is realizable

Multi-DUT probing requirements drive the need for more and more probe contacts across an ever-growing area. Ultimately contacting the entire wafer will be required and today some new contact/probe technologies claim full wafer contact capability or very close to it.

ELECTRICAL PERFORMANCE

Wafer probe technology—the probe card—provides electrical contact between the device(s) under test on a wafer and the test system electronics. The probe card must faithfully transmit/deliver device under test power and signals from/to the test system.

Within this ITRS document information can be found concerning device operating voltages and AC Characteristics. Additionally, within this Test and Test Equipment chapter tester performance information is provided on a wide range of electrical characteristics that may be helpful in understanding requirements for wafer probing.

There appears to be small growth in the current carrying capability of individual probes contacts, however, the aggregate total current across the DUT is expected to rise with growing circuit densities and pin counts. Of note is that there are some selected applications that are seeing the need for higher and growing current carrying capability, approaching 1 amp or more. Of note is that peak values for transient currents are growing as well.

Contact resistance is always a closely watched probe technology parameter. It is influenced by many factors such as pad/bump metallurgy, contamination from pads/bumps, multi-DUT “off-stepping,” contact force, scrub, cleaning, etc. The values shown in the requirements table reflect contact resistance under ‘normal’ usage conditions over the practical lifetime of the probe. Initial and after cleaning requirements are often considerably lower, typically in the 200 milli-Ohm range or lower. There is a growing requirement for lower contact resistance values for longer periods (numbers of touchdowns) before cleaning.

THERMAL PERFORMANCE

Though stable through the roadmap horizon, the thermal environment for the probe is demanding. With low end chuck set-point requirements well below the freezing point and the upper end past the boiling point, the total range is wide -

placing difficult demands on selecting materials that handle the extremes, but possibly more notably to deal with temperature co-efficient of expansion issues.

Additionally, handling the heat produced by very high transient current heating effects and/or by high power products, indicate the need for active thermal management within probers.

UNIT COST AND COST OF OWNERSHIP

Probe card unit cost and cost of ownership (COO) trends are not currently covered in this roadmap document. Though individual member companies may have their own approaches to unit cost and cost of ownership measurements and goals, there is a need to develop consistent models that can be used industry wide, that cover the wide range of probe card technologies that are in the marketplace.

LEAD-TIME

Driven by the accelerating pace of new design introductions and 'shrinks', lead-time requirements for initial orders and re-orders are trending rapidly downward. During this roadmap's horizon, lead-times are reduced by ~50%. The growing percentage of wafers that are tested in multi-DUT fashion, with more complicated probe assemblies, magnify the task of achieving the desired lead-times. Strategies, and perhaps technologies, that enable realizing lead-time reduction are needed.

CLEANING

Generally, online cleaning frequency for cantilever type probes rises slightly through the roadmap horizon, however increasing probe usage (touchdowns) before taking offline for cleaning is being seen for many of the product families. The goal is better utilization of the test systems and the probe.

For vertical probes, the rapidly growing number of touchdowns before online cleaning reflects a desire to reduce the vertical technologies' online cleaning frequency to more closely match/better cantilever technologies. Similar to cantilever technologies, the touchdowns before offline cleaning is increasing but across all product categories.

Notably, in some instances there is a move to eliminate online cleaning for memory products in the outer years of this roadmap's horizon. This is likely reflective of the design and/or complexity of probes with pin counts approaching full wafer contact.

Table 45a Wafer Probe Technology Requirements—Near-term

Year of Production	*2003*		*2004*		*2005*		*2006*		*2007*		*2008*		*2009*	
Technology Node			*hp90*						*hp65*					
DRAM ½ Pitch (nm)	*100*		*90*		*80*		*70*		*65*		*57*		*50*	
MPU/ASIC ½ Pitch (nm)	*107*		*90*		*80*		*70*		*65*		***57***		***50***	
MPU Printed Gate Length (nm)	*65*		*53*		*45*		*40*		*35*		*32*		*28*	
MPU Physical Gate Length (nm)	*45*		*37*		*32*		*28*		*25*		*22*		*20*	
I/O Pad Size (µm)	**X**	**Y**	**X**	**Y**	**X**	**Y**	**X**	**Y**	**X**	**Y**	**X**	**Y**	**X**	**Y**
Wirebond	**40**	**70**	**35**	**60**	**35**	**60**	**30**	**55**	**30**	**55**	**25**	**45**	**25**	**45**
Bump	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**60**	**60**	**60**	**60**
Scrub (% of I/O)	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**
Wirebond	**25**	**75**	**25**	**75**	**25**	**50**	**25**	**50**	**25**	**50**	**20**	**40**	**20**	**40**
Bump	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Multi-DUT Volume (% of Total Product Type Wafers Probed)														
Memory (DRAM)	**99.9**		**99.9**		**99.9**		**99.9**		**99.9**		**99.9**		**99.9**	
ASIC	**33**		**45**		**50**		**60**		**75**		**75**		**75**	
Microprocessor	**60**		**75**		**75**		**75**		**85**		**85**		**85**	
RF	**30**		**40**		**45**		**50**		**50**		**60**		**60**	
Mixed-signal	**40**		**45**		**45**		**45**		**50**		**50**		**50**	
Size of Probed Area (mm^2)														
Memory (DRAM)	**64 to 192 devices**		**64 to 380 devices**		**100% of wafer**		**100% of wafer**		**100% of wafer**		**100% of wafer**		**100% of wafer**	
ASIC	**1560**		**1700**		**2050**		**2050**		**2050**		**2400**		**2400**	
Microprocessor	**1560**		**1700**		**2050**		**2050**		**2050**		**2400**		**2400**	
RF	**625**		**625**		**900**		**900**		**1225**		**1225**		**1225**	
Mixed-signal	**1063**		**1225**		**1413**		**1413**		**1600**		**1600**		**1600**	
Number of Probe Points /Touchdown	**Signal**	**Total**	**Signal**	**Total**	**Signal**	**Total**	**Signal**	**Total**	**Signal**	**Total**	**Signal**	**Total**	**Signal**	**Total**
Memory (DRAM)	**1730-5180**	**2240-6720**	**1730-10260**	**2240-13300**	**14500**	**18700**	**14500**	**18700**	**14500**	**18700**	**14500**	**18700**	**14500**	**18700**
ASIC	**775**	**1550**	**950**	**1900**	**1050**	**2100**	**1050**	**2100**	**1050**	**2100**	**1200**	**2400**	**1200**	**2400**
Microprocessor	**310**	**925**	**400**	**1200**	**450**	**1350**	**450**	**1350**	**450**	**1350**	**560**	**1675**	**560**	**1675**
RF	**180**	**325**	**235**	**425**	**250**	**450**	**250**	**450**	**350**	**630**	**350**	**630**	**350**	**630**
Mixed-signal	**375**	**500**	**375**	**500**	**450**	**600**	**450**	**600**	**510**	**680**	**510**	**680**	**510**	**680**
Maximum Current (mA)	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**	**Probe Tip**	**DC Leakage**
Memory (DRAM)	**100**	**<10**	**100**	**<10**	**100**	**<10**	**125**	**<10**	**125**	**<10**	**125**	**<10**	**125**	**<10**
ASIC	**350**	**<10**	**350**	**<10**	**350**	**<10**	**400**	**<10**	**400**	**<10**	**400**	**<10**	**400**	**<10**
Microprocessor	**275**	**<10**	**275**	**<10**	**275**	**<10**	**325**	**<10**	**325**	**<10**	**325**	**<10**	**325**	**<10**
RF	**200**	**<10**	**200**	**<10**	**200**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**
Mixed-signal	**250**	**<10**	**250**	**<10**	**250**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
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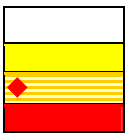

Table 45a Wafer Probe Technology Requirements—Near-term (continued)

Year of Production	*2003*		*2004*		*2005*		*2006*		*2007*		*2008*		*2009*	
Technology Node			*hp90*						*hp65*					
DRAM ½ Pitch (nm)	*100*		*90*		*80*		*70*		*65*		*57*		*50*	
MPU/ASIC ½ Pitch (nm)	*107*		*90*		*80*		*70*		*65*		***57***		***50***	
MPU Printed Gate Length (nm)	*65*		*53*		*45*		*40*		*35*		*32*		*28*	
MPU Physical Gate Length (nm)	*45*		*37*		*32*		*28*		*25*		*22*		*20*	
Maximum Resistance (Ohm)	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**
Memory (DRAM)	**<1**	**<4**	**<1**	**<4**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**
ASIC	**<1**	**<4**	**<1**	**<4**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**
Microprocessor	**<1**	**<3**	**<1**	**<3**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**
RF	**<1**	**<2**	**<1**	**<2**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**
Mixed-signal	**<1**	**<2**	**<1**	**<2**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**
Chuck Set-point (°C)	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
Memory (DRAM)	**-40**	**140**	**-40**	**140**	**-40**	**140**	**-40**	**140**	**-40**	**140**	**-40**	**140**	**-40**	**140**
ASIC	**25**	**100**	**25**	**110**	**25**	**110**	**25**	**110**	**25**	**110**	**25**	**110**	**25**	**110**
Microprocessor	**-20**	**125**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**
RF	**10**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**
Mixed-signal	**25**	**115**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**
Soak Time (minutes)														
Memory (DRAM)	**10**		**10**		**10**		**8**		**8**		**8**		**7**	
ASIC	**8**		**8**		**8**		**7**		**7**		**7**		**6**	
Microprocessor	**13**		**13**		**10**		**10**		**10**		**9**		**9**	
RF	**10**		**10**		**10**		**10**		**9**		**9**		**9**	
Mixed-signal	**10**		**10**		**10**		**10**		**9**		**9**		**9**	
Order Lead-time—Single DUT (weeks)	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**
Memory (DRAM)	**8**	**4**	**8**	**4**	**6**	**3**	**5.5**	**3**	**5**	**3**	**4**	**2**	**4**	**2**
ASIC	**4**	**2**	**4**	**2**	**2.5**	**1.5**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**
Microprocessor	**4**	**2**	**4**	**2**	**2.5**	**1.5**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**
RF	**5**	**2**	**5**	**2**	**4**	**2**	**3.5**	**1.5**	**3.5**	**1.5**	**3**	**1**	**3**	**1**
Mixed-signal	**3**	**2**	**3**	**2**	**3**	**2**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**
Order Lead-time—Multi-DUT (weeks)	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**
Memory DRAM)	**9**	**6**	**8**	**5**	**7**	**4**	**6**	**3**	**5**	**3**	**4.5**	**2.5**	**4.5**	**2.5**
ASIC	**6**	**2**	**6**	**2**	**5**	**2**	**4**	**1.5**	**3.5**	**1.5**	**3**	**1**	**3**	**1**
Microprocessor	**6**	**2**	**5**	**2**	**4**	**2**	**4**	**1.5**	**3.5**	**1.5**	**3**	**1**	**3**	**1**
RF	**7**	**3**	**6**	**3**	**5**	**3**	**4.5**	**2**	**4**	**1.5**	**4**	**1**	**4**	**1**
Mixed-signal	**5**	**2**	**5**	**2**	**4**	**2**	**3.5**	**2**	**3**	**1.5**	**3**	**1**	**3**	**1**

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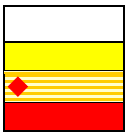

Table 45a Wafer Probe Technology Requirements—Near-term (continued)

Year of Production	*2003*		*2004*		*2005*		*2006*		*2007*		*2008*		*2009*	
Technology Node			*hp90*						*hp65*					
DRAM ½ Pitch (nm)	*100*		*90*		*80*		*70*		*65*		*57*		*50*	
MPU/ASIC ½ Pitch (nm)	*107*		*90*		*80*		*70*		*65*		***57***		***50***	
MPU Printed Gate Length (nm)	*65*		*53*		*45*		*40*		*35*		*32*		*28*	
MPU Physical Gate Length (nm)	*45*		*37*		*32*		*28*		*25*		*22*		*20*	
Touchdowns Before Clean (Cantilever)	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**
Memory (DRAM)	**300**	**15,000**	**400**	**20,000**	**400**	**20,000**	**400**	**20,000**	**450**	**20,000**	**450**	**20,000**	**450**	**20,000**
ASIC	**3,250**	**57,500**	**3,250**	**60,000**	**3,250**	**60,000**	**3,500**	**60,000**	**3,500**	**60,000**	**3,500**	**60,000**	**3,500**	**60,000**
Microprocessor	**1,250**	**50,000**	**1,250**	**50,000**	**1,250**	**50,000**	**1,500**	**50,000**	**1,500**	**50,000**	**1,500**	**50,000**	**1,500**	**50,000**
RF	**1,000**	**100,000**	**1,000**	**100,000**	**1,000**	**100,000**	**1,000**	**100,000**	**1,000**	**100,000**	**1,000**	**100,000**	**1,000**	**100,000**
Mixed-signal	**2,000**	**150,000**	**2,000**	**175,000**	**2,000**	**200,000**	**2,000**	**200,000**	**2,000**	**200,000**	**2,000**	**200,000**	**2,000**	**200,000**
Touchdowns Before Clean (Vertical)	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**	**Online**	**Offline**
Memory (DRAM)	**1,000**	**15,000**	**1,500**	**20,000**	**1,500**	**20,000**	**2,000**	**25,000**	**2,000**	**25,000**	**2,000**	**25,000**	**2,500**	**27,500**
ASIC	**1,000**	**15,000**	**1,500**	**17,500**	**1,500**	**17,500**	**2,000**	**20,000**	**2,000**	**20,000**	**2,000**	**20,000**	**2,500**	**22,500**
Microprocessor	**1,000**	**32,500**	**1,500**	**35,000**	**1,500**	**35,000**	**2,000**	**37,500**	**2,000**	**37,500**	**2,000**	**37,500**	**2,500**	**40,000**
RF	**100**	**15,000**	**100**	**20,000**	**100**	**20,000**	**100**	**25,000**	**100**	**25,000**	**125**	**25,000**	**125**	**27,500**
Mixed-signal	**1,000**	**82,500**	**1,500**	**85,000**	**1,500**	**85,000**	**2,000**	**87,500**	**2,000**	**87,500**	**2,000**	**87,500**	**2,500**	**90,000**

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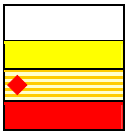

Table 45b Wafer Probe Technology Requirements—Long-term

Year of Production	*2010*	*2012*		*2013*	*2015*		***2016***	*2018*	
Technology Node	*hp45*			*hp32*			***hp22***		
DRAM ½ Pitch (nm)	*45*	*35*		*32*	*25*		*22*	*18*	
MPU/ASIC ½ Pitch (nm)	*45*	*32*		*28*	*22*		*20*	*18*	
MPU Printed Gate Length (nm)	*25*	*20*		*18*	*14*		*13*	*10*	
MPU Physical Gate Length (nm)	*18*	*14*		*13*	*10*		*9*	*7*	
I/O Pad Size (um)		**X**	**Y**		**X**	**Y**		**X**	**Y**
Wirebond		**20**	**35**		**15**	**25**		**15**	**25**
Bump		**50**	**50**		**50**	**50**		**50**	**50**
Scrub (% of Pad)		**AREA**	**DEPTH**		**AREA**	**DEPTH**		**AREA**	**DEPTH**
Wirebond		**20**	**40**		**20**	**40**		**20**	**40**
Bump		**30**	**30**		**30**	**30**		**30**	**30**
Volume (% of Total Product Type Wafers Probed)									
Memory (DRAM)		**99.9**			**99.9**			**99.9**	
ASIC		**75**			**75**			**75**	
Microprocessor		**85**			**85**			**85**	
RF		**60**			**60**			**60**	
Mixed-signal		**50**			**50**			**50**	
Size of Probed Area (mm^2)									
Memory (DRAM)		**100% of wafer**			**100% of wafer**			**100% of wafer**	
ASIC		**2400**			**2400**			**2400**	
Microprocessor		**2400**			**2400**			**2400**	
RF		**1225**			**1225**			**1225**	
Mixed-signal		**1600**			**1600**			**1600**	
Number of Probe Points/Touchdown		**Signal**	**Total**		**Signal**	**Total**		**Signal**	**Total**
Memory (DRAM)		**14500**	**18700**		**14500**	**18700**		**14500**	**18700**
ASIC		**1200**	**2400**		**1200**	**2400**		**1200**	**2400**
Microprocessor		**560**	**1675**		**560**	**1675**		**560**	**1675**
RF		**350**	**630**		**350**	**630**		**350**	**630**
Mixed-signal		**510**	**680**		**510**	**680**		**510**	**680**
Maximum Current (mA)		**Probe Tip**	**DC Leakage**		**Probe Tip**	**DC Leakage**		**Probe Tip**	**DC Leakage**
Memory (DRAM)		**125**	**<10**		**125**	**<10**		**125**	**<10**
ASIC		**400**	**<10**		**400**	**<10**		**400**	**<10**
Microprocessor		**325**	**<10**		**325**	**<10**		**325**	**<10**
RF		**225**	**<10**		**225**	**<10**		**225**	**<10**
Mixed-signal		**275**	**<10**		**275**	**<10**		**275**	**<10**
Maximum Resistance (Ohm)		**Contact**	**Series**		**Contact**	**Series**		**Contact**	**Series**
Memory (DRAM)		**<0.5**	**<3**		**<0.5**	**<3**		**<0.5**	**<3**
ASIC		**<0.5**	**<3**		**<0.5**	**<3**		**<0.5**	**<3**
Microprocessor		**<0.5**	**<2**		**<0.5**	**<2**		**<0.5**	**<2**
RF		**<0.5**	**<1.5**		**<0.5**	**<1.5**		**<0.5**	**<1.5**
Mixed-signal		**<0.5**	**<1.5**		**<0.5**	**<1.5**		**<0.5**	**<1.5**

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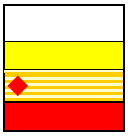


Table 45b Wafer Probe Technology Requirements—Long-term (continued)

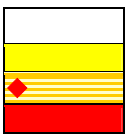
Year of Production	*2010*	*2012*		*2013*	*2015*		***2016***	*2018*	
Technology Node	*hp45*			*hp32*			***hp22***		
DRAM ½ Pitch (nm)	*45*	*35*		*32*	*25*		*22*	*18*	
MPU/ASIC ½ Pitch (nm)	*45*	*32*		*28*	*22*		*20*	*18*	
MPU Printed Gate Length (nm)	*25*	*20*		*18*	*14*		*13*	*10*	
MPU Physical Gate Length (nm)	*18*	*14*		*13*	*10*		*9*	*7*	
Chuck Set-point (°C)		**Min.**	**Max.**		**Min.**	**Max.**		**Min.**	**Max.**
Memory (DRAM)		**-40**	**140**		**-40**	**140**		**-40**	**140**
ASIC		**25**	**110**		**25**	**110**		**25**	**110**
Microprocessor		**-30**	**135**		**-30**	**135**		**-30**	**135**
RF		**5**	**120**		**5**	**120**		**5**	**120**
Mixed-signal		**25**	**125**		**25**	**125**		**25**	**125**
Soak Time (Minutes)									
Memory (DRAM)		**7**			**7**			**7**	
ASIC		**6**			**6**			**6**	
Microprocessor		**9**			**9**			**9**	
RF		**9**			**9**			**9**	
Mixed-signal		**9**			**9**			**9**	
Order Lead-time—Single DUT (weeks)		**1st Order**	**Re-Order**		**1st Order**	**Re-Order**		**1st Order**	**Re-Order**
Memory (DRAM)		**4**	**2**		**4**	**2**		**4**	**2**
ASIC		**2**	**1**		**2**	**1**		**2**	**1**
Microprocessor		**2**	**1**		**2**	**1**		**2**	**1**
RF		**3**	**1**		**3**	**1**		**3**	**1**
Mixed-signal		**2**	**1**		**2**	**1**		**2**	**1**
Order Lead-time—Multi-DUT (weeks)		**1st Order**	**Re-Order**		**1st Order**	**Re-Order**		**1st Order**	**Re-Order**
Memory (DRAM)		**4.5**	**2.5**		**4.5**	**2.5**		**4.5**	**2.5**
ASIC		**3**	**1**		**3**	**1**		**3**	**1**
Microprocessor		**3**	**1**		**3**	**1**		**3**	**1**
RF		**4**	**1**		**4**	**1**		**4**	**1**
Mixed-signal		**3**	**1**		**3**	**1**		**3**	**1**
Touchdowns Before Cleaning (Cantilever)		**Online**	**Offline**		**Online**	**Offline**		**Online**	**Offline**
Memory (DRAM)		**450**	**20,000**		**450**	**20,000**		**450**	**20,000**
ASIC		**3,500**	**60,000**		**3,500**	**60,000**		**3,500**	**60,000**
Microprocessor		**1,500**	**50,000**		**1,500**	**50,000**		**1,500**	**50,000**
RF		**1,000**	**100,000**		**1,000**	**100,000**		**1,000**	**100,000**
Mixed-signal		**2,000**	**200,000**		**2,000**	**200,000**		**2,000**	**200,000**
Touchdowns Before Cleaning (Vertical)		**Online**	**Offline**		**Online**	**Offline**		**Online**	**Offline**
Memory (DRAM)		**2,500**	**27,500**		**2,500**	**27,500**		**2,500**	**27,500**
ASIC		**2,500**	**22,500**		**2,500**	**22,500**		**2,500**	**22,500**
Microprocessor		**2,500**	**40,000**		**2,500**	**40,000**		**2,500**	**40,000**
RF		**125**	**27,500**		**125**	**27,500**		**125**	**27,500**
Mixed-signal		**2,500**	**90,000**		**2,500**	**90,000**		**2,500**	**90,000**

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



POTENTIAL SOLUTIONS

Figure 21 shows the high level Potential Solutions for Test and Test Equipment.

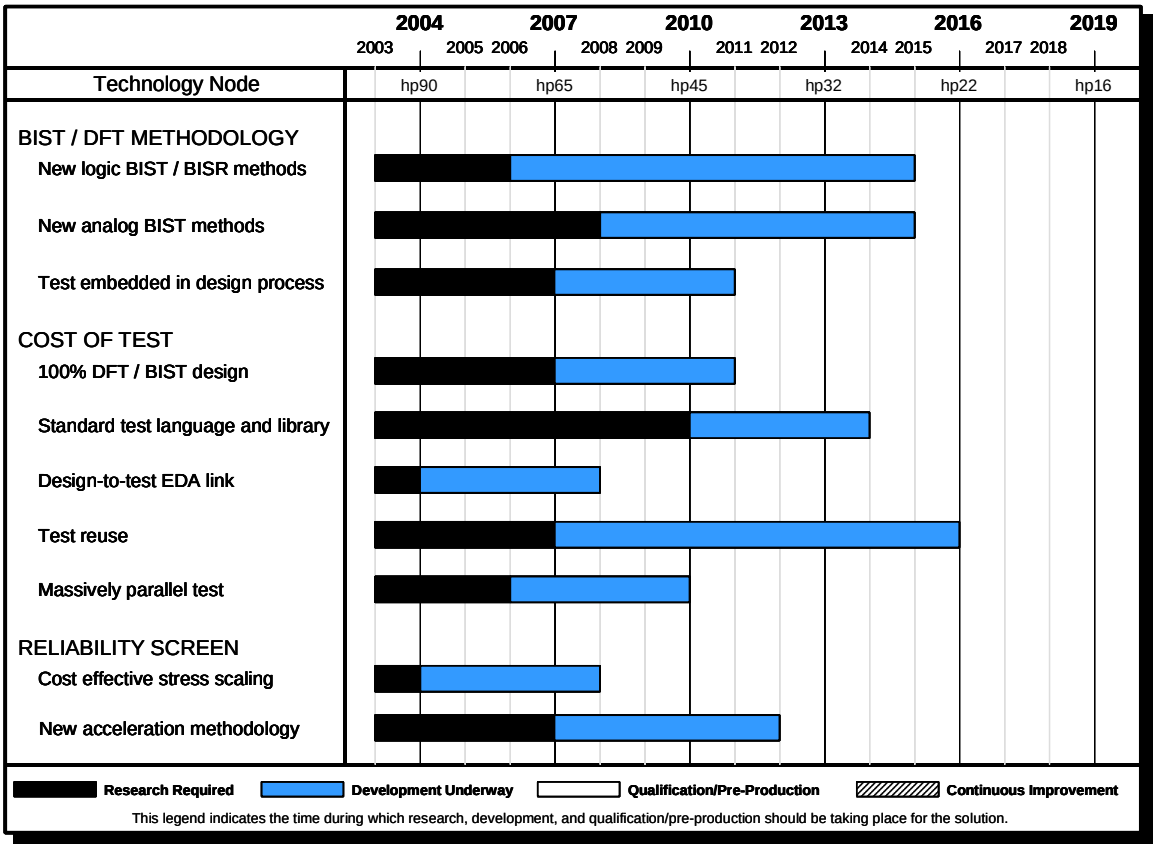


Figure 21 Test and Test Equipment Potential Solutions

CROSS-CUT ISSUES

MODELING AND SIMULATION

Modeling and simulation of test equipment instrument, electrical delivery path, probe card or loadboard, and the device-under-test are among the short-term challenges of the Test ITWG. Most important for Test is the signal integrity of power delivery of high-speed signals. Whereas modeling of these issues can built especially upon the field of interconnect and package simulation, some of the issues (for example, probe card) to be described are outside the classical domains of simulation considered by the Modeling and Simulation ITWG. It is, however, encouraged that the simulation community would extend their activities to also contribute to these problems that are important to support test activities.