INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS [A SECTION OF THE PROCESS INTEGRATION CHAPTER]

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RF AND AMS TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

SCOPE

Radio frequency and analog/mixed-signal (RF and AMS) technologies now represent essential and critical technologies for the success of many semiconductor products. Such technologies serve the rapidly growing wireless communications market. They depend on many materials systems, some of which are compatible with complementary metal oxide semiconductor (CMOS) processing, such as SiGe and others of which are not compatible with CMOS processing such as those compound semiconductors composed of elements from group III and V in the periodic table.

Recognizing wireless applications, which are enabled by RF and AMS technologies, as a new system driver for the ITRS, the International Roadmap Committee (IRC) requested that III-V compound semiconductor devices be discussed in technical detail in the 2003 ITRS. Unlike the IRC guidelines for 2001 ITRS, this IRC request also included addressing semiconductor market requirements that are likely to be met by products from CMOS compatible processing and those that are likely to be met by products from processing that is not compatible with CMOS processing.

The purposes of this 2003 ITRS RF and AMS section are as follows:

1. Present the challenges that RF and AMS technologies have in meeting the demands of wireless applications for cellular phones, wireless local area networks, wireless personal area networks (PAN), phased array RF systems, and other emerging wireless communication applications operating between 0.8 GHz and 100 GHz.
2. Address the intersection of Si CMOS, BiCMOS, and SiGe heterojunction bipolar transistors (HBTs) with III-V compound semiconductor devices. The co-integration of products from CMOS compatible and CMOS incompatible processing is expected to be addressed more fully in future editions of the ITRS than it is in this 2003 section.

The 2001 ITRS System Drivers chapter updated past drivers to include dynamic random-access memory (DRAM), system-on-chip (SOC), analog/mixed-signal (AMS), and microprocessors (MPU). Compound semiconductors were mentioned in its paragraphs on mixed-signal evolution in the context of improving the performance for analog to digital converters. The 2003 ITRS significantly expands RF and AMS technologies in this new section.

This section has four main sub-sections on analog/mixed-signal (0.8–10 GHz frequency range), RF Transceivers (0.8-10 GHz), power amplifiers and power management (0.8–10 GHz), and millimeter wave (10–100 GHz). The first two sub-sections are based on extending tables from the AMS Table 39 in the ITRS 2001. The last two sub-sections are new for the 2003 ITRS. The frequency region between about 10 GHz and 40 GHz is the region in which the interplay and competition among elemental and compound semiconductors is expected to occur. Today, group IV semiconductors (Si and SiGe) dominate below 10 GHz and III-V compound semiconductors dominate above 40 GHz. This range in frequencies for competition amongst elemental and compound semiconductors changes with time and is expected to move to high frequencies. Nevertheless, while SiGe has shown capability in the 10–40 Gbits range, it is unlikely to replace III-Vs in applications where either high power gain or ultra low noise is required.

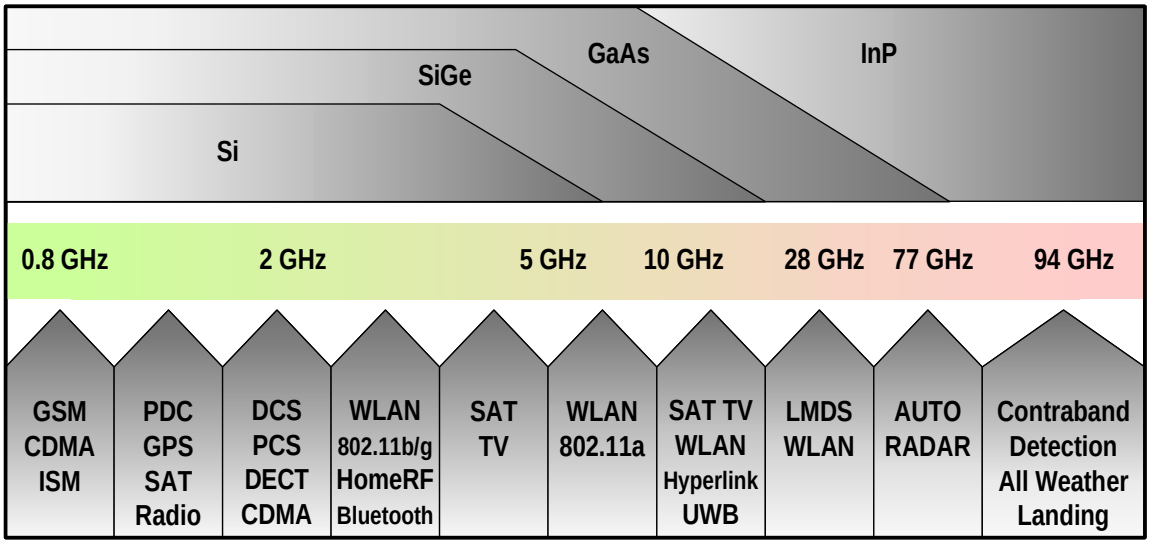

Figure 30 Application Spectrum[1]

Figure 30 schematically presents the scope of this section in terms of the interplay among commercial wireless communication applications, available spectrum, and the kinds of elemental and compound semiconductors likely to be used. The consumer portions of wireless communications markets are very sensitive to cost. As a result, developing RF and AMS technology roadmaps on such applications is not straightforward. Cost is one of the key factors determining the location of boundaries between the kinds of RF semiconductors (e.g., Si, SiGe, GaAs, and InP) shown in the top part of Figure 30. These boundaries are broad, diffuse, and change with time. The boundary between the group IV semiconductors Si and SiGe and the III-V semiconductor GaAs has been moving to higher frequencies with time and for other applications the boundary between GaAs and InP is tending to shift to lower frequencies. And eventually, metamorphic high electron mobility transistors (MHEMTs) may displace both GaAs pseudomorphic high electron mobility transistors (PHEMTs) and InP high electron mobility transistors (HEMTs). The wide bandgap semiconductors such as SiC and GaN, which are not shown in Figure 30, will be used for infrastructure such as base stations at frequencies typically above about 2 GHz. Increased interests for the 94 GHz band arises from its applications for all weather landing, contraband detection, and other security needs. III-V compound semiconductors have additional metrics than those usually associated with CMOS processes. These other metrics include carrier frequency for wireless applications and the printed gate length.

In future years, we expect the frequency axis in Figure 30 will lose its significance in defining the boundaries among technologies for some of the applications listed therein. This expectation occurs because most of the technologies in Figure 30 can provide very high operating frequencies. The future boundaries will be dominated more by such parameters as noise figure, output power, power added efficiency, and linearity. Performance tends to increase in the following order: Si CMOS, SiGe, GaAs, InP metamorphic. Two or more technologies may coexist with one another for certain applications such as cellular transceivers, modules for terminal power amplifiers, and millimeter wave (mm-wave) receivers. Today, bipolar CMOS (BiCMOS) in cellular transceivers has the biggest share in terms of volume compared to CMOS. But, the opposite may occur in the future. Today, both GaAs HBT and discrete laterally diffused metal oxide semiconductor (LDMOS) devices in modules for terminal power amplifiers have big market shares compared to GaAs PHEMT and GaAs metal semiconductor field effect transistor (MESFET). In the future, silicon based technologies having higher integration capabilities will gain importance. Today we see GaAs PHEMT and InP HEMT in mm-wave receivers. In the future, we may see competition from SiGe HBT, GaAs MHEMT and InP HEMT.

The drivers for wireless communications systems are cost, available frequency bands, power consumption, functionality, size of mobile units, very high volumes of product, appropriate performance requirements, and standards and protocols.

[1] *Adapted from Fig. 1 in Microwave Journal of the paper by D. Barlas, et. al., page 22, June 1999 and printed with permission from the Editor, Microwave Journal.*

Standards and protocols influence considerably parameters such as operating frequencies, channel bandwidth, and transmit power. Also, RF technologies often require additional headroom with respect to performance because several conflicting or competing requirements have to be met simultaneously. These include power added efficiency (PAE), high output power, low current, and low voltage. Increased RF performance for silicon is usually achieved by geometrical scaling. Increased RF performance for III-V compound semiconductors is achieved by optimizing carrier transport properties through materials and bandgap engineering. During the last two decades, technologies based on III-V compounds have established new business opportunities for wireless communications systems. When high volumes of product are expected, silicon and more recently silicon-germanium replace the III-Vs in those markets for which these group IVs can deliver appropriate performance at low cost.

In addition to the foregoing technical drivers, other wireless communication industries' drivers exist for RF and AMS technologies. They include the following: 1) regulations from various governments that determine the frequency availability and 2) standards and protocols that determine frequency channels and their bandwidths and that also impact overall system performance. Situations may occur where national or regional standards and protocols influence international technical competition. While beyond the scope of this section, they are mentioned to provide another perspective on the broader context in which to view RF and AMS technologies. Such drivers often affect advances in RF and AMS technologies much more than they affect advances in many of the other technologies described in this 2003 ITRS.

Electronic design and automation (EDA) software tools are not equipped today to handle the integration of the four distinct wireless system building blocks—1) analog/mixed-signal (including certain digital functions), 2) transceiver, 3) power amplifier, and 4) power management. (Including EDA tools in this section is beyond its scope. The Design chapter discusses EDA tools.) Nonetheless, some of the RF technical requirements for EDA tools are the need to be able to simulate not only the individual functions but also the interaction between the several circuits comprising the four wireless system building blocks. In addition, the need for fast and accurate 3D electromagnetic and RF simulation is growing due to the increased use of multi-layer module boards. This is especially true with the increased demand for the reduction of the time-to-market for new products.

ANALOG AND MIXED-SIGNAL

Mixed-signal ICs contain analog circuitry as well as the digital circuitry. Analog refers to "pure" analog circuits such as operational amplifiers, but mixed-signal chips often utilize functions such as analog-to-digital and digital-to-analog converters and digital signal processors. The focus of "purely" analog circuitry is shifting to higher and higher frequencies due to the increasing performance of post-analog digital signal processing. However, analog-to-digital and digital-to-analog conversion performance becomes increasingly important as it opens the door to new high-volume but low-cost applications (see Systems Drivers chapter, AMS-section). The commodity driver applications for mixed-signal ICs are projected to remain in consumer and communication markets where the off-chip interfaces require analog signals.

Certain analog IC technologies such as high voltage and power ICs are not specifically included, while others, such as microelectromechanical systems (MEMS), are included in the later, long-term years. Such devices and analog transistors must reuse and leverage the mainstream, digital CMOS technology to remain low cost and meet the demands for high-performance and reliability.

The scope of this sub-section includes: 1) analog speed devices (although the speed is mainly driven by RF there are certain analog-specific needs for both high speed bipolar and CMOS); 2) analog precision MOS device scaling but with relatively high voltages to achieve high signal to noise ratios and low signal distortion, 3) capacitors, and resistors; all devices are optimized for precision, matching performance, 1/f noise, low non-linearity, and low temperature gradients.

RF TRANSCEIVERS

Wireless RF transceivers are proliferating the marketplace and have become important technology drivers of advanced, high volume, semiconductor process technology. This section includes the technology metrics driven by the requirements of wireless RF transceivers. Technologies treated in this section include CMOS and Si or SiGe BiCMOS, as these are the dominant process technologies used for RF transceivers today and will remain to be in the foreseeable future.

Applications are focused on low noise amplifiers (LNAs), frequency synthesis and logic, voltage controlled oscillators (VCO), driver amplifiers, and filters. It is also important to consider improving isolation and functionality of circuits by going to higher integration levels. Devices include NPN (n-type emitter, p-type base, and n-type collector) bipolar transistors, RF-MOS (NMOS) field effect transistors, inductors, varactors, RF capacitors, and resistors. The primary metrics for performance are maximum frequency at unity current gain (max F_t), maximum frequency at unity power gain (F_{max}), noise figure, and trade-offs among power, noise, and linearity.

This section assumes that the frequency of RF transceivers is in the 800 MHz to 10 GHz range. This range covers both local and wide area standards such as global standard for mobile (GSM), code division multiple access (CDMA), wideband CDMA (WCDMA), 802.11 protocol for local area networks, and ultra wideband (UWB). "RF transceiver" will refer to the semiconductor content starting from the low noise amplifier (LNA) or power amplifier (PA) at the antenna end (including the LNA but not including the PA that is covered by the PA section) to the digital-to-analog converter/analog-to-digital converter (DAC/ADC) at the baseband end (not including the DAC or ADC that are covered by the mixed-signal section).

POWER AMPLIFIERS AND POWER MANAGEMENT

High voltage devices for use in base station power amplifiers, such as Si LDMOS, GaAs FET, GaAs PHEMT, SiC FET and GaN FET, are described in this sub-section. Also, PAs for terminals that require relatively high breakdown voltage devices [HBTs, PHEMTs, MOSFETs, and bipolars] are included herein. The key driving forces are integration of components and cost.

MILLIMETER WAVE

Today, compound semiconductors dominate the 10–100 GHz range. The device types most commonly used for analog mm-wave applications are HEMT, PHEMT, and MHEMT while MESFET and HBT predominate for mixed-signal and high speed applications. Except for MESFET and SiGe HBT, all device types employ epitaxial layer stacks that are composed of ternary or quaternary compounds derived from column III and V of the periodic chart. Because device properties are critically dependent on the selection of materials, thickness, and doping in the stack, which are proprietary to the manufacturer, there is great diversity in the nature and performance of these devices. Trade-offs among power, efficiency, breakdown, noise figure, linearity, and other performance parameters abound. One consequence of these trade-offs is that the "lithography node" is not the primary driver for mm-wave performance, although lithography dimensions are certainly shrinking with the drive to high frequency figures of merit (e.g., maximum F_t and F_{max}). Performance trends are more driven by a combination of desirable trade-offs and "bandgap engineering" of the epitaxial layer stack in concert with shrinking lithography. Thus, for the mm-wave tables in this section the focus is on the major performance metrics for near-term emerging markets—noise figure, power, efficiency, breakdown and, to a lesser extent, lithography dimensions. Because III-V technologies are rapidly changing, the long-term projections for tables on III-Vs in the 2003 ITRS are not included. Amongst the four sub-sections, this sub-section has the greatest diversity in combinations of materials, device types, applications, and performance.

DIFFICULT CHALLENGES

ANALOG AND MIXED-SIGNAL

Signal isolation, especially between the digital and analog regions of the chip, is a particular issue for scaled technologies. The difficulty and cost of integrating analog and high-performance digital functions on a chip are expected to increase with scaling. In particular, it will become a major issue to maintain analog performance parameters like mismatch and 1/f-noise together with new high-κ gate dielectrics. Finally, the transition to analog supply voltage of less than 1.8V will pose severe challenges to circuit design (see Systems Driver chapter).

Problems with integration of analog functions in digital CMOS are expected to increase depending on new materials or device structures added to the digital CMOS process. These problems include SOI and double-gate devices as well as changes in material choices for passive devices. Finally, the transition to analog supply voltage of less than 1.0V will pose even more challenges to circuit design than 1.8V (see Systems Driver chapter).

RF TRANSCEIVERS

The most difficult near-term challenges to achieving the RF transceiver roadmap include the following: aggressive scaling of passive elements (capacitors and inductors); reducing the cost of BiCMOS technology while improving power and performance trade-offs, and improving the performance of RF-CMOS devices to realize LNAs and drivers with performance comparable to that achievable with bipolar devices today, despite the barriers imposed by power supply scaling and reduced breakdowns. And finally, signal isolation must improve as more functions are integrated on a single chip.

Other near-term challenges for BiCMOS technology include the increased difficulty with integrating bipolar devices in aggressively scaled CMOS nodes due to conflicting thermal budget requirements. Other short-term challenges for RF-CMOS technology include sustaining acceptable 1/f noise and other analog performance metrics with the introduction of high-κ gate dielectrics and other materials and techniques driven initially by digital requirements.

The most difficult long-term challenges to achieving the RF transceiver roadmap include improving the performance (F_t and F_{max}) of active devices to levels that enable fundamental architectural simplification of the RF transceiver such as the direct synthesis and/or direct analog-to-digital conversion of the RF signal.

Other long-term challenges for BiCMOS technology include enabling the scaling of bipolar power supply to reduce power consumption versus CMOS technology. Other long-term challenges for RF-CMOS technology include the ability of aggressively scaled CMOS to meet the sensitivity and power delivery requirements of RF Transceivers despite the reduced voltage handling capability. Long-term challenges for passive elements will include the need to integrate new materials in a cost-effective manner to realize the high quality factor (Q) inductors and the high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap.

POWER AMPLIFIERS AND POWER MANAGEMENT

In 2003, the bulk of the consumer market for power amplifier technologies continues to be radio frequency integrated circuits (RFICs) and modules for cellular subscriber handsets, with handset volumes yearly sales exceeding 400 million units. Wireless LAN applications have quickly started to become another significant driver of integrated PA modules, with volumes expected to exceed tens of millions of units in 2003. These applications, which typically have very strict performance specifications, are extremely sensitive to price/performance trade-offs. This trade-off continuously drives the industry towards highly integrated low-cost system solutions. The market for power amplifiers is increasingly migrating away from packaged single die with RFICs to multi-band multi-mode integrated modules that deliver a complete amplifier solution and contain several different components. This preferred strategy requires a much-reduced RF component count at the handset assembly level. This preference is in line with the increase in outsourcing by the handset manufacturers to third party assembly houses. These RF modules typically integrate all or most of the matching and bypassing networks, and may also provide power detection, power management, filtering and RF switches for both transmit/receive and band selection.

As a logical extension of the integrated PA module, there is increased activity in the integration into the module of all other radio functions, such as transceivers, frequency synthesis, and filters and digital sections. This highly integrated solution would provide a true single radio module solution in a small footprint with a digital interface to the handset's digital signal processor/central processing unit (DSP/CPU) and handling essentially all post-baseband RF issues for a given application. There is little doubt that such system-in-package (SIP) single radios will eventually become commonplace in the industry. The challenges for the semiconductor technology community will likely be how to meet the cost and performance targets, with as much integration as possible available in the semiconductor technologies.

The signal isolation specifications necessary for the system integration of cellular chipsets represents a very significant challenge to both technologists and EDA tool providers. With the exceedingly high RF voltage created by the power amplifier and the power management circuits (in addition to the numerous frequencies generated internally by the intermediate frequency (IF) blocks signal isolation may become the most difficult obstacle preventing full system-on-chip implementation.

MILLIMETER WAVE

Compound semiconductor technologies have a number of similarities with silicon technologies and yet in many ways are distinctly different. While III-Vs have benefited from the advances in manufacturing equipment and chemistries, the development of these tools and chemicals is focused on the silicon industry and is not necessarily optimum for compound semiconductor processing. For example, the mass density of GaAs is about 2× that of Si, and because GaAs is more fragile, wafers are generally processed at 0.025-inch thickness (about 50% thicker than Si wafers) and result in a significant weight factor for automated wafer handling equipment and spinners. Additionally, the need to thin wafers to 0.002-inch thickness for thermal dissipation makes wafer breakage a yield issue that must be addressed.

Six-inch diameter semi-insulating GaAs wafers are routinely available and are becoming the *de facto* standard, although some foundries are still at four-inch. The move to six-inch and eight-inch substrates will be driven not only by economies of scale and chip cost but also by equipment availability. GaAs tends to be two generations behind Si in wafer size, with InP a further generation behind. It is crucial that substrate size keep up with Si advances if the III-V industry is to benefit from the advances in processing equipment. This continued pace in substrate size is particularly true for InP and SiC, the latter of which still suffers from a significantly high defect density. Today there is no production source of GaN substrates. Most GaN device epitaxy is done on SiC substrates. Significant technology breakthroughs will be required before GaN becomes commercially viable. Unresolved issues remain regarding SiC versus GaN substrates for GaN HEMTS. Advances in high resistivity Si substrates must also be addressed as SiGe HBT and RF CMOS push toward the mm-wave spectrum.

Device challenges, some of which are unique to III-Vs include the following: 1) the requirement for substrate vias for low inductance grounds in microstrip mm-wave circuits, 2) techniques for heat removal including wafer thinning and for low parasitic air-bridge interconnects, 3) high breakdown voltages for power devices, and 4) non-native oxide passivation. While these issues have been mostly solved for GaAs, they need to be successfully applied to the emerging III-V technologies of InP, SiC, and GaN. One of the critical challenges for high power III-V devices is thermal dissipation. This challenge is especially true for high-power density devices such as GaN.

TECHNOLOGY REQUIREMENTS

ANALOG AND MIXED-SIGNAL DEVICES

The previously identified trends of higher integration levels for logic with mixed-signal circuitry have continued and materialized into new application areas such as:

1. The steadily increasing digital processing capabilities enable more signal treatments to be done in the digital domain.
2. The use of I/O-transistor gate oxide, to accommodate higher voltages, continues to support interfaces to the outside world simultaneously with the high signal-to-noise requirements for mixed-signal, although this is accomplished at the cost of matching and 1/f noise scaling performance (see AMS section of System Drivers chapter for more details).

Moreover, the acceleration of the CMOS roadmap in the past years has hastened the integration possibilities of analog in logic processes. Continued focus on 1/f noise, passive component density and device matching is imperative to satisfy the increasing demands on power and area efficiency. Emerging issues from this increased integration level are with analog device modeling and protection against electrostatic discharge.

Performance and cost considerations will continue to drive modularity of process features in order to adapt the technology to specific SOC architectures. However, the more stringent mixed-signal transistor requirements may force the addition of process complexity to achieve integration goals. CMOS technology is gaining importance in the field of mixed-signal at the cost of bipolar and Si or SiGe-based BiCMOS processes, which will continue to be strong in the high-performance application areas that require high-speed and/or low noise, especially at low power. This strength in high performance occurs because the bipolar devices are carefully optimized and have intrinsic but non-scaling advantages in gain, noise, and matching. In contrast, the CMOS analog devices have extremely good frequency behavior combined with improved lower performance on the other parameters. This continued parallelism of technologies has been expressed in the mixed-signal table by having separate CMOS and bipolar device parameter requirements sections, making performance comparison possible. Refer to Tables 53a and 53b.

Table 53a Analog and Mixed-signal Devices Technology Requirements—Near-term

[1]	Year of Production		2003	2004	2005	2006	2007	2008	2009
	Technology Node			hp90			hp65		
	DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
[2]	Minimum Supply Voltage	Digital design (V)	1	1	0.95	0.9	0.85	0.8	0.75
[3]		Analog design (V)	3.3–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8
[4]	NMOS Analog Speed Device	T_{ox} (nm)	1.2–1.8	1.1–1.6	1.1–1.6	1.1–1.6	0.7–1.2	0.7–1.2	0.7–1.2
[5]		g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100	100
[6]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	300	200	200	200	150	150	150
[7]		σV_{th} matching ($mV \cdot \mu m$)	5	4	4	4	3	3	3
[8]	NMOS Analog Precision Device	T_{ox} (nm)	6.5–3	6.5–3	6.5–3	6.5–3	5–3	5–3	5–3
[9]		Analog V_{th} (V)	0.5–0.3	0.5–0.2	0.4–0.2	0.4–0.2	0.4–0.2	0.3–0.2	0.3–0.2
[10]		g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	300	300	300	300	300	300	300
[11]		1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	500	300	300	300	200	200	200
[12]		σV_{th} matching ($mV \cdot \mu m$)	15	12	12	12	9	9	9
[13]	Analog Capacitor	Density ($fF/\mu m^2$)	2	3	3	3	4	4	4
[14]		Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100	<100
[15]		Leakage ($fA / [pF \cdot V]$)	7	7	7	7	7	7	7
[16]		σMatching ($\% \cdot \mu m$)	1	0.7	0.7	0.7	0.5	0.5	0.5
[17]	Analog Resistor	Parasitic capacitance ($fF/\mu m^2$)	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02
[18]		Temp. linearity ($ppm/^oC$)	50–80	40–80	40–80	40–80	30–60	30–60	30–60
[19]		1/f-current-noise per current² ($1/[\mu m^2/Hz]$)	10^{-18}	10^{-18}	10^{-18}	10^{-18}	10^{-18}	6×10^{-19}	6×10^{-19}
[20]		σMatching ($\% \cdot \mu m$)	3	2.5	2.5	2.5	2	2	2
[21]	Bipolar Analog Device	g_m/g_{ce} at $W_{e\text{-}min}$ *	1200	1150	1150	1150	1100	1100	1100
[22]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	5	3	3	3	2	2	2
[23]		σcurrent matching ($\% \cdot \mu m^2$)	20	20	20	20	20	20	20

**Unusual measure for the voltage gain of bipolar devices, see notes. Added for 1:1 comparison with g_m/g_{ds} of MOS transistors (item 5).*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

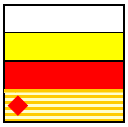

Table 53b Analog and Mixed-signal Devices Technology Requirements—Long-term

[1]	Year of Production		2010	2012	2013	2015	2016	2018
	Technology Node		hp45		hp32		hp22	
	DRAM ½ Pitch (nm)		45	35	32	25	22	18
[2]	Minimum Supply Voltage	Digital design (V)	0.7	0.7	0.65	0.65	0.6	0.6
[3]		Analog design (V)	1.8–1.2	1.8–1.2	1.8–1.0	1.8–1.0	1.5–1.0	1.5–1.0
[4]	NMOS Analog Speed Device	T_{ox} (nm)	0.5–0.8	0.5–0.8	0.4–0.6	0.4–0.6	0.4–0.5	0.4–0.5
[5]		g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100
[6]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	150	150	100	100	75	75
[7]		σV_{th} matching ($mV \cdot \mu m$)	2.5	2.5	2	2	1.5	1.5
[8]	NMOS Analog Precision Device	T_{ox} (nm)	3–2	3–2	3–1.3	3–1.3	2.5–1.3	2.0–1.3
[9]		Analog V_{th} (V)	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2
[10]		g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	300	300	300	300	300	300
[11]		1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	200	200	150	150	100	100
[12]		σV_{th} matching ($mV \cdot \mu m$)	7.5	7.5	6	6	5	5
[13]	Analog Capacitor	Density ($fF/\mu m^2$)	5	5	7	7	10	10
[14]		Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100
[15]		Leakage ($fA/[pF \cdot V]$)	7	7	7	7	7	7
[16]		σ Matching ($\% \cdot \mu m$)	0.4	0.4	0.3	0.3	0.2	0.2
[17]	Analog Resistor	Parasitic capacitance ($fF/\mu m^2$)	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02
[18]		Temp. linearity ($ppm/^oC$)	30–60	30–60	30	30	30	30
[19]		1/f-current-noise per current² ($1/[\mu m^2/Hz]$)	6×10^{-19}	3×10^{-19}	3×10^{-19}	3×10^{-19}	2×10^{-19}	2×10^{-19}
[20]		σ Matching ($\% \cdot \mu m$)	1.7	1.7	1.5	1.5	1.2	1.2
[21]	Bipolar Analog Device	g_m/g_{ce} at $W_{e\text{-}min}$ *	1050	1050	1000	1000	950	950
[22]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	1.5	1.5	1	1	0.7	0.7
[23]		σ current matching ($\% \cdot \mu m^2$)	20	20	20	20	20	20

**Unusual measure for the voltage gain of bipolar devices, see notes. Added for 1:1 comparison with G_m/G_{ds} of CMOS transistors (note 5).*

Manufacturable solutions exist, and are being optimized
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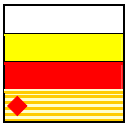


Notes for Tables 53a and 53b:

[1] Year of first digital product for a given technology generation as given in overall roadmap technology characteristics (ORTC) tables. Lithographic drivers for key technologies at each node are indicated. Year of first mixed-signal product at the same technology may lag by as much as one generation.

[2] Nominal supply voltage, V_{dd}, from low-operation power digital roadmap. Determines operating voltage of analog speed device. Lags the data of Table 48 "Low Operating Power Logic Requirements" by one year.

[3] Analog supply voltage is expected to lag digital by at least two or more generations. Additional voltage headroom is needed to avoid excessive power dissipation under reduced signal swing conditions. Analog CMOS designs may use thick gate oxide and low V_t techniques. The analog power supply reduction trend may lag digital backward compatibility trend for I/O such that a common thick gate oxide solution is not feasible. This line determines the operation voltage of analog precision n-channel field effect transistor (NFET) and of analog resistor and capacitor.

[4] SiO_2 equivalent physical CMOS gate dielectric thickness associated with the digital low-operational power (LOP) roadmap. Determines the color-coding in this NMOS RF device section, since its realization is crucial for obtaining the key parameters. The expected introduction of high-κ dielectrics will pose severe problems for analog performance.

[5] Measure for the amplification of a 5× minimum length low operating power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better G_{ds} amplification (at low frequencies). Operation point taken at 100 mV above the threshold voltage V_{th}. Can be compared to the bipolar equivalent in item [9].

[6] 1/f spectral density of digital NMOS device at a frequency of 1 Hz, critical for the minimum input signal in mixed-signal circuits (lower boundary for dynamic range) in low frequency circuits, mixers and VCOs. The 1/f noise is more prominent in MOS devices than in vertical (bipolar) or sub-surface devices (JFETs) due to carrier recombination in traps at the insulator-semiconductor interface (surface effect). Operation point at 100 mV above the threshold voltage V_{th}.

[7] Matching specification for the NMOS transistor's threshold voltage, assuming "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity, e.g. by using dummy structures, are required. Optimum situation obtained when scaling as gate oxide thickness: Avt = T_{ox} [nm] mV·µm, i.e., 5 mV·µm for T_{ox} = 5 nm. Statistical dopant fluctuations start limiting further improvement with SiO_2. Matching behavior of new high-κ gate dielectrics very insecure. Lower boundary for size of transistor in a mixed-signal circuit for a given accuracy and therefore often also for DC power consumption and speed. Also reliability related.

[8] SiO_2 equivalent physical CMOS gate dielectric thickness associated with the analog supply voltage roadmap in item [3]. Lags two generations or more behind digital, see item [14].

[9] Together with the analog supply voltage, item [3]; the threshold voltage V_{th} determines the maximum analog signal (upper dynamic range) the analog circuit is able to handle.

[10] Measure for the amplification of a 10× minimum length low operating power CMOS transistor. Using different lengths is an extra degree of freedom in mixed signal designs. Long devices have better Gds amplification (at low frequencies). Determines color-coding of this analog NMOS device section, reflecting the expected difficulty in obtaining the key parameters with devices optimized for lower supply voltages.

[11] See [8], values specified for thinnest oxide in [9].

[12] See [9], values specified for thinnest oxide in [9].

[13] Capacitors are mostly needed for weighting and comparing different analog signals. As digital content increases, chip size decreases, and capacitors occupy a larger percentage of the chip. Choice of implementation is driven by complexity/chip size trade-off (cost). MicroElectro-Mechanical Systems (MEMS) implementation for filter applications may be favorable at densities 7 fF/µm^2. Emerging integration on separate substrate in low-cost technology. Stacked (or trench) capacitors are not considered here since their increased corner areas pose new problems to leakage, mismatch and temperature behavior. For densities beyond 5fF/µm^2 high-κ dielectrics are assumed.

[14] The capacitors' second order voltage linearity is critical for the dynamic range of analog circuits. The first order component can be cancelled out by differential techniques.

[15] Leakage is driven by feedback capacitor applications, where a long time constant is required, and low frequency switched capacitor applications. Requirement is relaxed with increasing analog clock frequency. Highest quality dielectric is suggested.

[16] Lower boundary for size of capacitor for a given accuracy. Also reliability related.

[17] Parasitic capacitance per area of the analog resistor towards circuit ground for 1% mismatch between two neighboring resistors. Mainly determined by the capacitive coupling towards the substrate, and the square resistance that is important for the mismatch-behavior of the resistor. The range is determined by the choice of resistor realization (e.g., poly-Si, metal).

[18] Temperature coefficient (TC) is important for the analog resistor, e.g., in references. Low TC films or TC canceling techniques may be utilized.

[19] 1/f noise is critical for the minimum input signal in mixed-signal designs (lower boundary of dynamic range), such as low frequency circuits, mixers and VCOs. It is assumed that low 1/f solutions other than polysilicon coincide with high-Q RF-resistor solutions.

[20] Matching is important for the analog resistor (e.g., in references.) Careful layout and photolithographic uniformity, for example, using dummy structures, are required. Minimum dimensions assumed to be larger than minimum technology dimensions.

[21] Measure for the voltage gain of bipolar analog transistors with minimum emitter area: G_m ~ q.Ic/k.T and G_{ce} ~ V_{early} / Ic so in first order equal to the ratio of Early-over thermal-voltage, and not on the collector current specified in item [6]. Can be traded off against F_t/F_{max}. SiGe technology assumed for all nodes. To be compared with G_m/Gds at minimum gate length for CMOS, items [17] and [18], which are significantly less. Note, that these notes do not refer to a parasitic bipolar device often needed in analog CMOS.

[22] 1/f noise spectral density, at a frequency of 1 Hz, normalized to an active emitter area of 1 µm^2. The 1/f noise is less prominent in vertical (bipolar) or sub-surface devices (JFETs) than in baseline CMOS that has carrier recombination in traps at the insulator-semiconductor interface.

[23] Current matching specified for an active emitter area of 1 µm^2. Assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity, e.g. by using dummy structures, is imperative. In contrast to CMOS it does not scale with technology.

RF TRANSCEIVERS

Technology requirements today are driven by the need for lower power consumption, lower noise, and lower cost in RF transceivers. Refer to Tables 54a and 54b. In the near future, technology requirements will also be driven by the need to enable reconfiguring the RF transceiver in a software-defined radio. Further in the future, it is envisioned that the technology may be driven to enable direct digital synthesis architectures in RF transceivers. Additional technology requirements are to increase isolation and to enable multi-mode and multi-band capabilities.

Table 54a 0.8–10 GHz Transceiver Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Circuit Block—LNA							
NPN							
V_{cc} (V)	**2.5**	**2.5**	**1.8**	**1.8**	**1.5**	**1.5**	**1.5**
Emitter width (µm)	**0.2**	**0.18**	**0.15**	**0.15**	**0.13**	**0.12**	**0.1**
I_c (µA/µm) [1]	**75**	**59**	**43**	**37**	**28**	**22**	**16**
Peak F_t (GHz) [Vbc=1v]	**150**	**173**	**198**	**228**	**262**	**302**	**347**
Peak F_{max} (GHz) [2]	**180**	**203**	**239**	**256**	**295**	**330**	**387**
NF_{min} (dB)	**0.60**	**0.54**	**0.45**	**0.45**	**0.39**	**0.36**	**0.30**
NMOS							
V_{dd} (V)	**1.50**	**1.30**	**1.30**	**1.30**	**1.20**	**1.20**	**1.10**
I_{ds} (µA/µm) [3]	**26**	**23**	**21**	**16**	**12**	**10**	**9**
Peak F_t (GHz)	**110**	**120**	**140**	**170**	**200**	**240**	**280**
Peak F_{max} (GHz) [2]	**120**	**140**	**160**	**190**	**220**	**260**	**310**
NF_{min} (dB)	**0.8**	**0.7**	**0.6**	**0.6**	**0.5**	**0.4**	**0.4**
Circuit Block Synthesizer/Logic							
CMOS							
Gate length (nm) [4]	**80**	**75**	**65**	**53**	**45**	**37**	**32**
BiCMOS							
Gate length (nm)	**100**	**90**	**80**	**75**	**65**	**53**	**45**
Circuit Block—VCO							
Inductor							
Q (5 GHz) [5]	**15**	**16**	**17**	**19**	**20**	**22**	**24**
Varactor							
Tuning Range [6]	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Q (5 GHz)	**30**	**32**	**35**	**38**	**41**	**44**	**48**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

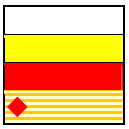


Table 54a 0.8–10 GHz Transceiver Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Circuit Block—Driver							
System Requirements							
Supply (V)	**3**	**3**	**3**	**3**	**2.4**	**2.4**	**2.4**
HV NPN							
BV_{CBO} (V)	**12**	**12**	**12**	**12**	**10**	**10**	**10**
Peak F_t (GHz) [Vbc=1V]	**35**	**40**	**46**	**53**	**61**	**70**	**81**
Peak F_{max} (GHz) [2]	**80**	**90**	**106**	**114**	**131**	**146**	**172**
HV MOS							
V_{ds} (V)	**3**	**3**	**3**	**3**	**2.4**	**2.4**	**2.4**
Peak F_t (GHz)	**30**	**30**	**40**	**40**	**50**	**50**	**60**
Peak F_{max} (GHz) [2]	**35**	**35**	**45**	**45**	**55**	**55**	**65**
Circuit. Block—Filters/Bypass							
Cap							
Density (fF/µm^2)	**5**	**7**	**9**	**12**	**15**	**19**	**23**
Q (5 GHz)	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**
Resistor							
$C_{parasitic}$ (fF) [7]	**70**	**63**	**57**	**51**	**46**	**41**	**37**
TCR (ppm/C)	**100**	**90**	**81**	**73**	**66**	**59**	**53**
Circuit. Block— Isolation							
S21 dB [8]	**60**	**70**	**80**	**90**	**100**	**110**	**120**

NF—noise figure TCR—temperature coefficient for resistance HV—high voltage

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

Table 54b 0.8–10 GHz Transceiver Technology Requirements—Long-term

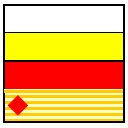
Year of Production	*2012*	*2015*	*2018*
DRAM ½ Pitch (nm)	*35*	*25*	*18*
Circuit Block—LNA			
NPN			
V_{cc} (V)	1.2	1.2	1.2
Emitter width (µm)	0.09	0.08	0.07
I_c (µA/µm) [1]	13	10	7
Peak F_t (GHz)	400	460	530
Peak F_{max} (GHz) [2]	438	498	572
NF_{min} (dB)	0.27	0.24	0.21
NMOS			
V_{dd} (V)	1.00	1.00	0.90
I_{ds} (µA/µm) [3]	7	4	1.5
Peak F_t (GHz)	400	700	1400
Peak F_{max} (GHz) [2]	450	750	1500
Nf_{min} (dB)	0.2	0.2	0.2
Circuit Block—Synthesizer/Logic			
CMOS			
Gate length (nm) [4]	22	16	11
BiCMOS			
Gate length (nm) [4]	22	16	11
Circuit Block—VCO			
Inductor			
Q (5 GHz)	26	28	30
Varactor			
Tuning range [6]	3.5	3.5	3.5
Q (5 GHz)	52	60	70

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

Table 54b 0.8–10 GHz Transceiver Technology Requirements—Long-term (continued)

Year of Production	*2012*	*2015*	*2018*
DRAM ½ Pitch (nm)	*35*	*25*	*18*
Circuit Block—Driver			
System Requirements			
Supply (V)	**2.4**	**2**	**2**
HV NPN			
BV_{CBO} (V)	**10**	**8**	**8**
Peak F_t (GHz) [Vbc=1V]	**93**	**107**	**123**
Peak F_{max} (GHz) [2]	**195**	**221**	**254**
HV NMOS			
BV_{DSS} (V)	**2.4**	**2.0**	**2.0**
Peak F_t (GHz)	**60**	**100**	**100**
Peak F_{max} (GHz) [2]	**65**	**120**	**120**
Circuit. Block—Filters/Bypass			
Cap			
Density (fF/μm^2)	**27**	**30**	**33**
Q (5 GHz)	**>50**	**>50**	**>50**
Resistor			
$C_{parasitic}$ (fF) [6]	**33**	**30**	**27**
TCR (ppm/C)	**48**	**43**	**29**
Circuit Block—Isolation			
S21 dB [7]	**130**	**140**	**150**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known



Notes for Tables 54a and 54b:

[1] I_c for F_t of 50 GHz for a minimum W_e and unit (1μm) L_e. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[2] Peak F_{max} (measured from unilateral gain extrapolated from 40 GHz with a 20 dB/dec slope).

[3] I_{ds} for F_t of 50 GHz for a minimum L and unit (1μm) W. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[4] RF CMOS technology nodes lag low standby power (LSTP) roadmap nodes by one year.

[5] Q at 5 GHz for a 1nH, 30,000 μm^2 inductor.

[6] Defined as C_{max}/C_{min}.

[7] Parasitic capacitance to substrate for a resistor of 1000 Ohms achieving 1% 3-sigma mismatch.

[8] Required to achieve direct modulation of the PA in short term (2–5 GHz). Required to achieve Tx/Rx integration in WCDMA (2 GHz).

POWER AMPLIFIERS AND POWER MANAGEMENT

POWER AMPLIFIERS

Transmitted power levels of the order of tens of milliwatts to a few Watts, (depending on the specific system) require efficient and linear RF power amplifiers. Because of the large signal nature of these amplifiers, these power devices require significant ruggedness and higher breakdown voltages than available in the standard CMOS submicron technologies. In addition, since these are typically in battery-operated devices, a low knee voltage must also be maintained. Today, these power amplifiers are typically built as stand-alone amplifiers with either GaAs HBT, silicon LDMOS or GaAs PHEMT FET technologies. The integration of the RF power function into the silicon SOC solution requires significant device optimization and development efforts, not just aimed at realizing the required RF functionality, but also with the required isolation necessary for effective system integration. Refer to Tables 55a and 55b.

POWER MANAGEMENT

Power management ICs are required for all but the simplest of wireless applications. This function conditions the power demands of the RF power amplifier and other wireless circuit blocks, regulating battery/charger surges; detecting power levels; and providing the appropriate temperature/ruggedness/leakage control for efficient system operation. This power management function is typically accomplished with high voltage CMOS technologies, typically requiring very large periphery pass FET devices. It is expected that the power management function will also be integrated as part of the SOC technology instead of a separate IC within a module. Tables 55a and 55b include the requirements for power management.

Table 55a Power Amplifier Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Nominal PA Supply Voltage (V)	**3**	**3**			**2.4**		
PA Product Solutions	**Integrated Module**		**Single Radio SIP [1]**			**Radio/ Baseband SIP [2]**	
PA Frequency (GHz)	**0.8–2.5**	**0.8–6**			**0.8–10**		
III-V HBT Transistor							
F_{max} (at V_{cc}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**
BV_{CBO} (V)	**25**	**25**	**25**	**25**	**18**	**18**	**18**
Linear efficiency (%) [3]	**52**	**52**	**52**	**52**	**55**	**55**	**55**
Area (mm^2) [4]	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**	**2**
Cost/mm^2 (US$) [5]	**0.4**	**0.4**	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**
III-V HBT Integration							
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Filter [8]	**N/A**	**N/A**	**N/A**	**Yes**	**Yes**	**Yes**	**Yes**
III-V PHEMT Transistor							
F_{max} (at V_{dd}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**
BV_{DGO} (V)	**20**	**20**	**20**	**20**	**16**	**16**	**16**
Linear Efficiency (%) [3]	**55**	**55**	**55**	**55**	**58**	**58**	**58**
PA Area (mm^2) [4]	**4**	**4**	**4**	**3.5**	**3.5**	**3.5**	**3.5**
Cost/mm^2 (US$) [5]	**0.4**	**0.4**	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

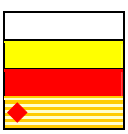


Table 55a Power Amplifier Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
III-V PHEMT Integration							
Power management [6]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Switch [7]	N/A	N/A	Yes	Yes	Yes	Yes	Yes
Filter [8]	N/A	N/A	N/A	Yes	Yes	Yes	Yes
III-V Passives							
Inductors Q [9]	15	15	15	25	25	25	25
Capacitor Q [10]	>100	>100	>100	>100	>100	>100	>100
Bypass capacitor density ($fF/\mu m^2$) [12]	0.6	0.6	0.6	2	2	2	2
RF capacitor density ($fF/\mu m^2$) [13]	0.6	0.6	0.6	2	2	2	2
Silicon MOSFET Transistor							
T_{ox} (PA) (Å) [11]	60	60	60	45	45	45	35
F_{max} (at V_{dd})	45	45	45	60	60	60	75
BV_{DSS} (V)	12	12	12	10	10	10	8
Linear efficiency (%) [3]	45	45	45	50	50	50	52
PA Area (mm^2) [4]	6	6	6	4.5	4.5	4.5	3
Cost/mm^2 (US$) [5]	0.1	0.08	0.08	0.06	0.06	0.06	0.05
Silicon MOSFET Integration							
Power management [8]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch [9]	NO	NO	NO	MEMS	MEMS	MEMS	MEMS
Filter [10]	NO	NO	NO	MEMS	MEMS	MEMS	MEMS
SiGe HBT Transistor							
F_{max} (GHz)	45	60	60	80	80	80	80
BV_{CBO} (V)	18	18	18	16	16	12	12
Linear efficiency (%) [3]	50	50	50	55	55	55	55
PA Area (mm^2) [4]	2.5	2.2	2.2	2	2	1.7	1.7
Cost/mm^2 (US$) [5]	0.15	0.15	0.12	0.12	0.11	0.11	0.11
SiGe Integration							
Power management	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch	NO	NO	MEMS	MEMS	MEMS	MEMS	MEMS
Filter	NO	NO	MEMS	MEMS	MEMS	MEMS	MEMS
Silicon / SiGe Passives							
Inductors Q [9]	10	10	10	14	14	14	14
Capacitor Q [10]	>100	>100	>100	>100	>100	>100	>100
Bypass capacitor density ($fF/\mu m^2$) [12]	2	4	4	20	20	30	30
RF capacitor density ($fF/\mu m^2$) [13]	2	4	4	6	6	8	8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

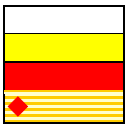


Table 55b Power Amplifier Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Nominal PA Supply Voltage (V)	**2.4**	**2.4**	**2.4**	**2**	**2**	**2**
PA Product Solutions	**Radio/Baseband SIP [2]**					
PA Frequency (GHz)	**0.8–10 GHz**					
III-V HBT Transistor						
F_{max} (at V_{cc}) (GHz)	**75**	**75**	**75**	**75**	**75**	**75**
BV_{CBO} (V)	**18**	**18**	**18**	**18**	**18**	**18**
Linear efficiency (%) [3]	**55**	**55**	**55**	**55**	**55**	**55**
Area (mm^2) [4]	**2**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**
Cost/mm^2 (US$) [5]	**0.24**	**0.22**	**0.2**	**0.15**	**0.15**	**0.15**
III-V HBT Integration						
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Filter [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
III-V PHEMT Transistor						
F_{max} (at V_{dd}) (GHz)	**75**	**75**	**75**	**75**	**75**	**75**
BV_{DGO} (V)	**16**	**16**	**16**	**16**	**16**	**16**
Linear efficiency (%) [3]	**58**	**58**	**58**	**58**	**58**	**58**
PA Area (mm^2) [4]	**3.5**	**3**	**3**	**3**	**3**	**3**
Cost/mm^2 (US$) [5]	**0.24**	**0.22**	**0.2**	**0.15**	**0.15**	**0.15**
III-V PHEMT Integration						
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Filter [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
III-V Passives						
Inductors Q [9]	**25**	**30**	**30**	**30**	**30**	**30**
Capacitor Q [10]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
Bypass capacitor density ($fF/\mu m^2$) [12]	**2**	**2**	**2**	**2**	**2**	**2**
RF capacitor density ($fF/\mu m^2$) [13]	**2**	**2**	**2**	**2**	**2**	**2**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

Table 55b Power Amplifier Technology Requirements—Long-term (continued)

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Silicon MOSFET Transistor						
T_{ox} (PA) (Å) [11]	35	35	35	35	35	35
F_{max} (at V_{dd})	75	75	75	35	35	35
BV_{DSS} (V)	8	8	8	2	2	2
Linear efficiency (%) [3]	52	52	52			
PA Area (mm^2) [4]	3	3	3	1.5	1.5	1.5
Cost/mm^2 (US$) [5]	0.05	0.05	0.05			
Silicon MOSFET Integration						
Power management [8]	Yes	Yes	Yes	Yes	Yes	Yes
Switch [9])	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Filter [10]	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
SiGe HBT Transistor						
F_{max} (GHz)	80	80	80	TBD	TBD	TBD
BV_{CBO} (V)	12	12	10	10	10	10
Linear efficiency (%) [3]	55	55	55	TBD	TBD	TBD
PA Area (mm^2) [4]	1.7	1.5	1.5	TBD	TBD	TBD
Cost/mm^2 (US$) [5]	0.11	0.1	0.1	TBD	TBD	TBD
SiGe Integration						
Power management	Yes	Yes	Yes	Yes	Yes	Yes
Switch	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Filter	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
Silicon / SiGe Passives						
Inductors Q [9]	14	18	18	18	18	18
Capacitor Q [10]	>100	>100	>100	>100	>100	>100
Bypass capacitor density ($fF/\mu m^2$) [12]	30	40	40	40	40	40
RF capacitor density ($fF/\mu m^2$) [13]	8	10	15	20	20	20

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

Notes for Tables 55a and 55b:

[1] Single radio SIP—system-in-package implementation of a complete post-baseband radio design, including power management, transceiver, power amplifier, filters, and switch functions.

[2] Radio/baseband SIP—system-in-package implementation of a complete baseband and radio design, including [1].

[3] Linear efficiency—power added efficiency of the final PA stage under personal communication service (PCS) CDMA (IS-95) modulation.

[4] Area—total semiconductor area necessary for the implementation of the quad-band GSM/general packet radio service (GPRS)/ Enhanced Data rates for GSM Evolution (EDGE) PA function, including matching/filtering.

[5] Cost/mm^2—approximate commercial foundry cost of the area mentioned in [4].

[6] Power management—capability of the technology to provide RF power detection/DC power management for the PA.

[7] Switch—capability of the technology to integrate cost-effectively a transmit/receive switch into the PA active die.

[8] Filter—capability of the technology to integrate high-quality band selection filters needed for the assumed PA solution; currently performed with surface acoustic wave (SAW) filter technology.

[9] Inductor Q—quality factor of a 5nH inductor at 1 GHz achievable with the technology with a metallization suitable for handling the power requirements of the PA.

[10] Capacitor Q—quality factor of a 10pF capacitor at 1 GHz achievable with the technology. Capacitor breakdown voltage must be rated for appropriate power amplification function.

[11] T_{ox} (PA)—thickness of the MOSFET transistor in the RF power amplifier function.

[12] Bypass capacitor density—bypass capacitor connected between V_{dd} (or V_{cc}) and ground. Capacitor breakdown voltage must be rated for appropriate power amplification function.

[13] RF capacitor density—capacitor used for all other functions (matching, harmonic filtering, coupling, etc). Capacitor must have adequate breakdown for the given application.

The major trends given in the near-term and long-term base station technology Tables 56a and 56b are as follows:

- The 2003 base station semiconductor market is primarily at 2 GHz and below. The future market is projected to expand to higher frequencies as new applications and frequency bands are allocated.
- Cost as measured by dollars per RF Watt is projected to steadily decrease from about $1/W today to less than $0.50/W by 2008.
- Application space is undergoing a conversion from ceramic to plastic packaging that will drive much of the cost reduction.
- In 2003, Si LDMOS FETs are the dominant semiconductor technology, easily commanding a 95% market share with GaAs FETs picking up the rest. SiC and GaN FETs are now appearing over the technology horizon.
- The trend for all semiconductor device technologies is to move to higher voltage that will increase power density and reduce device size for the same output power. The reduced device size requires less complex impedance matching networks and reduces power loss and increases power efficiency.
- Application space is moving from saturated power amplifiers to more linear power amplifiers to support the digital modulation formats of CDMA and WCDMA.
- For the same size devices the available linear power is about one-half the available saturated power.
- The PAE in linear operation is always less than in saturated operation.
- Maximum RF output power from a signal device will not increase above an approximate 240W unless there is a major change in the design of power amplifier systems.
- As frequencies increase, the challenge for LDMOS will be continuing to achieve low frequency (2 GHz) performance at higher frequencies. Failing to meet this challenge will result in other more expensive technologies.
- GaAs FET technology offers higher frequency performance, higher efficiency, and higher power density than LDMOS but at a higher cost.
- A major challenge for GaAs FETs is the move to a higher operating voltage that is closer to the operating voltage of LDMOS (28V).

- SiC technology is much less mature than LDMOS and GaAs but offers higher voltage operation and a higher power density.
- In 2003, the highest power SiC device is 10W, more than an order of magnitude below that available from LDMOS and GaAs. This technology uses a very expensive, high thermal conductivity SiC substrate.
- The long-term SiC technology will be supplanted by GaN technology and therefore has been removed from the long-term roadmap.
- GaN technology is immature, with first products expected by 2005 with the potential for higher power densities than LDMOS, GaAs, and SiC.
- GaN technology is being investigated using a host of substrate materials, such as SiC, sapphire, silicon, and GaN. Each of these materials offers advantages and disadvantages.
- The major challenge for GaN technology is achieving the very high level of device reliability that has been demonstrated using LDMOS and GaAs. High-heat dissipation packaging will need to be developed to take full advantage of the potential of GaN technology.

Table 56a Base Station Devices Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Application frequency (GHz)	**0.8–2**	**0.8–2.7**			**0.8–3.5**		
Cost ($$/Watt)	**1**	**0.9**	**0.8**	**0.7**	**0.6**	**0.5**	
Packaging (C-Ceramic, P-Plastic)	**C/P**	**C/P**	**C/P**	**Plastic**			
Si LDMOS							
Operating voltage (V)	**28**	**28**	**<40**	**<40**	**<50**	**<50**	**<50**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**0.7**	**0.7**	**0.9**	**0.9**	**1.2**	**1.2**	**1.2**
Saturated PAE (%)	**60**	**63**	**65**	**68**	**65**	**68**	**70**
Linear power (Watt)	**120**	**120**	**120**	**120**	**120**	**120**	**120**
Linear PAE (%)	**45**	**48**	**50**	**52**	**50**	**52**	**54**
GaAs FET							
Operating voltage (V)	**12**	**12**	**12**	**28**	**28**	**28**	**28**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**0.7**	**0.7**	**0.7**	**1**	**1.2**	**1.5**	**1.5**
Saturated PAE (%)	**65**	**65**	**68**	**70**	**68**	**70**	**72**
Linear power (Watt)	**90**	**90**	**90**	**90**	**90**	**90**	**90**
Linear PAE (%)	**50**	**50**	**52**	**55**	**57**	**55**	**57**
SiC FET							
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**10**	**30**	**60**	**60**	**60**	**60**	**60**
Saturated power density (W/mm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Saturated PAE (%)	**45**	**45**	**45**	**45**	**45**	**45**	**45**
GaN FET							
Operating voltage (V)	**-**	**-**	**28**	**28**	**48**	**48**	**48**
Saturated power (Watt)	**-**	**-**	**10**	**30**	**60**	**60**	**180**
Saturated power density (W/mm)	**-**	**-**	**2**	**2**	**4**	**4**	**4**
Saturated PAE (%)	**-**	**-**	**52**	**55**	**50**	**52**	**55**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

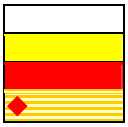
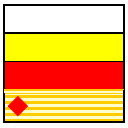


Table 56b Base Station Devices Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Application frequency (GHz)	**0.8–5**					
Cost ($$/Watt)	**0.4**		**0.3**			
Packaging (C–Ceramic, P–Plastic)	**Plastic**					
Si LDMOS						
Operating voltage (V)	**<50**	**<50**	**<50**	**<50**	**<50**	**<50**
Saturated power (Watt)	**240**	**240**	**240**	**240**	**240**	**240**
Saturated power density (W/mm)	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**
Saturated PAE (%)	**65**	**65**	**70**	**70**	**70**	**70**
Linear power (Watt)	**120**	**120**	**120**	**120**	**120**	**120**
Linear PAE (%)	**50**	**50**	**52**	**52**	**52**	**52**
GaAs FET						
Operating voltage (V)	**28**	**28**	**28**	**28**	**28**	**28**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**
Saturated PAE (%)	**68**	**68**	**70**	**70**	**72**	**72**
Linear power (Watt)	**90**	**90**	**90**	**90**	**90**	**90**
Linear PAE (%)	**52**	**52**	**55**	**55**	**57**	**57**
SiC FET						
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**60**	**60**	**60**	**60**	**60**	**60**
Saturated power density (W/mm)	**2**	**2**	**2**	**2**	**2**	**2**
Saturated PAE (%)	**45**	**45**	**45**	**45**	**45**	**45**
GaN FET						
Operating voltage (V)	**48**	**48**	**48**	**48**	**48**	**48**
Saturated power (Watt)	**180**	**180**	**180**	**180**	**180**	**180**
Saturated power density (W/mm)	**4**	**4**	**4**	**4**	**4**	**4**
Saturated PAE (%)	**50**	**50**	**52**	**52**	**55**	**55**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known



MILLIMETER WAVE

The millimeter wave technology requirements have been divided into two major device types—field effect and bipolar transistors. While the transport mechanisms and structure within each type are similar, there are vast differences in performance attributable to the selection of substrate material and design of the epitaxial layer stack. The major classes of millimeter wave transistors are listed in the following paragraphs.

Field effect transistors (FETs) are majority carrier devices in which electron transport is in a thin layer parallel to the wafer surface. The major types are as follows:

- MESFETs are composed of homogeneous layers in which electron transport occurs in an intentionally doped layer and are generally GaAs-based.
- HEMTs are composed of layers of different bandgap materials on a lattice-matched substrate. Carriers in HEMTs are provided by a highly doped layer and carrier transport occurs in an adjacent undoped layer, resulting in much higher mobility due to the lack of ionized charge scattering. HEMT are generally InP- and GaN-based.
- PHEMTs are composed of layers with different bandgap materials on a substrate in which the lattice constant of the layers are close, but not matched, to the lattice constant of the substrate. PHEMTs have higher mobility than HEMTs and are generally GaAs-based.
- MHEMTs are composed of layers of different bandgap materials on a substrate in which the lattice constants of the layers are mismatched to the substrate. The resulting strain is taken up by a specially designed buffer layer. MHEMTs offer the highest degree of flexibility in design and in mm-wave performance. Generally, they are made on GaAs substrates to take advantage of the more mature materials and processing technologies.

HBTs are minority carrier devices in which carrier transport is perpendicular to the wafer surface. The major types are as follows:

- InP HBTs are composed of ternary and quaternary layers in a number of III-V elements [In, Ga, As, Sb, P] that are closely lattice matched to InP substrates. GaAs HBTs are generally used below 10 GHz.
- SiGe HBTs are composed of a single crystal mixture of Si and Ge on a Si substrate.

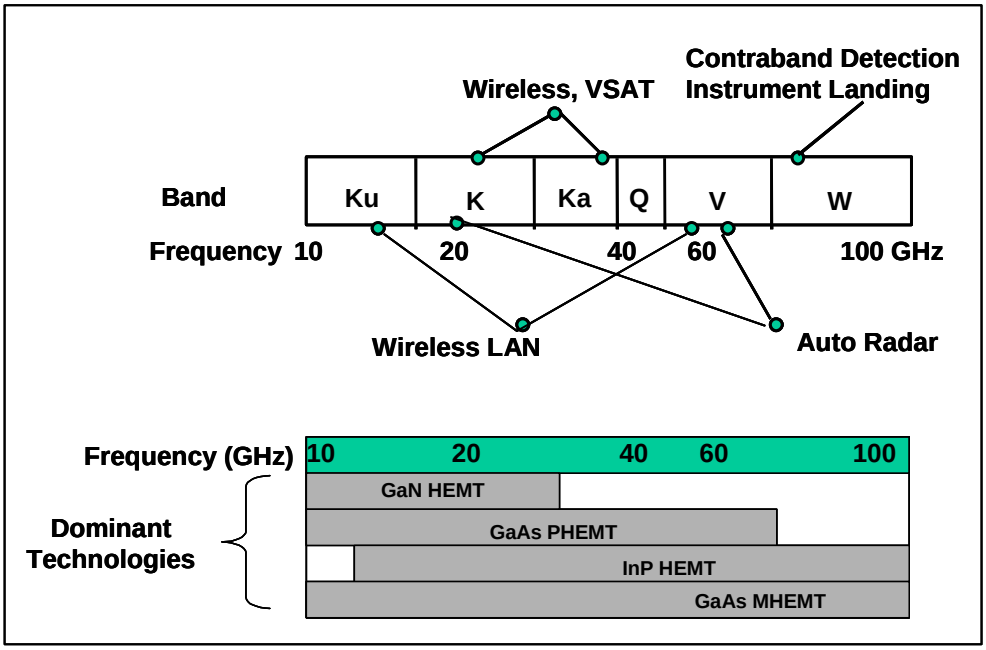


Figure 31 Millimeter Wave Commercial Applications Spanning 10 to 100 GHz

Figure 31 illustrates the potential high volume commercial markets for mm-wave devices. Following a major decline in the GaAs industry in 2001, the mm-wave market is likely to be led by automotive applications followed by wireless LAN opportunities. Figure 31 also shows the most likely scenario for deployment of device types over this frequency spectrum. Gallium nitride HEMTs have potential for supplanting all other III-Vs for power applications up to Ka band, but there exists substantial technical challenges yet to be resolved. While PHEMTs have been reported at 60 and even 94 GHz, it is likely that the higher mm-wave frequencies will be the domain of InP HEMTs and MHEMTs due to both higher performance and lower DC power requirements. PHEMTs will still have a play at the lower end of the spectrum due to a cost advantage, but they are likely to be supplanted by the end of the decade.

InP HBTs and SiGe are ideal for high-speed logic and mixed-signal applications. This application is due to the much better threshold control in bipolars, in which the threshold is a function of bandgap (a materials property) rather than the Schottky Barrier and Fermi Level (a processing property). HBTs are also the device of choice for low phase noise oscillators. MESFETs are likely to become obsolete for new applications in mid-decade as InP and SiGe cost and performance advantages overtake MESFETs. Although the gap between InP and SiGe is closing, InP will always have the advantage of higher breakdown, while SiGe BiCMOS holds the advantage for integration density.

Table 57 for millimeter wave is focused on low noise and power monolithic microwave integrated circuits (MMICs) for HEMTs and PHEMTs, and digital/mixed-signal for MESFETs and HBTs. While mixers, oscillators, varactors, switches, and phase shifters are as important, the technical challenges for all the devices can be embodied in the small signal (low noise) and large signal (power) functions. Other device types, as well as passives, should be included in future years.

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
GaAs MESFET (digital mixed-signal)							
Gate length—L physical (nm)	250	250	150	150	-	-	-
Minimum M1 pitch (nm)	1200	1200	680	680	-	-	-
F_t - enhancement mode (GHz)	80	80	120	120	-	-	-
F_t - depletion mode (GHz)	70	70	100	100	-	-	-
BV_{GD} (1mA/mm, V_g=0) (volts)	7.5	7.5	5 to 10	5 to 10	-	-	-
Power delay product at gate delay-FO=1 (fJ at pS)	2 at 25	2 at 25	1.2 at 18	1.2 at 18	-	-	-
Shortest DCFL gate delay (pS)	10	10	6	6	-	-	-
Interconnect metal layers	4	4	5	5	-	-	-
Interconnect metal	Al	Al	Al	Al	-	-	-
Inter line dielectric constant (effective)	4.2	4.2	3.1	3.1	-	-	-
GaAs PHEMT (low noise)							
Gate length (nm)	100	100	70	70	50	50	32
F_t (GHz)	130	130	150	150	170	170	200
Breakdown (volts)	7	7	7	7	6	6	5.5
I_{max} (mA/mm)	650	650	600	600	550	550	550
G_m (S/mm)	0.65	0.65	0.8	0.8	0.9	0.9	1
NF (dB) at 26 GHz, 18–20 dB associated gain	3.1	3.1	2.5	2.5	2	2	1.5
NF (dB) at 94 GHz, 8–10 dB associated gain	4.8	4.8	4	4	3.5	3.5	3
GaAs PHEMT (power)							
Gate length (nm)	200	200	100	100	70	70	-
F_{max} (GHz)	75	75	150	150	200	200	-
Breakdown (volts)	11	11	11	11	9	9	-
I_{max} (ma/mm)	650	650	750	750	850	850	-
G_m (S/mm)	0.52	0.52	0.67	0.67	0.85	0.85	-
P_{out} at 26 GHz and peak efficiency (mW/mm)	500	500	550	550	600	600	-
Peak efficiency at 26 GHz (%)	20	20	30	30	40	40	-
Gain at 26 GHz, at P_{1dB} (dB)***	10	10	12	12	14	14	-
P_{out} at 94 GHz and peak efficiency (mW/mm)	250	250	-	-	-	-	-
Peak efficiency at 94 GHz (%)	15	15	-	-	-	-	-
Gain at 94 GHz, at P_{1dB} (dB)***	6	6	-	-	-	-	-

DCFL—direct-coupled FET logic

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

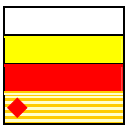


Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
InP HEMT (low noise)							
Gate length (nm)	-	100	70	70	50	50	32
F_t (GHz)	-	200	240	240	300	300	350
Breakdown (volts)	-	4	3.5	3.5	3	3	2.5
I_{max} (ma/mm)	-	700	700	700	650	650	600
G_m (S/mm)	-	1	1.2	1.2	1.5	1.5	1.8
NF (dB) at 26 GHz, 20–23 dB associated gain	-	2.2	1.8	1.8	1.5	1.5	1.2
NF (dB) at 94 GHz, 10–13 dB associated gain	-	3	2.5	2.5	2	2	1.8
InP HEMT (power)							
Gate length (nm)	-	-	150	100	100	100	100
F_{max} (GHz)	-	-	200	220	260	260	260
Breakdown (volts)	-	-	5	5	6	6	6
I_{max} (ma/mm)	-	-	750	700	650	650	650
G_m (S/mm)	-	-	0.8	0.9	0.9	0.9	0.9
P_{out} at 26 GHz and peak efficiency (mW/mm)	-	-	400	400	450	450	450
Peak efficiency at 26 GHz (%)	-	-	30	40	50	50	50
Gain at 26 GHz, at P_{1dB} (dB)***	-	-	12	15	15	16	16
P_{out} at 94 GHz and peak efficiency (mW/mm)	-	-	250	300	350	350	400
Peak efficiency at 94 GHz (%)	-	-	25	40	40	45	45
Gain at 94 GHz, at P_{1dB} (dB)***	-	-	6	8	10	10	12
GaAs MHEMT (low noise)							
Gate length (nm)	-	-	100	100	70	70	50
F_t (GHz)	-	-	250	250	300	300	400
Breakdown (volts)	-	-	5	5	4	4	3
I_{max} (ma/mm)	-	-	680	680	680	680	680
G_m (S/mm)	-	-	1	1	1	1	1
NF (dB) at 26 GHz, 10–23 dB associated gain	-	-	1.6	1.6	1.2	1.2	0.8
NF (dB) at 94 GHz, 10–13 dB associated gain	-	-	2.3	2.3	1.8	1.8	1.6

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

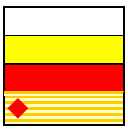


Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
GaAs MHEMT (Power)							
Gate length (nm)	-	-	-	200	100	100	100
F_{max} (GHz)	-	-	-	200	250	275	300
Breakdown (volts)	-	-	-	8	8	8	9
I_{max} (ma/mm)	-	-	-	600	600	600	600
G_m (S/mm)	-	-	-	0.8	0.9	0.9	0.9
P_{out} at 26 GHz and peak efficiency (mW/mm)	-	-	-	350	500	600	750
Peak efficiency at 26 GHz (%)	-	-	-	45	55	55	60
Gain at 26 GHz, at P_{1dB} (dB)***	-	-	-	12	15	16	16
P_{out} at 94 GHz and peak efficiency (mW/mm)	-	-	-	200	350	400	450
Peak efficiency at 94 GHz (%)	-	-	-	25	40	45	45
Gain at 94 GHz, at P_{1dB} (dB)***	-	-	-	6	8	10	12
GaN HEMT (low noise)							
Gate length (nm)	-	-	-	-	150	100	100
F_t (GHz)	-	-	-	-	100	100	120
Breakdown (volts)	-	-	-	-	>40	60	60
I_{max} (ma/mm)	-	-	-	-	>1000	1200	1500
G_m (S/mm)	-	-	-	-	>0.3	0.4	0.5
NF (dB) at 26 GHz, 14 dB gain	-	-	-	-	2	2	1.5
GaN HEMT (power)							
Gate length (nm)	-	-	-	-	150	100	100
F_{max} (GHz)	-	-	-	-	100	100	150
Breakdown (volts)	-	-	-	-	>40	60	60
I_{max} (ma/mm)	-	-	-	-	>1000	1200	1500
G_m (S/mm)	-	-	-	-	>0.3	0.4	0.5
P_{out} at 26 GHz and peak efficiency (mW/mm)	-	-	-	-	3000	5000	5000
Peak efficiency at 26 GHz (%)	-	-	-	-	35	40	50
Gain at 26 GHz, at P_{1dB} (dB)***	-	-	-	-	10	12	12

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—HBT **							
InP HBT							
Emitter width (nm)	1200	800	350	350	250	250	150
F_t (GHz)	170	170	300	300	300	300	400
F_{max} (GHz)	170	200	300	300	350	350	450
Breakdown (BV_{CEO}) (volts)	7	7	4	4	4	4	3
$I_{max}/\mu m^2$ (mA/μm^2)	1.5	2	5	4	4	4	5
Beta	20	50	50	50	50	50	50
3 sigma V_{BE} (mV)	50	40	40	30	30	25	25
Interconnect metal layers	3	4	4	4	5	5	5
Interconnect metal	Al, Au	Al, Au	Al, Au	Al, Au	Cu	Cu	Cu
Barrier	PVD	PVD	PVD	PVD	IMP	IMP	IMP
Wafer diameter (mm)	100	100	100	100	150	150	150
SiGe HBT							
Emitter Width (nm)	200	150	120	120	100	100	70
F_t (GHz)	150	175	200	230	265	300	350
F_{max} (GHz)	180	205	240	260	300	330	390
Breakdown (BV_{CBO}) (volts)	6	5.5	5.3	5	5	4.5	4.5
Breakdown (BV_{CEO}) (volts)	2.3	2	2	2	1.8	1.8	1.8
$I_{max}/\mu m^2$ (mA/μm^2)	7	8	10	14	14	18	18
Beta	140	200	200	200	250	250	300
Nf_{min} at 77 GHz (dB)	6.6	6.1	5.5	5.1	4.6	4.3	3.9

**Lithography dimensions are drawn dimensions.*
*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*
**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known
Interim solutions are known

The bubble charts of Figures 32, 33, and 34 portray the projected technology trends among the various device types over the near term. In Figure 32 the PHEMT bubble represents the noise figure versus frequency for devices commercially available today. While PHEMTs are the mainstay of low noise devices in the mm-wave spectrum at present, it is expected that they will quickly be supplanted by InP in the near term and eventually MHEMT by the end of the decade. This projection is exhibited by the InP/MHEMT bubble region that portrays the region in the noise figure/frequency realm of reported research results through 2003. Current R&D results project future commercial trends. Not only do InP HEMTs and MHEMTs exhibit lower noise figures, but also the required DC power dissipation is roughly 4× lower for equivalent NF and gain performance.

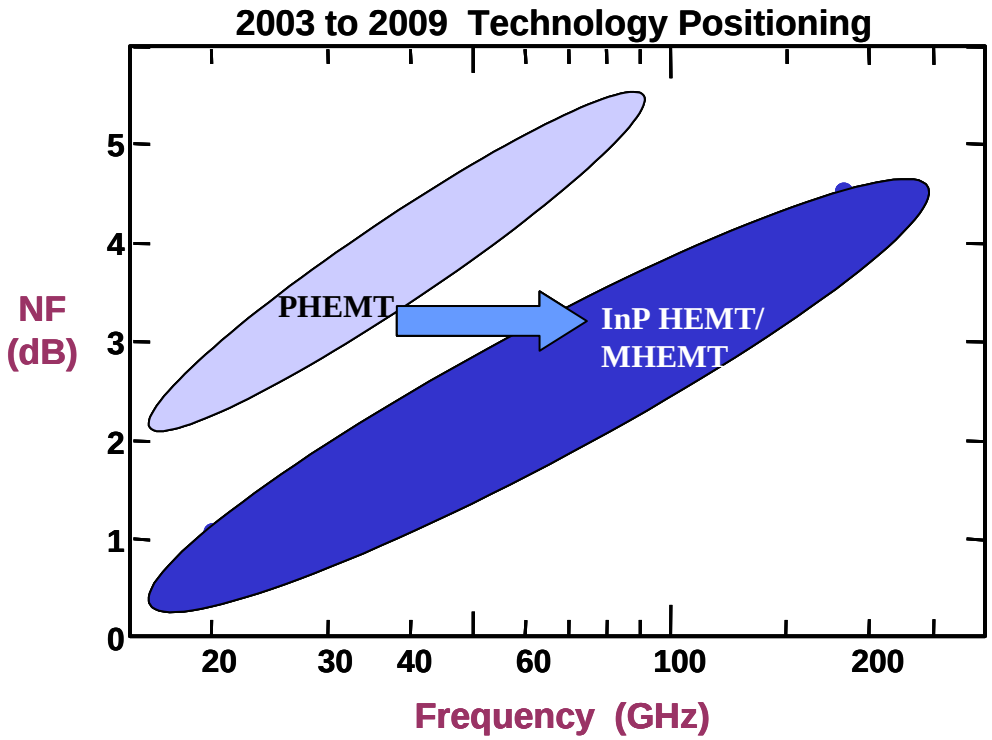


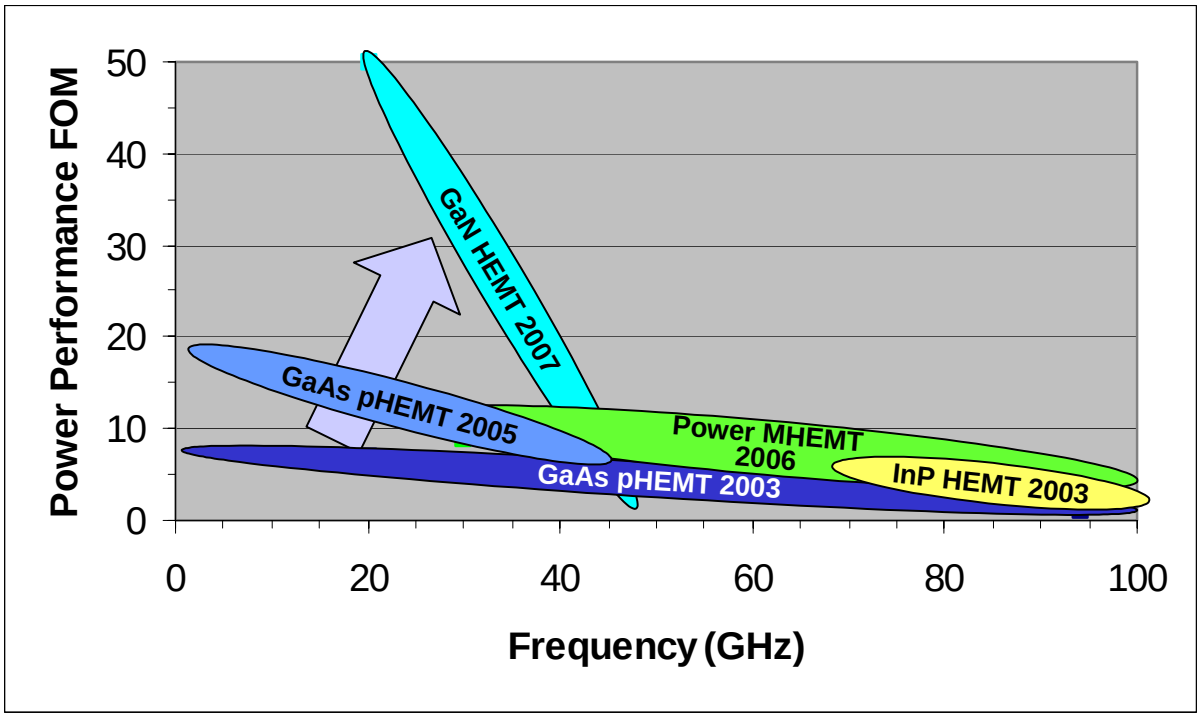
Figure 32 Low Noise Amplifiers

Figure 33 shows the evolution of millimeter wave power performance over time. The power performance figure of merit (FOM) is MMIC power density (W/mm) times MMIC small signal (SS) gain per stage (dB) at application center frequency for a typical 10–20% bandwidth. The power bandwidth product for the different device technologies could have also been used and would have provided a similar trend. GaAs PHEMT and InP HEMT are the premier millimeter wave power devices available today in production, with GaAs PHEMT the preferred technology for frequencies less than 77 GHz. However, present day GaAs PHEMT and InP HEMT do not have the power performance to meet future systems requirements. Continued evolution of GaAs PHEMTs and InP HEMTs will offer increased performance, but will still fall short of evolving demands.

In engineering a millimeter power device, the engineer is faced with a dilemma. Increased power (or power density) necessitates operating devices either at higher operating voltages or high current densities. For a given device technology, in addition to the trade-off between operating voltage and current density, increasing operating voltage comes at the expense of high frequency operation or gain. As an example, GaAs PHEMTs that can operate at higher voltages compared to InP HEMTs tend to be gain-limited in the upper millimeter frequency range. On the other hand, today's InP HEMTs that have superior high frequency gain are limited to low voltage (and subsequently low power) operation. The challenge for the device engineer is to develop a device structure that combines the best attributes of both GaAs PHEMTs (higher voltage operation) and InP HEMTs (high frequency gain).

One approach currently under development is MHEMT technology, which takes advantage of bandgap engineering to create a device structure that exhibits the best compromise between the relatively high voltage operation of GaAs PHEMTs and the high gain of InP HEMTs. As shown in Figure 33, power MHEMT technology is expected to eclipse both GaAs PHEMT and InP HEMT performance in the 40–100+GHz frequency range and will be available in production in the 2006+ timeframe.

Another promising approach is the wide bandgap semiconductor GaN. At microwave frequencies GaN HEMTs have exhibited 5–10 times the power density of GaAs PHEMT and GaN HEMTs have shown potential for operation through Ka-band. GaN HEMTs achieve this revolutionary power performance through a combination of high current density and significantly higher operating voltage with only modest reduction in gain compared to GaAs PHEMTs. With continued development within the next five years GaN HEMTs are projected to become the premier and preferred device technology for millimeter wave power applications through Ka band.



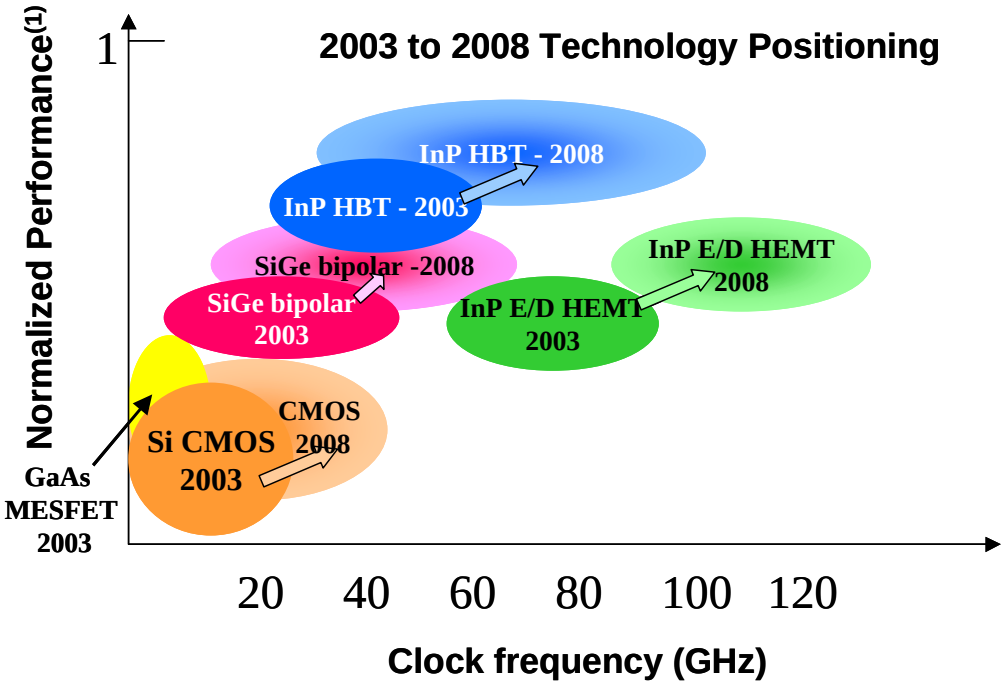
Performance figure of merit is MMIC power density (W/mm) times MMIC SS gain per stage (dB) at application center frequency (typical 10–20% bandwidth).

Figure 33 Evolution of Production Power Devices 2003–2009

Figure 34 shows the evolutions of mixed-signal technology for mm-wave applications. Such applications are driven by high center frequency, precise transistor matching, low noise operation, and high linearity in the under lying technology. With continuous scaling, CMOS technology is expected to address low-resolution circuits up to 10–20 GHz. SiGe bipolar extends the region of silicon performance to 40–50 GHz, but will likely be limited in dynamic range due to the breakdown voltage (BV_{CEO}) being less than 2V. InP heterojunction bipolar transistors (HBTs) are the ultimate performance technology once the core transistor technology is aggressively scaled. InP HBTs will be limited by substrate size that is typically at 100 mm, but with 150 mm being sampled. InP enhancement/depletion (E/D) HEMTs offer higher frequency operation than InP HBTs when scaled to sub 0.1 micron.

E/D technology is also lower power than the HBT alternative, but the threshold voltage control of the HEMT is not as good as the junction control turn-on of the HBT. The HEMT also does not have as good 1/f noise performance as the HBT. E/D technology should operate at lower power than a similar HBT circuit.

For applications where high dynamic range is required (e.g., collision avoidance radar) bipolar devices are often preferred due to their high linearity and low 1/f noise. The market force for advanced mixed-signal circuits will most likely drive increased wireless communications bandwidth through the real time correction and synthesis of analog signals using digital technologies. To do this, the associated digital and mixed-signal circuit must run three to ten times faster than the analog carrier frequency. Additional opportunities exist for performing the control and routing in optical networks.



The metric for performance depends on the class of circuit. It can include dynamic range, signal-to-noise, bandwidth, data rate, and/or inverse power.

Figure 34 Mixed-signal/Ultra High-speed Digital

POTENTIAL SOLUTIONS

ANALOG AND MIXED-SIGNAL DEVICES

In this sub-section, the potential solutions to the challenges in mixed-signal are discussed. The solutions here are different from, or in addition to, those already reviewed for memory and logic discussed in other sections of the PIDS chapter. Successful mixed-signal technologies will leverage the baseline digital platform while integrating value-added features and functions. Key ingredients to successful mixed-signal integration are the addition of special higher-voltage analog precision transistors, high quality passive elements, adequate signal isolation, and compatible active devices.

With the steady improvement in high-frequency performance and decrease in speed-power product of CMOS, this technology will gain on traditional BiCMOS and bipolar implementations. The introduction of SOI—though positive for signal isolation—will pose additional challenges for mixed-signal. However, analog device performance for SOI process is an area of research. Thermal and floating-body effects as well as high-resistive substrate connections pose challenges for circuit design.

The mixed-signal supply voltage continues to lag that of high-performance digital by two or more generations. A combination of multiple gate oxide thickness, multiple thresholds, and DC-DC conversion is needed to support the increased mixed-signal requirements. Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to extend the trend for lower supply voltages for mixed-signal applications. An alternative to full integration is the use of SIP that combines circuits on different technologies and is optimized for the desired functions. It is expected that full-digital implementations in CMOS will replace most analog functions except for A-to-D-conversion.

The trend of moving discrete passive elements from board level to chip level will continue. Solutions for achieving discrete-equivalent precision on-chip passive components are expected. Integrated resistors need low parasitic capacitance

and high temperature linearity. New high-κ dielectrics are needed to reduce integrated capacitor area. Alternatively, some passives may be integrated into the printed board or package as a method of cost reduction/simplification.

Matching requirements are driven by mixed-signal devices. Precise active and passive device matching will be achieved through careful layout and low thermal budget processes. Device matching is critical for high-precision analog circuit design using techniques like active circuit compensation.

As the integration density increases and the operation frequency rises, protection of noise sensitive analog circuits from "noisy" digital circuits will become increasingly difficult. Signal isolation is managed through a combination of substrate (e.g., high resistance), interconnect, and package solutions. Today, circuit blocks are protected by oxide isolation, guard rings, and buried wells (triple well). Integrated shielding structures may be required for protection of circuits and interconnects in the future. Novel design architectures may be employed to enhance circuit signal/noise performance. Any cost-effective solution addressing these problems and challenges must be compatible with the mainstream CMOS technology of the time. Figure 35 illustrates analog and mixed-signal potential solutions.

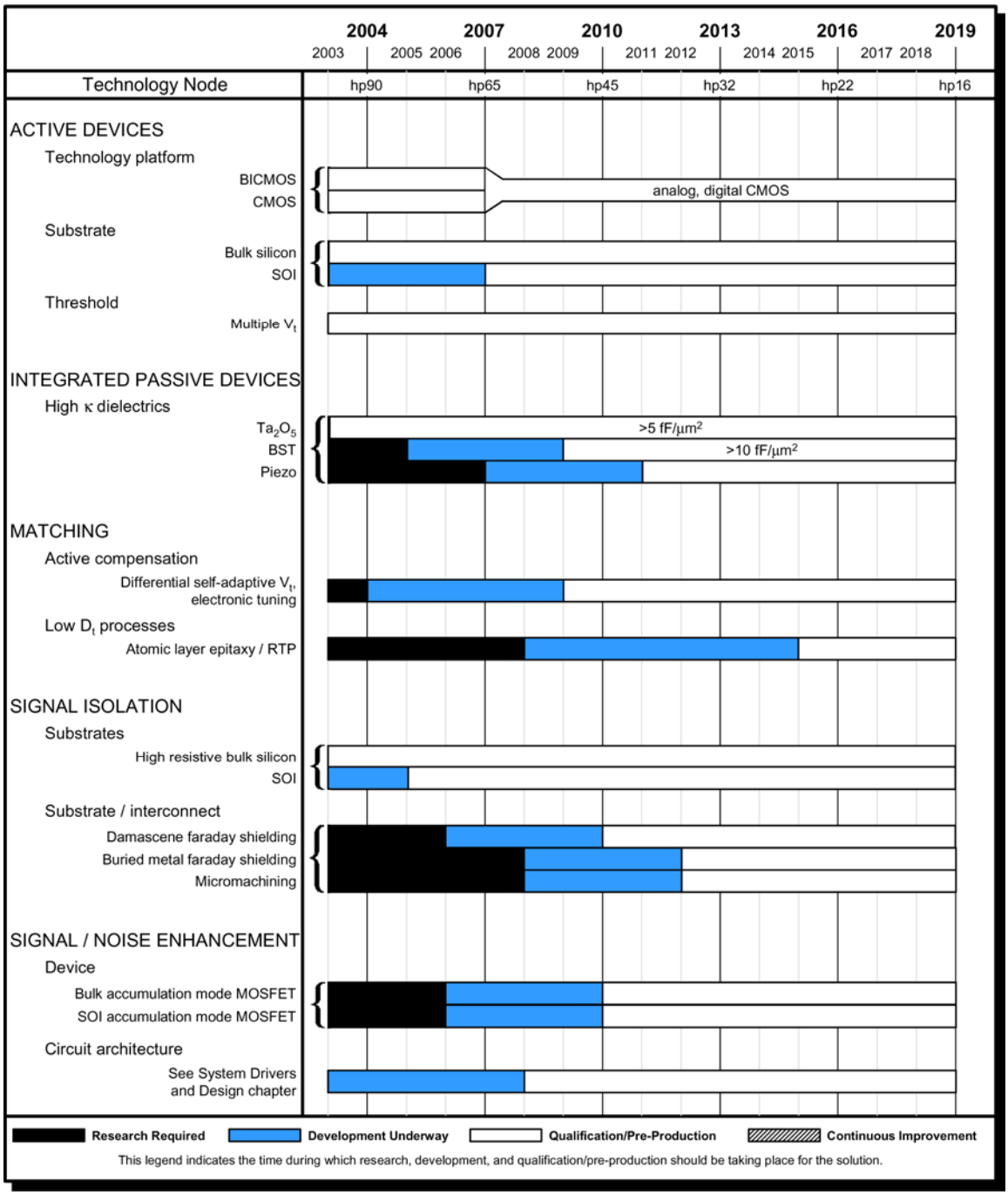


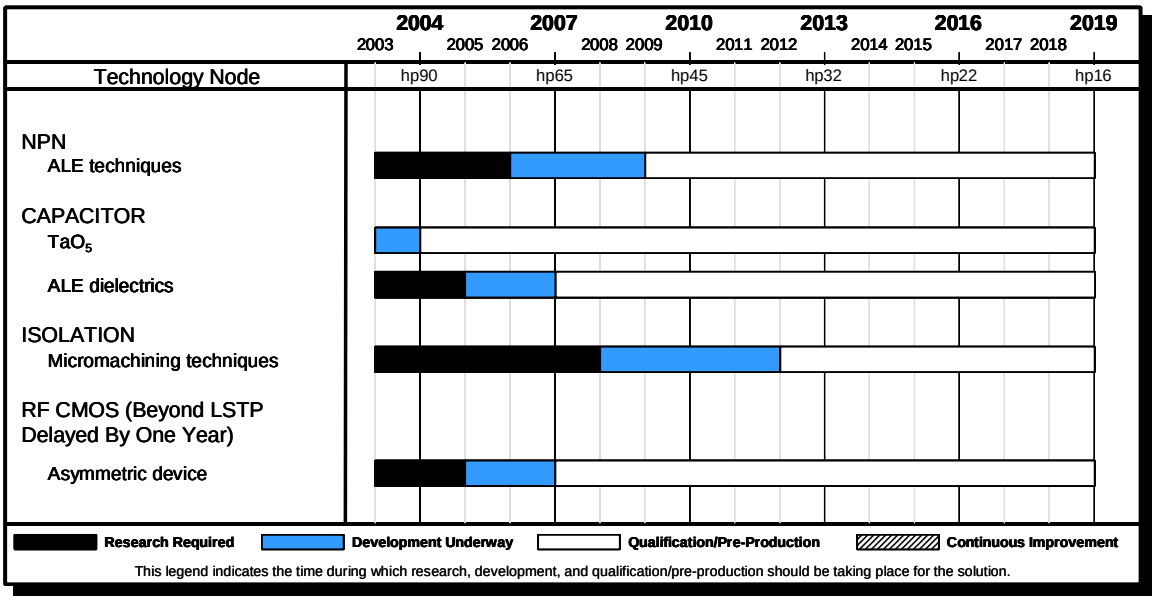
Figure 35 Analog and Mixed-signal Devices Potential Solutions

RF TRANSCEIVERS

Bipolar and RF NMOS performance show an aggressive roadmap for the F_t and F_{max} improvement of these active devices. This improvement will be accomplished up to an F_t of ~300 GHz for bipolar devices by techniques that continue to push both vertical and lateral scaling. Vertical scaling is likely to be accomplished with evolutionary improvement in current equipment and techniques and the addition of carbon doping. Beyond F_t of ~300 GHz, it is likely that more advanced epitaxial techniques will be required, such as atomic layer epitaxy. Beyond an F_t of ~400 GHz, it is likely that additional materials and dopants will need to be introduced. Lateral scaling will borrow heavily from techniques being adopted from digital CMOS and is not likely to add additional requirements to those already being applied to the scaling of digital CMOS.

CMOS devices will continue to benefit from progression along the digital roadmap. Challenges are similar to those already discussed in the mixed-signal section, but intensified because of the need to operate at higher frequencies. It is expected that the same potential solutions anticipated for the mixed-signal roadmap will be adopted for the RF transceiver roadmap. In addition, the RF roadmap will drive the need for integration of asymmetrical devices (drain extensions) to increase the voltage handling capability of CMOS drivers and power management devices and possibly the use of laterally diffused channels to improve performance of high voltage devices (LDMOS). Also metal gates may be introduced sooner than in mixed-signal technology because of the higher losses associated with gate resistance at higher frequencies.

Integration of higher quality and higher density MIM capacitors and inductors are also identified challenges for the RF transceiver roadmap. Potential solutions for MIM capacitors include the introduction of high-κ dielectrics now being developed for future use as gate dielectrics. For inductors, thicker layers of Cu and thicker top dielectrics are likely to enable the roadmap but these may co-exist with inductors integrated in the package for the most demanding applications.



ALE—atomic layer epitaxy

Figure 36 RF Transceivers Potential Solutions

POWER AMPLIFIERS AND POWER MANAGEMENT

SiGe has established itself as the technology of choice for cellular receivers. Its superior noise figure and gain characteristics, coupled with state of the art 1/f noise properties, allow extremely efficient and compact receiver block designs. However, its integration cost in a standard CMOS flow is quite significant. There are several design groups looking at deep submicron CMOS as an alternative to SiGe.

At this time, InP-based HBTs devices do not appear to have found a niche. The broadband business appears to be more than adequately covered by SiGe HBTs with the device actually ahead of current bandwidth requirements. In the commercial PA business InP does not have a high enough breakdown voltage to withstand the required specifications with the present day battery voltages. If the frequency of operation for commercial radios greatly increases, then the need for these devices will also increase.

Since the module footprint is continually shrinking while the module complexity is continually growing, a technology capable of integrating more of the radio functions will ultimately be the technology of choice. This approach is primarily to reduce the total number of chips in a module. Two of these RF functions are filters and transmit receive (T/R) switches. If MEM switch reliability improves and their voltage requirements decrease, they can potentially offer a post-processing integration solution for both GaAs and Si technologies. Integration of filter functions also presents an issue for inclusion in a semiconductor technology. To date, only filter bulk acoustic resonator (FBAR) technologies and MEMs resonators have appeared as possible candidates for integration.

MILLIMETER WAVE

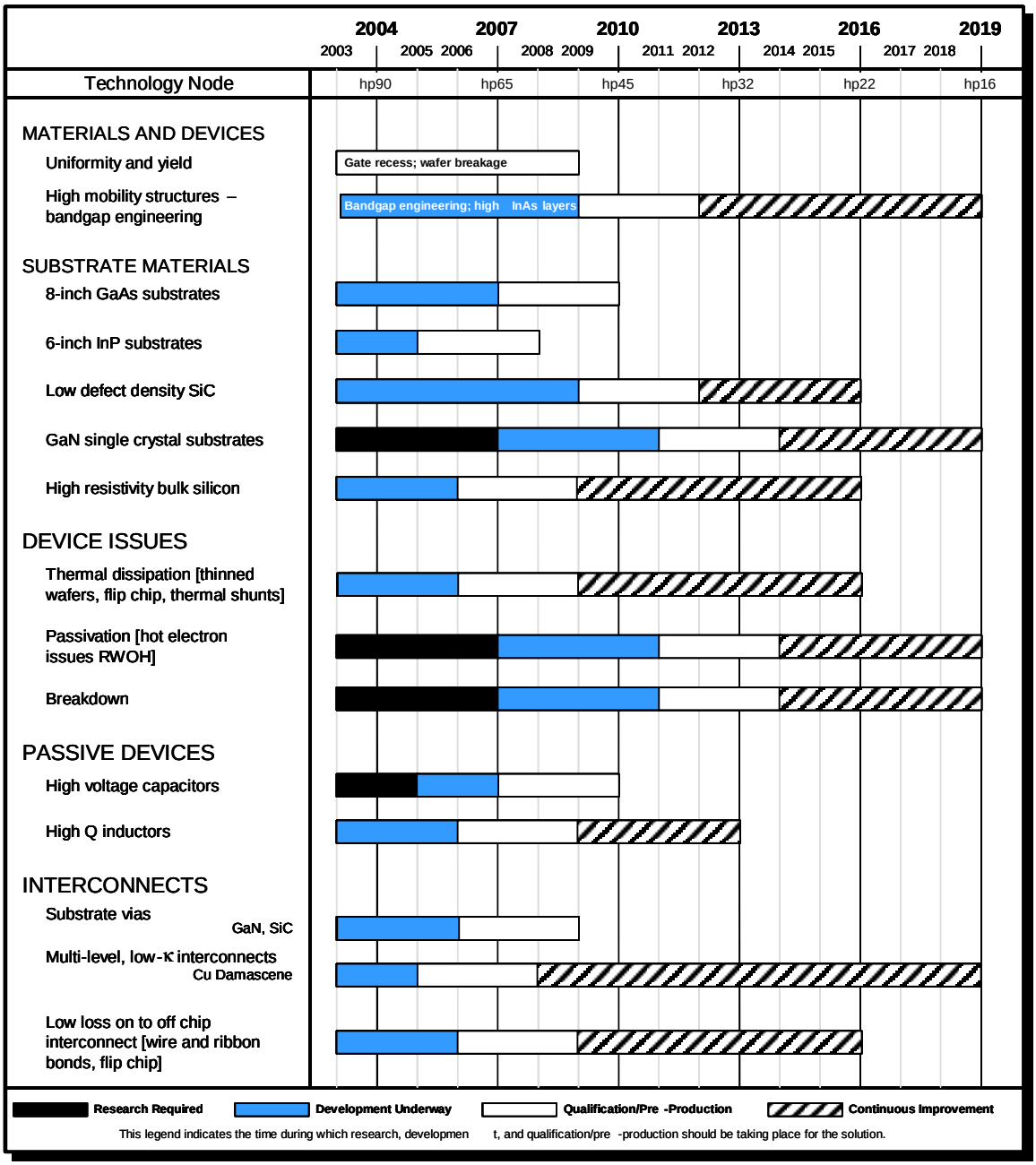
Compound semiconductors must take advantage of the advances in lithography and processing equipment that are evolving now in the digital silicon industry. In order to accomplish this, wafer diameter needs to be within one or two generations of the silicon industry. Six-inch semi-insulating GaAs wafers are in production now with InP not far behind. However, the III-V industry needs to continue to push to larger wafer sizes as silicon transitions from eight to twelve-inch diameter wafers. While significant advances are being made in optical lithography tools, the cost of masks is prohibitive for most of the relatively low volume III-V applications. Direct-write electron beam is a solution to the mask cost, but wafer through-put [measured in hours per wafer, as opposed to wafers per hour] needs to be improved with high current electron sources and fast alignment systems.

Substrate quality is still problematic for the emerging wide bandgap devices. Research on GaN templates is continuing, but in the interim, SiC substrates will become more viable as the defect density is improved. If SiGe is to challenge the mm-wave spectrum, high resistivity low-loss silicon needs to be addressed.

Thermal dissipation is the major challenge for wide-bandgap III-V power devices. While GaN and SiC substrates have higher thermal conductance values compared to GaAs and InP, the 5–10× higher power densities typically present in these wide bandgap semiconductors somewhat offsets the advantage in higher thermal conductance. These circumstances make thermal dissipation a critical device design aspect. Proven techniques include thin [0.002-inch] wafers, thermal shunts, and bathtub vias. These techniques, as well as more innovative solutions, need to be applied to the wide bandgap devices.

High voltage breakdown is desirable for both mixed-signal as well as high-power devices. As dimensions are scaled downward for higher frequency performance, the operating voltage suffers. This is particularly troublesome for mixed-signal devices that require more headroom for the analog functions than for the digital functions. In this regard, InP HBTs offer a distinct advantage over SiGe HBTs, although the integration level offered by SiGe will be orders of magnitude greater. Careful device scaling and wide-bandgap collectors can help maintain breakdown in InP HBTs. For power FETs, gate recessing has been used successfully to achieve higher breakdown, but this has yet to be applied to GaN. Tailoring of the vertical dimensions of the source-drain region to optimize the surface electric fields is a potential solution. Continued improvement of passivation and hot carrier effects is also needed.

Finally, high frequency performance in III-Vs is driven as much by epitaxy (vertical scaling) as by lithography (horizontal scaling). Carrier velocity and mobility in the transport layer can be tailored by proper engineering of the epitaxial layer stack and continued improvement in all of the III-V devices can be expected through bandgap engineering.



RWOH—reliability without hermiticity

Figure 37 Millimeter Challenges and Potential Solutions

CROSS-CUT ITWG ISSUES

Key crosscutting and liaison issues with other ITRS international technology working groups (ITWGs) are discussed below. The issues listed typically concern combinations of analog/mixed-signal, RF transceiver, power amplifier and power management, and mm-wave technologies.

ASSEMBLY AND PACKAGING

- RF module/SIP drives the need for chip and package co-design

EMERGING RESEARCH DEVICES

- Analog functions and performance with novel structures

FRONT END PROCESSES/INTERCONNECT

- Low inductance ground connection
- Suppressing electrical interference/cross talk/signal isolation
- High Q inductors
- Substrate (low/high resistivity)

MODELING AND SIMULATION

- SOC device/circuit/system modeling
- Accurate, fast and predictive analog/RF compact models
- Computationally efficient physical models for carrier transport in compound semiconductors

DESIGN/TEST

- Device design for reduced RF device/circuits characterization and test
- Find cost effective, but high performance mix of devices for RF, analog and digital circuits in SOC or SIP solutions for wireless technologies
- Build cross talk immune circuits for SOC and SIP integration

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

Because there have been no confirmed reports in the open literature of technical data on the RF and analog performance of emerging research devices, we cannot assess the impact of emerging research devices on RF and analog performance. Emerging research devices such as resonant tunneling devices, spin transistors, carbon nanotubes, molecular electronics, planar double-gate transistors, and 3D structures including vertical transistors, all are expected to present RF and AMS challenges and may also present opportunities for RF and AMS applications that demand increased performance, reliability, and functionality.

A common technical challenge for most, if not all, RF and AMS applications of emerging research devices is to understand the chemistry and physics of the electrical contacts well enough so that the RF and analog properties are controlled and reproducible in high volumes. Also, the impacts on figures of merit such as 1/f noise, power added efficiency, linearity, bandwidth, gain, ruggedness, and reliability are not known. Measuring and determining such impacts on figures of merit will present new areas for significant research and development. This research will exploit the additional degrees of engineering freedom that many emerging research devices offer. Two examples of additional degrees of engineering freedom controlling independently the voltage of multiple-gated devices and using an electric field applied perpendicularly to the axis of carbon nanotubes to alter their band structures.