INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

YIELD ENHANCEMENT

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

TABLE OF CONTENTS

Scope ... 1
Difficult Challenges ... 1
  Needed Research ... 2
Technology Requirements ... 3
  Yield Model and Defect Budget ... 3
  Defect Target Calculator ... 8
  Defect Detection and Characterization ... 9
  Yield Learning ... 12
    Visible Defects ... 14
    Non-visual Defects ... 14
    Parametric Defects ... 15
    Electrical Faults ... 15
    Data Management Systems ... 15
  Wafer Environmental Contamination Control ... 17
Potential Solutions ... 29
  Yield Model and Defect Budget ... 29
  Defect Detection and Characterization ... 29
  Yield Learning ... 30
    Visible Defects ... 31
    Non-visual Defects ... 31
    Parametric Defects ... 32
    Electrical Faults ... 32
    Data Management Systems (DMS) ... 32
  Wafer Environmental Contamination Control ... 33

LIST OF FIGURES

Figure 76 General Test Methodology for Ultrapure Water ... 19
Figure 77 Yield Model and Defect Budget Potential Solutions ... 29
Figure 78 Defect Detection and Characterization Potential Solutions ... 30
Figure 79 Yield Learning Potential Solutions ... 33
Figure 80 Wafer Environmental and Contamination Control Potential Solutions ... 34

LIST OF TABLES

Table 107 Yield Enhancement Difficult Challenges....2
Table 108 Defect Budget Technology Requirement Assumptions....4
Table 109a Yield Model and Defect Budget MPU Technology Requirements—Near-term....4
Table 109b Yield Model and Defect Budget MPU Technology Requirements—Long-term....5
Table 110a Yield Model and Defect Budget DRAM Technology Requirements—Near-term....6
Table 110b Yield Model and Defect Budget DRAM Technology Requirements—Long-term....7
Table 111 Defect Target Calculator....8
Table 112a Defect Detection Technology Requirements—Near-term....10
Table 112b Defect Detection Technology Requirements—Long-term....11
Table 113a Yield Learning Technology Requirements—Near-term....16
Table 113b Yield Learning Technology Requirements—Long-term....17
Table 114a Technology Requirements for Wafer Environmental Contamination Control—Near-term....21
Table 114b Technology Requirements for Wafer Environmental Contamination Control—Long-term....26

YIELD ENHANCEMENT

SCOPE

Yield Enhancement (YE) is defined as the process of improving the baseline yield for a given technology node from R&D yield level to mature yield. The definition assumes a functional baseline process for a given process technology and it's compatibility with the design of the product being fabricated. The definition reinforces the chapter focus on the yield ramp portion of the yield learning curve. The YE chapter scope is limited to wafer sort yield. The YE chapter does not address fab line yield, assembly/packaging yield, and final test yield.

The Yield Enhancement Chapter is partitioned into four focus topics: Yield Model and Defect Budget, Defect Detection and Characterization, Yield Learning, and Wafer Environment(s) Contamination Control. Key business metrics rely on the success of rapid yield ramp and the associated competencies found within these four focus topics, particularly with the introduction of 300 mm manufacturing. These competencies crosscut all process technologies, as well as the facility infrastructure, integrated circuit (IC) design, and process integration. Key messages include continued emphasis on reduction of process- and equipment-generated defects to meet defect targets for mature product yields. Significant efforts will be necessary to baseline, reduce and control yield loss associated with systematic mechanisms. Defect-to-fault and fault-to-defect mapping, kill ratios, and failure isolation techniques are also critical challenges as physical device dimensions and corresponding defect dimensions continue to shrink. There must be renewed development of defect detection, review, and classification technologies where much greater sensitivity and throughput is necessary. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and WIP data, will have to be developed to enable rapid yield learning. Specific recommendations are needed for standard monitor-wafer preparation, detection recipes, edge exclusion, test structures, short/long loops and sampling to ensure line control and yield improvement. Order-of-magnitude improvements in process critical fluid and gas impurity levels are not believed to be necessary well into the sub-90 nm technology nodes. Clarification of potential contamination from point-of-delivery to point-of-use will define control systems necessary for delivered purity. Pre-cursors for all new materials will need to be evaluated.

DIFFICULT CHALLENGES

The difficult challenges for the yield enhancement chapter are summarized in Table 107. Detection of ever shrinking yield critical defects, high aspect ratio defects, non-visual defects and timely elimination of yield detracting systematic mechanisms top the list of challenges for the Yield Enhancement chapter. Moreover, the yield enhancement community is constantly challenged to achieve acceptable yield ramp and mature yields due to increasing process complexity and fewer yield learning cycles with each subsequent technology node.

Defect budgets will require periodic revalidation and updates, as information about future processing technologies becomes available. Yield models need to better consider complex integration issues with respect to random defect-limited yield as well as systematic mechanisms limited yield (such as parametric yield loss, circuit yield loss, etc.) for future technology nodes. Future defect models must consider electrical characterization information, with reduced emphasis on optical inspections and analysis. Detecting defects associated with high aspect ratio contacts, and combinations of trenches and vias in dual-damascene structures will continue to be difficult defect detection challenges. More specifically, the detection of via defects within the structure of a damascene trench on a process layer containing up to 10 billion similar structures will continue to be the grand challenge. The challenge is complicated by the simultaneous need for high sensitivity and high throughput, two detection characteristics that normally are caught in a trade-off as the fabrication facility moves from optimization of tool performance for baseline yield learning to production line monitoring. Fault isolation complexity is expected to grow exponentially, combining the difficult tasks of defining fault dimensions in the horizontal plane and vertical layers (stack). Analyzing circuit failures that leave no detectable physical remnant presents an extremely difficult challenge. Statistical means of accurately dealing with near-zero defect adder data that frequently exhibit high coefficients of variation is a fundamental data reduction challenge. Through the use of advanced test structures and modeling techniques, the fundamental challenge in the area of process critical materials is to understand the correlation between impurity concentration and device yield, reliability, and performance. This correlation will determine whether increasingly stringent contamination limits are truly required and will provide early warning of the need for tighter specifications. Process tools must have increased capability to automatically self-monitor production for yield excursions, failures, and faults and to initiate corrective actions.

Table 107 Yield Enhancement Difficult Challenges

Difficult Challenge ≥45 nm/Through 2010	*Summary of Issues*
Design for Manufacture and Test (DFM and DFT) and Systematic Mechanisms Limited Yield (SMLY)—IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.	Design to process compatibility, design for manufacturability, design for test, design for diagnosability, systematic mechanisms limited yield (SMLY) model development.
High-Aspect-Ratio Inspection—High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Detection of Ever Shrinking Yield Critical Defects—High throughput, high capture rate detection tools are needed for ever shrinking critical defects of interest.	Line edge roughness, ACLV, subtle process variation. Where does process variation stop and defect start? Need to improve signal to noise to delineate defect from process variation.
Non-visual Defect Sourcing—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
Difficult Challenge <45 nm/Beyond 2010	*Summary of Issues*
Develop Yield Models that include New Materials and Integration—Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.
Correlation of Impurity Level to Yield—Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product.	Establish an employment methodology for each material type. Define a standard test for yield/parametric effect.
Yield Ramp and Mature Yields—With increasing process complexity and fewer yield learning cycles with each subsequent technology node, it would be impossible to achieve historic yield ramps and mature yield levels.	Long and complex process will make achieving historic yield ramps challenging. Also, new materials will introduce previously unseen yield problems. Need tools and methods to shorten yield learning cycles

NEEDED RESEARCH

The technology requirements and potential solutions described below call for continued cooperation between all stakeholders. For example, tool defect data is needed from semiconductor manufacturers to validate the random defect limited yield model. Innovative algorithms for defect sourcing will be required for rapid yield learning, particularly when the electrical fault has no detectable optical or SEM image.

For High Aspect Ratio Inspection (HARI) applications and at defect sizes below 100 nm (diameter), defect detection and characterization will be hampered by detection tools having low throughput and high cost-of-ownership. An economical solution must be found if large risk to production inventory is to be avoided.

Wafer Environment(s) Contamination Control must center attention on the point of use of a pure material since realistic cost of manufacture must be maintained. Innovative ideas need to be studied, such as local filtering of only undesirable contaminants from a re-usable process gas/fluid. Vendors for pre-cursors for all new materials will need to examine their purity requirements in the context of their respective applications.

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

$$Y_{Die} = Y_S * Y_R = Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha}$$

The overall die yield of an IC process can broadly be described as a product of systematic (or gross) limited yield (Y_S) and random-defect limited yield (Y_R). The defect budget technology requirements defined in Tables 109 and 110 are based on a negative binomial yield model where Y_R is the random-defect limited yield, A is the area of the device, D_0 is the electrical fault density, and α is the cluster factor. Assumptions for the defect budget technology requirements in this revision are indicated in Table 108. The defect budget target calculation for the 2003 ITRS is based on results of three studies (1997, 1999, and 2000) of particles per wafer pass (PWP) levels at international SEMATECH member companies. These targets were extrapolated from median PWP value per generic process tool type and then scaled to an MPU and a DRAM generic process-flow respectively. Note that the defect budget targets for all process steps include wafer-handling defectivity of the process tool. In addition a 10% wafer per lot sampling rate for inspection and measurement was assumed.

This PWP extrapolation equation was used to calculate PWP budget values from technology node to technology node. The extrapolation takes into consideration increase in chip size, increase in complexity, and shrinking feature size. In this equation PWP is the particles per wafer pass defect density per square meter, F is the average faults per mask level (determined by the random electrical fault density (D0) divided by number of masks at a given technology node), S is the minimum critical defect size, and n refers to the technology node. All PWP budget values are defined with respect to a critical defect size. Each entry in the PWP section of Tables 109 and 110 refers to a generic tool type used in the MPU and/or in the DRAM process flow. Since future actual tools and processes are not known, this roadmap assumes that no new process, material, or tool will be acceptable with a larger PWP budget than prior methods. This assumption needs periodic validation. This defect budgeting method tends to be a worst-case model since all process steps are assumed to be at minimum device geometry. In actuality, many processes allow process zones with more relaxed geometries. However, the same tools are used for both minimum and relaxed geometries. The costs of underestimating yield (unused capacity costs) are small and may be offset by the opportunity for additional production. The major driver for increased cost due to overestimating yield is the cost of scrapped material. Thus, a worst-case defect budgeting model is prudent.

Table 108 states the yield, and the product maturity assumptions that were used in calculating electrical fault density values and PWP defect budget target values for MPUs and DRAMs respectively. These assumptions for the most part are as defined in the ORTC. Cluster Parameter value returned to two from five, because the value two is more appropriate to explain the defect distribution among most fabs. Table 109 presents the random PWP defect budget targets necessary to meet the stated assumptions for a cost-performance MPU as defined in the ORTC Table 1a+1b. This MPU is assumed to have a small L1 cache, but the device consists primarily of logic transistor functionality. With respect to MPUs, this analysis assumes that the process/design improvement target factor (1g+1h) in each technology node is met. Similarly, Table 110 presents the random PWP budget targets necessary to meet the yield assumptions stated in Table 108 for DRAMs. The electrical fault density that is used to calculate faults per mask level (which is used as input to the PWP extrapolation equation) is based on only the periphery (logic/decoder) area of the DRAM chip. This is projected in the ORTC to be 37% of chip area at the stated product maturity. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM can implement redundancy to attain the overall yield target of 85%. DRAM chip size is enlarged at the timing of the new generation product introduction, and it shrinks during the period of the same generation product manufacturing as ORTC Table 1c+1d show. So the DRAM chip size fluctuates and the defect budgets, derived from the chip size, fluctuate accordingly. A calculator for scaling the contents of Tables 109 and 110 to specific user yield, technology, and chip size requirements is included in this ITRS revision as Table 111.

Besides continuous improvement in tool cleanliness, there are at least two other major challenges that must be addressed going forward in order to achieve acceptable yields:

1. With systematic mechanisms limited yield (SMLY) dominating the rate of yield learning, a concerted effort is required to understand, model and eliminate SMLY detractors.
2. The impact of line edge roughness (LER) on yield needs to be understood, modeled and controlled to achieve acceptable yields for current and future technology nodes.

Table 108 Defect Budget Technology Requirement Assumptions

Product	MPU	DRAM
Yield Ramp Phase	Volume Production	Volume Production
$Y_{OVERALL}$	75%	85%
Y_{RANDOM}	83%	89.50%
$Y_{SYSTEMATIC}$	90%	95%
Cluster Parameter	2	2

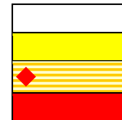
Table 109a Yield Model and Defect Budget MPU Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
MPU							
MPU ½ Metal One Pitch (nm) [A]	107	90	80	70	65	57	50
Critical Defect Size (nm)	54	45	40	35	33	29	25
Chip Size (mm^2) [B]	140	140	140	140	140	140	140
Overall Electrical D_0 (faults/m^2) at Critical Defect Size Or Greater [C]	2210	2210	2210	2210	2210	2210	2210
Random D_0 (faults/m^2) [D]	1395	1395	1395	1395	1395	1395	1395
Number of Mask Levels [E]	29	31	33	33	33	35	35
Random Faults/Mask	48	45	42	42	42	40	40
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 54 nm Critical Defect Size Or Greater							
CMP clean	397	263	195	149	129	93	72
CMP insulator	961	636	472	362	312	226	174
CMP metal	1086	719	534	409	352	255	197
Coat/develop/bake	174	115	85	65	56	41	31
CVD insulator	854	565	420	321	277	201	155
CVD oxide mask	1124	744	552	423	364	264	203
Dielectric track	273	181	134	103	89	64	49
Furnace CVD	487	322	239	183	158	114	88
Furnace fast ramp	441	292	217	166	143	104	80
Furnace oxide/anneal	285	188	140	107	92	67	52
Implant high current	381	252	187	143	124	90	69
Implant low/medium current	348	230	171	131	113	82	63
Inspect PLY	355	235	174	133	115	83	64
Inspect visual	380	252	187	143	123	89	69
Lithography cell	294	195	145	111	95	69	53
Lithography stepper	279	185	137	105	91	66	51
Measure CD	332	220	163	125	108	78	60
Measure film	285	188	140	107	92	67	52
Measure overlay	264	175	130	99	86	62	48
Metal CVD	519	343	255	195	168	122	94
Metal electroplate	268	177	132	101	87	63	48
Metal etch	1153	763	566	434	374	271	209
Metal PVD	591	391	291	222	192	139	107
Plasma etch	1049	694	515	395	340	247	190
Plasma strip	485	321	238	182	157	114	88
RTP CVD	317	210	156	119	103	74	57
RTP oxide/anneal	208	137	102	78	67	49	38
Test	81	53	40	30	26	19	15
Vapor phase clean	729	482	358	274	236	171	132
Wafer handling	33	22	16	12	11	8	6
Wet bench	474	314	233	178	154	112	86

Table 109b Yield Model and Defect Budget MPU Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
MPU ½ metal one Pitch (nm) [A]	45	35	32	25	22	18
Critical Defect Size (nm)	23	18	16	13	11	9
Chip Size (mm^2) [B]	140	140	140	140	140	140
Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater [C]	2210	2210	2210	2210	2210	2210
Random D_0 (faults/m^2) [D]	1395	1395	1395	1395	1395	1395
Number of Mask Levels [E]	35	35	35	37	39	39
Random Faults/Mask	40	40	40	38	36	36
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 54 nm Critical Defect Size or Greater						
CMP clean	58	35	29	17	12	8
CMP insulator	141	85	71	41	30	20
CMP metal	159	96	81	46	34	23
Coat/develop/bake	25	15	13	7	5	4
CVD insulator	125	76	63	37	27	18
CVD oxide mask	165	100	83	48	35	24
Dielectric track	40	24	20	12	9	6
Furnace CVD	71	43	36	21	15	10
Furnace fast ramp	65	39	33	19	14	9
Furnace oxide/anneal	42	25	21	12	9	6
Implant high current	56	34	28	16	12	8
Implant low/medium current	51	31	26	15	11	7
Inspect PLY	52	31	26	15	11	7
Inspect visual	56	34	28	16	12	8
Lithography cell	43	26	22	13	9	6
Lithography stepper	41	25	21	12	9	6
Measure CD	49	29	25	14	10	7
Measure film	42	25	21	12	9	6
Measure overlay	39	23	20	11	8	6
Metal CVD	76	46	38	22	16	11
Metal electroplate	39	24	20	11	8	6
Metal etch	169	102	85	49	36	24
Metal PVD	87	52	44	25	19	12
Plasma etch	154	93	78	45	33	22
Plasma strip	71	43	36	21	15	10
RTP CVD	46	28	23	14	10	7
RTP oxide/anneal	30	18	15	9	7	4
Test	12	7	6	3	3	2
Vapor phase clean	107	65	54	31	23	15
Wafer handling	5	3	2	1	1	1
Wet bench	70	42	35	20	15	10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 109a and 109b:
[A] As defined in the ORTC Table 1a+1b
[B] As defined in the ORTC Table 1g+1h
[C] Based on assumption of 75% overall volume production yield.
[D] As defined in the ORTC Table 5a+5b. Based on assumption of 83% Random Defect Limited Yield (RDLY)
[E] As defined in the ORTC Table 5a+5b

Table 110a Yield Model and Defect Budget DRAM Technology Requirements—Near-term

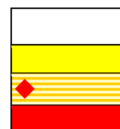
Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
DRAM ½ Pitch (nm) [A]	**100**	**90**	**80**	**70**	**65**	**57**	**50**
Critical Defect Size (nm)	**50**	**45**	**40**	**35**	**33**	**29**	**25**
Chip Size (mm^2) [B]	**139**	**110**	**82**	**122**	**97**	**131**	**104**
Cell Array Area (%) at Production [B]	**63%**	**63%**	**63%**	**63%**	**63%**	**63%**	**63%**
Non-core Area (mm^2)	**51**	**41**	**30**	**45**	**36**	**49**	**39**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**3288**	**4143**	**5568**	**3758**	**4735**	**3480**	**4385**
Random D_0 (faults/m^2) [D]	**2216**	**2791**	**3751**	**2532**	**3190**	**2345**	**2954**
Number of Mask Levels [E]	**24**	**24**	**24**	**24**	**24**	**24**	**24**
Random Faults/Mask	**92**	**116**	**156**	**106**	**133**	**98**	**123**
DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 50 nm Critical Defect Size or Greater							
CMP clean	**1068**	**1068**	**1068**	**598**	**598**	**367**	**356**
CMP insulator	**827**	**827**	**827**	**463**	**463**	**284**	**276**
CMP metal	**1267**	**1267**	**1267**	**709**	**709**	**435**	**422**
Coat/develop/bake	**331**	**331**	**331**	**185**	**185**	**114**	**110**
CVD insulator	**916**	**916**	**916**	**513**	**513**	**315**	**305**
CVD oxide mask	**1125**	**1125**	**1125**	**630**	**630**	**387**	**375**
Dielectric track	**464**	**464**	**464**	**260**	**260**	**159**	**155**
Furnace CVD	**633**	**633**	**633**	**355**	**355**	**218**	**211**
Furnace fast ramp	**597**	**597**	**597**	**334**	**334**	**205**	**199**
Furnace oxide/anneal	**477**	**477**	**477**	**267**	**267**	**164**	**159**
Implant high current	**555**	**555**	**555**	**311**	**311**	**191**	**185**
Implant low/medium current	**529**	**529**	**529**	**296**	**296**	**182**	**176**
Inspect PLY	**724**	**724**	**724**	**405**	**405**	**249**	**241**
Inspect visual	**746**	**746**	**746**	**418**	**418**	**257**	**249**
Lithography cell	**619**	**619**	**619**	**347**	**347**	**213**	**206**
Lithography stepper	**412**	**412**	**412**	**231**	**231**	**142**	**137**
Measure CD	**618**	**618**	**618**	**346**	**346**	**213**	**206**
Measure film	**582**	**582**	**582**	**326**	**326**	**200**	**194**
Measure overlay	**566**	**566**	**566**	**317**	**317**	**195**	**189**
Metal CVD	**583**	**583**	**583**	**326**	**326**	**200**	**194**
Metal electroplate	**443**	**443**	**443**	**248**	**248**	**152**	**148**
Metal etch	**1072**	**1072**	**1072**	**600**	**600**	**369**	**357**
Metal PVD	**639**	**639**	**639**	**358**	**358**	**220**	**213**
Plasma etch	**1136**	**1136**	**1136**	**636**	**636**	**390**	**379**
Plasma strip	**872**	**872**	**872**	**488**	**488**	**300**	**291**
RTP CVD	**570**	**570**	**570**	**319**	**319**	**196**	**190**
RTP oxide/anneal	**417**	**417**	**417**	**233**	**233**	**143**	**139**
Test	**81**	**81**	**81**	**46**	**46**	**28**	**27**
Vapor phase clean	**1206**	**1206**	**1206**	**675**	**675**	**415**	**402**
Wafer handling	**34**	**34**	**34**	**19**	**19**	**12**	**11**
Wet bench	**864**	**864**	**864**	**484**	**484**	**297**	**288**

Notes for Tables 110a and 110b:
[A] As defined in the ORTC Table 1a+1b
[B] As defined in the ORTC Table 1c+1d
[C] As defined in the ORTC Table 5a+5b. Based on assumption of 89.5% Random Defect Limited Yield (RDLY)
[D] As defined in the ORTC Table 5a+5b. Based on assumption of 89.5% Random Defect Limited Yield (RDLY)
[E] As defined in the ORTC Table 5a+5b

Table 110b Yield Model and Defect Budget DRAM Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
DRAM ½ Pitch (nm) [A]	**45**	**35**	**32**	**25**	**22**	**18**
Critical Defect Size (nm)	**23**	**18**	**16**	**13**	**11**	**9**
Chip Size (mm^2) [B]	**83**	**104**	**83**	**104**	**138**	**87**
Cell Array Area (%) at Production [B]	**63%**	**63%**	**63%**	**63%**	**63%**	**63%**
Non-core Area (mm^2)	**31**	**39**	**31**	**39**	**51**	**32**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**5524**	**4385**	**5524**	**4385**	**3315**	**5261**
Random D_0 (faults/m^2) [D]	**3722**	**2954**	**3722**	**2954**	**2233**	**3545**
# Mask Levels [E]	**26**	**26**	**26**	**26**	**26**	**26**
Random Faults/Mask	**143**	**114**	**143**	**114**	**86**	**136**
DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type Scaled to 50 nm Critical Defect Size or Greater						
CMP clean	**335**	**161**	**161**	**82**	**48**	**51**
CMP insulator	**260**	**125**	**125**	**64**	**37**	**40**
CMP metal	**398**	**191**	**191**	**97**	**57**	**61**
Coat/develop/bake	**104**	**50**	**50**	**25**	**15**	**16**
CVD insulator	**288**	**138**	**138**	**70**	**41**	**44**
CVD oxide mask	**353**	**170**	**170**	**87**	**51**	**54**
Dielectric track	**146**	**70**	**70**	**36**	**21**	**22**
Furnace CVD	**199**	**95**	**95**	**49**	**29**	**30**
Furnace fast ramp	**187**	**90**	**90**	**46**	**27**	**29**
Furnace oxide/anneal	**150**	**72**	**72**	**37**	**22**	**23**
Implant high current	**174**	**84**	**84**	**43**	**25**	**27**
Implant low/medium current	**166**	**80**	**80**	**41**	**24**	**25**
Inspect PLY	**227**	**109**	**109**	**56**	**33**	**35**
Inspect visual	**234**	**113**	**113**	**57**	**34**	**36**
Lithography cell	**194**	**93**	**93**	**48**	**28**	**30**
Lithography stepper	**129**	**62**	**62**	**32**	**19**	**20**
Measure CD	**194**	**93**	**93**	**48**	**28**	**30**
Measure film	**183**	**88**	**88**	**45**	**26**	**28**
Measure overlay	**178**	**85**	**85**	**44**	**25**	**27**
Metal CVD	**183**	**88**	**88**	**45**	**26**	**28**
Metal electroplate	**139**	**67**	**67**	**34**	**20**	**21**
Metal etch	**337**	**162**	**162**	**82**	**48**	**51**
Metal PVD	**201**	**96**	**96**	**49**	**29**	**31**
Plasma etch	**357**	**171**	**171**	**87**	**51**	**54**
Plasma strip	**274**	**131**	**131**	**67**	**39**	**42**
RTP CVD	**179**	**86**	**86**	**44**	**26**	**27**
RTP oxide/anneal	**131**	**63**	**63**	**32**	**19**	**20**
Test	**26**	**12**	**13**	**6**	**4**	**4**
Vapor phase clean	**379**	**182**	**182**	**93**	**54**	**58**
Wafer handling	**11**	**5**	**5**	**3**	**2**	**2**
Wet bench	**271**	**130**	**130**	**66**	**39**	**41**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



DEFECT TARGET CALCULATOR

The random defect targets in Tables 109 and 110 are based on predefined technology nodes, using data collected by International SEMATECH member companies on 164 tools, which are divided into 30 generic tool categories. Even with targets for both memory and logic products, rarely do actual user circuit line widths and areas match the ITRS technology node assumptions. Therefore Wright Williams and Kelly developed a defect target calculator[1] to help semiconductor suppliers and manufacturers compare the roadmap targets to their current or planned needs.

INSTRUCTIONS

The defect target calculator, shown as a static example as Table 111, allows users to enter key technology parameters and estimate a defect target for a specific chip.

To be able to activate click once here for the *live version file of this calculator* or right click to download the file to your computer.

The only parameters required are the *Minimum Critical Defect Size*, *Random Defect Limited Yield Requirement*, *Chip Size*, *Number Of Mask Levels, and for memory only, the Peripheral (Logic) Chip Area*. This calculator uses the same extrapolation method as the roadmap tables.

DEFINITIONS

Minimum Critical Defect Size—One half the user's Metal 1 pitch for the technology of interest (nanometers)

Random Defect limited Yield—Portion of your yield, which is reduced based on your random defectivity. Has to be multiplied by the systematic limited yield to calculate the overall die yield (%)

Chip Size—The area (critical or hole die size) of the user's device (square millimeters)

Mask Levels—The number of mask levels in the user's technology

Peripheral (Logic) Chip Area—Area of the layout without redundancy, chip area minus cell area (%). Only used in the DRAM calculation

Table 111 Defect Target Calculator

	MPU	**DRAM**	**User Input**	
Minimum Critical Defect Size (nm)	53.5	50	53.5	
Random Defect Limited Yield (%)	83.0%	89.5%	83.0%	
Chip Size (mm^2)	140	139	140	
Number of Mask Levels	29	24	29	
Peripheral (Logic) Chip Area (%)	NA	37.0%	100.0%	
Random D_0 (faults/m^2)	1395	2216	1395	1395
Random Faults/Mask	48	92	48	48
			User Targets	
			MPU	***DRAM***
CMP clean	397	1068	397	637
CMP insulator	961	827	961	493
CMP metal	1086	1267	1086	756
Coat/develop/bake	174	331	174	197
CVD insulator	854	916	854	547
CVD oxide mask	1124	1125	1124	671
Dielectric track	273	464	273	277
Furnace CVD	487	633	487	378
Furnace fast ramp	441	597	441	356
Furnace oxide/anneal	285	477	285	285
Implant high current	381	555	381	331
Implant low/medium current	348	529	348	316
Inspect PLY	355	724	355	432
Inspect visual	380	746	380	445
Lithography cell	294	619	294	369
Lithography stepper	279	412	279	246
Measure CD	332	618	332	369
Measure film	285	582	285	347
Measure overlay	264	566	264	338
Metal CVD	519	583	519	348
Metal electroplate	268	443	268	264
Metal etch	1153	1072	1153	640
Metal PVD	591	639	591	381
Plasma etch	1049	1136	1049	677
Plasma strip	485	872	485	520
RTP CVD	317	570	317	340
RTP oxide/anneal	208	417	208	249
Test	81	81	81	49
Vapor phase clean	729	1206	729	719
Wafer handling	33	34	33	20
Wet bench	474	864	474	515

[1] *Developed by Darren Dance, Wright, Williams, and Kelly. 1999.*

DEFECT DETECTION AND CHARACTERIZATION

The ability to detect inline yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production—process research and development (PRD), yield ramp (YR), and volume production (VP)—broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabs begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the chip manufacturers just-in-time for each phase of the process cycle. Tools that meet the requirements for PRD are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate YR must be available several months before production begins. Finally, the ability to monitor excursions at a technology node is needed when the product hits high yield levels.

Technology requirements are separated into unpatterned wafer inspection, patterned wafer inspection, and high aspect ratio inspection, as shown in Table 112. The effects of the buried patterning in post-chemical mechanical planarization (CMP) wafers makes patterned wafer inspection with grazing angle laser inspection tools approximate unpatterned inspection for the purposes of tool qualification, and appropriate for this roadmap. Also, unpatterned inspection utilized extensively for tool qualification, has implemented defect review from such scans, which has increased in importance in the last few years. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is treated separately from patterned wafer inspection due to special sensitivity requirements described in the Difficult Challenges section as well as note C under Table 112. Best HARI defect detection tools will be able to indicate 0.3 × technology node events for contact and via shape (defined at the bottom of the feature: highest resistive point), size, and remaining material, which is the optimum HARI defect definition. Again, current Table 112 revisions have the defect size at full feature, as detected by the current methods of voltage contrast, but manufacturing inputs still desire the .3× feature size due to detrimental resistivity impacts.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside requirements are based on lithography depth-of-focus considerations as stipulated in the *Lithography* chapter technology requirements table, and also defined slightly differently in the *Front End Process* Starting Materials table, and Surface Preparation table. A future requirement is the standardized inspection or contamination control on the wafer edge or on the wafer backside.

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers (defects that cannot be detected with conventional optical technologies) is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and back end of processing. Macro defects that impact large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved to match the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology node.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The price, fab space occupied, and the throughput of defect detection tools are major contributors to their cost-of-ownership (CoO). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table 112 have been stipulated on the basis of detecting accurately sized polystyrene latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pits pattern flaws, surface roughness, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers. Also, there is a need for developing unified

definition of defects based on yield impact. Another challenge is the separation of nuisance to real defects. A possible work around might be using ADC on inspection and review tools, which needs to be accurate and fast enough.

Defects detected on future technology generation wafers will require higher resolution microscopes for review. Rapid developments in Scanning Electron Microscopy (SEM) have already enabled quick review and classification of such defects. Speeding up SEM review could provide the opportunity to gather information on more defects than currently possible, thereby increasing yield learning.

Table 112a Defect Detection Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*								
Process R&D at 300 cm^2/hr (1 "200 mm wafer"/hr)	50	45	40	35	32.5	28.5	25	*0.5 x DR*
Yield ramp at 1200 cm^2/hr (4 "200 mm wafer"/hr)	80	72	64	56	52	45.6	40	*0.8 x DR*
Volume production at 3000 cm^2/hr (10 "200 mm wafer"/hr)	100	90	80	70	65	57	50	*1.0 x DR*
Tool matching (% variation tool to tool) [C]	5	5	5	3	3	3	3	
Wafer edge exclusion (mm)	2	1	1	1	1	1	1	
Cost of ownership ($/$cm^2$)	0.055	0.055	0.055	0.055	0.055	0.055	0.055	
*High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[D, E]*								
Sensitivity without speed requirement	100	90	80	70	65	57	50	*1.0 x DR*
Process verification at 300 cm^2/hr (1 "200 mm wafer"/hr)	◆ 100	90	80	70	65	57	50	*1.0 x DR*
Volume manufacturing at 1200 cm^2/hr (4 "200 mm wafer"/hr)	◆ 100	90	80	70	65	57	50	*1.0 x DR*
CoO HARI ($/$cm^2$)	◆ 0.66	0.66	0.66	0.66	0.66	0.66	0.66	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]								
Metal film	80	72	64	56	52	45.6	40	*0.8 x DR*
Bare silicon and non-metal film	50	45	40	35	32.5	28.5	25	*0.5 x DR*
Wafer backside (defect size, nm) [H]	100	90	80	70	65	57	50	*1.0 x DR*
CoO ($/$cm^2$)	0.0017	0.0017	0.0017	0.0017	0.0017	0.0017	0.0017	
Wafer edge exclusion (mm)	3	3	2	2	2	2	2	
Defect Review (Patterned Wafer)								
Resolution (nm) * [I]	2.5	2.3	2.0	1.8	1.6	1.4	1.3	*0.05 x pattern sensitivity R&D*
Coordinate accuracy (μm) at resolution [J]	1	1	1	1	1	1	1	
*Automatic Defect Classification at Defect Review Platform * [K]*								
Redetection: minimum defect size (nm)	40	36	32	28	26	22.8	20	*0.4 x DR*
Number of defect types [L]	◆ 10	15	15	15	15	15	15	
Speed (defects/hours)	512	720	720	720	720	720	720	
Speed w/elemental (defects/hours)	◆ 275	360	360	360	360	360	360	
Number of defect types (inline ADC) [M]	◆ 10	15	15	15	15	15	15	

**PSL—polystyrene latex (spheres utilized to simulate defects of known size during sizing calibration)*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

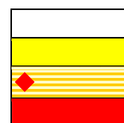
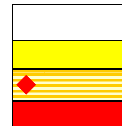


Table 112b Defect Detection Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*Driver*
Technology Node	*hp45*		*hp32*		*hp22*		
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*	
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*	
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*	
*Patterned Wafer Inspection, PSL Spheres * at 90% Capture, Equivalent Sensitivity (nm) [A, B]*							
Process R&D at 300 cm^2/hr (1 "200 mm wafer"/hr)	22.5	17.5	16	12.5	11	9	*0.5 x DR*
Yield ramp at 1200 cm^2/hr (4 '200 mm wafer"/hr)	36	28	25.6	20	17.6	14.4	*0.8 x DR*
Volume production at 3000 cm^2/hr (10 "200 mm wafer"/hr)	45	35	32	25	22	18	*1.0 x DR*
Tool matching (% variation tool to tool)[C]	2	2	2	2	2	2	
Edge exclusion (mm)	1	1	1	1	1	1	
Cost of Ownership ($/$cm^2$)	0.055	0.055	0.055	0.055	0.055	0.055	
*High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[D, E]*							
Sensitivity without speed requirement	45	35	32	25	22	18	*1.0 x DR*
Process verification at 300 cm^2/hr (1 "200 mm wafer"/hr)	45	35	32	25	22	18	*1.0 x DR*
Volume manufacturing at 1200 cm^2/hr (4 "200 mm wafer"/hr)	45	35	32	25	22	18	*1.0 x DR*
CoO HARI ($/$cm^2$)	0.66	0.66	0.66	0.66	0.66	0.66	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [F, G]							
Metal film	36	28	25.6	20	17.6	14.4	*0.8 x DR*
Bare silicon and non-metal films	22.5	17.5	16	12.5	11	9	*0.5 x DR*
Wafer backside (defect size nm) [H]	45	35	32	25	22	18	*1.0 x DR*
CoO ($/$cm^2$)	0.0017	0.0017	0.0017	0.0017	0.0017	0.0017	
Wafer edge exclusion (mm)	2	2	2	2	2	2	
Defect Review (Patterned Wafer)							
Resolution (nm) [I]	1.125	0.875	0.8	0.625	0.55	0.45	*0.05 x pattern sensitivity R&D*
Coordinate accuracy (µm) at resolution [J]	0.5	0.5	0.5	0.5	0.5	0.5	
Automatic Defect Classification [K]							
Re-detection minimum defect size (nm)	18	14	12.8	10	8.8	7.2	*0.4 x DR*
Number of defect types [L]	20	20	20	20	25	25	
Speed (defects/hour)	720	720	720	720	720	720	
Speed w/elemental (defect/hour)	360	360	360	360	360	360	
Number of defect types (inline ADC) [M]	20	20	20	20	25	25	

**PSL—polystyrene latex (spheres utilized to simulate defects of known size during sizing calibration)*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 112a and 112b:

[A] Patterned wafer scan speed is required to be at least 300 cm^2 /hour for process R&D mode, 1,200 cm^2 /hour for yield ramp mode, and, at least, 3,000 cm^2 /hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435. (Example: 3000 cm^2 /hr is about 10, 200 mm wafers and 4.3, 300 mm wafers).

[B] Patterned wafer nuisance defect rate shall be lower than 5% in all process phases. False counts in the R&D phase less than 5%, and less than 1% in the yield ramp and volume production phase. Nuisance is defined as an event indicated and a defect is present, just not the type of interest. These maybe significant and could be studied at a later date. The defect classifier must consider the defect type and assign significance. False is defined at an event is indicated, but no defect can be seen using the review optics path of the detection tool, which supports recipe setup validation.)

[C] Metric % variation tool-to-tool in number of non-matching defects/total number of defects from standard tool.

Procedure: Recipe sensitivity set on first (standard) tool with false <5. Transfer this recipe without changes and perform ten runs with a wafer containing a minimum of 30 defects.

[D] High Aspect Ration is defined as for contacts 15:1

[E] HARI defects are already considered "killers" at any process stage, but defined at the contact/via levels for full feature size capture. Hence, minimum defect sensitivity was stipulated as 1.0× technology node at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more is the model to be detected. If in the future, detection tools can determine size, shape, or remaining material on the order of 0.3× technology node, this will more adequately match known experience for resistance changes. Scan speed for HARi tools have been broken out into process verification and volume production types. Process verification usually refers to SEM-type tools (but not necessarily in the future) and includes voltage contrast capability. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435.

[F] Un-patterned wafer defect detection tools will be required to scan 200 (300 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually. Must meet haze and crystal originated pit (COP) requirements specified in the starting material section of the roadmap.

[G] Inspection tools must detect defects × 0.8 DR on metal films, and × 0.5 DR for non-metal and bare silicon.

[H] These values drives out of the overlay budget issues form the lithography TWG. The detection is limited by micro roughness of the backside surface

[I] Resolution of defect review is defined as 0.05 × Sensitivity at pattern inspection R&D

[J] Driver is redetection by SEM ADC instrument at a 5000× field of view.

[K] Assumptions: 5,000 wafer starts per week, defects per wafer based on surface preparation at FEOL, leading to defects per hour that need review, 100% ADC.

[L] Defect classifications need to meet: Repeatability 95 %, Accuracy 85%, Purity 80 %

[M] Defect classifications need to meet: Repeatability 95 %, Accuracy 80 %, Purity 80 %

YIELD LEARNING

Yield learning is defined as the collection and application of process and wafer knowledge to improve device yield through the identification and resolution of systematic and random manufacturing events. As seen from the yield learning technology requirements in Table 113, the key requirements for achieving historic yield ramps include the detection of ever shrinking yield-detracting defects of interest, timely identification of root causes with growing data volume, chip complexity and process complexity and improving the yield learning rate per each cycle of learning. With increasing process complexity and longer cycle times, tools and methods are needed to increase the number of yield learning cycles for each technology node. Also, with continuous move to smaller features and longer processes, 300 mm wafers and new materials (low κ, high κ, etc.), numerous tools and methods are required to understand all the yield detracting interactions. Use of SOI, SiGe and other new device structures and materials will further challenge yield learning.

Yield in most industries has been defined as the number of products that can be sold divided by the number of products that can be made. In the semiconductor industry, where silicon wafers act as batches for integrated circuits, the yield (Y_{total_i}) of a particular integrated circuit design product (i) can be expressed in terms of equation (1).

$$Y_{total_i} = (Y_{line}) * (Y_{batch_i}) \qquad (1)$$

Y_{line} in equation (1) denotes the line yield, wafer yield, or survival yield. It represents the fraction wafers that survive processing through the whole manufacturing line. Y_{batch_i} denotes batch yield, chip yield or die-sort yield, which represents the fraction of integrated circuits of a particular design (i) on each wafer that are completely functional at the end of the line.

Batch yield can be expressed in terms of equation (2).

$$Y_{batch_i} = (Y_{sys_i}) * (Y_{random_i}) \qquad (2)$$

Y_{sys_i} in equation (2) denotes the component of batch yield that results from systematic faults. Y_{random_i} denotes the component batch yield that results from randomly distributed faults. Y_{random_i} typically be expressed as a highly non-linear function of the random fault density and the critical area of an integrated circuit design—the area in a chip that is susceptible to random faults. Y_{random_i} is frequently expressed in terms of the negative binomial law.

Historically, the semiconductor industry has been driven by batch yield in general and its random component in particular. However, the semiconductor industry tends to operate in an environment of exponentially decaying product

prices, which put semiconductor manufacturers under time-to-market pressure. To a large degree, profitability is derived from an early and steep, yield ramp. The sooner a semiconductor manufacturer can generate high batch yield, the earlier the manufacturer can ramp to volume production, and the more profitable the semiconductor manufacturer's integrated circuit venture is likely to be. Improving the systematic component of batch yield, which frequently constrains batch yield in the early stages of manufacturing, can enhance profitability by enabling production at a point in time when chip prices are very high.[2] Yield learning in the early stages of manufacturing may thus differ significantly from yield learning in the later stages of manufacturing.

Also, yield learning in a foundry differs substantially from yield learning in a fabrication facility that produces a few high volume products. The high volume producer will be constrained by batch yield in the early stages of manufacturing. Line yield will be the limiting factor once batch yield is high and volume production has begun. By contrast, a foundry may introduce a plethora of low-volume products into a relatively mature process on a routine basis. On occasion, one lot of 300 mm wafers may provide a lifetime inventory of a particular design, which sells into a very short market window. A few chips of the design must exit the fab by a specific date. Under these circumstances, designing the circuit correctly the first time, fabricating flawless masks the first time, a rapid cycle time through the line and a high line yield may be more important than a high batch yield.

Another recent challenge is the process of rapid yield learning on 300 mm wafers. The 300 mm semiconductor manufacturing like all other wafer size transitions nodes has significant challenges set upon it to meet aggressive yield and cost goals. Most of these challenges are not new to 300 mm but are manifestations of old issues that occur with most new wafer size introductions. These challenges include: clean, defect-free substrates, substrate heat capacity, process uniformity, and new processing materials, all of which are just part of implementing a new substrate technology, and any of which can delay profitable yields for this node by months or years if not solved in planning or start-up phases of this transition.

On the positive side, generating higher yield in 300 mm manufacturing is the use of latest and greatest manufacturing tool sets. Tool sets that, for the most part have leveraged years of historical learning and improvement programs in their designs. Making them the most sophisticated tools ever built right from the start. Also benefiting the 300 mm activities are the better process designs and simulations that are occurring before any silicon ever reaches then manufacturing floor. Process simulation has proven to be a very cost effective and timely way to speed the rate of change. Also 300 mm manufacturing is universally being implemented with metrology needs being embedded as forethought and not an afterthought in manufacturing, as in the past. Finally, the physical "sweet" spot of a 300 mm wafer is greater than 2× that of a 200 mm wafer.

Working against higher initial yields in 300 mm manufacturing are the usual challenges that seem to pop-up in any substrate technology transition. Once again along with a substrate change come new materials specifically, low K films that everyone seems to want to implement in parallel with this new substrate. It is widely believed that the single largest issue on 300 mm is uniformity across the entire wafers surface area. Uniformity issues include the usual sources of film thickness, etch profiles, and dose control. Metrology monitoring capabilities to properly cover the vast surface area of a 300 mm wafer, and its ability to recognize when a non-uniform surface issues occur is also a huge challenge.

Yield Management in 300 mm factory is going to be more closely coupled to data management then in any previous factory or technology node currently in manufacturing. How data from all generating sources of the factory is collected, stored, compiled and accessed is going to be more vital then in any other manufacturing environment previously conceived. In advanced manufacturing any data generated could potentially hold the key to understanding and solving a yield issue that is identified at sort needs to be recorded in such a fashion as to be accessible by yield engineers if required. Accessing the raw data in such a way as to generate meaningful correlations and results is going to be a critical requirement in the 300 mm node. Data storage and consequently the user interfaces to access this data cannot be handled, as an afterthought if these factories are to be successful during the start up.

Different in the 300 mm world will be the sources of data. These sources will need to be greatly expanded as compared to the data sources used in 150 and 200 mm manufacturing. Specifically we are referring to the obvious in line metrology, electrical test and sort results but we are also including detailed process equipment information[3], FOUP wafer

---

[2] *See for example C. Weber, D. Jensen and E. D. Hirleman, "What drives defect detection technology?" Micro, June 1998, pp. 51-72.; C. Weber, "Yield Learning and the Sources of Profitability in Semiconductor Manufacturing and Process Development," Proc. IEEE/SEMI/ASMC, Boston, Mass., May 1, 2002, pp. 324-329.*

[3] *State of tool repair or maintenance at time of wafer processing, components or parts kits currently in use, operational states of sub systems including RF power, gas flows, vacuum pressures, etc. current particle results for system are only examples.*

position, factory environmental conditions and delivery service,[4] along with the more advanced process state conditions that are part of a fully implemented APC solution in the factory.

Implemented APC and FDC solutions in 300 mm will be more common than in any prior technology node. However, these control solutions will require tremendous data transport and data processing systems to support a full-scale implementation. Managing this, which must all be done in real time to benefit the factory, is a monumental undertaking. Maintaining standards and open access systems allowing the best internal and external solutions to work together is a must.

Down stream, or rather off line analysis, of all the factories data will also require new approaches, in addition to the existing ones, to fully grasp all information that can be correlated to yield. The greatest challenge to a comprehensive data management system required for yield learning is the ability to deal with and integrate data streams that are continuous, periodic, sporadic, and interval based such that they can all be linked through some common coupling system or user interface and be resolved by engineers. Keeping data aligned down to the wafer level or possibly the die level will require automated data matching techniques that are currently only done on an ad-hoc basis at an individuals desktop. For example the simple task of aligning all wafer surface information[5] through a universal coordinate system is a requirement to be effective in yield analysis yet even today this is not universally implemented in most companies. It is also critical to have all data sources open and accessible by multiple user interfaces in order to maximize the effectiveness of yield engineering resources in finding problems. The best of breed data systems going forward will allow internal as well as multiple third party software solutions (GUIs) to access the raw data formats giving engineers the greatest flexibility in identifying and solving yield limiting issues. Barriers such as these must be eliminated prior to going into manufacturing 300 mm wafers if companies are expected to address yield issues in the shortest amount of time.

The rapid identification of defect and fault sources through integrated data management continues to be the essence of rapid yield learning. Table 113 presents the technology requirements for the yield learning focus topic. Learning must proceed at an accelerated rate to maintain the yield ramp from introduction to maturity within the expected timeline despite the growth in circuit complexity and the larger amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. At future technology nodes, the time necessary to source manufacturing problems must at least remain constant, approximately 1× the process cycle time on average, during yield ramp. In the face of this increased complexity, strategies and software methods for integrated data management (IDM) have been identified as critical for maintaining productivity. IDM must comprehend integrated circuit design, visible and non-visual defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the IDM system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. IDM will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as automatic defect classification (ADC) and spatial signature analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information. The technology requirements for various types of defects are described below.

VISIBLE DEFECTS

Tools are needed to detect, review, classify, analyze, and source continuously shrinking visible defects.

NON-VISUAL DEFECTS

Defects that cause electrical failure but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-visual defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance or timing; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-visual defects) will become increasing challenging. Techniques

[4] Factory data includes the obvious temperature and humidity conditions both inside, outside and in all chemical storage and usage facilities, they also include data any chemical delivery system including the specific source and quality of the chemical currently in use.
[5] Wafer surface information includes film thickness metrology, CD and alignment metrology, defects, electrical test, electrical bit-map, etc.

need to be developed that rapidly isolate failures and partitions them into those caused by visible defects, non-visual defects, and parametric issues.

PARAMETRIC DEFECTS

As minimum feature size decreases, the systematic mechanism limited yield (SMLY or Ys) decreases as well. A major contributor to the Ys component of yield is parametric variation within a wafer and wafer-to-wafer. Parametric defects have traditionally been referred to as "non-visual defects." However, parametric defects require separation from the "non-visual defects" for rapid sourcing.

ELECTRICAL FAULTS

As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the number of transistors per unit area (cm^2) times the number of process steps, forming the defect sourcing complexity factor as shown in Table 113. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity. Moreover, the soft failures caused by sporadic cross-chip timing variation will require innovative new approaches to identify the root causes since these type of failures reside between a hard spot defect failure and consistent systematic failure issue.

DATA MANAGEMENT SYSTEMS

The current practice in data management system (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient IDM is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect and fault sourcing capabilities, methods must be established for integrating workflow information (such as WIP data) with the DMS, particularly in commercial DMS systems. This will be important when addressing issues of advanced process and tool control beyond simple tool shutdown, such as lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time-based data such as that generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time-based data such that it can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

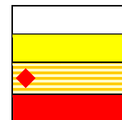
The purpose of the yield learning technologies requirements table is to provide a compact look at the impact of each new technology node on the ability to rapidly learn and correct yield impacting events that occur during device manufacturing. The concept of "Defect/Fault Sourcing Complexity" has been defined to describe both the instantaneous complexity at a technology node and the rate of increasing complexity of devices at future nodes. The defect sourcing complexity factor is the transistor density per unit area times the number of processing steps. It can be considered as an indicator of the "volume" of elements in a completed wafer that must be functional to arrive at a working device. For example, there are on the order of a billion elements per square centimeter, insinuating that one bad element in 1E9 can cause a failure. The "defect data volume" is an indicator of the number of data samples that are collected from a wafer during inspection and review. The value is a function of detection sensitivities at each technology node and the wafer size. The "data volume trend" is an indication of the increase in data volume across future nodes. This value can be related to the defect sourcing complexity in terms of a comparison of trends in each metric. For example, if the trend in complexity greatly surpasses the trend in data volume, then the process will not be sufficiently sampled and yield learning will be inhibited. The "Yield

Learning During Ramp" section of the table apply the concepts of sourcing complexity and data volume trends to indicate the time required to use this information to make yield correcting changes to the process. The overall goal is to provide manufacturers and suppliers with an understanding of the factors and technologies that are available, or will be required, to facilitate rapid yield learning at current and future technology nodes.

Table 113a Yield Learning Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Wafer Size (mm)	300	300	300	300	300	300	300
Number of Mask Levels	29	31	33	33	33	35	35
Number of Processing Steps	516	530	543	556	570	583	596
Cycle Time During Ramp (number of days)	43.5	46.5	49.5	49.5	49.5	52.5	52.5
Defect/Fault Sourcing Complexity [A] [G]							
Logic transistor density/cm^2 (1E6)	61	77	97	122	154	194	245
Defect sourcing complexity factor (1E9) [B]	31	41	53	68	88	113	146
Defect sourcing complexity trend [C]	1	1	2	2	3	4	5
Data Analysis for Rapid Defect/Fault Sourcing							
Patterned wafer inspection sensitivity (nm) during yield ramp	80	72	64	56	52	46	40
Average number of inspections/wafer during full flow	2.9	3.1	3.3	3.3	3.3	3.5	3.5
Defect data volume (DV) (number of data items/wafer) (1E13) [D]	4.7	7.2	9.7	12.7	14.6	18.7	21.6
Defect data volume (DV) trend [E]	1.0	1.5	2.1	2.7	3.1	4.0	4.6
Yield Learning During Ramp from 30% to 80% Sort Yield [F]							
Number of yield learning cycles/year based on full flow cycle time	8.4	7.8	7.4	7.4	7.4	7.0	7.0
Required yield improvement rate per learning cycle	6.0	6.4	6.8	6.8	6.8	7.2	7.2
Time to identify and fix new defect/fault source during ramp	43.5	46.5	49.5	49.5	49.5	52.5	52.5
Number of learning cycles/year for 4 defect/fault source/year [I]	4.4	3.8	3.4	3.4	3.4	3.0	3.0
Required yield improvement rate/learning cycle for 4 defect/fault sources/year [I]	11.4	13.0	14.8	14.8	14.8	16.9	16.9

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



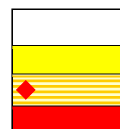
Notes for Tables 113a and 113b:
[A] Defect/fault sourcing means identifying the point of occurrence (identify process tool, design, test or process integration issue causing a visible or non-visual defect, parametric problem or electrical fault).
[B] Defect sourcing complexity factor = (logic transistor density #/cm^2)×(# processing steps).
[C] Defect sourcing complexity trend is normalized to 100 nm technology node.
[D] Defect data volume (DV) = (# of inspection/wafer in process flow)(wafer area)/patterned wafer sensitivity during ramp Assumes 10% of wafers are inspected on average at each mask step during ramp.
[E] DV trend is normalized to 100 nm technology node.
[F] Assumes cycle time of 1.5 days per mask level. Also, assumes linear reduction in yield learning time based on time to identify and fix each defect/fault source.
[G] Rapid defect sourcing and yield learning assumptions as follows:

- *Keep yield ramp constant (30% intro yield to 80% mature yield) for successive technology nodes.*
- *Keep time to source new yield detractors to 1× process cycle time.*
- *New material introduction should not increase defect/fault sourcing time.*
- *Focus defect/fault sourcing on ramp portion of yield learning curve.*

Table 113b Yield Learning Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Wafer Size (mm)	**450**	**450**	**450**	**450**	**450**	**450**
Number of Mask Levels	**35**	**35**	**35**	**37**	**39**	**39**
Number of Processing Steps	**610**	**636**	**650**	**676**	**690**	**716**
Cycle time During Ramp (number of days)	**52.5**	**52.5**	**52.5**	**55.5**	**58.5**	**58.5**
Defect/Fault Sourcing Complexity [A] [G]						
Logic transistor density/cm^2 (1E6)	**309**	**490**	**617**	**980**	**1235**	**1960**
Defect sourcing complexity factor (1E9) [B]	**188**	**312**	**401**	**662**	**852**	**1403**
Defect sourcing complexity trend [C]	**6**	**10**	**13**	**21**	**27**	**45**
Data Analysis for Rapid Defect/Fault Sourcing						
Patterned wafer inspection sensitivity (nm) during yield ramp	**36**	**TBD**	**26**	**TBD**	**17.6**	**TBD**
Average number of inspections/wafer during full flow	**3.5**	**3.5**	**3.5**	**3.7**	**3.9**	**3.9**
Number of data items/wafer (1E13) [D]	**28.7**	**TBD**	**60.4**	**TBD**	**135.6**	**TBD**
Defect data volume (DV) trend [E]	**6.1**	**TBD**	**12.9**	**TBD**	**28.9**	**TBD**
Yield Learning During Ramp from 30% to 80% Sort Yield [F]						
Number of yield learning cycles/year based on full flow cycle time	**7.0**	**TBD**	**7.0**	**TBD**	**6.2**	**TBD**
Required yield improvement rate per learning cycle	**7.2**	**TBD**	**7.2**	**TBD**	**8.0**	**TBD**
Time to identify and fix new defect/fault source during ramp	**52.5**	**TBD**	**52.5**	**TBD**	**58.5**	**TBD**
Number of learning cycles/year for 4 defect/fault sources/year [I]	**3.0**	**TBD**	**3.0**	**TBD**	**2.2**	**TBD**
Required yield improvement rate/learning cycle for 4 defect/fault sources/year [I]	**16.9**	**TBD**	**16.9**	**TBD**	**22.3**	**TBD**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table 114.

Wafer environment control—There is definitive consensus that as device geometries approach 90 nm and beyond, wafer isolation will prove to be an enabling technology. The percentage of process steps affected by non-particulate or molecular contamination is expected to increase. The use of copper and other novel materials in the process introduces other potential contaminants. Because of these trends, wafer isolation technology, integrated tool mini-environments and closed carriers (e.g., Front Opening Unified Pods (FOUPs)) are needed. FOUPs will also facilitate factory automation for wafer handling. The wafer environment contamination control (WECC) technology requirements indicate target levels of ambient acids, bases, condensables, dopants, and metals for specific process steps. Other exposure times and sticking coefficients may be scaled linearly.

Airborne Molecular Contamination—Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of Airborne Molecular Contamination (AMC). Oxygen and water vapor as well as low

concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden. Acid vapors in the air have been linked with the release of boron from HEPA filters and the impact of amines on DUV photoresists are well known examples of AMC affecting wafer processing. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation in the cleanroom to measure AMC at the part per trillion level. SAW devices and APIMS have been used to measure low level AMC, but low cost, routine monitoring may be required as devices approach molecular dimensions. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front-end processes. Although numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures, the need for nitrogen purging of wafer environment enclosures is being investigated for critical process steps. Not all process steps will be impacted by AMC. For example, future lithography systems will require vacuum processing and are not expected to impose new AMC control requirements in the cleanroom environment. The potential for AMC to impact new processes should be considered in all process integration studies.

Process critical materials—Little understanding exists today regarding impurity specifications in novel materials such as Cu plating solutions, CMP slurries, Chemical Vapor Deposition (CVD) precursors, and high/low-κ materials and additional experimental investigation is required. Particle levels per volume have been held constant at critical particle size. Assuming a $1/x^3$ power law relationship, this means a cleanliness increase of approximately 2× per generation. Measurement of particles at the critical size is desirable, but monitoring of larger size particles is likely with critical particle size concentrations inferred from assumed particle size distributions.

Ultrapure Water—Ultrapure water (UPW) is generally considered to be 18.2 MegΩ-cm resistivity at 25 °C and below 1 PPB in ionics (cations, anions, metals), total oxidizable carbon and silica (dissolved and colloidal). Particle levels are reduced as far as practical using the best available utrafiltration technology. Bacteria are present, on surfaces and to a lesser degree in the bulk fluid, and controlled to very low levels. The 2003 Roadmap values, presented in Table 114, represent typical UPW quality currently in use to manufacture the most advanced semiconductor devices. More stringent criteria beyond 2003 are only projected where manufacturing process requirements are expected to demand improvements. A discussion of the UPW requirements can be found in the *supplemental material*.

An important trend in UPW is the consideration of some parameters as process variables rather than contaminants, looking at stability more than absolute levels. Some semiconductor manufactures now treat *dissolved oxygen (DO)* in this way, while others still consider it a contaminant. Stability of temperature and pressure continue to be important.

Contaminant quality levels in UPW must be viewed in the context of where that quality is required and where it is to be measured. Points of measurement are referred to as the point of distribution (POD), point of connection (POC), and point of use (POU). The POD is just after the last treatment step of the UPW system, the POC is at the tool connection point, and the POU is in the tool. The 2003 Roadmap defines UPW quality at the POC. UPW quality, perhaps more than any other critical fluid, can change between these three locations, especially between the POC and POU, and requires particular attention to maintain quality throughout. In addition sampling techniques are critical to ensure accurate analytical results. As UPW specifications shift from the POC to the POU, sampling methods will become more difficult and costly. POU sampling has been limited to pulling batch samples from rinse tanks or hand spray nozzles. Sampling method development will be needed to collect accurate analytical results from spray processors, especially for on-line analytical testing methods. Some companies are investigating extending the use of well-established wafer surface contamination test methods to bulk UPW analysis. Standard test parameters, such as contact method, contact time etc. need to be developed to ensure reproducible results.

UPW Recycle—To promote resource optimization UPW use efficiency improvements are typically required. Cost effective technologies, including treatment and analytical methods, are needed to ensure UPW quality is maintained, as more waters are recycled back through the system. A well-implemented recycle program has been shown to improve final water quality by using a "cleaner" stream for the feed, in addition to providing other benefits.

UPW Measurement Methodologies—Recent advances have been made in both on-line particle counting and viable bacteria measurement. Particle counters are now capable of measuring to 30 nm in UPW. By extrapolating or assuming particle size distributions it is possible to infer particle concentrations below 30 nm. Bioluminescent bacteria measurement techniques are now available which reduces analytical time. General test methodologies for monitoring contaminants in UPW are indicated in Figure 76. A more complete treatment of UPW concerns is covered in the *supplemental material of this chapter.*

Parameter	Measured (POD/POC)	Test Method
Resistivity	Online	Electric cell
Viable bacteria	Lab	Incubation
TOC	Online	Resistivity / CO_2
Reactive silica	Online or lab	Colormetric
Dissolved N_2	Online	Electric cell
Total silica	Lab	ICP/MS or GFAA
Particle monitoring	Online	Light scatter
Particle count	Lab	SEM—capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP/MS
Dissolved O_2	Online	Electric cell

Figure 76 General Test Methodology for Ultrapure Water

Gases and Liquid Chemicals—The recommended minimum contaminant values in Table 114 represent typical gas/liquid chemical quality in use in 2003 to manufacturer the most advanced devices and are generally higher that in previous versions of the ITRS. In many applications, the requirements for the contaminants in these gases and/or liquid chemicals may be relaxed even further. Alternatively, some manufacturers have claimed benefits from lower contaminant levels. It may be that benefits attributed to low contaminant levels are actually more attributable to the reduction in contaminant variations achieved with high purity process gases and chemicals. Currently achievable purity levels for gases and chemicals used in semiconductor manufacturing are expected to be sufficient for multiple generations, with yield improvements being achieved more by reducing variations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials

Liquid chemicals—Tables 114a and 114b summarize the purity requirements for liquid chemicals delivered to process tools. Pre-diffusion cleaning requirements drive the most aggressive impurity levels. The ionic purity levels of liquid chemicals are expected to remain constant through 2016. Liquid particle level targets are shown to become purer each technology node. Particle counters currently are capable of measuring only to 65 nm for liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes. With the increased use of CMP and plating chemicals there must be a better understanding of purity requirements for the delivered chemicals.

Bulk/specialty gases—The major bulk gases have been listed separately in Table 114 for the 2003 roadmap. As indicated above, the recommended values are relaxed from previous versions of the roadmap. Although no specific information is available that would indicate that the requirements for these gases will need to be improved for future nodes in the roadmap, the table does anticipate that improvements may well be required at the 45 nm node. As indicated in the table, total hydrocarbons (THC) are often specified in the Bulk Gases. Methane has a naturally occurring concentration of about 2 ppm in air and is the most likely hydrocarbon impurity to be present in inert gases derived from air. The analytical technique generally used to quantify methane is a GC-FID. The FID (flame ionization detector) is sensitive to the C-H bond and can be viewed as a C atom counter for hydrocarbons. If the FID is used without a GC column for separating impurities, one can use it as a real time detector for total hydrocarbons. However, calibration of the FID is an issue, since the response to different hydrocarbons will be different (The response will be proportional to the number of CH bonds in the hydrocarbon.) Typically the FID is calibrated using a methane standard and the THC results are given as “THC as methane.” For most applications this serves the purpose of providing an indicator of the amount of total hydrocarbons that are present. Although it may not give an accurate quantification of the hydrocarbons, it can nonetheless be used as a real time relative monitor for the amount of hydrocarbons.

The concept of measuring methane and non-methane hydrocarbons (NMHC) has migrated from the environmental industry to the semiconductor industry. This method uses a GC column for separation and measurement of the methane concentration using a FID. After the methane measurement the GC effluent is back-flushed into the FID to detect the other hydrocarbons. This approach also has the same problem with quantification of NMHCs. The FID response to CH_4 is used to quantify NMHC. Although it is not explicitly stated, the NMHCs are usually quantified as methane. For some advanced lithography processes, very small quantities of "heavy" (e.g., C_6-C_{30}) hydrocarbons are detrimental because of increased adherence to the exposed surfaces. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities.

The only approach to accurately quantifying hydrocarbons is to detect each hydrocarbon separately and use standards to quantify the instrument response to each hydrocarbon. This can be done using a TD GC/MS, although this instrument requires significant analytical expertise and is time consuming. Even this approach may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks. Using an atmospheric pressure ionization mass spectrometer (APIMS) to provide real time measurement of individual hydrocarbons is possible, in principle, but calibration is difficult, because larger hydrocarbons are collisionally dissociated in the ionization process. The $CH4^+$ peak or another peak (depending upon ionization conditions) can provide a measure of the total hydrocarbon content if care is taken in calibration. The response to larger hydrocarbons will depend on the nature of the molecule and the analysis conditions, so calibration is not straightforward. Even in this approach the quantification of THCs will typically be reported in terms of a single hydrocarbon (i.e., methane). As a practical matter, for levels above 100 ppb, the straightforward FID THC measurement is recommended. For lower levels, APIMS will give satisfactory results to 10 ppt. If heavy hydrocarbons are a particular concern, direct calibration of the instrument with a mixture containing the hydrocarbons of interest is recommended.

Applications for both O_2 and Ar generally tolerate higher levels of N_2 contamination than other contaminants and the table reflects this observation. New requirements for "critical" clean dry air (CDA); lithography purge gases and supercritical CO_2 supply have been added to the table for 2003. The current purity levels for these gases also appear to be adequate for several more nodes in the roadmap.

For specialty gases, values for contaminants for etchants, dopants, and deposition gases have been included in the table. Values for particulate contamination in the specialty gases have been eliminated from the table for 2003, since on-line monitoring of particle concentrations is not commonly practiced and data verifying the efficacy of point of use particle filters is well established. No experimental information is available that suggests there is a need for improvement in the purity of specialty gases during the time span of the Roadmap. For both bulk and specialty gases, consistency of product purity is likely to be more important than further improvements in purity levels. Contaminant levels are not practical process control parameters, so consistent gas quality is currently maintained by quality assurance procedures. There is a need for statistical process control methods that correlate with product contamination.

Novel materials—Impurity specifications for novel materials used in processing will be increasingly important. Specifications for critical materials such as novel metal oxides, CMP slurries, low/high dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied. Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements.

Design-to-process interactions—Data, test structures and methods are needed to identify and control yield-detracting contaminants in the wafer environment, airborne and process critical materials and ultra pure water. The need for standard test structures is critical in determining defect sources and mechanisms. Once the design process interactions are understood, device design ground rules may be established and communicated that decrease process sensitivity. Cycles of process sensitivity analysis and reduction will be critical to advancing device design and yield. Additionally, sensitivities of designs to various levels of random defects need to be considered in the design process.

Process-to-process interactions—Interactions that result in defect formation (such as thickness of photoresist and contact density can affect the level of residue inside a via/contact) between process steps may drive particular requirements to a tool or process upstream or downstream that are not necessarily germane to that tool or process. Cluster tools and wet sinks are two examples of tools that must be carefully designed to ensure that their modules do not transfer any contaminants that degrade the performance of adjacent modules. To detect, to understand, and to eliminate unwanted process interactions, process monitoring and control will play a key role. The appropriate sensors and data must be available, along with an appropriate information management system to correlate process parameters to upstream/downstream parameters and yield and provide smart, inter-tool and intra-tool statistical process control (SPC).

Table 114a Technology Requirements for Wafer Environmental Contamination Control—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Wafer Environment Control							
Critical particle size (nm) [A]	**50**	**45**	**40**	**35**	**33**	**29**	**25**
Number of particles > critical size (/m^3) [B]	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**	**ISO CL 2**
Airborne Molecular Contaminants in gas phase (pptM)) [C] [H] [R]							
Lithography—bases (as amine, amide, and NH_3)	**750**	**750**	**750**	**<750**	**<750**	**<750**	**<750**
Gate—metals (as Cu, $E=2\times10^{-5}$) [I]	**0.15**	**0.1**	**0.1**	**0.07**	**<0.07**	**<0.07**	**<0.07**
Gate—organics (as molecular weight to 250, $E=1\times10^{-3}$) [D]	**80**	**70**	**60**	**60**	**50**	**50**	**50**
Organics (molecular weight to C_7H_{16}) normalized to hexadecane ($C_{16}H_{34}$) equivalent	**5000**	**4500**	**4000**	**3500**	**3000**	**3000**	**<2500**
Salicidation contact—acids (as Cl–, $E=1\times10^{-5}$)	**10**	**10**	**10**	**<10**	**<10**	**<10**	**<10**
Salicidation contact—bases (as NH_3, $E=1\times10^{-6}$)	**12**	**10**	**8**	**4**	**<4**	**<4**	**<4**
Dopants [E]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Airborne Molecular Contaminants, Surface Deposition Limits (for Si Witness Wafer, 24-hour Exposure to Closed FOUP, Pod, Mini-environment or Air)							
SMC organics on wafers, ASTM 1982–99, ng/cm^2 [0]	**4**	**2**	**2**	**2**	**2**	**2**	**2**
Front-end processes, bare Si, total dopants added to 24-hour witness wafer, atoms/cm^2 [E] [P]	**<2E12**	**<2E12**	**<2E12**	**1.E+12**	**1.E+12**	**1.E+12**	**1.E+12**
Front-end processes, bare Si, total metals added to witness wafer, atoms/cm^2 [G] [Q]	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<2E10**	**<1E10**
Process Critical Materials [H]							
Critical particle size (nm) [A]	**50**	**45**	**40**	**35**	**33**	**29**	**25**

SMC—surface molecular condensable

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

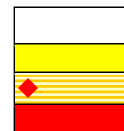


Table 114a Technology Requirements for Wafer Environmental Contamination Control—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Ultrapure Water [N]							
Resistivity at 25 °C (MOhm-cm)	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**
Total oxidizable carbon (ppb)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Bacteria (CFU/liter)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Total silica (ppb) as SiO_2	**1**	**1**	**0.75**	**0.75**	**0.5**	**0.5**	**0.5**
Reactive silica (ppb) as SiO_2	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Number of particles > critical size (/ml) [A]	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Dissolved oxygen (ppb) (contaminant based) [S]	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Dissolved oxygen (% value) (process variable based) [S]	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**
Dissolved nitrogen (ppm) [K]	**8–12**	**8–12**	**8–12**	**8–12**	**8–12**	**8–12**	**8–12**
Critical metals (ppt, each) [G]	**1**	**1**	**1**	**<0.5**	**<0.5**	**<0.5**	**<0.5**
Critical anions (ppt each) [G]	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Boron (ppt, each) [N]	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Temperature stability (°C)	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**
Liquid Chemicals [F]							
49% HF, 37% HCl: number of particles > critical size (/ml) [A] [L]	**—**	**—**	**<10**	**<10**	**<10**	**<10**	**<10**
30% H_2O_2, 29% NH_4OH, 100% IPA: number of particles > critical size (/ml) [A] [L]	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
49% HF, 30% H_2O_2, 29% NH_4OH, 100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Pt, Ca, Al, Zn (ppt, each)	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**
49% HF, 30% H_2O_2, 29% NH_4OH, 100% IPA: all other metals not listed in row above (ppt, each)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
49% HF: total oxidizable carbon (ppb)	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
29% NH_4OH: total oxidizable carbon (ppb)	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: total oxidizable carbon (ppb)	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30% H_2O_2: total oxidizable carbon (ppb)	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl, 96% H_2SO_4: K, Ni, Cu, Cr, Co, Pt (ppt)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
37% HCl, 96% H_2SO_4: other cations and metals (ppt)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

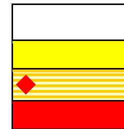


Table 114a Technology Requirements for Wafer Environmental Contamination Control—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Liquid Chemicals [F]							
BEOL solvents, strippers K, Li, Na, (ppt, each)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**
Planar slurries: scratching particles (/ml > key particle size) [J] [T]	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Planar rinse chemicals: particles>critical size (/ml) [A] [L] [T]	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Planar rinse chemicals: elements TBD (ppt, each) [T]	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [A] [L] [T]	**—**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., TEOS)							
Metals (ppb)	**<1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
H_2O (ppmV)	**<10**	**<5**	**<5**	**<5**	**<1**	**<1**	**<1**
Bulk Gases (Contaminants, ppbv)							
N_2 (O_2, H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
O_2 (N_2X_5, ArX_5, H_2, H_2O, CO, CO_2, THC) [U]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
H_2 (N_2X_5, O_2, ArX_5, H_2O, CO, CO_2, THC) [U]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
He (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
CO_2 (N_2, H_2O, O_2, THC)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Critical clean dry air (e.g., lithography) (H_2O, THC) (SOx, NOx, amines all X0.05)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
Lithography purge for 193 nm (O_2 and H_2O X1000, CO, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Lithography purge for 157 nm (CO, CO_2, THC)	**N/A**	**N/A**	**N/A**	**<0.01**	**<0.01**	**<0.01**	**<0.01**
Lithography purge for 157 nm (O_2, H_2O)	**N/A**	**N/A**	**N/A**	**<1000**	**<1000**	**<1000**	**<1000**
Number of particles > critical size (/M^3) [A]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

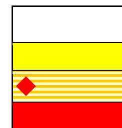
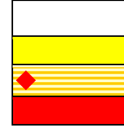


Table 114a Technology Requirements for Wafer Environmental Contamination Control—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Specialty Gases							
Etchants (Corrosive, e.g., BCl_3, Cl_2)							
O_2, H_2O (ppbv)	**<1000**	**<1000**	**<1000**	**<500**	**<500**	**<500**	**<100**
Critical specified metals/total metals (ppbw) [V]	**<10/1000**	**<10/1000**	**<10/1000**	**<10/1000**	**<10/1000**	**<1/TBD**	**<1/TBD**
Etchants (Non-corrosive, e.g., C_2F_6, NF_3)							
O_2, H_2O (ppbv)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Deposition (e.g., SiH_4, NH_3, $(CH_3)_3SiH$)							
O_2, H_2O (ppbv)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Critical specified metals/total metals (ppbw) [V]	**<10/1000**	**<10/1000**	**<10/1000**	**<10/1000**	**<10/1000**	**<1/TBD**	**<1/TBD**
Dopants (e.g., AsH_3, PH_3, GeH_4)							
O_2, H_2O (ppbv)	**<1000**	**<1000**	**<1000**	**<500**	**<500**	**<500**	**<100**
Inerts—Oxide/Photoresist Etchants/Strippers							
Inerts (O_2, H_2O, ppbv)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
He, H_2 cylinder carrier/purge gases (N_2, H_2O, ppbv)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 114a and 114b:

*[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles. Because of instrumentation limitations, particle densities at the critical dimension for nodes < 90 nm will need to be estimated from measured densities of larger particles and an assumed particle size distribution. Although the particle size distribution will depend on the fluid (e.g. water, clean room air, gases), f(x)=K*1/X 2.2 is a reasonable approximation for the fluids of interest.* [6, 7]

[B] Airborne particle requirements are based on ISO 14644-1. [8]

[C] Ion/species indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography projections is defined by lithography roadmap. Gate metals and organics scale as defined in the surface preparation roadmap for metallics and organics. All airborne molecular contaminants are calculated as S=E(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1), N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second).*

[D] The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general, molecular weights < 250 are not considered detrimental due to the higher volatility of these compounds.

[E] Includes P, B, As, Sb

[F] Contaminant targets apply at POC (point-of-connection at process tool), not incoming chemical or POU (point-of-use in bath at wafer).

[G] Critical metals and ions may include: Ca, Co, Cu, Cr, Fe, Mo, Mn, Na, Ni, W.

For UPW: Note that the level of 1 ppt if applied to all ions, would be very problematic as the process probably does not need it, the purification systems unable to produce it, and the analytical techniques unable to measure it. For many elements an order of magnitude higher or more would be appropriate. Only those ions that are the most critical to the specific process should be considered at this level. Measurement at these levels is limited to a few advanced labs, so validation may be difficult. With that stated, the need to go to these low levels for some ions is real.

---

[6] *Cooper, D. W., "Comparing Three Environmental Particle Size Distributions", Journal of the IES, Jan/Feb 1991, pages 21-24.*

[7] *Pui, D. Y. H. and Liu, B. Y. H., "Advances in Instrumentation for Atmospheric Aerosol Measurement", TSI Journal of Particle Instrumentation, Vol. 4, Number 2, Jul-Dec 1989, pages 3-2.*

[8] *ISO 14644-1 Cleanrooms and Associated Controlled Environments—Part 1: Classification of Air Cleanliness.*

Three different case studies were reviewed where the levels of Ca, Fe, and Ni in the UPW resulted in levels of problem densities (atoms/sq cm) on the wafer. These were reduced to acceptable levels by reducing the level of these elements in the UPW to levels well below 10 ppt. In only one case does the data exist that showed success by obtaining values below 0.5 ppt. In the other two, the problem existed at some level below 10 PPT (detection limit in UPW at the time). When additional ion exchange was added the problem went away. It is very reasonable to assume that the ion exchange reduced the level by an order of magnitude. These results drive the 1.0 ~ 0.5 ppt values.

[H] Units on all contaminants in Table 114 are often given as ppb (or ppm or ppt, we use ppb here solely for demonstration purposes). The reader should be aware that these units of parts per billion (ppb) may be ppb by mass, volume, or molar ratios. Where not designated, the following guidelines apply: Chemicals and UPW are typically ppb by mass, gases and clean room are typically ppb by volume. In the case of the fluid acting as an ideal gas, ppb by volume is equal to ppb molar. The notable exception to the above is metals in gases that are ppb by mass.

[I] Detection of metals at the levels indicated will be dependent on sampling time and flow rate.

[J] Key particle size for scratching particles depends on mean particle size of slurry. Target level will be specific to slurry and wafer geometry sensitivity.

[K] The dissolved nitrogen range is solely for the physical process needs of megasonics cleaning. Processes without megasonics cleaning can ignore the line item. The level is process specific and needs to be determined by the end user. Other gases can be used and they may have different levels that could be optimum. Also any process enhancements, thru chemistry associated with the other gases are outside of the scope of this chapter. Caution must also be exercised in gas addition with regard to bubble formation, particularly in that the solubility of the gases in hot UPW is lower at higher temperature.

[L] As of the 2003 update the finest sensitivity liquid particle sensor for chemicals is 0.065 µm. Values obtained by these particle counters are not directly comparable to the roadmap values and need to be normalized to critical particle size values in the roadmap using the equation and methods of Note an above.

[M] The values stated for UPW are taken at the POC. The goal is to carry these values to the POU but measurement there is difficult to impossible. Many values are not expected to change from the POC to the POU. On the other hand, some, such as dissolved O_2 (particularly if the UPW is carried in PFA tubing) will certainly change. Others, such as particles and bacteria may change based on the expertise of the tool manufacturer in maintaining water quality. The UPW dissolved oxygen target is held flat for future years; lower levels may be required for certain applications —refer to FEP Surface Preparation table footnote referring to surface oxygen for more details.

[N] Boron levels in UPW are an ongoing topic of discussion. For now, the best information available is that only high resistivity device structures (e.g. such as used in Flash memory) may warrant the value in the table. For other devices (logic, DRAM) an order of magnitude higher Boron levels may be acceptable.

[O] Single wafer shall be oxidized to make organic-free, then wafer shall be exposed for 24 hours and top side analyzed by TD-GC-MS with 400°C thermal desorption, and quantitation based on hexadecane external standard. TIC response factor per ASTM 1982–99.[9] Limits determined by above method are a guideline for many organics. Note higher limits can be used for process wafers oxidized or cleaned prior to subsequent process step. Processes such as gate oxide formation, or polysilicon deposition, may be more sensitive to organics, especially high boilers such as DOP. Silicon nitride nucleation may also be more sensitive than above for some processes. Please note dopants requirement is covered in earlier section

[P] Single wafer is first stripped with HF to yield dopant-free surface and than exposed for 24 hours. Topside of wafer is analyzed by methods known to give reliable recovery of boron. This is a guideline for dopants based on sampling in operating running fabs. Lower specifications may be required for key FEPs, especially for smaller geometries, lower thermal budgets, and for lightly-doped devices. If wafers are stripped with HF or BOE immediately prior to next thermal process, then steps may become less sensitive to surface molecular dopants, and higher limits apply. Note that BEPs tend to be orders of magnitude less sensitive to dopants than FEPs.

[Q] Single wafer known to meet the ITRS FEP spec of 1E10 atoms/cm^2, from the Starting Materials table, is exposed to a clean environment for 24 hours. Subsequent analysis of top surface by VPD-ICP-MS or VPD-GFAA. Lower specifications may be required for key FEPs, especially for smaller geometries. If wafers are cleaned prior to the next thermal process, then air exposure during earlier steps may be less of an issue. Note that majority of environmental metallic contaminants are particles, not molecular. If total particles on wafers are kept in spec than majority of metals, most metals from the environment should be within specifications. Back-end processes (BEPs) tend to be less sensitive to metals that FEPs provided not particles. Specs of twice the incoming wafer specs are readily achievable and readily measurable in case of wafers exposed for 24 hours.

[R] A 24-hour exposure will accentuate the contamination per wafer as wafers are often exposed too much shorter times in actual processing. The above SMC (surface molecular contamination) limits are preliminary, and no single value applies to all process steps or types of organics, dopants or metals. The SMC limits can vary substantially from process to process, and local air purification or purges may be needed to control contaminant levels.

[S] Dissolved oxygen (DO) should be considered as a contaminant and driven low or as a process variable and controlled. It is not needed to try and actively control the exact level of DO when it is at or near the "contaminant" level in the table.

[T] Uncertain at this time what target levels might be set given the variety of chemistries used in the industry and unknown sensitivity of the wafer to particles or ionic contamination in the chemical. This parameter is identified as a potentially critical one that should be considered and work is ongoing to define the correct levels.

[U] 5× after Ar and N_2 indicates that the values for these impurities are five times the value indicated in the row for the other impurities. This convention is used throughout the table for gases.

[V] The list of critical metals (e.g., Al, Ca, Cu, Fe, Mg, Ni, K, Si, Na) varies from process to process depending on the impact on electrical parameters such as gate oxide integrity or minority carrier lifetime as well as mobility of the metal in the substrate. The metals listed in note [G] for liquid process chemicals are of concern but the issues around metals in specialty gases are primarily around the potential for corrosion to add metal particles to the gas flow (e.g., Fe, Ni Co, P). The potential for volatile species containing metals must be considered for each specialty gas but are generally not present in the bulk gases.

---

[9] *ASTMF 1982–99e1, "Standard Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography," ASTM International.*

Table 114b Technology Requirements for Wafer Environmental Contamination Control—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Wafer Environment Control						
Critical particle size (nm) [A]	**23**	**18**	**16**	**13**	**11**	**9**
Number of particles > critical size (/m^3) [B]	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**	**ISO CL1**
Airborne Molecular Contaminants in gas phase (pptM)) [C] [I] [S]						
Lithography—bases (as amine, amide, and NH_3)	**<250**	**<250**	**<250**	**<250**	**<250**	**<250**
Gate—metals (as Cu, $E=2\times10^{-5}$) [J]	**<0.07**	**<0.07**	**<0.07**	**<0.07**	**<0.07**	**<0.07**
Gate—organics (as molecular weight 250, $E=1\times10^{-3}$ [D]	**40**	**40**	**30**	**30**	**20**	**20**
Organics (molecular weight C_7H_{16}) normalized to hexadecane ($C_{16}H_{34}$) equivalent	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**	**<2500**
Salicidation contact—acids (as Cl–, $E=1\times10^{-5}$)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Salicidation contact—bases (as NH_3, $E=1\times10^{-6}$)	**<4**	**<4**	**<4**	**<4**	**<4**	**<4**
Dopants (P or B) [E]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
Airborne Molecular Contaminants, Surface Deposition Limits (for Si Witness Wafer, 24-hour Exposure to Closed FOUP, Pod, Mini-environment, or Air)						
SMC organics on wafers, ASTM 1982-99, ng/cm^2 [P]	**1**	**1**	**1**	**1**	**1**	**1**
Front-end processes, bare Si, total dopants added to 24 hour witness wafer, atoms/cm^2 [E] [Q]	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**	**1.00E+12**
Front-end processes, bare Si, total metals added to witness wafer, atoms/cm^2 [G] [R]	**<1.00E+10**	**<1.00E+10**	**<1.00E+10**	**<1.00E+10**	**<1.00E+10**	**<1.00E+10**
Process Critical Materials						
Critical particle size (nm) [A]	**23**	**18**	**16**	**13**	**11**	**9**
Ultrapure Water [N]						
Resistivity at 25 °C (MOhm-cm)	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**	**18.2**
Total oxidizable carbon (ppb)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Bacteria (CFU/liter)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Total silica (ppb) as SiO_2	**0.01**	**0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**
Reactive silica (ppb) as SiO_2	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Number of particles > critical size (/ml)	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Dissolved oxygen (ppb) (contaminant based) [T]	**3**	**3**	**3**	**3**	**3**	**3**
Dissolved oxygen (% value) (process variable based) [T]	**+/- 10**	**+/- 10**	**+/- 10**	**+/- 10**	**+/- 10**	**+/- 10**
Dissolved nitrogen (ppm) [L]	**8–12**	**8–12**	**8–12**	**8–12**	**8–12**	**8–12**
Critical metals (ppt, each) [G]	**<0.5**	**<0.5**	**<0.5**	**<0.5**	**<0.5**	**<0.5**
Critical anions (ppt each) [G]	**50**	**50**	**50**	**50**	**50**	**50**
Boron (ppt, each) [O]	**50**	**50**	**50**	**50**	**50**	**50**
Temperature Stability (°C)	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**

SMC—surface molecular condensable

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

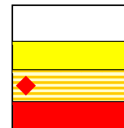


Table 114b Technology Requirements for Wafer Environmental Contamination Control—Long-term (continued)

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Liquid Chemicals [F]						
49% HF, 37% HCl: number of particles > critical size (/ml) [A] [M]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
30% H_2O_2, 29% NH_4OH, 100% IPA: number of particles > critical size (/ml) [A] [M]	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
49% HF, 30% H_2O_2, 29% NH_4OH, 100% IPA: Na, K, Fe, Ni, Cu, Cr, Co, Pt, Ca, Al, Zn (ppt, each)	**<150**	**<150**	**<150**	**<150**	**<150**	**<150**
49% HF, 30% H_2O_2, 29% NH_4OH, 100% IPA: all other metals not listed in row above (ppt, each)	**<500**	**<500**	**<500**	**<500**	**<500**	**<500**
49% HF: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
29% NH_4OH: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
30% H_2O_2: total oxidizable carbon (ppb)	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
37% HCl, 96% H_2SO_4: K, Ni, Cu, Cr, Co, Pt (ppt)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
37% HCl, 96% H_2SO_4: other cations and metals (ppt)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**
BEOL solvents, strippers K, Li, Na, (ppt, each)	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**	**<10000**
Planar slurries: scratching particles (/ml > key particle size) [K] [U]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Planar rinse chemicals: particles > critical size (/ml) [A] [M] [U]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Planar rinse chemicals: elements TBD (ppt, each) [U]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Plating chemicals: particles > critical size (/ml) [A] [M] [U]	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
ILD CVD Precursors (e.g., TEOS)						
Metals (ppb)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
H_2O (ppmV)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Bulk Gases (Contaminants, ppbv)						
N_2 (O_2, H_2, H_2O, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
O_2 (N_2X_5, ArX_5, H_2, H_2O, CO, CO_2, THC) [V]	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
Ar (N_2, O_2, H_2, H_2O, CO, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
H_2 (N_2, O_2, Ar, H_2O, CO, CO_2, THC)	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**
He (N_2X_5, O_2, ArX_5, H_2, H_2O, CO, CO_2, THC) [V]	**<5**	**<5**	**<5**	**<5**	**<5**	**<5**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

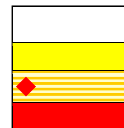
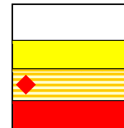


Table 114b Technology Requirements for Wafer Environmental Contamination Control—Long-term (continued)

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
Bulk Gases (Contaminants, ppbv)						
CO_2 (N_2, H_2O, O_2, THC)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Critical clean dry air (e.g., lithography) (H_2O, THC) (SOx, NOx, amines all X0.05)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
Lithography purge for 193 nm (O_2 and H_2O X1000, CO, CO_2, THC)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
Lithography purge for 157 nm (CO, CO_2, THC)	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**
Lithography purge for 157 nm (O_2, H_2O,)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
Number of particles > critical size (/m^3) [A]	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
Specialty Gases						
Etchants (corrosive, e.g., BCl_3, Cl_2)						
O_2, H_2O (ppbv)	**100**	**100**	**100**	**100**	**100**	**100**
Critical specified metals / total metals (ppbw) [W]	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Etchants (Non-corrosive, e.g., C_2F_6, NF_3)						
O_2, H_2O (ppbv)	**100**	**100**	**100**	**100**	**100**	**100**
Deposition (e.g., SiH4, NH3, (CH3)3SiH)						
O_2, H_2O (ppbv)	**100**	**100**	**100**	**100**	**100**	**100**
Critical specified metals / total metals (ppbw)	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**	**<1/TBD**
Dopants (e.g., AsH_3, PH_3, GeH_4)						
O_2, H_2O (ppbv)	**100**	**100**	**100**	**100**	**100**	**100**
Inerts—Oxide/Photoresist Etchants/Strippers						
Inerts (O_2, H_2O ppbv)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
He, H_2 cylinder carrier/purge gases (N_2, H_2O ppbv)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

The defect budget validation results obtained by International SEMATECH in 1997, 1999 and 2000 have been used for the 2003 revision. Another survey is needed as soon as possible to validate future defect budgets. Research into better yield modeling techniques is required to address future modeling challenges. Modeling of systematic mechanisms limited yield (SMLY) is increasingly becoming a significant focus of yield learning experts. This is being driven by the fact that SMLY issues tend to dominate in the early yield ramp stages, and these yield ramp rates continue to accelerate. In addition, parametric limited yield issues and design to process mismatch tend to limited yield in the early ramp timeframe. Furthermore, the recent process variation caused by line edge roughness (LER) is looming ahead. The increasing dominance of non-visual defects will further complicate yield modeling and defect budgeting. Thus, defect models will need to better consider electrical characterization information, and reduce emphasis on visual analysis. This will require research into new characterization devices and methods. Interconnect process layers are a particular challenge and have been so identified in the technology requirements. Some issues include modeling the yield impacts of ultra-thin film integrity, increased process complexity, interconnect speed and transmission characteristics, and the impact of wavelength dependent defects on reticles that may or may not result in defects. This research is complicated by the lack of state-of-the-art semiconductor processing capabilities in universities and other research sources. Figure 77 illustrates a few potential solutions that may help address the technology requirements for future yield modeling.

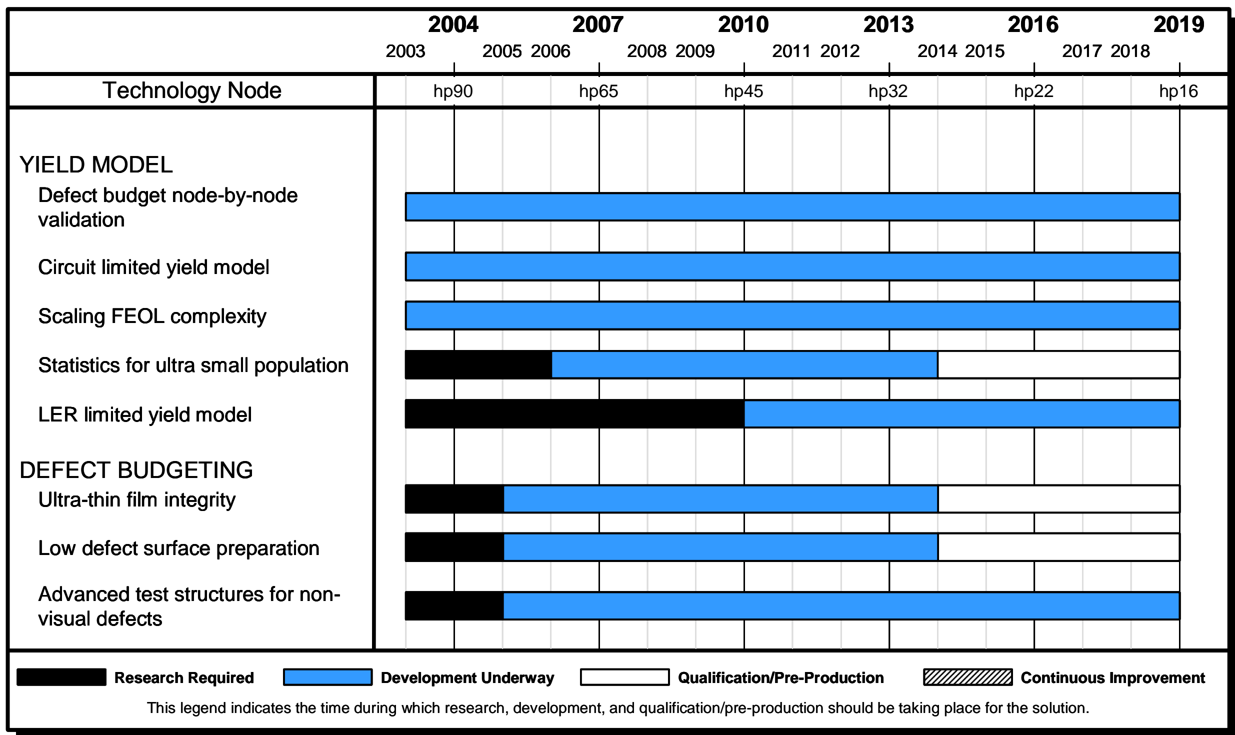


Figure 77 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION AND CHARACTERIZATION

Considerable research and development is now necessary to meet the technology requirements for advanced defect detection tools. Detection in high aspect ratio (HAR) structures created Post-Etch (Figure 78) is currently deficient. Light-scattering and optical-imaging solutions for production will consequently become limited by 2005. The quest for an effective solution to the detection of very thin residue at the bottom of an isolated HAR structures demands faster

development of novel methods such as holographic imaging, e-beam (scattering or imaging), acoustic imaging techniques, and X-ray imaging.

There is a lack of suitable component technologies for developing novel detection systems. Significant advancement associated with shorter wavelengths, continuous-wave lasers, detectors with higher quantum efficiency and higher acquisition speed, suitable low-loss and low-aberration lenses, waveplates and polarizers, and robust mechanical and acousto-optic scanners are needed now to continue the economical development of optical techniques.

Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. Arrayed detection schemes for parallel data acquisition from a larger area of the wafer need to be explored. Enhancement of signal-to-noise ratio using software algorithms could possibly extend optical approaches.

Potential solutions must comprehend the need for greater amounts of defect-related data, e.g., composition, shape, defect classification, and rapid decision-making. (Refer to the following section on Yield Enhancement for a comprehensive explanation of the needs in this area.) Automated defect classification, spatial signature analysis, adaptive sampling, yield-impact assessment, and other algorithmic techniques are already reducing time to decisions and product at risk. Defect detection and characterization equipment must produce more information for these techniques to analyze. The challenge of improved sensitivity to smaller defect sizes has moved characterization platforms in-line to provide higher resolution. The trade-off between associated throughput and the provided information is crucial. Thereby, defect detection is evolving closer to the defect source. Development to integrate defect detection into process equipment must progress at faster pace to implement automated process control.

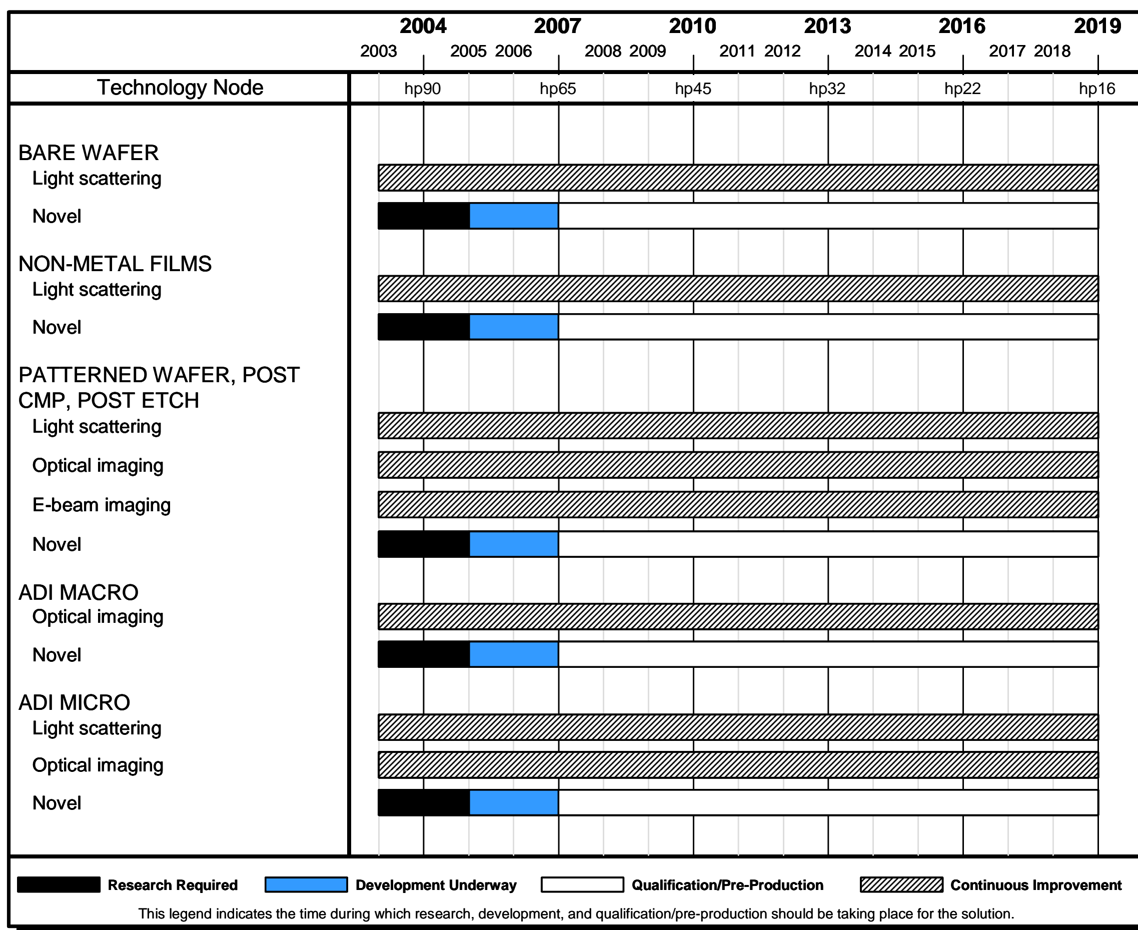


Figure 78 Defect Detection and Characterization Potential Solutions

Yield Learning

As indicated by the yellow and red areas of the yield learning technology requirements table, the two areas that require highest attention are data management and rapid defect/fault sourcing. A collaborative effort between the stakeholders

from device makers, metrology & information technology suppliers and academia is required to formulate and execute a strategic plan to manage all data relevant to rapid yield learning. Without such collaboration, much redundancy will continue to exist in data management and analysis. Additional potential solutions are provided in the Data Management System section below.

As noted above, yield learning rate can proceed at an acceptable improvement rate in the absence of defect/fault sources. However, given the technology transfer history of our industry, numerous defect/fault sources may be anticipated after the process technology is handed off to manufacturing by the process R&D group. There are two ways to achieve the required ramp of 30% to 80% yield in a year: 1) Reduce the total number of new defect/fault sources or mechanisms. 2) Reduce the time to source and fix each new defect/fault source or mechanism. Whereas the first approach is mostly company dependent, the second approach requires numerous tools and techniques for rapid defect/fault sourcing as shown below.

Moreover, with the continued increase in complexity of the design and fabrication process, the ability to detect and react to yield impacting trends and excursions in a timely fashion will require a larger dependence on passive data. This will be acutely true during yield ramp where maximum productivity and profit benefits will be achieved. Passive data is defined as defect, parametric, and electrical test data collected inline from the product through appropriate sampling strategies. The additional time required to perform experiments, such as short-loop testing, will not be readily available at future nodes. The time necessary to trend potential problems and/or identify process excursions will require the development of sampling techniques that maximize the signal-to-noise ratio inherent in the measured data. The goal of Integrated Data Management (IDM) is to identify process issues in as few samples as possible. Analysis techniques that place product data in the context of the manufacturing process provide a stronger "signal" and are less likely to be impacted by measurement noise since they comprehend various levels of process history and human experience (lessons learned). Therefore, potential solutions for rapid yield learning include the development of technologies that generate information from product data and tool-health or other in situ process measurements. Automation methods are also required that correlate product information with fabrication processes, sometimes referred to as data mining. Fundamental to the successful integration of new methods and technologies is a requirement for standards that facilitate data communications in the virtual and/or physically merged database environment.

VISIBLE DEFECTS

Although tools for sourcing visible defects are fairly well established (optical and SEM detection and review, SSA, ADC, EDX, FIB), new tools and methodologies will have to be developed to achieve adequate signal to noise ratio for differentiating real defects from background nuisance defects and to characterize the elemental composition of continuously shrinking visible defects.

NON-VISUAL DEFECTS

Affordable inspection techniques are needed that go beyond optical microscopy and offer high resolution without sacrificing throughput. To source non-visual defects, the resolution of analytical tools for failure analysis needs to be improved. Technology nodes below 90 nm will require the development of affordable failure analysis techniques that can extend the range of detectable defects down to the atomic level. In addition, the resolution of internal node DC micro probing for characterizing individual circuit/transistor parameters or isolating leakage paths needs to be improved. Design to process interactions that can lead to localized non-visual structural defects have to be researched and modeled. Design for testability/diagnose-ability techniques need to utilize these models to enhance the localization of a defect source.

Along with new technologies such as optical proximity correction (OPC), and the inclusion of alternating and phase shifting elements in lithographic masks, the potential for non-defect related yield problems are likely to increase. New strategies and technologies for comparing the measured, three-dimensional die structure to the expected printed pattern based on design data will be needed to identify and rapidly correct lithographic patterning and etch problems. Interferometric optical techniques, stereo scanning electron microscopy and high throughput atomic force microscopy will be able to provide three-dimensional topological structure at critical positions across the wafer (analogous to critical dimensional metrology for line width measurements). These measurements coupled with an ability to produce a reference topology based on the expected structure from design data, will provide yield engineers with the ability to track subtle variations in physical topology that impact electrical device function. The ability to rapidly make multiple measurements across the wafer and to render and compare the physical and expected structure will be critical for improving the learning rates for non-visual structural events that impact yield.

PARAMETRIC DEFECTS

Saving more parametric data as measured on circuit testers will aid in sourcing parametric source defects. This information will allow for correlation to process data, through a variety of techniques, including spatial signature analysis. Modeling the probabilities of factors that can lead to “parametric defects” can also reduce the time it takes to source the cause. Built-In Self Test (BIST) techniques must be developed to identify race conditions and other failure modes that are a function of parametric variation or mismatch.

ELECTRICAL FAULTS

Presently, memory array test chips and memory arrays within microprocessors are used to quickly isolate faults. This technique is likely to be extended to non-arrayed devices. Future products must be designed so that the test process can isolate failures. Design for test (DFT) and BIST are two methods that can aid in defect isolation. Both DFT and BIST failure pattern must map to a physical location on a circuit. Accurate fault to defect mapping models must also be developed to further assist in the defect localization process. Other test programs are needed to save failure pattern information so that it can be analyzed based on pre-determined (modeled) failure mode probabilities. All of these techniques will allow yield engineers to more quickly and precisely determine the locations and causes of circuit failures.

DATA MANAGEMENT SYSTEMS (DMS)

The following key areas of R&D investment have been identified by Oak Ridge National Lab (ORNL), as part of a SEMATECH-sponsored DMS assessment study, as necessary elements for meeting tomorrow’s DMS challenges:

- Standards for data/file formats and coordinate systems
- DMS/WIP integration
- DMS methodologies for data collection, storage, archiving and purging
- DMS for advanced tool/process control

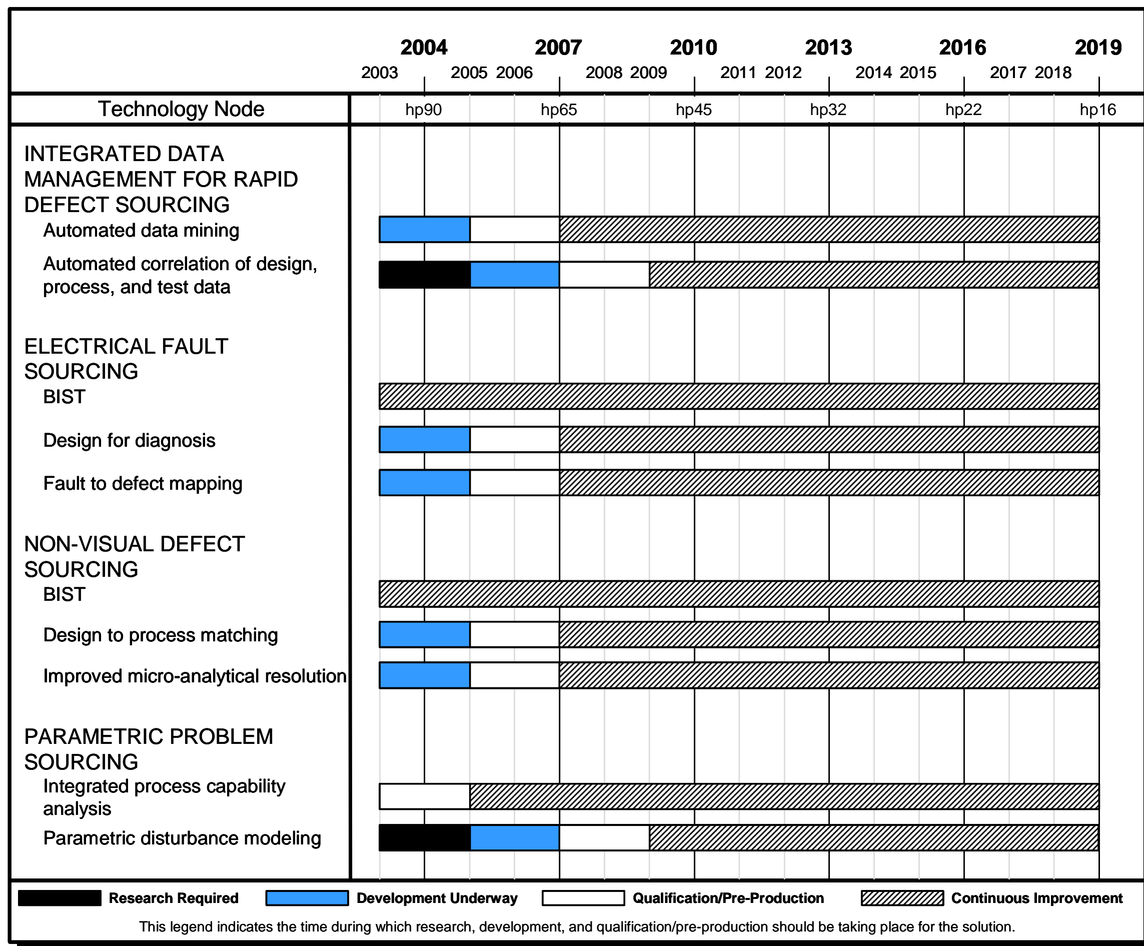


Figure 79 Yield Learning Potential Solutions

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and actually enable cost-effective high volume manufacturing for 130–100 nm devices. Refer to Figure 80. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, in situ chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from in situ sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. In situ process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

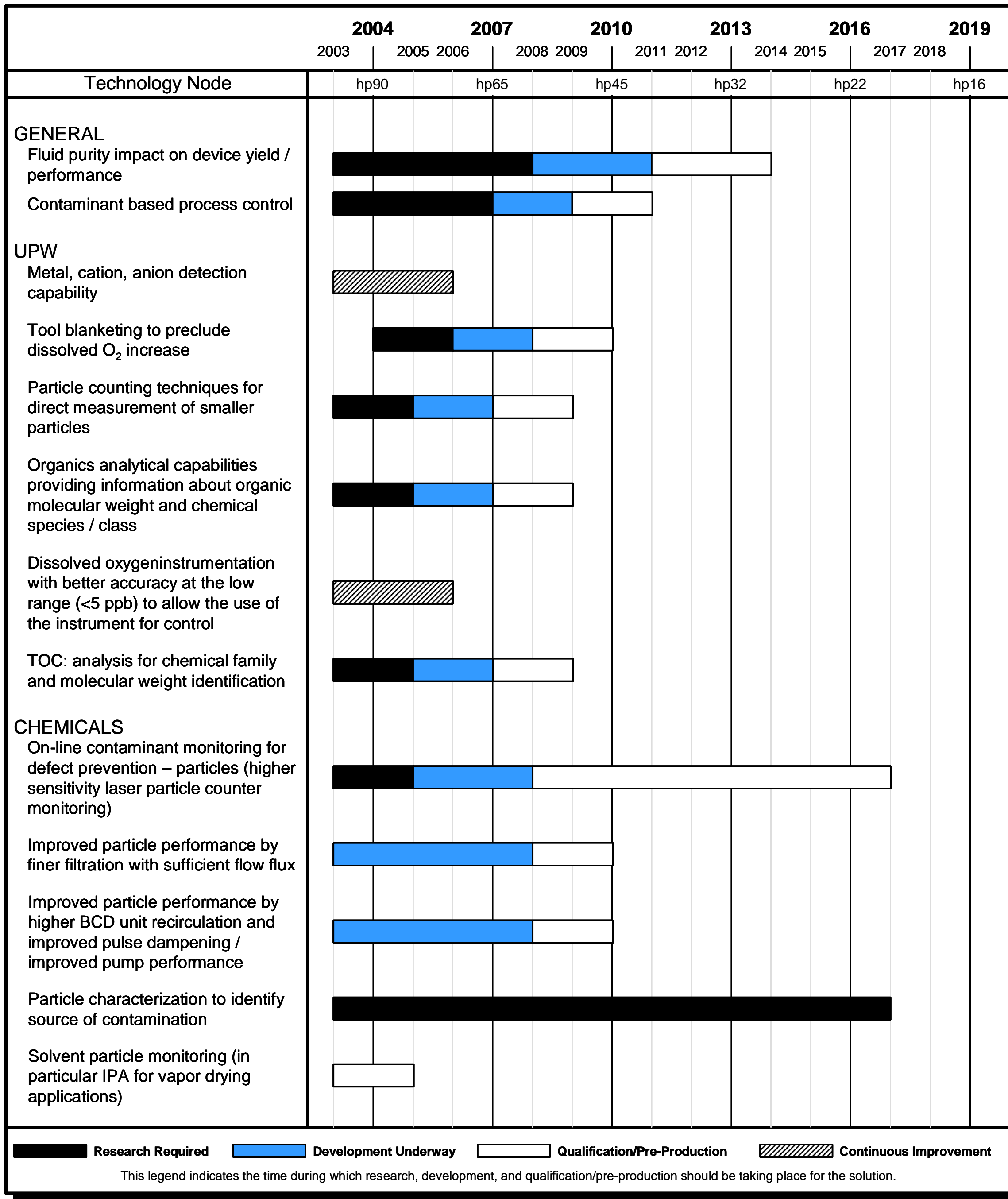


Figure 80 Wafer Environmental and Contamination Control Potential Solutions

Process critical materials—Figure 80 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities.

UPW—The quality focus needs to move towards the point of use. Water quality is generally measured at the point of production and not at the POU or at the wafer. An understanding of the impact of the tool upon water quality, specifically particles, silica, and dissolved oxygen, needs to be understood to ensure quality is carried to the wafer. Inline trace impurity analytical technology for process critical materials is needed to better understand purity levels at the POU. Ultrapure water particle levels are easily achieved with existing design and filtration practice and verified with available offline particle metrology. Improved online monitoring is required to detect excursions realtime for particle sizes below 0.1 µm. Improved analytical technology is needed to characterize ultra-trace levels of silica. Recycling and reclaiming

initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water.

Chemicals—Figure 80 shows various technological areas that may be required to enhance the purity of delivered chemicals to the wafer manufacturing process.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Availability of affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to effective wafer isolation deployment.