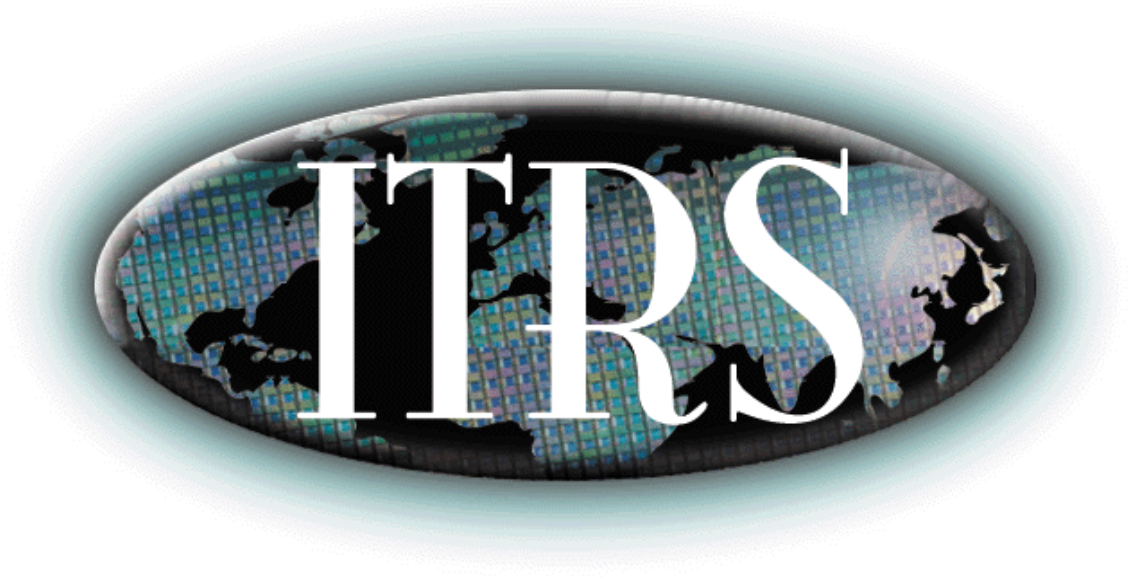

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2009 EDITION

EXECUTIVE SUMMARY

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2009 Friends of the Roadmap

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Link to 2009 ORTC tables.

INTRODUCTION

OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three and a half decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 35 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and most recently in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29%% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore

it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensures that the 2009 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete 2009 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site *http://www.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2009 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

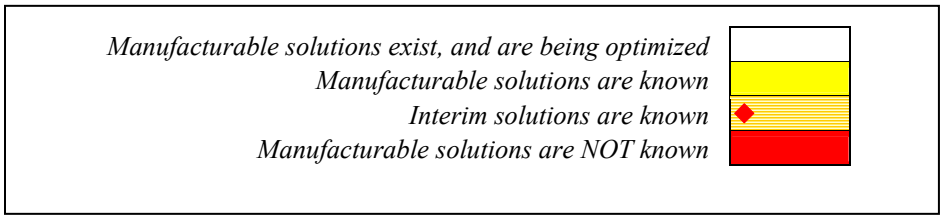
For the 2009 edition, three ITRS meetings were held worldwide as follows: Brussels, Belgium (sponsored by the ESIA and hosted by NXP Semiconductors); San Francisco, U.S.A., sponsored by the SIA, organized by SEMATECH and co-hosted with SEMI/North America; and Hsinchu, Taiwan (sponsored and co-hosted by TSIA and TSMC). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004, 2006, 2008) while complete editions are released each odd-numbered year (2001, 2003, 2005, 2007, 2009). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity and confidence levels, represented by colors in the tables, for these targets:



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge"

spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS road-mapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2007 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2009, 2010… through 2016) and "Long-term Years" (2017, 2018 … through 2024) This format is illustrated in Table B, which contains a few key rows from lithography-related Table ORTC1, including the Flash product uncontacted polysilicon half-pitch technology trend line item as the most aggressive technology target. In the previous 2005 Roadmap editions, the DRAM stagger-contacted M1 half pitch line item was used as a standard header for all the ITRS ITWG tables; however, beginning with the 2007 edition, the IRC has requested that only the year of first production be required as a standard header. At the discretion of the ITWGs, other product technology trend driver line items may be selected from Table ORTC1 for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

YEAR OF PRODUCTION	2009	2010	2011	2012	2013	2014	2015	2016
Flash Uncontacted Poly Si ½ Pitch (nm)	38	32	28	25	23	20	18	15.9
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	52	45	40	36	32	28	25	22.5
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21	18.9
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22	19.8
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17	15.3

Long-term Years

YEAR OF PRODUCTION	2017	2018	2019	2020	2021	2022	2023	2024
Flash Uncontacted Poly Si ½ Pitch (nm)	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5
MPU Printed Gate Length (nm)	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9
MPU Physical Gate Length (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes.

However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. In the 2009 ITRS, we will continue the practice of eliminating references to the term "technology node." As mentioned above, the IRC has recommended that the only standard header will be year of first production, and DRAM M1 half-pitch is just one among several historical indicators of IC scaling. With this latest change to standard ITRS table format policy, it is hoped that the ITRS will not contribute to industry confusion related to the concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage within the context of the application to the technology of a specific product.

For reference on the 2005 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 1.

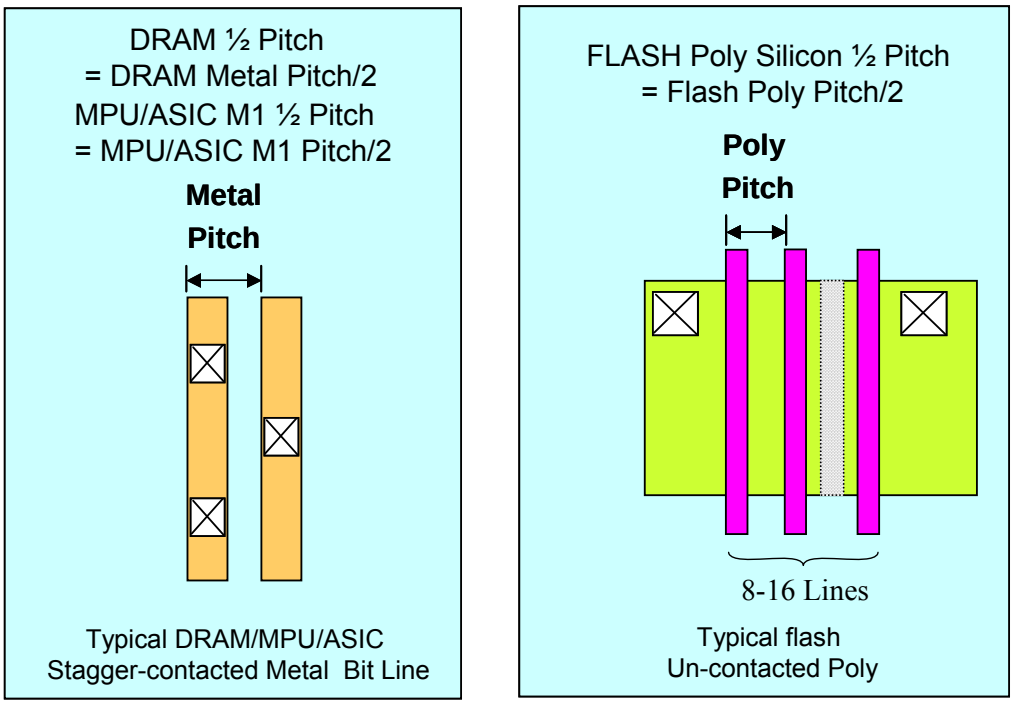


Figure 1 2009 Definition of Pitches

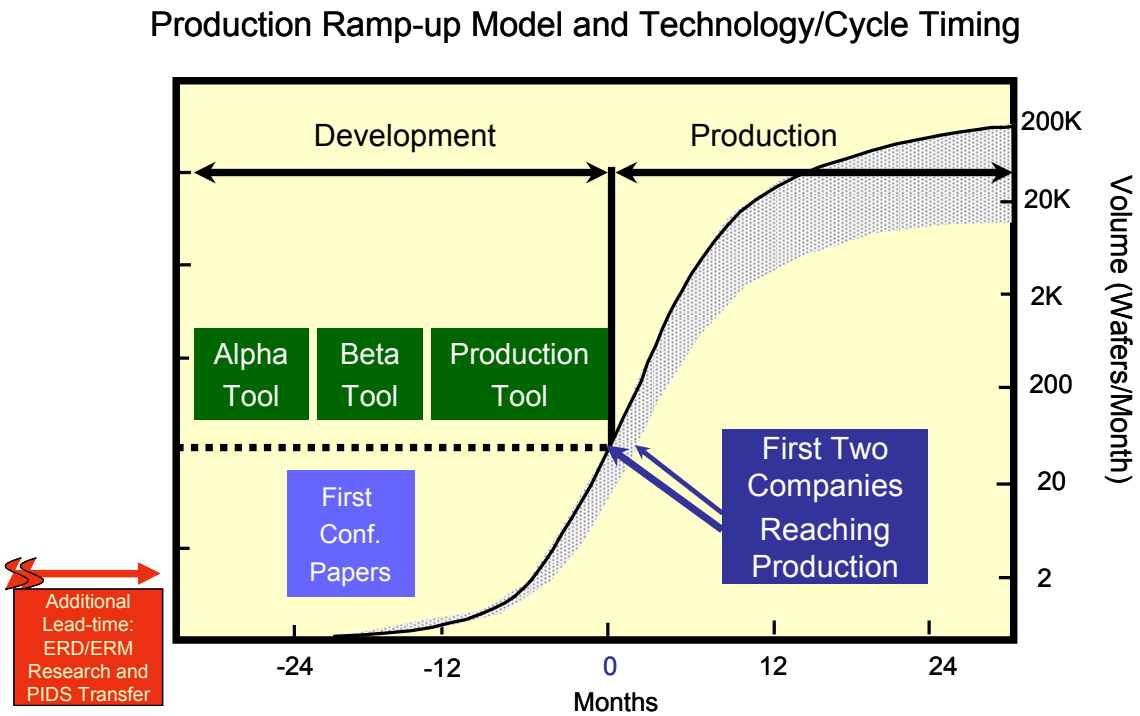
MEANING OF ITRS TIME OF INTRODUCTION

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 2a.

Figure 2a has been revised from previous roadmaps and no longer includes reference to volume parts per month, due to the variability of different product die sizes for first production targets. Therefore, only the typical industry high volume ramp scale is retained in the 2009 roadmap.

In addition, a graphical note was added at the request of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) TWGs to highlight that it is necessary to consider the very-wide-time-range required to capture early research activities that may result in Potential Solutions items for the ITWG Grand Challenges. It has become increasingly important to communicate a broad horizon encompassing both the period preceding the first manufacturing alpha tools and materials and also the period that extends to the classic ITRS 15-year horizon and even beyond. The preceding horizon is required to capture the period of the very first technical conference paper proposals until the start of development activities; at which point typically a transfer from ERD/ERM to PIDS/FEP ITWGs occurs.

For more explicit clarification, see Figure 2b, in which an example is shown for a new gate structure potential solution targeted for 2019 production. In this example, the first research papers appear in 2007, and the Potential Solution technology would be planned for transfer to PIDS during the 2011 ITRS roadmap work, when more detailed line item characteristics would be defined.



(also see Figure 2b below for ERD/ERM Research and PIDS Transfer timing; and also Figure 2c for Typical Wafer Generation Pilot and Production "Ramp Curves"

Figure 2a A Typical Technology Production "Ramp" Curve (within an established wafer generation)

The "Production" time in the ITRS refers to the time when the first company brings a technology to production and a second company follows, typically within three months; however sometimes there is a longer time for the second company to get into production. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figures 2a and 2b can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. As an example, this time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month [for the example of a chip size

at 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month)].

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the industry is approaching the time for a new 450 mm wafer generation transition, additional scrutiny has been given to the historical ramp rate for a technology cycle that has been ramped in two wafer generations of the first leading companies at the same time (see the discussion and the new 2009 ITRS Figure 5 in the 450 mm section). It is during that transition of a technology cycle coexisting within two wafer generations that the economic productivity gain modeling is also examined.

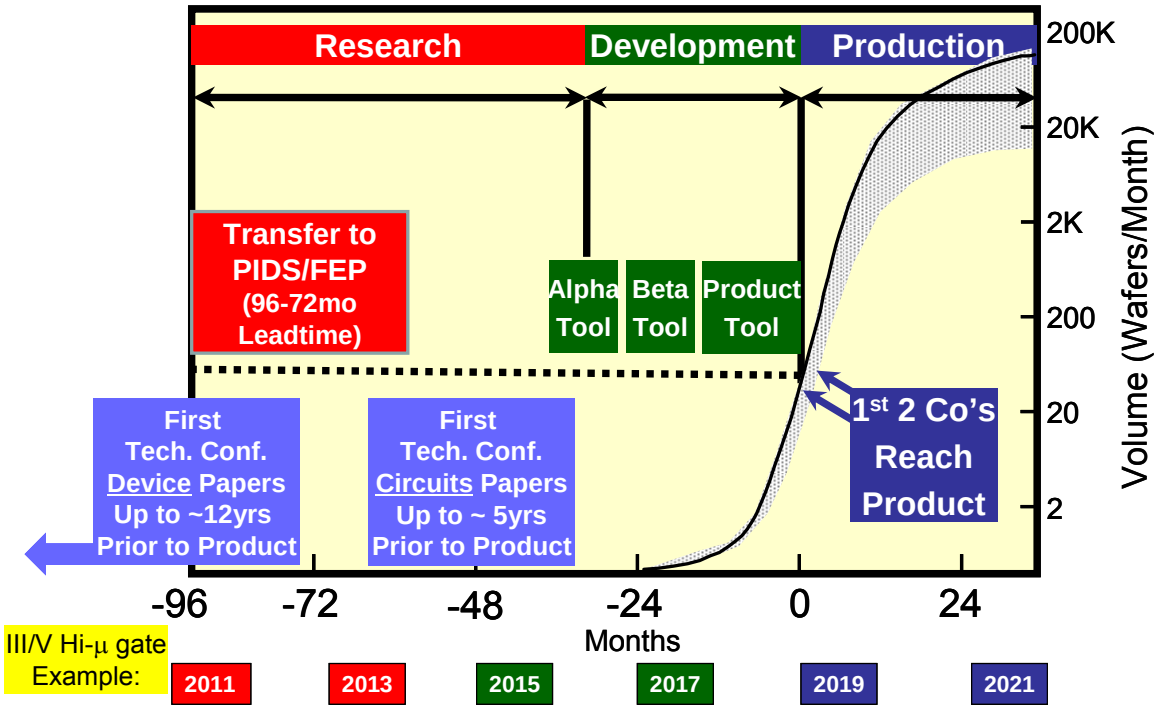


Figure 2b A Typical Technology Production "Ramp" Curve for ERD/ERM Research and PIDS Transfer timing (including an example for III/V Hi-Mobility Gate Technology Timing Scenario)

2009 SICAS Industry Manufacturing Technology Capacity Update

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

Furthermore, it has been observed that some companies consciously choose to utilize aggressively leading-edge technologies only for a subset of their product portfolio; because it is not economically attractive to do so for all products. Individual Companies decide to go slower or even stick to trailing technologies with specific products because further shrinking might not even make sense anymore. Therefore there appears to be a broader split of technologies in use which is becoming even broader.

Figure 3 [updated with 2Q09 SICAS data] shows, in horizontal bar graph format (each bar width is proportional to silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits, which are quite widespread.

The ITRS technology cycle, as measured by DRAM metal 1 (M1) half-pitch, is shown as yellow marks (for the historical actual timing), as reported by the industry surveys conducted by ITRS TWGs. The surveys conducted in 2003, 2005, and 2007 have indicated that first production of the leading-edge DRAM M1 half-pitch has been on a two-year cycle (for 0.71× reduction per technology cycle), from 250 nm in 1998 through 90 nm in 2004. However, the most recent survey update is indicating that the DRAM historical trend is tracking closer to the ITRS MPU trend. This was investigated further in 2007 and 2008, and reported in the 2008 Update.

The Table ORTC1 was revised in the 2008 Update so that the DRAM M1 contacted half-pitch was on the same 2.5-year cycle as the MPU M1 contacted half pitch targets. The DRAM M1 contacted half-pitch targets for the 2009 ITRS Table ORTC1 remains unchanged on a 2.5-year technology cycle through 2010/45 nm. From 2010 through the 2024 timeframe, the DRAM M1 targets retain the 3-year technology cycle. The Flash Memory uncontacted poly half-pitch targets for the 2009 ITRS Table ORTC1 was extended on a two-year pace through 2010/32 nm, at which point it turns to a three-year technology cycle pace. The MPU M1 contacted half-pitch targets for the 2009 ITRS Table ORTC1 were revised to a trailing two-year cycle pace that crosses the DRAM M1 in 2010/45 nm. The two-year pace continues through 2013 and then turns parallel to the DRAM and Flash three-year technology cycle pace.

The blue mark on the Figure 3 graph indicates the timing for the next 2009 ITRS target for the DRAM 2010/45 nm and then continuing on the three-year cycle to 2013. Also included in the updated Figure 3 graphics are the data points for the new two-year cycle MPU trend (blue circle) and the Flash (violet rectangle) trends

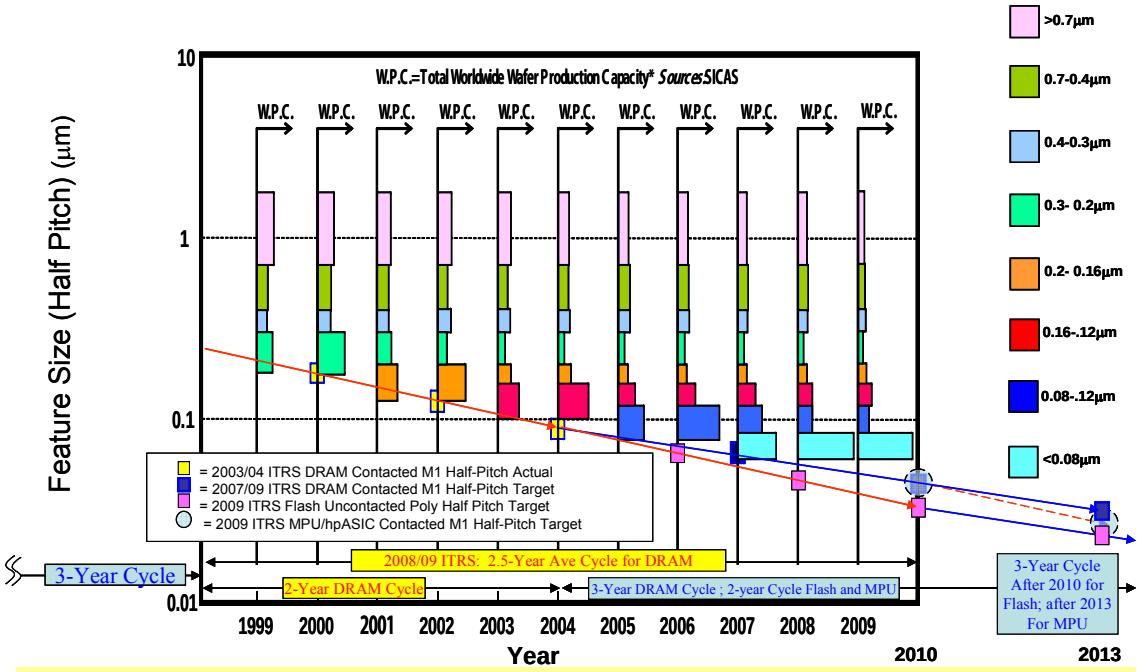
Note that the first production of the leading-edge feature size has historically ramped into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the same historical two-year-pace timing for first production. However, the latest SIA WSTS statistics for the "<0.08μm" technology demand split [added to the worldwide semiconductor trade statistics (WSTS) survey in 2008] indicate that the pace for that most-leading-edge capacity has actually accelerated faster than the two-year demand pace

Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations has typically grown to nearly half the capacity of the industry within two to three years after their introduction. The 2009 ITRS has updated the Flash technology trend to continue on a two-year cycle until 2010, which should add even more capacity at the most leading edge.

It can be observed in Figure 3 that the capacity for the most leading edge technology (45 nm) is presently only available within the SICAS "<0.08μm" capacity split. The availability of the "<0.06 μm" split survey data, which would include the rapidly ramping 45 nm Flash and MPU/ASIC technology cycle capacity, has been delayed from SICAS until 2010. Therefore, the actual analysis of the 1.5-year to three-year technology demand cycles (to the 20–30% of total MOS capacity ramp point) will not be available until possibly the 2010 Update of the ITRS.

It is notable that relative share of trailing edge capacity does not decline as rapidly as might be expected (migrate upward to leading-edge); and the leading-edge capacity split shares should be expected to continue to "crowd" as products migrate to the most leading-edge capacity ("<0.08 μm" capacity data). This phenomenon continues to hold significant implication for the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology Grand Challenges.

Suppliers must provide support for not only the longer-lasting trailing edge factories, but also the many diverse product and technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge to both suppliers and manufacturers, especially with the preparation for 450 mm wafer generation investments.



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2009. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Figure 3 Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution[1]

ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices and technology. Thus new technologies may involve not only new devices, but also new manufacturing and design paradigms.

Microprocessors, memories, and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption and communications bandwidth (e.g., RF), and many functional requirements, such as the functions performed by passive component, sensors and actuators, biological functions, and even embedded software functions, do not scale with Moore's Law. In many of these cases, non-CMOS solutions are employed. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, (SiP)) will become increasingly important. In terms of functionality, SoC and SiP can be complementary, and hence are not necessarily competing with each other. Functions initially fulfilled by non-CMOS

[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2009. The detailed data are available to the public online at the SIA website, www.sia-online.org.*

dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from core CMOS. Consequently, the partitioning of system-level functions between *and within* SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, extremely parallel software, etc. For SiP applications, packaging will be a functional element and a key differentiator. This trend is represented graphically in the 2009 ITRS Figure 4.

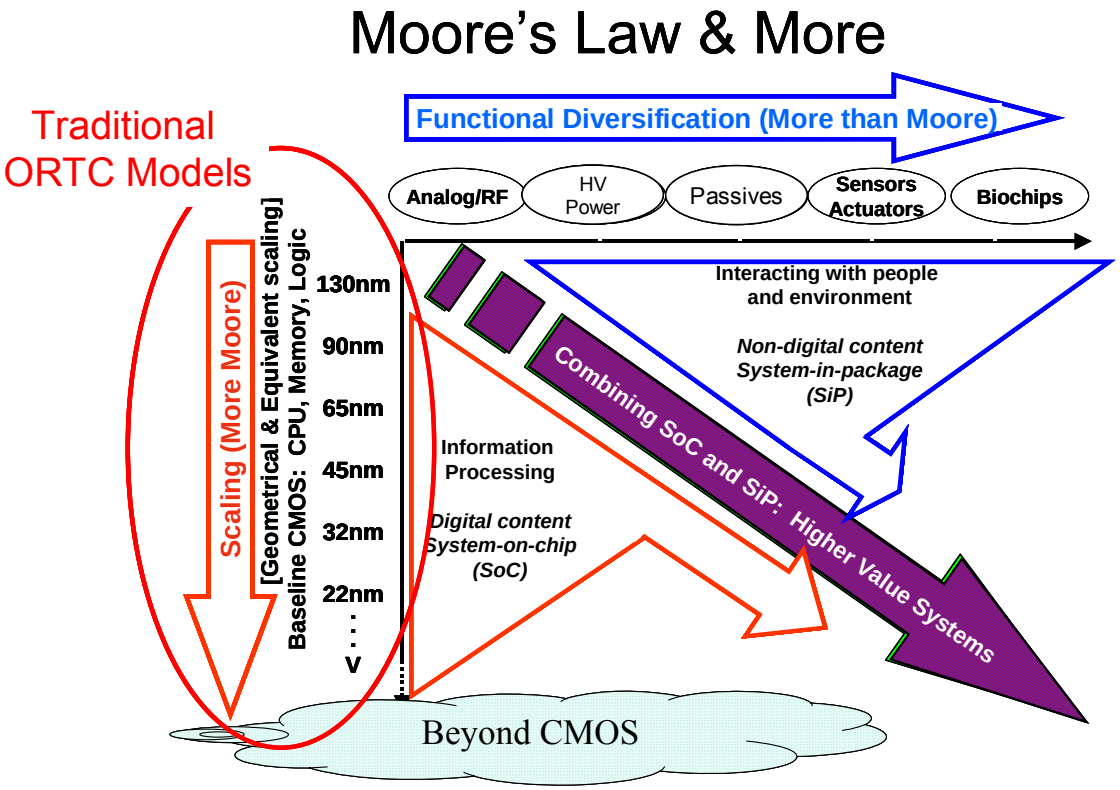


Figure 4 Moore's Law and More

MORE THAN MOORE

This concept of "More than Moore," introduced in the 2005 roadmap, has been further discussed and refined since. For example the "Beyond CMOS" concept has been given more discussion and detail in the ERD and ERM chapters, and white papers have been placed on the public website to provide more details on the "More Than Moore" and system-on-chip (SOC) and system in package (SIP) concepts. In addition consensus was reached on the following definitions, which were added and updated in the 2009 ITRS. (Refer to Figure 4 and the Glossary):

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling*—refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)*—refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)*—refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: design-for-variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multi-core SOC architectures."

- Addresses the need for quantifiable, specific design technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs; and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices (ERD) and Materials (ERM), focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system (NEMS) switches.

It is expected that the relative weight of the "More than Moore" component of the industry evolution will increase over time. This increase leads to a growing diversity of the scientific fields that the research must cover in order to sustain the pace of innovation, while the financial constraints are becoming tighter. The question of the guidance of the research efforts, in which the ITRS is playing a pivotal role, is therefore crucial. Taking this into consideration, various working groups of the ITRS have been investigating the consequences of the "More than Moore" trend in their field of expertise. The results of that work, which will further gain momentum in the coming years, can be found in their respective chapters.

The scope of the 2009 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

2009 ITRS SPECIAL TOPICS

ENERGY

Energy consumption has become an increasingly important topic of public discussion in recent years because of global CO_2 emission. Since semiconductor electronics are broadly applicable to energy collection, conversion, storage, transmission, and consumption/usage, it is not surprising that the ITRS addresses many factors of significance to energy issues. In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process, and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively.

At the next level, the ITRS addresses integrated circuit design and its system-level drivers. In both the ITRS Design and the ITRS System Driver chapters, there is increasingly direct influence of energy factors on design technologies, which started a number of years ago. Power consumption is now one of the major constraints in chip design, and the ITRS has identified it as one of the top three overall challenges for the last 5 years. Leakage power consumption, including its variability, has been identified as a clear long term threat and a focus topic for design technology in the next 15 years. The connection with the energy challenge is based on the increasing worldwide usage of information technology devices.

In addition to improved efficiency of the basic components (i.e., switches, wires, and memory bits) and of the circuits they compose, the major favorable impact on energy usage of advancing semiconductor technology is in the applications of the circuits themselves, which are often designed specifically to improve the energy efficiency of end-equipment systems which they control. For example, microcontrollers, signal processors, and power/battery management circuits are key to the efficiency of communications systems, household appliances, transportation (e.g., cars), industrial machines, etc.

The ITRS also addresses the minimization of energy usage in semiconductor manufacturing. In particular, the Factory Integration and the Environmental, Safety, and Health chapters present goals for further reducing the amount of energy and other resources required to produce integrated circuits and to generally increase the environmental friendliness of IC fabrication. For 2008, the Factory Integration Technology Working Group agreed to use Wait Time Waste and Equipment Output Waste as the first two high level metrics for which to define a roadmap for waste reduction.

Their next goal is to incorporate waste reduction roadmaps for these two metrics in the 2009 ITRS update. They report "Systematic waste visualization is expected to identify waste in both material and energy use. A strategy will be defined for how to determine the starting point/baseline value and the feedback mechanism for each high level metric."

Similarly, the 2008 Front-End Processing (FEP) Technology Working Group reports that with respect to the current global energy and environmental situation, technology development in FEP is now driven not only by a desire to improve circuit density and speed, but also by a desire to reduce power consumption and manufacturing waste. The implementation of high-k/metal gate technology for logic transistors provides faster transistors while simultaneously reducing leakage and power consumption. Both power consumption and performance will eventually drive the transitions to Fully Depleted Silicon-On-Insulator (FDSOI) and MG transistor structures. As has already been noted at various points in the 2007 ITRS publication, efforts continue to reduce chemical and material usage and waste. For instance, more dilute solutions continue to be implemented for cleaning steps. In addition, FEP continues to work closely with the Factory Integration technology working group to identify process equipment that could be put into a reduced power consumption 'sleep mode' condition while not being used to process wafers. Of course, the concept of "sleep" and other energy-saving modes originated in circuit design. The Glossary of the 2008 ITRS documents these techniques as part of Design Equivalent Scaling. See the previous section "More than Moore."

Finally, near its 15-year horizon, the ITRS anticipates beyond-CMOS devices that may greatly extend the energy efficiency of information technologies. As part of its work in this area, the Emerging Research Devices Technology Working Group summarized the output of the 2008 Virtual Immersion Architecture (VIA) Forum: "An area of concern is that the growing popularity of VIA applications is driving a substantial increase in global energy consumption. This emphasis on more computational throughput per unit of energy holds not only for desk-top machines but also for handheld devices. In hand-held applications very little energy is available for information processing, and much higher performance per joule of expended energy is required if the extended range of applications is to be realized. Both of these trends imply that computation performance, in some suitable metric, must be increased by one-to-two orders of magnitude by 2020. This raises the question of the maximum attainable performance per joule and suggests a rapprochement between information theory and thermodynamics. An approximate, first principles analysis of a four-instruction, single-bit processors indicates that operating efficiencies of less than thirty percent are being realized by CMOS technologies and classical computing architectures. Perhaps architectures that can adapt themselves to their workloads to achieve energy-efficient operation would offer an alternative approach with higher performance per joule of energy expended."

ITRS will continue to focus diligently on energy-related issues along the directions outlined above, and to make important contributions to the energy challenges facing the world.

EMERGING RESEARCH MATERIALS

Many of the new device and memory concepts that are being discussed in the ERD chapter will employ new materials, for example, for the device itself as well as for interconnect and passivation. The requirements for these new materials are critically dependant on the properties and specifications of the new devices and memories. This led in 2005 to the creation, within the ERD chapter, of a sub-group for Emerging Research Materials (ERM). In the 2007 edition of the roadmap, this subgroup had become a full-fledged working group, and the results of this work are further expanded and enhanced in 2009 and published in the dedicated Emerging Research Materials (ERM) chapter.

TRANSITION TO 450 MM

The rationale for a transition to 450 mm diameter wafer is productivity, one of the enablers of Moore's law. This is the ability—everything else staying the same—to decrease the manufacturing cost of each mm² of IC by the use of larger

diameter wafers. Based on economic considerations, during the 2007 ITRS roadmap development, the International SEMATECH Manufacturing Initiative (ISMI) had determined that to stay on this productivity curve, the industry needed to achieve 30% cost reduction and 50% cycle time improvement in manufacturing by 2012, which in their opinion would be achievable only via a transition to 450 mm (while the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). This was reinforced in 2007 by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program had cycle time opportunity but fell short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

More recently, Intel, Samsung, and TSMC (IST) announced in May 2008 that they will work together with suppliers, other semiconductor players, and ISMI to develop 450 mm with a goal of a pilot line in 2012. Full production may be two to three years after that.[2]. This Public announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI, as of the date of writing of the ITRS 2009 edition

The timing of the production ramp of 450 mm facilities (versus early pilot line capability) depends not only on the mastering of all technical issues, associated with this transition to a new diameter, but also on the preparedness of the industry. To assess the likelihood of that timing, the whole value chain must therefore be examined:

- On the equipment suppliers' side, the ITRS is lacking visibility on the plans of key suppliers for prototype tools.
- On the manufacturers' side, an important question is related to the initial investment "step function": the promises for productivity gains in 300 mm fabs have proved to become true for very large investments, in the range of $4B or beyond. One might expect that the minimal economical size of a 450 mm fab will be even larger, putting it beyond the reach of many companies. Furthermore, while an economic model which takes into consideration the industry as a whole may conclude that 2012 is the right time for transition to 450 mm (as concluded by the ISMI in 2007), decisions of individual companies may differ. So both the initial rate of growth of the 450 mm equipment market and its size at maturity can be questioned, which could lead equipment suppliers to delay their investment in the development of this new generation.

Taking lessons from the past, it can be observed that each wafer size transition has been different from any of the previous ones. The conversion to 300 mm wafer can be characterized by fact that for the first time the consortia (I300I and Selete) led the whole industry effort. The well-tested consortium effort is also the chosen approach for the 450 mm wafer size conversion. SEMI participation was also essential in the 300 mm wafer size conversion since for the first time "provisional standards" were agreed upon by the whole industry before the final manufacturing equipment was fully developed. In particular, the industry solved a fundamental problem by agreeing on adopting full wafer transport automation. All the suppliers abandoned their proprietary solutions to wafer transport, port design, and load size in favor of the agreed FOUP/ overhead solution. This effort took many years of discussion before the final solution was finally agreed by all parties. In this respect, the 450 mm wafer size transition is taking fully advantage of the work previously done to standardize the 300 mm wafer transport by having already adopted the same whole automation scheme with only minor upgrades thus placing the 450 mm automation schedule ahead of the corresponding 300 mm wafer size conversion schedule with respect to automation.

On the other hand, the Front-End Processes working group has advised the IRC that, although significant progress has been made and reported by SEMATECH/ISMI, specific development-level targets for epi and flatness have not yet been met, and is now estimating that wafer suppliers will move the work on 450 mm wafers from research to development by 2011. For 300 mm, this transition occurred approximately seven years before 300 mm was used by IC manufacturers in production, which would put 450 mm production timing by 2018 if development will continue at the same rate as before. Accelerated development on this item (which may be underway in the work at SEMATECH/ISMI with suppliers), will be required to achieve a transition date for IC manufacturers to start moving to 450 mm in the 2014–2016 timeframe. For that reason, the FEP starting materials metrics table (Table FEP10) colored 450 mm "yellow" for 2014, showing a possible timing disconnect with the IST/ISMI 2014 production date, while not excluding it, and the need for deliberate wafer supplier industry effort to be in line with the planning announced by ISMI and the three IST companies. Progress will continue to be monitored during the work and conferences of the ITRS 2010 Update work.

Given all of the above, and with advancements on the work of Next Generation Factory (NGF) programs at SEMATECH/ISMI that may create opportunities for improvement of 300 mm equipment which might eventually also be

[2] *Source: "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450 mm Transition Program Status Update for ITRS IRC,Seoul,Korea*

applicable to 450 mm processing, the ITRS IRC expects manufacturing tools to be available between 2012 to 2014 for pilot lines; with possible production manufacturing ramp from 2014–2016 and beyond, subject to 450 mm wafer high volume availability at that date. The ITRS/IRC further estimates that wafer diameter should not be tied to technology generations—leading edge technologies will for a limited period be running both in 300 and 450 mm technologies, as happened with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1) timeframe.

Furthermore, and new in the 2009 ITRS, a 450 mm Production Ramp-up Model Graphic has been provided (Figure 5) to clarify the special dual "S-curve" timing required when a new wafer generation is being introduced (modeled after the experience with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1) timeframe.

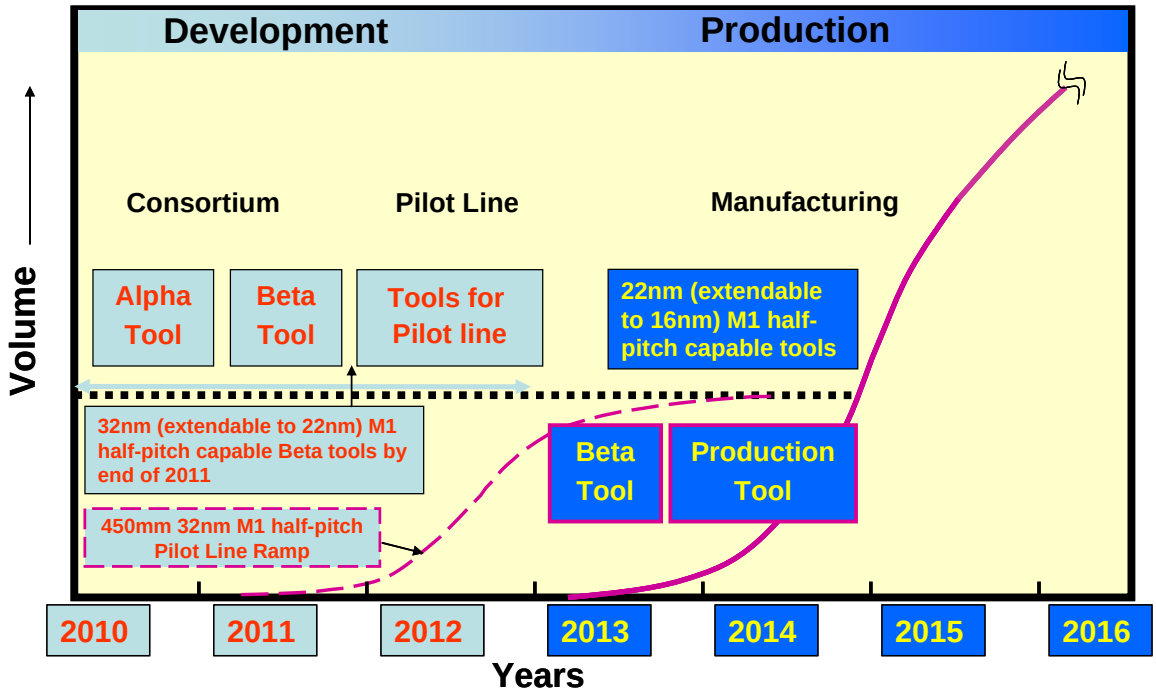


Figure 5 A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation

GRAND CHALLENGES

IN THE NEAR-TERM (THROUGH 2016) AND LONG-TERM (2017 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling. Flash device's scaling continues a two-year cycle until 2010, MPU is also on a two-year cycle until 2013, and DRAM is a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planar bulk metal-oxide semiconductor field effect transistor (MOSFET), multiple gate field effect transistors (e.g., FinFET), and silicon-on-insulator MOSFET.

The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in patterning, advanced materials, strain engineering particularly in non-planar device structures, junction leakage, process control, and manufacturability. Challenges also span SoC and SiP integration of CMOS with new types of memory devices. All these will be essential elements for the continuous growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges," which are included in this Executive Summary. In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2009 through 2016) and the "long term" (2017 through 2024) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~ 2017)

ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) will continue to be a difficult challenge particularly for the HP and LOP segments in the near term despite the inception of high-κ metal gate (HKMG). Interfacial layer scaling and/or silicon-high-κ interface quality are critical to the EOT scaling for the 22 nm node and beyond. Integration of higher-κ materials while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing are also challenges need to be faced in the near term. The complete gate stack material systems need to be optimized together for best device characteristics (power and performance) and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as multiple-gate MOSFETs (e.g., finFETs) and ultra-thin body FD-SOI are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now includes both stand-alone and embedded DRAM and SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. For stand-alone DRAM, high-κ materials are currently being used in an SIS structure for trench capacitors. Metal top electrode will be needed by 2007 and a full MIM structure with high-κ dielectric may be needed by 2009, when a dielectric constant greater than 60 is required for beyond 50 nm. Embedded DRAM in SOC applications will drive additional integration challenges. One such key challenge is the matching between the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic devices.

The need for advanced capacitor materials in trench DRAM are postponed relatively to the stacked capacitor by a few years; however the cell size factor for stack capacitor DRAM is 6, while that for the trench DRAM remains at 8. Novel cell concepts for the trench capacitor, depending upon the replacement of the conventional planar transfer device by 3D array transistor structures, are envisaged for 65 nm in order to alleviate device scaling issues.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory is becoming a new technology driver for both critical dimension scaling and material technology. The effective dimension, F, of Flash NAND device now appears to lead the DRAM half pitch.

The key challenges in Flash memory device are non-scalability of tunnel dielectrics, non-scalability of interpoly dielectrics, dielectric material properties, and dimensional control. In Flash memory devices, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. It is no longer feasible for the control gate poly Si to overlap the sides of the floating gate as the space between adjacent poly Si gates shrink. Thus high-κ interlayer dielectrics will be required to maintain an acceptable coupling ratio. Flash memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory, and FeRAM, for example. MRAM scalability of cell-size and write-power reduction still needs further breakthroughs. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size. Another challenge for MRAM and FeRAM going forward is their cost effective integration with logic technologies, FeRAM being particularly more challenging while MRAM seems more suitable for integration in the backend of the flow. Complex/transitional metal oxides resistive cells could have the potential for high density apps, if cross-point diode and 3D integration are successful.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Cost, power consumption and performance of wireless transceiver ICs in the <10GHz and the mm-wave applications continue to be the main technology drivers. The <10GHz application space, serviced by deep sub-micron CMOS technologies with emerging high κ dielectrics and channel strain engineering may require techniques to keep the device mismatch and the 1/f noise within acceptable levels. Applications that use HBT devices will benefit from a more aggressive vertical scaling. Less expensive integrated passive components with higher Q factors and higher densities for the MIM capacitor may require integration of new materials. MEMS development, MEMS integration with active Si and off-chip passive network processes are expected to significantly contribute to the overall system performance. Mm-wave applications will benefit from development of non-Si (GaN) based devices.

Signal isolation between the digital and the analog regions of the chip is becoming more critical as the chip complexity and operating frequencies increase while the power supply voltage decreases. While noise coupling through the power supply and the ground line can be addressed by design techniques, substrate noise coupling reduction may require significant amount of innovation.

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Major breakthrough in the gate stack of silicon-based field effect transistors in advanced microprocessors with nitrided SiO_2 gate dielectric replaced by a hafnium-based dielectric with a dielectric constant (κ) approximately 20 took place in 2008. The n- and p-doped polysilicon gate electrodes also got replaced by dual work function metal gates that eliminated poly depletion effects. Still, reduction of the equivalent gate oxide thickness (EOT) below 0.8 nm for 16 nm node and below 0.6 nm beyond 16 nm node with appropriate metal gates remains as the most difficult challenge associated with the future device scaling. Higher dielectric constant dielectrics with adequate conduction and valence band offsets with silicon and thinner interfacial silicon dioxide layer are required. Reduction of interface states for gate stack on multi-gate devices is one of key challenges for 16 nm node and beyond. Another critical challenge is scaling the interfacial layer between the high-κ dielectric and the silicon without channel mobility degradation from increased Coulomb and remote phonon scattering. Higher mobility materials such as Ge, SiGe, and III-V compound semiconductors will be needed for channel transport enhancement which will introduce additional challenges for future high-κ dielectric stacks due to the complex nature of their surfaces and lack of a high quality native interfacial oxide. Furthermore, reliability requirements for newer high-κ oxides, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability) must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance of 25–35 fF to ensure reliability of stored data. This will result in the introduction of dielectric materials with a higher dielectric constant (higher-κ), such as tetragonal zirconium oxide, tantalum oxide, Ba/Ti doped high-κ dielectrics or a combination of them in a multi component stack, along with a 3D memory structure. Going down to sub 3Å equivalent oxide thickness beyond the sub-45 nm node while maintaining very low leakage current (femto ampere per cell) is one of the major challenges the DRAM industry is facing.

In Flash memory devices, on the other hand, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. This difficult trade-off problem hinders scaling, suggesting the need to introduce high-κ material and 3D structure devices into Flash memory processing. While replacing the floating gate by either charge trapping layers or embedded nanocrystals will facilitate scaling, the grand challenge is to maintain adequate electron storage during cycling within the trapping layers in scaled device footprints to ensure sufficient read margins. This will be more challenging in multi level cells (MLC) where less than 10 electrons will separate the storage bits.

32 AND 22 NM HALF PITCH [LITHOGRAPHY]

32 nm half pitch remains a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double patterning or exposure; however the lithography cost will almost double. Extreme-UV lithography (EUVL) with wavelength reduced to 13.5 nm, an order of magnitude smaller than that of the water-immersion wavelength of ArF excimer lasers, is the official hope of the industry to advance Moore's law. It does not need double exposure until approaching the 11 nm half pitch. As a result there is less restriction in design rules. However, EUVL is still awaiting high-power and high-efficiency sources, fast resists, defect-free and high-flatness masks, as well as related infrastructures. Development efforts in these areas are heavy. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties, remove restricted design rules, and provide manufacturing flexibility, is in an early-stage of development. Two pre-alpha tools are in the field. Progress has been made in demonstrating high-resolution imaging and CD control. Timing of manufacturing tools, costs, defects, overlay accuracy, and resists are other areas to further develop.

For 22-nm half-pitch lithography, water-immersion 193 nm scanners and double patterning will be severely stretched with extremely large mask error enhancement factor (MEEF), wafer line edge roughness (LER), and design rule restrictions. Resorting to more than two passes through the patterning tools can alleviate some of the above problems at the expense of higher costs. The numerical aperture of EUV systems will have to be raised to more than 0.36 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate per beam or more parallelism to maintain the increased pixel count within the same-size field. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications.

MASKS [LITHOGRAPHY]

The mask technology is becoming very expensive and challenging. Mask cost has escalated each generation. Increased resolution plus larger MEEF, due to higher levels of resolution enhancement technique (RET), make the mask CDU difficult to meet. Double and multiple patterning impose stringent requirement of mask pattern placement accuracy. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. EUV masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths. Actinic mask inspection and verification are eventually inevitable for EUVL. It further adds to the cost and complexity of the EUV mask infrastructure.

RESISTS [LITHOGRAPHY]

LER of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology-generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices. For EUVL, resist outgassing can contaminate the delicate reflecting optical surfaces. The tradeoffs between high resist sensitivity for throughput, low resist sensitivity for shot noise, and low LER, impose more problems than just resist collapse. E-beam resists also have to trade off for sensitivity and shot noise as well as LER. The sensitivity requirement is not as severe as that of EUVL.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. The inception of increasingly restrictive design rules aimed to promote design regularity have become mainstream as key enablers for near term scalable CD control. Line-edge-roughness (LER) has become also a critical element of device variability. Suppression of LER will continue to pose significant challenges to patterning processes (etch and lithography) as well to metrology in terms of accuracy and throughput. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm. Even lower permittivity dielectric has been introduced at 45 nm. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. The fast introduction of new metal/dielectric systems becomes critical. For low-κ dielectrics, the conventional approach is the introduction of homogeneous porous low-κ material. Reduction of κ damage due to Etch and CMP processes becomes more important with more porous materials. Another approach is air gap. It attracted attention because it keeps same low-κ materials with more volume of air gaps that gives lower effective κ. Among various techniques to incorporate air gaps, thermal or UV degradable sacrificial layer method is one of the low-cost approaches. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling. For the metal, fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary has become a key challenge. A very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. The low-κ material with good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures,

different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, and optimization tools for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. Driven by the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expand upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

CIRCUIT ELEMENT AND SYSTEM MODELING FOR HIGH FREQUENCY (UP TO 160 GHZ) APPLICATIONS

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS-, and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

FRONT-END PROCESS MODELING FOR NANOMETER STRUCTURES [MODELING AND SIMULATION]

Advanced USJ formation is critical to support continued scaling of device features. Millisecond anneal and SPER are expected to be widely used to reduce diffusion and enhance activation. Modeling capability and accurate calibration of the model parameters for dopant diffusion/activation and damage evolution during millisecond anneal and SPER will be critical. Since various channel materials will be required to further enhance mobility, such modeling will need to be done for various Si-based substrate including Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices. Such modeling will also need to account for additional factors, including, possible anisotropy in thin layers, co-implants and stress dependence, over layer influence including interface effects and the layer formation thermal process. Modeling of advanced implant technology such as use of molecular species for reducing damage will be needed. Epitaxial processes such as SiGe:C will be expanded to multi-channel devices with complex geometries, therefore, modeling of epitaxially grown layers including the shape, morphology will be useful to optimize such epitaxial processes. Extensive use of stress to enhance device mobility will continue. More accurate modeling of stress including material properties evolution during process such as plastic deformation during anneal, and stress relaxation due to defect generation will be needed. There will be continued needs for refining metrology / reverse modeling of USJ - 2D/3D doping/stress profiling to sufficient resolution to help calibration of simulation models and parameters. Devices are expected to largely deviate from quansi-2D and become 3D in nature, therefore more advanced 3D meshing to improve 3D computational efficiency and accuracy, especially for moving boundaries will be needed. Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces will be helpful in understanding nano-scale feature related effects. High-κ/metal gate is expected to be the basic building block, therefore modeling of High-κ/metal gate work function per charge and their reliability implications will be necessary.

COST-EFFECTIVE MANUFACTURING

DESIGN PRODUCTIVITY AND DESIGN FOR MANUFACTURING [DESIGN]

The number of available transistors double every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design to minimize performance/power variability, lithography-friendly designs (regular layout styles consistent with increasingly more restrictive design rules), and design for testability and reliability.

TEST COMPLEXITY [TEST AND TEST EQUIPMENT]

The complexity of next generation technologies is further convoluted by design and process interaction, which imposed challenges in yield learning for production ramp. Actual device characteristics on silicon could be dependent on layout environment and difficult, if not impossible, to be fully captured by model. As a consequence, the occurrence of abnormal product behavior either hard defect or parametric shift related is expected to worsen. The effectiveness and efficiency of test and analysis of product failure becomes the gating factor for yield ramp. Although the field of semiconductor failure analysis moves along with technology advancement, more effort is required to shortening the cycle time from product failure to root-cause fix by process or design. The areas for further improvement includes new equipment, methodology and software for (1) effective localization by DFT scan diagnostics and BIST, (2) physical failure analysis techniques, and (3) efficient implementation of refined DFM solution.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. Design for test innovations, widespread use of structural test techniques such as scan testing, and the enabling of higher levels of test parallelism have been very successful in keeping test costs in check to date. However, new test requirements for increasingly complex devices, testing for yield learning, increasing quality requirements, and practical limits on parallel testing continue to present great challenges to test cost. In particular, test tooling cost including probe cards are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. Automation of generation entire test programs for automatic test equipment (ATE), convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Wide ranging business models beyond the integrated device manufacturer (IDM) such as the fabless and foundry model, joint venture, and the variety of task sharing and out-sourcing scenarios have become pervasive in response to customers' rapidly changing complex business requirements. Furthermore, diversified customers' requirement on SoC devices have placed strong demand on manufacturing environments to rapidly and efficiently adapt to high-mix and low-volume product runs. These requirements continue to pose critical near-term challenges in several areas such as integration of larger numbers and different types of equipment, software applications, and fully featured software systems to manage the factory complexity while enabling decreasing time to ramp high volume production.

Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge. Continuous improvements to model factory capacity and performance to optimize output, improve cycle time, and reduce cost are key to successful high-mix factory operations.

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

Enhanced tool availability, improvements in material handling automation and systems for operational flexibility and control; single-wafer manufacturing; and the reduction/elimination of non product wafers (NPW); are representative areas for continuous improvement in 300 mm lines to meet the challenges of cycle time and cost reduction. The transition from

300 mm to the next wafer size (i.e., 450 mm) is another critical challenge for the semiconductor industry in the 2014–2016 time frame. This transition is considered critical to simultaneously meet the 30% cost/die reduction and a 50% improvement in cycle time.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

"More than Moore" is driving rapid change in packaging technology. Everything is changing: architectures, materials, processes, and equipment. Many new materials have been introduced in IC packages and more new materials will be continuingly introduced in the next few years in order to meet requirements of environmental regulations; to improve package performance; and to be compatible with low-k dielectrics used in Cu interconnects with 45 nm half pitch and beyond. Nano-materials present significant opportunities for the packaging community. 3D/SiP packaging requirements are stimulating new technologies: stacked die, wafer level packaging, through silicon vias, passive network interposers, embedded components, wafer thinning, wafer-to-wafer bonding, die-to-wafer bonding, and new materials. For automotive packaging, the rapid growth in hybrid and electric vehicles brings an additional class of electronics and a new subset of environmental conditions.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation. As such, near-term challenges - include emissions reduction from processes using chemicals classified as having significant global warming potential (GWP), the complete transition to lead-free packaging, and the need for a robust and rapid assessment of new materials/chemicals critical to surmount technology roadblocks while complying with ESH requirements

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently. Continuous improvement is needed in chemicals and materials utilization and energy consumption reduction in facilities and processing equipment, as well as in efficient thermal management of clean rooms.

DETECTION OF MULTIPLE KILLER DEFECTS AND SIGNAL-TO-NOISE RATIO [YIELD ENHANCEMENT]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends; however challenges arise in terms of efficiently and cost-effectively differentiating defects of interest (DOI) from a vast amount of nuisance and false defects. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation. Increasing aspect ratios and interconnect complexity will continue to pose increasingly difficult challenges and also opportunities to inspection tools development.

LAYOUT STYLE AND SYSTEMATIC YIELD LOSS: HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

Random logic areas are very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Solutions exist but need continuous improvements. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel are known to cause yield problems. Development and continuous improvement in terms of defect detection, throughput, and cost of ownership (CoO) of wafer edge and bevel defect inspection tools are increasingly critical to yield enhancement in advance device technologies.

FACTORY-LEVEL AND COMPANY-WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules and ever increasing aspect-ratio levels

MEASUREMENT OF COMPLEX MATERIAL STACKS, INTERFACIAL PROPERTIES, AND STRUCTURES [METROLOGY]

Metal-gate high-κ gate stacks, advanced strain and mobility enhancement techniques, as well as advanced interconnect and low-κ dielectric structures require novel or continuous improvement of measurement methodologies and standards in terms of critical dimensions (film thickness, feature sizes, LER, etc.), materials' physical properties (e.g., strain), and electrical properties including interface characteristics (e.g., workfunction, interface states, etc.). Metrology of film stacks for both front-end and back-end generally provide average physical or electrical property behavior from large area test structures. Therefore, new metrology techniques capable of characterizing stack structures at near nominal dimensions are also needed in the near term.

CRITICAL METROLOGY CONSIDERATION—PRECISION AND UNCERTAINTY [METROLOGY]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term "precision" is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool, and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

LITHOGRAPHY METROLOGY [METROLOGY]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

IN THE LONG TERM (~2017 THROUGH 2024)

ENHANCING PERFORMANCE

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness, and threshold voltage. This presents severe challenges in light of both technology scaling and variability. Off-currents in low-power devices increase by a factor of 10 per generation, and will emphasize a combination of drain and gate leakage components. Therefore design technology must be the key contributor to maintain constant or at least manageable static power.

IMPLEMENTATION OF NON-CLASSICAL CMOS CHANNEL MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND EMERGING RESEARCH DEVICES]

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to integrate physically or functionally onto a CMOS platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate which is challenging. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development

IDENTIFICATION, SELECTION, AND IMPLEMENTATION OF NEW MEMORY STRUCTURES [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND EMERGING RESEARCH DEVICES]

Line-dense, fast, and low-operating-voltage non-volatile memory will become highly desirable, and ultimate density scaling may require three-dimensional architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness (EOT) and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Line edge roughness, trench depth and profile, via sidewall roughness, etch bias, thinning due to cleaning, CMP effects, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. Etching, cleaning, and filling high aspect ratio structures, especially low-κ dual damascene metal structures and DRAM at nano-dimensions are also big challenges. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo-mechanical effects. Novel/active devices may be incorporated into the interconnect lines. Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets is a key challenge.

RESIST MATERIALS [LITHOGRAPHY]

Limits of chemically amplified resist sensitivity come after 22 nm half pitch due to acid diffusion length. With aggressive scaling of devices, the required gate CD control comes down to 1.5 nm in 3σ with a line width reduction (LWR) of less than 1.4 nm in 3σ in 2016 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) New resist materials with improved dimensional, LWR control and low defect density in less than 10 nm size are necessary. Resist and antireflection coating materials composed of alternatives to PFAS compounds are expected for future ESH concern.

TRANSITION TO NOVEL STRUCTURES FOR BOTH CMOS AND MEMORY DEVICES [FRONT END PROCESSES]

Several scenarios coexist for keeping continued scaling of CMOS and memory devices. It is anticipated to proceed with scaling (equivalent scaling), by introducing new materials, new structures, and/or 3D integration. Among all, the selection of a fundamental structure for CMOS is very challenging, for example, a channel material and a multi-gate structure will require new process technologies to be concurrently developed. These technologies include starting materials, surface preparation, lithography, pattern etching, and gate stack with booster technique, doping, metrology, process uniformity, and reliability. Once selected, there is no going back. Coordination and discussion are needed in all aspects among ITWGs viewed from process integration and manufacturing. In the memory area, charge-based devices are facing physical limits such as variability and cross-talk. In order to maintain scaling trends in both cost and functionality, innovative technologies will be needed by realizing new data-storage mechanisms or cost-effective 3D integration.

NON-DESTRUCTIVE, PRODUCTION WORTHY WAFER AND MASK-LEVEL MICROSCOPY [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. The combination of high-resolution optics, waveform analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement including sidewall shape and trench structures of damascene process. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

SYSTEM-LEVEL DESIGN CAPABILITY TO INTEGRATED CHIPS, PASSIVES, AND SUBSTRATES [ASSEMBLY AND PACKAGING]

Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Embedded passives may be integrated into the “bumps” as well as the substrates.

MATERIALS TECHNOLOGIES [EMERGING RESEARCH MATERIALS]

There are many challenges to define, prioritize, and reach consensus to recommend potential solutions that will deliver materials with controlled properties. Furthermore these properties must be defined in sufficient detail to enable ultimately to transfer to the Process and Integrated Device Structures (PIDS) teams in a timely fashion for further pragmatic research and development. These properties must be able to describe the operation of emerging research devices in high density at the necessary nanometer scale of the long-range roadmap timing horizon and beyond. In order to improve control of material properties for high density devices, research on materials synthesis must be coordinated and integrated in parallel with work on new and improved metrology and modeling.

POST-CONVENTIONAL CMOS MANUFACTURING UNCERTAINTY TECHNOLOGIES [FACTORY INTEGRATION]

Uncertainty of novel device types replacing conventional CMOS, and the impact of their manufacturing requirements, will have a big influence on a factory design. Due to the timing uncertainty of the industry to identify and develop new devices, and to create new evolutionary and disruptive process technologies, there is a need to model and design next-generation factories for a wide spectrum of flexibility. Such future factories must have the ability and flexibility to be implemented through early development phases and into production just in time for low risk industry transitions; and also taking into account the potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and with cost efficiency. These are huge industry challenges to simply imagine and define and also for the Factory Integration resources to implement.

COST-EFFECTIVE MANUFACTURING

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Computational material science tools need to predict materials synthesis, structure, properties, process options, and operation behavior for new materials applied in devices and interconnects. Especially needed are modeling of: gate stacks; predictive modeling of dielectric constant; bulk polarization charge; surface states; phase change; thermo-

mechanical (including stress effects on mobility); optical properties; reliability; breakdown; leakage currents (including band structure); and tunneling from process/materials and structure conditions. Novel integration in 3D interconnects needs modeling of airgaps; and data is also needed to model ultrathin material properties, and new ultra-low-κ (ULK) materials (whose models must also able to predict process impact on their inherent properties). Modeling-assisted metrology needs to link between: first principle computation; reduced models (classical MD or thermodynamic computation); and metrology (including ERD and ERM applications). Accumulation of databases for semi-empirical computation is becoming increasingly important.

IN-LINE DEFECT CHARACTERIZATION AND ANALYSIS [YIELD ENHANCEMENT]

Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

COST CONTROL AND RETURN ON INVESTMENT [LITHOGRAPHY]

Extending lithography to beyond 22 nm half pitch requires the introduction of new lithography technologies such as Extended-Ultraviolet Lithography (EUVL) or new techniques such as multiple patterning. All of these techniques introduce large changes into the single exposure immersion lithography process, targeted presently for the 32 nm Flash Poly uncontacted half-pitch and the 45 nm DRAM contacted M1 half pitch technology cycle. Therefore, achieving constant/improved ratio of exposure-related tool cost to throughput might be an insoluble dilemma. Mask costs are a significant component of lithography costs even up to high mask usage, so development of cost-effective post-optical masks is necessary. Also cost effective lithography systems are expected for the upcoming 450 mm wafer generation manufacturing.

TEST FOR YIELD LEARNING [TEST AND TEST EQUIPMENT]

Test's peripheral role as a feedback loop for understanding underlying defect mechanisms, process marginalities, and as an enabler for rapid fabrication process yield learning and improvement has traditionally been considered a secondary role to screening hard defects. With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficacy, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of Design-for-Test (DFT) and test-enabled diagnostics and yield learning becomes paramount. In other words, the yield learning rates of the past process generations are not sustainable by historical fault isolation and failure analysis methods per se. Rather, they need to be augmented by more universal deployment of enabling on-die circuitry (DFT, etc.) across and throughout products, as well as improvements in the on-die instrumentation and diagnostic software tools with respect to fault isolation specificity. Where it may have been sufficient to isolate to failing bit in an array or failing gate in logic in the past, there is a real business need to be able to isolate electrically to at least the failing transistor or interconnect in the future, or suffer the economic consequences of reduced yield improvement learning rates on new process technologies, perhaps even to the point of lowering the asymptotic maximum achievable yields per die size on future processes.

SUSTAINABILITY AND PRODUCT STEWARDSHIP [ESH]

Business considerations and also sustainability metrics (in a cost-effective and timely way) are required for product stewardship. In addition, Design for Environment, Safety, and Health (DFESH) should become an integral part of the facility, equipment, and product design as well as management's decision-making. Environmentally friendly end-of-life reuse/recycle/reclaim of facilities, manufacturing equipment, and industry products are increasingly important to serve both business and ESH needs.

AC POWER SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

While the DC power is controlled by I_{off}, off current, the AC power is largely dependent on Vdd, supply voltage. Due to the fact that Vdd cannot be scaled effectively in order to attend adequate drive current for the requirement of speed, the power density and total power continue to climb. Alternate channel materials are required to provide potential solutions.

MEETING THE FLEXIBILITY, EXTENDIBILITY, AND SCALABILITY NEEDS OF A COST-EFFECTIVE, LEADING-EDGE FACTORY [FACTORY INTEGRATION]

Ability to load the fab within manageable range under changeable market demand and to utilize task sharing opportunities such as manufacturing outsourcing is required to keep the manufacturing profitable. Enhanced customer

visibility for quality assurance of high reliability products including manufacturing outsourcing continues to challenge. Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] promotes reuse of building, production and support equipment, and factory information and control systems across multiple technology generations. Cost and task sharing scheme is highly expected on industry standardization activity for industry infrastructure development such as data standardization and visualization methodology.

WHAT IS NEW FOR 2009— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS

In 2009 the System Drivers teams made the following updates to the System Drivers chapter:

- Updated in detail the SoC Consumer drivers to indicate the reasoning and detail of the updates in the section itself, relevant to key parameters such as power consumption.
- Other updates have been also included as necessary maintenance and evolution.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions

Table ITWG1 Major Product Market Segments and Impact on System Drivers (continued)

IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

DESIGN

In 2009 the Design teams made the following updates to the Design TWG chapter:

- Started a resilience / reliability roadmap. We have consequently added text to (a) crosscutting challenges (b) DFM section (c) other scattered spots elsewhere in the Design Chapter – for this new topic, attached to reliability.
- Updated crosscut text from Modeling and Simulation
- Overhauled the DFT section, thanks to a collaboration from our colleagues in the Test chapter. There is a new DFT challenges table (see spreadsheets). We have deleted DFT solutions table. There is new DFT section text.
- Updated the ORTC power consumption challenge.
- Extended all key tables and figures until the 2024 year, consistent with the rest of the 2009 roadmap.
- Added requirements (rows) in the system level section tables to indicate the impact of system level design versus lower level design, on power reduction.

Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 32 nm	*Summary of Issues*
Design productivity	System level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/layout: analog circuit synthesis, multi-objective optimization
Power consumption	Logic/circuit/layout: dynamic and static (leakage), system and circuit, power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/layout: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/layout: signal integrity analysis, EMI analysis, thermal analysis
Challenges <32 nm	*Summary of Issues*
Design productivity	Complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	SOI power management
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test
EMI—electromagnetic interference ESL—Electronic System-level Design HW/SW—hardware/software
MTTF—mean time to failure SOI—silicon on insulator

TEST AND TEST EQUIPMENT

The 2009 edition of the Test Roadmap contains some significant changes to many of the tables; includes a new section on Adaptive Test; includes some discussion of 3D silicon devices; and added accelerometers to the Specialty Devices section. A survey on Cost of Test was completed in 2009 and the results are included in the Cost of Test Focus topic section. The high speed interfaces section was heavily updated. Other sections of the chapter contain only minor revisions.

Adaptive test has been being adopted as a method to reduce overall product test cost and improve product yields. The Test chapter now devotes an entire section to adaptive test concepts, challenges, impact to engineering and factory methodology, IT infrastructure requirements; and some implementation examples.

3D (Three Dimensional) silicon devices have been added to the key drivers for 2009. The concept of 3D devices is that a single design is implemented across multiple die connected by TSVs (Thru Silicon Vias) in order to optimize the cost and performance of devices. The SoC methodology of integrating a very complex system on a single chip can require many mask layers to be added to a technology to accommodate the requirements of the SoC. The 3D concept allows each die domain to be process optimized (i.e. Logic, DRAM, NVM, Analog), but introduces design and test complexities.

The test parallelism table has remained controversial even though new device categories have been added since 2005, so typical functional pin count assumptions have been added as notes. However, as many devices are being tested at wafer probe using reduce pin interfaces; all possible parallelisms cannot be included in the table.

The SoC table has been revised to reflect the latest trends and the chapter section has been appropriately changed. Formulas based changes in the Logic Table reflect the impact of the 2009 MPU and Consumer transistor count changes in the ORTC tables. Memory changes were also driven by the 2009 ORTC density roadmap.

Carrier frequency range in the RF table has been broken into general and special radio categories and the rapid increase in modulation bandwidth required for technologies such as UWB has moved out in time. The remainder of the table reflects small changes in numeric values and some cell color changes.

Prober, probecard, Handlers and test socket tables have had significant changes. The prober table has had a near complete rewrite, so changes are not easily summarized. Probecards now reflect a special LCD display driver probe requirements section to specify the unique challenges of testing these devices. Handlers broke the high power (>10W) device requirements into a med-hi (10-50W) range and a high range (>50W). Test sockets now covers blade rubber contacts and also included a table showing socket self-inductance must be reduced below 0.3nH to properly support 6GHz; and below 0.1nH for support of 20GHz signals.

There were either no changes, or only cell color changes or small numerical changes to the Vector multiplier, Mixed Signal, Burn-in and Probing difficult challenges tables.

2010 DIRECTIONS

Only tables will be updated for the 2010 roadmap, but the team will be preparing for the 2011 update which will include high speed test challenges, DFT enhancements and an update to the SoC and 3D device sections.

KEY TEST DRIVERS, DIFFICULT CHALLENGES, AND OPPORTUNITIES

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth (# of signals and data rates) Increasing device integration (SoC, SiP, MCP, 3D packaging) Integration of emerging and non-digital CMOS technologies Complex package electrical and mechanical characteristics Device characteristics beyond one sided stimulus/response model 3 Dimensional silicon - multi-die and Multi-layer Multiple I/O types and power supplies on same device
Increasing test process complexity	Device customization during the test process "Distributed test" to maintain cost scaling Feedback data for tuning manufacturing Dynamic test flows via "Adaptive Test" Higher order dimensionality of test conditions
Continued economic scaling of test	Physical limits of test parallelism Managing (logic) test data and feedback data volume Defining an effective limit for performance difference for HVM ATE versus DUT Managing interface hardware and (test) socket costs Trade-off between the cost of test and the cost of quality Multiple insertions due to system test and BIST
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	Implementation challenges and efficacies of burn-in, IDDQ, and Vstress Erratic, non deterministic, and intermittent device behavior
Potential yield losses	Tester inaccuracies (timing, voltage, current, temperature control, etc) Over testing (e.g., delay faults on non-functional paths) Mechanical damage during the testing process Defects in test-only circuitry or spec failures in a test mode e.g., BIST, power, noise Some IDDQ-only failures Faulty repairs of normally repairable circuits Decisions made on overly aggressive statistical post-processing
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

PIDS has three main sections: Logic, Memory (DRAM and Non-Volatile Memory), and Reliability. Major changes are listed under each section heading below.

LOGIC

- Recent surveys and literature indicate that the gate-length scaling has been/will be less aggressive than the past roadmap predictions. Realignment for this effect was the major change in the ITRS 2008 Edition. Reiterating that change in 2008 in comparison to that in 2007, the physical gate length L_g scaling for HP logic is slowed down by three to five years, with a change of slope. It is also observed that with the new L_g scaling model, the *CV/I* speed metric has a slope of ~13% increase per year instead of 17%. Similar changes were made to LOP technology whose physical gate length had a slow-down of one to three years, also with a change of slope. In this 2009 Edition, a minor adjustment of one-year slow-down is made compared to the 2008 Edition for most logic devices.
- Ring oscillator delay is added besides *CV/I* as a more realistic speed metric. Both fan-out of 1 and fan-out of 4 are included.
- In order to simulate a CMOS inverter in a ring oscillator, the saturation current of *p*-channel MOSFET is added. All other parameters are assumed symmetric to those of *n*-channel MOSFET.
- The subthreshold source-drain leakage currents are held constant independent of years. The values used for HP, LOP, and LSTP are 100 nA/μm, 5 nA/μm, and 50 pA/μm respectively.
- The criterion for source/drain parasitic resistance is set for degradation of 33% (1/3) of saturation current compared to an idealized case without any series resistance.

MEMORY: DRAM

- Smaller cell size of $4F^2$ is introduced, starting in 2011.
- Total bit size per chip is shifted later by 1 year.

MEMORY: NON-VOLATILE MEMORY (NVM)

- Transition from floating-gate type to charge-trapping type is delayed by 2 years, to 2012.
- 3-D charge-trapping flash is delayed by 1 year to 2014.
- Transition from 3-bit/cell to 4-bit/cell is delayed by 2 years, to 2012.
- NAND flash half-pitch is pulled-in by 1 year.
- Spin-torque-transfer MRAM table is added.

RELIABILITY

- Major correction in the reliability requirement specifications.
- Increase emphasis on circuit impact of device reliability issues. Bring up the need for paradigm change and the challenges involved.

DIFFICULT CHALLENGES

Table ITWG4 Process Integration Difficult Challenges.

Difficult Challenges for $L_g \geq 16$ nm	*Summary of Issues*
1. Scaling of logic MOSFETs	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain
2. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectric Low leakage in access transistor and storage capacitor Low resistance for bit and word lines to ensure desired speed Improve bit density and to lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
3. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Non-scalability of tunnel dielectric and interpoly dielectric in flash Difficult lithography and etch issues with pitch scaling Maintain high gate coupling ratio in floating-gate flash
4. Reliability due to material, process, and structural changes	Threshold voltage shifts due to traps, carrier injection, and program/erase cycling in memory cells Mobility degradation due to mechanical stress relaxation or interface states New or changed failure mechanisms resulting from high-κ/metal gate and new doping/activation processes New failure mechanism resulting from fundamental length scales or new device structures Process variability
Difficult Challenges for $L_g < 16$ nm	*Summary of Issues*
1. Implementation of advanced non-classical CMOS structures	Advanced non-planar multi-gate MOSFETs below 10 nm gate length Control of short-channel effects Drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Implementation of non-classical CMOS channel materials	Identification and demonstration of alternate channel materials New issues from materials, devices, and processing Integration of alternate channel materials on Si platform
3. Identification and implementation of new memory structures	Density and voltage scaling of NVM 3-D integration of NVM Implementing non-charge-storage type of NVM Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions
4. Reliability of novel devices, structures, materials, and applications	Reliability characterization of new devices Dealing with fluctuations and statistical process variations Impact of microscopic physical effects Need for Design for Reliability tools
5. Power scaling	V_{dd} scaling Controlling subthreshold current
6. Beyond CMOS	Identification and implementation of non-CMOS devices and architectures Integration onto Si-CMOS platform See ERD and ERM chapters for more discussions and details

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

OVERVIEW

- Micro-electro-mechanical systems (MEMS) now are treated in a separate technology section of the RF and AMS roadmap. In 2007, they were part of the More-than-Moore Section
- 3-D integration trends are affecting many RF and AMS technologies.

RF AND AMS CMOS

- Many product families skip nodes entirely when migrating to new application versions.
- Power-management and analog are being supported by optional devices since perhaps the 90 nm node.
- Millimeter-wave CMOS technologies are now discussed in the mm-wave section

RF AND AMS BIPOLAR DEVICES

- High-speed (HS) HBTs underwent a major update for the 2009 RFAMS roadmap to reflect higher f_{MAX} / f_T ratios.
- High-voltage (HV) HBTs were removed from the table for this section
- High-speed (HS) PNP transistors are now included in this section.
- Power-amplifier (PA) HBTs were update to anticipate changes in battery-voltages.

ON-CHIP AND OFF-CHIP PASSIVES FOR RF AND AMS

- On-chip: 3D integrated circuits enable improved performance of passive devices.
- Off-chip: The section now includes inorganic substrate roadmaps to reflect 3D integration and passives-only integration.

POWER AMPLIFIERS (0.4 GHZ–10 GHZ)

- This section addresses four major trends in handsets - 1) Drive to lower end-of-life battery voltage, 2) More complex biasing schemes, 3) Low-cost markets driving CMOS Pas, and 4) Growing number of modes supported by PA modules.
- It also addresses two major trends in basestations – 1) Due to the increasing use of GaN, discussions on GaAs were removed from the section and 2) The use of very-efficient architectures is increasing.

MILLIMETER WAVE (10 GHZ–100 GHZ)

- The parameter for maximum current (Imax) was removed as a technical requirement in the tables for low noise devices.
- Maximum available gain] (MAG) predictions at 60 and 94 GHz were added to the SiGe HBT and CMOS tables.
- The prediction for the production of mm-wave GaN power HMETs was delayed to 2010.

MEMS

- The roadmap for 2009 now includes bulk acoustic wave (BAW) devices, resonators, and both metal-contact and capacitive-contact switches.
- The roadmap acknowledges other emerging MEMS devices such as gyroscopes, accelerometers, microphones, and displays and growing interests in sub-THz applications.
- There remain needs to develop appropriate quantitative metrics in tables such as insertion loss and tuning ratio for capacitive-contact switches and other key metrics per device or area.

DIFFICULT CHALLENGES

Table ITWG5 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
CMOS	New materials (e.g., high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes) make predicting trends uncertain for transistor mismatch and for 1/f noise.
Bipolar HS-NPNs and HS-PNPs transisters	Increasing f_T by more aggressive vertical profiles and still maintaining acceptable figures of merit, manufacturing control, and punch-through margins
Bipolar Power Amplifiers	Improving the trade-off between f_T/f_{MAX} and breakdown voltages to provide acceptable voltage handling and power densities at performance levels that can effectively complete with alternative technologies.
On-Chip Passive Devices	Integrating new materials in a cost-effective manner to realize compact and high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap for increased RF performance.
Off-Chip Passive Devices	The large number of options for embedded passives increases complexity and cost. And accurate models for process tolerance and parasitic effects and computer assisted design (CAD) tools.
Handset Power Amplifiers	Increasing functionality in terms of operating frequency and modulation schemes and simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
Base-station Power Amplifiers	Enhancing performance with continual product-price pressure. And Improving amplifier efficiency.
mm-Wave Devices	Thermal management for high power density circuits, multi-level integration and E/D mode transistors. And reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
MEMS	Incorporating the great process diversity of MEMS into specific ITRS processes. And developing design tools, packaging, performance drivers, and cost drivers for each MEMS device type.

EMERGING RESEARCH DEVICES

The 2009 edition of the Emerging Research Devices chapter evaluates emerging research logic and memory devices, proposed for two different scenarios, complemented by a re-directed section discussing architectural opportunities. One scenario addresses charge-based devices and technologies for extending CMOS scaling to the end of the Roadmap. The other explores "Beyond CMOS" devices for complementing and enhancing CMOS by, for example, performing synergistic accelerator functions in the nearer term, and, eventually, for supplementing CMOS in a new information processing paradigm. For example, research on MOSFETs employing an alternate channel material (Ge or III-V Compound Semiconductor) has made substantial progress in the past two years and is beginning to show significant potential for sustaining performance scaling of CMOS to the end of the Roadmap. Similarly, a "Beyond CMOS" device could potentially use particle spin to perform non-volatile memory and logic functions on a CMOS chip, or could perform an information processing function utilizing spin waves.

Connecting these two scenarios, the 2009 ERD chapter features a particular emerging research information processing technology, carbon-based nanoelectronics, which exhibits high potential and is maturing rapidly. Carbon-based nanoelectronics, including carbon nanotubes, graphene, and graphene nanoribbons, was chosen because of its potential performance advantages when applied to MOSFETs and the rich physics it enables for realizing a new information processing device.

Several new research technologies are emerging for non-volatile random access memories offering potential for dense, high speed and lower power memory devices. Operation of most of these technologies is based on employing a resistive element for storing binary data. Leading candidates include the Spin Transfer Torque RAM, the Nanothermal RAM (i.e., PCM and Fuse/Antifuse), and the Nanoionic RAM (i.e., Atomic Switch and Memristor). Of particular interest are those technologies capable of being scaled to and beyond the 16 nm generation. Two other memory technologies, Nanocrystal Memory and Engineered Tunnel Barrier Memory, tracked and evaluated by ERD through several previous editions, have reached sufficient potential and maturity to be transferred to PIDS and FEP for their treatment in 2009.

The Architecture section has been re-directed and expanded to include new activities for benchmarking emerging research logic and information processing devices, a new memory architecture section, a new example of processing using a Bayesian inference network, and a new analysis of limits. These are summarized below:

1. Benchmarking— The Nanoelectronics Research Initiative (NRI) has begun developing a new methodology for benchmarking the performance of nineteen alternative information processing devices on both Boolean and special purpose logic operations. The Boolean logic operations are parameterized in terms of energy and delay for three selected logic gates. These methods are currently being further developed and applied to compare disparate device technologies. Results of this benchmarking analysis are planned for publication when available, tentatively next year.
2. Memory Architecture is discussed in the context of using new memory technologies to reduce the substantial energy dissipation inherent in current memory technologies
3. An example of a Bayesian inference network is discussed to illustrate the potential of merging one or more Beyond CMOS devices with a completely new architecture to extend information processing into scaling, power, and performance domains beyond that attainable by ultimately scaled, end-of-the-roadmap CMOS.
4. A new thermodynamic analysis of limits is outlined in which the physics of an emerging research device in the Boltzmann-Heisenberg limit is connected to the parameters of digital circuits implemented using these devices. The proposed methodology should be extensible to estimate the optimal achievable performance for information processors implemented in that technology.

DIFFICULT CHALLENGES

Difficult challenges related to emerging research devices, as shown in the table below, are divided into those related to memory technologies and those related to information processing or logic devices. One challenge is the need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with CMOS process flow scaled to and beyond the present limits of SRAM and FLASH, 22–16 nm. A related challenge is to sustain scaling of CMOS logic technology beyond 16 nm.

Table ITWG6 Emerging Research Devices Difficult Challenges

Difficult Challenges ≥ 16 nm and < 16 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond the 16 nm technology generation.	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel and source/drain to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in t
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development

EMERGING RESEARCH MATERIALS

The 2009 Emerging Research Materials (ERM) chapter is an updated version of the 2007 ITRS ERM. The 2009 ERM Chapter has been reorganized to review material for specific applications, while the 2007 ERM reviewed materials and discussed their potential applications to future roadmap needs. The 2009 ERM reviews materials for ERD Logic and Memory applications, lithography including novel resist, front end process and process integration and devices applications, interconnects, and assembly and package applications. The ERM chapter also identifies metrology, modeling, and environmental safety and health research needed to support these materials for their potential applications. While these ERMs have properties that make them attractive as potential solutions to future technology needs, significant progress is required for them to be adopted in future technologies.

In addition to restructuring the ERM to focus on applications, several new applications and materials are included. Materials for Emerging Research Devices includes materials for Logic including "Alternate Channel Materials (that includes a critical assessment of Ge, III-V, graphene, carbon nanotubes, and nanowires), "Materials for Charge Based Beyond CMOS Devices," and "Materials for Noncharge based Beyond CMOS," and a new section on Materials for Memory. Lithography Materials has been expanded beyond Materials for Directed Self Assembly" to also include a materials for non-evolutionary 193 nm and EUV resist materials including non chemically amplified resist (Non-CAR), negative tone resist, materials for pitch division, novel EUV approaches including negative tone cationic, negative tone Non-CAR, inorganic-organic hybrids, and other Non CAR materials. Materials and Processes for Front End Processes reviews a number of technologies for deterministic dopant placement and directed self assembly materials for selective etch, clean and deposition processes. Interconnect materials now includes a review of potential ultrathin Cu barrier layers and low κ ILD materials to extend Cu interconnects, as well as single wall and Multiwalled carbon nanotubes and single crystal nanowires for via and interconnect replacements. Assembly and Package Materials reviews nanometals for low temperature solders and anisotropically conducting interconnect materials, carbon nanotubes for high current chip to package interconnects, and the use of nanoparticles and macromolecules to deliver package polymers to meet the multiple conflicting properties required for application to underfill, mold compound, and multiple adhesive applications.

The ERM and ERD chapters also highlight the need for an increased focus on carbon based (i.e. carbon nanotubes and graphene) electronics for potential application as alternate channel materials and for potential application to Beyond CMOS applications, based on an assessment of Beyond CMOS technologies.

DIFFICULT CHALLENGES

The current set of sub-16 nm ERM Difficult Research Challenges is summarized in Table ITWG7. Perhaps ERM's most difficult challenge continues to be delivering material options, with controlled and desired properties, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the sub 20 nanometer scale and be extensible to nanometer scale. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled orientations. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties.

Table ITWG7 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤16 nm	*Summary of Issues*
Integration of alternate channel materials with high performance	III-V has high electron mobility, but low hole mobility
	Germanium has high hole mobility, but electron mobility is not as high as III-V materials
	Demonstration of high mobility n and p channel alternate channel materials co-integrated with high κ dielectric
	Demonstration of high mobility n and p channel carbon (graphene or carbon nanotubes) FETs with high on-off ratio co-integrated with high κ dielectric and low resistance contacts
	Selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers (III-V, Graphene, Carbon nanotubes and semiconductor nanowires)
	Achieving low contact resistance to sub 16 nm scale structures (graphene and carbon nanotubes)
	Ge dopant thermal activation is much higher than III-V process temperatures
	Growth of high κ dielectrics with unpinned Fermi Level in the alternate channel material
Control of nanostructures and properties	Ability to pattern sub 16 nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.)
	Control of CNT properties, bandgap distribution and metallic fraction
	Control of stoichiometry, disorder and vacancy composition in complex metal oxides
	Control and identification of nanoscale phase segregation in spin materials
	Control of surfaces and interfaces
	Control of growth and heterointerface strain
	Control of interface properties (e.g., electromigration)
	Ability to predict nanocomposite properties based on a "rule of mixtures"
	Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability
Controlled assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components
	Control of line width of self-assembled patterning materials
	Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials
	Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.)
	Characterization of spin concentration in materials
	Characterization of vacancy concentration and its effect on the properties of complex oxides
	3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties
	Characterization of transport of spin polarized electrons across interfaces
	Characterization of the structure and electrical interface states in complex oxides
	Characterization of the electrical contacts of embedded molecule(s)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures
	Device structure-related properties, such as ferromagnetic spin and defects
	Dopant location and device variability

FRONT END PROCESSES

In 2009, the FEP chapter has been restructured. The 2009 FEP chapter now starts with device-related Technology Requirements (logic devices, including high performance, low operating power, and low stand-by power; memory devices, including DRAM, flash, phase-change, and FeRAM) followed by the material and process Technology Requirements (starting materials; surface preparation; thermal/thin films/doping; plasma etch; and CMP). After studying current industry practice, and in consultation with ORTC, PIDS, Design, and other Technology Working Groups, the scaling rate of the logic physical gate length was further delayed by one-year, compared to the 2008 update.

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures. Continued scaling of planar bulk CMOS is becoming more and more difficult. As a consequence we must be prepared for the emergence of CMOS technology that uses non-conventional MOSFETs or alternatives such as planar FDSOI devices and dual- or multi-gate devices either in a planar of vertical geometry. An overview of the device alternatives is presented in the *Emerging Research Devices chapter*. Projections for the manufacturing introduction of non-conventional MOSFET devices are 2013–2015 for FDSOI and/or multi-gate. The challenges associated with integration of these diverse new materials and structures are the central theme of the FEP difficult challenges.

High-κ gate dielectric with metal gate electrode is in production. Continued scaling of equivalent oxide thickness (EOT) below 0.8 nm while preserving electrical performance and reliability, will be a challenge. Continued improvement in strain engineering and application to new device structures is identified as an FEP difficult challenge. The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. Series resistance is critical in the near term and needs to be addressed to achieve the goals through 2015.

In the memory area, stand-alone DRAM device manufacturing has narrowed to the stacked capacitor approach. Therefore, the Technology Requirements table and text for DRAM trench capacitor has been removed. A new requirements table has been added to address charge-trapping Flash technology scaling. FeRAM will make a significant commercial appearance where ferroelectric and ferromagnetic storage materials would be used. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In starting materials, it is expected that alternatives to bulk silicon such as silicon-on-insulator substrates will proliferate. An important difficult challenge expected to emerge within this 2009 Roadmap horizon is the need for the next generation 450 mm silicon substrate. Based upon historical diameter change cycles, the industry is already several years behind the pace necessary to allow the next generation 450 mm silicon substrate to be ready for device manufacture in the year 2014.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ dielectrics, metal gate electrodes, and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed.

The persistent challenge in scaling device sizes is the control of gate length critical dimensions (CD). As gate CD shrinks, the presence of line width roughness (LWR) is becoming the biggest portion of CD variation at 28 nm technology node and beyond. The LWR is at best staying constant as the line width shrinks, which makes it a major scaling concern. Current methods of quantification need to be standardized to allow the industry to address the problem. As non-planar transistors become necessary, etch becomes much more challenging. FinFET configurations bring new constraints to selectivity, anisotropy, and damage control.

Chemical-Mechanical Planarization (CMP) is becoming more important for Front End Processing and is being given specific consideration in the 2009 FEP Chapter for the first time. Uniformity, selectivity, and pattern density dependency continue to be challenges for CMP processes.

DIFFICULT CHALLENGES

Table ITWG8 Front End Processes Difficult Challenges

Difficult Challenges ≥ 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Strain Engineering - continued improvement for increasing device performance - application to FDSOI and Multi-gate technologies
	Achieving DRAM cell capacitance with dimensional scaling - finding robust dielectric with dielectric constant of ~60 - finding electrode material with high work function
	Achieving clean surfaces free of killer defects - with no pattern damage - with low material loss (<0.2 A)
	High-k/Metal Gate - introduction to full scale manufacturing for HP, LOP, and LSTP - scaling equivalent oxide thickness (EOT) below 0.8 nm
	450 mm wafers - meeting production level quality and quantity
Difficult Challenges < 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Lowering required DRAM capacitance by 4F2 cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued EOT scaling below 0.7 nm with appropriate metal gates
	Continued charge retention with dimensional scaling and introduction of new non-charged based NVM technologies

LITHOGRAPHY

It is becoming increasingly more difficult to extend optical lithography as we know it today. In 2010, flash devices will be manufactured using 32 nm half-pitch (hp) double patterning (DP) as a way of extending the half-pitch while keeping the NA and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm hp and flash starts to test the limits of optical solutions at the 22 nm half-pitch node in 2013. But it is at this point that an alternative next generation lithography (NGL) must be introduced into manufacturing to ensure a smooth transition into the lithography approaches beyond 22 nm.

At the 22 nm node, the international community that contributes to the ITRS saw four possible technologies that could be used and that could extend the roadmap out to 11 nm half-pitch. These were all ranked at each year for their desirability and feasibility as solutions. EUV lithography is the lead candidate because of its lower cost of ownership (COO). Second is extending 193 immersion double patterning down to a k1 of 0.15 for the 22 nm half-pitch node, followed by maskless lithography (ML2) and imprint lithography. Alpha and soon beta tools are being delivered to the semiconductor industry for evaluation and further development using all of these approaches. In many cases, the technology is not limited by the lithography tool, but rather by the supporting technologies.

DIFFICULT CHALLENGES < 22 NM VERSUS TECHNOLOGY

The difficult challenges moving into the NGL regime are many and are not just incremental improvements in the technologies that we know and understand. The technology options are still vast, and in many cases the technology and the supporting infrastructure technologies need significant inventions to approach the manufacturing stage. The Difficult challenges table for ≤22 nm shows the major challenges that must be solved to bring NGL technologies to the manufacturing stage. These challenges are listed in the order of perceived difficulty. For EUV lithography, three major components have long been flagged as needing substantial improvements. First is EUV source brightness/reliability. The leading contender for a bright EUV source has changed from discharge produced plasma (DPP) to laser produced plasma (LPP) in recent years, but the sustained proven power levels are still about 4 to 6× less than the power that is needed for manufacturing. The second is the EUVL resist system since specifications for resolution, linewidth roughness (LWR), and sensitivity must be achieved simultaneously at a low exposure dose. Additionally, each photon of EUV radiation has 15× more energy than a 193 photon. Thus the dose for exposure is achieved by 15× fewer photons, putting the image closer to the quantum noise limits. The third issue involves the EUV mask and the infrastructure that is needed to support it. A printing defect on this mask can derive not only from the traditional opaque defect in the patterning layer but also from small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. These phase defects are at the limits of today's metrologies and as such are very difficult to observe and improve upon. Currently, the infrastructure inspection equipment (substrate, blank, patterned mask, AIMs) needed for EUV mask manufacturing at the 22 nm node does not exist.

Maskless lithography is another NGL technology that must overcome major challenges before being considered a manufacturing technology. Foremost is the system throughput combined with the resist sensitivity that will also provide adequate LWR and resolution. This is both a system issue with respect to the e-beam flux and a resist material issue. The second most pressing concern is the inability to inspect wafer images at the same capability that we now have for 4× mask patterns. Inspection involves two issues: the resolution of the wafer inspection (at sufficient speed) and die-to-database inspection to ensure no systematic recurring defects are present.

Imprint lithography has three major needs: 1× masks, imprint materials, and imprint systems. The 1× mask has many areas contributing to difficult obstacles. First is mask inspection. The mask must be inspected to find defects in the 1× pattern that are just 10% of the width of the feature. An e-beam system might be able to do this but not at the speeds needed for manufacturing. Second is the write time to expose the slower speed e-beam resists to meet the LWR and CD specifications for 1× patterning. Third, 1× defect sizes are 4× smaller than what current 4× optical mask processes require; therefore, imprint template and e-beam resist patterning processes need to be developed to match these specifications. Another challenge is that the imprint materials must be of sufficiently low viscosity to be applied quickly for sufficient throughput. The last major challenge is with the imprint system. The lithography community believes that throughput, defect levels, and overlay all need a significant overhaul for the technology to be accepted in manufacturing.

Although there are many near-term challenges, the industry is addressing them. Lithographic systems are being made to run at throughputs that are about 2× the throughput of older steppers, thus addressing some of the COO issues associated with double patterning. Registration and overlay issues with lithographic mask patterning systems are also being

addressed to move double patterning into manufacturing. The industry is likewise addressing the fundamental challenges associated with the NGL technologies, in particular the EUV lithography and the mask infrastructure that is needed. With these gains, the lithography industry will be back on course for improving ROI into the future.

Table ITWG9A Lithography Difficult Challenges >22 nm

Difficult Challenges > 22 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features Registration, CD, and defect control for masks Eliminating formation of progressive defects and haze during exposure Understanding and achieving the specific signature and specifications for a Double Patterned mask Establishing a stable process so that signatures can be corrected.
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs Availability of high productivity scanner, track, and process to maintain low cost-of-ownership Photoresists with independent exposure of multiple passes Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time ROI for small volume products Resources for developing multiple technologies at the same time Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume 450 mm diameter wafer infrastructure
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error Controlling LER, CD changes induced by metrology, and defects < 10 nm in size Greater accuracy of resist simulation models Accuracy of OPC and OPC verification, especially in presence of polarization effects Lithography friendly design and design for manufacturing (DFM)

Table ITWG9B Lithography Difficult Challenges ≤22 nm

Difficult Challenges ≤22 nm	*Summary of Issues*
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm^2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm RMS figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion length Materials with improved dimensional and LWR control add (limits) Resist and antireflection coating materials composed of alternatives to PFAS compounds Low defects in resist materials (size < 10 nm) Line width roughness < 1.4 nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair) Mask process control methods and yield enhancement Cost control and return on investment
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput Development of cost-effective post-optical masks Cost effective 450 mm lithography systems Achieving ROI for small volume products
193 nm Immersion Multiple Patterning	Cost control and return on investment Wafer processing to tighter overlay and CD controls Mask fabrication to tighter specifications
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s Metrology for achieving < 2.8 nm 3s wafer overlay error Template inspection for 1× Imprint Patterned Masks Phase shifting masks for EUV
Gate CD control improvements and process control	Development of processes to control gate CD < 1.5 nm 3s with < 1.4 nm 3s line width roughness Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3s overlay error, especially for imprint lithography
Maskless Lithography	Wafer throughput Cost control and return on investment Die-to-database inspection of wafer patterns written with maskless lithography Pattern placement - including stitching Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free imprint templates at 1× dimensions Infrastructure for 1× technology templates (key here is inspection!) Template fabrication to tighter specifications Protection of imprint templates from defects without pellicles Mask life time Throughput Cost control and return on investment Overlay Process control methods to compensate for systematic CD and overlay errors

INTERCONNECT

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of the integrated circuit, along with providing necessary power and ground connections. For 2008, the scope has been expanded to include the contact level and continues up through the device from metal 1 through to the global wiring levels. Traditionally, global wiring delay has been the "Grand Challenge" and tackling delay generally, is still a primary focus.

The current approach of the 2008 Interconnect Technical Working Group (TWG) for addressing delay is to enable high-bandwidth low-power signaling solutions and a new table, INTC6 High Density Through Silicon Via Specification has been added. The group continues to project the use of copper as the primary conductor in a dual-damascene architecture; however, much of the work in progress focuses on the latest challenges and trends related to 3D integration and emerging technology.

- The Technology Requirements Table (INTC2) has been substantially revised and reorganized and divided into
  - general requirements – e.g., bulk resistivity and dielectric constant
  - level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-k roadmap – small slowdown
  - New range for bulk κ
  - Air gaps moved out of emerging sections – considered mainstream
  - Air gaps expected to be the solution for $\kappa_{bulk} < 2.0$
- Atomic layer deposition (ALD) barrier processes and metal capping layers for Cu are lagging in introduction – needed to meet sub 1 nm specifications
  - Hybrid barriers containing ruthenium are proliferating
- J_{max} current limit model show a width dependence – a new reliability concern
- Technology drivers expanded to support both traditional geometric scaling and equivalent scaling
  - Requirements for CMOS-compatible equivalent scaling are highlighted in an expanded *Emerging Interconnect Properties* section along with a new first principle consideration of interconnect properties for new (non-FET) switches
- Design and processing of three-dimensional chip stacking through the use of high-density through silicon vias (TSVs) is a key focus area to address delay and power concerns and a new TSV table has been introduced

DIFFICULT CHALLENGES

Table ITWG10 Interconnect Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 16 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

** Top three challenges*

CMP—chemical mechanical planarization DRAM—dynamic random access memory

FACTORY INTEGRATION

The Factory Integration ITWG identifies needed operational factory services and relevant technologies, and it updates the near term and longer term technology requirements and potential solutions to meet these requirements. FI ITWG has five thrust teams and their technology focuses are shown in the following table.

Functional Area	*Key technology focuses and issues*
Factory Operations (FO)	1) Systematic productivity improvement methodology prior to 450 mm insertion 2) Systematic factory waste visualization of cycle times and factory output losses
Production Equipment (PE)	1) 450 mm production tool development 2) Reliable and predictable equipment availability improvement
Material Handling Systems (MHS)	1) Reduction in average material delivery times 2) More interactive control with FICS and PE for accurate scheduled delivery
Factory Information and Control Systems (FICS)	1) Increased FICS reliability performance for more complex factory control 2) Enhanced system extendibility
Facilities	1) Enhanced extendibility for 450 mm and facility cost reduction 2) AMC management, electric static control on masks, wafers, and facility surfaces

2009 HIGHLIGHTS

The Factory Operations technology requirements table was updated so to accommodate *Next Generation Factory* (NGF) and *Waste Reduction Management* requirements with the new metrics introduction. The other FI thrusts' technology requirements tables were revised in accordance with the Factory Operations technology requirements table and their specific technology updates.

NGF TECHNOLOGY REQUIREMENTS INCLUSION

The FI focus areas activity concluded that a significant productivity improvement as NGF is to be promoted before 450 mm introduction. NGF is best described as systematic waste reduction approach that should facilitate comprehensive productivity improvement with the aid of proactive service visibility. NGF can be loaded with so-called 300 mm Prime mission as well. The industry can focus on common technology development for the current wafer diameters and 450 mm.

WASTE REDUCTION MANAGEMENT

Waste Reduction approach has been identified as the effective NGF driver. The ultimate goal for waste reduction is that all the technology requirements tables in the ITRS roadmap adopt waste reduction scheme, i.e., as a new driving axis in addition to the historic Si scaling cost reduction. Two high-level waste metrics have been introduced to promote this approach into Factory Operation technology requirements table. They are Factory WTW (Wait Time Waste) defined as a total sum of wait time for a wafer to go through all the process and Factory EOW (Equipment Output Waste) defined as opportunity loss of production calculated as normalized difference between instantaneous throughput and averaged throughput.

CROSS CUT ISSUES

Green Fab Initiative, Advanced Process Control, fab temperature and humidity control, single wafer versus batch processing for thermal processes and 450 mm cross-cut issues are reflected to the requirements and solutions tables.

FUTURE TREND AND FI ACTIVITIES

Systematic factory services requirements specific to 450 mm manufacturing should be captured as they become available. Onset of single wafer manufacturing is located for 2019 as an ultimate implementation of waste reduction. More understanding is needed for this manufacturing method. Waste Reduction Management needs to be comprehended extensively by ITRS and the industry. It is also required for the industry members to comprehend their own factory-level waste reduction requirements and come up with their own waste reduction roadmap. Green Fab Initiative should be understood from factory services so to have comprehensive set of FI requirements.

DIFFICULT CHALLENGES

Table ITWG11 Factory Integration Difficult Challenges

Difficult Challenges through 2017	*Summary Of Issues*
1. Responding to rapidly changing, complex business requirements	Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production) Rapid and frequent factory plan changes driven by changing business needs Ability to load the fab within manageable range under changeable market demand Enhancement in customer visibility for quality assurance of high reliability products
2. Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Increased requirements for high mix factories. Examples are (1) significantly short life cycle time of products that calls frequent product changes, (2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies Ability to model factory performance to optimize output and improve cycle time for high mix factories Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools Comprehending increased purity requirements for process and materials
3. Achieving growth targets while margins are declining	Ability to visualize cost and cycle time for systematic waste reduction from all aspects. Reducing complexity and waste across the supply chain Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	Increased impacts that single points of failure have on a highly integrated and complex factory More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing Design-in of equipment capability visualization in production equipment Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste. Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1]
5. Emerging factory paradigm and next wafer size change	Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost
Difficult Challenges Beyond 2017	*Summary of Issues*
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules Complexity of integrating next generation lithography equipment into the factory More comprehensive traceability of individual wafers to identify problems to specific process areas Comprehensive management that allows sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods
3. Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
4. Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

[1] Dandori operations: Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

ASSEMBLY AND PACKAGING

The rapid growth in three dimensional electronics, System in Package (SiP) and other new technologies that enable "More than Moore" has resulted in an accelerated pace of change in the Roadmap for Assembly and Packaging. There will be several sections added or expanded in the 2009 ITRS to address these emerging technologies. Several of these areas are initially addressed in the table changes for 2008.

The major changes include:

- Optical interconnect on chip and chip to chip within a SiP has been added as a volume technology in 2011.
- Modifications were made to Tables AP3 and AP4 to reflect changes in bonding pitch for specific technologies. In some cases driven by changes in demand rather than capability.
- A new table, AP4b was added to address the increasingly serious issues associated with warpage and its impact on assembly.
- Tables AP5a, AP5b and AP5c were altered to provide greater clarity for differences between the Roadmap for polymer package substrates and the glass-ceramic substrate used for certain high temperature device types.
- Table AP9 was restructured to provide quantitative projections to replace the qualitative information in the 2007 version of the table.
- Table AP10 has been modified to provide greater detail and has been segmented into the major process types.
- Table AP11 has been modified to incorporate changes in component sizes, reflow temperatures and other parameters that are changing to meet the requirements emerging package architectures such as SiP.
- Table AP15 has added Active Optical cables. This table and the associated text will see major revisions in 2009 reflecting the incorporation of optical interconnect in SiP and system interconnect.
- Table AP16 has been segmented by application in recognition of the different packaging challenges for different optoelectronic applications.
- Table AP19 is in the process of a major revision that will be incorporated into the 2009 ITRS.
- Table AP21: Automotive Operating Environment Specifications has been added. This material was treated in the text for 2007 but with the increase in electronic content including components for electric and hybrid cars it needs to be a numbered table. This topic will be substantially expanded in the text of the 2009 ITRS.

There are a number of other minor changes incorporated in the AP tables for 2008. The most important issues identified in this update are related to major changes already underway for the rewrite in 2009. They will incorporate a more detailed treatment of the materials, processes and design changes required to address the challenges of 3D electronics and the functional diversification of the "More than Moore" era.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG12 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥22 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ
Wafer level CSP	-I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design is needed now. -EDA for "native" area array is required to meet the Roadmap projections. -Models for reliability prediction
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
Thinned die packaging	- Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration

Table ITWG12 Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Close gap between chip and substrate Improved organic substrates	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for operation temp up to C5-interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology -Production techniques will require silicon-like production and process technologies after 2005 -Tg compatible with Pb free solder processing (including rework at260°C)
High current density packages	-Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
Flexible system packaging	-Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
3D packaging	-Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer via structure and via fill process -Singulation of TSV wafers/die - Test access for individual wafer/die -Bumpless interconnect architecture
Difficult Challenges <22 nm	*Summary of Issues*
Package cost does not follow the die cost reduction curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
High frequency die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz -“Hot spot” thermal management There is currently a “brick wall” at five-micron lines and spaces.
System-level design capability to integrated chips, passives, and substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the “bumps” as well as the substrates.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TSV—through silicon via

ENVIRONMENT, SAFETY, AND HEALTH

The four basic ITRS ESH Chapter strategies in 2009 remain as they were in the previous edition; namely: 1) Understand (characterize) processes and materials during the development phase; 2) Use materials that are less hazardous or whose by-products are less hazardous; 3) Design products and systems (equipment and facilities) that consume less raw material and resources and, 4) Make the factory safe for employees.

There is one additionally significant new element in 2009, which is the addition of ESH Categories. Previous ESH chapter tables presented a requirements set that related ESH concerns to the technical thrusts (e.g., Interconnect, Front End Processes, etc.). They also identified ESH concerns that are broader and more general than those pertaining to a single technology thrust (referred to as Intrinsic).

To focus available resources toward those areas of greatest added benefit, in addition to the ESH improvements gained, all ESH requirements have now been placed in one of three Categories:

1. *Critical*—Any requirement in this category is an essential item for technology success/implementation as well as ESH benefits. If not addressed, it could compromise the ability to insert the technology into manufacturing.
2. *Important*—Any requirement in this category is a key item for process success as well as ESH benefits. If not addressed, it could compromise the cost of ownership (CoO) of the technology in manufacturing, based on factors such as throughput, yield, and chemical/material and/or tool costs.
3. *Useful*—Any requirement in this category is a key item for ESH benefits ("best practices"), but without any clear additional factors that would place it in either of the above two categories. If not addressed, it could compromise the ability to achieve the lowest ESH impact for the technology when inserted into manufacturing.

Also new for 2009 is a table of all ESH requirements considered for the 2009 Roadmap sorted according to the following ESH domains for easy reference. These are *Restricted Chemicals, New Chemicals, Nanotechnology (*former subset of New Chemicals*), Utilization/Waste Reduction, Energy,* and *Green Fab.*

For 2010 one critical area for the ESH chapter will be to further refine needs in technical terms to efficiently incorporate impacts from ESH policy (government and public) on materials. This will be done by continued harmonizing of the ESH Categorization with technology requirements.

Other areas for 2010 emphasis will be Energy and Carbon Footprint (improving perspective for new technology role in energy conservation), improvements needed for the timely availability of Chemical Assessment Data and Methodologies, more in depth evaluation of potential 450 mm impacts and evaluation of how ESH requirements may differ between memory and logic roadmaps.

DIFFICULT CHALLENGES

Table ITWG13A Environment, Safety, and Health Difficult Challenges—Near-term

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. Given the global movement possible for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory/policy differences, and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use In addition, methods for anticipating and forecasting such future requirements are not well developed.. • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed, and can use improvement.
Process and equipment management	• *Process Chemical Optimization* There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be addressed. • *Global Warming Emissions Reduction*: There is a need to reduce emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation:* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization:* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of them and their process emissions and byproducts. • *Byproducts Management*: There is a need for improved metrology for byproduct speciation. • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE) • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes, and products. • *End-of-Life Reuse/Recycle/Reclaim:* There is a need to design facilities, equipment and products to facilitate these end-of-life issues

Table ITWG13B Environment, Safety, and Health Difficult Challenges—Long-term

Difficult Challenges < 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed.
Process and equipment management	• *Chemical Reduction*: There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to reduce emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation:* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization:* There is a need for more efficient chemical/material utilization, with their increased reuse/recycle/reclaim (and of their process emissions and byproducts). • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure a technology generation's sustainability, and also sustainability at a factory infrastructure level. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes, and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim*: There is a need to design facilities, equipment and products to facilitate these end-of-life issues

YIELD ENHANCEMENT

DIFFICULT CHALLENGES

The key challenges were adapted to latest developments and challenges recognized by the 2009 International Technical Working Group Yield Enhancement. In 2009 a new long term key challenge was identified. This is the introduction of 450 mm wafers which is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450 mm wafers requires a new generation of inspection tools. The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 45 mm wafer size. Therefore, the tool costs are crucial. 450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review. Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.

The order and type of near term key challenges was not changed in 2009. Currently, the most important key challenge will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high through put. Furthermore, it is a dare to identify but yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority the requirement for 3D inspection was identified. This necessitates for inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases. E-beam inspection seems not to be the solution for all those tasks any more.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- Process Stability vs. Absolute Contamination Level Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
- Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems. Currently, the monitoring and contamination control methods require intensive development.

In the long term the following key challenges are currently identified:

- Non-Visual Defects and Process Variations: Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.
- In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.
- Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.
- Introduction of 450 mm substrates (see above)

The Yield Enhancement chapter consists of three subchapters as Defect Budget and Yield Model, Defect Detection and Characterization, and Wafer Environment and Contamination Control. The major work during 2009 was the control and update of the tables. The changes summarizes as follows:

Defect Budget and Yield Model

- The tables for Defect budgets were not updated. The ITWG requires a solution to access updated particle per wafer pass data or particle control limits to supply defects and tolerable particle per wafer pass data to equipment suppliers and integrated device manufacturers in the future.

Defect Detection and Characterization

- The tables YE 6, 7 and 8 were checked carefully against latest developments for defect inspection and detection.

Table ITWG14 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection of Multiple Killer Defects / Signal to Noise Ratio - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
3D Inspection – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.	Detection of non visible defects e.g. voids, embedded defects, and sub surface defects in the structures. The demand for high-speed and cost-effective inspection is crucial. Large number of contacts and vias per wafer E-beam inspection seems not to be the solution for all those tasks any more. Sensitivity of the inspection tool to process variation and definition of maximum process variation (control limits).
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.	Currently, the monitoring and contamination control methods require intensive development.

Table ITWG14 Yield Enhancement Difficult Challenges

Difficult Challenges < 16 nm	*Summary of Issues*
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	SMLY, resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	Data volume + quality: strong increase of data volume due to miniaturization The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	A lot of models should be operated at the design stage. For example, Optical Proximity Correction, Well Proximity, Stress Proximity, CMP and so on The Amount of models seems to be rapidly increasing. Not only accuracy of models, but also optimization of trade-off between models might be requested. Development of test structures for new technology generations
The introduction of 450 mm wafers is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the subtrate. The introduction of 450 mm wafers requires a new generation of inspection tools.	The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 45 mm wafer size. Therefore, the tool costs are crucial. 450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review. Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.

[1] Cross-link to Metrology chapter

METROLOGY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The introduction of dual patterning and double exposure lithography add the complexity of measuring two distributions of linewidth, sidewall angle, and line width roughness inside the same measurement area. Another key challenge to critical dimension metrology is tool matching. Precision requirements for the next several years can be met using single tools. There are many gaps in metrology for EUV lithography especially for mask metrology. The entire mask fabrication process needs advances in capability especially for actinic patterned mask inspection and aerial imaging. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continues to drive metrology to provide measurements for new higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. The sub 1 nm EOT gate stacks require greatly improved film thickness and composition control during manufacturing. Interconnect structures continue the cycle of new materials. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation TSV now has potential solutions that are under investigation. In the area of metrology for Beyond CMOS R&D, graphene measurements have advanced in the areas of microscopy and electrical characterization. In addition, there are now several means of determining the number of graphene layers in a sample. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG15 presents the ten major challenges for metrology.

Table ITWG15 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

MODELING AND SIMULATION

Modeling and Simulation is the virtual counterpart of semiconductor device and chip fabrication and characterization: Computer programs are used to predict the geometries, strain and chemical composition (dopants, SiGe, etc.) of devices, their electrical performance and reliability, and finally the behavior of circuits and systems. The overall aim of Modeling and Simulation is to support the development of real-world technologies, devices, circuit and systems by providing information which is more difficult, more costly, less efficient or too time-consuming to obtain from experiments, and in this way to reduce development times and costs. To enable this, Modeling and Simulation tools must contain appropriate physical models including appropriate parameter settings, and also meet various requirements in terms of generality of application, speed of simulation, complexity of the applications which can be addressed, and, last but not least, user interfaces and interactions. In turn, dedicated research and development activities on Modeling and Simulation capabilities are needed.

In order to best meet the needs of the users of simulation tools in industry and research, the Modeling and Simulation group in the ITRS has also in 2009 based its work strongly on the industrial requirements, both from own assessments and from the results of the other groups in the ITRS, which deal with the various areas of process technology, integration, and fabrications issues. Starting from thorough review of all their texts and presentations and detailed discussions with these groups, also for the 2009 ITRS so-called crosscut sections have been prepared for the 2009 Modeling and Simulation chapter, and been used for the 2009 work.

The main part of the Modeling and Simulation chapter was prepared based on these crosscuts and an overall assessment of the state-of-the-art. In the following, the main elements of the chapter are summarized especially in view of the changes made compared with the 2007/2008 ITRS.

Similar to earlier years, the Modeling and Simulation Difficult Challenges are emphasized in the beginning of the chapter. The six short-term challenges refer in 2009 to nodes until 16 nm including. Among these, two challenges have been renamed to *Nanoscale device simulation capability: Methods, models and algorithms that contribute to prediction of CMOS limits* and *Electrical-thermal-mechanical modeling for interconnect and packaging*. Because of the developments of the industrial needs and the state-of-the-art, the detailed contents of all of these challenges were significantly changed, as displayed in Table ITWG16 below and Table MS-1 of the 2009 Modeling and Simulation Chapter. The long-term challenges now refer to nodes smaller than 16 nm. Here, only the contents of the first two of them were slightly modified.

Similar to these crosscuts with the other groups of the ITRS, there are also strong links between the areas covered by the Modeling and Simulation chapter, ranging from the area of equipment simulation through processes, devices, interconnects and circuits up to packages. Also in 2009 Modeling and Simulation chapter contains seven subchapters which deal with the various levels of modeling: *Equipment / Feature Scale modeling*, *Lithography Modeling*, *Front-end Process Modeling*, *Device Modeling*, *Interconnects and Integrated Passives Modeling*, *Circuit Modeling*, and *Package Simulation*. Whereas the scope of these subchapters has not changed compared to 2007, the requirements described therein have considerably evolved based on the development of the industry and the state-of-the-art in modeling and simulation.

In the 2007 ITRS, there were three topics which crosscut these seven areas, namely *Materials Modeling*, *TCAD for Design, Manufacturing and Yield*, and *Numerical Methods*. For the 2009 ITRS, the latter subchapter was extended to also include the *Interoperability of Tools*, which is an important requirement for the efficient use of simulation in industry and research. The second of these crosscutting subchapters has evolved in scope to a subchapter on *Modeling for Design Robustness, Manufacturing, and Yield*. Furthermore, because reliability issues get more important at all levels of simulation and, moreover, reliability problems at device, circuit, or package level are partly based on details of fabrication processes and their variations, a new separate crosscutting subchapter on *Reliability Modeling* has been added in the 2009 Modeling and Simulation chapter.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above.

Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs. Currently, the shortage of such research funds is even more severe than the technical difficult challenges summarized above. For example, several Modeling and Simulation requirements listed in the 2005 and 2007 ITRS had in this 2009 issue to be pushed out and delayed in time because sufficient R&D could not be done due to insufficient research funding.

DIFFICULT CHALLENGES

Table ITWG16 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Lithography simulation including EUV	Models and experimental verification of optical and non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning including database splitting
	Multi-generation lithography system models
	Simulation of defect influences/defect printing in EUV. Mask optimization including defect compensation
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
	Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, mechanical stability, leaching, and time-dependent effects in single and multiple exposure; resist processing techniques special for double patterning
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Simulation of ebeam mask making (single-beam and multibeam)
	Simulation of directed self-assembly of sublitho patterns
	Modeling lifetime effects of equipment and masks
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment for enhancing its accuracy
Front-end process modeling for nanometer structures	Coupled diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe, SiGe:C, Ge-on-Si, III/V-on-Si, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of cluster or cocktail implants
	Modeling of plasma doping, e.g. for FinFETs
	Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping
	Modeling of stress memorization (SMT) during process sequences
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries
	Front-end processing impact on device leakage (e.g. residual defects) and reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Simulation of polishing, grinding and wafer thinning in backend processing

Table ITWG16 Modeling and Simulation Difficult Challenges

	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulation
Nanoscale device simulation capability: Methods, models and algorithms that contribute to prediction of CMOS limits	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like MRAM, PCM/PRAM, etc
	Gate stack models for ultra-thin dielectrics with respect to. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
	Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure and dopant variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel materials, e.g., high-κ stacks, Ge and compound III/V channels, etc.: Morphology, band structure, defects/traps, etc.
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
	Reliability modeling for ultimate CMOS
	Physical models for stress induced device performance
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, etc.). Size effects (microstructure, surfaces, etc.) and variability of thinned wafers.
	Signal integrity modeling for stacked die
	Model effects which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture, dielectric breakdown, piezoelectric effects)
	Physical models to predict adhesion on interconnect-relevant interfaces (homogeneous and heterogeneous)
	Simulation tools for adhesion and fracture toughness characteristics for packaging and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to 160 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains
	Scalable active component circuit models [1] including non-quasi-static effects, substrate noise and coupling,, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
	Scalable passive component models [1] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [1] for More-than-Moore devices including switches, filters, accelerometers, …
	Physical circuit element models for new memory devices, such as PCM, and standardization of models for III/V devices

Table ITWG16 Modeling and Simulation Difficult Challenges

	Computer-efficient inclusion of aging, reliability and variability including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations
Difficult Challenges < 16 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	*Ab-initio* modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping, quantum dots, atomic electronics, multiferroic materials and structures, strongly correlated electron materials)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling
	Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)
	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

[1] In More than Moore, scalability refers to the ability to model litho-defined device variations

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2008. Additionally, the ORTC Glossary has been updated in 2009.

OVERVIEW OF 2009 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds thousands of units per month of ICs from a manufacturing site using "production tooling." Furthermore, a second company must begin production within three months (see Figure 2a). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology "node" manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of "node" advancement. This approach of measuring technology progress complicates the "node" relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology "node" references in Flash memory product announcements, and Flash technology received increased emphasis in both the 2005 and 2007 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage.

The International Roadmap Committee (IRC) decided in the 2007 ITRS roadmap that the best way to minimize confusion between the ITRS and individual company public announcements was to continue the separate tracking of the various technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM

product is referenced to un-contacted poly dense parallel lines (refer to Figure 1). Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the emphasis on separate product trend tracking, no common product technology header is required. Only the year of production of the referenced technology line item is required as the minimum ITWG table header. In each of the roadmaps since the 2007 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) are emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item, as further defined by the ITRS Executive Summary and Glossary.

Individual product technology trends continue to be monitored, and the most recent TWG survey update is indicating that the DRAM historical trend continues to track close to the average 2.5-year cycle (*cycle = one-half reduction per two cycle periods) trend, and the 2009 DRAM M1 half-pitch targets are therefore unchanged from the 2008 ITRS Update ORTC Tables. The modeled and calculated projection trends may produce slight differences from the actual survey results, however the timing which influences the Grand Challenges and Potential Research and Development solutions are consistent with the average trends of latest survey results.

In the most recent Flash technology survey, the overall lithography resolution continues to be driven at the most leading edge by the feature size trend from Flash product. For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is now projected to be even further ahead of DRAM stagger-contacted M1 half-pitch (by three years by 2010). A two-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to a one-year lead of the DRAM stagger-contacted M1 half-pitch, and this additional timing lead increase is therefore causing Flash memory technology to continue to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2009 ITRS table technology trend targets continue as annualized targets from 2009 through the 15-year Roadmap horizon in 2024. However, per previously established IRC guidelines, the 2009 ITRS retains the *definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures 6 and 7.

Please note from the 2009 ITRS Table ORTC-1 that the timing of a technology cycle remains different for a particular product. For example, the DRAM stagger-contact half-pitch M1 in the 2009 ITRS is still forecast to be on an average 0.71× reduction every two and one-half years (0.50×/5-years) timing cycle until 2010/45 nm). After 2010, the DRAM M1 trend is forecast to be on a three-year cycle through the 2024/~9 nm target. The annual multiplier for the three-year cycle timing is 0.8909× reduction per year, which is used to calculate the interim annual trend targets (examples: 2011/40 nm, 2020/14 nm).

After taking into account the available industry PIDS survey data and other ITWG and IRC inputs, consensus was reached on a new Flash product technology timing model (based on the uncontacted polysilicon half-pitch definition). The Flash uncontacted polysilicon half-pitch is now set on a two-year cycle timing pace from 2000/180 nm, but extended through 2010/32 nm. The Lithography ITWG also continues to use the Flash uncontacted polysilicon half-pitch (now projected to be numerically three years "ahead" of the DRAM stagger-contacted M1 half-pitch in 2010) to drive the technology process equipment being used to achieve that target. After 2010/45 nm, the Flash uncontacted polysilicon half-pitch is expected to turn to a three-year timing cycle, parallel, but three years ahead of the DRAM trend, and would extend to 2024/6 nm on an annual basis.

In response to new Design TWG data and model updates for the 2009 ITRS, the MPU (and high-performance ASIC) (MPU/hpASIC) Product Trend cycle timing (based on the same stagger-contact M1 half-pitch definition as DRAM) has been updated. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch is now delayed behind the DRAM trend; however the MPU/hpASIC is set on a two-year (reducing in half every 4-years) cycle timing pace through 2013/27 nm. At the 2010/45 nm point, it was decided that the MPU/hpASIC M1 targets would cross over the DRAM M1 cycle timing target and at the 2013/27 nm point will turn to a three-year timing cycle through the end of the roadmap in 2024.

The MPU/hpASIC final physical gate-length (phGL) was significantly revised in the 2008 Update, and then again during the 2009 ITRS work. The targets for a portion of the historical trend remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2003/45 nm point. From that point through the new 2009/29 nm target, the trend was adapted to track actual data points provided by the FEP and PIDS ITWGs. From the 2009/29 nm point the model tracks the PIDS survey data, and utilizes trend targets calculated by using

a 3.8-year timing (reducing in half every 7.6 years; or 0.9128 reduction per year) cycle through the end of the Roadmap to 2024/7.4 nm. The Lithography and FEP ITWGs revised their agreement on a new consensus variable ratio between the printed gate length targets and the final physical gate length, which includes etch.[3]

The low-operating-power ASIC gate length targets are likewise adapted to the new PIDS survey data (by shifting their introduction timing relative to the MPU printed and physical gate lengths); and a new standby-power physical gate length line item was added in the 2008 Update and is updated in the 2009 ORTC tables.

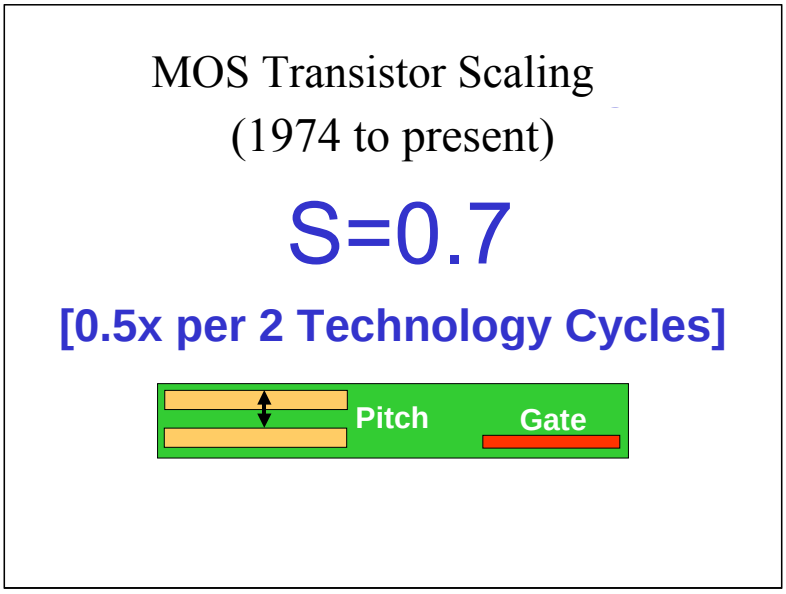


Figure 6 MOS Transistor Scaling—1974 to present

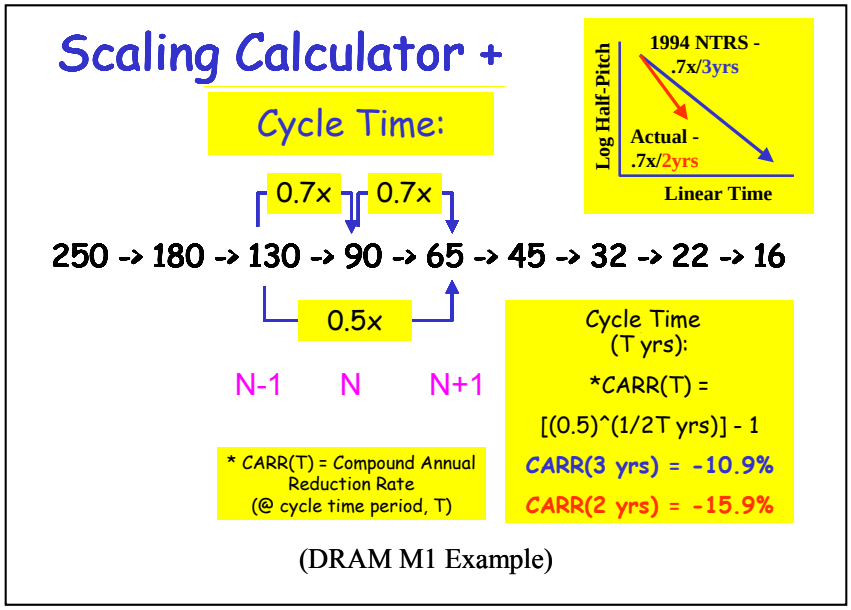


Figure 7 Scaling Calculator

[3] *Special thanks to John Boyd, Principle Process Analyst at UBM Techinsights and Dick James, Senior Technology Analyst at Chipworks for data contributions to Front End Processes' ITRS modeling for physical gate length.*

ROADMAP TIMELINE

The 2009 edition of the Roadmap maintains a 15-year projection, from 2009 as a reference year and through 2024. The timing trends of the future technology pace of the DRAM product, in past roadmaps, has represented the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size) after 45 nm/2010, unchanged from the 2008 edition. In the 2008 Update, from surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2005, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

Also based on the PIDS TWG surveys, the 2008 ITRS Table ORTC-1 DRAM product M1 half-pitch trend targets were calculated to align with an observed industry historical 2.5-year technology cycle (calculated from 180 nm/2000, 90 nm in 2005, and forecast to be 45 nm in 2010). Data provided by DRAM manufacturers suggests a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch from the 2007/45 nm–2024/9 nm Roadmap period, as illustrated in Figure 8a.

Also mentioned above, the DRAM interconnect half-pitch will no longer continue to be used as a representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). In fact, the Flash uncontacted polysilicon half-pitch feature is expected to continue on its 2-year cycle pace through 2010/32 nm, when it will be leading the DRAM M1 targets numerically by three years, and now is acknowledged by the Lithography ITWG to be the most leading driver of leading-edge technology manufacturing. Similarly, as mentioned, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2-year cycle pace and are presently expected to cross over the DRAM half-pitch in 2010/45 nm, and continue the 2-year pace through 2013/27 nm With the new product-oriented focus since the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figures 8a and 8b.

ROUNDED TREND NUMBERS

Using 180 nm DRAM product half pitch in the year 2000 as the calculation standard for trends, the 2009 ITRS now includes an update of the past "rounding" convention for the technology cycle trend target. The actual calculated mathematical trend data (used for model calculations in the ORTC and TWG tables) reduces by 50% every other technology cycle, resulting in actual versus rounded number targets comparison below, starting from 350 nm in 1995, as follows in Table C.

Table C Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	1995	1998	2000	2002.5	2004	2005	2006	2007.5
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**103.4**	**90**	**68.2**	**63.6**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**

YEAR OF PRODUCTION	2009	2010	2012	2013	2015	2016	2018	2019	2022	2023	2024
Calculated Trend Numbers (nm)	**51.7**	**45**	**35.7**	**31.8**	**25.3**	**22.5**	**17.9**	**15.9**	**11.3**	**10.0**	**8.9**
ITRS Rounded Numbers (nm)	**52**	**45**	**36**	**32**	**25**	**22.5**	**17.9**	**15.9**	**11.3**	**10.0**	**8.9**

Note that the rounding corrections have become more critical as the industry moved into the two-digit data cycles of the nanotechnology (sub-100 nm) era. Please note also that some regions, for their own legacy publication consistency, will retain their right to continue to track the previous technology generations beginning with "100 nm"/2004. Starting from "100 nm" in 2004 will result in "milestones" that are targeted one year earlier than the present 2009 roadmap convention (example: 70 nm/2006; 50 nm/2009; 36 nm/2012; 25 nm/2015, etc.). By consensus of the IRC both number sets are available for long-term calculations, since the original 2001 ITRS long-term columns were retained (2010/45 nm; 2013/32 nm; 2016/22 nm), and interim columns (2012/36 nm; 2015/25 nm; 2018/18 nm; 2021/13 nm) are now annualized and included as columns. It was decided for the 2008 ITRS ORTC Update to include one decimal place of rounding accuracy after 2016 for the Table ORTC-1 header technology trend line items. The 2009 ORTC tables are now available in excel table files at www.itrs.net; and even more decimal places of accuracy calculated by the models are available for the use of readers in those excel tables.

UPDATES TO THE ORTC

The MPU/hpASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. The DRAM trend is unchanged from 2008, however the MPU/hpASIC M1 half-pitch has been revised to a lagging two-year cycle trend that crosses DRAM in 2010/45 nm, and then continues to 2013/27 nm before it turns to a three-year cycle for the balance of the roadmap period. The Flash product half-pitch continues to be defined as an uncontacted polysilicon half-pitch, and has also been revised from the 2008 ITRS by continuing the two-year cycle trend through 2010/32 nm, then turning to a three-year cycle through 2024. Refer to Figures 8a and 8b.

Due to trade-offs with "equivalent-scaling" process enhancements (copper and low-κ interconnect, strained silicon, high-K/Metal Gate, etc.), as performance and power management alternatives (see Figure 8c), the *printed* MPU and *physical* gate length trends received major corrections in the 2008 and 2009 ITRS ORTC. As described above, the physical gate length trend has been aligned with historical and survey data and is on a slower 3.8-year cycle trend beginning 2009/32 nm through 2024/7.5 nm. The printed gate length begins a delayed three-year cycle trend in 2011, and continues through 2024 on a "shrinking" ratio relationship to the physical gate length out to 2024/7.9 nm, just slightly larger than the expected final physical gate length at that time. Refer to Figure 8b.

The ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will continue to provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2010 ITRS Update process, and the possibility of additional adjustments to the technology cycle in some of the individual product technology trends. As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap trend shifts, it was agreed to continue the practice of publishing annual technology requirements from 2009 through 2016, called the "Near-term Years," and also annual requirements from 2017 through 2024, called the "Long-term years." As can be noted in Figures 8a and 8b, the Long-term years of the 2009 ITRS are somewhat aligned with the timing of the especially-challenging sub-16 nm technology era.

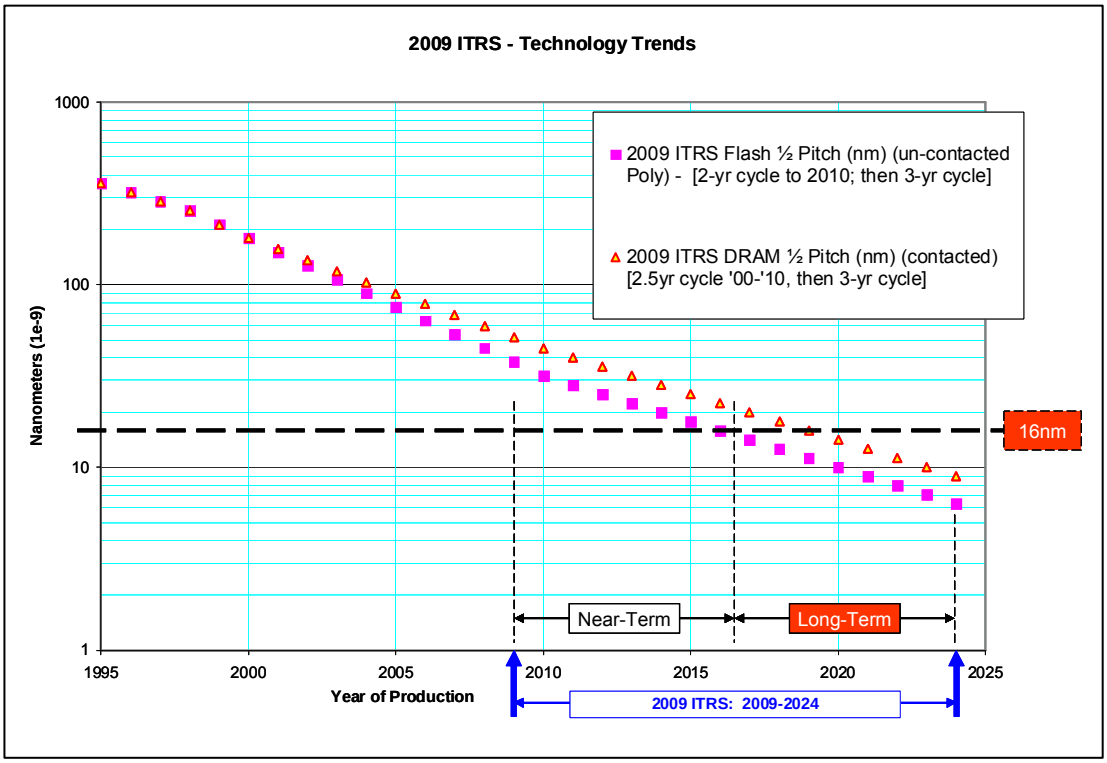


Figure 8a 2009 ITRS—DRAM and Flash Memory Half Pitch Trends

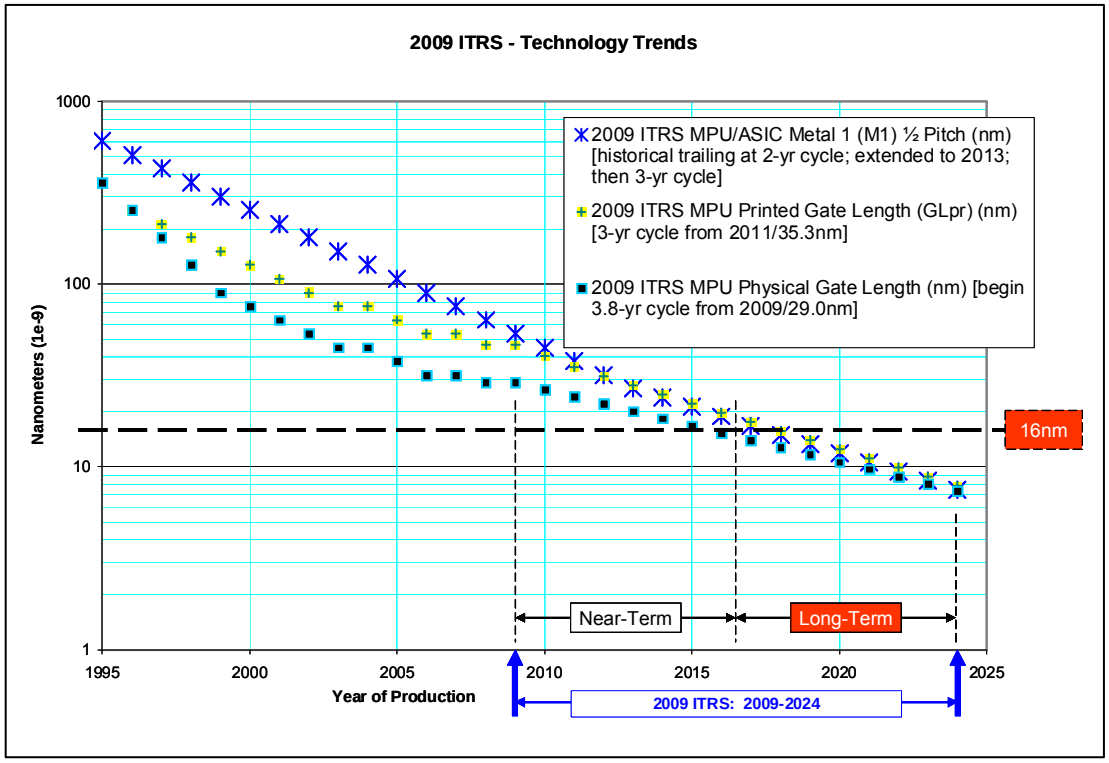
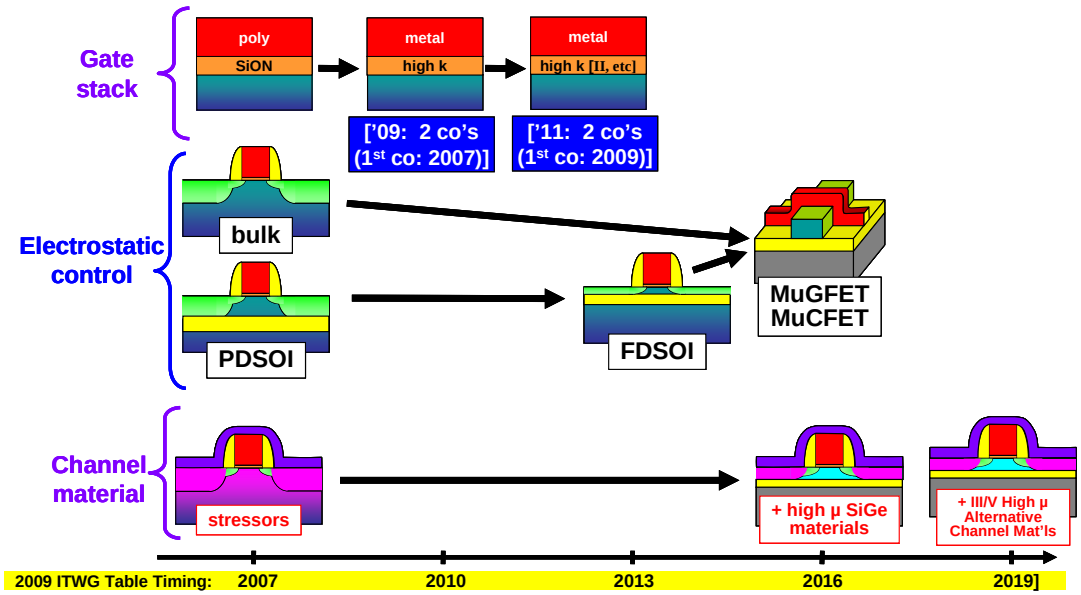


Figure 8b 2009 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends



(See also PIDS, FEP, ERD, and ERM chapters' text and tables for additional detail)

Figure 8c 2009 ITRS "Equivalent Scaling" Process Technologies Timing compared to ORTC MPU/high-performance ASIC Half Pitch and Gate Length Trends and Timing

PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. Continuing a practice that began with the 2005 ITRS, the 2009 ITRS edition bases the technology pace drivers on individual product technology trends. These product-based technology trends may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolutions/shrink paths become more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic [as exemplified by MPU/high-performance ASIC (MPU/hpASIC)] technology moved at the same pace as DRAM technology, but lagged behind. The 2007 PIDS surveys of DRAM manufacturers concluded that after 2000/180 nm DRAM technology advancement was moving at an average 2.5-year. During the last few years, the development rate of new technologies used to manufacture MPU/hpASIC has continued on the 2-year pace, and is expected to continue on the 2-year pace through 2013/27 nm, while DRAM technology is presently forecast to slow to a three-year cycle pace beginning 2010/45 nm through the 2024 Roadmap horizon. By moving on the faster 2-year cycle pace, MPU/hpASIC products are closing the half-pitch technology gap with DRAM, and are expected, along with Flash technology needs, to drive the most leading-edge lithography tools and "equivalent-scaling" processes—especially for the capability to process and add power-management and performance enhancement characteristics to the isolated-line feature of the printed and physical gate length (such as etch-shaping, strained silicon, high-K/Metal Gate, etc.). As noted above, the Flash technology, as defined by uncontacted polysilicon, and has also accelerated to the point where it is now driving at the most leading edge. As mentioned, the latest Flash technology also drives the most leading lithography and the PIDS surveys forecast the Flash 2-year un-contacted poly half-pitch technology cycle pace to continue to 2010/32 nm before turning to a 3-year cycle pace through 2024.

However, several fundamental differences exist between the families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch. The 2009 ITRS is now forecasting the insertion of new buried word and bit line cell technology, which will enable the $4f^2$ cell size beginning 2011 (4=design factor and f=half-pitch in microns).

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2009 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the updated ORTC tables. The MPU product chip size tables continue to be similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations.

Table ORTC-1 summarizes the technology trend metrics summarized above. For completeness, the ASIC/low power gate length trends are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of "equivalent-scaling," design factor, half-pitch, and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize Figures 8a and 8b, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2010/45 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (2000/180 nm–2010/45 nm) average 2.5year cycle rate is approximately 13%/year reduction on an annual basis (~24% reduction/two years). As noted above, the Flash memory uncontacted polysilicon is now expected to change to the three-year pace in 2010 and leads both the DRAM M1. The MPU/hpASIC M1 (generically referred to as MPU/ASIC in graphs) crosses over the DRAM M1 in 2010/45 nm, and is forecast to continue on the two-year pace through 2013/27 nm before changing to a three-year pace.

Table ORTC-1 ITRS Technology Trend Targets

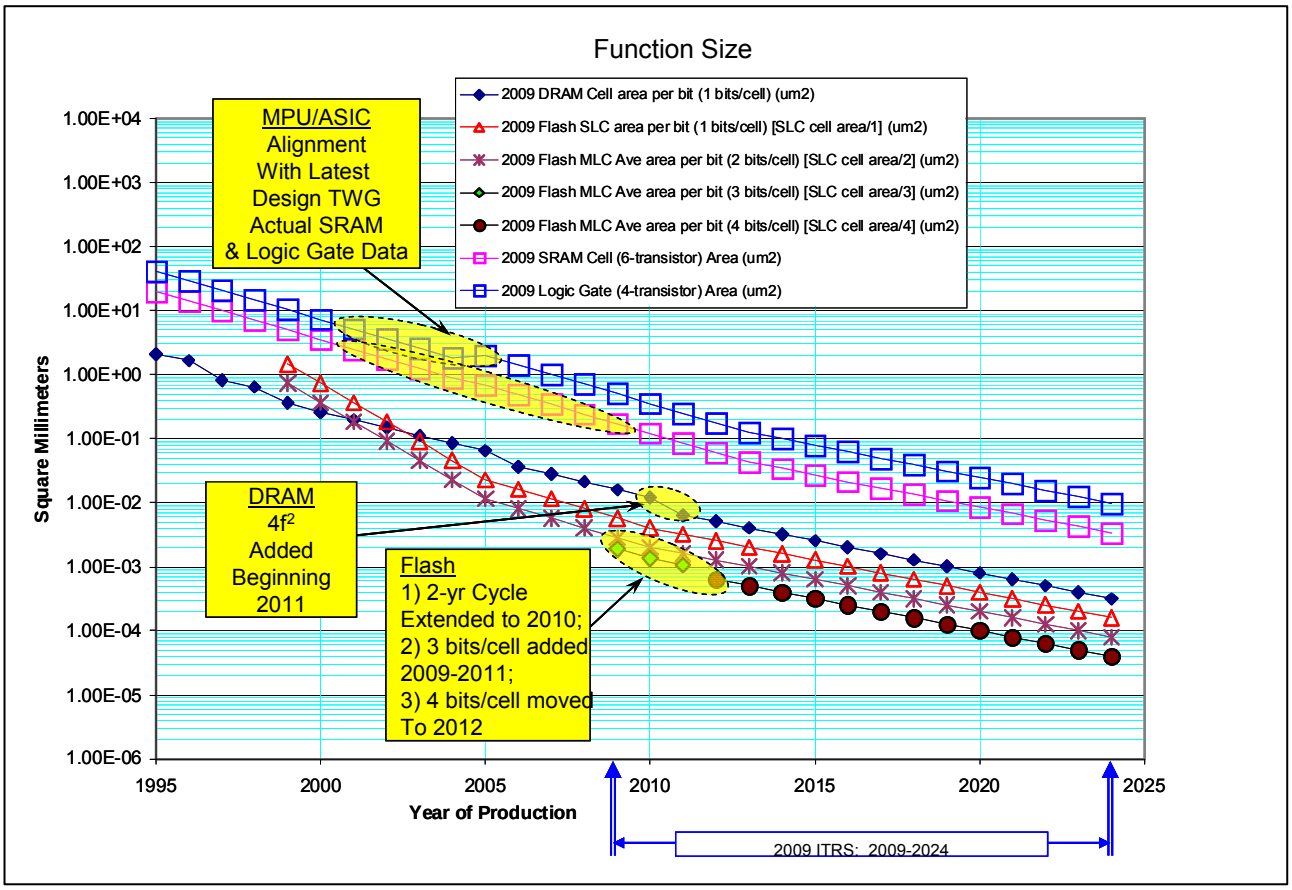


Figure 9 2009 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

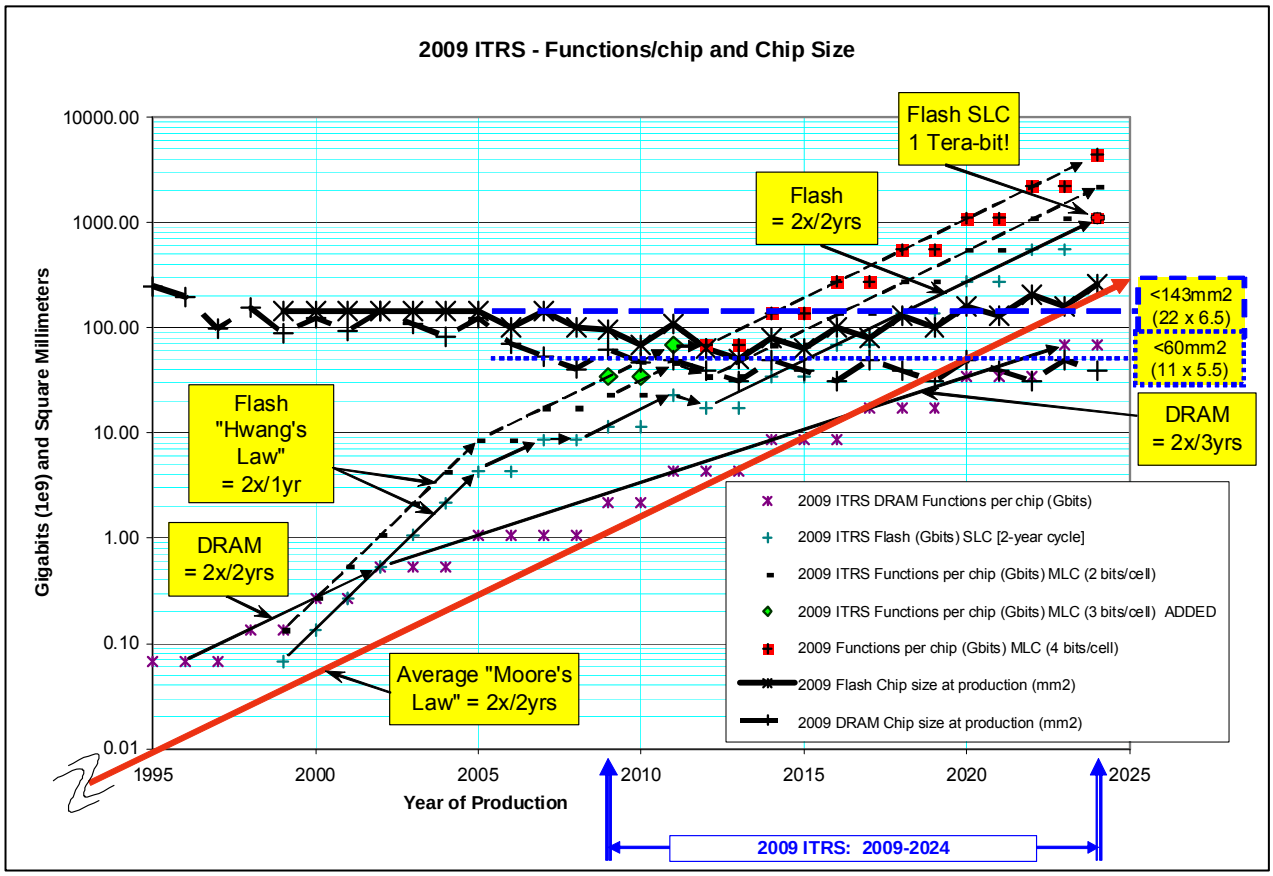


Figure 10a 2009 ITRS Product Technology Trends:
Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

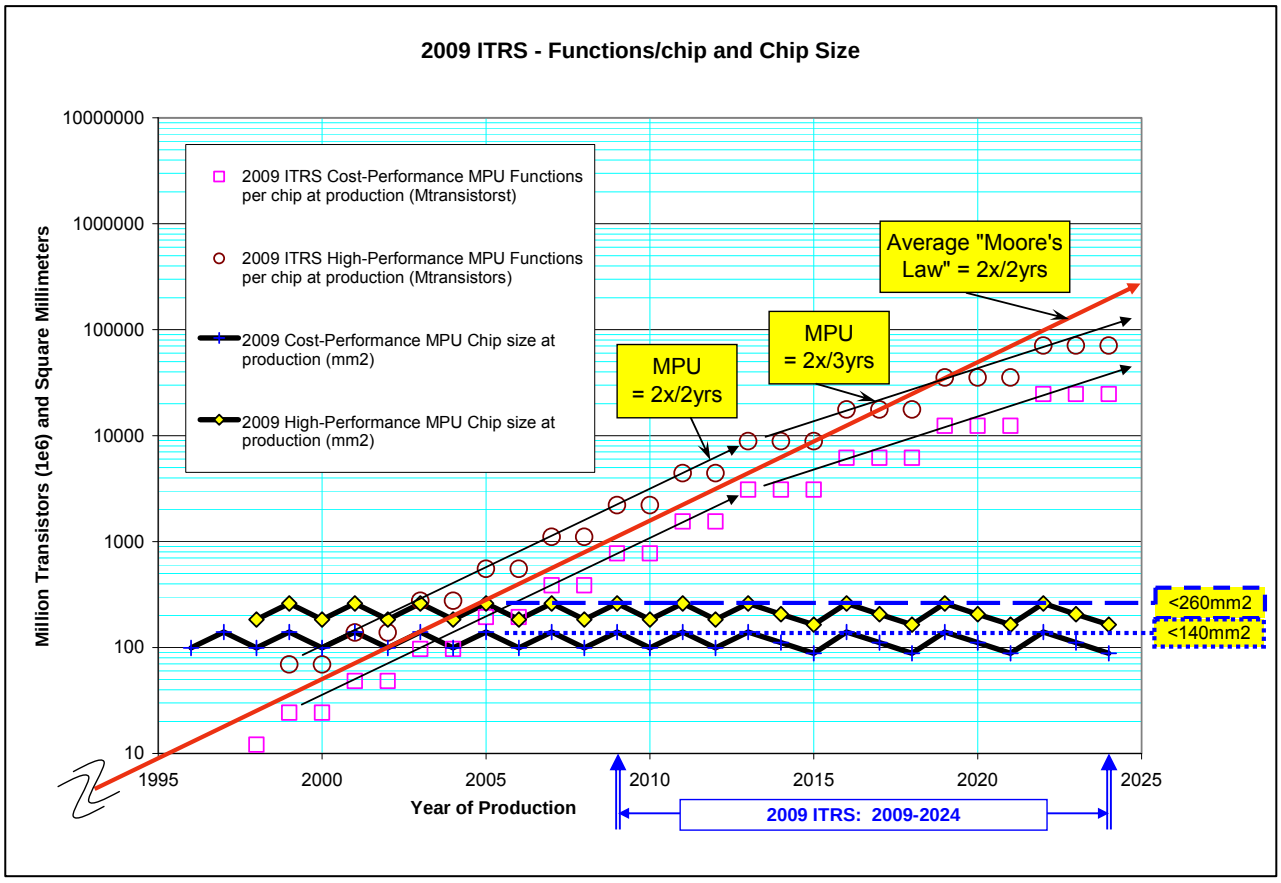


Figure 10b 2009 ITRS Product Technology Trends:
MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area

goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in Tables ORTC-2A and 2B. (Also refer to the Glossary for additional details).

Table ORTC-2A DRAM and Flash Production Product Generations and Chip Size Model

Table ORTC-2B DRAM Introduction Product Generations and Chip Size Model

Notably, the most recent survey data and publicly available announcements indicate that reduction rate of DRAM cell area factors for the 2009 ITRS models will accelerate, placing the $4f^2$ area factor in 2011 (versus the flat $6f^2$ area factor in the 2005 ITRS). Beginning 2011 the area factor is expected to remain flat at $4f^2$ through the 2024 ITRS horizon. In addition to the $4f^2$ factor insertion, the survey extends the 56% array efficiency from 2006 to the roadmap horizon in 2024. These gains in DRAM cell design efficiency and function density were traded off against a lower targeted production chip sizes, which are now targeted for production sizes to be below $60mm^2$. Therefore, the DRAM "Moore's Law" bits per chip targets have been delayed by one year, and continue to target 2× every three years in both the near term and long term. The 64 Gbit DRAM product now sits at the ITRS year 2023 horizon (refer to Function Size and Functions per Chip in Figures 9, 10a and 10b).

In the updated 2009 ORTC Flash product model, the function bit size is still calculated based upon the single-level cell (SLC) design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. The 2009 PIDS Flash survey indicated that the rapid 2-year scaling cycle now is expected to continue through 2010; however, the single-level-cell physical design factor limit remains at 4. Therefore, the Flash model function (bit size) area reduction has accelerated, and the Flash uncontacted polysilicon half-pitch will numerically lead the DRAM stagger-contacted M1 half-pitch by three years. The Lithography TWG now believes that leading-edge Flash manufacturing technology is clearly driving the most-leading-edge manufacturing, which also uses comparable processing equipment to manufacture leading-edge DRAM products.

Flash SLC bit technology was thus able to drive quickly to a 76 nm uncontacted polysilicon half-pitch and a "4" design factor in 2005; and is expected to continue the scaling reduction to 32 nm in 2010, reducing SLC bit size to 0.004 um^2, one third the size of a DRAM cell that year (see Figure 9, 2005 ITRS Product Function Size Trends). This continued acceleration of Flash technology will enable the production of a 96 mm^2 11 Gbit SLC product in 2009, when DRAM product is still at 2 Gbit (however, is only $61mm^2$ to meet demanding market affordability and productivity requirements). Furthermore, Flash technology is able to create an electrical doubling of bits (multi-level-cell, or MLC) in the same area, resulting in a virtual doubling of bits per chip to 22 Gbits in the $96mm^2$ affordable first production chip size range. The PIDS Flash survey has also added a three-bits-per-chip MLC product beginning 2009, enabling the more difficult quad-bit MLC to shift to 2012 production.

By recommending the most dramatic changes since the 2001 ITRS, the Design ITWG has improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including new transistor design improvement factors. The new Design ITWG model utilizes a 60 design factor (significantly down from over 100 in previous roadmaps), in SRAM transistors, and is no longer expected to slowly improve over time. The logic gate transistor design factor was also dramatically reduced from over 300 to 175, and is also expected to remain flat throughout the roadmap period. Barring any significant changes in array efficiencies (the only other variable affecting the chip size models), the "shrink" and density improvements will continue to come from lithography-enabled interconnect half-pitch scaling.

The present 2009 ITRS MPU model ties to historical data by lagging an M1 half-pitch data trend on a two-year cycle trend, which crosses over the DRAM M1 half-pitch in 2010/45 nm, and then continues on the two-year cycle to 2013/27 nm before turning to a three-year cycle parallel to both DRAM M1 and Flash Poly half-pitch trends. The technology dimension and design factor model is significantly revised from past ITRS roadmaps, but still continues to reflect the competitive requirements for affordability by targeting flat chip size trends for both high-performance MPUs (now lowered to $260mm^2$) and cost-performance MPUs (still 140 mm^2).

Due to the MPU two-year-cycle half-pitch "catch-up-and cross-over phase" through the year 2013, the MPU products are targeted to maintain flat chip sizes due to lithography improvements alone. However, after 2013, the inter-generation

MPU chip size model can remain flat only by slowing the rate of on-chip transistors to double every technology generation (3-year cycle after 2013).

In the 2009 ITRS, the MPU model continues to use the approach of doubling the logic cores only every other technology cycle. However, function size and density of the core was kept unchanged by doubling the transistors per core targets. The Design ITWG consensus opinion is that this approach to the MPU Model is more representative of current design trends. Refer to Function Size and Functions per Chip in Figures 9, 10a and 10b.

Due to the latest forecast extension of the MPU M1 half-pitch two-year technology cycle, the present MPU chip-size model can continue the historical Moore's Law doubling of on-chip functionality (transistors) until the 2013/27 nm point. After 2013, the Moore's Law rate of on-chip transistors slows to 2× every three years, to match the slower 3-year technology cycle (in order to maintain flat chip size targets). To keep the effective historical functional productivity on track after the 2013 point, MPU chip and process designers must add even more "equivalent scaling " design/process improvements to the designs to enhance the improvements provided by the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables ORTC-2C and 2D.

Table ORTC-2C MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model

Table ORTC-2D High-Performance MPU and ASIC Product Generations and Chip Size Model

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields (26×33 = 858 mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG limits the absolute maximum field size at 858 mm^2 and allows the individual memory and logic product chip size surveys and models to drive the requirements up to the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2009 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 750 mm^2 lithography field size well under the 858mm^2 maximum, and fitting at least one introduction-level chip size within that field size. The latest 2009 ITRS production-level DRAM chip size model (less than 60 mm^2 flat target) fits nine die within a 572 mm^2 field.

The combination of technology generation scaling and cell design improvements (including the new $4f^2$ A-factor reduction from $6f^2$ in the 2007 ITRS) accomplishes that goal, while also allowing a goal of doubling on-chip bits to a slower 3-year cycle. As mentioned in the product chip size model discussions above, the 2011 accelerated DRAM design improvement to 4, and the new 60mm2 affordable production chip size target, caused a requirement to add fewer on-chip bits to stay under the affordable chip size and lithography field size. This was accomplished in the present DRAM model by delaying the production bits/chip generations by 1 year, and continuing the slower Moore's Law bits/chip rate at 2×/ three years to the end of the roadmap period. The data targets for the DRAM model are included in Tables ORTC-2A and 2B.

The Flash production chip size model is also included in those tables, and still targets the Flash maximum affordable chip size at 143 mm^2, while continuing to target the doubling of Flash bits per chip every two years. Due to the extension of 2-year technology cycles to 2010/32 nm poly half pitch processing, plus the addition of 3bits/chip and 4bits/chip multi-level cell (MLC) devices, the Flash product chip sizes remain below 143mm^2 through 2021. In 2022, the chip size hits the industry maximum affordable 200mm^2 limit, and may require adjustment of the Flash bits per chip model in future ITRS work.

The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG (26 × 33 =

858 mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 $mm^{2,}$ reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue are provided by the Lithography TWG in their chapter. The maximum Lithography field size targets are shown in Table ORTC-3, and are unchanged from the 2007 ITRS targets.

Table ORTC-3 Lithographic-Field and Wafer Size Trends

The 2009 ITRS DRAM, MPU and Flash models depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for upgrading 200mm manufacturing to 300 mm productivity boost (and also continuous improvement of the productivity of fabs) has increased in urgency more than ever, especially for leading-edge independent and foundry manufacturers. However, the poor economy, especially the most recent global recession, has created financial challenges and limited capital investment. The maximum substrate diameter in Table ORTC-3 (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity, which began in 2001, and has now achieved 50 per cent of the industry silicon area capacity.

The challenging economy has also affected the investment into, and the timing of, the incremental productivity boost expected from the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter (as described in the 450 mm section of the Executive Summary above). Therefore the availability of the 450 mm productivity boost has been re-targeted by the ITRS executive steering committee (IRC) for 32 nm (M1 half-pitch processing measured) pilot-line capability in 2012, with 22 nm production ramps anticipated by leading microprocessor, memory, and foundry companies to be required 2014-2016.

However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter, or other equivalent processing solutions, to drive productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion require the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work continues to be sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH. Most certainly, pre-competitive cooperation between the semiconductor supplier and manufacturer companies will be required to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development.

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Table ORTC-4).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. MPU and high-performance ASIC products approach 3–7K pads over the ITRS period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table ORTC-4 Performance and Packaged Chips Trends

Package pin count and cost-per-pin (Table ORTC-4), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow, while the cost/pin decreases. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually.

In the very competitive consumer electronics product environment (which is a focus end-product segment for characterizing Design and System-Driver Chapter Grand Challenges and Potential Solutions), prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases while the average cost per pin decreases, then: the average packaging share of total product cost will continue to increase over the 15-year roadmap period; and the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip (SOC) and through the use of multi-chip modules (System-in-Package, i.e., SiP), bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. However, beginning in earlier roadmaps and continued in the latest 2009 ITRS, historical and forecast trends are suggesting a significant slowing in the rate of increase of on-chip frequency, to approximately only 8% growth per year or less. Performance increases accomplished historically by geometrical scaling (refer to Glossary) are now being provided through process "equivalent scaling" and also design-related "equivalent scaling" (see new definition updates in the Glossary) architecture and software improvements that enable the continued delivery of SOC, SIP, and system-level performance to customers while keeping power management under control.

For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational performance will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Table ORTC-4, which include line items contributed by the Design TWG to forecast the maximum on-chip trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip – see the A&P chapter for details).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Table ORTC-5. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 2 for DRAM and microprocessors. In addition, the data in the table are reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield

Enhancement chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity, and work in underway in 2009 by the Lithography TWG to survey companies and revise the targets for the 2010 update.

Table ORTC-5 Electrical Defects

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Table 6, the value of the power supply voltage is now given as specific target, rather than a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.6 volts are not expected to be achieved by high-performance processors until 2024. . The lowest V_{dd} target is still 0.6V in 2021 for the low operating power applications, and is not expected to drop below that level out to 2024.

Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable (low-cost, hand-held) battery operations. In all cases, total power consumption targets are relatively flat in the 2009 Table ORTC-6, despite the use of a lower supply voltage. The power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

The approach for calculating maximum power targets is being re-evaluated in 2009, and the 2010 roadmap update calculation models from the Design and Assembly and Packaging (A&P) ITWGs are expected to take into account specific "hot-spot" area calculations rather than the overall chip area.

Table ORTC-6 Power Supply and Power Dissipation

COST

Table ORTC-7 is dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year (0.5× per 2 years) has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, 2005, 2007 and now the 2009 ITRS models *all continue to use that idealized and simplistic model*, which results in 29% cost reduction of a function (bit, transistor, etc.). Note that the 29% average rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2009 ITRS DRAM and MPU cost models continue to use the need for that average 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 1.3 microcents for DRAMs in 2009. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in

cost/bit should be expected.[4] A corresponding analysis conducted from published data for microprocessors provides similar results.[5] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2009 ITRS has significantly revised the MPU chip size model. The Design ITWG has updated the MPU model in the 2009 ITRS, based upon their most recent available data and models. The new data and model indicate that logic transistor size is improving at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat to the 140mm2 target, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to be on a 2-year cycle through 45 nm/2010, and turn to a three-year cycle after 2010. Therefore the transistors per MPU chip can double only every three years after 2013, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements is expected to accelerate, as reflected in the 2009 ITRS DRAM Chip Size Model targets (see Table ORTC-2). The "4" design factor, a 33% improvement over the "6" factor, is now expected to be implemented in 2011, accelerating incrementally the long-range cost-reduction productivity. Furthermore, the latest PIDS TWG survey of DRAM manufacturers has indicated that the target for the cell array efficiency percentage achieved 56% after 2006 is expected to continue through the roadmap horizon, 2024. The recent model changes, along with the new goal of a more affordable starting production chip size (less than 60mm2 versus previous 100mm2) has delayed the bits/chip increase rate of DRAM by one year, while continuing the increase rate of bits per chip at 2×/3 years. These DRAM model changes have pushed the 64 Gbit generation (introduction in 2013) to 2023 for production and moved the 128 Gbit DRAM (introduction 2016) beyond even the present 2024 ITRS horizon. .

To compensate for slowing DRAM and MPU (after 2013) functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the "equivalent" productivity scaling benefits of chip, package, board, and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (see Table ORTC4) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2009 ITRS. Further discussion is detailed in the Test and Test Equipment chapter.

Table ORTC-7 Cost

[4] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

[5] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, December 9, 1996, 148–152.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

PLEASE NOTE THAT THE 2009 ITRS GLOSSARY INCLUDES NEW DEFINITION ADDITIONS AND UPDATES.

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
    - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS TWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-K interconnect materials; strained silicon; high-K/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit) , for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years.(-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[6]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-two and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

[6] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.