# INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

# 2009 EDITION

# ASSEMBLY AND PACKAGING

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# ASSEMBLY AND PACKAGING

## SCOPE

This chapter addresses the near term assembly and packaging roadmap requirements and introduces many new requirements and potential solutions to meet market needs in the longer term. Assembly and Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability.

Today assembly and packaging is a limiting factor in both cost and performance for electronic systems. This is stimulating an acceleration of innovation. Design concepts, packaging architectures, materials, manufacturing processes and systems integration technologies are all changing rapidly. This accelerated pace of innovation has resulted in development of several new technologies and expansion and acceleration of others introduced in prior years. Wireless and mixed signal devices, bio-chips, optoelectronics, and MEMS are placing new requirements on packaging and assembly.

The electronics industry is nearing the limits of traditional CMOS scaling. The continued growth of the industry, driven by a continuous reduction in cost per function, will require new devices types and new materials. There will be a gap between the time CMOS scaling can no longer maintain progress at the Moore's Law rate and the time a new generation of device architectures and electronic material will support a continued drop on cost per function. As traditional Moore's law scaling becomes more difficult, assembly and packaging innovation enabling functional diversification and allowing scaling in the third dimension is taking up the slack.

Assembly and Packaging provides a mechanism for cost effective incorporation of functional diversification through System-in-Package (SiP) technology. This technology enables the continued increase in functional density and decrease in cost per function required to maintain the progress in cost and performance for electronics.

New architectures including printed circuits, thinned wafers and both active and passive embedded devices are emerging as solutions to market requirements. The materials and equipment used in assembly and packaging are also changing rapidly to meet the requirements of these new architectures and the changing environmental regulatory requirements.

This chapter is organized in nine major sections:

- Difficult Challenges
- Single Chip Packaging
- Wafer Level Packaging
- System Level Integration in Package (SiP)
- 3D Integration
- Packaging for Specialized Functions
- Advanced Packaging Elements
- Environmental Issues
- Cross-Cut Issues

Wherever possible we have aligned the ITRS Assembly and Packaging chapter with other industry roadmap organizations including iNEMI, JISSO and IPC.

# DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in Table AP1. Meeting these requirements will demand significant investment in research and development.

The investment required to meet these challenges is greater than the current run rate and cannot be met through the current gross margin of the assembly and packaging suppliers alone. The recent increase in cooperative development represented by University programs and Research Consortia is evidence that the technical community is responding:

- University research in packaging is increasing around the world
- Materials companies have increased their investment in the new materials required to meet the future needs beyond copper metallization and low κ dielectric materials to new polymers and nanomaterials. New materials addressing future requirements are described in *the Emerging Research Materials* chapter of this Roadmap.
- Venture capital investment in packaging and interconnect technology is increasing after several years of absence.
- Equipment companies are investing in new capability to meet the needs of emerging requirements for making and handling thinned wafers/die, molding (e.g., compression molding, molded underfill), through silicon vias, wafer level packaging and 3D packaging.
- Government and Private research institutes are increasing their investment in this area. A list of

  Consortia addressing Assembly and Packaging development can be found in the Assembly and Packaging tables.
- Consumer product companies are driving innovation in SiP and other new system integration architectures.

Even with this increased investment the current level may be inadequate to meet the Difficult Challenges within the Roadmap time frame. The acceleration of investment and the efficient coordination of development among groups will be necessary to achieve the scheduled Roadmap milestones for assembly and packaging. A major objective of this chapter is to encourage and facilitate the coordination and focus of these efforts to meet the Difficult Challenges.

*Table AP1 Difficult Challenges*

# SINGLE CHIP PACKAGING

## OVERALL REQUIREMENTS

Electronic products continue to find applications in traditional markets for data processing, communication and computing as well as new applications in personal communication such as smart phones and PDA, game consoles, home and home entertainment, medical and health care, green and energy conservation, automotive, and security systems. In this chapter the packaging and assembly technology requirements are divided into devices serving five different market segments:

- Low cost low end: Low end consumer electronics and memory, e.g. electronics in household appliances, toys, MP3, DVD players, portable hard sic drive portable products, electronic books, and low end phones.
- Mobile Products: cell Phones and smart phones, portable personal devices, portable video systems.
- Cost Performance: PC, Notebook, Netbook, Blade Server and Processors, Game Consoles, and small business routers and servers.
- High End : High performance servers, routers and computers
- Harsh Environment: Automotive, aerospace, and military systems

There will be gray areas between the five market segments. While the very low end cell phone belongs to the low end market, it is, by definition, part of the mobile market. While the game consoles performance rival those of blade servers, the market drive for portable video entertainment will, inevitably, elevate the speed and bandwidth for mobile products.

For each of the five market segments, their technology requirements, cost per pin, die size, power, package pin count, operating characteristics, and environments, have been addressed in Table AP2. Where solutions are not proven or unknown, they will be color coded to show the solution status. In many cases the reason for the color is not that the parameter cannot be met, but that the cost of implementation would be beyond the cost targets for that specific product segment.

The technology requirement for the Cost Performance Market has been the leader for package technology innovations in the past decade with the drive for performance in notebooks, game consoles, routers, and servers as the technology nodes advances while keeping cost at bay. The leading package technologies are flip chip ball grid array organic packages with large die and high density. The issues have been speed, heat dissipation, reliability and cost. The rise of the mobile market with cell phones, smart phones, smart phones, portable personal devices, and portable entertainment systems has brought up a different set of technology challenges in form factor and weight, functional diversification such as RF and video, system integration, reliability, time to market, and cost. The packaging community has responded with wafer level packaging, new generations of flip chip CSPs, various forms of 3D stacked die and stacked packages, fine pitch surface mount and 3D IC. They illustrate the dynamic nature of the Packaging and Assembly world in “More Moore” and “More than Moore”. As the decade closes the transition from lead based solder, and the implementation of low k and E low k dielectric and finer bond pad pitch adds a new set of challenges to the packaging technologists. Finally, the continued rising price of gold works against consumer markets expectation for cost reduction.

*Table AP2 Single-chip Packages Technology Requirements*

### ELECTRICAL REQUIREMENTS

Manufacturing tolerances have a major impact on the performance of electrical designs. The manufacturing tolerance roadmap reflected by the tables, for via diameter, via alignment, metal thickness, line width and dielectric thickness must be aligned with the electrical requirements. The major issues defining requirements for single chip packages are discussed below.

### CROSS TALK

Circuit speed and density continue their improvements from one CMOS generation to the next. Faster circuits translate into shorter clock cycles and increased density gives rise to more closely spaced parallel threads. These device advancements demand increased package I/O at ever-increasing speed. These advanced circuits require packages that minimize device, package, and system noise

A major noise source is crosstalk between parallel signal lines. Crosstalk noise is roughly proportional to the ratio of dielectric thickness to edge spacing between adjacent signal lines. For a given signal line width and spacing, a lower dielectric constant medium requires a thinner dielectric to obtain the same characteristic impedance, resulting in smaller crosstalk noise. Cross talk issues are also associated with fine pitch bonding wires and fine pitch vias.

### POWER INTEGRITY

Power integrity issues are becoming more critical for high-speed integrated circuits as frequency and increases and operating voltage decreases. Discrete decoupling capacitors are extensively used today to damp AC noise. The Equivalent Series Inductance (ESL) associated with discrete capacitors is the major factor limiting performance at high frequency. Embedded planar capacitors and on-die decoupling cells are used to reduce high-frequency noise due to high ESL in discrete capacitors. The cost and complexity of on-die decoupling will be an increasing problem. Due to resonance between package and die and package and PCB, it is difficult to control power distribution impedance over a wide frequency range. This results in a packaging related bottle-neck in high-speed power delivery system design and new technology is required.

### THERMAL REQUIREMENTS

Temperature control is critical for the both operating performance and long term reliability of single chip packages. The high junction-to-ambient thermal resistance resulting from an air-cooled heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of this roadmap. Today, a massive heat sink, which may be larger than the chip by orders of magnitude, is attached to a silicon chip through a heat spreader and variety of thermal interface materials (TIM). Not only does this insert a large thermal resistance between the chip and the ambient, it also limits the chip packing density in electronic products thereby increasing wiring length, which contributes

to higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses. The ITRS projected power density and junction-to-ambient thermal resistance for high-performance chips at the 14 nm generation are >100 $W/cm^2$ and <0.2 °C/W, respectively. The main bottlenecks in reducing the junction-to-ambient thermal resistance are the thermal resistances of the thermal interface material (TIM) and the heat sink. There is a need for TIMs that provide the highest possible thermal conductivity, are mechanical stable during chip operation, have good adhesion, and conform to fill the gaps between two rough surfaces. To address this need, new TIMs are being explored. The integration of carbon nanotubes (CNTs), which exhibit very high thermal conductivity, within a TIM's matrix is being investigated. More detail on these materials can be found in the *Emerging Research Materials* chapter.

### HOT SPOTS

Hot spot thermal management generally dictates the thermal solution of the component. Even when the total power of a component is unchanged, hot spot power density increase could limit the device performance. While this is a critical issue for SiP it is also important for single chip devices such as SoC circuits, high power lasers and diodes, RF devices and other high power devices that have portions of the die generating thermal loads substantially higher than the die average.

New liquid and phase change (liquid to gas) active heat sinks are in limited use today and are addressed in more detail in the System in Package section of this chapter. They hold the promise of decreased thermal resistance and improved heat spreading capability to address the effect of hot spots.

### MECHANICAL REQUIREMENTS

The constant drive for increased functionality and flexibility in the end product will be the key driver for the electronic industry in future. With shorter design turns and faster time to market, there is little room for error during the design, development, and validation phases. The continued geometric scaling of integrated circuits and the introduction of low-κ dielectric film materials raise concerns about mechanical stress damage in the dielectric layers due to thermo-mechanical stresses in the combined package device structure. Legislative requirements for lead free and halogen free materials in electronic products introduced higher temperature stresses and new packaging materials and materials interfaces into the package. New package types including stacked die packages, Package on Packages (PoPs), Package in Packages (PiPs), and wafer level packages have brought forth new failure mechanisms. The packaging industry will face the challenge of integrating multiple device technologies such as digital, RF and MEMS, optoelectronics, displays and others on the same packaging platform. Expanding consumer markets introduced new paradigms in reliability requirements. For example drop tests, in various forms, are being added to components to be used in cell phones and other portable electronic products. To ensure reliability of the end products, it is imperative to have focused R&D efforts in mechanical and thermal modeling and simulation tools.

## MECHANICAL MODELING AND SIMULATION

Electronic packages represent a classic case of convergence of multi-scale, multi-physics, multi materials, and multi-materials interface systems. The length scale varies from nm to cm, a wide range of materials with mechanical properties from stiff and brittle inorganics like Si, glass and other dielectrics with property modifications such as micro-pores to achieve low-κ, to softer materials like solders or polymers and polymer composites with very non-linear time and temperature dependent material behaviour are combined. Material response varies from elastic to non-linear in time-temperature dependent characteristics. It is critically important to have practical and usable tools for predictive thermal mechanical and dynamic modeling of electronic packaging structures to assist packaging engineers in predicting failure modes and elucidate the failure mechanisms in the development stages. This would enable trade-offs in design, materials and manufacturing processes, and ultimately in feature, performance, cost, and time to market. Such predictive modeling tools would need to be integrated into device package co-design environments. Coupled analysis for thermal, electrical, hydrothermal, and mechanical characteristics is also needed.

To complement mechanical analysis and modeling efforts, it is necessary to develop accurate materials properties data over a range of loading and environmental conditions. Characterization of interface properties such as polymer/metal and polymer/polymer interface fracture toughness and micromechanical properties is required. A key challenge in this area is associated with the small dimensions. Bulk properties are often not usable for thin material layers. Interface effects, grain size and pre-stresses due to process or adjacent materials become very important. Metrologies are needed that can handle thin films of sub-micron thickness to measure both bulk and interfacial response. Properties of materials such as intermetallics formed from solder under bump metallurgy (UBM) metals interaction which grow and evolve over time and temperature will be required. Physical failure mechanisms such as electromigration, thermal migration in combination with mechanical stresses need to be understood and modeled for practical life assessment.

There is also a need to develop metrologies that can be used to efficiently measure either stress or strain under both thermal and mechanical loading conditions in thin films (for example in layers within Silicon) in packaged form. For

example, interferometry-based techniques with sub-micron resolution are required whereas the current state of art methods have spatial resolution of 1 to 2 µm. Efforts are needed in extending other known techniques such as digital image correlations, micro-Raman spectroscopy, and PZT sensors to sub-micron length scales.

## COST

The continuous reduction in cost per function has been the key to growth of the electronics industry. This has been achieved historically through scaling of the wafer fabrication processes and improvements in design. The cost of assembly and packaging has not kept pace with the cost reduction in wafer fabrication and today packaging costs often exceed silicon IC fabrication cost. The cost reduction challenge is made more difficult by several factors increasing cost of packaging. Cost of packaging materials such as bonding wire, molding compound, substrate, contributes substantially to the cost of the package. For example more than 70% of devices are packaged in wirebond. The cost of gold wire is a substantial portion of the package cost. Lead-free solder materials, halogen free molding compounds, low-κ dielectrics, and high-κ dielectrics are more costly than the materials they replace. Higher processing temperatures and a wider range of environmental temperature associated with portable consumer electronics require new, more expensive, substrate and interconnect technology. The increasing power density and decreasing junction temperature require more efficient thermal management. The details of the chip to package substrate technology are covered in Table AP3 and the specific issues associated with package warpage during processing are covered in Table AP5.

New technology is required to meet the demand for more cost effective packaging. Wafer-level packaging and systems in a package (SiP) are among the innovative approaches to reduce cost and achieve advantages of scaling similar to the front end processes.

*Table AP3 Chip-to-package Substrate Technology Requirements*

*Table AP4 Package Failure Modes*

*Table AP5 Substrate to Board Pitch*

## RELIABILITY

Rapid innovation in packaging is evident from the introduction of new package formats including area array packages (flip chip BGA and flip chip CSP); leadless packages, direct chip attach, wafer level packaging (WLP), wirebond die stacking, flip chip-wirebond hybrid, PoP, PiP and other forms of 3D integration and others. In addition there are new packaging requirements emerging such as Cu/low-κ materials, interconnects to address the need for flexibility and expanding heat and speed requirements. The introduction of low k and E-low k materials makes the low k layer in the chip susceptible to mechanical stresses in the combined chip package structure. New environmental constraints such as Pb-free and halogen-free requirements enforced by law, and use of electronics in extreme environments also force rapid changes. The introduction of these new materials and package architectures are posing new reliability challenges. For example in the flip chip package the interaction of the stiffer Pb free solder bump to the mechanically weaker low k dielectric requires chip and design and materials selection to address reliability risks in chip to packaging interaction (CPI). This comes at a time when there must be substantially higher reliability on a per transistor basis to meet market requirements. Many of the reliability issues involve the Chip to Package Substrate Technology which is covered in Table AP3.

Some new package designs, materials, and technologies will not be capable of the reliability required in all market applications. More in-depth knowledge of failure mechanisms coupled with knowledge of end product use conditions will be required to bring reliable new package technologies into the market-place. For example mobile products have drop test requirements for dynamic mechanical integrity in drop impact environments.

There are many factors that determine the reliability of electronic components. The factors that must be considered are similar for all systems but the relative importance changes for consumer products. Consumer products have higher thermal cycle count due to the use pattern of consumer electronics and greater mechanical stress due to vibrations and dropping for the same reason. Typical package failure modes are presented in Table AP4.

The storage and use environments also have a wider range than components not used in consumer applications. Meeting the reliability requirements for future components will require tools and procedures that are not yet available. These include:

- Failure classification standards
- Identification of failure mechanisms
- Improved failure analysis techniques
- Electrical/thermal/mechanical simulation
- Lifetime models with defined acceleration factor
- Test vehicles for specific reliability characterization
- Early warning structures

As described earlier, the use of low-κ ILD to reduce on-chip interconnect parasitic capacitance has exacerbated the difficultly of maintaining high thermomechanical reliability of die assembled on organic substrates in flip chip packages. Due to the fragile nature of low-κ ILDs in the die and their relatively poor adhesion to the surrounding materials, it is becoming progressively critical to minimize stresses imparted on the chip during thermal cycling and wafer-level probing. The large CTE mismatch between the silicon die (3 ppm/°C) and the organic substrate (17 ppm/°C) have been shown to be destructive for ILD materials and their interfaces. This issue has motivated the investigation of new I/O interconnect technologies that minimize mechanical stresses on the chip. The pending replacement of lower modulus lead solder bump material by lead free solder bump material or copper pillar makes the problem more difficult. To this end, the device and package communities must collaborate together to address the chip package interaction issue in the design of UBM structure, solder bump or Cu pillar, underfill materials, and surface finishes. In addition, the use of solder bumps augmented with mechanically flexible electrical leads to replace underfill is a potential solution.

In addition to compliant/flexible interconnects, thin solder interconnects and micro-bumps (diameter: <20 µm) as well as Cu pillar bump structures (Figures AP1 and AP2) are used to improve interconnect reliability. The selection of the type will depend on die sizes, thickness and interconnect density.

Moving forward reliability considerations of dies with TSV and microbumps will pose significant challenges to the chip and package designers and their reliability counterparts. This will be addressed in future editions for the roadmap.

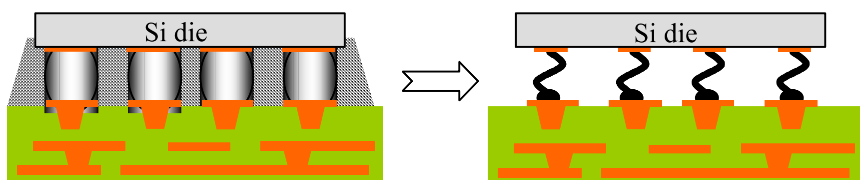
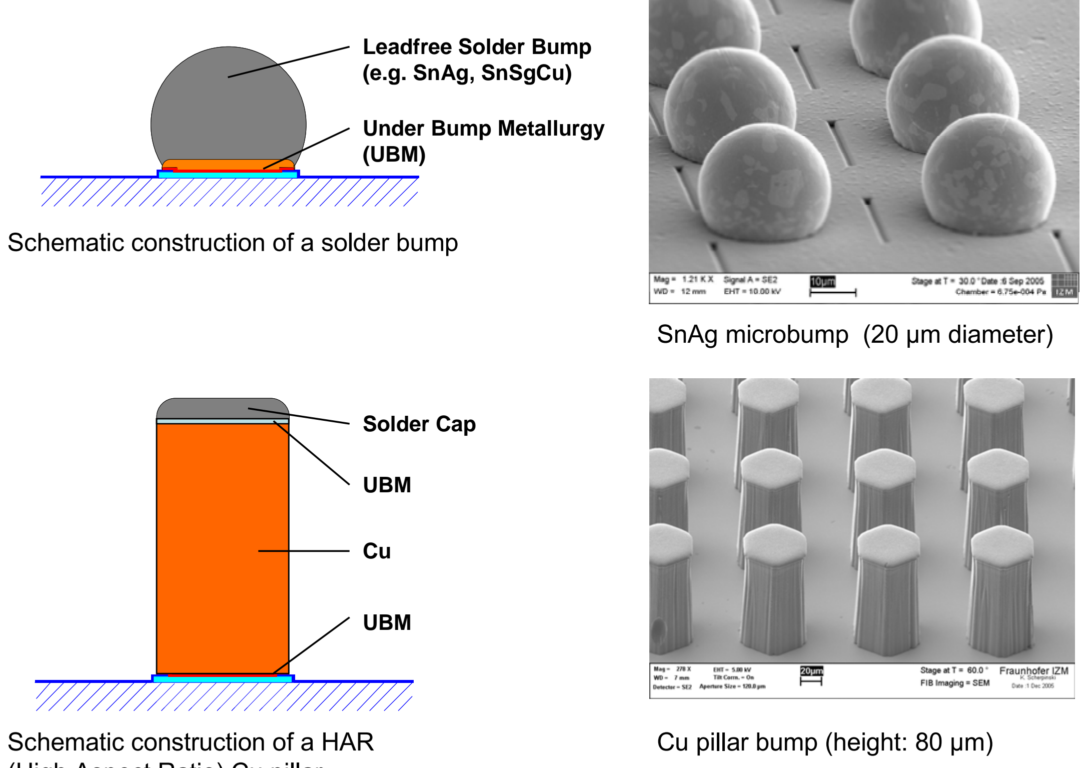



*Figure AP1 The Use of Compliant/Flexible I/O Can Potentially Eliminate the Need for Underfill*




Schematic construction of a solder bump

SnAg microbump (20 µm diameter)

Schematic construction of a HAR (High Aspect Ratio) Cu pillar bump with solder cap

Cu pillar bump (height: 80 µm)

*Figure AP2 Micro Bump and Pillar Bump Structures for High Reliable Chip-to-substrate Interconnects*

## CHIP TO PACKAGE SUBSTRATE

There are several factors that drive the selection of the appropriate chip to package substrate technology. The issues are addressed in *Table AP3*: Chip to Package Substrate Technology, *Table AP5*: Substrate Board Pitch and Table AP6: Package Warpage at Peak Processing Temperature. The specific technologies are discussed in the sections below.

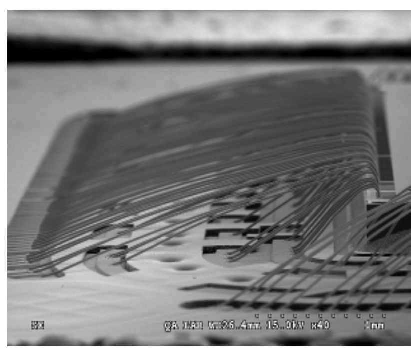
*Table AP6 Package Warpage at Peak Processing Temperature*

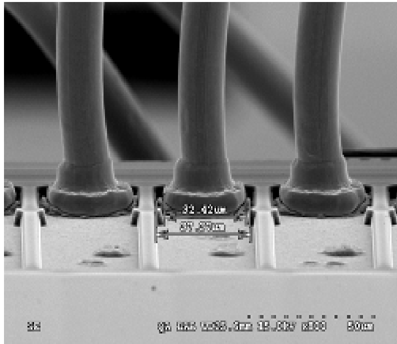
### *WIRE BONDING*

Wire bonding has been the workhorse of the semiconductor industry. It is the dominant method for interconnecting to semiconductor device. IC devices, wire bonded to various forms of lead frames and organic substrates and molded in epoxy molding compounds have been the standard of the industry for years. Despite repeated predictions that wire bond technology has reached its practical physical limit, wire bond technology continues to re-invent itself with new innovative concepts and technology improvements. Multi-tier wire bonding has provided good practical solutions to meet increased IO requirements. Wire bonded stacked die packaging, typically with two to five vertically stacked dies with a leadframe, laminate substrate or flex circuit base has proven to be particularly versatile method for multi-chip or SiP in the mobile market. While the majority is for various memory to memory combinations, a significant proportion involves memory stacked with logic devices. The developments that enabled die stacking package include wafer thinning, low profile wire bonding, mold compound flow and filler size, and wafer level test for known good die. The requirements for finer pad pitch spacing and lower materials cost has led to development for finer diameter gold wire. Today 16 um gold wire is in qualification while 12 um gold wirebond is in development. Figure AP3 shows a 16 mil gold wirebond package.

Since the publication of 2007 ITRS, fine pitch copper wirebond has been introduced into the industry mainstream. Replacement of Au wire by Cu is the last frontier for packaging materials cost saving. At the same time the introduction of advanced nodes and low k materials will demand finer diameter wires for Au as well as Cu below the 18 um being

practiced today. While copper wirebond has been in use for power devices with 50 micron diameter wires and low IO counts, fine pitch Cu wirebond is a recent development. Fine pitch applications with Cu wire diameters at 25 micron and below requires improvements in understanding of wire properties, IMC formation and evolution, wire bonding processes and equipment development and control for wire oxidation. Pd coated wire has been introduced to eliminate the need to for forming gas in production. Shown below in AP3 is an example of an 18 um Cu wirebond in PBGA.





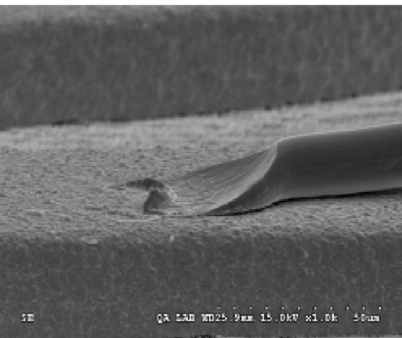




*Figure AP3 Examples of 18 um Cu wire bond in PBGA*

In order to meet thinner and more densely integrated package requirements lower profile wire bond loops are necessary. Innovations such as forward bond loops with 50 µm loop height are in production. Other innovations such as die to die bonding, cascade bonding, and bonding overhang die are shown in Figures AP4, and AP6. While many of these developments have been in production for Au wires, it is expected that these capabilities would be extend Cu wirebond in time.

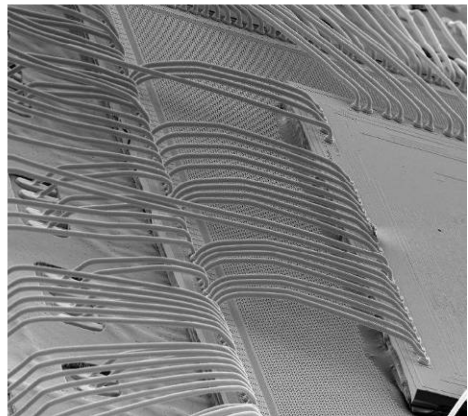
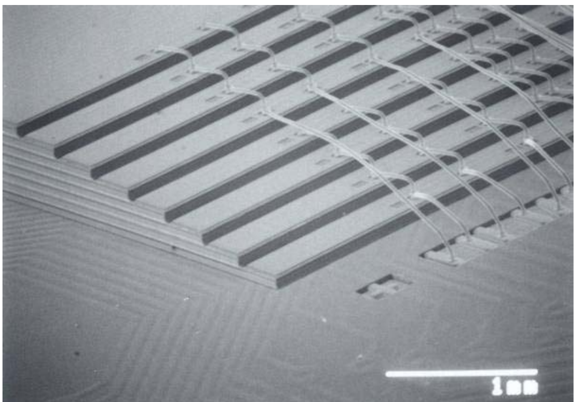


*Figure AP4 Example of Low Profile Bond Loop Die- to- die Wire Bonding*



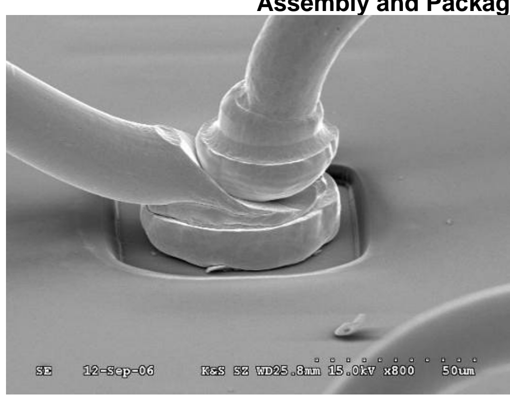




*Figure AP5 Example of Cascade Bonding and Die to Die Bonding*

Some of the technology issues being addressed are bonding overhang die and wire bonding on both sides of the lead frame shown in Figures AP6 and AP7.

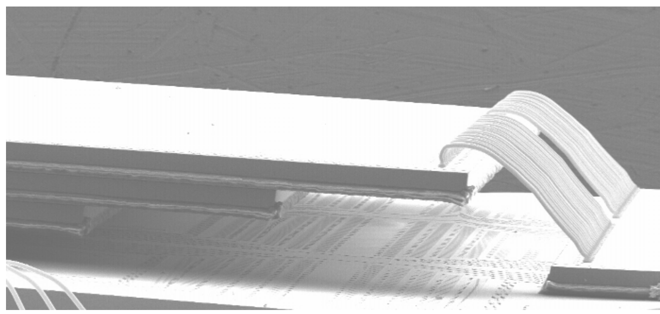


*Figure AP6 Bonding Overhang Die*

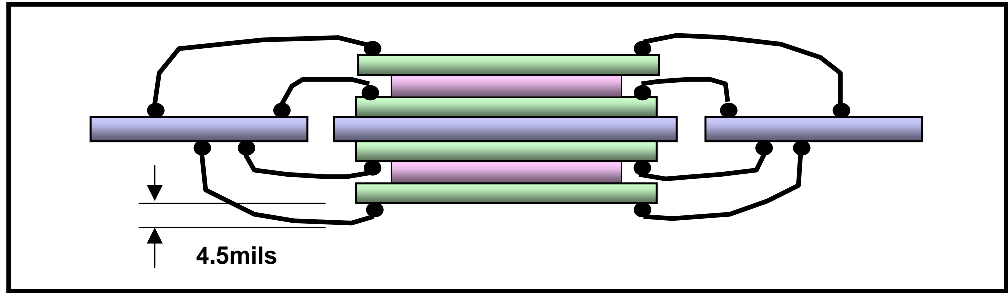


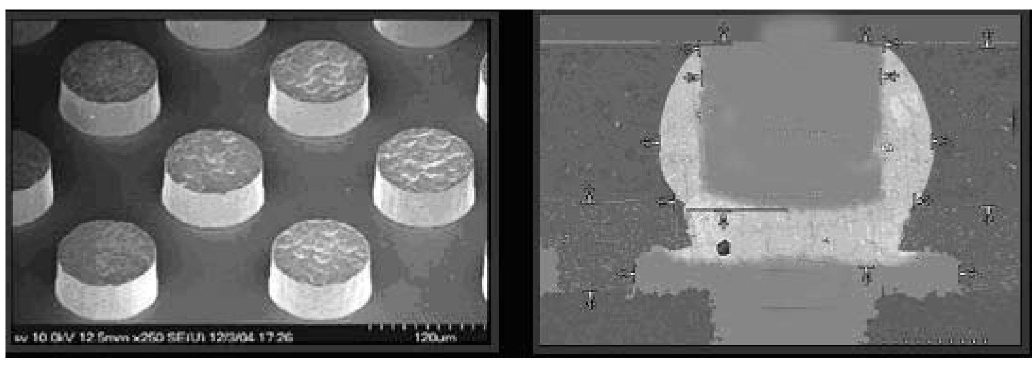

*Figure AP7 Wire Bond on Both Sides of Lead Frame Substrate*

There is a well established global infrastructure and supply chain for wire bonded and molded packages from design practices and tools, materials, manufacturing processes, and equipment. The industry has been developing faster wire bonders, larger format substrate assembly, and more efficient molding processes to address the market demand for efficiency and cost saving. The next few years will see significant innovations in design, process, materials and equipment for the implementation of Cu wirebond. As the wafer technology approaches 45 nm node and below, the bonding wire diameter will be reduced correspondingly to 20 nm and below. In the long term such cost improvements efforts may be approaching their practical limits and are of diminishing returns.

### *FLIP CHIP*

Flip chip and wire bond are the two standard processes to connect die to a substrate. Flip chip PBGA processes evolve from technologies originally developed for multi-chip applications on ceramic modules with high lead solder bumps. It

has become the standard die interconnect solution for organic substrates for microprocessors and graphics processors in the cost performance and high end markets. The key elements are: wafer bumping (UBM and bump metallurgy), underfill, TIM, and build-up substrates. For these applications flip chip pitch, lower than 150 µm, has been limited by availability of high-volume cost-effective substrates and high-volume defect-free underfill processes, with higher Pb-free temperature, higher Tj, and increased current density, there are requirements to improve underfills, UBM structure, high lead solder, eutectic and lead free alternatives, and TIM materials in order to meet the demands of future technology nodes and market applications. Plated wafer bumping including copper pillar wafer bumping is being introduced in microprocessor applications and will be expanded to broader applications. The advantages are in finer pitch, lead free and electrical/thermal performance.



*(a)* *(b)*

*Figure AP8 Examples of Copper Pillar Bumps (a) and Assembled Copper Pillar (b)*

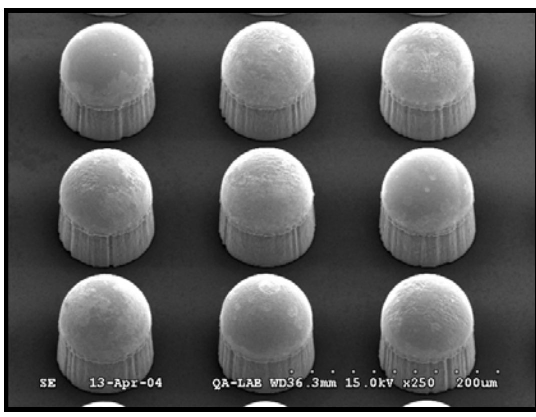



*Figure AP9 Example of Copper Pillar Bumps with Solder Tips*

For applications beyond the microprocessor, graphics and game processors, flip chip FC CSP packages have been developed for applications with smaller die, lower IO array pitch and low profile small package format requirements. Primary driver has been the mobile market application, and drop test is an important requirement. Laminate substrate and 1+2+1 buildup substrates are used to meet cost targets. These flip chip CSP packages may have multiple dies side-by-side or they may be stacked onto other flip chip and wire bond packages. Analog and RF ICs have different electrical requirements than digital only applications. The industry has developed several package variations to meet different application requirements, In addition to the classical underfill process, they include molding and underfill plus molding processes. The large format overmolding process (no underfill) provides significant cost saving. Potential solutions include redesigned UBM, copper pillar or flexible interconnect, fluxless reflow and PoP and PiP package structures. There is a movement for a new generation of flip chip structures, materials, manufacturing processes and equipment sets to serve the industry for the More than Moore era.

### *Molding*

Conventional bottom-gate molding has been a highly successful workhorse for the industry. For some complex stack dice and complex SiP package there is risk for excessive wire sweep and yield loss. New developments in top center mold gate (TCMG) provides a radial mold compound flow from a top gate that minimizes wire sweep and filler separation that can occur as the fine pitch bond wires filter out part of the fillers as the compound moves between them.

Also compression molding is entering the mainstream. The liquid mold compound is dispensed onto the substrate before it is placed into the mold die. No gate is needed and the mold flow speed is minimized preventing wire sweep. A new approach presently under investigation is underfill molding for flip chip in package solutions.

Thin packages are prone to warpage, and chips with low-κ dielectrics are more sensitive to stress. In both cases, low modulus molding compounds are in development to minimize the problems.

A novel approach to reduce or eliminate the occurrences of wire shorts in molding is the use of coated wire. Coated wire has been in development for some years and has achieved some level of technical success. However the high cost of coated wire has limited its application and prevented its broad proliferation into the industry.

## Package Substrate to Board Interconnect

### *Lead Frames*

Lead frame carriers have thrived for their low cost and good reliability for more than 30 years. They are expected to continue to thrive with innovations in package design and processes. New material related challenges appeared because environmental and health regulatory requirements demand the elimination of Pb. The move from Pb to Sn led to the challenge of tin whiskers. For improved reliability and low-cost new plating materials are required, e.g., based on NiPd, Cu, lead-free solder alloys. Other challenges include improved heat dissipation and higher interconnect density including increased pin count capability for platforms such as QFN and QFP. Innovations in advanced multi-row QFN has extended the I/O and performance for QFN packages.

### *High Density Connections*

The density of connections between the package substrate and the system printed circuit board continues to increase and the size of devices for a given functionality and the number of contacts required continues to increase. The Roadmap for chip to package substrate pitch is found in *Table AP5*.

The increase in pin count is driven by the requirement to maintain power integrity and the increasing width of the data communication. Ensuring power integrity in an environment where operating voltage is decreasing and the number and speed of the transistors is increasing requires a larger number of contacts to handle the larger current spikes without fluctuations in power or ground. The slow improvement in board line width and spacing would provide some board routing density increase, but there is better opportunity for this density increase by reducing BGA pad pitch on board and package.

The greatest contact density in conventional packages will be available for the fine pitch ball grid array (FBGA) packages which are projected to reach 100 µm area array pitch in 2014. The higher density and resulting smaller pads bring issues related to joint reliability and package ball co-planarity requirement. The joint reliability needs to be achieved through innovations in pad design, innovations in solder metallurgy and surface finishes, and in some cases use of board level underfill. The co-planarity issue needs to be addressed through improvements in substrate material and design, better understanding of package behavior at high temperature, and working with process flow to do key co-planarity sensitive operations prior to solder ball attach. The package to printed circuit board pitch for existing package types is presented in *Tables AP5* and *AP6*. Greater contact density will be in use for die-to-system substrate and die-to-die interconnect architectures using TSV structures.

## Package Substrates

Package substrates are both the most expensive element of packages as well as the factor limiting package performance. Innovation in package substrate technology is required to meet the cost and performance projections of the Roadmap. The substrate properties required to meet each market demand are shown in the following tables:

*Table AP7* *Package Substrates: Low Cost (PBGAs)*

*Table AP8* *Package Substrates: Hand-held (FBGA)*

*Table AP9 Package Substrates: Mobile Products (SiP, PoP)*

*Table AP10 Package Substrates: Cost performance (CPU, GPU, Game Processor)*

*Table AP11 Package Substrates: High Performance (High End)*

*Table AP12 Package Substrates: High Performance (LTCC)*

### FOR LOW-COST APPLICATIONS—LAMINATE FOR PBGA

PBGA is a relatively large-size package and mostly used for low-cost applications, demanding substrates in low cost, high volume production, and are mostly two- or four-metal layer laminates. *Table AP7* shows the roadmap of laminate for low-cost applications. Their roadmaps tend to be moderate based on the traditional manufacturing processes with critical cost constraints. Increasing strip sizes are the trend of package substrates to provide higher productivity in package assembly and materials utilization. Assembly equipment must meet the increasing strip sizes, e.g., molding press must be designed to have larger die-set bases with higher clamping pressures. Equipment suppliers need the guidelines for increasing strip sizes, although they differ among package manufacturers. Lowering material costs is another challenge. The core material of the substrate, high Tg FR4, dominates the physical property of package substrate; thus, package manufacturers are accustomed to specify the product number of core material for their substrates. Standardizing the properties of core materials and substrate frame size is necessary to accelerate the market competition. In terms of quality requirements, package warpage during reflow is a significant problem for this package due to its large body size. One of the approaches to reduce package warpage during reflow is matching the properties of the substrate and molding compound. Lower CTE and higher fracture modulus of the substrate will mostly mitigate the warpage.

### HAND-HELD APPLICATIONS—FINE LAMINATE FOR FBGA

Handhelds are driving ever thinner substrates and finer patterns with laminate (See *Table AP8*). These requirements result can drive smaller panel sizes in substrate manufacturing processes for accurate alignment and finer pattern as one solution. Total thickness has been reduced to 100 µm based on 60 µm cores in high volume manufacturing. 50 µm cores and 35 µm prepregs are available but cost is still high and improvements in handling equipment are needed to take these materials to high volume. Below 35 um thickness, new high performance low cost material is required to meet the market needs.

### MOBILE APPLICATIONS—BUILD-UP SUBSTRATE FOR SIP

Mobile packages with wire bonded die are utilizing high density substrates with blind vias in laminate, essentially a build-up technology using prepreg instead of unreinforced resin. To achieve finer resolution (See *Table AP9*), glass cloth with more uniform glass fiber density or glass mats will have to be developed while overall thickness of the resultant prepreg has to be reduced below 40 µm. Thereafter, film forming resin systems with wire bonding resilience after lamination will have to be developed. In general, the lack of the latter type of materials is impeding the improvement of resolution of lines and spaces. The pattern formation itself is shifting from a subtractive process to pattern plating.

Mounting flip chip die and wirebond die on the same package, either side by side or stacked, provide challenges for substrate surface finish. A number of finishes can coexist: organic solder preservative (OSP), immersion tin or pre-solder with electroplated nickel/gold versus electroless nickel immersion gold (ENIG) with electroplated nickel/gold. Each case requires a carefully tuned assembly and substrate manufacturing process to be successful in high volume. Hence, the search for a universal surface finish has been reinvigorated and electroless nickel electroless palladium immersion gold (ENEPIG) seems to be the most likely candidate. This surface can be wire bonded, flip chip soldered as well surface mount soldered. The cost of this universal finish seems to be competitive with mixed finishes.

### COST PERFORMANCE APPLICATIONS—BUILD-UP SUBSTRATE FOR FCBGA

The advent of organic substrates changed the structure of flip chip packages to through-hole technology based on printed wiring boards in contrast to the stacked-via approach of ceramics. The invention of build-up technology introduced redistribution layers over cores. While the build-up layers employed fine line technology and blind vias, the cores essentially continued to use printed wiring board technology albeit with shrinking hole diameters.

As copper thickness shrinks in traces and plated through holes, these features become susceptible to thermal expansion in the z-direction. Hence, CTE in z-direction must be reduced to 20 ppm/degree for core materials (See *Table AP10*). The

typical approach is to add filler to the resin system which typically degrades other material properties or introduces process disadvantages.

Adhesion of copper traces has been primarily by physical adhesion: rough, dendritic copper anchored in the resin. This anchoring treatment results in larger surface roughness, exacerbating conductor loss. The latest developments are primers which are applied with the help of Cu foil and will provide chemical adhesion to the electroless Cu of pattern plated Cu. The primer provides a smooth surface and chemical adhesion thereby enabling much tighter trace pitches. Instead of primers, adhesion promoters based on porphyrene chemistry may be used to provide adhesion to electroless Cu or smooth Cu foil. Soldermask is emerging as another challenge for flip chip substrates. Planarity and thickness need to be controlled more tightly in the future. Dry film materials can achieve the requirements but cost is still too high for wide spread implementation.

### *HIGH PERFORMANCE—LOW κ DIELECTRIC SUBSTRATE FOR FCBGA*

High-speed transmission characteristics drive the demand for ever decreasing dielectric constant and low loss materials. Incremental materials improvements enable κ~3.4 today (See *Table AP11*). Materials are available with κ down to 2.8 but are still far too expensive for broad market application. There is no cost effective solution available for κ~2.5 and below. For such low κ, new reinforcement materials need to be developed. Thermoplastic resins with high heat resistance based on olefine systems seem feasible as well as new materials discussed in the Emerging Research Materials chapter of this Roadmap. These include the development of porous systems. Dielectric loss needs to be reduced by one order of magnitude. While PTFE and some cyanate resins achieve this, cost effective solutions are not yet available.

The next step in the evolution of substrates was to develop high density cores where via diameters were reduced to the scale of blind vias, i.e., 50 µm. The initial applications were based on PTFE dielectrics with metal alloy cores to manage package stresses. The full advantage of the dense core technology will be realized when lines and spaces are reduced to less than 25 µm. Thin photo resists (<15 µm) and high adhesion, low profile copper foils are essential to achieve such resolution.

In parallel, coreless substrate technologies are being developed. One of the more common approaches is to form vias in a sheet of dielectric material and fill the vias with metal paste to form the basic building block. A second building block is formed by laminating copper foil on both sides of the basic building block. Subsequent circuitization completes this second building block. By laminating the appropriate selection of building blocks, a raw substrate is formed which only needs external finishing. Variations of this process are to form the building blocks on carrier sheets as single layers of circuitry which are the transferred by lamination to the composite stack. In either case, the dielectric materials have little or no reinforcing material. Control of dimensional stability during processing will be essential. While different coreless technologies with proprietary designs and processes are emerging, significant market development is required to broaden the supply base, ensure stable quality and force cost reduction. Currently, coreless substrates are not in high volume production applications because these substrates have a tendency to warp during assembly. High volume assembly requires greater substrate stiffness with improved tolerance for warpage. The environmentally driven modifications to improve temperature robustness for lead-free assembly and to achieve halogen-free flame retardation are nearing completion for their first generation.

The primary advantages of Low Temperature Co-fired Ceramics (LTCC) over conventional $Al_2O_3$ ceramics for high performance applications are a significantly lowered dielectric constant, Dk, and conductor resistivity. In addition, the thermal coefficient expansion (TCE) of LTCC substrates more closely matches silicon than organic substrate materials. The combination of low dielectric constant, Dk, low dissipation factor, Df, high electrical conductivity, and matched Si/substrate TCE make LTCC an attractive material for high power, large die, high performance applications (See *Table AP12*). Future development challenges include establishment of finer pitch metallization printing and high-productivity laser vias to improve routing density. Laser vias also allow for lower-cost, quick-turn prototyping, compared to conventional mechanical via punching. The ball diameter will continue to decrease as the interconnect pitch reduces as shown in Figure AP10 below. This will cause additional challenges for production processes and reliability

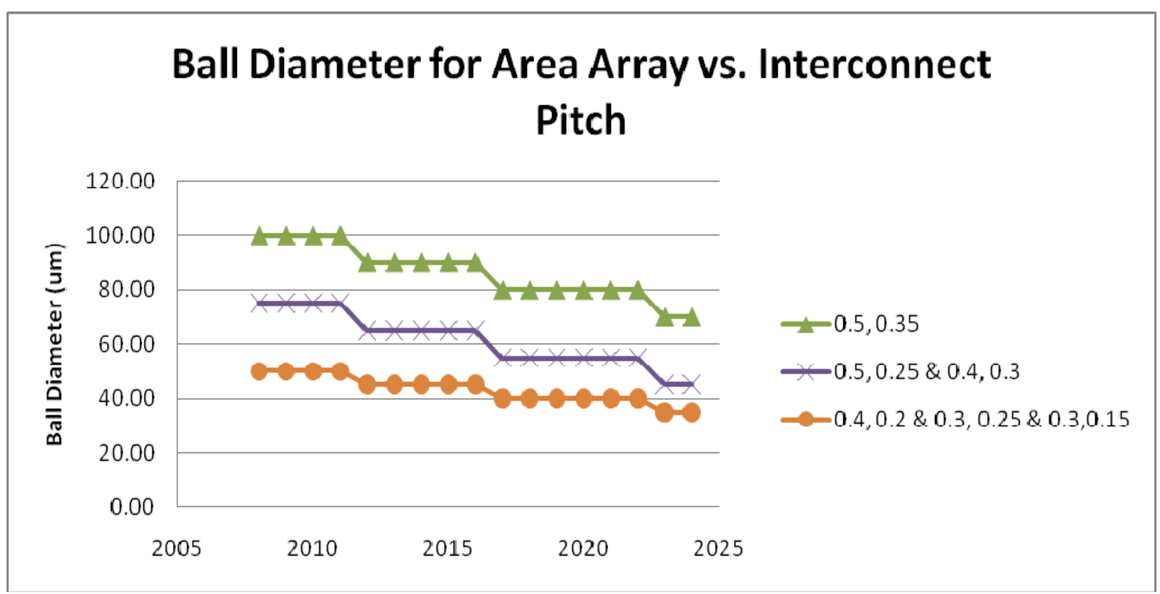



*Figure AP10 Ball Diameter for Area Array versus Interconnect Pitch*

## WAFER LEVEL PACKAGING

Wafer level packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at the wafer level. The original WLP definition required that all package IO terminals be continuously located within the chip outline (fan-in design) producing a true chip size package. This definition described a Wafer Level Chip Scale Package, or WLCSP, with the processing of a complete silicon wafer. From a systems perspective, under this definition, the limitation on WLP was how many I/O could be placed under the chip and still have a board design that can be routed. WLP can provide a solution when requirements for a continued decrease in size, increase in IC operating frequency and demand for cost reduction are not met by traditional packaging e.g. wire bonding or flip chip bonding.

However, there are products coming to market that do not fall under this earlier definition of WLP. These new packages have been described as "Fan-out" WLP. They are processed by placing individual sawn die into a polymer matrix that has the same form factor as the original silicon wafer. These "Reconstituted" artificial wafers are then processed through all of the same processes that are used for "real" silicon wafers, and finally sawn into separate packages. The die are spaced in the polymer matrix such that there is a perimeter of polymer surrounding each placed die. This are can be used during redistribution (RDL) to "fan out" the RDL to an area larger than the original die. This allows a standard WLP solder ball pitch to be used for die that are too small in area to allow this I/O pattern without 'growing" the die to a larger size. With the implementation of this technology, it is no longer only intact silicon wafers that can be processed as a "WLP", but hybrid silicon/polymer matrices in wafer form that also can be now classified as WLP products.

WLP technology includes wafer level chip size packages (WLCSP), Fan-out wafer level packages, wafer capping on a MEMS, wafer level packages with Through Silicon Vias (TSVs), wafer level packages with Integrated Passive Devices (IPD), and wafer level substrates featuring fine traces and embedded integrated passives.

Wafer Level CSP was the first generation of a wafer level package product to be introduced into the market place. Today WLP technology (fan-in WLP) with and without redistribution layers (RDL) are used for a large variety of products. WLPs with fan-in design today are typically for low I/O count and small die sizes, although the I/O count for today's products exceed 150. They are mainly being used in portable consumer markets where small size, thickness, weight, and electrical performance are additional advantages to cost. A major trend is to work for cost efficient rerouting with multi-layer RDL.

With the introduction of TSVs, IPDs, Fan-out, and MEMs packaging technologies, WLP products can be used in a much broader range of applications, with higher I/O counts, and greater functional complexity. These packaging technologies open new opportunities for WLPs in the packaging field.

WLP now incorporates many different structures to meet specific application targets. A variety of WLP types are shown in Figure AP11 below. *Table AP13* presents the technology requirements.

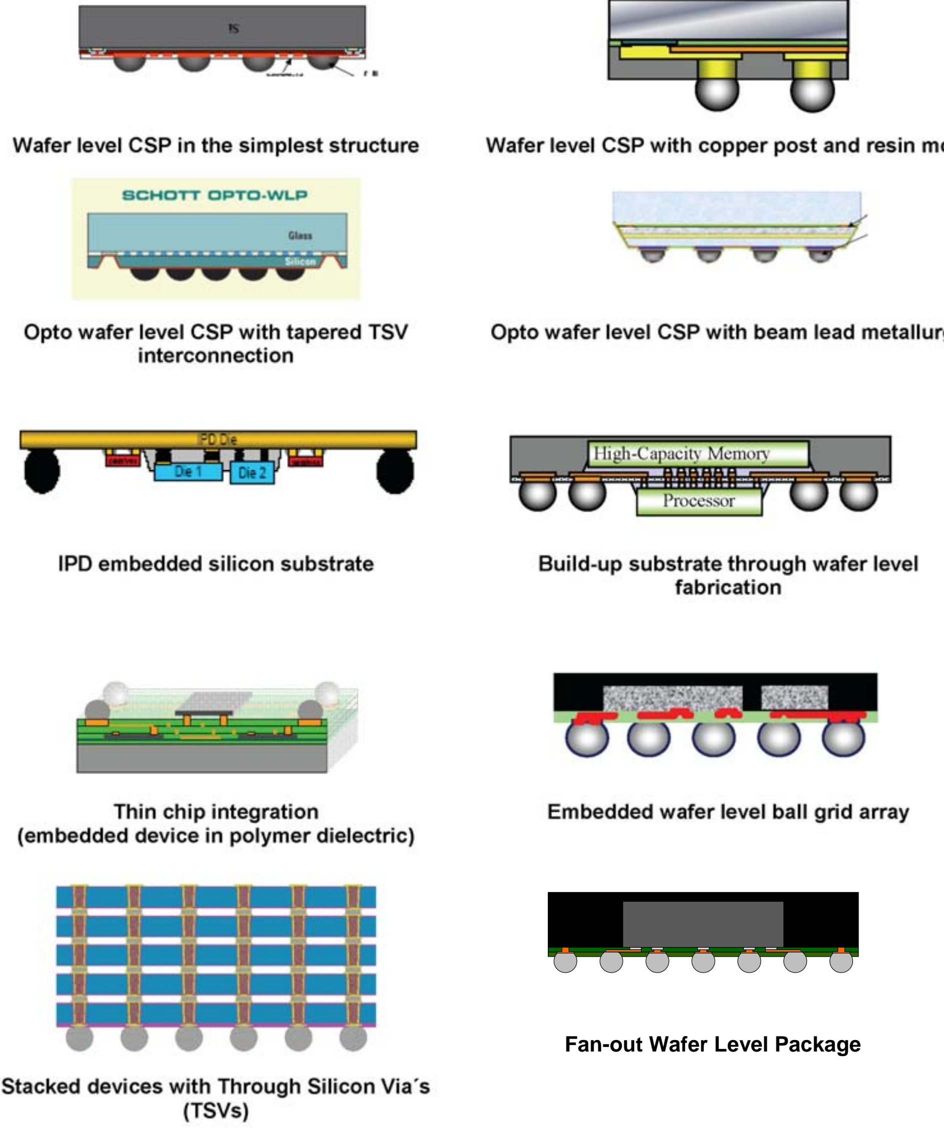



*Figure AP11 Examples of Wafer Level Packaging Types*

*Table AP13 Wafer Level Packaging*

The manufacturing process technology and high volume infrastructure enabling wide spread implementation of Wafer Level CSP in the market place have been based upon the adoption and implementation of established flip chip wafer bumping (under bump metallurgy, solder bumping, repassivation, redistribution, wafer inspection, wafer probing) processes and equipment in the merchant market. The infrastructure has been developed to serve the high volume needs of flip chip packaging in the high performance and cost performance markets.

In contrast to flip chip assembly, WLP assembly typically does not require underfill. For solder joining, solder balls are typically used with a diameter larger than 250 µm. However, for specific applications where low package height is required, smaller solder balls can be used for lower stand-off heights. The smallest pitches used in the market are 0.4 mm. For standard WLP under-fill may be used to meet specific reliability requirements such as drop test.

The traditional drop ball WLCSP designs and processes are being further developed with modifications to the stress absorbing layers, underfill in board level assembly, and stress absorbing bump structures to allow for larger die

applications. Thicker copper trace redistribution features have been introduced for higher reliability, higher power and lower signal loss applications.

The processes developed for copper redistribution are being introduced and extended to the fabrication of copper studs and passive components such as inductors, to be followed by capacitors and resistors. The combination of these components will lead to capabilities for the fabrication of filters and other sub-system circuit elements. Integration of these components into WLP-SiP packages constitutes a next step towards 3D wafer integration.

Memory devices are being used in portable consumer products such as cell phones and PDAs in increasing quantities. WLP offers advantages in these applications, due to inherent lower cost, improved electrical performance, and lower power requirements. Key enabling technologies to take full advantage of WLP for these applications will be the development of cost effective wafer level test and burn-in.

## WAFER LEVEL PACKAGE DEVELOPMENTS AND TRENDS

Today, WLP developments are motivated by the recognition that wafer level processing technology, i.e., parallel processing on the wafer, opens additional alternatives to traditional packaging and assembly. WLP includes not only processing on active devices, but also processing of silicon dice with integrated passives, other substrates such as glass leading to wafer level substrates, and artificially reconstituted polymer wafers with embedded die.

For package substrates, fine design rules and the capability of creating integrated passive devices are attractive features. Dielectrics and traces are built on silicon substrate by wafer process technology and the following assembly is performed on the wafer level substrate. Some wafer level substrates are not made of silicon but dielectric layers and traces built up on a wafer, which was removed during the manufacturing process.

Currently, different technologies at wafer level are in development to satisfy the need to increase performance and functionality while reducing size, power, and the cost of the system. This development leads to more complex packages for both single and multi-die Wafer Level Packages.

The wafer level CSP may incorporate copper post terminals with thicker resin coat providing a package that is more durable to the rough handling and more tolerant of CTE mismatch. This package is used for a variety of the applications from power amplifier to CPU with the ball pitches as fine as 0.20 mm.

The wafer level CSP specialized for image sensing is a glass-sealed optical wafer level CSP. Die are sandwiched or laminated on the circuit side by clear glass and terminals are routed to the reverse side of the die via TSVs or beam-lead metallurgy extending to the side of the die.

Low cure polymers, with cure temperatures below 200 Celsius are being developed to allow the implementation of embedded flash into WLPs, insuring the integrity of the memory states during standard WLP processing. These lower cure polymers are also needed for fan-out packaging, as the mold compound used to reconstitute the wafers are typically epoxy based systems with relatively low Tg's. They also serve the special needs of WLP with TSV and IPD processing.

## FUTURE TRENDS FOR WAFER LEVEL PACKAGING

Developments needed to meet the future requirements of wafer level packaging include:

- Continued reduction of processing temperatures, particularly for dielectric curing
- Wafer-level substrates with passives in silicon or passives in RDL
- Integrated passive structures into the RDL by thin film polymer deposition
- Embedded active and passive devices
- Wafer-level assembly—die to wafer—of Si (memory, MPU), MEMS, III/V (InP, GaAs, GaN etc.) and SiGe devices
- Integrated shielding (RF and power)
- Functional layers integration (actuators, sensors, antennas)
- Through-silicon-via (TSV) formation and metallization, wafer thinning and adjusted bonding technologies for stacked dies on wafer
- Optical chip to chip interconnects
- TSVs on WLP to allow double-sided connectivity, including Package on Package (POP) applications for WLPs
- Continued development of WLP for mechanical MEMS, in addition to the current optical MEMS applications

The development of wafer level packaging (WLP) is proceeding in several directions:

- Processes for larger die and higher functionality application based on RDLs (fan-in)
- Fan-out approaches (see various Embedded Wafer Level Package approaches)
- Higher complexity applications such as System in Package (SiP) with chip to wafer and 3D configurations and passive device integration. This includes face-down and face up approaches on active Si devices, carriers with passives, etc.
- New applications such as multiple IC stacks (memories, processor-ASIC-memories, MEMS); based on through silicon via (TSV) technology.
- Wafer to wafer stacks
- These WLP technologies are driven by market demand for higher integration density and system capability (See SiP section)

## DIFFICULT CHALLENGES FOR WLP

Wafer level packages are expected to have better reliability even for larger die with small ball pitch. The physical structure and the materials used are being refined to satisfy the requirements of specific applications. This is a particular challenge for MEMS devices.

Key challenges include:

- Board level reliability especially for large die
- Testing of wafer level stacked packages and new 3D architectures with multiple die
- Vias through chip (WLP) and package (for embedded wafer level architectures)
- Thin package profile using very thin silicon die for extremely thin applications
- Mechanical tolerances required for chip alignment to small pads
- Contacts on small pads
- High reliability (electromigration, drop test) I/O pad metallization (UBM; Solder)
- Topology of multilayer RDLs
- Topology for thick metals for high current
- Reduction of metal roughness for RF (skin effect)
- Cross talk on chip because of small vertical distance
- Yield and defect repair possibilities for embedded WLP products

## EXAMPLES FOR EMERGING WAFER LEVEL PACKAGE TECHNOLOGIES

### *WAFER LEVEL THROUGH SILICON VIA (TSV) FOR 3D INTEGRATION*

The realization of vertical interconnected devices/chips using through silicon vias is one of the key emerging trends in wafer level packaging. This technology offers significant advantages in terms of electrical performances, e.g., signal transmission, interconnect density and reduced power consumption as well as form factor, heterogeneous integration, and manufacturing cost reduction. Today, new approaches are in development to incorporate TSVs into the Front End (FE)-CMOS process or as a post-CMOS process with VIA first or VIA last process (see Figure AP12). The key technical parameters for stacked die architectures using TSV are presented in *Table AP14*.

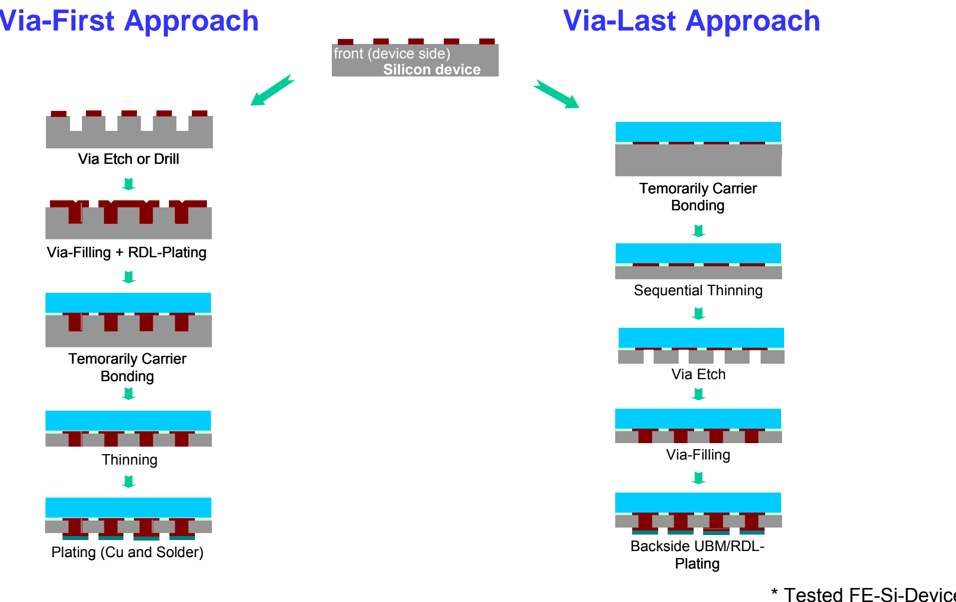



*Figure AP12 Basic Process Flow Via-first versus Via Last*

*Table AP14 Key Technical Parameters for Stacked Architectures Using TSV*

The implementation of TSVs into the front-end processes will be covered by the *Interconnect* chapter of this Roadmap; here some aspects from the assembly and packaging view point will be discussed. The basic processes for the TSV formation are via etching (DRIE, laser), insulation, and metallization, which are well known from front-end processing. Additional processes which are required for the stack formation are wafer thinning, deposition of redistribution layer (RDL) and under-bump formation, wafer level bonding processes (die-to-wafer or wafer-to-wafer, e.g., micro bump soldering or Solid Liquid Interdiffusion (SOLID), as well as final encapsulation. Today the TSV process is demonstrated at the R&D level and only a few companies are running on the product level. The transition from R&D demonstrations to high-volume processes requires viable business models, the development of an equipment infrastructure, and the existence of viable costs for competitive applications.

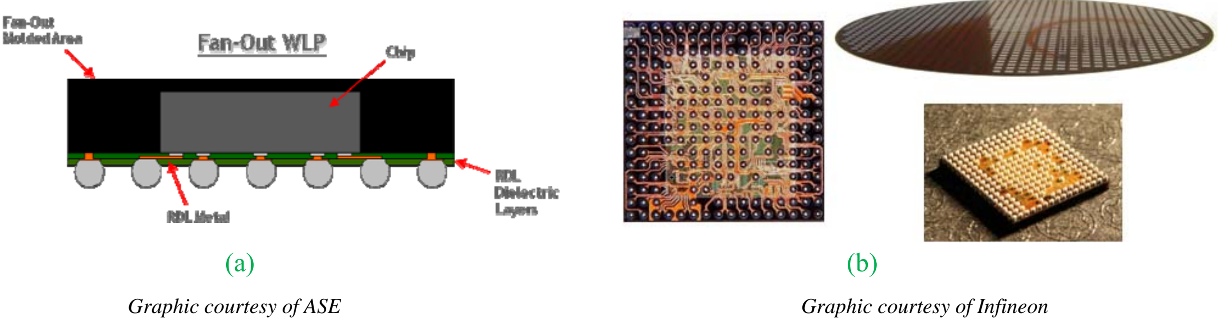
Key technical challenges for the TSV approach are:

- High density and high aspect ratio via etching
- Low temperature processes for passivation and metallization
- High speed via filling (e.g., electroplating (Cu), CVD (Cu, W)
- Thinned wafer/device handling
- High speed and precise wafer level alignment and assembly processes (die-to-wafer and wafer-to-wafer)
- Testing and methodology
- Competitive cost

The first applications of TSV are used for CMOS image sensors and are in production today. Stacked die approaches for memory devices are in development and will be in high volume production by 2011. Future applications for stacked die with TSV will include mixed architectures like analog, logic, processor, memory, and sensors.

### FAN OUT WLP USING RECONFIGURED WAFER LEVEL TECHNOLOGIES

New package developments that have begun production and in consumer products are fan out or embedded wafer level package technologies. These technologies allow higher integration density and fan-out solutions using WLP technologies. For this new approach the chips are reconstituted and embedded in an epoxy compound to rebuild an artificial wafer. A thin film redistribution layer is applied (see Figure AP13) instead of a laminate substrate, which is typical for classical BGAs. Laminate substrates are reaching their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layers opens new opportunities for SiP. The possibility to integrate passives, like inductors, capacitors or even active devices into the mold compound or various thin film layers opens additional design possibilities for new SiP. There are other approaches that incorporate a copper pillar over ball integrated arrays. Special difficult challenges for these types of embedded wafer level packages are their implementation in the packaging industry infrastructure from design to manufacturing, and surface mount assembly to the board and board level reliability. These packaging technologies will require closer cooperation between the die design and packaging engineering groups to insure the manufacturability of the entire die/package structure. This will minimize the packaging cost and maximize the manufacturing yields.




(a) *Graphic courtesy of ASE*

(b) *Graphic courtesy of Infineon*

*Figure AP13 Example of a Side-by-side Solution of a Fan-out WLP (a) and a Reconstituted Wafer (b)*

## SYSTEM LEVEL INTEGRATION IN PACKAGE

Predictions that Moore's Law has reached it limits have been heard for years and have proven to be premature. We are now nearing the basic physical limits to CMOS scaling and the continuation of the price elastic growth of the industry cannot continue based on Moore's law scaling alone. This will require "More than Moore" through the tighter integration of system level components at the package level. In the past scaling geometries enabled improved performance, less power, smaller size, and lower cost. Today scaling alone does not ensure improvement of all four items. The technical requirements for SiP are presented in *Table AP15*. The primary mechanism to deliver "More than Moore" will come from integration of multiple circuit types through SoC and SiP technology. The most important as the electronics industry becomes ever more dominated by the consumer will be System in Package. This will allow the efficient use of three dimensions through innovation in packaging and interconnect technology. The result will support continued increase in functional density and decrease in cost per function as the industry begins to reach the limit of conventional CMOS scaling. A comparison of the advantages and disadvantages of the SoC and SiP architectures are presented in *Table AP18*.

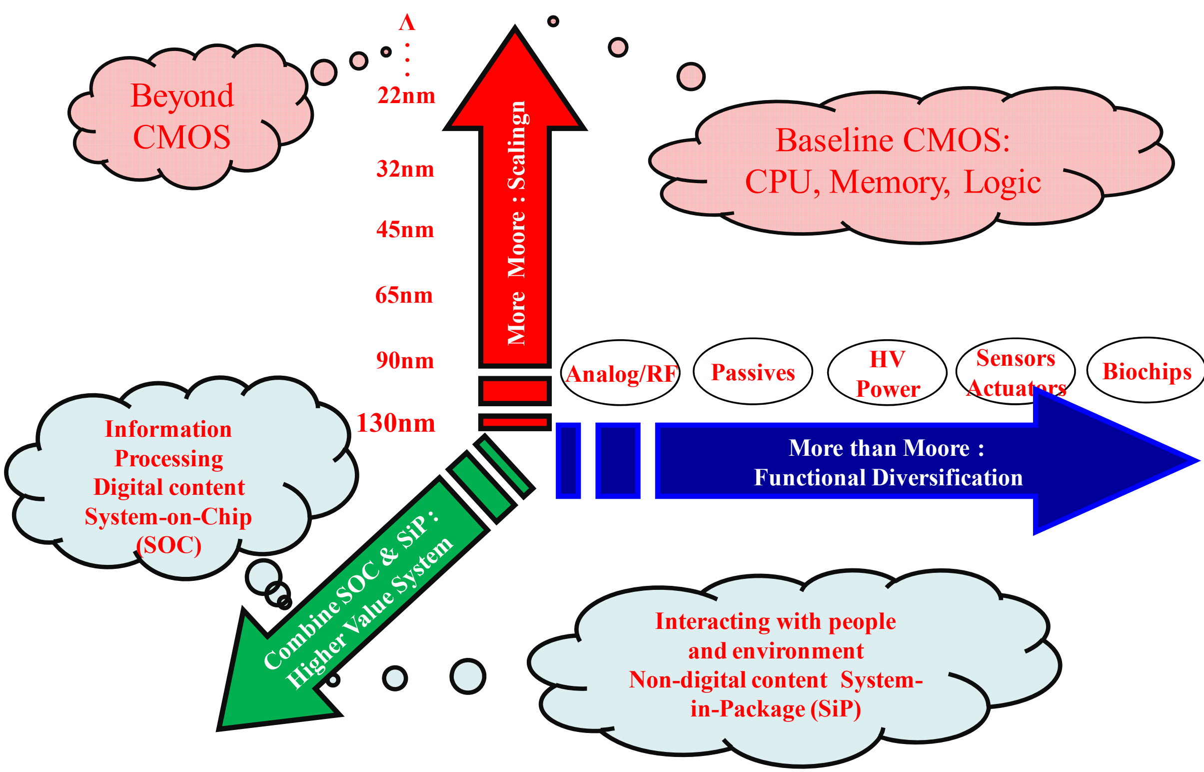



*Figure AP14 Beyond CMOS Scaling*

System in Package (SiP) technology is rapidly evolved from specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications. Numerous concepts for 3D SiP packaging are now emerging driven largely by the demands of portable consumer products.

*Table AP15 System in Package Requirements*

## DEFINITION OF SIP

> *System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit, which provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components, and other packages and devices.*

There are many types of SiP packages. They are divided into horizontal placement, stacked structures, and embedded structures. Examples of the major categories are shown in Figure AP15 below.

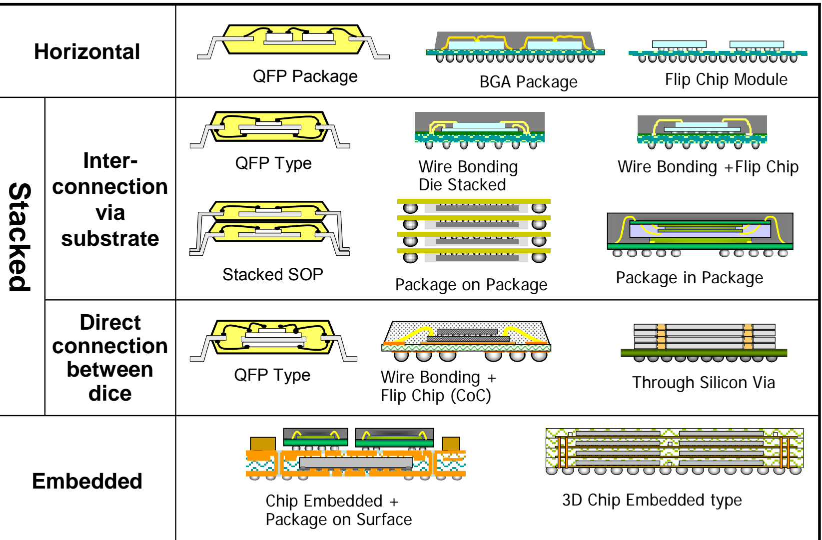



*Figure AP15 Categories of SiP*

## DIFFICULT CHALLENGES FOR SIP

System integration is aimed at higher performance, miniaturization, heterogeneous integration, and eventual cost reduction at the package level. For those purposes structures have diversified. Many critical technology challenges must be solved to achieve the ultimate performance goals and other benefits of SiP. The difficult challenges for SiP are presented in *Table AP16* below.

*Table AP16 Difficult Challenges for SiP*

| *Category* | *Difficult challenges for SiP* |
|---|---|
| Design | Heat-dissipation design<br>Heat-isolation design between stacked die with different maximum operation temperatures<br>Chip-package-system co-design<br>3D-Design and simulation tools<br>Complex standards for information types and management of information quality along with a structure for moving this information will be required.<br>Partitioning of system designs and manufacturing across numerous companies will make optimization for performance, reliability, and cost of complex systems very difficult. |
| Material | Stress resistant, superior electrical characteristics, high temperature resistant, low elasticity<br>Substrate; CTE, fine pattern, low elasticity, water permeability<br>Development and selection of materials which minimizes high-temperature warpage |
| Process | Wafer thinning, handling, and stress relief<br>Molding requirement: narrow gap fill, better flow characteristics over larger map format, less wire sweep, better package flatness<br>DAF attachment method for dicing-before-grinding process, and thinner DAF<br>Less fluctuation of heat-exposed duration of TSV dice while being stacked<br>Device yield immune from accumulating individual defect rates<br>Wafer to wafer bonding<br>Singulation of TSV wafers/die<br>Bumpless interconnect architecture |
| Test | KGD assurance<br>Test access for individual wafer/die<br>TSV nondestructive observation |

## 3D INTEGRATION

There are several driving forces for 3D integration. The potential benefits include higher performance, reduced power requirement, smaller size and eventually lower cost than conventional 2D packaging. Some of the basic driving forces for 3D integration are presented Figure AP16 below.

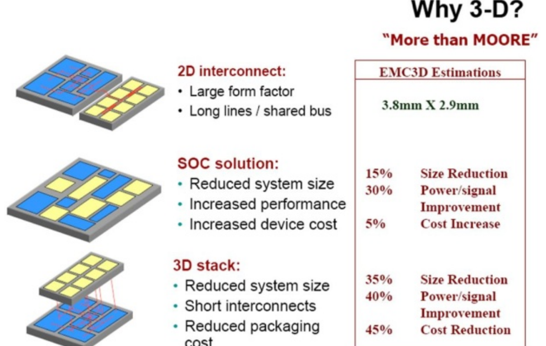



*Figure AP16 Driving Forces for 3D Integration*

There have been several 3D integration techniques and associated challenges presented in the Wafer Level Packaging and System-in-a-Package sections above. The issues specifically related to TSV are presented in *Tables AP13*, *AP14* and *AP18* with TSV related materials issues in *Table AP33*. There is a separate section below that addresses the thinning processes required for 3D integration. Many difficult challenges remain related to cost, reliability, alignment accuracy for D2D, D2W and W2W, and bonding techniques but rapid progress is being made by industry Consortia such as EMC-3D and others and volume production of TSV based product has already commenced. An example of process flow and equipment requirements is presented in Figure AP17 below.

Figure AP17 Example of Process Flow and Equipment for 3D Integrations

(Source: EMC-3D)

## INFRASTRUCTURE NEEDS FOR 3-D ICS

### *WAFER/DEVICE STACKING*

A variety of options have been proposed for the actual stacking of die, and packaging of the stacks. The relative merits of wafer-to-wafer and die-to-wafer stacking, with the process requirements of high assembly yield, and low complexity and cost will initially point to die-wafer stacking until progress on standards and alignment accuracy allow wafer-to-wafer to be adopted. The choice will be determined based on application and economic grounds.

The industry is currently focused on two bonding methods: metal-to-metal, which uses the preferred foundry-based TSV technology and has the advantage of simultaneously forming the mechanical and electrical bonds, and oxide bonding. Current copper-copper thermocompression bonding is very slow (~8 bonds/hr in a four-chamber tool) as opposed to oxide bonding, which requires via-last processing but is capable of performing 25 bonds/hr in a single-chamber tool. With a high alignment accuracy of better than 1 µm, which is expected to be in the sub-0.5 µm range within the next two years, interconnect pitches of 6–10 µm can enable high interconnect densities of ~1–3 million interconnects/cm2. For the next 2–3 years, alignment capability will not be the bottleneck.

Oxide diffusion bonding is 3× faster than copper bonding. However, the electrical interconnect is formed after the bonding, thus requiring an extra process step and potentially a level of complexity. Still, from a throughput point of view, it is more attractive than copper diffusion bond processing. The challenge is not feasibility or equipment technology at this point it is cost.

### *NEW STACKING SOLUTIONS*

What is needed is a stacking solution with the speed of oxide bonding, which uses foundry-based vias to form metal-to-metal bonds upon bonding.

The methods for bonding/die attach used for 3D integration include:

- Micro bump solder (Solid Liquid Interdiffusion-Solid)
- Copper to Copper Bonding
- Direct Oxide Bonding at low temperature (to minimize alignment shifts)

One such technology is Direct Bond Interconnect (DBI) covalent bonding technology, which enables room-temperature W2W or D2W bonding. With DBI, nickel can be used to interconnect to copper, tungsten or aluminum TSVs, while providing for adequate planarity of the oxide/metal interface to achieve a strong, reliable bond. The direct bond

interconnect process flow, one of the promising options for 3D integration, offers high throughput and low process temperature as illustrated in Figure AP18 below. *Table AP17* following summarizes selected properties of the bonding processes for 3D TSV interconnect methods.

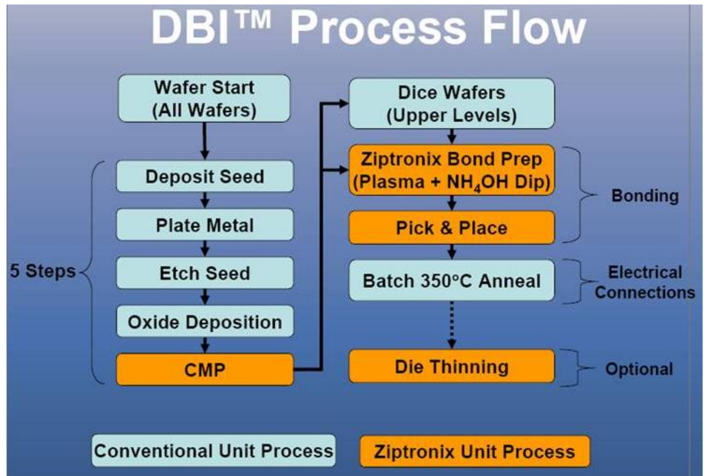



*Figure AP18 Direct Bond Interconnect Process Flow*[1]

[1] *Source:Ziptronix*

*Table AP17 TSV Interconnect Methods*

| Stack Method | W2W | W2W | W2W<br>D2W | W2W<br>D2W |
|---|---|---|---|---|
| Interconnect | Metal – Cu to Cu<br><br>Copper diffusion bonding<br><br>Thermocompression | Oxide Diffusion Bonding | Direct Bonding Interconnect<br><br>Covalent bonding | Copper Pillar / Solder Cap<br><br>Flux |
| Orientation | Face to Face<br>Back to Face | Face to Face?<br>Back to Face? | Face to Face<br>Back to Face | Face to Face<br>Back to Face |
| Via Type | Via First | Via Last | Via First<br>Via Last | Via First<br>Via Last |
| Attach Type | Mechanical / Electrical | Mechanical interconnect<br><br>Electrical interconnect with via last after oxide bonding | Mechanical and Electrical interconnect | Mechanical and Electrical |
| Attach Temperature | 400C anneal | <400C | Room Temp = 1J /m2 | <300C |
| Force | 20-100kN | | No force required | |
| Time | 7 minutes | | Spontaneous attach | |
| Throughput | ~8 bonds/hr | | ~25 bonds/hr in single chamber tool | |
| Notes | Inter-diffusion<br>No loss of conductivity | Provide planarity of the oxide/metal interface | Surface prep<br>Standard CMP and cleaning<br><br>A very high bond energy > 1 J/m2 can be obtained at room temperature<br><br>Temp can accelerate attach process or bond energy<br><br>Bond formed between oxide layers of die | |
| | | Crystalline silicon<br><br>Bond fused silica, glass, and polysilicon carbide | Nickel to copper, tungsten, or aluminum TSVs | |
| Hermetic | | | Yes | |

## DIE CONNECTIVITY

While multi-core, and eventually many-core, processors will provide a means for improving processor performance and power efficiency, the demand for off-chip bandwidth will greatly increase as the number of cores increases.[1, 2, 3, 4] In an effort to address this ever increasing demand for off-chip bandwidth, a number of innovations in off-chip interconnection and system integration are being pursued by industry and academia.

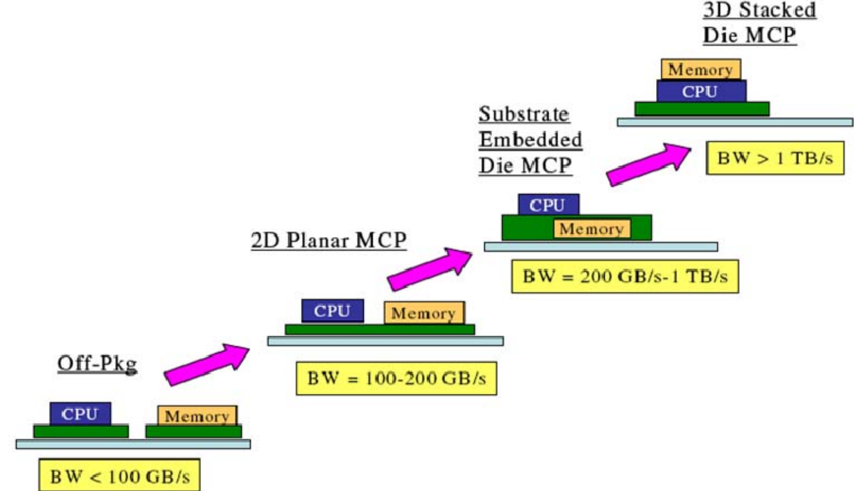



*Figure AP19 Roadmap for Package Transitions addressing the Memory Bandwidth Challenge.*
*Source: Intel Technology Journal Vol. 11, pp.197-205, 2007*

Latency, bandwidth (bandwidth density), power dissipation (or energy in pJ/bit), Bit Error Rate (BER) and cost of the overall off-chip network (which includes the drivers and receivers) are metrics that must be optimized. This will involve the migration to and/or integration with optical interconnects, 3D integration using through-silicon-vias (TSVs), capacitive and inductive signal I/Os, and other innovations in packaging and system integration. Some of these are illustrated in the figure below. While each of these methods of interconnection has advantages and disadvantages, they each are intended to greatly improve off-chip signal connectivity in a system.

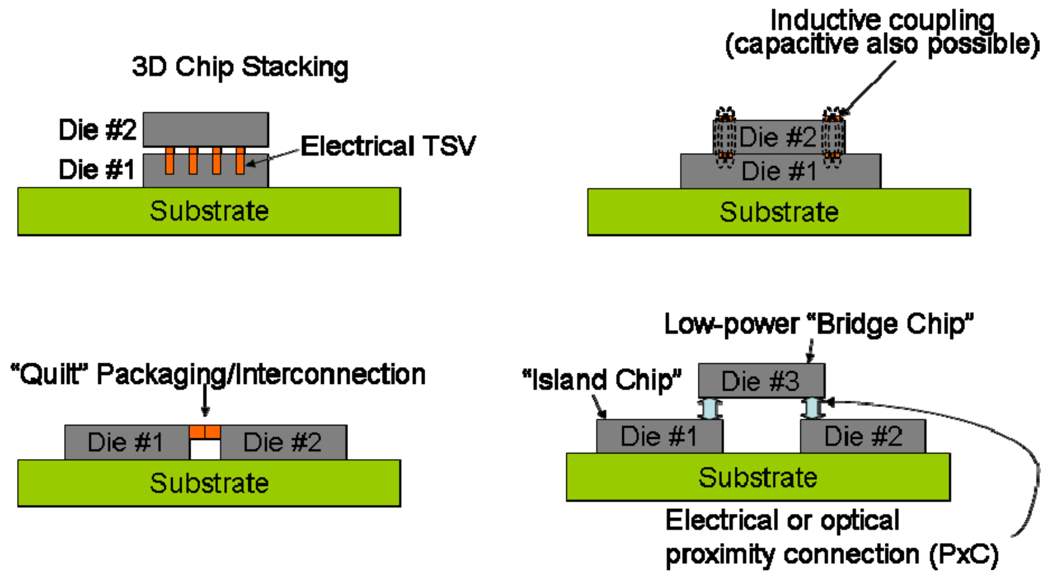



*Figure AP20 Methods of System Interconnect for 3D Integration*

Three-dimensional chip stacking can be accomplished in a number of way, but in general, require through silicon vias to enable vertical electrical interconnection. In some proposed 3D stacking methodologies, electrical TSVs are not used.

Rather, inductors are integrated in each of the stacked dice, possibly using semiconductor BEOL processing, and used for inductive wireless communication.[5, 6] Capacitive coupling has also been demonstrated for 3D stacked die,[7] it requires the die be face-to-face bonded and have at most a small gap between the chips (i.e., a short distance between the electrodes) in order to maximize transmitted voltage. Inductive coupling can overcome this limitation as it can provide communication through the silicon substrate (thus face-up-to-face-up bonding is possible, for example). However, as the communication distance between the inductors increases, the diameter of the coil has to increase for a given transmitted voltage, and the spacing between coils may increase to avoid coupled noise. Using inductive coupling, 19.2Gbps/channel at an energy efficiency of 1pJ/b has been demonstrated.[5] Power can be delivered using wire bonds as well as using inductive coupling.[8]

Quilt packaging is based on the fabrication of microscale nodules on the periphery of each chip to enable direct die-to-die edge interconnection.[9] This enables one to bypass the package based interconnects and provide, in principal, a seamless electrical die-to-die interconnection. The microscale nodules can be bonded using a number of processes including solder. Power delivery as well as alignment between modules and CTE mismatch issues are some of the potentially difficult challenges.

Yet another method to system interconnection is depicted in the figure above.[3, 10] Proximity Communication (PxC) technology enables die to be tiled and interconnected in a face-to-face topology. The interconnection between the tiled face-to-face formed dice can be achieved using capacitive or optical coupling. When capacitive coupling is used, each electrode of the capacitor is formed on either of the dice, while when optical coupling is used, two mirrors, one on each chips, are aligned to provide vertical interconnection between optical waveguides. Capacitive based PxC offers communication with chip-to-chip latency of 2.5 ns at 4Gbps/channel with a power efficiency of ~2.5 mW/Gbps and an areal bandwidth density of greater than 0.8 Tbps/mm2.[11] In principle, inductive coupling can also be used. As noted in above paragraph, the need for small gap between pads in capacitive coupling (or mirrors in optical PxC) is important.

### *SIP THERMAL MANAGEMENT*

3D technology can be used to enhance communication between ICs (larger bandwidth, lower latency, and lower energy per bit)[12, 13, 14, 15] but it also presents some challenges. Aside from issues relating to manufacturing, power delivery[16] and cooling[17, 18, 19, 20] of a stack of logic chips becomes more complex as compared to the single chip case. Challenges in power delivery include issues that relate to reducing power supply noise and losses in the power delivery network (as well as issues relating to electromigration). The continued reduction in supply voltage (although slower in the future) and timing margins causes the tolerated peak noise in high performance circuit to also decrease. This problem becomes worse as current consumption of microprocessors increase and circuits switch faster. Furthermore, power delivery becomes even more exacerbated when logic chips are stacked as the total current that needs to be delivered to the stack increases. Solutions to the power delivery problem will involve, among other things, co-design and optimization of both on-chip (for example, on-chip decoupling capacitors) and off-chip resources for power delivery including the number of power/ground pads and through-silicon vias. Trade-offs and analysis of the interaction of these is important to the understanding how to best minimize power supply noise in 3D stack.

Cooling represents another challenge for 3D logic ICs. Historically, in order to maintain constant junction temperature with increasing power dissipation, the size of the heat sink used to cool a microprocessor has been increasing (along with improved heat spreaders and thermal interface material (TIM)), and thus imposing limits on system size, chip packing efficiency, and interconnect length between chips. The cooling of hot-spots (power density up to 500 W/cm2) greatly exacerbates the complexity of cooling and it is becoming increasing challenging to meet thermal performance needs of chips. Challenges in cooling become magnified in 3D chips because it requires: 1) "paving" a path for heat flow from within the stack to the periphery of the stack (i.e., the thermal resistance to the ambient for chips within the stack increases compared to a single chip), and 2) methods of removing the increased power density to the ambient once the heat is "routed" to the periphery of the stack (usually the top of the stack). The low thermal conductivity of the on-chip interlayer interconnect dielectric increases the challenges to the former. Many researchers have proposed the use of "thermal TSVs" to enable "routing" of the heat to the top of the stack where it can be extracted to the ambient. However, such an approach may require a prohibitively large number of vias (especially with stack count increase). Another approach that is being explored by a number of researchers it the use of inter-layer microliquid cooling using microchannels or micro pin fin array as illustrated in the figure below.[3, 8, 9]

In order to achieve high heat transfer, low thermal resistance, and low pressure drop, a relatively tall microchannel heat sink is typically needed (~250 µm, for example). As a result, this necessitates a "thick" silicon wafer and is different from other 3D integration technologies, which seek to polish the silicon wafer to as small a thickness as possible before wafer handling and mechanical strength become limiters. [3, 8] As a result, this presents interesting set of constraints on the

fabrication and integration of E-TSVs, which had been demonstrated recently. Ultimately, the number of electrical TSVs that can be placed will impact the connectivity between tiers in a stack, including power delivery.

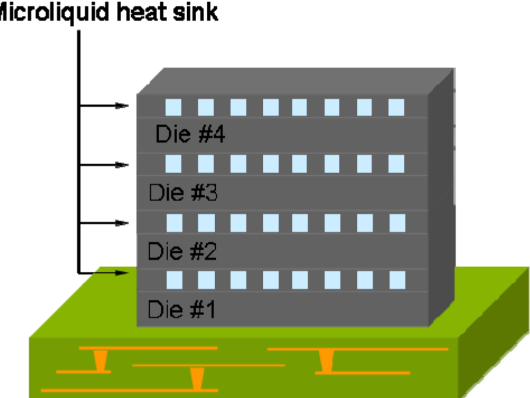



*Figure AP21 Interposer based Microliquid Heat Sink for Stacked Die*

### THERMAL CHALLENGE OF HOT SPOTS IN SIP

The heat generation from IC is highly non-uniform with areas of very high local heat fluxes at few locations on the die. Future trends show an increase in thermal design power and an increase in both average power density and local power density (also known as "hot spots"). Hot spot thermal management would limit the thermal solution of the component. Even when the total power of the component remains within design specification, the hot spot power density increase could limit the device performance and reliability.

For a SiP, thermal management must take account of the hot spot thermal dissipation within the die as well as within the package. Higher power dissipation with suboptimal placement of heat sources increases the risk of "hot spots" in 2D/3D integrated circuits. Also, difficulty in removing heat from the interspersed chips with a relatively poorly conducting thermal interfaces in 3D die stacking (e.g., thermal impedance of C4 attach/underfill for flip-chip package, thermal resistance of chip attach material for low density wire-bond package) signify the cooling challenge of hot spots in SiP.

### COOLING SOLUTION DESIGN REQUIREMENTS FOR SIP

For the side-by-side configuration in SiP, the challenge over the single chip packaging with individual heat sink is the need to deal with the thermal cross-talks between devices as well as increased total power. For example, devices will heat each other inside a package, so that even the low power device can possibly get hot, if its neighboring devices dissipate excessive heat. The cooling solution design for SiP addresses all the devices in the package.

Different devices inside the same package may have different Tj_max specifications. For example, the typical Tj_max for microprocessor is about 100C, while the typical Tj_max for memory device is about 85C. The cooling solution design for SiP needs to accommodate different Tj_max specifications of all the devices.

For stacked die configuration and for embedded device configurations, the decreased volume and available exposed surface provide significant challenges. For low profile packages with 3D die stacking, various package and system level thermal solutions should be considered. The hot devices need to be located with due consideration for various primary heat flow paths as shown below.

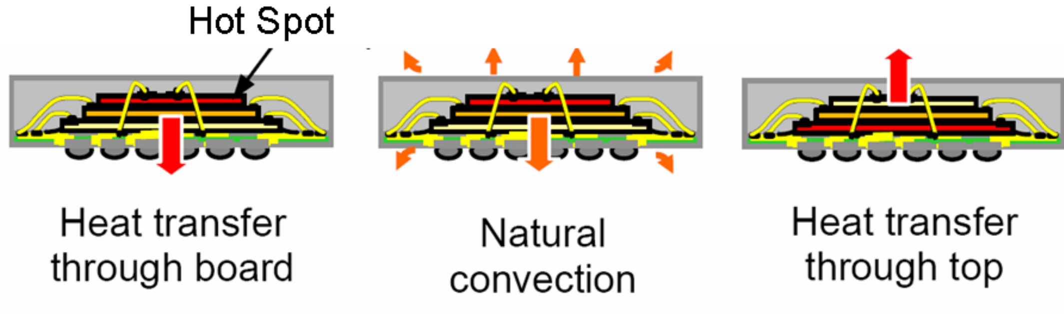



*Figure AP22 Location of High Power Die versus Primary Heat flow Path*

The hot spot generally occurs farthest from the primary surface used for heat dissipation. The higher power devices need to place closest to the primary heat dissipating surface. Technology improvement to the primary heat flow paths needs to continue. For top side heat flow path, use of higher conductive molding compound, embedded heat spreaders and improved package to casing thermal interface material are potential thermal management options. For bottom side, i.e. board side, heat flow path, thermal performance enhancement options include use of thermally conductive under-fill between package and board, dummy solder balls between package and board, embedded heat spreader within the package substrate, and high conductive die attach between die and die to substrate. System level enhancement options include use of thermally conductive enclosure, venting grill, and active air moving device close to the device.

### THERMAL CHALLENGES OF PROCESSOR AND MEMORY DIE SIP

In packaging a multichip module with one high power process and several low power memory chips, the preferred technique has been to locate the module lid precisely above the processor chip, permitting use of a thin layer of thermal interface material (TIM). The inevitable variations in chip heights and planarity of memory chips are accommodated by use of gap-pad (conductive elastomeric) TIM which results in significantly higher thermal resistance than that of the processor. Since the processor power density is typically several times that of the memory dice, resulting junction temperatures of all chips are similar.

For 3D stacked die configuration with TSV interconnects, the processor die is preferred to be placed at the bottom in 3D die stacking to make it closer to the substrate due to IO signal performance and power delivery efficiency, but cooling performance from the high power process will be the bottleneck. If the processor die is placed on the top, TSV requirements in both counts and size would cause significant mechanical concerns (e.g., crack, stress) for the memory dice at the bottom.

### POWER DELIVERY/POWER INTEGRITY

The power level of high end microprocessors places very stringent requirements on power integrity as the power density increases and the operating voltage decreases. The power integrity and product cost requirements cannot be met for high performance devices without chip/package/system co-design. (See section on The Need for Co-Design Tools below) The voltage level for 45nm and 28nm chips are in the sub one volt range resulting in reduced noise margin. Even with low resistive losses, the higher current transients due to multiple cores on the chip requires lower interconnect inductance and more decoupling capacitance on the substrate. The capacitor path requires multiple thin dielectric layers to meet the target impedance of the power delivery system. For multi-chip packages, placement of the various chips and decoupling capacitors is crucial and requires system level simulations. New materials will also be needed with higher dielectric constant and lower leakage currents to deliver the high capacitance density required to ensure power integrity at low cost.

Power delivery for multi-chip packages is also getting complicated due to multiple power supplies for different types of circuits such as core, memory, back-biasing, etc. Due to the test and system requirements, noise margins for the various power supplies are also different. Managing multiple power supplies requires more layers in the package which may restrict the use of some package technologies.

## SIP VERSUS SOC

The benefits of "More than Moore" can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future. The pros and cons of each architecture are outlined in Table AP18 below.

*Table AP18 Comparison of SoC and SiP Architecture*

| Market and Financial Issues | | |
|---|---|---|
| ***Item*** | **SiP** | **SoC** |
| Relative NRE cost | 1× | 4-10× |
| Time to Market | 3–6 months | 6–24 months |
| Relative Unit Cost | 1× | 0.2–0.8× |

| Technical Features PROs | |
|---|---|
| **SiP** | **SOC** |
| Different front end technologies; GaAs, Si, etc. | Better yields at maturity |
| Different device generations | Greater miniaturization |
| Re-use of common devices | Improved performance |
| Reduced size vs. conventional packaging | Lower cost in volume |
| Active & passive devices can be embedded | CAD systems automate interconnect design |
| Individual components can be upgraded | Higher interconnect density |
| Better yields for smaller chip sets | Higher reliability (not true for very large die) |
| Individual chips can be redesigned cheaper | Simple logistics |
| Noise & crosstalk can be isolated better | |
| Faster time to market | |

| Technical Features CONs | |
|---|---|
| **SiP** | **SOC** |
| More complex assembly | Difficult to change |
| More complex procurement & logistics | Single source |
| Power density for stacked die may be too high | Product capabilities limited by chip technology selected |
| Design Tools may not be adequate | Yields limited in very complex, large chips |
| | High NRE cost |

## TESTING OF SIP

The complexity of SiP based products continues to increase and, with that, test becomes a more difficult problem. The challenges are many and they include:

- Test access

- Contacting for testing thinned wafers and/or thinned die
- Thermal management during test
- Testing mechanical and thermal characteristics in addition to electrical test

### *TEST ACCESS*

If we assume that we begin the assembly and packaging process with known good die (KGD) the test problem is limited to confirming the assembly process and testing the performance of the on-package interconnect. If SiP is to meet its potential the off-chip drivers will be similar to the core transistors and only the off-package drivers will require more power. The SiP will not deliver all the test points to package pins for these more complex packages. There are several potential solutions including the incorporation of a "BIST" chip on-package that can have access to device pins that are not delivered to package pins. In some cases the more cost effective solution may be to test the SiP functionally without retesting the KGD post assembly if yields are high.

### *CONTACTS*

The continued reduction in geometries is approaching a terminal density that cannot be met with even the leading edge of conventional MEMS contactors. Several solutions are being evaluated including capacitive coupling which will suffice for digital signals but cannot provide power delivery or appropriate contact for analog signals. RF contactors have also been proposed and may offer a solution for some contact challenges. None of these proposed solutions has been proven to meet the requirements.

The test contactor required to deliver KGD for thinned wafers/die may be an even more difficult problem. The competition between ensuring power integrity when contacting these thinned die and damage to the die associated with the contactor force and potential pad damage.

These challenges and others may prevent the industry from delivering KGD for thinned wafers as we approach devices with a billion transistors and more. The concept of "probably good die" with redundancy in the SiP is being explored as a potential approach for ensuring the quality of complex SiP products.

### *THERMAL MANAGEMENT*

Today we encounter hot spots in integrated circuits which have circuit elements of different thermal density in the same IC. This presents a problem for package design but it has known solutions. The problem is becoming more difficult as the industry introduces new generations of microprocessors with many cores and incorporates core hopping to address local heating problems. This presents significant hot spot problems exacerbated by the fact that we now have no way to know where the hot spot will be located since it will move during operation. Finally we may have circuits included in a SiP with different maximum junction temperature. The challenges associated with these issues are discussed elsewhere in this chapter. The specific requirements to provide a cost effective mechanism to manage junction temperature while minimizing test time remains a major challenge for testing complex SiP devices.

### *MECHANICAL AND THERMAL TESTING*

The thermal cycles and specific use cases for many consumer products impose mechanical stresses that require test to ensure reliability of the products. The "drop test" approaches that have been used for cell phones and some other consumer products need to be replaced by new approaches that test a wider range of stresses including those associated with the thermal cycles experienced in the use cases. In addition we need tests that fit in a production flow without excessive test time or test cost. This remains a challenge not yet met.

### *COST OF TEST*

These test challenges must be met with low cost. Most SiP are today are used in consumer electronics. These markets are very price sensitive and any SiP for the consumer market with excessive test cost will not be successful. The major elements of conventional test cost are applications programming, test time, cost of ATE equipment, and cost of probe cards. Complex SiPs may require both conventional test and BIST testing to accomplish adequate testing. This is due to test access limitations in high component density, the very high speed of RF and digital communications circuits, and the requirement to test system level characteristics.

We have introduced some of the details for test challenges that are specifically relevant to assembly and packaging. The *Test* Chapter of the ITRS should be reviewed for a more complete description of test challenges.

## SIP FOR TERA-SCALE COMPUTING

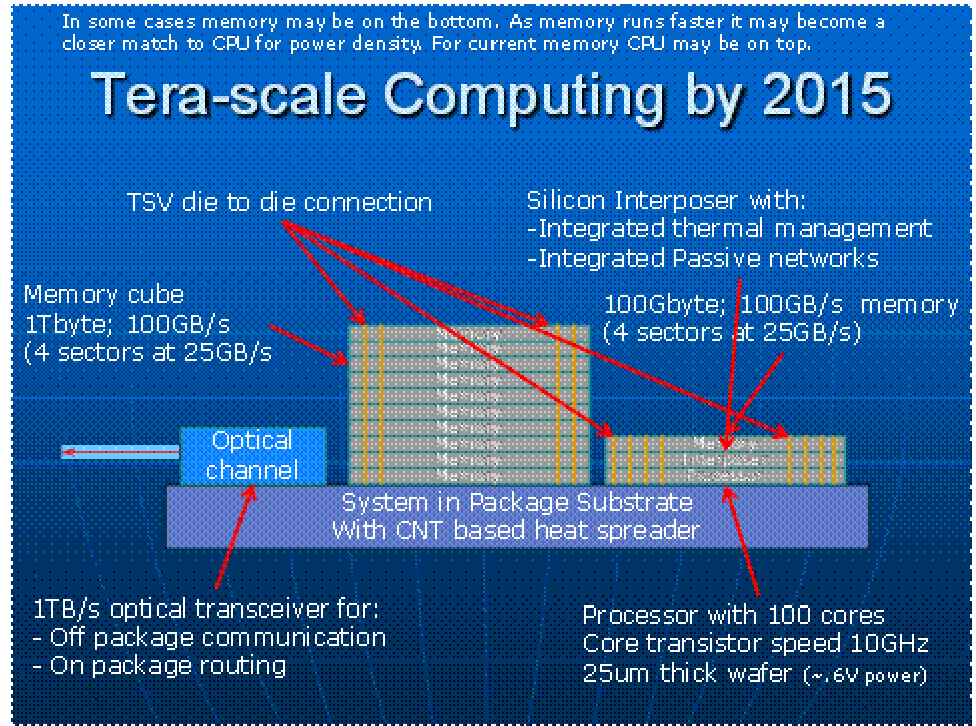



*Figure AP23 The Most Current Vision for Packaging in 2015 Utilizing These Concepts*

## THE NEED FOR CO-DESIGN TOOLS

Chip-package-system co-design methodology is a vital enabler for integrating SoCs efficiently into System-in-Package. Chip-package-board design collaboration is essential to reduce cycle time and cost and to optimize performance for stacked die, PoP, PiP, and 3D packaging in general. A more detailed overview is available in the paper titled *"The Next Step in Assembly and Packaging: Systems Level Integration."*

Failure to identify and meet essential system-level requirements and to apply lessons-learned, will result in lower-than-expected performance. Understanding design trade-offs and the performing critical system-level analysis is essential to produce designs that can meet the desired cost and performance targets. Incomplete feasibility studies and failure to capture some key interaction at the system level can result in extra iterations before the package design is finalized. It is important to identify essential system-level requirements and to apply lessons-learned for good optimal design. Without the benefit of co-design and simulation, there is risk that a device will be late to market with an expensive, overly conservative package.

Some key challenges in 3D packaging are design for manufacturability, design for low cost, reducing design time, design for reliability, complex wire bond and/or flip chip rules checking, chip design flexibility trade-offs. Also critical are interface/alignment with tools and flows such as those provided by EDA design software tools, IDM specific design flow and tools, and alignment with substrate suppliers and assembly sites. Implementing co-design methodology requires iterative design reviews; collaboration between chip, package and system design; application development; electrical, thermal, and mechanical modeling; simulation, and high-density substrate design teams. A suggested design flow is shown in Figure AP24 Below.

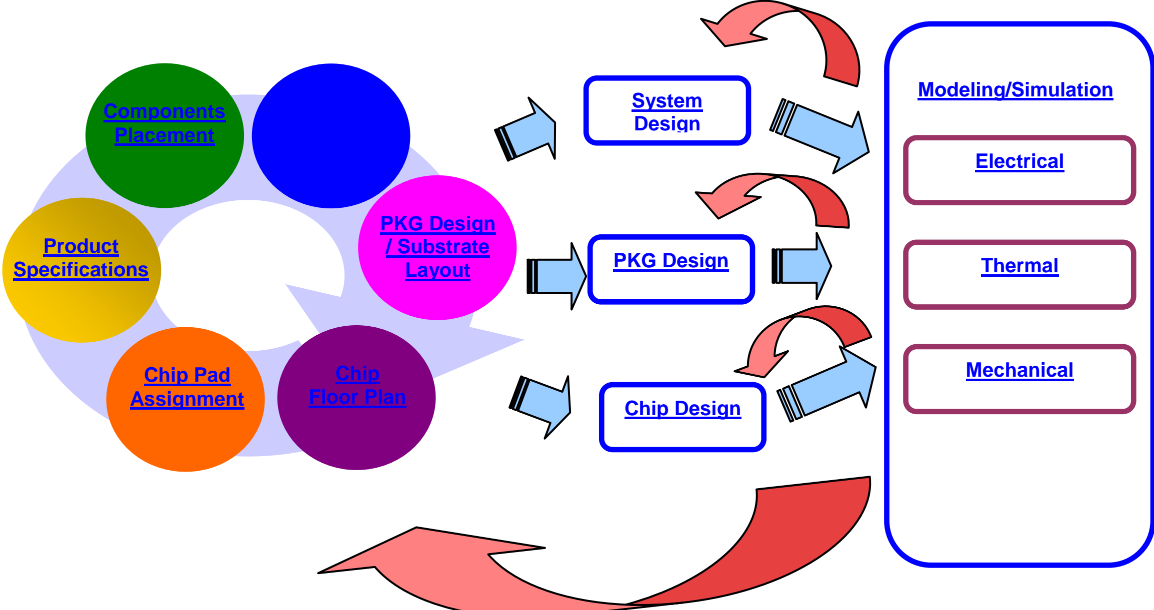



*Figure AP24 Chip-Package-System Co-design flow*

### COLLABORATION, COST, AND TIME TO MARKET

Expert users of each tool environment chip/package/system must collaborate to optimize the design. Thus, for the future, appropriate user interfaces are required. Co-design can improve performance while reducing costs and cycle time dramatically—often by 2×. Without the benefit of extraordinary collaboration within the design team, the package is almost impossible to optimize at the system level. The cost trade-offs are not clear, system level performance impacts are uncertain, and changes are cumbersome to implement. To avoid this, designers often use overly conservative design margins and assumptions that lead to higher package costs. Without co-design analysis tools that function across design environments, "what-if" analyses are difficult and time-consuming, leading to longer design cycle times.

### IMPORTANCE OF RELIABILITY FOR SIP

Effective co-design should comprehend the interaction between physical, thermal, mechanical, electrical design, and reliability. Many of the trade-offs between design areas and reliability that are evident in conventional packaging become more complex for SiP configurations. Thus, it is not good practice, especially in SiPs, to run the electrical, mechanical, thermal and reliability design portions separately. Because of the complexity of sub-component interactions, there is not a universal or specific list of parameters to design for reliability. In general, one needs to examine the sub-component interactions, design goals, trade-offs, design rules, specifications, and existing design for reliability practices in order to select the appropriate design for reliability guidelines.

### THE NEED FOR A SYSTEMATIC APPROACH

Package design requirements and changes originate from many different functional areas and usually end up being applied in stages. A potential solution would be for the chip-package co-design to borrow methods and tools from modern systems design. This approach can head off constant iteration and other challenges. One way to reduce iterations is to use "look-ahead" test and modeling vehicles to support system-level reliability and manufacturability testing, as well as system-level electrical and thermal modeling. Look-ahead vehicles come in two forms: an actual mechanical vehicle for reliability and manufacturability testing, and a paper design vehicle for feasibility, thermal and electrical modeling analysis. These vehicles require a certain discipline and commitment. This approach could help to answer many general design questions early in the process, and at a fraction of the cost of using production test vehicles.

### THE NEED FOR CO-DESIGN TOOL DEVELOPMENT

SoC and SiP package design requires 3D capable thermal, electrical, and mechanical modeling tools that allow integration and analysis of chip, package and system level requirements, and interactions. We also need electronic design automation (EDA) tools for powerful chip-package-system design and routing capability, built-in checks, standards and reporting features like design rule checks (DRC), standard net list syntax, and connectivity reports.

Custom automation tools can provide fast and efficient communication and verification of design data between different design environments. Spreadsheets are a common platform for these automation tools since they are available in almost all design environments and readily scale to handle large volumes of data. These tools have three primary uses: 1) convert data to pictures, 2) convert data to standard formats, and 3) compare the standard format datasets. This type of automation is essential on typical SoC designs to reduce the time spent manipulating relatively large datasets, and to reduce possible manual errors in handling large amounts of raw data.

The development of chip-package-system co-design methods and tools is an ongoing process. A comprehensive, user-friendly, and tightly integrated tool(s) that can seamlessly span all the different design environments is not yet available. Nevertheless, existing chip-package co-design tools, with the right methodology and custom-developed internal tools can provide useful benefits including reduced package costs, and design and verification cycle time.

### Generic Chip-Package-System Co-Design Tool Development Requirements

- Improve design cycle time, accuracy and design-for-manufacturability
- Align with critical tools, import/export data formats, flows and rules such as: IDM's internal tools die design tools, suppliers, assembly sites, electrical constraints and modeling tools
- Reduce iterations, less manual/more automated checking, capture complex design rules and enable more chip-package-system trade-off capabilities
- Forward-looking: better methods, more complexity, collaboration, and technology combinations
- Easier verification: Substrate, substrate plus die, manufacturability, electrical, functional, thermal, and mechanical verification. Import/export to IDMs internal tools
- Easier and more rapid feasibility analysis
- Collaboration with die and system design teams. Unified data formats, chip plus package plus system verification tools, etc.
- Comprehend the interaction and I/O planning of multiple functions within a single package (also passives)
- Great complexity—amount of design data, multiple layers, elaborate patterns, multiple net lists
- Complicated electrical constraints (long traces/wires, crossing traces/wires…). Enhanced constrain management
- Allow minor tweaks in IC or package design without leading to significant cycle time hit
- Need faster design iterations in early phase to avoid more costly design iterations in the later phase
- Capture complex mechanical, wire bond and flip chip bond assembly-rule constraints driven by smaller and thinner packages
- Better design for manufacturability and cost analysis. More and easier to use manufacturability constraints
- Real-time chip-package-system design trade-offs
- Interface and alignment with internal tools and flows
- Shortening design cycle of complex designs
- Cost-weighting of constraints
- More flexibility to handle frequent design changes
- Flexibility of design flow, user-defined design starting point from chip or from system
- Tighter integration with chip, system and manufacturability design teams
- System-level electrical modeling, including high-speed applications
- Complexity drives verification tools that work across different design environments
- Tight collaboration with suppliers, support, development, production, and customers to enable better methods and tools for complex package co-design
- More powerful user-friendly scripting capabilities
- Common, technology independent database to enable reuse

### Co-simulation of RF, Analog/mixed signal, DSP, EM, and Digital

SiPs that combine RF, analog/mixed signal, DSP, EM, and digital bring not only design and manufacturing challenges but also simulation challenges. Usually different functions of an IC require a different simulation technology. For instance, frequency domain simulations such as Harmonic Balance are adequate simulation technologies for RF circuit designs; whereas time domain simulations are typically used to predict nonlinearity and VHDL or C based system simulation for digital applications. It is important to understand the system's behavior with packages and interconnect parasitics.

Simulation and Modeling of Embedded Passives and Integrated Passive Devices in SiP applications need to be considered. Embedded passives are used to replace traditional surface mount parts.

# PACKAGING FOR SPECIALIZED FUNCTIONS

## *OPTOELECTRONIC PACKAGING*

Optoelectronics packaging covers a wide and expanding range of technical requirements as the use of optical components in electronic systems continues to rise. In this chapter we address several of the applications including long range data transmission, short range optical communication that is moving closer to the silicon with each technology node and lighting applications. Examples of optoelectronic packages and their applications are presented in Table AP19.

*Table AP19 Some Common Optoelectronic Packages and Their Applications*

### *DATA TRANSMISSION*

The packaging methods for telecommunications applications, meaning distances over 10 Km at data rates usually over 1 Gb/s, are well established and generally follow the demanding Telcordia or less demanding CATV standards. The major packaging issues relate to reducing cost, implementing data rates of 40Gb/s and higher and provisioning and building out dense wavelength division multiplexing technology.

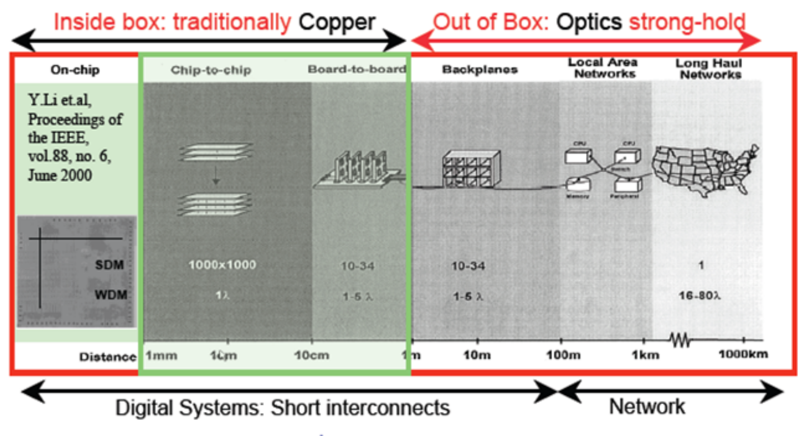



*Figure AP25 Optical Interconnect Approaches the Chip*

The figure above illustrates the role of optical technology in data communications and highlights the current position of the transition between optical data transmission and conventional electronic, or copper, data transmission.

Over the last 30 years, optical methods have replaced copper for virtually all long haul (>10Km) applications and are continually encroaching on copper methods for shorter distances. Table AP20, "Telecommunications: Long Haul," addresses the technologies used for long haul communications. The current transition is in the 1 to 100 meter distance at data rates of 1 Gb/s to10Gb/s generally implemented with Active Optical Cables (AOC) discussed below. The technologies used for shorter distance datacom are presented in *Table AP21*: Datacom Receivers.

*Table AP20 Telecommunications: Long Haul (100's of Km) to Metro (>1Km)*

*Table AP21 Datacom Receivers: Short range LAN, FTTX, Active Optical Cable (AOC), Backplane, On-circuit Board and On-to and Off-of chip Data Transfer Applications*

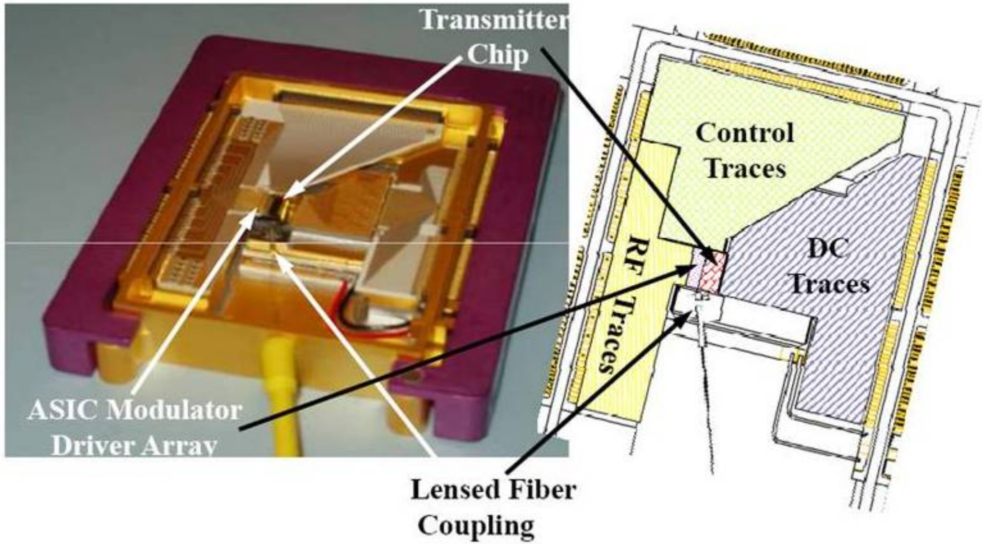



*Figure AP26 100Gb/s DWDM Telecommunications Transmitter Module.*[2]

The packaging issues for the standardized, well established local area network (LAN) applications generally over distances of 100 to 10 Km, are also largely cost reduction driven. These applications are often implemented with multimode methods and increasingly plastic optical fiber. These methods eliminate sub micron alignment and minimize assembly and field installation costs.

*Figure AP27 An Active Optical Cable*[3]

AOCs for distances of 1 to 300 meters are just emerging so methods to package these are not well established. The market has seen multiple entrants since 2007 with multiple packaging methods used. The driver is primarily cost reduction with power reduction growing in importance. Most of the AOCs utilize multimode so the packaging issues are not generally high tolerance but yield to engineering to reduce parts and simplify assembly increasingly with automation as volume grows. AOCs have a standard electrical connector on the two ends with a transceiver built into each end. The connection to the optical fiber is permanent so the optical technology is “transparent” to the end user.

Plastic optical fiber for less than 100 meter applications is growing in importance for transportation, meaning mostly automotive but also aircraft and military. As with AOCs, this packaging technology is undergoing rapid cost reduction with the goal of achieving <$1/Gb/s.

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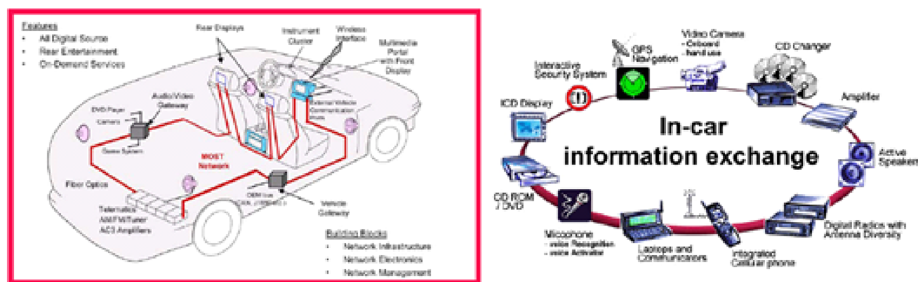
[2] *Source: Infinera*
[3] *Source: Luxtera*

MOST® - Automotive Networking

Fiber Optic Infotainment LAN for 50MBd/25Mb MOST®




⇨ MOST initiative lead by Daimler-Chrysler, BMW, Audi, Harmon Becker and Oasis/SS (SMSC)

⇨ MOST Consortium started in 1997

⇨ Peer-to-peer synchronous multimedia network using Plastic Optical Fiber

⇨ In production vehicles since end 2001

*Figure AP28 The Use of Plastic Optical Fiber in Automotive Applications*[4]

The methods of packaging optical technology for distances < 1 meter are the subject of continuing R&D by many organizations. The drivers for these applications are increasing data rates and power reduction, ideally without cost increases. The major issues include:

1. The limit of electronic methods (the general opinion is that electrical methods are viable up to 18Gb/s over distances of up to 1 meter if signal conditioning and detection, SERDES, are used)
2. Methods to implement optics in backplanes
3. Methods to implement on-to and off-of chip data transfer
4. The role of through silicon vias and the option of stacking chips made with different technologies.

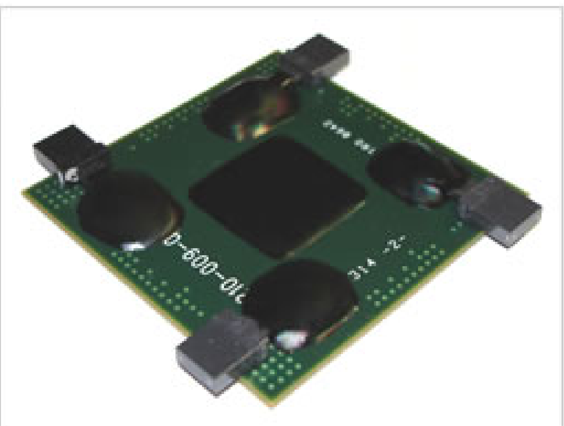
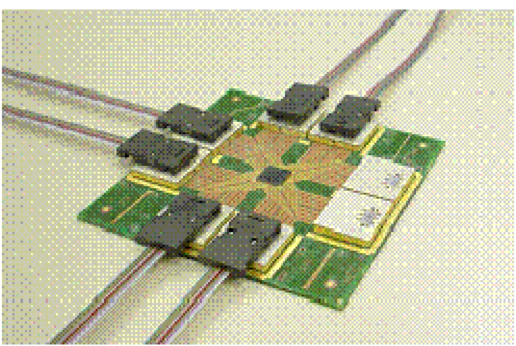


*Figure AP29 Implementing Gb/s Data Rates On-To and Off-Of Chip using Optically Connectorized Packaging*[5]

[4] *Avago Technologies*

[5] *Reflex Photonics*



OE module (fibre pigtailed/optical connector)

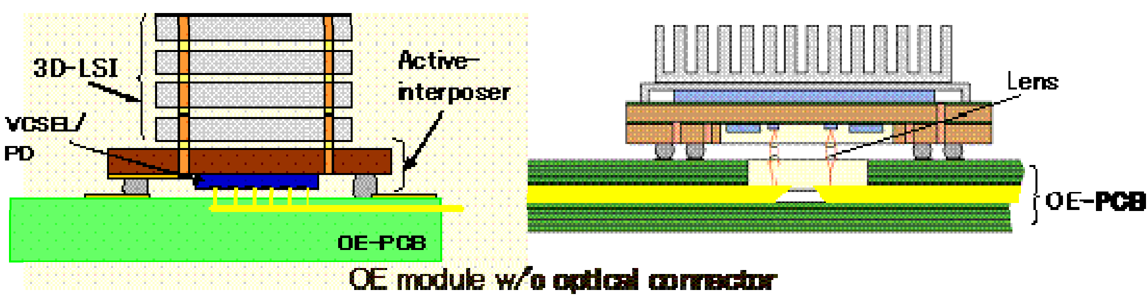



*Figure AP30 Methods to Implement an Optical Wiring Board*[6]

The final potential data transmission packaging issues relate to optics-on-chip where the motivation is achieving the data rates required, especially to interface multicore processors to memory, and in principal, to reduce power requirements. A consensus has not emerged regarding the role of optics, if any. Not only are packaging issues being re-evaluated, but system architecture and physical structures as well.

One view is that optical methods will not be needed or cost effect especially if through silicon vias (TSV) come into wide used. Another view is that TSVs will enable optical methods by enabling an optics layer in a multi-die stack to provide on-to and off-of chip optical methods and potentially to replace copper for some global interconnect.

[6] *Based on the work of Mr. Takahara of NTT Advanced Technology,Presented at IEC/TC86/TC91/JWG9 at Locarno, Switzerland on 2009-04-22*

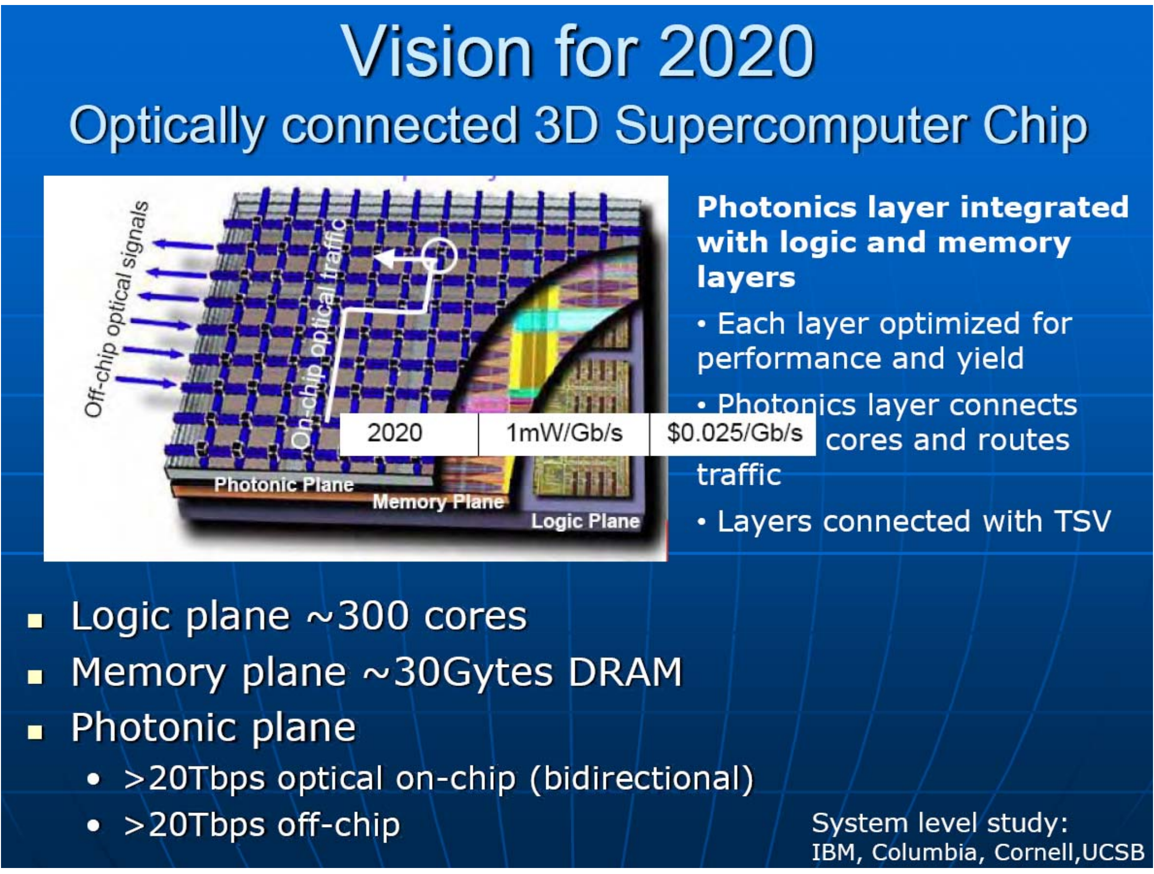



*Figure AP31 A Vision Meeting 2020 Projected Needs with On-Chip Optical Data using TSVs and Specialized Chip Layers*

The data transmission applications above generally require 3 classes of optical transceivers;

- Telecommunications transceivers for distance greater than 1 km that are all single mode, generally at data rates over 1Gb/s or higher. The primary need is for low attenuation over 100's of kilometers that can only be achieved with single mode technology even though that technology is expensive to implement due to the tight tolerances that must be maintained over extended periods in a variety of unpredictable environments.
- Transceivers for LANs and data transfer over distances of 1 meter to 1 km. These are a mix of single mode and multi mode methods with multi mode dominating, especially at the shorter distances. This group might be split further into POF and glass fiber based methods. Much innovation is currently taking place for products in this regime. Even though multimode attenuation rates are greater than those of single mode technology, multimode is effective for this application because the component costs, assembly tolerances and field installation and maintenance costs are lower than those of single mode technology.
- Methods to implement transceivers for distances less than 1 meter are not well established and are the subject of continuing discussion.

There are many difficult challenges remaining for optical packaging and they will become increasingly critical as the optical communication gets ever closer to the chip. A list of these challenges is presented in *Table AP22*. The technology requirements are presented in *Table AP23*, the potential solutions in *Table AP24* and the Cross TWG issues in *Table AP25* below.

*Table AP22 Difficult Challenges for Optical Packaging*

| *Distance* | *Difficult Challenges* |
|---|---|
| Telecommunications, generally >1km | Cost reduction, achieving >40Gb/s data rates in a small form factor, provisioning DWDM |
| AOC 1 to 300 meters | Cost reduction, reducing part count and assembly cost, reducing power required, developing more automated methods to reduce cost further as volume grows, developing standards |
| POF, <100 meters | Reducing optical loss in the fiber, developing a multimode optical amplifier, minimizing the number of standards, |
| Backplane, on-board, on-to and off-of chip, 1 cm to 1 m | Developing cost effective modulators and/or modulated light sources, defining an overall physical structure that cost effectively integrates optical and electrical methods |
| On-chip | Reducing power to < 0.1pj/bit, developing single mode technology that will tolerate temperature variation, developing multiwavelength light sources, |

*Table AP23 Technology Requirements for Optical Packaging*

| *Distance* | *Technology Requirements* |
|---|---|
| Telecommunications, generally >1km | 40 year life in a variety of environments, low attenuation, data rates per wavelength of 40Gb/s and potentially higher, multiplexing of 120+ wavelengths, multiple bits per cycle of bandwidth |
| LANs, generally 10m to 1 km | Low cost, minimal installation and maintenance costs, data rates of 1Gb/s and growing |
| AOC, 1 to 300 meters | Low cost vs. electrical alternatives, compatibility with electrical cabling they replace, data rates of 40Gb/s per link and higher |
| POF, <100 meters | Tolerance of automotive environments, rugged, easily made field termination methods, reduced attenuation for longer distances |
| Backplane, on-board, on-to and off-of chip, 1 cm to 1 m | Bandwidth greater than 10Gb/s per wavelength, efficient, low cost modulated source, |
| On-chip | Power consumption of less than 0.1 pJ/bit, transmission of Tb/s of data with multiple single mode wavelengths, waveguide technology compatible with CMOS chip technology |

*Table AP24 Potential Solutions for Optical Packaging*

| *Distance* | *Potential Solutions* |
|---|---|
| Telecommunications, generally >1km | Non-hermetic packaging, growing volume and standardization enabling increased automation |
| LANs, generally 10m to 1 km | Non-hermetic packaging, growing volume and standardization enabling increased automation |
| AOC, 1 to 300 meters | growing volume and standardization enabling increased automation |
| POF, <100 meters | Improved materials, non-hermetic packaging, growing volume and standardization enabling increased automation |
| Backplane, on-board, on-to and off-of chip, 1 cm to 1 m | Waveguides built into backplanes and circuit boards, acceptance and standardization of improved materials, low cost modulated sources, addition of the functions to drive sources, like VCSELs, and detectors, like API, into silicon die |
| On-chip | A small (< $10{,}000^2$ microns) modulator compatible with CMOS for use with off die light sources, stacking of a photonic technology enabling chip with conventional CMOS chips utilizing TSV |

*Table AP25 Cross TWG Issues for Optoelectronics*

| *Distance* | *Cross TWG Issues* |
|---|---|
| Telecommunications, generally >1km | None known |
| LANs, generally 10m to 1 km | Non-hermetic packaging materials are of interest for all semiconductor packaging |
| AOC, 1 to 300 meters | None known |
| POF, <100 meters | None known |
| Backplane, on-board, on-to and off-of chip, 1 cm to 1 m | Lifetime of VCSELs, cell designs and tools to add VCSEL drivers and photodetector support electronics to chips |
| On-chip | Comparison of optical methods with electrical methods by chip designers, evaluation of the impact and role of TSV on the potential role of optical methods |

### HIGH BRIGHTNESS LEDS FOR SOLID STATE LIGHTING

According to the US Department of Energy (DoE), lighting is one of the major energy uses in human society. The satellite picture in Figure AP32 shows where on earth there is lighting at night. It covers substantial areas of land. Nevertheless, this picture only exhibits the outdoor lighting. There are many more indoor and underground lighting applications not shown in this picture. Figure AP33 compares various power uses in commercial buildings. Lighting

obviously consumes the most indoor electricity. The amount of energy consumption by lighting is indeed far beyond what most people would expect. Therefore, any improvement in lighting efficiency will save a great deal of energy.

*Figure AP32 A Satellite Picture Showing Where on Earth Lighting Uses the Most Electricity*

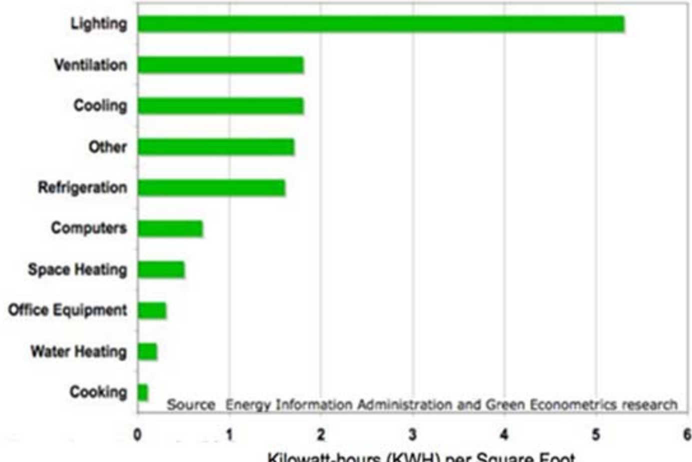



*Figure AP33 Lighting Consumes the Largest Amount of Electric Energy in Commercial Buildings—Three Times the Energy Consumption of Air Conditioning*

The conventional light sources include incandescent, halogen, and fluorescent lamps. The first two have rather low luminous efficiency (in term of lumens per watt). The fluorescent lamps have relatively high luminous efficiency (up to 90 lumens/watt, see Fig. 34). But they contain mercury vapor, which is not environmentally friendly. The emerging light source is light-emitting diode (LED). LED is a type of semiconductor device. Therefore, the light source made of LEDs is called solid state lighting (SSL). Although the lighting principle was discovered in early $20^{th}$ century, LEDs were not introduced to the industry as practical devices until early 1960s. In the first three decades, due to the low luminous efficiency and limited colors, LEDs were mainly used for signals and decorations. In 1990s, the efficiency of LEDs had substantial improvement. In addition, blue LEDs were invented to complete the spectrum for white light generation. As a result, today LEDs are suitable for general lighting. Currently commercial LEDs with 100 lumens/watt are available in the market. Even higher luminous efficiency (>150 lumens/watt) can be reached in the laboratory. The projected luminous limit of LEDs is around 350 lumens/watt. In addition to the improving efficiency for energy saving, LEDs also have very long operational life and contain no hazardous substance, which can reduce the cost of repair/replacement services and waste treatment, respectively. With all these advantages, it is obvious that SSL has very high potential to grow.

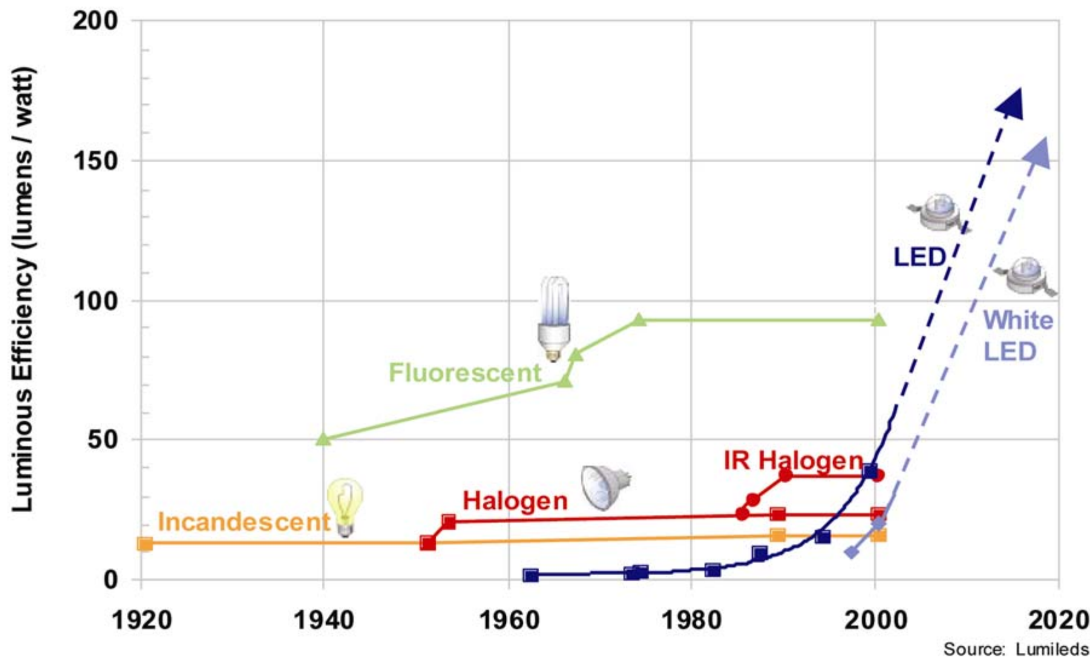



*Figure AP34 Comparison of Luminous Efficiency among Various Light Sources*

Commercial LEDs come in many different forms as shown in Fig. 35. One way to categorize LEDs is to go by their power rating. Typical classifications include low-power LEDs (<0.1 watt), medium-power LEDs (0.1-0.5 watt), and high-power (or high-brightness) LEDs (>0.5 watt). Typically people use 1 watt high-brightness LEDs for general lighting applications. Another way to classify LEDs is by their package structure. The 5 mm (or $\phi 5$) type shown in Fig. 36 is conventional package using lead-frame for insertion mounting. This type typically has very high thermal resistance and, therefore, is only suitable for low-power LEDs. The surface mount (SMT) type of package shown in Fig. 37 is mainly for high-brightness LEDs. The packaging of high-brightness LEDs is similar to that of power IC devices. Nevertheless, there are two major differences. LEDs are light emitting devices. Therefore, issues related to optical output must be considered. Furthermore, the typical die size of LEDs is 1x1 mm or less, resulting in relatively high heat density. The optical performance and the long term reliability of LEDs are very sensitive to the junction temperature. Therefore, the thermal management of LEDs is a critical factor in package design.

*Figure AP35 Various Forms of LEDs*

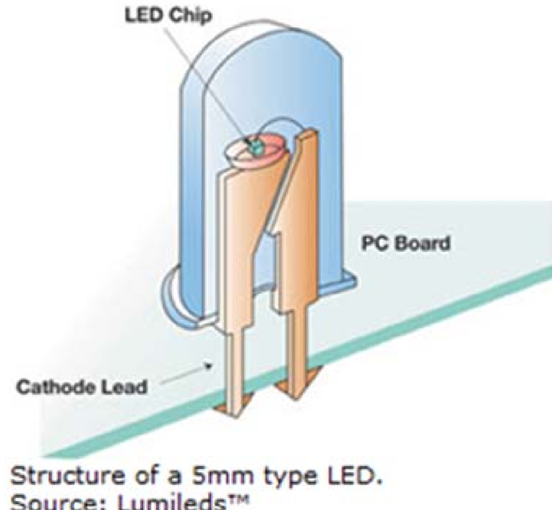



*Figure AP36 5 mm Type of Package for Low-Power LEDs*

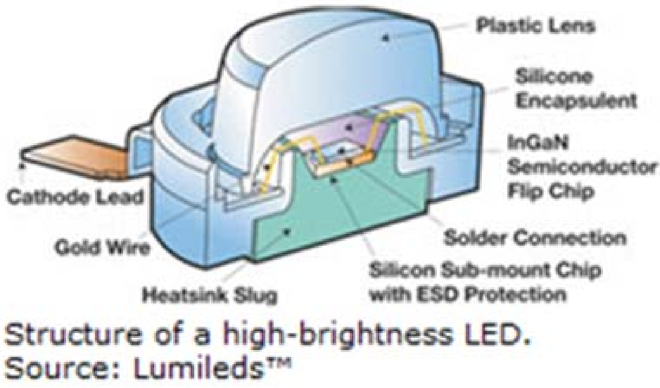



*Figure AP37 SMT Type of Package for High-Brightness LEDs*

Color tuning is another major issue in optical performance of LEDs. For SSL applications, white light illumination is usually required. In principle, there are three ways to generate white light from LEDs: a) mix the output of red, green, and blue (RGB) LEDs; b) use UV-emitting LED to excite RGB mixed phosphors; c) use blue LED to excite yellow phosphor (see Fig. 38). The last one is the most popular method for general lighting applications. It should be noted that the efficiency of phosphor materials and the packaging density/thickness uniformity of phosphor coating are critical factors for the optical output of LEDs. Another important element for the optical output is encapsulation materials of LEDs. Currently most high end high-brightness LEDs use optical grade silicone for encapsulation.

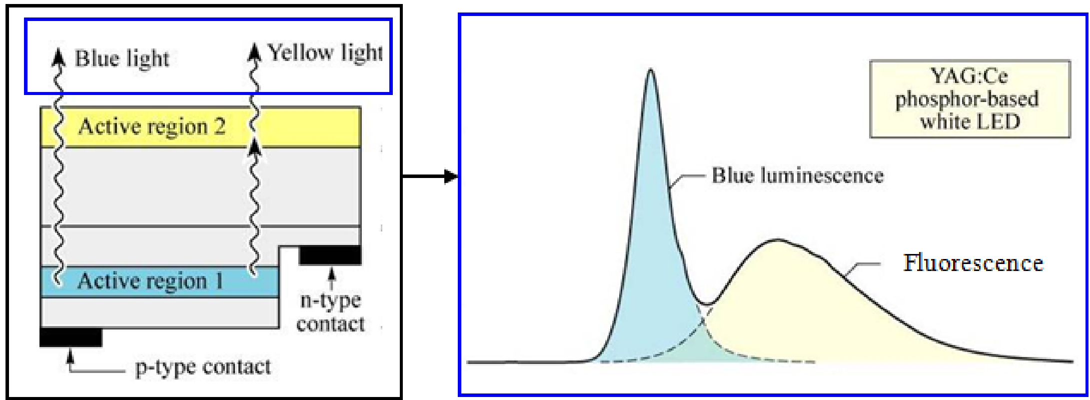



*Figure AP38 Generation of White Light Illumination with Blue LED and Yellow Phosphor*

Heat dissipation is one of the major functions of packaging. For most applications of LEDs, thermal management may be more important than anything else because the junction temperature can affect the operational life and optical performance of LEDs. The main heat transfer path of LEDs is thermal conduction. Therefore, the substrate design and thermal interface materials (TIM) play major roles in the success of LED applications.

Applications of high-brightness LEDs for SSL is an emerging market driven by the advantages LEDs have over other lighting sources. *Table AP26* presents key parameters for high brightness LEDs. The major advantages of using LEDs include energy saving, long service life, no hazardous substance, and fast response time. The luminous efficiency of LEDs has now passed that of conventional light sources. Nevertheless, for further propagation of high-brightness LEDs for SSL, there still exist several challenging issues:

- The initial cost is too high. The current unit cost per lumen of LEDs is much higher than that of fluorescent lamps. Low cost mass production processes and package designs are needed.
- In order to compensate for the high initial cost, further improvement in luminous efficiency is needed. In addition to the semiconductor thin films, package structure and packaging materials are key issues. Low cost high throughput substrate thinning technology is required. Also, more efficient phosphors and better encapsulation silicones should be developed.
- Thermal management continues to be a critical issue for high-brightness LEDs. Development of more effective TIMs is highly desired.
- The typical failure in SSL applications is not the breakdown of LEDs. LEDs tend to have rather long service life. The more vulnerable part of a SSL system is usually the constant current device for driving LEDs. Therefore, durable LED drivers with matching service life to LEDs are required for heavy duty SSL systems.

*Table AP26 High Brightness LEDs*

### RF AND MILLIMETER WAVE PACKAGING

Mobile phones are the driver for RF packaging up to a frequency of 5 GHz. Today mobile phones include more and more frequency bands for the various standards like GSM, GPRS, EDGE, UMTS or the new HSDPA (High Speed Downlink Package Access) standard. In addition mobile phones include more and more functionalities like GPS, WLAN, WiFi or Bluetooth, which are related to RF. Typically the RF part of a mobile phone consists of an RF front-end, a transceiver and a power amplifier (+ power management) chip including passive components like SAW and BAW filters or RF MEMS. General trend is higher system integration. Today already SoC solutions for RF parts which include GSM, GPRS, EDGE, and HSDPA exist.

Today for transceiver with less I/Os (often single band transceiver) VQFN type packages, which are comparable cheap, are typically used today. But also due to improved front-end chip design VQFN type packages appear for multi-band applications, because less I/O are achieved. LFBGA type packages are typically used for more complex transceiver, which include multi-bands. Transceivers are also set-up for higher integration as System-in-Package, including e.g. SAW

filters or even baseband parts. In today's new mobile phones one can also find transceiver with WLP type devices, which offer the advantages of low cost, miniaturisation and RF performance, but have less integration capability.

Power amplifiers are especially designed as modules. Some solutions also integrate the power amplifier with the front-end antenna switches in the module.

The main interconnect technology used for RF parts is wire bonding and it is expected that this technology will still be important for the future up to 5 GHz. Flip chip is used for some more complex SiP set-ups. A clear trend for transceiver is increasing integration of passives. Here passives integrated in Si substrates offer interesting solutions.

A challenge for the RF part is the ongoing increase of complexity. Thus, for the future new package approaches are required. A promising new solution could be a thin film technology which allows reduction of complexity by appropriate rerouting. Embedded wafer level ball grid array solutions based on reconfigured wafers and thin film technologies are a promising example for future complex RF devices in various frequency ranges. They allow integration of passive components and open interesting possibilities for combining baseband and RF parts. For the future with increasing Si technology performance also software radio based architectures are discussed which require appropriate package solutions.

RF CMOS and CMOS based technologies like SiGe or CMOS on SOI substrates meanwhile are investigated up to 100 GHz region and even beyond. Regions for investigations are automotive radar in the 24 and 77–81 GHz region. For these high frequencies packaging is extremely difficult: The most important challenges are as follows:

- Material constraints (high frequency data for many of the new materials are not available)
- Heat dissipation (~ 3w/mm$^2$ needs to be removed)
- Shielding
- Transmission lines (coplanar or micro strip lines)
- Crosstalk

These high frequencies packaging technologies involving thin film are highly attractive because of their capability for transmission line design. At frequency beyond 40 GHz integration of antennas to the package becomes very attractive. An integrated SiP based solution has the advantage that the internal transmission lines need not be adjusted to 50 Ohm, which allows performance improvement.

### *MEDICAL AND BIO CHIP PACKAGING*

The requirements of medical electronics are often best met with SiP solutions. This is particularly true for implantable and wearable devices such as biosensors, hearing aids, pacemakers, implantable cardioverter defibrillators and similar products. Additional implantable electronic and electromechanical systems are being developed and qualified at a rapid pace. The emerging applications range from drug delivery through integration of biomaterials with integrated circuits for neurostimulation. Future products will incorporate telemetry for real time data monitoring which incorporate RF circuitry and antenna structures that are biocompatible. The requirements for SiP based medical products are similar to those of SiP based products for other applications with two important exceptions. First the reliability required for medical SiP based products is at the highest possible level since a failure may be fatal for the user. Second the environmental requirements of the package have to include exposure to body fluids. There are several areas where additional development is needed for medical SiP. Among those are:

- Low power, biocompatible radios with a signal that can reliably penetrate the human body and package to reach a remote receiver. This receiver is most likely worn by the user.
- Reduced power consumption through improved interconnect
- Power scavenging from the user's body temperature (up to 30 micro Watts/cm2) or motion (up to 10 micro Watts/cm2) to extend battery life of implantable products. This will require research and development of biocompatible MEMS SiP components
- Biological and silicon integration such as neurons grown on silicon. This allows silicon to monitor brain waves to detect seizures and provide counteracting neurostimulus.
- Reliable interoperability of wireless telemetry for medical devices in a world where RF devices operating across a number of frequencies have become ubiquitous.

One common method used in biomedical devices is to illuminate a sample with a suitable light source, then look for the presence, absence, or difference in intensity between two or more wavelengths with photo detectors that may require narrow band optical filters.

Many of the biomedical devices incorporating this sensor concept are disposable products made to detect pregnancy, glucose levels, blood oxygen levels, CO or NOx levels in the air, etc. Thus, they must be rugged, small, required minimal amounts of power to operate on batteries and be manufactured for low cost.

The packaging issues with these products are:

- Mechanical design, especially of the optical elements, to
- ensure optical alignment is achieved initially
- ensure alignment is retained for the life of the product
- protect the optical chain integrity over the lifetime of the device
- Materials selection, especially adhesives
- Protection of the optical system and related electronics from external light and EMI effects
- Protection of the device from the environment including from fluids that are samples either to be evaluated or used in the detection process.
- Selection of the processes and assembly methods for the optical alignment

### MEMS DEVICE PACKAGING

MEMs devices are packaged in an unusually wide variety of ways due to the great variation in requirements. These requirements, and the resulting package solutions, go well beyond those of microelectronic packaging and result in an unusual variety of packages. Examples include MEMs packages for the following:

- Devices, such as transmit/receive switches, must exclude moisture to prevent deterioration or corrosion and might require an inert atmosphere to remain stable
- Pressure sensors must be open to atmospheric pressure but not be susceptible to moisture damage
- Optical devices, such as camera modules, must exclude particles, must not have organics that can condense on optical surfaces over time, require optical windows and must maintain optical chain alignment over the product life.
- Devices requiring controlled atmosphere; vacuum, inert gas, etc.
- Devices that analyze fluids require containment of those liquids and must not leak
- Devices requiring ESD protection greater than that required by CMOS devices

Even though the term MEMS means “micro electro mechanical system”, many devices that are considered to be MEMS devices have no moving mechanical parts.

The first choice for a MEMS device package is a standard, off the shelf microelectronic package. Unfortunately, those packages are often inadequate for specific MEMS applications, so engineers must modify the design or design a unique package for manufacturing.

MEMS devices are sometimes designed to use wafer level packaging. Some wafer level methods use overmolding; some use wafer to wafer bonding; some build a cavity within the MEMS structure and seal it at the device fabrication level. The selection and design of a MEMS package can be a major portion of the effort needed to bring a MEMS product to market.

One key emerging technology used to reduce cost and improve performance of MEMS devices is the integration of MEMS devices with standard semiconductor devices which provide drive, control, and signal processing functions. This approach enables increased integration and reduction in cost. This may be enabled for many MEMS device types through a low cost wafer level package which can provide cavities. Technologies which enable the decoupling of package stress through the bump or die attach to the MEMS structure are also a critical challenge for MEMS in wafer level packages.

The approach consisting to introduce the cap at the wafer level (called Wafer Level Caps) is today in production. This technique requires further steps (wire bonding, overmolding, BGA). WLC caps are done for absolute pressure sensors, inertial sensors or capacitive sensors. Thin film encapsulation at the wafer level scale could be employed for RF MEMS and inertial MEMS (no contact with environment, specific pressure on cavity). Bonding technologies are developed with intermediate layer (glass frit, adhesive, metal) or without intermediate layer (anodic, direct or fusion bonding). The main technical challenge on WLC is to shift on high vacuum and hermetic bonds on resonators and accelerometers sensors in order to increase the sensibility.

Wafer level packaging approach where the wafer encapsulation is doing with interconnections and bumps. The developments for WLP MEMS focus on developing capping technologies with through silicon vias, redistributive die

layers and bumping steps. It's clearly the way to 3D integration. Wafer level packaging has just starting in production last year for inertial MEMS and Si microphones.

Tables AP27 and AP28 provide a broad overview of the MEMS packaging methods and some specific examples.

*Table AP27 MEMS Packaging Methods*

*Table AP28 MEMS Packaging Examples*

## *ELECTRONICS IN TEXTILES AND WEARABLE ELECTRONICS*

### WEARABLE ELECTRONICS

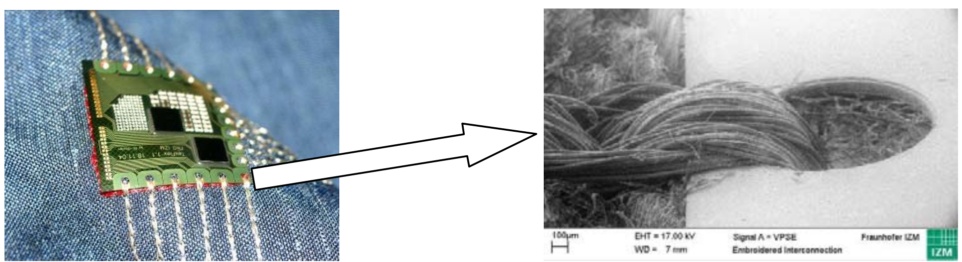
The integration of electronics into textiles requires four important issues to be solved:

- Interconnection of electronics with conductive textiles
- Encapsulation of electronics and interconnections
- Isolation of conductive textiles or the local removal of pre-isolated textile conductors
- Development of reliability tests for electronics in textiles in different applications
- High volume low cost manufacturing

The most popular interconnection approaches are soldering, adhesive bonding, crimping, and embroidering. Some R&D in this field is covered by research institutes, e.g., Fraunhofer IZM. Encapsulation technologies that are currently investigated for the use in electronics in textiles are transfer molding, hot-melt encapsulation, liquid encapsulation, and dam-and-fill and glob top encapsulation. The main challenge for the interconnection and the encapsulation are ensuring the reliability during textile typical treatment, be it for wearable electronics or for technical textiles applications.

A critical issue that has not been investigated much is how to isolate conductive textiles or alternatively how to locally remove the isolation of pre-isolated conductive textiles. Ideas include lamination or liquid coating. Materials in focus are polyurethane or silicone either in solvent or as two component material that cures. Even more challenging is the development of a smart coating that coats only metallic parts and leaves the non-conductive textiles unchanged.

Before manufacturers incorporate electronics in textiles developing wash tests, wear tests and other reliability tests for textile integrated electronics is essential. This is not simply summing up electronics test standards and textile test standards since they are not compatible. New reliability tests and test standards have to be developed based on the real stress on electronics in textiles. See Figure AP39.




*Graphic courtesy of Fraunhofer IZM*

*Figure AP39 Texflex Embroidered Interconnects*

Standard flex circuit assemblies only allow for bending deformation along one dimension, allowing for cylindrical and conical shapes. More complex surface shapes, such as spheres, cannot be realized. This requires stretching of circuit surface. Elastomeric polymers, such as silicones and polyurethanes, can be used to make the flexible substrate "stretchable." However, an electronic interconnect also requires electric interconnects that run on or inside this polymer

matrix. The challenge is to realize stretchable electrically conductive interconnect lines on/in stretchable polymer materials.

Techniques used to achieve flexible conductors:

- The use of metal interconnects incorporating electrical conductors in spring shapes (e.g., horseshoe meandering lines). This typically results in longer interconnect lines with a lower interconnect density. Good results are shown for stretchable conductors in a single direction. More challenging designs are needed for stretchability in two perpendicular directions, as follows:
- Use of conductive particles in the polymer matrix. This requires a high filling density, above the percolation limit for conductivity, which may fundamentally limit its stretchability. Conductivity will vary significantly with applied strain.
- Use of conductive polymers to render part of the polymer body conductive. Obtaining a high conductivity is a key challenge.

Combinations of metal tracks and conductive polymers or embedded conductive particles: normally conductive metal tracks are used in parallel to the higher resistance conductive polymer solutions. Stretching of the conductors occurs mainly in localized parts of the polymer matrix. Most of the current is conducted through the parallel conductor straps.

#### FLEXIBLE ELECTRONICS

Flexible electronics is projected to grow into a multibillion-dollar industry over the next decade and will revolutionize our view of electronics. The unique properties of flexible electronics, such as its compliant structures, ultra-thin profiles, low weight, and potential low cost and high reliability could have enormous impact on consumer electronics, aviation and space electronics, life sciences, military applications and telecommunications. Flexible electronics will enable a broad range of devices and applications not possible today. Smart clothing with integrated electronics and displays will have many consumer, medical and military applications. Realizing the possibility of smart active bandages, and other medical devices such as reconfigurable systems and sensors, micro drug-delivery systems, active/integrated prostheses and massively parallel secure and fault free distributed environmental field sensors will have the potential to change the way people detect and deal with disease and pathogen exposure. Some examples are:

- Energy: large area, low cost photovoltaic devices; energy efficient lighting
- Military: soldier portable power products and rugged, lightweight imaging devices
- Medical: medical sensors, intelligent bandages and soft tissue implants
- Agriculture and civil infrastructure: large area sensor nets; food safety
- Transportation: hazard warnings; automated roadways; cargo container tracking

The application areas and products shown above will require significant infrastructure development in the areas of tooling, processes, and materials. Many of products identified will require large area flexible electronics, with feature scales ranging from meters to the sub micron on the same product. Tools and processes to build such products do not currently exist. There will also be a need to develop new substrate materials, new barrier materials, new coatings, and adhesives. For example medical applications that require implanting electronics will have to be constructed of materials that are non toxic, stable and that withstand specific harsh chemical environments. Avionic and space applications will require specific radiation hardening. Wearable textile electronics will require ability to withstand common laundry process.

### *AUTOMOTIVE PACKAGING*

In the automotive use, normal packages are basically used. The requirements for automotive packaging are as follows.

- Miniaturization: The miniaturization of the electronics set is demanded to enlarge the space that the human being occupies.
- High performance: In correspondence with high frequency and high functionality of devices, high performance (high pin count, low resistance etc.) are demanded.
- High temperature: High temperature is demanded by the deployment to the engine room and the high performance of devices.
- High thermal dissipation: Low thermal resistance is demanded by the high frequency and high performance of devices.
- High reliability: As the machine in which a human being rides, a demand to the reliability is very strong.

In particular the requirements for automotive packaging are high temperature, high thermal dissipation and high reliability. The operating environment specification for automotive electronics is presented in Table AP29. Due to the high temperature, high device operating temperature is necessary, but high Tg (Glass transition temperature) of the mold resin material and the package substrate material is important. For high thermal dissipation, the package structure with heat-spreader such as HQFP, HSOP and HBGA is used, and the further lower thermal resistant structure is demanded. For high reliability, the high reliable design including materials, structure and process, and the high quality process management are important. For high performance, SiPs are also used for automotive packaging.

*Table AP29 Automotive Operating Environment Specifications*

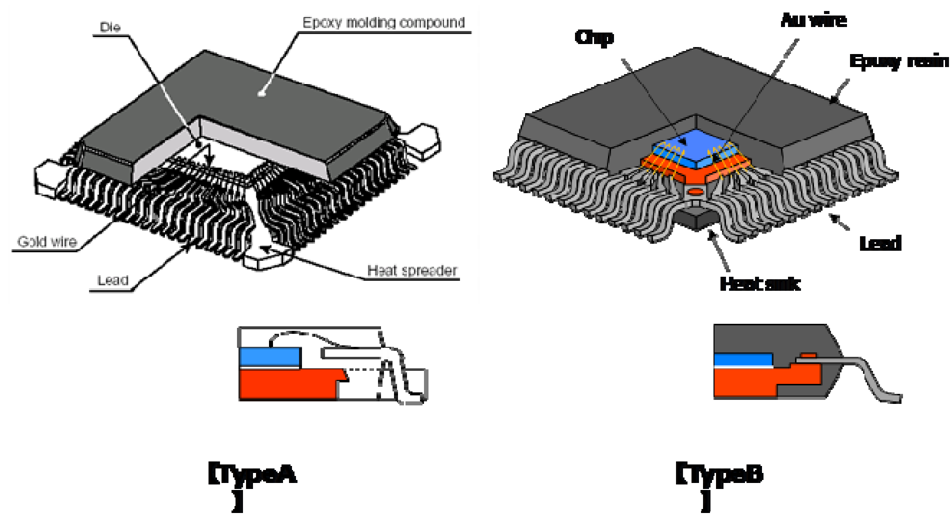



*Figure AP40 HQFP for Automotive Electronics*

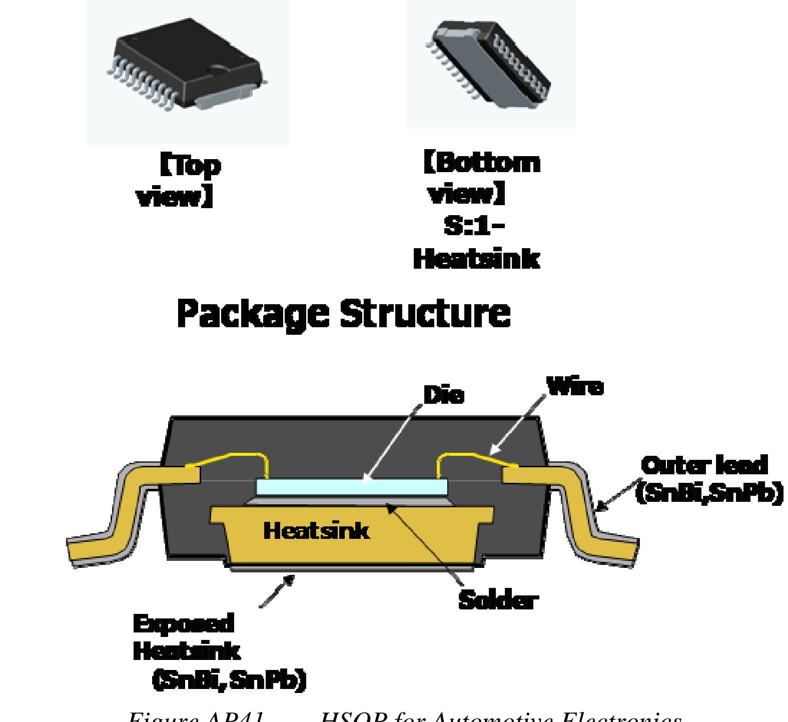



*Figure AP41 HSOP for Automotive Electronics*

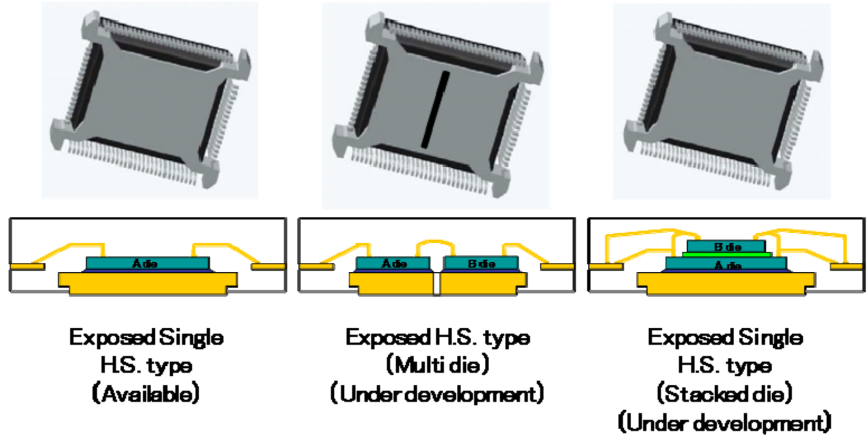



*Figure AP42 SiP-HQFP for Automotive Electronics*

### SOLAR CELL PACKAGING

The rapid growth of the solar power has generated a need to address the unique packaging requirements for packaging solar cells and solar cell arrays. Solar cell modules face temperature extremes and must have a very long life compared to almost any other packaging requirement. The current state of the art for the photovoltaic modules used in solar cell arrays is:

- Semiconductor thickness 180 µm
- Soldered with high-throughput tabber-stringer
- Vacuum lamination
- EVA as encapsulant

- Guaranteed lifetime of 25 years

The continued expansion of solar power and the changes anticipated in the solar cells will require focus on additional parameters to meet the packaging requirements. Table AP30 presents the key parameters for packaging of multiple-sun solar cells. These new requirements include:

- Low-stress interconnection for very thin solar cells (between 100 and 150 µm thick)
- High throughput lamination technology
- Pb-free soldering solutions
- 30 years lifetime
- Design for easy recycling at end of life

*Table AP30 Multiple-Sun Photovoltaic Cell Packaging Issues*

# ADVANCED PACKAGING REQUIREMENTS

## *EMBEDDED AND INTEGRATED ACTIVE AND PASSIVE DEVICES*

Integrated passive devices (IPD) are subcomponents, which exclusively contain passive components. They contain all three types of passives (R, L, and C) as well as only two or one type or any combination. The elements can be connected to each other in order to realize certain network, matching or filter functions or stand for their own to realize only single resistive, inductive, or capacitive functions.

The introduction of new materials like thin oxides or filled polymers as dielectric extends the value range for capacitors to maximum values in the micro farad range. Besides standard redistribution wiring systems it is also possible to realize ground planes and transmission lines to create impedance controlled RF-signal transmission.

The use of wafer level thin film processes (polymer-metal-oxide) technology offers the possibility to manufacture application specific WL-IPDs with passives in the following value ranges:

- Resistors: 10 Ohm–150 kOhm (e.g., NiCr 100 Ohm/sq; TaN 25 Ohm/sq.)
- Inductors: 1 nH–80 nH (Q: 30–150)
- Capacitors: (3–6) pF/ mm² (er=2.65, e.g., polymer BCB)
- Capacitors: (1–3) nF/ mm²(er=23, e.g., $Ta_2O_5$)

With this value range nearly 70 % of capacitors and 95% of resistors and nearly all inductors of the required passive elements for a wireless cellular can be realized, which demonstrate the large potential for system miniaturization.

WL-IPDs are designed as flip chip mountable as well as wire bondable components by using different thin film substrates like silicon, alumina, or glass. Figure AP43 shows an example of an integrated passive device as a CSP with 2× low-pass filter with 3× inductors 3.9 nH, 2× capacitors 1.8 pF realized with a multi-layer polymer-metal (Cu) redistribution layer on Pyrex.

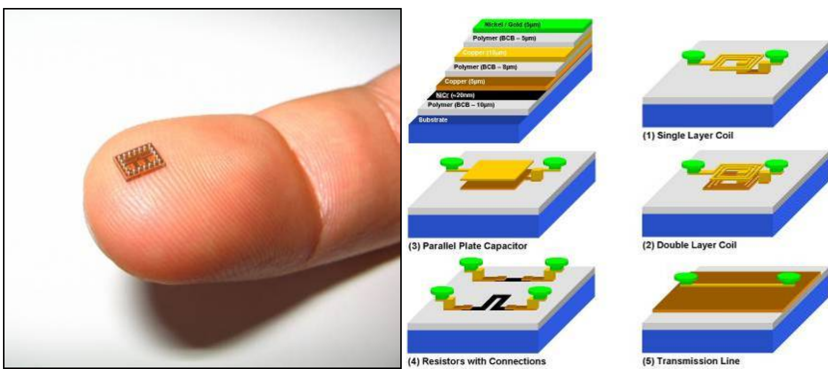



*Figure AP43 CSP with Integrated Passive Devices and Thin-film Build-Up Passive Elements*

Today's bottleneck for the realization of integrated passive devices are capacitors, in combination with high aspect ratio deep reactive ion etching (DRI) in silicon deep trench capacitors with a value of (20–30 nF /cm$^2$) can be realized. This very promising technology is currently in development by several companies with focus to wafer level System in Package approaches. With respect to cost and form factor, larger passive devices are implemented as SMD devices on top or embedded into substrates for System in Package approaches.

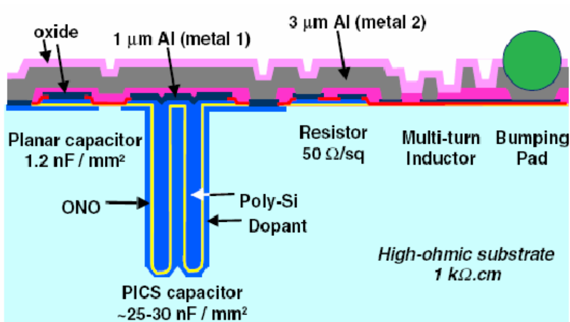



*Figure AP44 PICS Substrate with High Density "Trench" MOS Capacitors, Planar MIM, Multi-Turn Inductors, and Poly-Si Resistors*

### APPLICATIONS FOR EMBEDDED ACTIVE AND PASSIVE DEVICES

Current applications on embedded active devices are cellular phone related products e.g., TV tuner, finger print ID sensor. Cellular phone and semiconductor manufacturers are expecting next generation products on embedded active devices for communication modules e.g., GPS and wireless LAN with passive devices on surface which use the space "liberated" by embedding active devices. In addition, power supply units with embedded actives and surface mounted passives have also strong demands from market place. Also, image sensors such as CMOS sensor and strobe light for cellular phone camera will adopt embedded active devices with surface mount passives for reducing form factor. In the very near future, ASICs and graphic processor with stacked memory devices as well as DSC will use embedded active and passive devices.

At this time, two different types of active device are common for embedded applications. One is wafer level package with thinned embedded active devices without copper post for enhanced mechanical strength which are directly interconnected by thin film RDLs, and the other is flip chip with stud bump or copper posts embedded in organic laminates substrates. Figure AP45 represents a schematic overview.

For the economical production of embedded active and passive devices in organic substrates, a chip bonder compatible with printed circuit board work panel size is required. The major issues for embedded technologies are test, yield and quality assurance. Test standards and the implementation of a responsible supply chain are needed for market adoption of embedded active and passive devices.

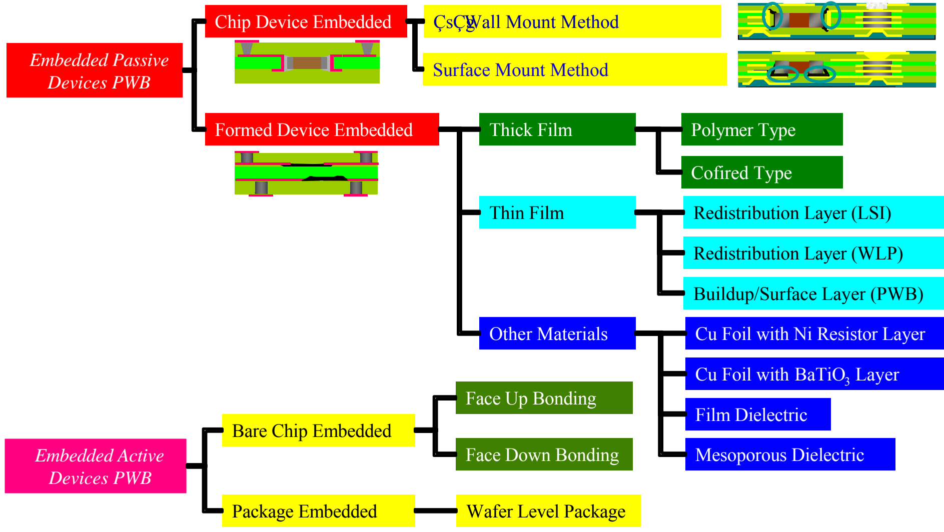



*Figure AP45 Overview of Embedded Active Devices and Passive Devices*

## Wafer Thinning and Singulation

Wafer thinning is a key enabler for thin packages, stacked die packages and, most recently, packages with through silicon vias (TSV). While wafer singulation typically follows wafer thinning, several new process combinations are possible to accommodate packages which have multiple die and wafer based processes. These are described in Figures AP46, AP47 and AP48 below.

### Wafer Thinning

In 2009, thinned wafers of 50-75 µm are common. The roadmap for wafer thinning is shown in *Tables AP31* and *AP32*. Wafers are typically processed by mechanical grinding with a resin bonded abrasive wheel, followed by chemical mechanical polishing (CMP). Dry and wet etch methods are also available, but are less economical. Prototypes of 5 µm thickness, after careful processing, have been reported, but the infrastructure for such thin wafers is limited. The major technical challenge in wafer thinning is to retain wafer and die strength. Two prominent failure mechanisms and their mitigation are described below.

First, mechanical grinding generates defects on the wafer surface. These defects may propagate as cracks during wafer handling and assembly operations, possibly leading to failures after assembly and environmental exposure. Stress relief by polishing, commonly by CMP, removes the defect layer and thereby strengthens the wafers.

Second, during thinning, the wafer rim progressively changes shape from a round profile to a sharp edge. Edge defects may initiate cracks during handling, leading to wafer breakage. The thinnest wafers have the sharpest edge and therefore are most susceptible to damage. New techniques have been developed to avoid edge cracking. A first technique is to cut the wafer circumference to remove the sharp edge. A second method is to grind the wafer over a region which does not include the wafer rim. The intact wafer rim supports the wafer during subsequent handling. A third method is to employ a carrier which supports the wafer though the processing after thinning, such as in the double sided processing required for TSV. A fourth option is to perform dicing before grinding (DBG), described as a singulation technique below.

Bumped wafers are thinned by mechanical grinding. The wafer is partially immersed in an adhesive material during processing. Dry etching may be used to remove top layer defect. As the bump side of the wafer is not protected, however, CMP is typically not used. Alternatively, wafers may be bumped after thinning by using special handling equipment or a sacrificial carrier.

*Table AP31 Thinned Silicon Wafer Thickness 200 mm/300 mm*

*Table AP32 Challenges and Potential Solutions in Thinning Si Wafers*

### WAFER SINGULATION

Sawing by a resin bonded diamond blade is the most common singulation method. However, the blade sawing process creates defects at the die edge. So called *chip-outs* may propagate as cracks during assembly and environmental exposure and may result in full die cracks. Chip-outs become more severe with thinner wafers and narrow scribe lines, and are typically reduced by optimizing the dicing blade and process parameter. Nevertheless, a residual amount of defects persist, especially for low-k wafer fabrication technologies. To arrest crack propagation, wafers are designed with seal rings at the die periphery. In recent years, laser based techniques provide a way to significantly reduce chip-outs. The two most common techniques are full laser cutting and laser grooving on both side of the scribe line which is followed by a mechanical saw cut to remove the remaining material.

Dicing before grinding (DBG) is another way to reduce wafer defects while mitigating wafer edge and surface defects in thin wafers. In DBG, the wafer is "pre-cut" by either etch or sawing, followed by wafer thinning to complete the wafer singulation process. Several process options are reported elsewhere. [7]

Recently, a new technique has been developed where a laser beam is focused at the wafer center, rather than the surface as in laser grooving. The localized heat converts the crystalline silicon at the wafer center into polycrystalline silicon which has more volume and, in turn, creates a localized compressive stress. The silicon is then cleaved by stretching the wafer film frame, leading to a clear separation into individual dice along the laser scan lines. The technique has been shown to reproducibly singulate dice with scribe lines below 16um, leading to very optically smooth surfaces without chip-out. By contrast, the scribe line region in conventional is typically 60-100um in width. The proposed applications for the new technique for (i) die where very little or no chip-out is allowed, such as automotive, wafer level packaging, or wafer with low-k dielectric which are susceptible to chip out, (ii) small die where a very narrow scribe line will allow a greater number of dice per wafer and (iii) wafers with multiple die of different size or non-rectangular die shapes.

### PROCESS FLOWS ASSOCIATED WITH WAFER THINNING AND SINGULATION

As noted above, there is additional complexity to the process flows for packages with multiple die (System-in-Package) and wafer based processing. Figures AP46-48 divide these process flows into three categories and show examples of the flows for wafer thinning and singulation in the context of each category. For simplicity, the use of a sacrificial carrier(s) is not shown explicitly in the figures. The three categories are:

1. Single die flows – process of thinning and singulation for a single die; may have multiple die in a package by stacking single die or side-by-side format.
2. Heterogeneous die flows/die on wafer – one or more dice are thinned and singulated before bonding to a thinned wafer which is, in turn, singulated.
3. Homogeneous die flows/wafer bonding – thinning and stacking of wafers prior to singulation.

Following the final singulation, the single die or die stacks are processed further using common interconnection technologies such as wirebond, flip chip and ball attach.

[7] *Shinya Taku, et al. SiP Whitepaper. page 98. ECTC 2006.*

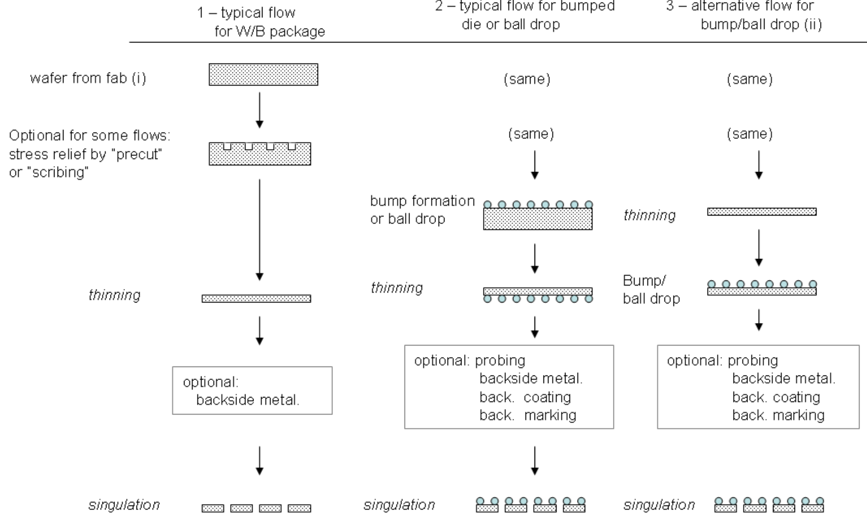



*Figure AP46 Extract of Thinning and Singulation Process Flow for Single Die Package*

Heterogeneous Stacked Die / Die-on-Wafer
(based on 2-die case, stack additional die as needed**)

#1 (top)
#2 (bottom)
#2 (bottom w/TSV & bumping)
wafers from fab
bumping*
thinning*
thinning*
bumping*
singulation
**
die bond
(option to stack >1 die)
**
singulation

* may change order of bumping & thinning

**presents handling challenge

*Figure AP47 Extract of Thinning and Singulation Process Flow for Packages using Die on Wafer Process*

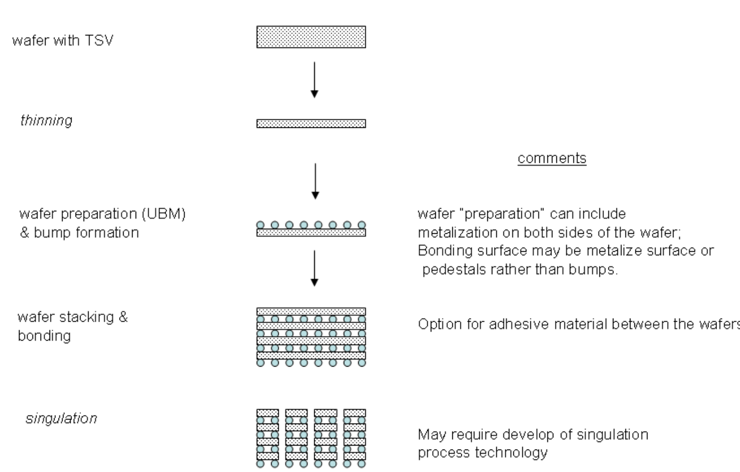



*Figure AP48 Extract of Thinning and Singulation Process Flow for Packages using Bonded Wafers*

# PACKAGING MATERIALS REQUIREMENTS

Packaging materials are at the heart of Assembly and Packaging Technology. Packaging material contributes significantly to the packaged device performance, reliability, and workability as well as to the total cost of the package. With the advent of the “More Moore” and “More than Moore” initiatives, the challenges for packaging materials have broadened from requirements for traditional packages for future generations of devices as well as for new package types such as the SiP package families, wafer level packaging, IPDs, TSVs and for applications in RF, MEMs, and optoelectronics.

The Assembly and Packaging industry has been in the midst of a sea change in materials. The bill of materials in today’s packages may not be the same tomorrow. Furthermore, these changes are expected to accelerate in pace and scope in the coming years. Much of the near-term new materials introduction is driven by environmental regulatory compliance requirements including Pb-Free and RoHS compliance (European Union Directive for Reduction of Hazardous Substances). The migration to “green” materials that are lead-free and halogen-free compatible are in full swing. Industry has been adopting “green” materials for the new products packages when they transition to new packaging materials to meet RoHS requirements. Materials for the traditional wire bond and flip chip packages including molding compound, die attach materials, underfill materials, thermal interface materials (TIM), and package substrates, will have to be improved to meet lead-free, halogen-free, and low-κ/ULK requirements.

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly advanced next generation devices. While wirebond and flip chip remain the two basic interconnect methodologies, the introduction of low-κ dielectric materials, increasing power density and hand held consumer products, imposes additional requirements to traditional materials applications. For example, with the mechanically weak low-κ and the still weaker ultra low-κ dielectrics in the device, comprehensive design of underfill materials properties compatible with the bump materials properties are crucial in addressing the risk for interface stress damage to the dielectric layer. With the increasing thermal output and uneven temperature distribution of many IC device applications, thermal interface materials represent an important opportunity for innovation. The drive for miniaturization through die stacking, package stacking, and low profile packages requires improvements in molding compounds, underfill materials and die attach materials originally developed for traditional single chip packages.

The developments of potential solutions, such as SiP, wafer level packaging, embedded die and passives, and TSV, will call for innovations in design of materials and materials processing innovations beyond what is available today. Wafer level packaging will require materials with improved or different properties as it evolves to meet new packaging applications. Different metallization systems for both redistribution traces and under bump metallization, as well as new dielectric polymers, are needed to meet the ever changing reliability requirements for portable electronic devices. The

development of fan-out WLP and embedded passives/actives will require new low-temperature embedding polymers and low-temperature cure redistribution layer polymers. TSVs will benefit from new dielectric insulators and conductive via filling media for improved low cost manufacturability. Integrated passive devices (IPDs) will also require better materials, with improved electrical properties, for both resistive and capacitive devices. The major materials challenges are summarized in Table AP33.

*Table AP33 Materials Challenges*

# CROSS-CUT ITWG ISSUES

## ENVIRONMENTAL ISSUES

Environmental issues are gaining more attention with expanding restraint on the use of chemical substances in legislation and additional regulatory actions as new materials are developed and the health and safety issues associated with materials currently in use are better understood. The environmental protection laws originated in Europe have been affecting the legislation in other industry countries, thus resulting in the establishment of similar laws in these countries (see Figure AP49). These laws have constrained packaging engineers from adopting restricted substances. One of leading actions in electronics industry has been lead-free conversion. Today, most of packages used in consumer market do not use lead-contained materials except die-attach materials for power devices and some flip-chip bumps. The deployment of lead-free material in consumer market is now affecting other market segments for fear of phasing out conventional lead-contained materials and possible increases in cost. Even heavy duty-industry sectors have started to find a replacement for the conventional lead-contained devices. Following the lead-free requirement, halogen-free packages would be the next requirement to solve, such as halogen-free retardants for molding resin or solder resist for a package substrate.

The recent regulation, REACH, gives greater responsibility to industry to manage the risks from chemicals and to provide safety information for these substances. Manufacturers and importers will be required to gather information on the properties of their chemical substances, which will allow their safe handling, and to register the information in a central database. It requires complete chemical database on the manufacturer's side through the entire supply chain from the raw material to the final products. A leading example of the activities that integrate the chemical information through supply chains is "Joint Article Management Promotion Consortium (JAMP)" in Japan, which attempts to manage seamless information transfer of restricted substances through whole global supply chain and promote cross-industrial activities to facilitate disclosure and conveyance of information on chemicals contained in the products. This type of consortium will be helpful globally as industry works to comply with the evolving tighter environmental regulations.

| | |
|---|---|
| ELV | Directive on end-of life vehicles |
| RoHS | Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment |
| WEEE | Directive on waste electrical and electronic equipment |
| EuP | Directive on the eco-design of Energy-using Products |
| REACH | Registration, Evaluation and Authorization of Chemicals |
| SB20 | Electronic Waste Recycling Act in California, US |
| J-Moss | The marking of presence of the specific chemical substances for electrical and electronic equipment |

*Figure AP49 Environmental Protection Laws Spreading Worldwide*

There are many environmental considerations and the issues are changing rapidly as nano-materials are incorporated into devices and packages. Please refer to the *Environment, Safety and Health* chapter for information about these issues.

## DESIGN

The complexity of emerging packaging technology is blurring the boundary between wafer fabrication and packaging. This requires Co-design tools addressing electrical, mechanical and thermal properties for advanced packaging. The EDA industry has been making progress but much work is yet to be done. Collaboration between Design, Interconnect and Assembly and Packaging TWGs is in process to identify the specific needs. Specific actions planned include:

- Joint effort to define metrics for functional density and cost which can be used to prepare a table for quantification of the relative value of functional diversification vs. More Moore.
- Select an emulator for design of complex SiP which can be used to identify difficult challenges and potential solutions
- Assembly and packaging will prepare specific TSV requirements for the Design TWG

## INTERCONNECT

The boundary between Assembly and Packaging and On-chip interconnect has been a major issue as we enter the era of 3D integration. We working together to minimize duplication, establish a clear delineation between assembly and global interconnect and clarity between chapters to ensure no conflicting input.

The issues associated with Through Silicon Via are addressed in both the *Interconnect* chapter and the Assembly and Packaging chapter. The Interconnect TWG focus is centered on the CMOS process and on-chip global interconnect while the Assembly and Packaging focus is on post CMOS process and 3D integration with multiple die. While each of the TWG focuses are distinct and separate we recognize that there is a blurring at the boundaries. The reader interested in a full understanding of the Roadmap for 3D integration should review both the Interconnect and Assembly and Packaging chapters.

Cross TWG Issues between Assembly and Packaging and Interconnect for 2010 will include:

- Better dielectrics (both low k and high k)
- Assembly implications for air gap structures
- Nano wires
- Embedded passives
- 450 mm
- Continued refinement of 3D issues

## RF/AMS WIRELESS

The RF/AMS Wireless TWG has set up a separate group focused on MEMS devices used in RF/AMS circuits. The MEMS devices they address include:

- RF switches
- Resonators
- Passive networks

- Power amp
- Base band elements
- Shielding
- Antenna structures

There has also been a MEMS section in the Assembly and Packaging TWG. A focus of the cross-TWG activity will be to coordinate the content of these MEMS sections very closely with the long term objective of combining the sections into a separate MEMS section for the Roadmap. This has increasing importance as "More than Moore" drives the incorporation of MEMS devices in larger number as both stand alone packaged devices and as components in SiP.

### MODELING AND SIMULATION

The rapid change in package requirements as new packaging processes and architectures are adopted places a premium on modeling and simulation tools to speed the introduction of new packages that successfully meet all requirements. The issues for Assembly and Packaging identified in cross TWG meetings include:

- Tools for modeling packages to address:
- Support for co-design and simulation
- Modeling for SiP
- Modeling for Wafer level packaging
- Thermal/mechanical modeling for packages
- Interconnect models for packages
- Interface between the modeling tools for devices with those for packages

Diversification of package types and incorporation of more 3D structures with a large number of interfaces has complicated the simulation requirement and increased the need for the simulation capability. Thinned die and packages also require dynamic simulation of mechanical properties for flexible substrates and packages. These areas are long range projects and will require continued cross TWG coordination.

### EMERGING RESEARCH DEVICES, EMERGING RESEARCH MATERIALS (ERD, ERM) COORDINATION

There has been close cooperation between ERM and Assembly and Packaging to identify materials requirements for future packaging requirements. The requirements identified through our collaboration can be found in the *ERM* chapter and will not be repeated here.

The work in ERD to identify future device types will result in new package requirements. The incorporation of extreme CMOS is one example which brings new problems in stress management. The identification of these potential problems through coordination between these TWGs should provide adequate lead time to develop solutions.

### TEST

New architectures and new material in packaging are placing new requirements on test. These issues include:

- The need for functional test of known good die as components in SiP architectures
- Test access for SiP and other 3D architectures
- Handling of thinned die for testing at acceptable cost
- Contactors that can handle the tighter contact pitch
- Low pressure contactors compatible with porous dielectrics and thinned die

Many of these challenges are covered in the *Test and Test Equipment* chapter in more detail.

## SUMMARY

The material in this chapter is changing as the architecture, materials and processes for packaging change. The slowing of Moore's Law scaling has contributed to an accelerated pace of innovation in the technologies for assembly and packaging to continue the increase in performance and reduction in cost that has driven the growth of electronics. There are several areas where gaps in the Roadmap and technology needs are known that may not be addressed in the body of this chapter for 2009. *Table AP34* presents a list of these gaps and technology needs.

Assembly and Packaging must contribute to reduced cost, higher functional density, improved performance and reduced power consumption it the price elastic growth of the industry is to continue. The rapid pace of innovation in 3D integration, wafer thinning, direct bonding, etc. requires significant investment in research and development. This comes at a time when the companies engaged in assembly and packaging are working with very low margins and lack the ability to make large investments in research and development. The response to this has been the growth of consortia where companies combine their resources to address major technical challenges. Table AP35 lists consortia that address assembly and packaging challenges.

*Table AP34 Packaging/Gaps/Technology Needs Summary*

*Table AP35 Consortia and Research Institutes in Packaging Technology*

# GLOSSARY

*System in package (SiP)*—System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system.

*Wafer level packaging (WLP)*—Wafer level packaging (WLP) is a technology in which all the IC packaging and interconnection is performed on the wafer level prior to dicing. All elements of the package must be inside the boundary of the wafer. Chips mounted on a structured wafer (e.g. by face to face technologies) and packaged at wafer level before dicing are also considered as wafer level packages.

*Integrated passives*—Integrated passives are arrays or networks of passive elements including resistors, capacitors, and inductors integrated on a single substrate to form a single passive component.

*Embedded passives*—Embedded passives are passive components that are incorporated into an IC, added on top of an IC through the addition of a layer, embedded in a build-up polymer interconnect layer or embedded in a package substrate.

*3D packaging*—3D packaging refers to packaging technologies where a substantial fraction of the die to die interconnections are not planar to the package substrate.

*QFP*—A ceramic or plastic chip carrier with leads projecting down and away from all sides of a square package. Usually, the back side of the die is bonded to the lead frame substrate, and the electrical connections are made on the active top side of the die through wirebonding process and the whole package is encapsulated by a molding process.

*QFN*—A ceramic or plastic chip carrier with contact leads underneath the four sides of the package. Usually the backside of the die is bonded to the lead frame substrate, and the electrical connections are made to the die active surface through the wirebonding or flip chip process.

*P-BGA*—A plastic package employing an array of solder balls for physical connection to the next level which is usually a printed circuit ball. Usually the back side of the die is bonded to a laminate substrate, and the electrical connections are made on the active top side of the die through wirebonding process, and the top side of the package is encapsulated by a molding process.

*T-BGA*—Tape BGA. Similar to P-BGA where the substrate are made of a circuitized metal on a polymer tape. The interconnection to the die may be made by thermocompression bonding in a single step.

*FC-BGA*—Flip Chip BGA. Similar to P-BGA where the die to substrate interconnection is made with the flip chip process, i.e. the die faces down with interconnection made through metal (solder) bumps on the die. Usually the space between the die and the substrate is filled with an underfill material.

*FC-LGA*—Flip Chip Land Grid Array. Similar to FC-BGA, without the solder balls on the array of contact lands on the substrate

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