INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2009 EDITION

EMERGING RESEARCH MATERIALS

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EMERGING RESEARCH MATERIALS

SCOPE

This chapter provides the material research community with guidance on specific research challenges that must be addressed in a laboratory setting for an emerging family of candidate materials to warrant consideration as a viable ITRS solution. Each international technology working group (ITWG) has identified needs for new materials to meet future technology requirements and assessed the potential for low dimensional materials (carbon nanotubes (CNTs), nanowires, graphitic systems, and nanoparticles), macromolecules, self-directed assembled materials, spin materials, complex metal oxides, and selected interfaces. For these emerging materials, this chapter presents requirements for materials, processes, interfaces, and supporting metrology, modeling, and simulation. In the 2009 ERM, we include a critical assessment of alternate channel materials for CMOS extension. To enable this assessment, the ITRS ERM is being restructured focus on applications where different materials for the same application will be discussed in the same section. In addition, the ERM includes results of a joint ERD-ERM assessment of beyond CMOS technologies needing increased focus to accelerate progress.

The scope of emerging research materials (ERM) covers materials properties, synthetic methods, metrology, and modeling required to support future emerging research devices (ERD), lithography, front end process (FEP), interconnects, and assembly and package (A&P) needs. For ERD memory and logic devices, the scope includes planar III-V, Ge, nanowires, carbon nanotubes, graphene and graphitic materials, spin materials, and complex metal oxides. Furthermore, the special assessment of beyond CMOS logic identified that carbon based (carbon nanotubes and graphene) materials and devices receive increased focus, so a potential solutions table is included. Some of the evolutionary and some of the revolutionary ERD can be fabricated with conventional materials and process technologies that are already covered in other sections of the ITRS, so the ERM chapter will not cover these materials and processes. Emerging lithographic materials include novel molecules, macromoloecules, and mechanisms that exhibit the potential to enable ultimate feature patterning with resist, or self assembled technologies. FEP materials include ERM required for future device technologies including technologies to place dopants in predetermined locations (deterministic doping) as well as novel materials to support selective etch, deposition, and cleaning of future technologies. Interconnect materials include emerging materials for extending Cu interconnects (novel ultrathin barriers), novel low resistance sub-20 nm electrical contacts, interconnects, vias, and ultra-low κ inter level dielectrics (ILD). Assembly and Packaging materials include novel materials to enable reliable electrical and thermal interconnects, polymers with unique and potentially useful combinations of electrical, thermal, and mechanical properties, and ultra-high power density high speed capacitors.

This year's ERM chapter includes the following material families: III-V and Ge materials, low dimensional materials, macromolecules, self assembly mechanisms and self-assembled materials, spin materials, interfaces, complex metal oxides, and heterointerfaces. Many of these materials exhibit potential to address projected requirements in multiple application areas. *Table ERM2* in the Introduction section maps families of ERMs to potential applications identified by the above Focus ITWGs. Future editions of this chapter also will comprehend and evolve projected ERM requirements for targeted functional diversification related applications.

DIFFICULT CHALLENGES

The Difficult Challenges for Emerging Research Materials is summarized in *Table ERM1*. Perhaps ERM's most difficult challenge is to deliver material options, with controlled and desired properties, in time to impact insertion decisions. These material options must demonstrate the potential to enable high density emerging research devices, lithographic technologies, interconnect fabrication and operation at the nanometer scale, and packaging options. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled directions, dimensions, and compositions. Another critical ERM factor for improving emerging device, interconnect, and package

technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. For novel nanometer scale materials emerging within the research environment, methodologies and data also must be developed that enable the hierarchical assessment of the potential environment, safety, and health impact of new nanomaterials and nanostructures.

The difficult challenges listed in Table ERM1 may limit the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and nanostructure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish quantitative relationships between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the design and optimization of the required materials properties. The need for validated models requires strong alignment between experimentalists and theorists when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

Table ERM1 Emerging Research Materials Difficult Challenges

Difficult Challenges ≤16 nm	*Summary of Issues*
Integration of alternate channel materials with high performance	III-V has high electron mobility, but low hole mobility
	Germanium has high hole mobility, but electron mobility is not as high as III-V materials
	Demonstration of high mobility n and p channel alternate channel materials co-integrated with high κ dielectric
	Demonstration of high mobility n and p channel carbon (graphene or carbon nanotubes) FETs with high on-off ratio co-integrated with high κ dielectric and low resistance contacts
	Selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers (III-V, Graphene, Carbon nanotubes and semiconductor nanowires)
	Achieving low contact resistance to sub 16nm scale structures (graphene and carbon nanotubes)
	Ge dopant thermal activation is much higher than III-V process temperatures
	Growth of high κ dielectrics with unpinned Fermi Level in the alternate channel material
Control of nanostructures and properties	Ability to pattern sub 16nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.)
	Control of CNT properties, bandgap distribution and metallic fraction
	Control of stoichiometry, disorder and vacancy composition in complex metal oxides
	Control and identification of nanoscale phase segregation in spin materials
	Control of surfaces and interfaces
	Control of growth and heterointerface strain
	Control of interface properties (e.g., electromigration)
	Ability to predict nanocomposite properties based on a "rule of mixtures"
	Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability
Controlled assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components
	Control of line width of self-assembled patterning materials
	Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials
	Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.)
	Characterization of spin concentration in materials
	Characterization of vacancy concentration and its effect on the properties of complex oxides

Table ERM1 Emerging Research Materials Difficult Challenges	
Difficult Challenges ≤16 nm	*Summary of Issues*
	3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides Characterization of the electrical contacts of embedded molecule(s)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

INTRODUCTION

The materials included in the ERM include new thin film materials, low dimensional materials, macromolecules, self assembled materials, spin materials, complex metal oxides and transition metal oxides, and heterointerfaces and interfaces. These materials types could be used to solve technical issues in future devices, lithography, front end process, interconnect or assembly and package challenges. Many of these ERM material classes may be applied to solving applications in multiple areas and this is highlighted in Table ERM2. In some cases, the materials are not new, such as III-V materials, but their potential application as an alternate channel FET material would be new. The details of these applications are explained in more detail in each of the application sections.

Table ERM2 Applications of Emerging Research Materials

For the ERM to be successfully improved in research and prepared for applications, the environmental safety and health properties of the materials must be understood and available, and metrology and modeling are needed to improve and assess the ERM for the applications. Metrology is needed to characterize the structure and composition at the nanometer scale, and important physical properties whether exposed or embedded in a structure. Modeling is needed of synthesis to determine whether desired structures can be achieved and the properties of these structures modeled to determine how they will function in the application. The requirements for these are explained in more detail in their respective sections.

EMERGING RESEARCH DEVICE MATERIALS

EMERGING LOGIC MATERIALS

Emerging logic materials include alternate channel materials to extend CMOS to the end of the roadmap, materials to support charge based non-conventional FETs, and materials to support non-FET, non-charge-based Beyond CMOS devices. In some cases, materials and processes will be useful for multiple device types, so they will be discussed in detail for one application and differences highlighted for the other applications.

ALTERNATE CHANNEL MATERIALS FOR EXTENDING CMOS

The replacement of silicon channels by other semiconductors, such as III-V, Ge, graphene, carbon nanotubes, and semiconductor nanowires offers the possibility of reduced power consumption and enhanced performance for MOSFETs in future technologies. These benefits come from the higher field effect mobility of other semiconductors such as Ge for p-channels and III-V's for n-channels, graphene, carbon nanotubes, or nanowires. These carrier-transport enhanced channels can provide both higher on-currents, I_{on}, and lower gate capacitance at constant I_{on}. This combination can result in higher MOSFET performance at reduced power. To achieve complimentary MOS high performance, co-integration of different materials (i.e. III-V and Ge) on silicon may be necessary. Significant materials issues must be addressed before such improvements can be achieved.

These issues include the heteroepitaxial deposition of high crystalline quality p and n channel materials on silicon substrates, the deposition of high-k dielectrics with unpinned Fermi level with good interface properties after integration,

ability to control dopants in channel and source drain regions and electrically activate them without degrading other devices, source/drain formation with low resistance and low leakage current, gate electrodes with matched work functions, and low contact resistances for the source/drain and gate.

Graphene is another potential channel material, though at a much earlier stage in evaluation as a replacement for CMOS than Ge or III-V materials. Graphene is a zero bandgap semiconductor that transports charge through massless Dirac fermions and that offers the possibility of reduced power consumption (via lower supply voltages) and enhanced performance through increased carrier velocities. Graphene is ambipolar, however, and could serve as both n-channel and p-channel material. In fact, charge carriers have been observed to "puddle" in graphene layers at zero field so that both n- and p-carriers can co-exist in the same layers. Many significant issues for graphene remain, including: processes capable of depositing on a CMOS compatible substrate, ability to deposit atomically uniform thicknesses of films, pattern and etch with low edge defect, development of basic fabrication techniques such as doping, contacts, etc., and integration with CMOS-compatible processes. For device applications, the bandgap of graphene must be generated and controlled independently through either shape modification or applied electric fields.

The low dimensional materials for equivalent scaling include Si, Ge, and III-V nanowires, and carbon nanotubes. These nanostructured materials share common challenges; the ability to deposit in controlled locations and directions with CMOS compatible catalyst. On the other hand, the carbon nanotubes have a much larger high field-effect carrier mobility than the nanowires, but control of semiconductor bandgap is very challenging. The potential advantages and challenges of these nanostructured semiconductors are described in more detail in Table ERM3.

Table ERM3 Challenges for ERM in Alternate Channel Applications

Carbon based (CNT and graphene) devices have been identified as needing more focus to accelerate their potential use as alternate channel materials and for use in Beyond CMOS applications. The ERM and ERD chapters also identify when solutions are needed to overcome the difficult challenges that must be overcome for these materials to be viable in the required timeframe as is highlighted in Table ERM4.

Table ERM4 Alternate Channel Material Properties

III-V MATERIALS

FORMATION OF HIGH CRYSTALLINE QUALITY THIN III-V FILM CHANNEL MATERIALS:

There are several current approaches for growing heteroepitaxial semiconductor layers on silicon:

1. Direct growth of Ge and III-V heteroepitaxial layers by CVD on silicon
2. Ge (CVD) on insulator (GeOI)
3. III-V growth on GeOI on silicon[1]
4. Aspect ratio seeding for III-V growth on silicon[2,3]
5. III-V growth on GaAs/GeOI[1]
6. Ge condensation by the selective oxidation of SiGe heteroepitaxial layers[4]

There are many issues and challenges in growing III-V materials on silicon with controllable defect and strain levels and acceptable mobilities after integration with silicon substrates. *Defects* are a major problem due to the generation of misfit dislocations from lattice parameter differences and have been reduced significantly in active regions by the use of selective growth in high aspect ratio trenches in and subsequent lateral overgrowth on oxidized silicon.[3] The lowest achievable defect density has not yet been determined. Other defects that must be controlled are growth twins and III-V antiphase domains although the lowest levels needed for minimum impact on carrier transport are not known. *Elastic strain* in the deposited layers may be potentially useful for enhanced carrier transport just as it is in strained silicon but may also inadvertently degrade the mobility due to defect generation, and some are investigating using strain to split the hole bands and achieve a higher hole mobility. Thermal strains due to differential expansion and contraction and strains from lattice mismatch can occur.[4] Multigate structures make such stress control very complex. Also III-V films generally will not support the stress levels needed for enhanced carrier transport due to the lower yield stresses.[5] *Crystalline*

orientation is another variable that can be controlled for both best epitaxial film quality and for lowest effective mass and density of states along the current flow direction. The effective mass perpendicular to the film-substrate interface should be maximized to reduce the inversion layer thickness and increase the inversion capacitance so that I_{on} is increased.[4] *Heterostructure design* is another parameter that can be adjusted. For example InGaAs/InAs/InGaAs heterostructures are used to provide a buffer layer that reduces the adverse effects of interfaces on the active InAs channel.[6] Also III-V channel surfaces need to be capped to reduce their chemical reactivity during subsequent processing, although at the expense of reducing coupling with the gate. Carrier scattering mechanisms such as Coulomb and phonon scattering need more careful study as dimensions are reduced for these heterostructures. Lastly, *process control* challenges exist for the growth of uniform and controlled thickness of heteroepitaxial structures on 300mm or 450mm wafers, particularly for complex processes such as lateral overgrowth and Ge condensation. The tradeoff between channel thickness and carrier injection velocity will need to be determined.

DEPOSITION OF HIGH-K DIELECTRICS ON III-V'S:

The current approaches for dielectric deposition on III-V's include:

1. Molecular beam deposition of Ga_2O_3/GdGaO/Si_3N_4[7]
2. As cap/in-situ As decap + ALD HfO_2[8]
3. HfO_2 deposition on NH_4S-passivated GaAs by ALD[9]
4. NH_4OH clean before ALD Al_2O_3[10] or HfO_2
5. InAlAs barrier[11]
6. Amorphous Si interfacial layer + PLD/MBD of high-k dielectric[12]
7. *In-situ* clean in III-V MOCVD + high-κ ALD[13]

The issues and challenges for dielectrics on III-V channels are due to the problem of chemical and electronic control of the resulting interface. III-V surface passivations and interface layers have been developed to manage the interface properties. Passivations such as wet NH_4S, NH_4OH, nitrides (of Ga, In, or Al),[14] and atomic H have been successful in controlling surface oxidation effects on III-Vs to achieve lower Dit's and unpinned interfaces. Such passivations enable sample transfers between process chambers. Interface layers such as a-As, a-Si/SiO_2, Ga_2O_3/Gd_2O_3, and ALD Al_2O_3 have been used to provide a suitable surface for the high-k deposition. Different high-k dielectrics may be needed for different semiconductor surfaces in order to prevent Fermi-level pinning in specific materials systems and modeling of interface stability should be explored.[15] This unpinning depends on surface reconstruction differences among the various III-V semiconductor surfaces.[16] Characterization methods to measure interface bonding (such as XPS), interface state density, fixed charge density, and surface inversion are needed. Furthermore, dielectric reliability issues will need to be addressed.

GE EPI MATERIALS AND HIGH K

Several current manufacturing technologies include the growth of SiGe for strained silicon and other devices, so growth of pure Ge is not expected to be a major challenge, but may include a SiGe graded layer. On the other hand, the deposition of a high κ gate dielectric with a passivated interface may be more challenging.

The current approaches for dielectric deposition on Ge include:

1. GeOxNy nitridation[17]
2. ALD high-κ dielectric (HfO_2) on ozone-oxidized Ge[18]
3. LaGeOx-ZrO_2 high-κ[19]
4. Si cap on Ge to serve as an interface for high-κ dielectric deposition[20]

The issues and challenges for dielectrics on Ge channels are mainly due to the unwanted formation of GeOx before or during the high-k dielectric deposition. Methods for eliminating or reducing this effect include ozone pre-treatment, Si caps, or the use of oxidation barriers such as GeN or AlN. More needs to be learned about the interface states that pin the Fermi level by using techniques such as scanning tunneling microscopy and spectroscopy as well as by density functional theoretical analyses.[21]

CO-INTEGRATION OF III-V AND GE

The integration of either III-V compounds or Ge with CMOS devices will be challenging, but if both are integrated on CMOS the challenges will be even more complex. These challenges include dopant incorporation and activation, and source/ drain formation with low resistance contacts.

Dopant Incorporation and Activation

Incorporation and activation of dopants in III-V materials can be achieved at low temperatures, but activation of dopants in Ge requires high process temperatures for n-type dopants.[22] Recent work using metal-induced dopant activation in Ge has shown that activation may be achieved as low as 380°C.[23] Thus, if Ge and III-V devices are fabricated on the same substrate, these competing requirements may require the Ge devices to be fabricated prior to the growth of III-V materials, which may significantly increase the integration complexity.

Source/drain (S/D) formation:

Very little has been reported on the formation of sources and drains with low resistance and low leakage currents. It is possible that metal Schottky S/Ds may be useful. For III-Vs the S/D design will depend on the nature of the heterostructure channel and transport carrier physics. The extent to which S/Ds determine the carrier transport in the channel will need to be determined as the ballistic limit is approached.

Future research will need to address the problem of gate electrode and S/D contact material selection and process integration. Also work will be needed on the problem of dopant control as the number of dopant atoms is reduced at the nanoscale.

Graphene and Graphitic Materials

The primary advantage of these materials is their potentially high mobility (as seen in carbon nanotubes) and the ability to process in a planar form.

The critical issues for graphene include the ability to:

1. Deposit graphene over large areas with controlled thickness, registration, and orientation
2. Generate and control a bandgap in graphene
3. Reduce or control surface and interface effects on charge transport
4. Achieve a high mobility on a silicon compatible substrate
5. Deposit a high κ gate dielectric with a high quality passivated interface
6. Form reproducible low resistance contacts to graphene (contacting without etching through a monolayer film)
7. Integration, doping and compatibility with CMOS

As is identified in the ERD chapter, graphene should receive additional focus to accelerate progress for potential application as an alternate channel material and then for extension to Beyond CMOS applications. A timeline for potential solutions in shown in *Table ERD8* which assumes the graphene would be needed for application in technologies in 2019-2020.

Graphene Deposition

The preferred approach for deposition of graphene would be a CVD "like" process or epitaxial process on a silicon wafer; however other techniques could be used. Currently studied graphene deposition techniques include mechanical, chemical oxidation, or solvent exfoliation from highly oriented pyrolytic graphite (HOPG), direct CVD epitaxy on single crystal metal substrates, and sublimation of silicon from SiC. Emerging methods such as growth on polyethylene terephtalhate (PET) or polydimethylsiloxane (PDMS) which provide moreover underlying substrates that can be twisted or stretched (up to 11% without any conductivity loss) are also worth investigating. Obviously, physicochemical characterization of the graphene layers should be developed to determine thickness control and chemical purity of the layers. For graphene to be a viable technology, as CMOS compatible, potentially high volume deposition technique needs to emerge from research before 2012 as shown in Table ERD8.

Formation of high crystalline quality graphene materials:

Mechanical exfoliation of graphene has produced high quality films on silicon,[24] but control of location and thickness may not be adequate for development of integrated circuit technologies. The decomposition of SiC[25] has the advantage that the graphene is grown on a silicon-like substrate, but it requires process temperatures approaching 1200C and the reported mobility has been low.

Initial progress was made in growing CVD graphene on single crystal Ni[26], Ir[27, 28], and Pt[28], but this would be very costly. Recently small areas of graphene has been grown by CVD on a polycrystalline Ni thin films[29], and patterned polycrystalline Ni films[30], but most recently large areas of graphene have been grown with CVD on Cu foil[31] with room temperature electron mobilities of over $4000 cm^2 V^{-1} sec^{-1}$. While these graphene films are deposited on metals, transfer of

these films has been demonstrated to SiO2/Si substrates where device structures have been fabricated and properties characterized.[29, 31] While these CVD techniques are not directly on a silicon compatible substrate, the use of polycrystalline substrates with thin film transfer may offer a more cost effective approach. This appears to be a fast developing area, so new work may quickly surpass these results.

An alternative approach for selectively growing graphene on desirable substrates is through the evaporation of silicon from silicon carbide.[25] This technique requires annealing the SiC in H2 ambient at 1200°C to effectively evaporate the silicon. Thicness control of several monolayers on a mm scale has been demonstrated, with field mobilities in excess of of 25000 cm^2/V-s.[32] Recently, a technique has been demonstrated to deposit a thin layer of SiC on a silicon wafer and then "evaporate" the silicon leaving a thin layer of graphene several atomic layers thick.[33] One of the drawbacks of these approaches, however, is that the required high temperature processing may produce defects in 300mm or 450mm wafers.

Mechanical exfoliation of graphene from HOPG has produced the highest mobility graphene reported to date. While mechanical exfoliation lacks precision in placement onto a substrate, other techniques such as Graphene Oxide (GO) and solvent exfoliation are being explored to improve control of graphene thickness and potentially enable controlled deposition. Graphene oxide is synthesized by functionalizing the edges of the graphite with C-OH –COOH groups and interlayer with epoxy C-O-C and hydroxyl groups.[34] After oxidation, graphene is separated by immersion in a solvent, deposited on a surface and converted to graphene with hydrazine or hydrogen plasma. Graphene formed from GO is found to consist primarily of monolayer graphene with mobility between 10 and 1000 cm^2/V-s. Conduction was found to be dominated by hopping transport through regions of highly ordered graphene surrounded by disordered graphene.[35] Maximum graphene flakes achieved to date are in the size range of 10μm to 100μm. Hydrazine has also been used to form GO and transfer graphene to SiO_2.[36] Furthermore novel printing techniques have been demonstrated to selectively stack layers of graphene on top of each other.[37] Critical future work is to reduce the defective regions in the graphene by reducing the damage inherent the oxidation process. Graphene can be exfoliated in solvents from HOPG[38] with ultrasound, but solvent choices are limited because of solvent surface energy requirements. The high boiling point of the solvents makes deposition onto a substrate difficult and allows graphene to reagglomerate when dried on a substrate. Dispersion of graphene can also be accomplished with surfactants in water.[39]

MOBILITY OF GRAPHENE

The highest mobility of free-standing graphene (7×10^4 cm^2/V-s.) has been achieved at room temperature by controlling the surface chemistry of the membranes and by using dielectric screening with solvent dielectrics having a dielectric constant of 47.[40] Without the dielectric screening, values of $2–3 \times 10^3$ cm^2/V-s have been achieved on free-standing membranes. For graphene attached to surfaces, the mobilities are generally in the 10^2 to 10^3 cm^2/V-s range; however mobilities as high as 8000 cm^2/V-s.[41] have been reported for FETs, and contact resistance effects must be extracted[41] to get the true mobility.

GENERATION OF A GRAPHENE BANDGAP

Graphene has a zero bandgap and the two techniques for generating the bandgap are to 1) pattern the graphene into nanoribbons or 2) apply a back gate bias to a bi-layer of graphene to open the bandgap. Electrically tunable bandgaps have been fabricated using dual gate structures and different dielectrics for each gate so that the bandgap and carrier concentrations can be independently varied by different top gate and bottom gate biasing.[42, 43] With graphene nanoribbons, the bandgap increases to above 100mV at widths of 15nm and increases with decreasing width; however, the electronic properties become more sensitive to the edge states, so passivation of edge states will be critical. Applying a back gate bias effectively separates the conduction and valence bands and enables an on-off ratio of 5-10X.[43] Another option is to design the structure with a built in field due to work function differences or fixed charges in the structure. A viable technique to control bandgap needs to emerge from research before 2014, as shown in *Table ERD8*.

HIGH K GATE DIELECTRIC DEPOSITION

Since the graphene surface is chemically unreactive high κ dielectric deposition is normally initiated at edges or defects in the film. This has been demonstrated with the deposition of HfO_2 and Al_2O_3 on graphene.[44] Recently, deposition of a thin Al layer that was oxidized served as a nucleation layer for ALD Al_2O_3 on graphene which resulted in mobility above 6000 cm^2/V-s at room temperature[45], improving over previously obtained results by surface functionalization of graphene.

Processing of 2D transistors has so far being performed on small samples of graphene layers, and using sophisticated tools such as e-beam lithography. IBM Research has recently achieved a frequency of 26 GHz for graphene transistors with a gate length of 150 nm making it the highest frequency obtained for graphene so far.[46] The availability of large graphene layers on silicon substrates will then allow the use of high k dielectrics developed using either in ALD or MOCVD, the use of standard passivation layers and metal contacts of the silicon technology. This will allow a direct

benchmark with current materials using the same mask-set. A viable high κ dielectric deposition technique needs to emerge from research before 2012, as shown in Table ERD8.

DOPANT INCORPORATION AND ACTIVATION:

If graphene is to be used for extreme CMOS applications, processing must be capable of doping the material p-type and n-type for the channel region and either metallic or n-type or p-type for the S/D region. To date, the proposed approaches for doping the channel regions are to 1) deposit the graphene on a surface that injects carriers into the graphene layer and 2) chemically bonding dopants at edge states of a graphene nanoribbon. Modeling has predicted that graphene could be controllably doped by charge transfer from a substrate layer or materials deposited onto the surface, and a number of experiments have demonstrated that n-type and p-type graphene can be fabricated through deposition of metals with different work functions. More recently, graphene nanoribbon edge states have been doped n-type through high temperature electrochemical ammonia treatment.[47] Experiments have demonstrated that n-type graphene can be produced through deposition of NH_3 and CH_4[48], while p-type graphene can be produced through deposition of H_2O and NO_2.[49] Experiments on graphene ribbons indicate that edges can convert to p-type, while the center of the ribbon is n-type.[50]

The challenge with these doping techniques will be to maintain the carrier doping in an integrated structure with interconnects. Since the S/D doping will be affected by the contact metallurgy, as will be covered in the contact formation section below. A viable technique to control doping and carrier concentration in graphene needs to emerge from research before 2012, as shown in Table ERD8.

CONTACT FORMATION

The source-drain contacts need to provide a low resistance electrical contact to the graphene, but also maintain the graphene in the conductivity type that is needed for the n-channel or p-channel device. Similar to using charge transfer to generate doping, modeling has proposed the use of weak bonding contact metals to generate n-type contacts at work functions greater than 5.4eV.[51] Experiments have demonstrated that n-type graphene can be produced through deposition of NH_3, while p-type graphene can be produced through deposition of H_2O or NO_2. Ohmic contact formation may be easier than in small diameter carbon nanotubes, but more research is needed. A viable graphene contact formation technique needs be demonstrated in research before 2012, as shown in Table ERD8.

NANOWIRES

Metal-catalyzed nanowires have been suggested as the channels of MOSFETs. Si nanowires have been examined most extensively, with additional demonstration of Ge and compound semiconductors.[52, 53] The potential advantages of nanowires are 1) compatibility with gate-all-around structure that improves electrostatic control, 2) the smooth surfaces that can be achieved by this "self-assembled" or "bottom-up" approach should reduce diffuse surface scattering that limits mobility, and 3) nonclassical physics at small dimensions. Furthermore, with nanowires it is possible to fabricate defect free lattice mismatched heterojunctions in the growth direction[54] and low defect density heterojunctions in the lateral direction[55], which could enable flexibility in device design. On the other hand, there are significant challenges to realizing these advantages integrated into CMOS including identifying catalyst materials compatible with CMOS, control of placement, direction, and doping. These are described in more detail in *Table ERM3*.

Non-classical quantum effects depend significantly on the Bohr radius and this varies widely between materials. The Bohr radius in Si is short, so non-classical quantum effects (e.g., bandgap changes) are not expected for Si nanowires of currently practical (>~ 8 nm) diameters. The mobility in nanowires of selected compound semiconductor field-effect transistors can be much higher than that in corresponding Si nanowires, making nanowires of these alternative materials attractive. In addition, selected compound semiconductors, as well as Ge, have larger Bohr radii, so non-classical effects are more likely to be observed in nanowires of practical dimensions. The introduction of heterojunctions in FET structures may also be employed to improve device functionality.[56]

Although nanowires have potential advantages as the channels of field-effect transistors, significant challenges must be overcome for them to be integrated in high density applications. Nanowires can be positioned between two electrodes in a number of different ways.[57] They can be attracted from a suspension to a given pair of electrodes by a nonuniform electric field (dielectrophoresis)[58, 59] or grown in place using pre-formed electrodes[60], catalyst, and growth surfaces[60], or fabricated in vertical FET structures[61]. Due to the difficulty of placing grown nanowires, it may be more practical to define and pattern nanowires by more conventional lithography and modify their shape by nonconventional processing.[62] Incorporation of dopants may be difficult; dopants may be integrated in the deposition process[63], but due to kinetics may require high temperature diffusion processes though the nanowire sidewall. Processing of dense arrays of laterally placed nanowires with surround gates and low resistance contacts may be challenging.

CARBON NANOTUBES

The primary potential advantage for carbon nanotubes is their very high carrier mobility[64], but very difficult challenges must be overcome for them to be practical. Key challenges for carbon nanotubes to be viable in high performance FETs is the requirement for processes that provide a tight distribution of semiconductor bandgaps, with each nanotube placed in a desired location, with a specified direction, low contact resistance, and catalyst compatible with CMOS. The advantages and challenges are highlighted in more detail in Table ERM3. *Please refer to the 2009 ITRS ERD chapter for detail on these devices*.

NANOTUBE BANDGAP CONTROL

Carbon nanotube FET-related applications are motivated by their high mobility and ballistic transport.[64] For SWCNTs to be viable for future CMOS applications, the ability to grow them with a tight bandgap distribution must be demonstrated. To achieve *in situ* bandgap distribution control, the diameter and chirality must be controlled in the growth process. Little progress has been reported in the past two years with the best results being (~90%) of semiconducting CNTs by plasma CVD[65, 66] and wet processing such as dielectrophoresis,[67] selective precipitation,[68] ion exchange chromatography,[69] compaction/centrifuging[70, 71] achieving purities of 99%, and DNA purification approaching 99%.[72] These levels of bandgap distribution control are far short of the projected requirements (better than parts per trillion). Considerable research is needed to develop understanding that will enable design of catalysts and processes for *in situ* growth of CNTs with sufficiently controlled bandgap distributions. A viable technique to control bandgap of carbon nanotubes needs to emerge from research before 2014, as shown in *Table ERD8*.

CONTROL OF POSITION AND DIRECTION

For CNTs to be used for devices, they must be grown in precise locations and aligned in required directions. Progress has been made in the past two years in growing nanotubes in desired locations with catalyst patterned on quartz or sapphire to grow ~10 aligned CNTs per micron.[73, 74] While this is less than the required density, this alignment is significantly better than achieved by other techniques. Other approaches discussed in the 2007 ITRS chapter have not made significant progress in growing CNTs in desired locations and directions. A potentially manufacturable process to control nanotube position and direction must be demonstrated in research before 2012 for this to be a viable technology as shown in Table ERD8.

CONTROL OF CARRIER CONCENTRATION (NANOTUBE "DOPING")

A critical device challenge is carrier concentration control in embedded p-type and n-type materials. Typically, semiconducting CNTs tend to be p-type after growth. Doping the CNTs with potassium (K) to convert them from p-type to n-type[75] is becoming more commonly used in the fabrication of FETs.[74] CMOS compatible techniques to control carrier concentration in channel and source/drain regions need to be demonstrated in research before 2012, as shown in Table ERD8.

GATE DIELECTRIC INTERFACE

Although most CNT-FETs have been fabricated with a back gate electrode[76], top gate structures have been fabricated with ALD HfO_2.[77, 78]. Since a CNT's sidewall is relatively inert, the surface may be chemically functionalized to improve dielectric adhesion. The behavior and operational stability of the CNTs can be influenced by functionalization and by the nature of the local passivation film environment. CNT-FETs that use SiN as the passivation layer appear to exhibit very low I-V curve hysteresis.[79] Research and guiding material design principles are needed for enhancing functionalization, interface passivation, and dielectric deposition. A viable technique to deposit a passivated high κ gate dielectric needs to emerge from research before 2012, as shown in Table ERD8.

NANOTUBE ELECTRICAL CONTACTS

Pd is the most commonly used contact material with resistance approaching the quantum contact resistance[80], and recently Sc-CNT contacts[81] have been employed to fabricate n-FETs. On the other hand, researchers have also reported high variability in contact resistance for small diameter nanotubes. Characterization of interface potential of Pd to small diameter nanotubes indicates the formation of a Schottky barrier that varies inversely proportional to the nanotube diameter.[82] Recent modeling of Sc-CNT contacts (Sc work function ~3.3eV) predicts a barrier height of only 0.08eV vs. 0.34eV[83] with Pd contacts on single walled CNTs with chirality of (8,0) and predicts an ohmic contact, but this must be verified on small diameter CNTs. A CMOS compatible, reproducible contact formation technique needs to emerge from research before 2012, as shown in Table ERD8.

ALTERNATE CHANNEL MATERIALS CRITICAL ASSESSMENT

The ERM and ERD have performed critical assessments of some of the same devices. The ERD assessment assumes that all of the integration and fabrication issues are resolved, while the ERM assesses the difficulty of resolving the materials, processing, and integration issues. This ERM survey is based on votes of whether an alternative should be better than CMOS (3), the same as CMOS (2) or worse than CMOS (1). In the ERM critical assessment, *Table ERM4*, all alternate channel materials were viewed to have potentially better mobility than silicon CMOS. Not surprisingly, from an integration perspective, all of the options were viewed less capable than CMOS (a score of 2), but the Ge alternate channel was closest (~1.8), with the III-V and nanowires tying for second (~1.6), and the carbon nanotubes and graphene having the lowest scores (~1.4). As indicated in the table, entries that exceeded an average vote of 2.0 over the categories were viewed as being "easy' to integrate into CMOS (none of the options met this criteria). Entries that exceeded an average vote of above 1.7 was viewed that it should be possible to integrate onto CMOS with significant work, and Ge, III-V, and Nanowires met this criteria. Based on the voting, carbon nanotubes and graphene had more votes indicating that multiple technical issues didn't have potential solutions demonstrated and there are highlighted in red, so significant research is required to demonstrate potential solutions. Even though Ge, III-V, and nanowire materials were viewed more favorably, each had significant issues that must be addressed. For Ge and III-V materials, the biggest concern was the ability to grow defect free material on silicon and this is fundamental to integration of these materials. For nanowires, the voting indicated the biggest concern to be the ability to form low resistance contacts to the nanowires, but this should be soluble with additional focus and research. The technical challenges for all of these materials are described in more detail in the alternate channel section.

This critical assessment is based on voting by eight ITRS participants from the ERM, ERD, FEP and PIDS technology workgroups and will be updated in the ERM in future ERM revisions.

MATERIALS FOR CHARGE BASED BEYOND CMOS

A wide variety of charge based devices are considered for beyond CMOS charge based devices. Most of the materials used in these devices are discussed in detail in other sections, so key differences and research needs are discussed here.

TUNNEL FETS,

Tunnel FETs operate with band-to-band tunneling between either n+/p+ doped regions[84] or heterojunctions.[85] The homojunction devices can utilize either silicon or higher mobility junctions such as Ge, but the doped junction must be extremely abrupt, so control of doping is critical. Heterojunction devices require having band offsets that are very abrupt, but with a low potential barrier to tunneling, so the choice of materials is crucial. Fabrication of lateral heterojunctions[85] with low defects may be difficult, but fabrication of surround gate vertical nanowire heterostructures may eliminate some of these issues (See Nanowire Device Materials Section).

IMPACT IONIZATION MOS (IMOS)

IMOS is a gated p-i-n structure where the gate overlaps the n+ region and intrinsic regions.[86] The gate modulates the breakdown of the n+/i junction and controls the impact ionization. Since this structure generates hot carriers, this may cause shifts in the threshold voltage as these hot carriers cause damage in the gate or buried oxide in the case of SOI. This would require either designing the device to keep hot carriers from being generated close to these oxides or developing oxides that are immune to hot carriers. These devices could be fabricated with planar Si, Ge, or III-V materials or nanowires which are described in the alternate channel materials section.

SPIN TRANSISTOR:

The spin transistor includes both "Spin FET" and "Spin MOSFET" devices. Both devices have magnetic Source/Drains with a semiconducting channel and a MOS gate. The channel of the spin FET is a material with high spin orbit coupling such as GaAs or other III-V compounds, while the channel region of the Spin MOSFET is a material with low spin orbit coupling. In both devices, the spin is injected from the ferromagnetic source, and then transported through the channel to the drain and electrons with spin aligned with the drain are passed and generate current. In the case of the Spin FET, the source and drain have the same spin alignment, the gate voltage couples to the spin through the spin-orbit coupling and changes the spin precession angle, and the drain accepts spins with the same alignment, so current is modulated. In the case of the spin MOSFET, the alignment of the drain magnetization is fixed, while that of the source can be changed, so the gate allows current to flow from the source to the drain without modulation. In these devices, the injection of spin is important and can be achieved through either a Schottky barrier or a tunnel barrier, and both of these materials are described in the (Spin Materials Section). The channel materials and gate dielectrics are described in the ERM Alternate Channel Section and the Spin Transport Materials Section while material options for the S/D are described in Ferromagnetic Materials Section. A more detailed description of these devices is found in the *ERD chapter*.

SINGLE ELECTRON TRANSISTORS

The single electron transistor must occupy a small volume for a single electron to change the "threshold voltage".[87] The critical issues for fabricating these devices are often made in low dimensional structures such as nanowires, but control of diameter is essential for minimizing device to device variability. Thus, processes are needed to produce structures with low variability in diameter and confinement length and reproducible carrier concentrations. Research is needed on catalyst that could produce nanotubes or nanowires with reproducible diameter and possibly heterojunctions to confine carriers.

NEMS SWITCH

The materials for this device are discussed in the ERM Memory Materials Section

MOLECULAR DEVICES

Materials issues for these devices and their interfaces are discussed in the Beyond CMOS Section

NEGATIVE GATE CAPACITANCE FET

The proof of concept for this device is a silicon FET with a P(VDF TrFE)/SiO_2, gate dielectric stack[88]; however results were not definitive, so further research is needed. The potential advantage the P(VDF TrFE) has over oxide ferroelectric materials is lower leakage current. Conventional ferroelectric materials are discussed in the Memory Materials Electronics Effects Section.

MATERIALS FOR NON-FET, NON-CHARGE-BASED BEYOND CMOS

The ERD in this category include "Collective Spin," "Moving Domain Wall", "Atomic Switch", and "Molecular" devices. The spin materials have application to collective spin, moving domain wall, but they are also needed for the Spin FET, Spin MOSFET in the charge based Beyond CMOS, and the STT RAM in Memory. Molecular materials and contact issues also apply to molecular memory devices. The applications of these materials in other sections will identify differences of requirements and challenges to those of the materials in this section.

SPIN MATERIALS

A number of spin based devices are being evaluated in the Emerging Research Devices Chapter for Memory and Logic applications. In these devices, electron spin orientation is employed to represent information by either using an individual spin or a collection of spins in a magnet. The operation of these devices depends on nanometer scale material properties and multiple materials will be needed to enable these devices. A few of the basic functions required for most devices are 1) Electrical signal to spin conversion, 2) spin state storage, 3) spin transport, 4) electric or magnetic field induced spin modifications, and 5) spin state to electrical signal conversion. Materials that support these functions need to operate up to ~400ºK. These functions may be performed in a single material, at an interface, or in a combination of coupled materials and will need to operate in nanometer scale structures. These spin-based materials, along with their critical properties and challenges, are listed in Table ERM5.

Table ERM5 Spin Material Properties

SPIN MATERIAL CHALLENGES

The key material challenges for the realization of a device are: (1) reproducible synthesis of semiconducting magnetic materials with higher Curie temperature, i.e., Tc > 400 K and high remnant magnetization, (2) materials or structures with high coupling of electrical potential to magnetic alignment or spin alignment, (3) compatibility of these materials with CMOS processing, and (4) metrology to characterize spin and domain physics. A more detailed list of materials challenges is listed in Table ERM5 and detailed discussion of spin metrology needs is included in the ERM Metrology Section.

SPIN MATERIAL PROPERTIES

The set of critical properties for different spintronics materials, Table ERM5, will depend on the specific device applications, as discussed in the ERD Chapter. Within the context of evaluating progress in fabricating a semiconductor based or an all metallic spin device (as in the ERD), this section focuses on materials that exhibit the following physical phenomenon: (1) Spin wave propagation and modulation for Bus and logic, (2) magnetic cellular automata for logic (3) the field effects of spin polarized electrons and holes for memory and logic. Thus, this section sequentially focuses on the following materials and their properties.

1. Dilute Magnetic Semiconductors
   - Ferromagnetic transition temperature (T_C)
   - Size dependence of T_C – Nano materials
   - Wide band gap magnetic doped oxides and nitrides
   - Group III-V and Group IV
2. Spin Injection/detection Materials
3. Spin Tunnel Barriers
4. Semiconductors and Nanostructures
5. Materials for Spin Wave Spintronics devices
6. Materials for Magnetic Cellular Automata logic

DILUTE MAGNETIC SEMICONDUCTORS

The potential value of dilute magnetic semiconductors, also known as ferromagnetic semiconductors, is that the magnetism can be turned on or off by changing the carrier concentration in the material. Several III-V compounds doped with Mn have been validated to have carrier mediated magnetic properties at low temperature and group IV Mn doped alloys have also been reported to be ferromagnetic. Wide bandgap transition metal oxides doped with Mn or Co also have been reported to exhibit magnetic properties, but carrier mediated (coupled) magnetism has yet to be validated in these materials. Since many of these materials are group III-V semiconductors doped with 3d transition metals, such as Mn and Co, it is feasible to integrate them with the current CMOS technology. Since magnetic material properties can be induced with the application of an electric field and their spin alignment can be manipulated electrically, these materials could have many applications in spin devices. However, the primary constraint in using this material, (Ga,Mn)As, is that its highest ferromagnetic transition temperature, with verified carrier mediated exchange achieved to date (Tc<190 K)[89], is still well below room temperature. Research is needed to identify alloys compatible with semiconductor technology, having Curie temperatures above 400ºK, high remnant magnetization, and carrier mediated exchange.

Since the greatest challenge is to identify DMS materials that have carrier mediated exchange to 400ºK, it is important to understand what factors control this behavior and what could be done to extend this property to higher temperatures. By far, the most studied compound is $Ga_{1-x}Mn_xAs$, usually with $0<x<8\%$. According to the theory, when a Mn atom substitutes for the Group III element in GaAs, it acts like an acceptor and induces a spin-polarized localized acceptor level composed primarily of p-orbitals in the surrounding material. Ferromagnetism occurs when the acceptor level clouds surrounding nearby Mn atoms overlap.[90] Other III-V compounds have been reported to have ferromagnetism at higher temperatures, but it has not been determined whether this can be controlled with carrier concentration. Although ferromagnetism has been reported in (Ga,Mn)N with Curie temperatures up to 940ºK (*See the Tc Table*), modeling indicates that the acceptor levels are quite localized, which suggests that robust ferromagnetism with carrier mediated exchange is unlikely in this material. One of the challenges is that magnetism in these materials can also be caused by precipitates, second-phase alloys and nanometer-scale clusters, so it is important to rule out their presence. Thus, the growth of homogeneous GaN based DMS with Curie temperature above 350 K is still in need of further study.

Group IV semiconductors (Si and Ge) doped with transition metals (e.g., Mn, Co) are reported to be ferromagnetic, with variability of Curie temperature depending on different growth conditions.[91, 92] There are conflicting reports on the origin of ferromagnetism in Group IV materials such as MnGe DMS.[93] A recent study also predicts that the Curie temperature can be increased by increasing the substitutional doping of Mn in Ge and Si, which can be achieved by co-doping - by adding conventional electronic dopants such as As or P during the Mn doping process.[94] Theory[95] and experiments indicate that the ferromagnetic transition temperature is related to the ratio of interstitial to substitutional Mn similar to that in the Group III-V system.[90] GeMn nanowires have been reported to have room temperature ferromagnetism.[96] Modeling supports these results,[97] although carrier mediated exchange has yet to be experimentally verified. As in the III-V materials, ferromagnetic properties can be caused by precipitates, second-phase alloys and nanometer-scale clusters, so it is important to rule out their contributions.

Transition metal doped oxide semiconductors have been reported to be ferromagnetic well above room temperature, but they exhibit a low remnant magnetization. It is not clear whether the magnetism can be modulated with carrier concentration, and these materials also have low carrier mobility. The current understanding of ferromagnetic (FM) ordering is far less developed than in the (III,Mn)V materials. The stronger ionic character of the wide gap oxide hosts suggests that a broad impurity band, created by the relatively high concentration of dopant atoms (~ 1-10%), enabled the

relatively long range interactions necessary to produce the FM order in dilute magnetic systems.[98] Experimental results suggest the FM order is correlated with n- or p-type character. Mn doping produced ferromagnetism in p-type (but not n-type) nanocrystals, and Co doping produced ferromagnetism in n-type (but not p-type) material.[99, 100] Other experimental work on single crystal films reported a strong dependence of the FM order on electron concentration at room temperature for Co:ZnO and Mn:ZnO[101, 102] and in $Cr:In_2O_3$.[103] Modeling supports high Curie temperatures for Co:ZnO[104] and $Cr:In_2O_3$.[105]. While carrier doping has been demonstrated to modulate magnetism in these doped oxides, the ability to modulate magnetism with an electric field has not been demonstrated. Furthermore, the low carrier mobility in these oxides may limit their use for spin transport.

In summary, III(Mn)-V materials demonstrate carrier mediated exchange only below 200K. Group IV(Ge) and transition metal doped oxide materials have low remnant magnetization (<10%) at room temperature and field controlled carrier mediated exchange has not been identified in these materials. Thus, significant material innovation and improvement is required, and the current understanding of DMS remains unsettled. Reproducibility of materials growth and the ability to control and avoid the formation of secondary phases is continuously a major challenge. Theory and numerical modeling have provided some guidance in designing the electronic structure and transport in the DMS compounds, but their results are far from predictive. Other approaches such as quasiparticle self-consistent *GW* approximations[106, 107, 108], or high-end *ab initio* Hamiltonians as benchmarks to establish parameters for empirical models[109] may need to be pursued to make the models more predictive.

SPIN INJECTION MATERIALS

The purpose of the spin injection material is to inject a highly spin polarized current into a semiconductor. This can be accomplished either through high intrinsic spin polarization, or band symmetry matching with the adjacent semiconductor and/or tunnel barrier, as discussed in "Spin Tunnel Barriers."

The material to be used for a spin injecting contact should have several key attributes.

(a) It must be ferromagnetic, with a Curie temperature of over 400ºK;
(b) It must have significant easy axis remnant, i.e., zero field magnetization, and at least 50% of the saturation magnetization;
(c) Provide high spin polarization of the injected current, producing high spin polarization in the semiconductor; and
(d) Be thermally stable against intermixing with adjacent layers, and degradation of its FM properties with processing.

Requirements (a) and (b) provide the non-volatile reprogrammable characteristics, which are highly desirable for applications such as field programmable gate arrays, logic elements, or memory. In general, the spin injection contact material needs to be selected and tailored for a particular semiconductor or tunnel barrier.

Three broad families of materials could be used for polarized spin injection, ferromagnetic metals, half metals, and ferromagnetic, but each has different challenges.

1. **Ferromagnetic metals (FMMs)—**Traditional FMMs such as Fe, Co, Ni and alloys are well-known to the magnetic recording industry and readily meet criteria (a) and (b) above. Because of the large conductivity mismatch between a FMM and a semiconductor, an intervening tunnel barrier is required to enable efficient spin injection. This may take the form of a tailored reverse-biased Schottky contact or a discrete metal oxide layer (e.g., Al_2O_3, MgO, etc.). Several FMMs have been shown to meet criteria (c) for selected semiconductors and/or tunnel barriers. For example, efficient electrical spin injection has been demonstrated for the following: (Fe.FeGa)/GaAs(001) Schottky tunnel barrier, (Fe,FeCo)/MgO/GaAs(001), (Fe,FeCo)/Al_2O_3/GaAs(001), Fe/Al_2O_3/Si(001) and Fe/ZnSe(001) Schottky barrier. Thermal stability (criterion (d)) is likely to be an issue and the thermal budget for processing needs to be studied and controlled. Other FMMs, such as transition metal pnictides (e.g., MnAs) and silicides (Fe_3Si, CoSi), have been used successfully as spin injecting contacts. For example, MnAs has be shown to have good spin injection into GaAs(001), but fails criterion (a) due to its low Curie temperature, and is marginal for criterion (d). Fe_3Si has been used as a spin injecting contact for GaAs and Si, and significant progress has been made to produce a stable interface between Fe_3Si and Si.[110] Recently, relatively high spin polarization (about 60 %) was experimentally observed in Fe_4N grown on AlN[111], Fe_3Si and Fe_4N[112] are expected to be good candidates for meeting all criteria (a) ~ (d). Other pnictides and silicides may prove useful, but have yet to be demonstrated.
2. **Half Metals**—Half metals are characterized by the absence of occupied states near the Fermi energy for one spin channel, so that they are 100% polarized, making them very attractive as spin contacts. They generally meet criteria (a) and (b). In principle, such a 100% spin polarized metal does not require a tunnel barrier contact to alleviate the conductivity mismatch with a semiconductor. However, their polarization is highly sensitive to defects (a relatively low density of bulk defects reduces their polarization very rapidly), so these materials exhibit spin polarizations ~

50%, typical of other FM metals at room temperature to 400ºK. In addition, defects associated with the semiconductor interface also appear to severely suppress the ideal spin polarization. Only modest electrical spin injection into a semiconductor (GaAs) has been reported to date[112, 113] and, thus, half metals have not yet been demonstrated to meet criterion (c). Criterion (d) will likely pose significant challenges, although a few carefully tailored systems may be viable.

3. **Ferromagnetic Semiconductors (FMS)—**FMS are materials that are simultaneously semiconducting and ferromagnetic. As semiconductors, there is no issue of conductivity mismatch, and device design follows the standard principles of semiconductor band gap engineering. They can readily be grown epitaxially on other semiconductors, and incorporated into complex heterostructures, unlike most metals. FMS generally have Curie temperatures well below room temperature (<200ºK), as noted in the section under "Ferromagnetic Semiconductors." Therefore, they fail criterion (a). There are a few notable exceptions which are currently being investigated as discussed before.

Spin Tunnel Barriers

The large difference in conductivity between a ferromagnetic (FM) metal and a semiconductor precludes efficient spin injection, since the semiconductor accepts spin-up and spin-down carriers with equal equally and very low conductivity. The resulting polarization is essentially zero regardless of the spin polarization of the FM metal. To solve this "conductivity mismatch" issue, the interface resistance must be the largest in the series to control current flow, and also provide some spin selectivity. A tunnel barrier fulfills both criteria.[114, 115]

Robust spin injection from a FM metal into a semiconductor was first demonstrated using a reverse-biased Schottky barrier formed at the Fe/AlGaAs interface.[116] The surface region of the semiconductor was heavily n-doped, so that the depletion width was exceedingly narrow to form a tunnel barrier.[117] The electron spin polarization achieved in the GaMnAs was 60-70%.[118]

The canonical tunnel barrier is a thin (~ 1 nm) metal oxide, such as Al_2O_3, which has been used routinely in metal spin dependent tunnel junctions (e.g., Fe/Al_2O_3/FeCo). This requires deposition of a thin and uniform discrete layer of well defined thickness, which is often difficult to achieve reproducibly. A nominally amorphous aluminum oxide tunnel barrier has been used to enable electrical spin injection from a FM metal into AlGaAs/GaAs, InAs, Si and graphene, resulting in significant spin polarization in the semiconductor. Other oxides may be particularly attractive for spin injection into Si, including SiO_2 and the newer high-k dielectrics, such as HfO_2. Crystalline MgO has also been used successfully as a tunnel barrier in Fe/MgO/GaAs and CoFeB/MgO/GaAs heterostructures.[119, 120]

If the tunnel barrier is crystalline, rather than amorphous, theory predicts that the band symmetry, and more specifically the orbital composition (s,p,d) of the bands in the FM metal and tunnel barrier play a significant role in determining the efficiency of the spin injection into the semiconductor.[121,122] The conduction band states of many semiconductors of interest, including Si, Ge, and III-V, the majority spin band in Fe, and the propagating state in the MgO tunnel barrier are all Δ_1.Thus, in theory, majority spin electrons could be efficiently transmitted from the Fe in to the semiconductor[123, 124, 125], with modeling predicting over 99% spin polarization of the transmitted current, in the ideal case. The relative spin polarizations achieved in (001) GaAs by electrical injection from Fe Schottky and Fe/MgO tunnel barriers is likely due to the fulfillment of these conditions, leading to a very large tunneling magneto resistance (TMR)[126].However, the observed TMR is several orders of magnitude lower than predicted. There are many other factors that also influence spin injection, such as (1) band energy alignment, (2) whether this energy occurs at the same value of the transverse momentum, (3) the Schottky barrier that forms at the interface of the metal and the semiconductor, and (4) spin dephasing that happens at the interface etc.

The temporal response of the magnetic tunnel materials, which is of great importance for switching applications, has been studied extensively. For a metal insulator metal (MIM) tunneling junction, less than 500ps was obtained using X-ray magnetic circular dichroism (XMCD), with a resolution of sub 200ps.[127] This X-ray imaging experiment on metallic spin valves reveals two distinct spin torque valve switching processes: vortex formation and spin torque alone.[128] Further smaller samples demonstrated a higher chaotic process developing into a spin torque transfer switching process, without any formation of vortices inside the sample. Modeling suggests that both mechanisms may be required to switch the magnetization.[129] If chaotic processes in the tunnel junction limit the switching speed, this could limit the speed of devices based on spin tunnel barriers.

Spin Transport in Semiconductors and their Nanostructures

For several devices, once the spin is injected into a semiconductor, it is important that the spin not loose coherence in the time that transport, manipulation, and detection occur. Most experimental work on spin transport in semiconductors typically focuses on III-V direct gap materials, such as GaAs, because polarization dependent optical absorption /

emission spectroscopies provides easy, direct and quantitative insight into carrier spin polarization and dynamics. The long spin lifetimes expected for the low-Z (weak spin orbit) Group IV semiconductors make spin angular momentum especially attractive. Spin transport, via electrical injection and detection of spin polarized carriers from FM metal contacts (e.g., Fe, CoFe) into Si, has been demonstrated[130, 131], with reported electron spin polarizations of 30% or more. Magnetic field induced coherent precession of the pure spin current and spin polarized charge current has been demonstrated in lateral and vertical transport geometries, respectively.[132, 133] These results collectively show that information can be fed in, processed and read out using spin rather than charge as the state variable. However, these results are all at low temperature, due to thermal noise generated by the contact resistance. Options to reduce this contact resistance, by controlling the depletion width in the Si, have been identified.[134]

Graphene exhibits *spin* transport characteristics that surpass those of any other semiconductor studied to date, demonstrating magnetoresistance *at room temperature.*[135] This has not been seen in any other semiconductor materials or nanostructures, including InAs to GaN to Si.

For low dimensional materials, CNTs are attractive as spin transport materials because their low dimensionality results in a suppression of certain spin orbit scattering mechanisms at higher temperatures (>70K), leading to longer spin lifetimes. Limited successes have been reported for spin injection into CNTs from magnetic metal contacts at low temperature. However, obtaining reliable contacts and reproducible results continue to be challenges. At present, for nanowires of any semiconductor, there are limited results for spin injection and transport, though several experimental groups are currently working in this area.[136]

MATERIALS FOR SPIN WAVE SPINTRONICS DEVICES

The key challenges in building a practical spin wave logic circuit are the efficient injection, detection, and modulation of spin waves in the wave guide. For this to be a viable option, efficient spin wave generators and modulators need to be integrated onto the spin wave guides, which requires an optimized interface between materials. At present, research on magnetic modulators is based on spin valves/magnetic tunnel junctions or multiferroic materials.[137, 138] This section will discuss material properties required for fabricating an efficient spin wave guide and spin wave modulator, based on multiferroics.

The fundamental physical property required for fabricating an optimized spin wave guide is to have high saturation magnetization (~10 KG), low Coercive field (tens of Oersteds), and long attenuation time (at least 0.5 ns). Currently, the most popular materials used for a spin wave bus are soft ferromagnetic metallic conducting films, such NiFe, CoFe, CoTaZr that are sputter deposited. These ferromagnetic metals possess high saturation magnetization (about 10kG) and Curie temperatures much higher than room temperature (Ni 627K, Fe 1043K, Co 1388K). Another advantage of using these materials are their compatibility with the silicon platform. Prototype spin wave devices are also fabricated using ferrite materials, such as Yttrium Iron Garnet (YIG). However, achieving nanometer thick and uniformly dense ferrite materials on silicon substrate is a challenge.

There are theoretical models demonstrating how to integrate a multiferroic structure onto a spin wave guide[138], but this integration has yet to be experimentally demonstrated. There are two major requirements for multiferroic materials: (i) Prominent magnetoelectric coupling (in V/cm Oe), and (ii) a fast switching time. Conducting and insulating materials are applicable to the spin wave based logic devices. They may be single phase multiferroics (e.g. $BiFeO_3$ 7 mV cm^{-1} Oe^{-1}) or composite (two phase) multiferroics comprising piezoelectric and ferromagnetic materials (e.g. PZT/$NiFe_2O_4$ (1,400 mV cm^{-1} Oe^{-1}), $CoFe_2O_4/BaTiO_3$ (50 mV cm^{-1} Oe^{-1}), PZT/Terfenol-D (4,800 mV cm^{-1} Oe^{-1}). Two-phase composite structures show magnetoelectric coefficients almost three orders of magnitude higher than those of single phase systems, while single-phase multiferroics switching speeds are intrinsically higher. Experimental studies have shown about 100ps (10GHz) switching times in single-phase multiferroics, and only 1 ns(1GHz) in the composite multiferroics.

The above approaches to material selection are postulated for fabricating an efficient spin wave bus or an interferometer based spin wave majority logic device.[138]

MATERIALS FOR MAGNETIC CELLULAR AUTOMATA

Magnetic cellular automata for logic is based on ferromagnetic islands arranged in cellular arrays, where local interconnectivity is provided by magnetic field interactions between neighboring magnetic dots.[139] In early work, 100nm diameter dots of 30-50nm thick islands were made of permalloy and supermalloy.[140] Since the state of one MCA is changed by the magnetic field generated by other local MCA, a critical challenge for this technology is to have reliable propagation of alignment between multiple MCAs. One option is to use magnetic materials with magnetocrystalline biaxial anisotropy. The biaxial anisotropy creates a metastable state for a rectangular nanomagnet, when it is polarized along the hard axis[141] and improves switching reliability. Material systems that exhibit such biaxial anisotropy include: epitaxial Co on single crystal Cu substrates[142], epitaxial Fe on GaAs[143], and epitaxial Co/Cu on Si.[143]

To increase the magnetic flux density in the MCA, one option is to surrounding magnets with a different material to increase absolute permeability. This effect has been demonstrated in MRAMs, where enhanced permeability dielectrics had embedded magnetic nano-particles to increase a word/bit line's field strength without increasing current.[144] Proposed materials could increase the absolute permeability range by 2-to-30. Moreover, the fact that particle sizes are below the superparamagnetic limit should help ensure that magnetic the state is not unduly influenced.

While these approaches are based on magnetic islands with in-plane magnetization, utilization of layered stacks, e.g., cobalt-platinum multi-layers with magnetization perpendicular to the plane, is possible. A recent study demonstrated single-domain magnetically-coupled islands with perpendicular magnetization, fabricated with focused-ion-beam patterning of Co-Pt multilayers.[145]

MAGNETOELECTRIC COUPLING (MULTIFERROICS)

Coupling an electric field to magnetic alignment is a critical capability in spin based memory or logic and magnetoelectric multiferroic materials may provide a potential solution. The materials of interest include ferroelectrics and magnetics (either ferro- or antiferromagnetism) with magnetoelectric coupling.[146, 147] If the electric and magnetic orders are coupled, it could be possible to exert mutual control of the electric polarization, with a magnetic field, or controlling magnetization, by an electric field. However, a critical challenge will be to reduce the operating voltage for logic operations.

$BiFeO_3$ is the only (known) compound, which is both antiferromagnetic and ferroelectric, with a high polarization to 400ºK. The crystal structure of these thin films is monoclinic, whereas it is rhombohedral in bulk. The ferroelectric polarization along the (100) direction is ~ 50-60 $\mu C/cm^2$.[148] This large value was originally thought to be due to strain enhancement. However, it was shown that high quality single crystals also exhibit similar Pr values of 60 $\mu C/cm^2$ normal to the (001) plane[149, 150], and thin films had similar Pr values.[151] The ferroelectric polarization value and its relative insensitivity to strain were predicted by *ab initio* calculations.[152] Enhanced ferromagnetism was reported in thin films[148], but its microscopic origins are still unclear and need further study. The possible role of strain and/or domain walls in enhancing the magnetic moment also needs to be further understood.

Electrical control of antiferromagnetic domains in $BiFeO_3$ has been demonstrated in single crystals[153, 154] and thin films.[155] Polarization switches of 71° or 109° changes the orientation of the easy magnetization plane. The control of antiferromagnetism by an electrical field opens up the route to the control of ferromagnetism (to read magnetic information in MRAMs for example) with an electrical field, using the exchange bias mechanism. Exchange bias between a ferromagnet, such as CoFeB[156, 157] or $Co_{0.9}Fe_{0.1}$[158] and the antiferromagnet $BiFeO_3$, has been demonstrated. The exchange bias leads to a shift of the ferromagnetic layer's hysteresis loop. The coercive field, H_c, depends on the ferroelectric domain size.[157] The demonstration of using exchange bias coupling to electrically switch the magnetization in a ferromagnetic layer (Co) has been recently reported and is a major breakthrough for the potential application of $BiFeO_3$ in spintronics.[159]

Ferromagnetism and the insulating properties of multiferroic films can be exploited to design a spin filter. By inserting a thin layer of $BiMnO_3$ or $(Bi,La)MnO_3$ between $La_{2/3}Sr_{1/3}MnO_3$ and Au electrodes, a spin efficiency of 22 or 36 % respectively were measured.[160, 161] Eventually, combining the ferromagnetic and ferroelectric characters of the insulating barrier allowed to control both magnetically and electrically the tunnel current, leading to a 4-state memory device.[162] This achievement is a major breakthrough showing the potential of multifunctionality.

Since single-phase multiferroic compounds are rather scarce, especially those operating at room temperature, other strategies are developed to design magnetoelectric multiferroics, i.e. two-phase systems. These systems involve the combination of a ferroelectric and a ferromagnetic compound, in the form of multilayers[163] or composites composed of nanopillars in a matrix.[164, 165] Each compound can be optimized for its functionality. An indirect magnetoelectric effect can arise from a strain-mediated coupling between the electrical and magnetic order parameters. When $CoFe_2O_4$ nanopillars were embedded in a ferroelectric $BiFeO_3$ matrix, an electrically-induced magnetization reversal was reported.[165]

INTERFACES AND HETEROINTERFACES

All of the devices fabricated with these materials depend on having high quality interfaces, and the important properties depend on the application. For spin tunnel barriers, the interface must not scatter the majority spin carriers. For spin transport, the interfaces must have spin specular reflections that don't cause decoherence.

MOLECULAR DEVICE MATERIALS

Significant challenges for molecular state electronics include: Fabrication of low potential barrier electrical contacts, reliable operation, the high resistance of molecules in their "on" state, and deposition of the top contacts that don't change molecular properties. Molecular state devices are reported to exhibit a range of useful properties, including non-linear IV and bi-stable behavior, but the electrical performance of many molecular-based devices currently under study appear to be dominated by the high potential barriers of each molecule-electrode contact or defect-like processes. Results suggest that changes in molecule-contact conformations or near neighbor interactions may be responsible for observations of electrical switching.[166, 167] On the other hand, a serious challenge is presented by the high resistivity of molecular devices. For instance, short 1D conjugated molecules, ~2nm in length like BPDN-DT, typically exhibit a few GOhm resistance in their "off" state and a few hundred MOhm resistance in their "on" state[168] With a ~1-2 nm footprint, this resistance would result in ~1GW/m^2 power dissipation, which is unacceptable. The resolution may come by way of using molecules as part of superconducting electronics. Thus, superconductivity may be induced even in highly resistive non-conjugated DNA strands[169] Another striking example is the superconducting nanobridge fabricated with a 2 nm gap with a trapped Gd:C82 dimer.[170] There, the proximity effect induced superconductivity in the dimer, and transport was sensitive to the spin state of Gd ions. This is an example of a molecular spintronic switch[170] Despite significant challenges and knowledge gaps, these emerging molecular systems show some promise for reducing device variability and enabling very high density circuit functionality.

MOLECULAR STATE CONTACTS AND CONTACT MATERIAL

Fabricating reliable molecular-scale devices requires identifying molecule/substrate contacts and top contact materials and deposition processes that produce high quality electrical contacts. Parameters ranging from the bond dipole to molecular orientation affect charge-transport parameters and switching voltages. Research is needed to elucidate the structural and electronic properties of molecule/substrate and top contacts, in order to engineer these contacts with reliable performance characteristics.

Previous and ongoing work has focused on the alignment of the low lying molecular states, relative to the contact material Fermi level, and modifying the work function of the substrate material. Most molecular systems contain low lying π-states that reduce the barrier height. Although factors such as molecular structure, molecular conjugation, and substitution have been studied, strategies for controlling their influence on charge transport are in their early phase of research. Most studies have focused on nanoscale bottom contacts, fabricated on gold with a thiol (sulfur) bond, but it is not optimal for achieving optimal electrical contact behavior. Recent studies have shown that changing the molecular contact has the biggest effect on the alignment of the low lying valence states. New molecule-contact material systems, such as isocyanides, cyanides, dithiocarbamates, dithiols, alcohols, and others, are needed on metal and semiconductor contact materials that enable stable, reproducible low potential barrier contacts.

The alignment of low lying molecular states has shown to be influenced by the contact material work function. Additional molecular modeling, synthetic, and experimental work, exploring the dependence of the metal work function on new molecular contacts, is needed.

ATOMIC SWITCH MATERIALS

The atomic switch operates with oxidation /reduction processes where a metal atom moves to form a bridge between two different electrodes. The materials include a metal such as Cu and sulfur.[171] Research is needed to determine the mechanism and determine its potential reliability; however, the mechanisms appear to be similar to those in the nanoionic memory.

EMERGING MEMORY MATERIALS

Emerging Research Memory Devices includes capacitive memories (FE FET, FeRAM), and resistive memories including nanoelectromechanical, spin transfer torque MRAM, macromolecular and molecular memories, electronic effects, nanothermal, and nanoionic memories. The ERM used in these devices includes, carbon nanotubes, nanowires, complex metal oxides, transition metal oxides, magnetic materials as well as engineered interfaces between these materials. The potential advantages and challenges of ERM for Memory Devices are summarized in Table ERM6. Since many of these devices use complex and transition metal oxides, a section will review challenges for these materials.

Table ERM6 ERM Memory Material Challenges

FE FET

FeFET operates with two stable polarization states available in the ferroelectric film used as a gate oxide. The main issues in FeFETs for non volatile memories are the short retention time and charge traps at the Si-ferroelectric interface.[172] Insertion of a dielectric layer such as HfO_2 or Hf-Al-O between silicon and the ferroelectric has strongly improved the retention time. The material requirements for FeFETs are different from those used in conventional FRAMs. Ferroelectrics with a lower P_r are optimal, which is why $YMnO_3$ (P_r ~5.5 μC/cm^2) has been considered for such applications. However, recently promising results have been achieved with a Pt/$SrBi_2Ta_2O_9$/Hf-Al-O/Si structure.[173]

NANOELECTROMECHANICAL MEMORY

As mentioned in the ERD, the carbon nanotubes and other nanostructured materials are being investigated for nanoelectromechanical memories. Suspended or free-end structures are caused to physically move, contacting and decontacting to bridge an electrical gap under the influence of an applied field. A number of challenges must be overcome for this to be viable including being able to fabricate these devices with a high density and optimize the design so the cantilever doesn't get stuck in one state. First of all, these devices are large and scaling to smaller dimensions increases the voltage required for switching. The switching times of these devices are 10-100 nsec., which may be difficult to reduce due to scaling challenges.

SPIN TORQUE TRANSFER MRAM

This memory employs switchable giant magnetoresistive material stack composed of a ferromagnetic material that has a fixed alignment (pinned due to exchange bias coupling with an anti ferromagnetic layer), a spin selective tunnel barrier, and a free switchable ferromagnetic material. The properties of these materials are described in the beyond CMOS device materials section. These devices use ferromagnetic metals (See Ferromagnetic Metals), antiferromagnetic pinning layers(See Multiferroic Magnetoelectric Materials), and tunnel barriers (See Tunnel Barriers). The spin selective tunnel current provides magnetic switching in the forward bias, while reflected spin provides counter-switching under reverse bias. Difficulties in implementation of this technology are coupled to the difficulty in obtaining significant spin torque for switching under reasonable operating currents.

MACROMOLECULAR MEMORIES

Macromolecular memories consist of a polymer, containing embedded conductive components, sandwiched between two electrodes. As described in the ERD Memory Section, the conductive components could be metallic thin films, metal nanoparticles, C60, organometallic macromolecules or other nanomaterials. Critical challenges are to determine the mechanism for the charge storage operation and determine the reliability and scalability of this mechanism.

MOLECULAR MEMORIES

See the Beyond CMOS Molecular Devices Section

ELECTRONIC EFFECTS MEMORY

These memories include charge trapping, Mott transition, and Ferroelectric barrier effects devices and all of these utilize complex metal oxides or transition metal oxides.

CHARGE TRAPPING

As mentioned in the ERD chapter, carriers are injected through Fowler Nordheim tunneling into either defect states or conductive nanoparticles in a dielectric, which changes the tunneling resistance of the dielectric. The key challenge for this type of memory is the reliability of the switching mechanism, due to generation of electrical defects with carrier transport. Depending on the oxide used, anion and cation vacancies can be generated and migrated with applied fields.

MOTT TRANSITION

As mentioned in the Emerging Research Devices Memory Section, the Mott Transition (a metal-insulator transition driven by a gate induced change in carrier concentration) has been reported in a number of transition metal oxides and complex metal oxides. While this transition is proposed to be electronically driven by strongly correlated electron effects, several of these materials (e.g., VO2[174]) or NSMO[175] also undergo a first order structural phase transition. If the first order phase structural phase transition is required for this switching process, the material may need to be cooled below the transition temperature to restore the insulating state. Also, control of temperature for this device could be crucial to maintain the material close to the phase transition temperature.

A metal insulator transition has been reported in a number of heterointerfaces between complex metal oxides that have an electronically switchable 2D electron gas.[176] On the other hand, the role of oxygen vacancies at these interfaces is not fully understood and their field driven migration could complicate the operation of the structures. It is critical that the role of oxygen vacancies in these structures be understood and controlled.

FERROELECTRIC POLARIZATION[88]

As highlighted in the ERD, ferroelectric polarization can modify the tunneling properties of ultrathin insulating layers or modify the Schottky type space charge region in an adjacent semiconductor, which could change the apparent tunneling current of a device. This tunneling barrier resistance has been demonstrated with a probe memory on BaTiO3/La0.67Sr0.33MnO3 thin film single crystal stack on a NdGaO3 substrate.[177] Critical challenges for these structures will be to establish stable and reliable interfaces between the ferroelectric and the tunnel dielectric or the semiconductor substrate, as tunneling induced vacancies can change the conductivity of the material or accumulate at the interfaces. Another key concern is whether these devices necessitate the use of high-quality, single crystal ferroelectrics, or can they be reliably fabricated from amorphous or polycrystalline materials.

NANOTHERMAL MEMORY MATERIALS

Nanothermal includes chalcogenide nanowires and oxide based thermal phase change memories although the mechanisms are very different.

CHALCOGENIDE NANOTHERMAL

Chalcogenide thin film memories are covered in the PIDS chapter. These nanothermal devices use nanowires, which allows integration of a diode and the increases the thermal resistance of the chalcogenide structure. It allows lower power operation. The nanowires undergo a crystalline (low resistance) to amorphous (high resistance) change with current induced heating. This phase change is expected to be more controllable, due to the higher thermal resistance of the nanowire vs. a thin film and the limited number of phonon states in the nanowire.[178]

OXIDE THERMAL

In the case of the oxide based thermal phase change memory, conducting nanofilaments are formed with application of an electric field to induce a low resistance state. Conversely, a high current can be applied to heat the filament and return it to the high resistance state. Multiple mechanisms are proposed for this phenomenon including cation and anion migration, so it will be important to determine the reliability of the correct and/or dominant mechanism.[179] Counter-ions and oxygen vacancies may play a critical role in the operation of these oxides, so these behaviors needs to be better characterized.

NANOIONIC MEMORY

In the case of filamentary conduction systems,[180] when oxides and sulfides are doped with a metal, such as copper and an electric field is applied, single or multiple random conductive filaments can form within the oxide between electrodes. These conducting filaments may be broken by reversing the bias or re-formed by reapplying the programming bias. It is desirable to make the oxide defect-free to eliminate alternate conduction paths that can increase OFF state leakage. Oxygen electro-migration in these materials may produce device reliability issues, because it produces time dependant changes in oxide resistance that vary with electric field and current density.[181] Further, the dopant/dielectric combination must be chosen to increase cation mobility, which impacts switching speed. An added materials challenge is that lateral diffusion barriers may be required to keep cations in place within the memory cell. In all of these cases, it is crucial to maintain control of oxygen vacancies and stoichiometry.

COMPLEX METAL OXIDE MATERIAL CHALLENGES

Emerging complex metal oxide based memory and logic device concepts exploit the novel properties of these materials, including: dielectric constant, resistance change, ferroelectric, magnetic and coupled of electric and magnetic properties. For all applications, it is important to understand the role of vacancies in operation and reliability, so further research is needed to develop this fundamental understanding. Furthermore, interfaces and heterointerfaces of these complex metal oxides can modulate properties of these structures, so by developing fundamental understanding of these interfaces may enable development of new coupling of properties. A critical need is for material systems with highly coupled electric and magnetic properties (magnetoelectric) to temperatures of 400K, for application in memory or logic devices.

The first challenge for these materials is to understand the role of defects and disorder on their behavior and how to control this through the life of devices. Oxygen vacancies have been observed to degrade the behavior of ferroelectric materials and devices[182], and disorder has been observed to reduce the Curie temperature of some materials.[183] Key challenges include understanding the significance of this degradation behavior and whether they can be eliminated and

prevented during operation within active device regions so strategies can be developed to address these in synthesis. If these defect issues can't be resolved, the potential for these materials in future technologies may never be realized.

A foundational understanding is needed on how properties can be modulated with interface control during fabrication and whether defect generation and degradation of material properties are intrinsic or changeable. Critical knowledge is needed to determine whether existing limitations on properties at room temperature are intrinsic to the materials, as these intrinsic limitations can't be overcome with engineering thus other solutions would need to be sought. The ability to design material systems that achieve high coupling of electric fields with magnetic properties at room temperature, e.g., magnetoelectrics is urgently needed. It would be important to predict the reversibility of "states," 'switching' time constants, and propagation speeds are expected for these new materials. Kinetic and equilibrium studies are needed to provide sufficient insight into the switching dynamics and stability of these materials. It is important to develop an understanding of which fields and what magnitudes of fields produce detrimental defects that can degrade material properties. Also, it is important to determine whether internal fields, doping, strain, or other effects could drive defects to inactive regions or neutralize them.

The challenge for magnetoelectric applications of these materials is to find systems with a high order of coupling that proceeds above room temperature. Since the orbital structure of these materials is highly coupled, it is important to understand how structural changes could be employed though novel structures such as superlattices to achieve highly coupled properties at desired temperatures. For example, superlattices combining ultrathin films of the proper ferroelectric $PbTiO_3$ and of the paraelectric $SrTiO_3$ oxides behaves like a prototypical improper ferroelectric (with high room temperature polarization and dielectric constant of 600) due to interface coupling based on rotational distortions.[159, 161, 184, 185] Defects and vacancies can degrade the properties of these materials, so the lack of ability to control defects and fabricate these materials with uniform, useful, and reliable properties at relevant dimensions and at temperatures up to 400ºK may limit their insertion potential.

A second major challenge for these magnetoelectric materials is to achieve ferromagnetism to above 400ºK, with a high remnant magnetization that is coupled to electrical properties. As was mentioned in the Beyond CMOS Logic section, many of the perovskite materials have coupled electrical polarization and magnetic properties at low temperatures, but only $BiFeO_3$ is ferroelectric and antiferromagnetic, with significant polarization at room temperature.[148] Stress coupling between room temperature ferroelectric and ferromagnetic materials has been achieved with strain coupling between thin films[163] and nanostructures.[164, 165] A critical question is whether novel complex metal oxide superlattices could couple properties such as ferroelectric and ferromagnetism. Superlattice interfaces can also change the nature of the coupling between competing instabilities and produce new properties, so as these structures are explored, efforts should be made to understand how important properties, such as ferromagnetism, could be improved and the Curie temperature increased to over 400ºK. Progress and issues on complex oxide heterointerfaces and superlattices are discussed in more detail in the document: *Complex Metal Oxide Heterointerfaces and Superlattices*.

LITHOGRAPHY MATERIALS

The future of scaled technologies depends upon emerging patterning (resist or self assembled) materials to enable extensible lithographic capabilities. New resist materials must concurrently exhibit higher resolution, higher sensitivity, reduced line edge roughness, and sufficient etch resistance to effect robust pattern transfer. Evolutionary approaches for enhancing positive, negative, and chemically amplified families of resists will continue to be evaluated. Several process approaches to pitch division, such as spacer patterning (SP), double patterning (DP) and double exposure (DE), are under consideration as options for extending 193nm lithography. For DE, new materials are needed that utilize more radical supramolecular materials with metastable states. Alternate technologies that utilize patterning materials include directed self assembly and imprint patterning. The advantages of and challenges to these patterning materials are summarized in Table ERM7. Please see the *2009 ITRS Lithography chapter* for a more detailed review of pitch division technologies.

Table ERM7 Challenges for Lithography Materials

RESIST MATERIALS

Advanced lithographic processes are challenged to simultaneously achieve high resolution (R), low line width roughness (L) and high sensitivity (S), with sub-100 nm resist thicknesses. The current set of extensible exposure technology potential solutions include: 1) ArF dry or immersion lithography, which represents a significant increase in process complexity; 2) EUV lithography, 3) and maskless lithography.[186] Advanced resist materials must be developed to satisfy

the RLS requirements, as well as specific ArF dry, ArF immersion, EUV or maskless lithographic technology requirements. Of the three pitch halving approaches (see the *ITRS 2009 Lithography Chapter*), ArF double exposure (DE) single development lithography may provide a lower cost of ownership than the process intensive spacer patterning (SP) or double resist patterning (DP) methods. Aggressive research and development are needed for potential DE materials that satisfy 193 nm insertion targets.[187] EUVL requires revolutionary resist materials that address the RLS tradeoff and exhibit reduced outgassing.[188-190] Resist film thicknesses may continue to shrink with feature size, in part, to avoid pattern collapse.[191, 192] Below a critical thickness, the resist mechanical and thermal properties change. (Figure 1).[193-195] For example, the glass transition temperature of ultrathin multicomponent ArF and EUV resist films depends on the PAG/resist combination.[196] Also, line width roughness appears to increase with decreasing film thickness, as shown in Figure 1.[188, 197, 198] Future semiconductor processes might also require several different post processing methods[199] to meet the projected 16 nm LWR requirements. While work on positive chemically amplified resists will continue, research is underway to explore other potential material candidates that satisfy projected requirements for enabling emerging lithographic technologies. Organic, inorganic, and hybrid materials are under consideration for targeted resist applications that include: non-chemically amplified resists, novel negative resists, and 193 nm double exposure resists.

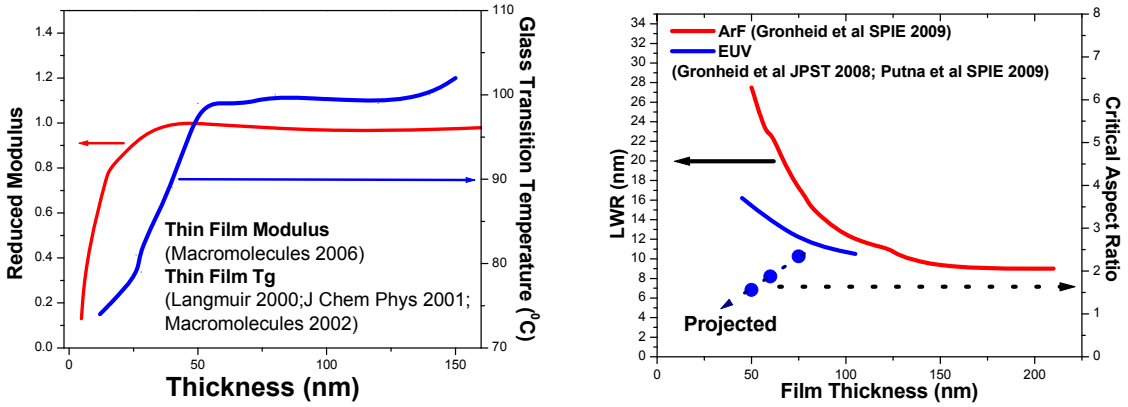

Figure 1 *Thermal and Mechanical Properties of Thin Polymer Films (left) and the Resist Film Thickness Effect on Lithographic Performance (right)*

NM RESIST EXTENSION OPTIONS

The primary focus of resist development will continue to be the evolutionary design of positive photoresist for use with chemical amplified resist; however, the challenge of simultaneously achieving resolution, sensitivity, and line edge roughness remains daunting. Consequently, older material systems, such as nonchemically amplified resists, negative resists, and materials to support pitch division are also being explored.

NM NON-CAR MATERIALS

Recent advances in ArF excimer laser technology will soon result in lasers with enhanced exposure intensity and throughput.[200] Recent increases in ArF immersion scanner speeds provide excess photons that may enable the reevaluation of low sensitivity resist materials, including non-CARs. Also, up to 7× sensitivity improvement can be realized by reducing PMMA film thickness to ~ 20 nm.[201] Polysulfones, which are more sensitive than PMMA, also are under consideration for 193 immersion lithography applications. A post exposure bake can accelerate polysulfone depolymerization. 193 nm irradiation of polynorbornenesulfone[201] results in film thinning, reduced SO_2 content, and E_0 of <50 mJ/cm^2, when developed in an IPA/CHN mixture. Successful non-CAR thin film materials must demonstrate enhanced ArF sensitivity, resolution, and plasma etch resistance, while maintaining acceptable levels of LER. This consideration may limit the applicability of chain scissioning type chemistries, or polymer designs. Many of these systems include significant levels of heteroatoms, such as oxygen or sulfur.

NM NEGATIVE TONE RESIST MATERIALS

Several ArF negative tone resist materials were developed to operate by a cross-linking or a polarity change mechanism.[202, 203] Negative resists tend to perform better than positive tone resists with binary masks, but respond less well to 6% phase-shift mask designs. This behavior may limit the use of negative imaging in some types of memory cell layouts, in which dipole illumination is preferred.

Recently, a top coat free ArF negative tone resist was developed and demonstrated, utilizing a 1.07NA 193nm immersion scanner. Its performance was similar to that of a corresponding positive tone resist.[204] Historically, negative tone resists tended to exhibit pattern bridging. For 193I exposure applications, this defect path must be addressed. The tendency to form microbridging with negative resist materials may increase when the aerial image has significant flare or when light is diffracted into dark areas (low κ_1). Negative resist designs must take this into consideration.

nm Pitch Division

Pitch division technology options, such as spacer patterning and dual pattering, should not require new materials. However, the double exposure option would require new materials that exhibit a nonlinear response in the resist and a new exposure mechanism. Alternatively, a single exposure process with dual, positive and negative, tone developer has been demonstrated.

Single Exposure Dual Tone Develop

In this method, a positive developer removes resist with the highest dose, while the negative developer removes the lowest dose resist, leaving an intermediate dosed resist pattern. Dense 38 nm L/S features were demonstrated with 1.35 NA exposure and dual tone develop. This result represents a proof of concept for enhancing CD uniformity and achieving low LWR.[205] However, significant work is needed to optimize dimensional control.

Double Exposure Materials for 193 nm Lithography

"Double exposure materials" refers to materials that enable pitch-division imaging with two arbitrary sequential exposures, without de-chucking the wafer between exposures. Such a material would provide benefits in cost, improved overlay, and greater design rule flexibility, versus other pitch-division approaches. What makes these materials so challenging is that their behavior depends on the total dose received, a well as the time history in which the photons were received. For example, the acid produced in the photoresist could be proportional to the sum of the squares of the two exposure doses, e.g., $D1^2 + D2^2$, but not $(D1+D2)^2$. This property, called non-reciprocity, is needed for the material to distinguish information, which would normally be lost in regions of overlap in a double exposure scheme. The reason for this nonreciprocity behavior can be seen in the figure below, which depicts two interleaved exposures. With each exposure at the pitch-limit of the exposure tool, these exposures manifest as pure sine waves, e.g., 1+cos(kx) and 1-cos(kx). Since the sum of the exposures is a constant, a material whose response is linear in dose yields no pattern. On the other hand, the acid yield of certain materials is a function of the sum of the quadratic doses, e.g., $D1^2 + D2^2$. Under this scenario the acid concentration yield is modulated at half the pitch of a single exposure (green line).

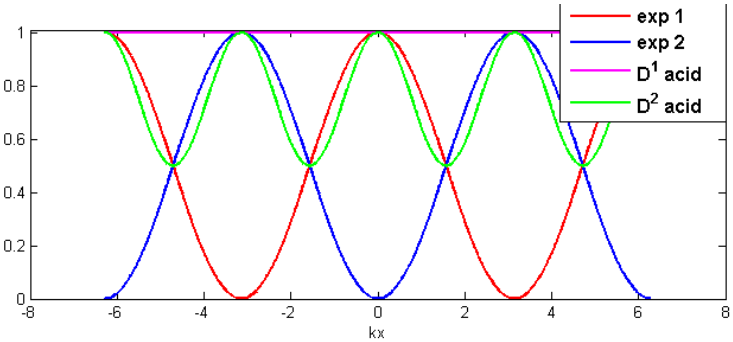

Figure 2 *Ideal Acid Response of A 2-Stage PAG, after 2 Exposures, at the Pitch Limit of the Tool.*

True two-photon absorption produces an intensity squared (I^2) response; however, the required cross-sections for relevant lithographic pulse lengths are many orders of magnitude greater than those available.[206, 207] Thermal response is also naturally non-reciprocal; however, this suffers from resolution limits due to diffusion. The reversible contrast enhancement layer (rCEL) approach, has been modeled extensively[206, 207], but the resulting contrast is simply too low, due to diffractive effects and the imperfect bleaching available from even remotely realistic materials.

Promising results have been reported with use of an "optical threshold layer"[206], in which a reversible 193-activated "sieve" layer permits anisotropic diffusion of a photoacid or other reactive species. While many different systems are under active investigation, none have yet demonstrated a sufficiently sharp diffusion switch to enable high resolution patterning.

The current leading approaches utilize a reversible two-stage PAG system. After one photon is absorbed, the PAG or sensitizer goes into an intermediate state, which then absorbs a second photon that causes an acid to be released. If the

acid is not released, then the intermediate state reverses back to the original state. The reversibility can happen automatically or can be forced by flood exposure of a non-patterned wavelength (e.g., with a photo-switched sensitizer). Experimental evidence has been published for two different systems displaying much of this behavior. A dimeric 2-methoxynaphthalene sensitizer with a 193nm transparent PAG showed zero acid production at low dose, and then increasing acid production at later doses.[208, 209] A modified tethered bromo-anthracene system showed evidence of D^2 behavior in solution (acetonitrile), and apparent reversibility without acid release.[207] However, this system showed significant single exposure acid release as well. In general, the latter effect of preventing the sequential photochemistry pathway from bypassing the intermediate step may prove to be quite a difficult challenge.

Even if the necessary 2-stage PAG works in the sense of reversible 2-photon behavior, it is not clear how much time would be required to develop such a chemically-amplified system to support robust imaging with the needed performance; such a system would still need to satisfy photo-speed, resolution, and line edge roughness requirements. If spacer pitch division techniques are ready on time, they would presumably be adopted and the DE materials would not. However, given the cost saving and scaling potential, DE resist could provide significant benefits.

EUV RESIST

The primary focus of resist development is on the extensibility of positive chemically amplified resist. Alternate materials are under consideration for addressing the simultaneous challenges of achieving high sensitivity, high resolution, low line edge roughness, low outgassing, and pattern collapse.

EUV NEGATIVE TONE CATIONIC RESIST MATERIALS

EUVL is expected to have 7 % flare (background illumination), which affects resolution and the process window. Negative tone resist was investigated to reduce the flare effects intrinsic to the bright field mask. Negative tone resist showed the largest process window for 60 nm isolated lines.[210] Molecular glass fullerene resist, composed of a fullerene derivative, novolac epoxide and a photoacid generator was evaluated using a scanning electron microscope and developed using organic solvent.[211] These chemically amplified fullerene based resists show high sensitivity (11 $\mu C/cm^2$), good resolution (20 nm hp), and low line width roughness (2.5 to 4.5 nm). The etch resistances of these resists are comparable to that of SAL601, a high durability commercial resist. A negative tone molecular glass, synthesized via a cationic polymerization mechanism, was developed and evaluated using e-beam and EUVL and developed using organic solvent.[212] Epoxy functionality was varied systematically in these molecular glass resists, which resolved 35 to 25 nm hp patterns with high sensitivity (38 to 22 $\mu C/cm^2$) and showed low line edge roughness.

NON-CHEMICALLY AMPLIFIED NEGATIVE TONE RESIST MATERIALS

If the negative tone resist operates by a mass-conserving cross linking mechanism, then it should exhibit low out gassing. Cross-linking chemistries also are being investigated to determine whether they can achieve resolution, sensitivity, LER and etch resistance. A number of these individual properties have been demonstrated. The challenge is to develop a single resist system that satisfies the combined set of projected requirements. One high resolution, low molecular weight resist material, i.e., 3,3-dimethoxy-4,4-diazidobiphenyl and cresol novolak, resolved 20 nm L/S arrays and 20 nm dot patterns with e-beam lithography.[213] Similarly, a polyphenol molecular glass and azide cross-linker also shows good resolution and reduced LER.[214] Another molecular glass approach, using the calixarene derivative, shows ultrahigh resolution (10 nm), little side roughness, and high durability to halide plasma etching.[215, 216] Photo-radical crosslinking approaches are mass-conserving and should generate little out gassing. For example, a resist containing a low polydispersity PHS- thiol compound and a photo-radical initiator resolved 60 nm isolated lines, at a dose of 5-6 mJ/cm^2 with EUV.[217] This new resist out gassed less than the SELETE standard resist. A particularly attractive aspect of non-chemically amplified negative toned resists is that there is likely to be fewer molecular structural design tradeoffs between plasma etch resistance and photospeed, when compared to positively toned non-CA resists. This suggests that the negative toned resist approach appears to be more likely to achieve good etch resistance, while maintaining photospeed.

INORGANIC AND ORGANIC-INORGANIC HYBRID RESIST

As features continue to scale, pattern collapse represents another emerging challenge to overcome. Electron beam inorganic resist can exhibit higher contrast than organic resist. They also can exhibit superior mechanical properties that could prevent the collapse of dense high aspect ratio features. For example, e-beam exposed HSQ based negative tone resists have resolved 20 nm features[218] with low line edge roughness, <2nm.[220, 221] However, inorganic resists tend to offer low exposure sensitivity. New inorganic electron-beam resists with Zr and Hf[222] have demonstrated sensitivities as low as 8 $\mu C/cm^2$, achieved 15-nm lines and 36-nm dense features at higher doses, with a line-width roughness of approximately 2 nm. These resists also exhibit high etch resistance (>7× that of thermal SiO_2) in reactive-plasma etching. Incorporation of 4–15 wt % silica particles within commercial e-beam resists, such as ZEP520 and KRS-XE increased etch resistance in O_2[223] without degrading the sensitivity and contrast. E-beam lithography of (20–100 keV) silica nanoparticle bearing

resists exhibit significantly enhanced resolution over their pure counterpart. These systems enable enhanced pattern definition, with up to 100% reduction of line broadening in some cases. Resist component out gassing from inorganic and organic-inorganic hybrid resist materials adversely impact their insertion potential. Considerable work is needed to quantify and analyze the type and number of out gassing molecules, as well as the impact of hybrid nanoparticle bearing resists on defect generation and the post-etch transfer of LER and LWR.

EUV NON-CAR MATERIALS

Non-chemically amplified resists tend to operate by a chain scission mechanism. It remains to be seen whether these resists could exhibit lower out gassing than that observed in chemically amplified resist systems. PMMA has resolved line/space patterns down to 20 nm with EUV exposure. It also exhibited very small apparent line edge roughness (LER) and nearly vertical sidewalls.[224] The mean size of the PMMA was five times larger than standard CAR resist and was developed using a MIBK:IPA solution. The number of out gassed molecules per cm^2 for PMMA was observed to be on the order of 1E14. α-Trifluoromethane substituted PMMA[198, 225] exhibited increased EUV absorption and reduced out gassing. T When subjected to EUV exposure, this system resolved 50 nm 1:1 LS features, with a photospeed 4.0 times higher than a corresponding exposure in PMMA. To increase sensitivity, glass transition temperature, and etch resistance, linear polycarbonates with polysulfone backbones were evaluated. These systems demonstrated resolution that ranged from 35 to 50 nm LS, with low LER and increased sensitivity compared to PMMA.[226] EUV patterned poly(1-butene sulfone) can resolve 50 nm half pitch patterns.[227] A key requirement for the successful implementation of non-CAR materials will be the demonstration of enhanced plasma etch resistance, while maintaining good EUV sensitivity. This could be difficult to achieve, since the molecular structural considerations for plasma etch resistance and sensitivity are generally in opposition.

DIRECTED SELF ASSEMBLY FOR LITHOGRAPHY EXTENSION

Directed self-assembly (DSA) refers to the alignment of self-assembled patterns in desired locations, with predictable shapes, controlled dimensions, and registered within a lithographically generated pattern. Progress has been made in demonstrating alignment to sparse patterns, domain sizes down to 7 nm, and lithographically useful anneal times. The challenges for directed self assembly are summarized in *Table ERM7*.

CRITICAL CHALLENGES

If DSA is to be considered a viable and competitive patterning option, it must be able to form a desired set of structures at dimensions at least a factor of two smaller and with twice the density as can be achieved by conventional lithographic methods. This corresponds to resolution, LER, and LWR targets of <12 nm, <1.3 nm, and < 1.7 nm, respectively. The structures must form in predefined locations with respect to existing structures, and with low defect density. The net time required to form and fix a pattern must be compatible with conventional inline process requirements and a throughput of one hundred twenty 300 mm wafers/hour. Also, the ability to achieve pattern registration, required feature sizes, density, low defect levels, etch resistance, and process times must be demonstrated simultaneously in an experiment with the same material.

STATE-OF-THE-ART

Recent research has brought progress in each of these aspects, but no material/process combination currently satisfies all of these requirements. Block copolymer self-assembly can easily define a limited set of highly symmetric patterns, i.e. repeating lines/spaces and hexagonal arrays of cylindrical holes, that may be useful in defining circuit elements. The ability to draw from a richer set of shapes would broaden its utility and range of application. A variety of DSA methods provide the means to position self-assembled patterns on a wafer, to orient the pattern with a specific directionality, and to register the pattern with respect to previous lithography levels. Annealing times, which depend on the rate at which the system approaches thermodynamic equilibrium, have been reduced from multiple days and hours to a few minutes, through the use of solvent annealing, which represents a realistic timescale for potential processing applications. Self-assembled structures have been generated with dimensions well below 10 nm, providing evidence of this approach's extensibility. Defect densities represent a significant research challenge, as the best results observed to date are orders of magnitude larger than the requirement of $<.01/cm^2$.

Two distinct DSA methods have been widely practiced. The first, a form of graphoepitaxy, employs a trench or other relief feature to confine self assembly. In the second, a surface pattern with contrasting chemical properties directs self assembly. Both of these techniques require a "neutral" layer to enable assembly of vertically aligned structures over the substrate materials.

DSA GRAPHOEPITAXY

In this approach, lithographically-defined topographic features and boundaries direct the ordering of a self-assembled block copolymer film. The self-assembled patterns self register to the lithographically defined and etched pattern and subdivide it into features with sublithographic resolution. The surface properties of the recesses control pattern alignment. For example, if the bottom of a groove is neutral but the sidewall is preferentially wetted by one block, then lamellae form in parallel with the groove. If all surfaces are neutral, then the lamellae orient perpendicular to the groove. Lines also tend to reproduce and track defects in the lithographically defined wall. Therefore, for the graphoepitaxy approach, the quality of the final self-assembled patterns depends on precise control of the lithographic process forming the guide pattern. A key challenge is to develop systems that are tolerant of small variations in the lithographic pattern.

These self assembled block copolymeric systems exhibit placement errors that depend upon template edge roughness and polymer domain non-uniformity. Registration accuracy is dictated by phase-separation thermodynamics, composition, and polydispersity effects.[228] The projected requirement of 1.4 nm registration accuracy for 16 nm half pitch corresponds to a spacing accuracy of ~0.04 percent of the intrinsic period of the polymer pattern (termed L_0). This is considerably smaller than typical domain size/spacing distributions of 3σ ~0.09–0.3 L_0 for sphere or cylinder-forming patterns.[229] Research is needed to develop less sensitive material systems or methods that maintain constant film thickness over substrate topography.

In an alternate strategy for graphoepitaxial DSA, a sparse lattice of nanoscale posts can template growth of a two-dimensional array of spherical microdomains. The guide posts substitute for a small fraction the spherical domains in a regular fashion and thereby provide periodic constraints that induce long range order with reduced defectivity.[230]

DSA SURFACE ENERGY

Directed block copolymer assembly on substrates bearing lithographically defined chemical nanopatterns offers a second route for aligning and registering patterns of block copolymer microdomains.[231] In this approach, a thin organic layer, for example, a self-assembled monolayer or a polymer brush, is deposited on a substrate, lithographically patterned, and that pattern is transferred to the organic layer (for example, by an oxygen plasma etch) to define regions with distinct chemistry and surface energies. When the surface-modified substrate is coated with a thin block copolymer film and thermally annealed, preferential wetting drives each block to migrate towards chemically compatible surface regions, so as to minimize the free energy of the system. If the contrast in the surface pattern is strong, then significant mismatch in the periods L_s and L_o can be tolerated before increased defectivity is observed.[232] With strong polymer-surface interactions, the block copolymer domains can be directed into many of the essential features required for manufacturing integrated circuits with regular fabric architectures, including dense and isolated bends, jogs, spots, line terminations, and T-junctions.[231, 233] Improved CD control and LER at nanoscale dimensions are key benefits of this directed self-assembly approach: such films can correct for line width variations in the chemical surface pattern and maintain the copolymer pattern CD equal to 0.5 Ls[234], and the polymer also appears to exhibit some self healing behavior.

Recent research has demonstrated the spatial frequency multiplication of sparse, lithographically-defined chemical surface patterns using block copolymer DSA. Examples of forming cylindrical[235, 236] and lamellar[237] microdomains have been described. In each case, the quality of the final microdomain structures is superior to that of the chemical surface patterns, as measured by placement error, dimensional uniformity, and LER. These sparse patterning methods provide a means to bridge the gap between the dimensional scale accessible by advanced optical lithography and the sublithographic scale, where self-assembly offers the greatest benefit.

This approach depends upon a multi-step process to produce the local alterations of the neutral layer's chemical properties. Further research is needed on materials and one step methods that would enable direct lithographically induced spatial variation in surface chemistry and functionalization.

APPLYING SUPRAMOLECULAR AND HYBRID CONCEPTS TO SELF-ASSEMBLY

As was mentioned earlier, although many of the critical capabilities have been demonstrated in individual experiments, they have yet to be demonstrated in one experiment and new materials with more flexibility are needed. Systematic studies of the self-assembly of new diblock and triblock copolymers materials and architectures will broaden their utility and improve their functionality. For example, recent work using hybrid blends of block copolymers with organisilicate oligomers[238] and blends of homopolymers with triblock polymers[239] have demonstrated characteristic microdomain spacing well below 10 nm, an indicator of potential extensibility. In another recent report, supramolecular assembly of hydrogen-bonding units was combined with the controlled phase segregation of diblock copolymers to fabricate highly-ordered square arrays of sub-20 nm via structures, instead of the hexagonal ordering that is normally observed.[240] A more evolutionary path may require a hybrid resist formulation that incorporates phase segregating diblock copolymers to yield

a resist that can self-assemble within the patterned feature, and a proof of concept has been demonstrated.[241] However, significant research in these areas is needed for these systems to warrant consideration for sub-22 nm potential solutions.

PROCESS SIMPLIFICATION

A critical challenge is to simplify the process used to define the patterns that direct the alignment of the block co-polymers. Graphoepitaxy requires multiple process steps to pattern, etch, and tune the substrate surface energy. The integration of photoresist functionality with self assembly[241] could provide a potential path to process simplification, but significant research is needed to make this a viable technology.

EMERGING FRONT END PROCESSES' AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES' MATERIAL CHALLENGES AND OPTIONS

Key challenges for future FEP and PIDS materials and processes are to support extending CMOS to smaller dimensions with reduced variation in device performance. This will require more accurate placement of dopants in active device areas, directed self assembly of useful nanomaterials, and materials to enable selective deposition, etch, and cleans to enable self aligned structures in future devices. The requirements and challenges for ERM applied to FEP and PIDS applications are summarized in Table ERM8.

DOPING AND DEPOSITION

CRITICAL CHALLENGES: THE IMPORTANCE OF DETERMINISTIC FABRICATION

Table ERM8 FEP / PIDS Challenges for Self Assembly

A key challenge for scaling semiconductor devices towards 10 nm is the ability to achieve high doping levels within source/drain regions, with abrupt dopant gradients with small variations at the source/drain interface to the channel, as well as controlled dopant positions within the channel. For example, the series resistance of a MOSFET continues to be a difficult challenge that becomes more severe with scaling. A large part of the parasitic series resistance critically depends on the lateral doping and the abruptness of the source/drain junction. Currently, the total series resistance degrades the on-current by more than 30%. To a lesser degree, variations in S/D interface doping degrade on-current uniformity. It will be difficult to maintain the same degradation percentage variation for smaller gate lengths. This S/D doping interface profile determines the length of the transition region between the S/D regions and the channel. An ideal transition is a step profile. In practice, this transition region must be small compared to the channel length. One way to control the doping profile is by deterministic processing and doping. Additionally, the threshold voltage, V_t, is sensitive to small variations in channel dimensions, the gate stack structure, and dopant variations in the depletion layer. V_t variability will gate the extensibility of bulk planar CMOS device technology.[242] Over the next six to thirteen years, MPU physical gate lengths, L_{gate}, are projected to scale from 17 nm to 9 nm. Also, the trend in the number of channel electrons suggests that by the year 2014 there may be less than one hundred active dopants in the channel region[243] For channel doped devices, this low number of channel dopants may emerge as a another critical performance and yield limiter. (A more detailed discussion on the number of dopants in the channel can be found in the supplemental document.).[244, 245] In general, dimensional control and variability are emerging as key materials challenges. Ideally, source-channel-drain interfaces would be atomically abrupt and exhibit atomically precise control of dopant position and composition. Research is needed to develop new materials and fabrication methods that enable deterministic control of the composition and structure of doped material and gradient systems.

For FEP and PIDS applications, deterministic fabrication refers to 3D nanopatterning and assembly methods that provide sufficient control of the composition and structure of doped interfaces and components to yield several orders of magnitude improvements in device to device performance variability.[246] Doping processes with atomic-scale placement and concentration control will enable tunable device performance characteristics and reduced device-to-device variations. A reduction in device noise enlarges the useable design space, circuit-level uniformity, and system performance. The ability to accurately place dopants also may enable radically new device concepts, such as emerging quantum computing devices, based on coherent manipulation of single dopant atomic states within Si[247] or diamond matrices.[248] Candidate doping options must address the following: 1) accurate control of the number and position of dopants; 2) statistical fluctuation of dopant numbers on device characteristics; 3) compatibility and integration with existing fabrication platforms; and 4) economics, which depends upon on R&D and equipment costs, yield, and throughput.

The deterministic 3D dopant placement and structural control technology required to enable atomically abrupt and reproducible source-channel-drain interfaces is in the early phases of exploratory research. This year's revision considers three potential options for extensible channel doping: Single ion implantation, shallow doping via Langmiur self-assembly and dopant deposition, and scanning tunneling microscope induced dopant placement.

STATE-OF-THE-ART

A. **Single ion implantation (SII)**[249]—This technology seeks to deposit a specified number of desired dopant ions at precise locations within the active region. Key objectives are to achieve ion implantations with:
   - High spatial resolution and flexibility in dopant species, as well as 100% single dopant detection.
   - Scanning probe alignment, combined with single ion impact sensing through monitoring of 2DEG upsets, as a universal tool for single atom placement

   Key research challenges include: dopant counting and dopant placement. Single ion implantation can be measured by the detection of secondary electrons, photons, electron-hole pairs, changes in transistor channel currents, or direct imaging changes in surface topography. Significant sources of dopant positioning errors, such as implantation spot size, range straggling, and diffusion and segregation during annealing, must be addressed for SII to be relevant for ultimately scaled doped devices and related application opportunities, such as:
   - Single atom device development, which requires a method for reliable single atom doping
   - Systematic studies of dopant fluctuation effects and tests of quantum computer architectures (qubit readout, control and coupling) in relevant device platforms and substrates, e.g., silicon and diamond

B. **Self-assembly and surface chemistry**[250]—This chemistry based approach teaches that the dose can be modulated precisely by the formation of a mixed monolayer, consisting of tunable blank and active precursor components. Additionally, controlled nanoscale semiconductor doping by self-assembled molecular monolayers can achieve sub-5 nm ultra-shallow junctions with spike anneals, due to the lack of transient enhanced diffusion often encountered in ion implantation. A key objective is to heavily dope 'self aligned' semiconductor materials for nanowire and planar device applications.

C. **STM positioning**[251]—Fabrication of atomically precise devices has been demonstrated in silicon, using a combination of scanning probe microscopy and molecular beam epitaxy. Potential benefits of the STM approach include: The ability to pattern with atomic precision in three dimensions; extremely high density, atomically planar and abrupt doping profiles; the ability to pattern sub 10nm MOSFET architectures; the investigation of novel device architectures; and applicability to other dopant sources/metal/organics. It is highly unlikely that this technique will warrant consideration as a potential solution for advanced device fabrication, because of low throughput, STM tip stability, reproducibility. On the other hand, the patterning accuracy of this technique may enable exploration of unique devices.

KEY MESSAGES

Extremely high placement accuracy, <1 nm, doping methods, e.g., STM, are not likely to become manufacturable, as the proposed massively parallel approaches face significant data management challenges. However, these methods may enable the exploration of fundamental device limits and new functionality, such as symmetry and quantum effects. Medium placement accuracy, ~10 nm, doping methods (i.e., single ion implantation) exhibit the potential for device development applications. The projected manufacturing requirements create a need for new doping concepts. Research is needed on high throughput doping options that also deliver high placement accuracy. Emerging candidate doping research focus areas include directed self assembly and the use of molecular monolayers as scaffolds for controlled dopant delivery.

DIRECTED SELF ASSEMBLY OF USEFUL NANOMATERIALS (SEE THE LITHOGRAPHY SECTION DISCUSSION).

The use of directed self assembly to position nanostructured materials, such as carbon nanotubes[252, 253] has made progress but, considerable improvement in control of location direction and defect density is needed before this would warrant consideration for fabricating future charge based devices.

SELECTIVE ETCH AND CLEAN/SURFACE PREPARATION

With the wide range of new materials potentially being integrated into future technologies, there are significant needs for materials that enable selective and customized etching, cleaning or material deposition. Either macromolecules or self assembly processes that can enable coating of a specific material in the presence of other chemical processes, such as etching or chemical mechanical polishing could improve process selectivity and yield. Similarly, as feature sizes are reduced, cleaning processes will need to be more selective in removing particles without disturbing the desired structures.

Thus, there are opportunities for macromolecules and self assembled materials to enable the enhanced selectivity of future manufacturing processes.

SELECTIVE ETCH

Etch represents a critical step in conventional top-down pattern transfer processing. The lithographic and etch processes are significant contributors to the final dimension, dimensional variation, and functionality of a patterned feature. It may be advantageous to consider simplified fabrication scenarios that reduce the number of pattern transfer steps and the corresponding process related variability. The directed self-assembly of electronically useful materials represents an identified set of emerging technology options that show some potential for process simplification and for reducing patterning related variability. Early approaches for directed self assembly target resist applications that complement and leverage existing and projected lithographic and etch technologies. Future generations of self-assembling systems may be designed to incorporate electronically useful materials that would obviate the need for some etches.

CLEAN/SURFACE PREPARATION

Many of the projected surface preparation and cleaning requirements will depend upon the device technologies chosen for sub-22 nm applications. While most specific ERM related surface preparation challenges have yet to be defined, interface control represents one example of an emerging surface preparation challenge that is expected to become increasingly critical for ultimately scaled and functionally diversified systems. Current models that estimate pre-gate clean metrics are outdated, as they cannot address the atomic and nanoscopic factors that drive the performance of future engineered surfaces. New concepts, methods, and models are needed that anticipate advanced cleaning scenarios and guide projected clean requirements for future technologies. Several cleaning and surface preparation technology options are receiving considerable research and development support. These include laser, electrostatics, depositions of engineered functional macromolecules, i.e. designed dendrimers, molecular glasses, etc. Macromolecules are needed that can attach to a specific material, protect against etch or cleans, and then be easily removed. Within the next few years, a few of these emerging technologies may warrant a critical assessment of their potential as PIDS and FEP related potential solutions for improving process stability and enabling high density beyond CMOS devices.

EMERGING FEP AND PIDS MATERIAL AND STRUCTURAL CHALLENGES AND OPTIONS

CONTACTS

Understanding and engineering atomic level contacts is critical for molecular scale devices. For these systems, nanoscopic factors, such as bond formation and configuration, significantly impact contact potential barriers.[254] Additionally, metal molecule interactions[255] and deposition variability may dominate nanoscale device operation. The nature of the metal-molecule orbital overlap will be important in determining the properties of their combined occupied states and available conduction pathways. For good mechanical or electrical contacts to be established with a low potential barrier[254], significant orbital overlap optimization between the molecule and the electrode is needed. Research is needed to understand the structure and properties of metal-molecule interactions and to design and synthesize new molecule-electrode material systems that enable stable, reproducible low potential barrier contacts.

INTERCONNECTS

Key challenges for continued increasing of performance of future integrated circuit interconnects are: maintaining reductions of RC time constants for delivery of signals and power with high reliability. For copper interconnects to be extensible through 2024, the sidewall copper barrier thickness must be reduced to less than 2nm, which is very difficult and challenging for technologies, as is summarized in *Table ERM9*. For post copper interconnect scaling, novel interconnects, such as carbon nanotubes, are being explored for their low resistivity and electromigration resistance and the challenges for these technologies are summarized in *Table ERM10.* Also, lower dielectric constant (κ intra and inter level dielectric are needed; however, each of these emerging families of materials must overcome significant challenges for them to warrant adoption, but if airgap were to be adopted, this would place additional requirements on barrier layers or novel interconnects.

COPPER EXTENSION MATERIALS

ULTRATHIN BARRIERS

The scaling of barrier thickness below 2nm faces several challenges including the ability to block diffusion of Cu during processing, packaging and operation, have good adhesion to Cu and the low-κ ILD, block H_2O/O_2 diffusion into the Cu, and be compatible with Cu interconnect processing, such as CMP, ILD etch, and photoresist ashing. New barrier materials, such Ru and CuMn that are discussed in the Interconnect chapter, are in development and expected to maintain

barrier thickness scaling several generations, but forecasts project Cu barrier layer thicknesses of < 2 nm by 2015 and < 1 nm by 2021. At these dimensions, it is anticipated that all barrier materials in development may fail and new materials or multilayer thin films will be needed, and if the industry moves to airgap ILD technology, the requirements on this barrier structure will become more challenging. A serious issue is that all research on alternate barrier layers only reports results down to 5nm, but this needs to be extended down to 1nm. (See the critical challenges in Table ERM9)

Table ERM9 Interconnect Material Challenges

A logical extension of the current Ta and TaN barrier materials would be to identify new transition metal nitrides or ternary nitrides with improved barrier capabilities that meet future requirements. Alternate transition metal nitrides currently under consideration include ZrN, ZrGeN, Mo/WN, HfN, and HfGeN[256-258], at thicknesses on 5–70 nm. For these materials to warrant further insertion consideration, their Cu diffusion barrier performance must be demonstrated at thicknesses of 5 to <1 nm. Other options to consider include deposition of multilayer thin film stacks with each material having a specific function, but also enhancing the performance of other materials in the structure.

PVD barrier candidates for 30 and 22 nm technology nodes that enable direct Cu plating, such as Ru face serious challenges, as described in the Interconnects chapter. Consequently, continued research on promising alternate direct plate barrier materials, such as Os and Ir, is needed.[259] Recent results show that a 5nm Ir/5nm TaN composite serves as an adequate Cu diffusion barrier.[260, 261] Research is needed on these and other emerging materials (Pt, Pd, Rh[259]) to demonstrate the feasibility of barrier performance down to 1–2nm and gap fill on < 100 nm trenches and passivation to inhibit oxidation.[262]

Self assembled monolayers (SAMs) represent a recent addition to the 2009 ITRS set of Cu barrier material. SAMs can be utilized to enable an all "wet" Cu barrier and Cu fill electroless plating process, or to serve as the Cu barrier. SAMs + Pd activation is reported to enable electroless plating of various Ni compounds (NiB, NiP, NiReP), which serve as the Cu diffusion barrier[263, 264], followed by electroless Cu plating. The Cu gap fill and diffusion barrier performance of NiB has been demonstrated down to 6 nm and needs to be investigated further. Other challenges to this all wet barrier plus Cu route include demonstrating: barrier plating and Cu gap fill in sub 100 nm trenches and vias, minimal (< 1%) impact to the low-κ ILD dielectric constant, and good adhesion to the low-κ ILD and Cu. Finally, additional research is needed to explore SAMs potential as a Cu barrier technology.

CU CAPPING LAYERS:

Concurrent thickness and dielectric constant scaling remains a difficult challenge for future Cu capping / etch stop technologies and there are tradeoffs between density, which improves barrier properties, and dielectric constant which increases with density. Difficult challenges include identifying materials with good adhesion to the low-κ ILD and Cu, Cu out diffusion and H_2O_2/O_2 in diffusion prevention, electromigration and leakage, and compatibility with Cu interconnect processing, (ILD etch, photoresist ashing, etc.). The scaling of current low-κ SiCN and SiOC capping layer technologies are expected to continue; however, research is needed on the feasibility of monolayer thick capping layers with a dielectric constant of < 4.0, since current SiN/SiCN/SiOC materials are expected to fail at these dimensions. Another high potential impact research challenge is the elimination of the dielectric capping layer/etch stop by implementing selectively deposited metallic capping layers (such as Cobalt) or self forming CuSiN barriers. Also initial investigation of self assembled monolayers (SAMs) as the top side capping layer can reduce surface oxides[265], curtail in plane Cu transport and electrical leakage[266], but the best results with amino-phenyl terminated SAMs represented only 50% of the leakage performance of a SiN capping layer.[267] Additionally, to warrant potential solution consideration, more research is needed to address several challenges related to SAMs as top side Cu capping layers, which include: low-κ ILD deposition compatibility (thermal stability, plasma damage, etc.), Cu/low-κ ILD and top side low-κ ILD adhesion, diffusion barrier performance to Cu and O_2/H_2O diffusion, and compatibility with interconnect processing (wet/dry etch, CMP, etc.).

Other candidate capping layer materials that require additional research to address these material challenges include, but are not limited to: a-C:H[268], CNx[269], and BCNx[270], which exhibit low-κ (κ < 4), some compatibility with interconnect processing, and the ability to impede Cu diffusion.[270, 271]

NOVEL INTERCONNECTS

Successful copper replacement materials must provide lower resistivity and higher electromigration resistance than copper, at the same dimensions. Potential interconnect replacement materials, such as carbon nanotubes for vias and interconnects and possibly single crystal copper metal nanowires for interconnects, must overcome significant challenges to warrant insertion consideration as identified in Table ERM10.

Table ERM10 Nanomaterial Interconnect Material Properties

NANOTUBE INTERCONNECTS

Emerging SWCNT or MWCNT nanotube interconnects or vias must demonstrate high densities of highly conducting nanotubes in desired locations, with controlled directionality, low-resistance contacts, and be gown with catalyst that are compatible with the ILD and semiconductors. SWCNTs exhibit ballistic transport over longer distances,[272, 273] but consist of a mixture of metallic and semiconducting tubes, while the MWCNTs are metallic. A potential advantage of CNT vias is their ability to carry high current density without electromigration. Their low resistivity may offer potential advantages for interconnect applications, which include their ability to achieve ballistic transport, high current carrying ability, and potential electromigration resistance. Since SWCNTs also exhibit quantum limited contact resistance, their length must be sufficient to yield favorable effective resistivities, as described in the *Interconnect chapter*. Additionally, CNT conductivity must remain high and stable during operation. Research and guiding material-design principles are needed for improved CNT functionalization, deposition, and positional control.

GROWTH IN CONTROLLED LOCATIONS WITH ALIGNMENT

For CNTs to be used as either devices or interconnects, they must be grown in precise locations and aligned in required directions. While progress has been made in growing nanotubes in desired locations,[274] directional alignment remains a challenge. Recent results suggest that CNTs grown in a directed electric field[275] has achieved general directional alignment, but growth on catalyst patterned sapphire or quartz crystal steps has grown aligned CNTs[276,277], placement remains a challenge. While this is less than the required density, this alignment is significantly better than other techniques. Use of zeolite to control CNT growth diameter[278], location and direction, but it still needs to be demonstrated that such a templating matrix has no impact on the CNT conductivity. While several approaches have been identified the practical implementation of this concept to manufacturing remains elusive. Post-growth assembly options also are being explored.

Since interconnects span relatively long distances, high speed growth method should be strongly pursued.[279, 280] Quality of CNTs may affect the ballistic length of carrier transport in a tube. Therefore, high quality CNT growth and evaluation of their quality are important. The length must be sufficient to yield favorable effective resistivities, as described in the Interconnect chapter.

NANOTUBE VIAS

Vertical interconnects (vias) can benefit from the integration of CNTs into future technologies; although an approach for the integration of CNTs into contemporary CMOS technology has already been demonstrated[281, 282] using a scheme based on remote plasma chemical vapor deposition CNT synthesis at low temperature (< 400 °C) into a suitable CMOS single damascene test structure completed with a chemical mechanical polishing step, a number of unsolved critical issues still remain to be addressed. Thus, new hybrid integrating schemes (combining top down and bottom up paths) compatible with the actual CMOS technologies and engineered at a level that also thermal budgets (below 600 °C to reduce the thermal damages to LSI) are needed. In addition, theoretical studies have been carried out to derive electrical properties and offer an important guidance and insight on the applications of CNTs as vias for gigascale-integration chips.[283-287] CNTs can significantly improve the RC delay and thermal conductivity at the intermediate and global level (the lower the via resistance, the lower the delay). For CNT vias to be viable they must be fabricated with catalyst that are compatible with the ILD and semiconductor devices and their electrical and thermal reliability must be demonstrated. A number of key processes for which a control needs to be established to realize the potential of CNTs are the following:

CONTROL OF CHIRALITY AND OF METALLIC VS. SEMICONDUCTING FRACTION:

In order to reach same resistances predicted for Cu-based wirings, it is necessary to produce dense arrays (~1E14 tubes/cm^2) of small diameter (~1.2 nm) metallic SWCNTs and DWCNTs. The variability of CNT-via resistance is a function of the distribution of chiralities, which could exceed projected requirements. Hence, additional research is needed that enables enhanced chirality control. In the case of MWCNTs tradeoffs may need to be made in the diameter and number of walls to achieve the highest density; however, the chirality control may not be a serious issue here as the overall behavior is metallic.

CONTROL OF CONTACT RESISTANCE AND ELECTRICAL CONDUCTIVITY:

The lower intrinsic limit of the resistance for a metallic SWCNT (or a metallic shell of MWCNTs) is 6.5 kΩ (independent of the tube diameter)[288] and reflections at the CNT-metal contact interface and phonon scattering contribute to an increase in total resistance.[289-292] Therefore, reliable and reproducible low resistance ohmic contacts are needed, since high

resistances turn into current downturns. Transparent SWCNT ohmic contacts, scaled to diameters <1.5 nm, remain a key challenge to achieving high-performance nanoelectronic devices, due to the presence of positive Schottky (semiconducting nanotube) and tunneling barriers (metallic nanotubes). Fabricating direct metallic connections between all the nanotube shells also remains a technological challenge, since contact resistances at the bottom and top of CNT-based vias may enhance the risk of local heating and electromigration.[282] In the case of vias filled with MWCNTs, resistances down to 0.6 Ω have been reported for 2 μm diameter vias[282], and 34 Ω was reported for 160 nm diameter vias.[293]

HIGH DENSITY CNT ARRAYS IN SMALL VIAS:

Ideal SWCNT arrays and contact exhibit potential to improve intermediate and global RC delays by >40% over Cu wires. Locally, short low resistance CNT vias are needed that reduce the total capacitance, relative to Cu. Also, in-situ CNT growth and integration on relevant substrates is far from manufacturable. A catalytic process is needed that exclusively promotes growth of metallic SWCNTs, with the required density of ~1E14. Also, appropriate, reliable, and reproducible analytical tools and statistical methods must be developed to help guide the integration studies and assess the insertion potential of this potential via technology.[284, 285, 294, 295]

In the case of MWCNTs, the resistance of a 70 nm diameter via filled with close packed nanotubes of 4 nm diameter 6-wall MWCNTs including the top and bottom barrier layer can be estimated to be as low as that of Cu via. Based on this estimation, the target density of the MWNTs will be 5×10^{12} cm^{-2}. To date, density of 1×10^{12} cm^{-2} vertically aligned diameter-controlled MWCNTs has been reported.[296] Independently, the fabrication of 70-nm diameter vias with MWCNTs grown by pulse-excited remote plasma-enhanced CVD has been also reported.[279, 297]

GRAPHENE AND GRAPHITIC CARBON INTERCONNECTS

Graphene is also a promising candidate for an interconnect material. Graphene is inherently a two-dimensional material, so it may be ideal for horizontal interconnects. Graphene can sustain a high-density current, like carbon nanotubes can, with research demonstrating that a few-layer graphene peeled off from graphite sustained a current larger than 10^8 A/cm^2. [298] Numerical simulations predict that graphene nanoribbons can potentially have smaller resistances compared to copper wires with a unity aspect ratio for widths below 8nm and that piles of non-interacting nanoribbons can have significantly smaller resistivities than Cu wires.[299] In order to realize graphene interconnects, low temperature synthesis of graphene on a substrate should be realized. Recently, synthesis of graphene by chemical vapor deposition has been reported.[300-302] However, the synthesis temperatures are still around 1000°C, which is too high for the interconnect application. Moreover, synthesis by CVD usually requires a catalyst film, which may have to be removed after the synthesis. Anyway, much more efforts in low-temperature synthesis are required to realize graphene interconnects.

CU AND SILICIDE NANOWIRE INTERCONNECTS AND VIAS

If single crystal nanowire metals could be grown with smooth surfaces[303-305], they could reduce many of the issues associated with grain boundary induced resistivity increases and sidewall roughness scattering, as illustrated in the Interconnect Cu Resistivity chart in the *Interconnect chapter*. Research is needed to demonstrate the feasibility of the following: self-assembled nanowires with smoother surfaces and reduced surface scattering; hydrogen passivation to reduce the diameter dependence of resistivity, diffuse surface scattering, and the grain boundary scattering in polycrystalline nanowires.

LOW K INTERLEVEL DIELECTRIC

As identified in the interconnect chapter, to realize lower κ effective interconnects, mainly two different approaches are being pursued 1) pore introduction into ILDs and 2) air gap ILD. Porous low-κ materials exhibit low dielectric constant as low as 2.3 due to low density and pore sizes in the range of less than several nm. Reducing κ value below 2.0 is possible requires increasing the pore volume in ILDs; however, integration issues such as mechanical properties, process compatibility, and moisture absorption, limit their adoption in manufacturing. In order to overcome these issues, alternative molecular designs should be investigated. The second approach is air gap ILD with a κ value close to 1.0. Two typical methods for fabricating air gap interconnect are described below. One is non-conformal CVD deposition on metal lines with materials between them partially or completely removed, and another is damascene metal lines with an embedded sacrificial material which can be selectively removed through a dielectric cap. One of critical challenges in air gap interconnects from the view point of materials is developing sacrificial materials. A summary of the low κ dielectric challenges is included in *Table ERM9*.

In order to reduce dielectric constant of ILD materials, polarizability per unit volume needs to be decreased. For polarizability reduction, one existing method is lowering density of the film and other is using chemical structure having low polarizabilities, and combinations of these two methods are also studied. As a low density ILD material, silica-zeolite

is a possible candidate[306], which exhibits low-κ characteristics due to a porous structure in its silica skeleton, and high mechanical strength due to a three dimensional silica network. Polycarbosilane-based dielectrics with Si-C bonds have smaller dipole moments than Si-O bonds with nonporous films had dielectric constant as low as 2.3[307] and excellent resistance to Cu diffusion under a standard bias temperature stress test conditions. This fact indicates that interconnect structure without barrier metals can be formed by polycarbosilane low-κ dielectrics as ILD, and low resistive Cu wiring can be realized due to barrier-metal-less wiring structure. With smaller volume of pores, κ-value of polycarbosilane may become lower than 2.0. Another low polarizability chemical structure was reported for nonporous fluorocarbon film deposited by plasma enhanced chemical vapor deposition using C_5F_8.[308] The dielectric constant of the films is less than 2.0, and the elastic modulus is higher than 8GPa. Moreover, the fluorocarbon films exhibits excellent adhesion to SiCN barrier dielectric and low leakage current density measured by a current density-electric field characteristics. This film also has a good thermal stability arise from preventing overdecomposition of C_5F_8 gas which results in volatile CF radical generation.

Airgap formation using sacrificial materials is another candidate for realizing low κ effective interconnects. Although the materials are common polymers, the application is new and the potential impact on other interconnect ERM could be significant. Sacrificial polymers must decompose clearly for forming airgaps without any harmful residues, and be compatible with Cu wiring fabrication before airgap formation. A sacrificial polymer based on poly(cyclohexyl methacrylate) formed by initiate chemical vapor deposition left less than 0.3% residue[309] when annealed in a nitrogen ambient with a thermal decomposition temperature of 270°C, which may be compatible with Cu interconnects. By using Poly(neopentyl methacrylate-*co*-ethyleneglycol diacrylate) copolymer, onset temperature can adjust from 290°C to 350°C with removal percentages varying from 93% to 98%.[310] The sacrificial materials exhibit some adequate elastic modulus (3.9-5.5GPa) and high onset decomposition temperatures compatible with Cu interconnect fabrication. Process simplification is needed to enable this technology and this would place additional requirements on the other interconnect materials. The Cu adhesion and barrier layers must have good adhesion to the air gap polymer, but also provide mechanical constraint and electromigration resistance.

ASSEMBLY AND PACKAGE

Key challenges for future assembly and package technologies are to provide a controlled stress package that meets electrical and thermal requirements and is reliable through assembly and product life. Future technologies will require complex packages to electrically connect the boards and other components and with the ability to protect them from stresses, moisture, and other environmental stresses and cost effectively. ERM including nanomaterials, macromolecules, and complex metal oxides may provide solutions to these future requirements, but they must overcome a number of challenges identified in Table ERM11. (3D package and system in package overlap with interconnects) Highly coupled and shared problems and solutions.

Table ERM11 Assembly and Packaging ERM Challenges

MATERIALS FOR LOW TEMPERATURE AND HIERARCHICAL ASSEMBLY

To support assembly of "system on a package" and high performance flip chip packages a hierarchy of lower assembly temperature solders is needed. For system on a package, lower melting point solders are needed to initial mount components and keep them mechanically in place when other components are attached and alloyed with all solder joints form high reliability joints on a final cure. The initial low temperature solder joints need to provide mechanical strength through the following higher temperature reflow operations. For high performance flip chip packages, lower temperature assembly is needed to reduce stress thermal expansion stress. The move to Pb-free electronic packaging, has resulted in the use of higher melting point (>30ºC higher) Pb-free solders, such as those based on the Sn-Ag-Cu (SAC) family, and these have higher mechanical modulus and lower wettability to common surface finishes. Due to the higher melting point and higher mechanical modulus of these solders, this increases the thermo-mechanical stresses in the package. Key emerging research challenges are to identify novel interconnect materials that exhibit potential for addressing these issues, associated with SAC alloys, and provide for lower temperature and stress electronic packaging processes. A few novel materials have been identified, including nano-solders based on Pb-free alloys and electrically conductive adhesives. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements.

For lower temperature flip chip assembly other options under investigation include: Conventional low temperature soldering using the Sn-Bi or Sn-In family of alloys, flip-chip packaging with all-copper connections to replace soldered

copper interconnects[311], and carbon nanotube based first level interconnections. Each of these potential options faces significant challenges. Research and industry consortia engagement is required to demonstrate the feasibility of these materials to address projected packaging requirements

NANOPARTICLE BASED SOLDERS

For many metallic nanoparticles, e.g., Cu, Sn, In, Bi, Ga, Au, it has been shown[312] that their melting points and latent heats of fusion decrease with particle size. This behavior is attributed to the surface pre-melting characteristics, due to their increased surface to volume ratio, which is a key factor in determining the melting behavior. Solders based on low-melting point nanoparticles, could be useful for low-temperature electronic packaging assemblies, forming relatively compliant interconnects. However, their current-carrying capability, electromigration resistance, and scalability remain to be understood. For example, it has been demonstrated[313] that SnAg based nano-solders, with an average particle size < 10 nm, showed a melting point reduction from ~225ºC for bulk material to 194ºC. The corresponding 10nm SAC alloy melting point was reduced to 199ºC). The key challenge to synthesizing solder nanoparticles is to prevent oxidation, which can be reduced by surface passivation. Surfactants de-bond/decompose at the low temperatures to form an initial "half-solder joint." The final solder joint can then be formed in the conventional reflow process. While this may meet the needs of some applications that require an initial low temperature solder attach followed by higher temperature cure, most package applications need the lower temperature solder to produce a good solder joint. The key challenge for nanoparticle based solders is to identify novel techniques, including optimizing nanoparticle size and surfactant chemistries to enable a complete low temperature solder joint formation process.

ELECTRICALLY CONDUCTIVE ADHESIVES

Electrically conductive adhesives (or ECAs) represent another family of emerging research material under consideration for low temperature assembly. ECAs contain metallic nano-fillers, typically Ag and Ni flakes, embedded in an epoxy matrix.[314] These embedded materials can be cured at much lower temperatures than solder reflow temperatures, ~175ºC, between the two surfaces requiring the interconnection. Key challenges for implementing isotropic or anisotropic ECAs include: Unstable contact resistance, due to formation of metal hydroxide or oxide on the nano-flake surfaces during aging, poor impact performance, lower electrical and thermal conductivity, poor current carrying capability, and metal migration compared to Pb-free solders. Additionally, materials innovation is needed to improve drop strength, (improved polymer adhesion), electro-migration resistance, integration compatibility that enables a scalable, reliable package level interconnection technology.

POLYMER MATERIALS FOR FUTURE PACKAGING

Polymers are used in a wide number of assembly and packaging applications including as adhesives for a wide range of applications, underfill materials, molding compound, thermal interface materials, and others. These polymers must protect the integrated circuit and interconnects from mechanical, thermal, and environmental stresses while providing the required functional performance through the life of the product. In addition, these materials must have one set of properties during application, a different set in process, and then the final product properties. Unfortunately, many of the properties are coupled with current materials, so adding a material to change one property often has a detrimental effect on other properties. A critical challenge is to identify materials additives that can modify polymer properties independently.

PACKAGE POLYMER PROPERTIES

New packaging related polymers are needed to meet the requirements of future technologies. For most applications, these polymers primarily serve as an adhesive layer that provides moisture protection and mechanical properties including coefficient of thermal expansion (CTE), modulus, fracture toughness, and adhesion to other materials. Additionally, it also must provide application specific properties such as dielectric constant, for high κ and low κ applications, electrical resistance, and thermal/ electrical conductivity. If low thermal resistance is required for a composite polymer, the interfacial thermal resistance between the thermal conducting materials and the other materials interfacing to the polymer must be very low.

Future underfills will need to accommodate smaller gaps between the chip and package. Capillary underfills will require polymers with lower viscosity in application, good wetting to multiple surfaces, low shrinkage during cure and low CTE (10-14 ppm) post cure. Current approaches to achieving the low CTE often increase viscosity, but nanomaterials may offer the opportunity to add small amounts of fillers, and meet the CTE without increasing viscosity. Research is needed into techniques to effectively integrate nanomaterials into epoxy systems and modify CTE without degrading viscosity in application and adhesion. Alternate approaches to underfill such as wafer level adhesives need to have low CTE and good adhesion to solder, polymers and the other materials, but not shrink upon cure. Again research is needed in integrating nanomaterials that will enable low CTE, low shrinkage thermoset polymers and not interfere with solder joint formation.

Molding compounds will need to support a wide range of applications from high performance stacked chips to flexible electronics, such as smart cards. With increased use of flip chip molding compounds will be needed to underfill the gap between the chip and substrate as well as encapsulating the chip, so viscosity in application and adhesion to all surfaces will be important. Innovation is also needed for materials with designed properties including flexibility to avoid cracking from bending stresses with thin silicon, compatible CTEs between silicon and the flexible substrate, and strong adhesion to IC materials.

For wafer or die level and stacked chip packaging, adhesives are needed to provide a stress absorbing attachment between silicon and other die materials, and exhibit a low shrinkage, low CTE, low modulus and low dielectric constant and in some cases has a high lateral thermal conductivity. Again, research is needed integration of nanomaterials into thermoset polymers to independently modulate mechanical, thermal and moisture absorbance.

Nanotechnology provides benefit in terms of multi-functional nano-composites, with simultaneous and step-function improvements in properties and novel property modifications.[315] Such composites may find potential applications in future mold compounds, under-fills, or die attach materials. Decreasing particle size helps to lower the composite CTE.[316] Another benefit of nano-composites is their potential for decoupling stiffness and toughness. However, persistent challenges with processing and dispersion (intercalation-delamination) remain barriers to nanocomposites realizing their full potential. Filler surface chemistries, such as: epoxy, acids, amines, and siloxanes onto silica-like fillers can play crucial role in achieving in matrix filler intercalation and dispersion. Once the fillers are well dispersed and intercalated (bonded) with the matrix, they act as temporary cross linkers during deformation, thereby improving toughness and preventing or diverting cracks. If well bonded, the fillers may move with the polymer chains during deformation. While the resulting nano-composites express only a marginal increase in modulus, they also exhibit a significant increase in toughness, with lower CTE. The addition of oxide fillers has shown increase in composite surface energy, thereby improving adhesion. However, research is needed to understand the fundamental factors that enable this improvement in adhesion.[317] The grand challenge, as identified in the 2007 ITRS ERM chapter, is the concurrent requirements of achieving low CTE, low modulus, high fracture toughness, high adhesion, and lower moisture absorption.

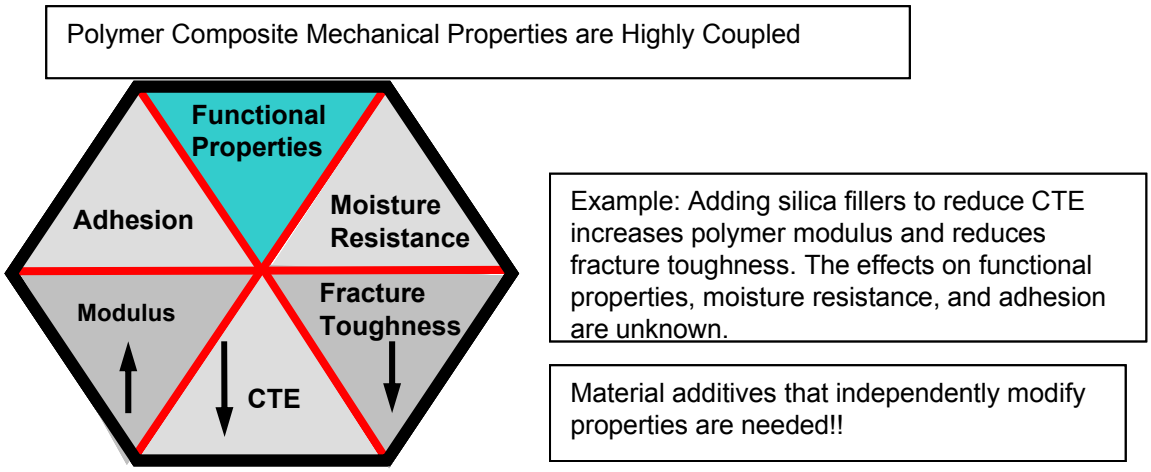

Figure 3 Polymer Composite Materials' Coupling Example

Package polymers must simultaneously meet mechanical and moisture resistance requirements and functional properties such as resistance, dielectric constant, thermal conductivity. In current approaches, the properties are highly coupled so addition of fillers to decrease CTE is often detrimental to the other properties. Research is needed to determine whether nanomaterials can be added into the polymers to independently modulate many of these properties.

LOW DIMENSIONAL MATERIALS FOR FUTURE PACKAGING

NANOTUBE INTERCONNECTS

The 2007 ITRS ERM chapter introduced low-dimensional materials, such as carbon nanotubes, as potential candidate materials for electro-migration resistant chip interconnects. However, several key challenges were identified for these materials, such as: 1) Packaging compatible assembly processes; 2) demonstrating the required electrical resistance and reliability, including interface electro-migration, and 3) low assembly cost.

While the challenges remain daunting, research is underway to explore two potentially packaging compatible nanotube assembly methods, which include: 1) *in situ* low temperature (< 300°C) nanotube growth, or 2) remote synthesis of nanotube arrays, which are subsequently transfer to substrate. In the first approach, growth temperatures as low as 350-500°C have been reported.[318] The second approach suffers from nanotube array collapse during transfer, especially during the fabrication of fine pitch FCBGAs.

Another challenge is the high contact resistance associated with nanotubes. Certain metals, such as Pd, Rh are known to lower contact resistance with nanotubes, by matching of work functions.[319] Modeling reports[320] suggest that high nanotube densities must be achieved to satisfy the projected contact resistance requirements. Thus, future efforts need to be geared towards growth of high density nanotube arrays, with low contact resistance metal contacts.

NANOTUBES FOR PACKAGE THERMAL MANAGEMENT

The 2007 ITRS ERM chapter also introduced nanotubes and other low dimensional materials as potential thermal management candidates for future package applications. The intrinsic high thermal conductivity of nanotubes justifies their consideration as potential candidates for thermal interface materials. The key challenges that must be overcome for this material to be viable include: 1) Lower thermal contact interface resistance and 2) a high density of nanotubes that provide a direct thermal path between the heat source and the heat sink. Nanotube density and adhesion with Si or Silicon dioxide, through a metallic interface, needs to be optimized for the best thermal performance.

ADVANCED THERMOELECTRIC NANOMATERIALS FOR PACKAGE THERMAL MANAGEMENT

Thermoelectric cooling offers the potential for satisfying projected thermal management requirements of advanced semiconductor packages. The thermoelectric cooling ability is estimated by the non-dimensional figure of merit ZT that has hovered below 1 until recently when a spike has been seen in semiconductor nanostructures.[321] Values of ~1.3-1.6 have been reported for PbSeTe/PbTe quantum dot superlattices.[322] The highest reported ZT (~2.4) so far has been in nanostructured thin-film superlattices of Bi_2Te_3 and Sb_2Te_3[323] and devices based on these systems were recently demonstrated.[324] While these new nanomaterials show some promise for enabling extensible thermal management of semiconductor packages significant challenges remain. These include contact parasitics that emerge whenever a device is fabricated and which severely degrade the intrinsic cooling potential of these nanomaterials.

HIGH PERFORMANCE CAPACITORS

High speed, high power density capacitors are needed for power isolation in high performance logic. Future power isolation capacitors need to work at GHz frequencies and deliver high amounts of current quickly. Materials needed to support this are high dielectric constant materials, low resistance interconnects, and fabrication of the structure with a small spacing between the electrodes. The highest dielectric constant materials are complex metal oxides which are discussed in the Device Materials Section and have challenges with cation and oxygen vacancies reducing reliability. Nanotubes and nanowires described in the interconnect section have potential as low resistance interconnects, but the largest issues will be in developing low cost techniques to assemble the electrodes in close proximity with a low resistance structure. Potential options would be to use directed self assembly of the electrode materials and the high dielectric constant capacitors, but this would require the materials to also have low defect densities when integrated.

ENVIRONMENT, SAFETY, AND HEALTH

Over the past decade, the introduction of new materials has enabled the semiconductor industry to continue increasing the density of transistors and increasing their performance through "equivalent scaling." Examples of this include the introduction of Cu and low κ interconnects to increase interconnect speed and the introduction of high κ gate dielectric with new gate electrodes to extend transistor performance while reducing power consumption. The introduction of these new materials into the integrated circuit also required the use of multiple new materials in the manufacturing process. The semiconductor industry faces many significant challenges to continue delivering higher density, higher functionality technologies in the future and very few material options could provide solutions. Since the difficulty of introducing a new material into a technology is high, the new material would need to provide a significant performance advantage over evolutionary approaches. However, in some cases all of the options have known or unknown toxicological behavior. In cases where the need for a solution is compelling and toxicological behavior is unknown, the need for research to characterize potential acute toxicity and chronic effects will be highlighted. As the materials become more viable as technology options, our industry needs to better understand technical and ESH properties and behavior so mitigation and management strategies can be developed. As critical ERM get closer to potential insertion, the ESH TWG will assess the viability of strategies for managing potential issues for these materials.

To support the ESH technology work group and the research community in identifying when new materials are becoming more viable, the earliest potential insertion timing table has been developed in collaboration with the other technology work groups. As can be seen in Table ERM12, earliest potential time varies greatly depending on the application with potential applications in 3-5 years for carbon and metal nanotubes, oxide nanoparticles, macromolecules, and self assembled materials. Assembly and Packaging has potential applications for carbon and metal nanotubes in this timeframe in embedded applications. Oxide nanoparticles may have application as novel photoresist additives in Lithography, and as a package polymer additive in Assembly and Packaging. Novel macromolecules have potential for application in process chemicals and photoresist in Lithography. Self assembled materials could also be used in embedded package applications. These are viewed as the potential earliest insertion times for the ERM. This table will be updated in future ERM Roadmaps.

Table ERM12 ITWG Earliest Potential ERM Insertion Opportunity Matrix

METROLOGY

Metrology is needed to characterize the atomic and nanoscopic 3D structure, composition, and properties of emerging research materials (ERM). Also needed are non-destructive methods for characterizing the local nanoscopic structure of embedded materials, interfaces, and defects, as well as platforms that enable the simultaneous measurement of complex nanoscopic properties. For additional discussion on ERM related metrology, see the *Metrology for Emerging Research Materials and Devices section* in the *Metrology chapter*.

CHARACTERIZATION AND IMAGING OF NANO-SCALE STRUCTURES AND COMPOSITION

The integration of a wide range new and complex functional materials into nanometer scale structures, requires enhanced metrology tools to image their atomic structure and composition. These materials include: III-V semiconductors; low atomic weight (z) materials, such as carbon nanotubes and graphene; nanostructured materials, such as heteronanowires; dielectrics; metal interconnects; spin materials, such as dilute magnetic semiconductors; complex metal oxides; and doped transition metal oxides. Nondestructive in-situ measurement methods are needed that offer real time characterization of their nanostructure, composition, and orientation. Such tools are critical for establishing correlations between a material's nanostructure and its macroscopic properties. For example, there is a need for precise doping control at the source and drain interfaces, as well as within the channel region. Within a few years, a few misplaced dopant atoms will induce significant variability in the device performance of nanoscale circuits and systems. Such tools will be needed to assess the extent to which emerging nanofabrication methods, such as directed self assembly or deterministic fabrication, enable tighter control of the structure and functionality of novel nanodevices and circuits.

METROLOGY NEEDS FOR INTERFACES AND EMBEDDED NANO-STRUCTURES[325, 326]

The ERMs under consideration for device or interconnect applications will be integrated with other materials that form interfaces. It is becoming increasingly critical to understand and control of their atomic structure, composition, interfacial bonding, defects, stress, and effect on nanoscopic properties. For embedded contacts and other heterostructures, the ability to nondestructively characterize the structural and electronic properties and stability of these interface structures is important and necessary, but very difficult to achieve. Characterization of the nanoscopic structure, atomic architecture, as well as the electronic, polarization and electronic states at these interfaces will enhance our understanding of whether interface states are affecting their operation. Current subsurface / buried interface imaging and measurement techniques are marginally adequate for understanding interface phenomena. Many of these techniques are destructive, since they require cross-sections. The challenge of understanding these environmentally sensitive properties requires the development and application of appropriate nondestructive 3D characterization tools and methods. In addition, as alternate state variables are explored for beyond CMOS applications, there is a need for correlated, multimodal microscopies to maximize information return from nanoscale objects and interfaces. For these systems, multiple measurement techniques may be applied, simultaneously or asynchronously. In addition, modeling is needed to separate the probe-specimen interactions and resolve the unperturbed interface structure and properties.

CHARACTERIZATION OF VACANCIES AND DEFECTS IN NANO-SCALE STRUCTURES[327]

The properties of most nanostructured materials are dramatically affected by small concentrations of vacancies and defects. Therefore, the ability to accurately map vacancies, defects, dopant atoms, and interface structures may be needed to enable future emerging device options. In the case of CMOS or alternate channel transistors, statistical changes in dopant distribution cause variations in threshold voltage distributions. When interfaces are formed between materials,

bonds can be broken and defects generated, which can diffuse in the structure. In the case of graphene and carbon nanotubes, a local C-H bond or missing carbon atom can change the electronic properties of the system. Alternatively, functionalization also can result in the formation of vacancies, or rehybridization of the carbon that introduces states in the gap. Such material perturbations can dramatically change these materials' electronic or thermal properties. Complex metal oxide properties, including electrical, ferroelectric, and ferromagnetic, also are strongly affected by the presence and location of oxygen vacancies, since they create local distortions of the crystal structure that can break symmetry and induce different and uncontrolled electronic states. In complex metal oxide heterointerfaces, the interface carrier concentration can be changed by the presence of oxygen vacancies. The challenge will be to detect the positions of small concentrations of vacancies and defects in nanometer scale structures. In addition to the identified need for developing enhanced microscopy capabilities, other physical measurement methods also should be advanced so that the relationship between defects and properties can be measured, quantified, and understood.

WAFER LEVEL MAPPING OF PROPERTIES OF NANOSCALE ERM[326, 328-331]

The ability to measure and map properties of a large number of low-dimensional materials is needed to support improvements in material synthesis for a wide range of potential applications. Such synthetic advances depend on the reproducible production of high-quality materials, and rapid methods for characterizing the structure, purity, and properties of such samples. For example, some methods for growing graphene tend to yield varying numbers of graphene layers[329], and samples with various defects.[330] While spectroscopic techniques have distinguished between graphene monolayers, bilayers, and bulk graphite[331], rapid predictions of the number of graphene layers, or the presence of defects are needed. Robust fabrication requires an ability to map bandgap distributions, preferably in-line, across a wafer, to identify those regions with properties outside of the target, and assess the interaction of graphene with the underlying substrate. While some techniques, such as Raman spectroscopy, fluorescence and other spectroscopic techniques, are sensitive to the local chemical environment, alternative options are needed to support the local electronic characterization of these materials. Emerging characterization methods require further advancements that are appropriate for specific potential application opportunities, especially with respect to improving the balance between measurement speed, accuracy, and precision.

Metrology Needs for Simultaneous Spin and Electrical Measurements[332-337]

Several beyond CMOS devices use spin control as an alternate state variable. This set of devices includes spin transfer torque magnetic random access memory (MRAM), nanoscale spin transistors, spin wave devices, hybrid-ferroelectric/ magnetic structures, and other spin-based logic concepts.[332] The characteristics and properties of these types of emerging nanoscale spin-based devices and materials differ from those in conventional CMOS devices, which are based on the transport of charge. Specific spin materials characterization challenges include the atomic scale imaging of domains, the dynamics of domain wall motion, the interface conditions needed for efficient and fast spin injection from ferromagnetic to semiconductor materials, and the measurement of spin transport and lifetime. Measurement and imaging techniques for magnetic materials characterization have been recently summarized.[336] These techniques include scattering based techniques (neutron, x-ray, electron, and photon) and proximal probe techniques (force microscopies, spin-polarized STM, scanning near-field magneto-optic microscopy). More recently, magnetic circular dichroism (XMCD) has been used to image domain wall motion in multilayer film stacks.[337] Electron scattering methods for domain imaging include Lorentz imaging in the transmission electron microscope and polarization analysis in the scanning electron microscope (SEMPA). Scanning near-field optical microscopy is being developed to measure Kerr rotations at the nanometer scale. Work function lowering effects are being measured by photoelectron spectroscopy.

METROLOGY NEEDS FOR COMPLEX METAL OXIDE SYSTEMS[338-343]

Correlated oxide systems, such as multiferroics, have competing and coupled charge, spin, orbital and lattice degrees of freedom, which drive the formation of new electronic and magnetic phases. These materials have the potential to enable new device concepts. Novel memories based on spin logic could couple electric and magnetic spin alignment. It has been shown that domain walls can possess functionalities, such as electrical conductivity, not inherent in the parent multifunctional material.[338] For these electrically conducting interfaces to be useful, factors that drive their nucleation and positioning must be understood and controlled reproducibly.[339] Piezoforce microscopy may be useful for characterizing static and dynamic properties of ferroelectric and piezoelectric materials at the nanometer scale.[340] The coupled phases have been found to be sensitive to cationic disorder and vacancies. Metrology options are needed to characterize these phases, their transition dynamics, and their correlations with local electric, magnetic, and orbital order.

METROLOGY FOR MOLECULAR DEVICES

Metrology capabilities are beginning to enable an understanding of transport through individual molecules and molecular interfaces. These tools include inelastic electron tunneling spectroscopy[344], and backside FTIR[345] to study vibrational

states, transition voltage spectra[346], STM, Conductive AFM, and Kelvin Probe AFM. However, additional research is needed to develop new metrology concepts, such as nondestructive, *in situ*, 3D methods that can characterize contact interactions with molecules, as well as the electronic properties of the embedded interfaces and molecules.

Metrology Needs for Macromolecular Materials[347-355]

New families of designed macromolecules and corresponding material characterization methods are needed to satisfy projected long term patterning requirements. For example, nanoimprint lithography (NIL) is emerging as a potential patterning solution beyond 22 nm. This technology faces several performance challenges related to the templates, release layers, and resist and imprinted functional materials. New metrologies are needed to assess projected critical materials requirements, such as pattern fidelity, distortions and defects, shear stresses and pattern collapse, adhesion and release behavior.

METROLOGY NEEDS FOR DIRECTED SELF-ASSEMBLY[356-363]

For directed self assembly to be viable as a lithography extension or to assemble nanostructured materials in predefined locations and alignment, metrology is needed to evaluate critical material properties. However, it is difficult to image and characterize local nanoscopic structures within sub-100 nm thick organic films with conventional metrology tools. For block co-polymer based directed self assembly to be a viable potential lithographic solution, robust non-destructive nanoscale measurement methods are needed. Specifically, research is needed to enable 3D characterization of phase segregating films. Critical characterization metrics include: feature size, uniformity, line width roughness, location, alignment to existing structures, engineered surface energies, anneal dynamics, and defects, etc.

MODELING AND ANALYSIS OF PROBE-SAMPLE INTERACTIONS

Nanometer scale measurement tools, such as electron microscopes or scanning or optical probes, exhibit significant coupling between the probe and sample states. Significant research is needed to develop methods for decoupling these interactions and to accurately determine nanoscopic structures and properties. Also needed are dynamic sample-probe interaction models for characterizing changes in nanoscale structure, defect locations, and electronic, magnetic, and optical properties. Additionally, algorithms need to be evolved that enable the extraction of actual structures and properties from the coupled signals.

METROLOGY NEEDS FOR ULTRA-SCALED DEVICES[364-367]

New metrologies and models are needed to characterize the performance and reliability of emerging nano-scale devices. Emergent nanoscopic properties will introduce new mechanisms for compromising device performance and reliability. For example, the trend towards increasing percent variability, with scaling, is becoming a critical challenge to achieving robust device attributes and driving the perceived lower limits for device operation. Analog circuits are particularly susceptible to decreasing signal-to-noise ratios. A thorough understanding of the sources of variability and their impact on device noise is critically needed for enabling the successful design and integration of emerging materials into nanoelectronics.[37] This foundational need will drive the development of tools for identifying and characterizing the significant emergent nanoscopic sources of variability and noise in nanoscopic systems.

METROLOGY FOR ERM ENVIRONMENTAL SAFETY AND HEALTH

Metrology is needed to detect the presence and dynamics of nanoparticles in the workplace and in the waste stream.

MODELING AND SIMULATION

With device dimensions reaching 22 nm or below, materials modeling or computational materials science is becoming a critical part of technology development. It is needed to address several components of technology development, which include[368]:

1. *Synthesis to structure and composition*, especially for the interfaces and multi-interface material structures. Since a material's structure determines its properties, it is important to accurately characterize specific a nanoscopic structure and its relations with synthesis.
2. *Properties* of these structures, including the interface physics of state transitions, defects states, etc., as well as selected non-equilibrium properties, such as conductance and mobility,
3. *Probe interactions* with samples to enhance quantification of structure, composition, and critical properties.

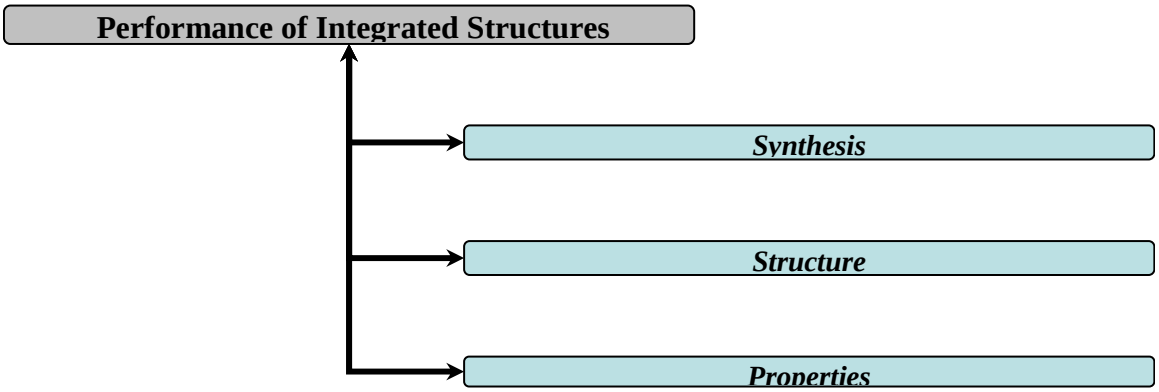

Figure 4 Performance of Integrated Structures

Materials modeling is applied at different levels, based on the accuracy and the end application requirements. There are multiple stages in which materials modeling can provide value in technology development. In the *first* stage, during early material development, the need is to relate structure and chemistry to material properties. Since a material's properties determine its utility in the technology, this is a primary application of material models. In the *second* stage, the models are applied to material improvement, where they are used to optimize structure, composition, and purity. In the *third* stage, models are used to relate material properties to the functional properties of the device. The models at this stage, in conjunction with experimental observations, are used to optimize synthesis and integration.

Material behaviors directly correlate with their electronic structure and lattice physics. These correlations apply to charge-based and non-charge-based technologies, as physical and chemical effects in these dimensions are directly related to the electronic structure. Physical modeling and numerical simulations are critical, as they:

1. Explain observed phenomena
2. Predict new phenomena
3. Direct experimental studies to desired outcomes
4. Interpret metrology

In addition, they provide a fundamental understanding of the mechanistic dynamics and the interactions between processes and materials.

ERM material's application require a fundamental understanding and characterization of synthesis, structure, and properties. This is the natural logical flow of interactions for integrating newer materials into emerging systems, whether for devices, interconnects, or packages. The choice of synthetic method and reactions conditions determine the structure and composition of the engineered materials. This structure determines the material's properties and performance. As can be seen in the following figure, models must span multiple scales and need to be simulated, using appropriate assumptions. The key intent of material simulation is to identify and quantify chemical parameters at atomic and nanoscopic levels for clusters of atoms or interfaces, as well as thin film dimensions that modulate the behavior of the integrated devices.

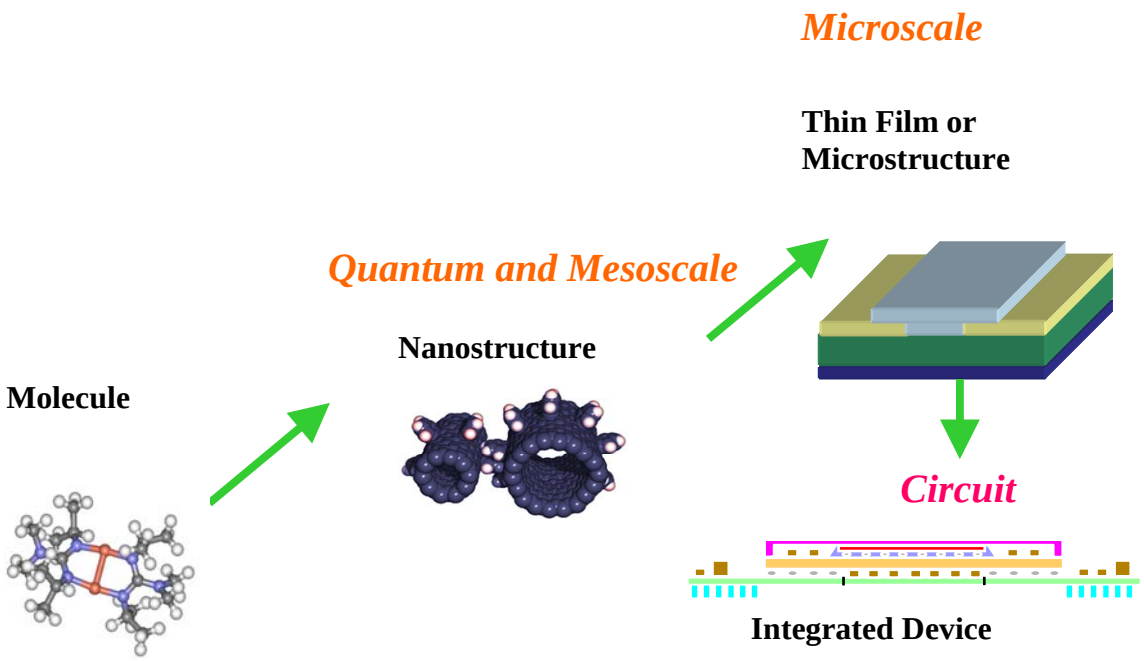

Figure 5 *Multi-scale Perspective in Nanotechnology where Materials Form an Important Role at Different Levels.*

The complexity of materials modeling in nanotechnology is increasing, due to increasing complexity from a variety of factors, which include:

1. *Combinatorial System*—Number of materials has continued to increase with each technology.
2. *Size*—Most of the devices have dimensions close to material domain sizes (e.g. grain size, thin film thickness).
3. *Topography*—Non-planar material structures modulate properties and behavior, due to different materials at multiple interfaces.
4. *Topology*—of the nanostructures and molecules.

SYNTHESIS

The ability to predictively model synthesis and determine the effect of process conditions on the resulting material is important for understanding whether a proposed nanostructure can be achieved. Synthesis determines the structure and composition of materials and thin films. To predict material properties, characterization and physical modeling of the relevant structures are needed. From a modeling perspective, a key requirement is to understand the roles and mechanism of precursors and the growth process on the specific structure resulting from the synthesis. Controlling the morphology of the nanoscopic material requires detailed information on phase stability and the dynamics of atomistic processes. In small nanoscale systems, in which dimensions may not be significantly larger than the range of interatomic interactions, classical thermodynamic concepts, such as extensive and intensive properties, may no longer be valid.[369, 370] It may be critical to develop of a theory of phase transitions in finite size systems for understanding the dynamics of phase transition and its role in controlling the nucleation and growth of certain nanoscale materials. Multiple techniques are used to model different aspects of material synthesis. Density functional theory typically applies to quantum level attributes, Monte Carlo techniques or molecular dynamics are used to model material dynamics, and continuum models help to simulate the processes.[371, 372] Given the limited size of problems that can be solved, a combination of techniques that span different length and time scales are needed to model structures effectively. More details are covered in the section on Modeling and Simulation.

STRUCTURE AND PROPERTIES

The ability to model and simulate properties of nanomaterials, with different compositions, structures, and defects, is critical to understanding structural factors that control properties. The material properties themselves are determined by

the atomic and electronic structure of the condensed matter. Any solution of the Schrodinger equation for electrons in a realistic macroscopic system is generally achieved using one of two simplified techniques: 1) a single particle approximation and/or 2) multi-scale techniques, with distinct formalisms representing different scales. Since structural dimensions are currently at 45 nm or below, the materials properties at this scale may behave differently than those for the material that is integrated into the bulk, due to size and interface effects.

One of the practical difficulties in the application of material's modeling is the inability to scale to larger size domains efficiently. Most of the full quantum simulations or *ab-initio* simulations can be done for smaller systems, i.e., up to 1000 atoms, which correspond to `30 cubic nanometers. This poses an equation solvability challenge for practical applications. Consequently, , Density Functional Theory (DFT) represents the most widely used technique in which the 3N dimensional system is reduced to three dimensional ground state problems.[373, 374] Several approximations are used to increase the applicability of DFT methods for most semiconductors and interconnect materials.

On the other hand, strongly correlated electron state materials (e.g., Mott transition, spin-orbital coupling) are being evaluated for beyond CMOS logic device and new memory devices. These materials can't be modeled with DFT, due to many body effects. As a result, many-body theories are entering mainstream applications.[375, 376, 377, 378] These techniques model the equilibrium properties by including correlation effects, in terms of self-consistent formalisms based on cluster theories. For nonequilibrium properties, in which the system is open, techniques include solutions of the dynamic Schrodinger equation, time-dependent density functional theory, and a non-equilibrium Green's function. For modeling spin, both collinear and non-collinear, a variety of methods are used, which includes solution of Dirac's relativistic equation[379]. All these techniques are computationally intensive and are limited in the size of the physical problems to which they can be applied. Currently, they can't predict longer range interactions, such as nanoscale phase segregation.

Semi-empirical models for extending to larger systems of million atoms are characterized by a variety of techniques in which interaction energies are defined by different potentials. The applicability of atomistic models can be increased to over 100 million atoms by using more semi-empirical characterizations, like force fields. Some of the semi-empirical methods used for modeling materials include following:

1. Classical molecular dynamics, which are based on interaction potentials formulated from quantum simulation.
2. Kinetic Monte Carlo methods, which use energies estimated from *ab initio* methods, are used to simulate time-dependent states of a system.
3. Tight binding methods, in which the quantum methods are approximated by parameters the enable scaling to large numbers of electrons and atoms.

Although the techniques have been demonstrated to be useful in certain applications, they still need to be scaled to meet realistic system sizes (~100 nanometers) and physical times (microseconds or seconds).

Despite recent advances, theory has many limitations that gate applicability to systems of practical interest for quantitative correlations. Current applications include: equilibrium energies, density of states, reaction rates, effects of defects in parts per thousand, and transport within nanostructures with interfaces. At the quantum scale, the current applicability of available models is rather limited. Major issues that need to be addressed in the modeling are:

1. Extension to larger scales for equilibrium calculations and assessing the temperature dependence of properties and processes.
2. Ability to model transition and inner transition metals with d and f orbital electrons.
3. A more generalized extension for accurate determination of band gaps and excited states.
4. Strongly correlated systems require model development to explain the interaction between spin, charge, and lattice dynamics and longer range interactions, such as phase separation.
5. Coupling of electronic structure predictions to non-equilibrium processes, such as transport, are necessary since most of the devices operate in non-equilibrium environments.
6. Lattice physics includes atomic and ionic responses to multiple externally applied fields. This topic needs to be extended to include phonon dynamics and energy transport in nanostructures with interfaces.
7. Extensions of molecular dynamics and Monte Carlo methods to simulate from femtoseconds to microseconds or longer to emulate realistic synthesis and transport.

METROLOGY AND CHARACTERIZATION

As mentioned previously, when new material properties are characterized, models must be developed to guide synthesis and further enable exploration of new structures and more complex interactions between materials. The establishment of an experimental database, with results from well-characterized structures, could accelerate the development of more

accurate full *ab initio* and self-consistent reduced models. More quantitative material property mapping at the nanometer-scale requires development of models to probe interactions of nanostructured materials. Improved structure and property mapping for more accurate TEM, AFM, Conductance AFM, Kelvin Probe AFM, Magnetic Force Microscopy (MFM) and other new techniques could improve the development of nanometer scale material models.

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