INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2009 EDITION

INTERCONNECT

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INTERCONNECT

SCOPE

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit, along with providing necessary power and ground connections. The process scope begins at the contact level with the pre-metal dielectric and continues up to the wirebond pads, describing deposition, etch and planarization steps, along with any necessary etches, strips and cleans. A section on reliability and performance includes specifications for electromigration and calculations of delay. Expanded treatment of Emerging Interconnect and 3D integration are new features.

INTRODUCTION

The Interconnect chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap for Semiconductors (ITRS) emphasized an ongoing change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low-κ dielectric introduction for microprocessors (MPUs) and application-specific ICs (ASICs) was one of the central issues for the 2003 ITRS Interconnect area. The 2005 ITRS showed the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A crosstalk metric was also introduced in 2007. Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, radio frequency (RF), or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuit/system functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips, despite further scaling of feature sizes. Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant indicated by the ITRS has been problematic. Fluorine doped silicon dioxide (κ = 3.7) was introduced at 180 nm, however insulating materials with κ = 2.7–3.0 were not widely used until 90 nm. The reliability and yield issues associated with integration of these materials with dual damascene copper processing proved to be more challenging than expected. The integration of porous low-κ materials is expected to be even more challenging. Since the development and integration of these new low-κ materials is rather time invariant, the anticipated acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable κ to later technology generations. The various dielectric materials that are projected to comprise the integrated dual damascene dielectric stack for all years of the roadmap are depicted in the Dielectric Potential Solutions figure. The range of both the bulk κ values and effective κ values for the integrated dielectric stack are listed in the Technology Requirements *Table INTC6*. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge. (For a more thorough explanation, the Appendix illustrates the calculation of the effective κ for various integration schemes.) The imminent convergence of the M1 pitches for MPU and DRAM, expected by 2010, negates the need to identify a single technical product driver but technical specifications are included for both high performance logic and DRAM.

WHAT'S NEW FOR 2009?

- The Technology Requirements Table (INTC6) has been substantially revised and reorganized and divided into
  - General requirements – e.g., bulk resistivity and dielectric constant
  - Level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-k roadmap – slight slowdown
  - New range for bulk κ
  - Air gaps moved out of emerging sections – now considered mainstream
  - Air gaps expected to be the solution for κ_{bulk} <2.0

- Atomic layer deposition (ALD) barrier processes and metal capping layers for Cu are lagging in introduction – needed to meet sub 1 nm specifications
  - Hybrid barriers containing ruthenium are proliferating
- J_{max} current limit model exhibits a width dependence – a new reliability concern
- Technology drivers have been expanded to support both traditional geometric scaling and equivalent scaling
  - Requirements for CMOS-compatible equivalent scaling are highlighted in an expanded *Emerging Interconnect Solutions* section along with a new first principle consideration of interconnect properties for new (non-FET) switches
- Design and processing of three-dimensional chip stacking through the use of high-density through silicon vias (TSVs) is a key focus area to address delay and power concerns and a new TSV table has been introduced

INTERCONNECT ARCHITECTURES

3D INTERCONNECT ARCHITECTURES

INTRODUCTION

New developments in electronic system integration look increasingly to the third dimension for a variety of reasons, such as miniaturization, heterogeneous integration, improved circuit performance and lower power consumption. A broad variety of technologies is proposed by all players in the electronic manufacturing supply chain (IC foundry → wafer level processing (WLP) → semiconductor assembly and test (SAT) → printed circuit board (PCB) → assembly…), often blurring the traditional interfaces between them.

In order to come to a clear vision on roadmaps for 3D technologies, it is important to come to a clear definition of what is understood by 3D interconnect technology and to propose a classification of the wide variety of technologies. This definition should capture the functional requirements of 3D technology at the different hierarchical levels of the system and correspond to the supply chain manufacturing capabilities.

3D-INTERCONNECT TECHNOLOGY DEFINITIONS

When breaking down any electronic system into its basic components—the transistors, diodes, passive circuit elements, MEMS, etc.—we observe that electronic systems consist of two parts: thebasic components and the highly complex interconnect fabric linking them. This interconnect fabric is organized in a hierarchical way, from narrow short interconnects between basic elements to longer and larger interconnects for interconnecting circuit blocks. For integrated circuits with well-defined local, intermediate and global interconnect layers, on chip circuit-hierarchy is organized from transistors to logic gates, sub-circuits, circuit-blocks, and finally, bond pad interface circuits. This is also the case for electronic systems as a whole, which typically consist of multiple integrated circuits, passive components, crystals, MEMS, etc., and which also are organized in different levels corresponding to, for example, the IC-package, system-on-package, module, board, rack, level. An example is the classification according to JISSO.[1]

Within a certain level of the interconnect hierarchy, interconnects are essentially routed in a 2D-topology: isolated lines are defined on a surface without crossing each other. Crossing of lines are realized on adjacent interconnect planes. Connections between planes are realized through features, such as vias, plated through holes, pins, solder balls, and/or connectors. These "via" interconnects allow for the 3D stacking of interconnect levels. The combination of basic circuit elements with multiple 2D-interconnect planes is considered a 2D-device, such as the integrated circuit or the printed circuit board.

What is commonly considered a "3D technology" today is a different type of "via" technology that allows for the stacking of basic electronic components in the third dimension, not only interconnect planes. This is the main distinctive feature of 3D integration technologies. It allows for the realization of electronic systems with very high packaging efficiency, measured either per unit area or per unit volume.

3D DEFINITIONS AND NAMING CONVENTIONS

3D Interconnect Technology—technology which allows for the vertical stacking of layers of basic electronic components that are connected using a 2D-interconnect fabric are as follows:

[1] *http://jisso.ipc.org*

- "Basic electronic components" are elementary circuit devices such as transistors, diodes, resistors, capacitors and inductors.
- A special case of 3D interconnect technology is the Si interposer structures that may only contain interconnect layers, although in many cases other basic electronic components (in particular decoupling capacitors) may be embedded.

3D Bonding—operation that joins two die or wafer surfaces together

3D Stacking—operation that also realizes electrical interconnects between the two device levels

3D-Packaging (3D-P)—3D integration using "traditional" packaging technologies, such as wirebonding, package-on-package stacking or embedding in printed circuit boards.

3D-Wafer-Level-Packaging (3D-WLP)—3D integration using wafer level packaging technologies, performed after wafer fabrication, such as flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging, and fan-out reconstructed wafer chip-scale packaging

3D-System-on-chip (3D-SOC)—Circuit designed as a system-on-chip, SOC, but realized using multiple stacked die. 3D-interconnects directly connect circuit tiles in different die levels. These interconnects are at the level of global on-chip interconnects. This allows for extensive use/reuse of IP-blocks.

3D-Stacked-Integrated-Circuit (3D-SIC)—3D approach using direct interconnects between circuit blocks in different layers of the 3D die stack. Interconnects are on the global or intermediate on-chip interconnect levels. The 3D stack is characterized by a sequence of alternating front-end (devices) and back-end (interconnect) layers.

3D-Integrated-Circuit (3D-IC)—3D approach using direct stacking of active devices. Interconnects are on the local on-chip interconnect levels. The 3D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack.

Table INTC1 presents a structured definition of 3D interconnect technologies based on the interconnect hierarchy. This structure also refers to the industrial semiconductor supply chain and allows definition of meaningful roadmaps and targets for each layer of the interconnect hierarchy. [1]

Table INTC1 3D Interconnect Technologies Based on the Interconnect Hierarchy

Level	*Suggested Name*	*Supply Chain*	*Key Characteristics*
Package	3D-Packaging (3D-P)	OSAT Assembly PCB	▪ Traditional packaging of interconnect technologies, e.g., wire-bonded die stacks, package-on-package stacks. ▪ Also includes die in PCB integration ▪ No through-Si-vias (TSVs)
Bond-pad	3D-Wafer-level Package (3D-WLP)	Wafer-level Packaging	▪ WLP infrastructure, such as redistribution layer (RDL) and bumping. ▪ 3D interconnects are processed after the IC fabrication, "post IC-passivation" (via last process). Connections on bond-pad level. ▪ TSV density requirements follow bond-pad density roadmaps.
Global	3D-Stacked Integrated Circuit/ 3D-System-on-Chip (3D-SIC /3D-SOC)	Wafer Fab	▪ Stacking of large circuit blocks (tiles, IP-blocks, memory –banks), similar to an SOC approach but having circuits physically on different layers. ▪ Unbuffered I/O drivers (Low C, little or no ESD protection on TSVs). ▪ TSV density requirement significantly higher than 3D-WLP : Pitch requirement down to 4-16µm
Intermediate	3D-SIC	Wafer Fab	▪ Stacking of smaller circuit blocks, parts of IP-blocks stacked in vertical dimensions. ▪ Mainly wafer-to-wafer stacking. ▪ TSV density requirements very high: Pitch requirement down to 1-4 µm
Local	3D-Integrated Circuit (3D-IC)	Wafer Fab	▪ Stacking of transistor layers. ▪ Common BEOL interconnect stack on multiple layers of FEOL. ▪ Requires 3D connections at the density level of local interconnects.

3D-THROUGH-SI-VIA TECHNOLOGY DEFINITIONS

A wide variety of technologies can be used to realize the 3D interconnect technologies described above. Of particular interest here are the so-called "Through-Si-Via" technologies used for 3D-WLP, 3D-SOC, and 3D-SIC interconnect technologies.

A Through Silicon Via connection is a galvanic connection between the two sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections. The isolation layer surrounding the TSV conductor is called the *TSV liner*. The function of this layer is to electrically isolate the TSVs from the substrate and from each other. This layer also determines the TSV parasitic capacitance. In order to avoid diffusion of metal from the TSV into the Si-substrate, a *barrier layer* is used between the liner and the TSV metal.

Numerous methods have been proposed for realizing these TSV-stacked 3D-SIC and 3D-WLP structures. Common to all these approaches are three basic technology modules:

1. The Through-Si-Via process
2. Wafer thinning, thin wafer handling, and backside processing
3. The actual 3D-stacking process

The sequence of these process modules may vary, resulting in a large variation of proposed process flows, as shown in Figure INTC1.

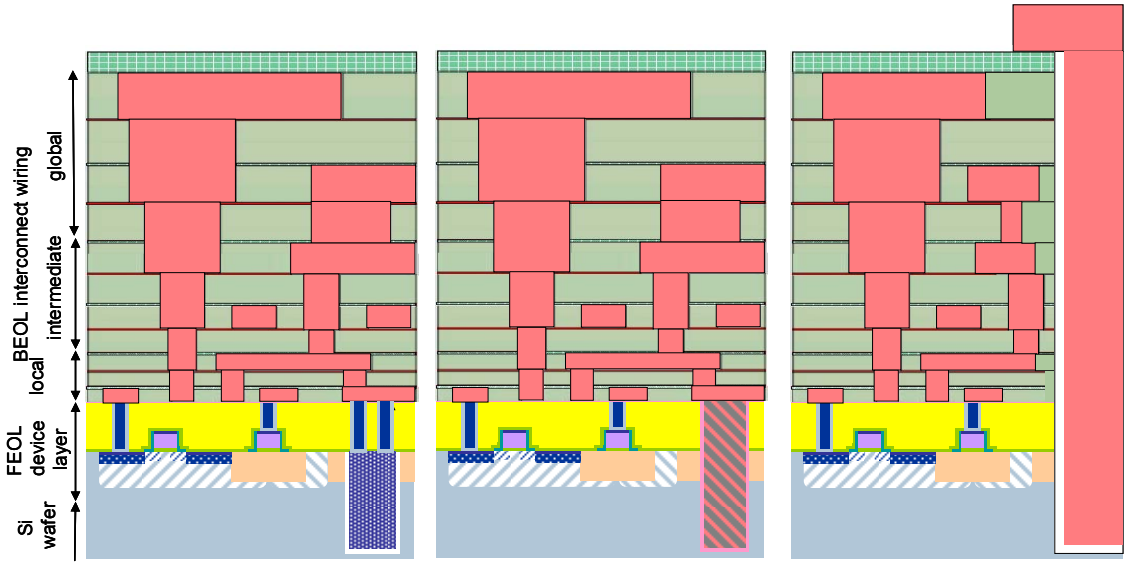


Figure INTC1 Schematic Representation of TSV First, Middle and Last Process Flows

The different process flows may be characterized by four key differentiating characteristics:

1. The order of the TSV process with respect to the device wafer fabrication process: (see Figure INTC1)
   - o *"Via-first"*—fabrication of TSVs before the Si front-end of line (FEOL) device fabrication processing.
   - o *"Via-middle"*—fabrication of TSVs after the Si FEOL device fabrication processing but before the back-end of line (BEOL) interconnect process,
   - o *"Via-last"*—fabrication of TSVs after or in the middle of the Si BEOL interconnect process.
2. The order of TSV processing and 3D-bonding—TSV before or after 3D-bonding[2]
3. The order of wafer thinning and 3D-bonding—Wafer thinning before or after 3D-bonding.
4. The method of 3D-bonding:

[2] *In literature, sometimes TSV processing after 3D bonding is also referred to as "via last" technology. We however define "via last" in relation to the semiconductor wafer fabrication process, which makes the "via last" definition more general and not restricted to TSV after 3D bonding only.*

- Wafer-to-wafer (W2W) bonding
- Die-to-wafer (D2W) bonding
- Die-to-die (D2D) bonding

In addition to these four main characteristics, three secondary characteristics are identified:

- *Face-to-Face* (F2F) or *Back-to-Face* (B2F) bonding
- For "via-last": "*Frontside*" TSVs realized starting from the top surface of the wafer or "*Backside*" TSVs starting from the thinned wafer backside. (The top surface of the wafer being the side with the active devices and back-end interconnect layers)
- Removal of the carrier-wafer before or after bonding (i.e., temporary bonding and permanent bonding).

The generic flow characteristics defined above are applicable to 3D-WLP and global and intermediate interconnect level 3D-SIC process flows. For 3D-WLP TSV technology, the via-last route is the most important and is realized before 3D bonding either as frontside or backside TSV, as shown in Figure INTC2.

The different approaches presented are not only applicable to regular semiconductor devices, but can also be applied to passive redistribution or interposer substrate layers. Key processing technologies for 3D integration are the various temporary or permanent bonding and debonding operations. The requirements for the materials and processes used may vary significantly, depending on the chosen route.

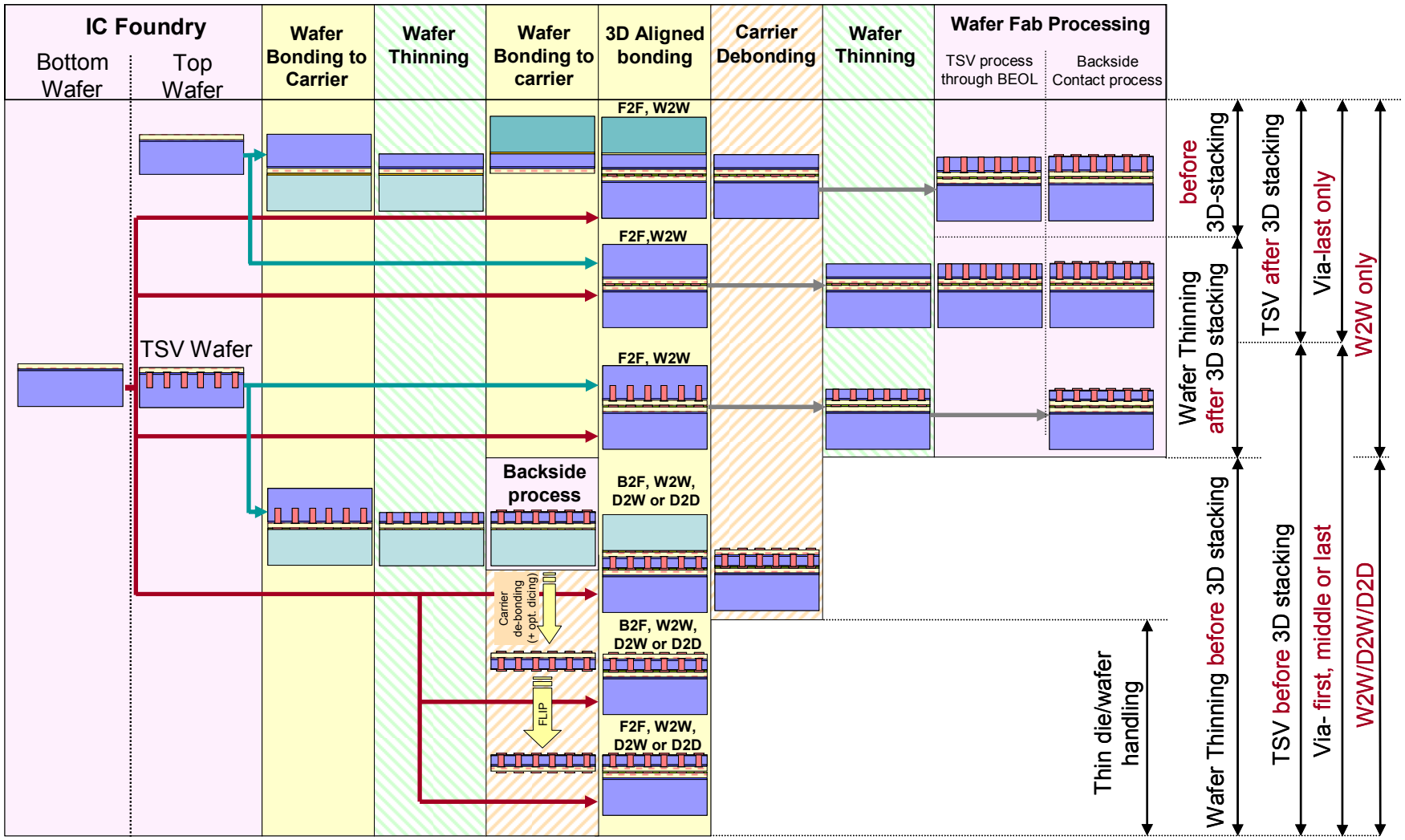


Figure INTC2 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-SIC Technologies[3]

[3] *IMEC*

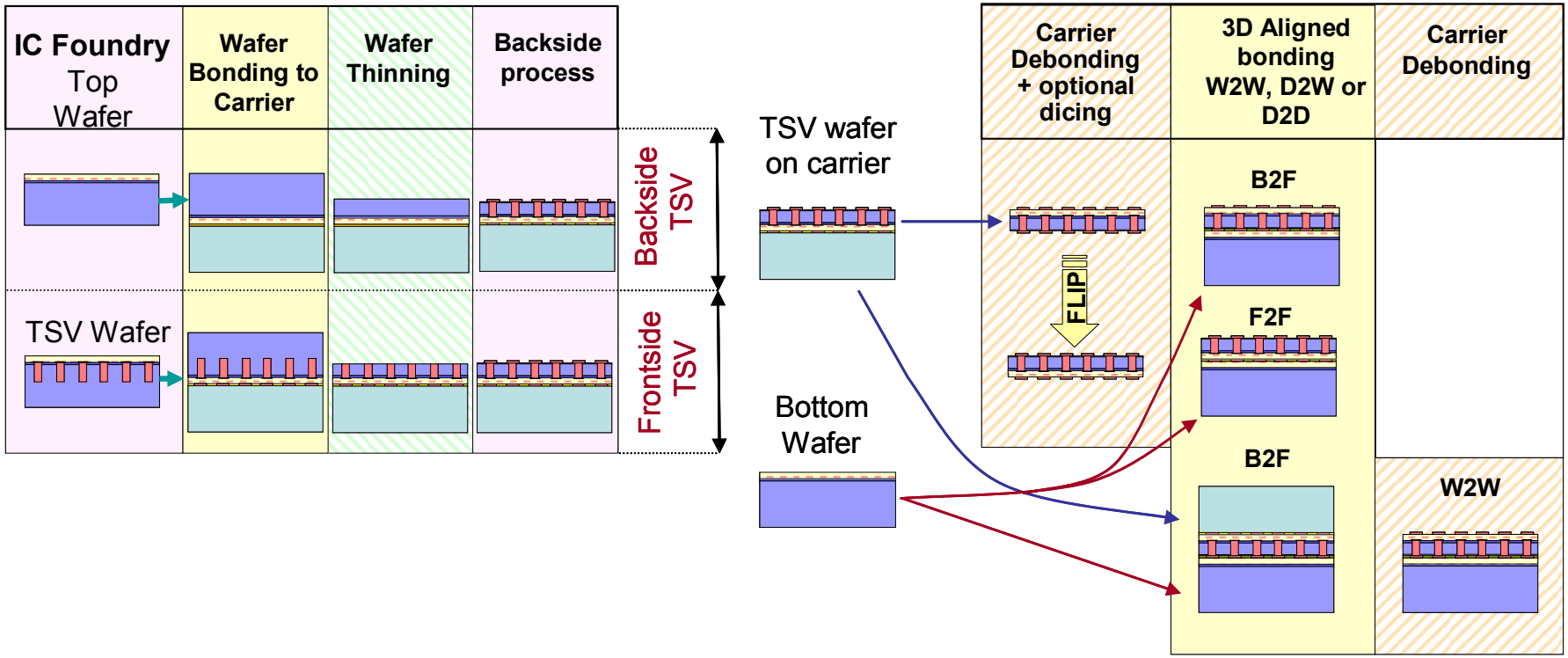


Figure INTC3 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-WLP Technologies[4]

[4] *IMEC*

3D-TSV ROADMAP

Using the 3D interconnect hierarchy and 3D process definitions described above, it is possible to define TSV roadmaps in relation to the interconnect hierarchy they serve.

3D-WLP

This is a 3D-technology for bond-pad level stacking. The 3D-TSV roadmap should therefore follow the chip I/O bond pad roadmap, as shown in Table INTC2.

Table INTC2 3D-WLP Via Pitch Requirements Based on Table ORTC-4—Chip Pad Pitch Trend (µm)

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
1-row wedge-bond pitch (µm)	20	20	20	20	20	20	20
1-row ball pitch (µm)	40	40	35	35	30	30	25
2-row staggered pitch (µm)	45	45	45	40	40	40	40
Three-tier pitch (µm)	60	55	55	50	45	45	45
Area array flip-chip (µm) (cost-performance, high-performance)	130	130	120	110	110	100	100

3D-SIC

This technology is defined at two levels of the interconnect hierarchy.

1. 3D-SIC for connecting at the global interconnect level, e.g., 3D stacking of IP-blocks (3D-SOC). This technology allows for W2W, D2W and D2D stacking. This 3D-TSV process is typically integrated in the Si-wafer fabrication line. The 3D-stacking process is generally done outside the standard Si-process line.

Table INTC3 Global Interconnect Level 3D-SIC/3D-SOC Roadmap

Global Level, W2W, D2W or D2D 3D-stacking	*2009-2012*	*2012-2015*
Minimum TSV diameter	4-8 µm	2-4µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSV depth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch (thermocompression)	10 µm	5 µm
Minimum contact pitch (solder µbump)	20 µm	10 µm
Number of tiers	2-3	2-4

2. 3D-SIC for interconnects at the intermediate level, e.g., 3D stacking of smaller circuit blocks. This technology is mainly a W2W stacking technology.
Both the 3D-TSV process and the 3D stacking are typically integrated in the Si-wafer fabrication line.

Table INTC4 Intermediate Interconnect Level 3D-SIC Roadmap

Intermediate Level, W2W 3D-stacking	*2009-2012*	*2012-2015*
Minimum TSV diameter	1-2 µm	0.8-1.5µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

3D-TSV CHALLENGES

- Large variety of approaches and compatibility with the microelectronic industrial supply chain
  Due to the large variety of approaches for 3D integration, the supply chain, and the possible flows for 3D integration, defining the limits or solutions is beyond the scope of this work. Many of the choices will be dictated by the available capabilities of the various manufacturers in the supply chain and business decisions. Clear definitions of ownership will be critical to the success of the non-IDM business.
- Compound yield—design and test strategies for obtaining high yield 3D-stacked devices
- Design challenges—required tool capabilities for seamless 3D system design
- Interactions between the 3D interconnect and the device packaging and assembly requirements
- Electrical requirements for 3D-interconnects—RLC values for different application regimes
  The main challenge with TSV parasitics is to achieve a low TSV capacitance. The delay and power consumption of 3D-interconnects using TSVs will be mainly determined by the TSV capacitance. This capacitance should be on the order of the capacitance of global interconnect wiring in equivalent 2D-circuits to avoid degradation of circuit performance by going to 3D stacking. This requirement puts an upper limit on the TSV capacitance for a given technologys
- Electrostatic discharge (ESD) protection of the devices during the 3D process sequence
  While 3D promises a dramatic increase in the number of I/O on a layer of Si, these implementations lead to a corresponding increase in the number of circuit elements exposed to ESD. The fine pitch of these new tier-to-tier I/O limit the Si area available to provide active ESD protection. Thus, the design and manufacturing of 3D devices require that attention is paid to the protection of circuits from ESD.
  3D manufacturing brings new sources of ESD during such steps as wafer handling, TSV etch, TSV liner, TSV fill, bonding, debonding and stacking. While little is currently known about the level of possible ESD damage these new steps may generate, every effort should be made to reduce ESD in 3D manufacturing. This is required to keep the size (cost) of ESD protection of 3D circuit elements to a minimum. Once the 3D structure is fully integrated, ESD protection is no longer required unless the 3D structure is part of an external path for I/O/P or G. Thus, any ESD protection for internal 3D elements will be a liability adding to the active power and reducing circuit performance.
- Cost of ownership
- Factory integration of processing using bonded and/or thinned wafers
  Backside processing of bonded and thinned wafers is required in many of the process flows described above. This presents a number of manufacturing and factory integration challenges. In many cases, these wafers will deviate from the SEMI M1.15 spec for 300 mm wafers. This spec covers such items as wafer diameter, thickness, notch, and edge bevel.[5] This standard is referenced by other SEMI standards that deal with FOUPs (E47.1), FOSBs (M31), Load ports (E15.1), and Wafer identification (T7).[6] Depending on the specific 3D processes used, bonded and thinned wafers may be in violation of several of these specs. Also, introducing bonded and thinned wafers into a fab requires ensuring that they can be safely re-introduced into the line without causing contamination or added particles, and qualifying them on each of the tools in the manufacturing flow for both wafer transport issues and tool-specific processing issues. Examples include possible hardware and/or software adjustments for handling thicker wafers and accommodations for the different edge zone.
- Particles and issues of cross-contamination
- Advanced process control requirements
- Environmental, Safety, and Health (ESH) regulation concerns
  Carbon emissions regulation—carbon footprint impact to the environment given the significantly larger volume of patterning feature sizes that require high chemical usage (e.g., SF_6)

[5] *M1.15. SEMI M1.15, Standard for 300 mm Polished Monocrystalline Silicon Wafers (Notched)*
[6] *E47.1. Mechanical Specification for FOUPS Used to Transport and Store 300 mm Wafers, 1997.*

PASSIVE DEVICES

INTRODUCTION

In recent years there has been a trend towards moving discrete passive devices from board level to chip level. This has resulted in new and demanding challenges for on-chip interconnect architectures. The request for precision and high quality capacitors, inductors, and resistors is mainly driven by advanced mixed-signal, high frequency (RF), and system-on-a-chip (SOC) applications. Reduction and control of substrate coupling noise and other parasitics for mixed-signal and RF CMOS applications is one of the major tasks. From an application point of view, the most important requirements for passives are listed in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter.

The traditional method of realizing passive circuit elements (for example, capacitors, resistors) on ICs was integration during front-end processing. In this case, doped mono-crystalline Si substrates, poly-crystalline Si and Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during front-end processing suffer increased performance degradation especially when used at high frequencies. Therefore, there is an increasing demand for low loss, low parasitics and high quality passive devices in the interconnect levels.

For interconnect integration, the key challenge is to achieve this goal in a modular and cost-effective way,without sacrificing overall interconnect performance and reliability. Currently, two fundamentally different approaches are being pursued for on-chip integration. One is the introduction of optional or additional interconnect levels, in combination with new materials, to fulfill the necessary functions while maintaining the highest Q-factors and minimizing usage of additional chip area. In general, this approach has the disadvantage of higher process complexity and potentially higher manufacturing cost. The alternative is simply to design passive devices by using the native or "parasitic" properties, e.g., capacitance, inductance and resistance, of the existing interconnect levels. This second approach is the least demanding for wafer manufacturing, but suffers, typically, from reduced Q-factors of passive devices and a larger consumption of precious chip area. Other approaches make use of post-passivation redistribution layers of the wafer-level package or may integrate passive devices directly into the package. Innovative system-in-a-package (SiP) modules or 3D IC stacking techniques with TSVs may also be used more frequently to replace the highly complex and expensive SoC manufacturing process. In the end, cost isexpected to become the decisive factor in the selection of the optimal approach to realizing passive elements with sufficient system performance, quality and reliability.

CAPACITORS

MIM CAPACITORS

High quality metal-insulator-metal (MIM) capacitors are widely used in CMOS, BICMOS, and bipolar chips. Typical applications are filter and analog capacitors (for example, in A/D or D/A converters), decoupling capacitors, RF coupling, and RF bypass capacitors in RF oscillators, resonator circuits, and matching networks. Key attributes of MIM capacitors are high linearity over broad voltage ranges (low voltage coefficients), low series resistance, good matching properties, small temperature coefficients, low leakage currents, high breakdown voltage, and sufficient dielectric reliability.

The economic demand for small chip area consumption leads directly to the request for higher MIM charge storage densities. Above a capacitance density of 2 $fF/\mu m^2$, further thinning of the traditionally used Si-oxide or Si-nitride dielectrics is no longer useful because of increased leakage currents and reduced dielectric reliability. Therefore, new high-κ dielectric materials, such as Al_2O_3, Ta_2O_5, HfO_2, Nb_2O_5, TiTaO, BST, STO, etc. or laminated layer stacks of different materials are being evaluated as MIM dielectrics and may be used in future applications.

As always, the introduction of new materials leads to new challenges in material processing (such as advanced plasma vapor deposition (PVD), chemical vapor deposition (CVD), or ALD methods), process integration, and reliability. High quality films with excellent thickness uniformity, low defect density, and high dielectric constant need to be deposited below 450 °C to be compatible with the overall interconnect architecture. To reduce parasitic substrate coupling and allow for high quality factors of the MIM capacitors, integration into upper metallization levels is preferred.

Low resistive capacitor electrodes and perfectly engineered electrode-dielectric interfaces are necessary to achieve high MIM quality factors and the required reliability targets. Some promising integrations of high κ materials in MIM capacitors have been demonstrated in the literature (see the *Appendix: Passive Devices*).

NATIVE CAPACITORS

The main disadvantage of MIM capacitors is the higher process complexity (i.e., typically two additional lithography and patterning steps) resulting in added cost during wafer manufacturing. Therefore alternative approaches making use of the native or "parasitic" inter-metal capacitance between metal lines in minimal design rules are more attractive, especially for advanced CMOS technologies beyond 90 nm. Capacitors consisting of interdigitated metal fingers and interlayer vias

are stacked over several metal layers and can be designed and built in the ordinary interconnect scheme without any additional process steps. Depending on the number of metal layers used and the minimum design rules, it is realistic to achieve capacitance densities of 2–4 fF/μm^2 or even more. Today 3D stacks of vertical parallel plate (VPP) capacitors, vertical natural capacitors (VNCAP) or metal-over-metal (MOM) capacitors are standard offerings in advanced CMOS platform technologies with Q-factors > 20 at GHz frequencies. The increasing capacitance densities of VPP or MOM capacitors, due to the scaling of metal line width and metal spacing, makes their use even more attractive for future technology nodes. The only open question is whether the porous low-κ dielectrics in between the minimum metal spacings are able to pass the leakage current and dielectric reliability targets of the capacitor structures.

INDUCTORS

High quality on-chip inductors are critical components in analog/mixed signal and high frequency (RF) applications. Currently they are widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers, and low noise amplifiers (LNA). Key attributes are high quality factors, Q, at high inductance, high self-resonance frequency, low Ohmic losses, low eddy currents, and low capacitive substrate losses.

Today, spiral inductors in the upper thick Al- or Cu-metallization levels are most widely used in order to fabricate low resistive coils with sufficient spacing from the Si-substrate to achieve optimal quality factors. These simple spiral inductors can be fabricated relatively easily using standard interconnect processes. In several standard CMOS platform technologies, optional super-fat wiring levels with metal thicknesses of 2–6 μm are offered to realize specific high Q inductors. But they may not, in every case, be good enough to fulfill all future RF requirements. Therefore, some more advanced constructions and approaches are being pursued.

Shunted coils, realized in several metallization levels, the use of metallic or even magnetic ground planes, suspended spiral inductors in air-gaps, post passivation add-on modules with coils in fat redistribution metal layers (with metal thicknesses of several μm) and solenoidal inductors with and without ferro-magnetic core fillings have been successfully demonstrated. Other possibilities for reducing substrate losses are the use of high Ohmic Si substrates, SOI substrates or localized semi-insulating Si-substrate areas after ion- or proton- bombardment (see Appendix: Passive Devices).

However, not all of these alternative fabrication schemes are suitable for manufacturing because of integration and process complexity issues or incompatibilities with device or product requirements. These different inductor concepts are an expression of the constant struggle between low manufacturing costs on the one side and the best possible performance (i.e., highest inductance at high frequencies; Q-factor improvement by reducing Ohmic losses in the coil, and reduction of parasitic substrate coupling) on the other side.

RESISTORS

Precision thin film resistors are widely used in analog and mixed-signal circuits and specific SOC applications. Key attributes are precise resistance control, excellent matching properties, high voltage linearity, low temperature coefficients, low 1/f noise, and low parasitics resulting in high Q values. Today the most widely used Si-substrate-, poly-Si-, or silicide- resistors fabricated during front-end processing suffer mainly from poor 1/f noise performance and substrate losses.

Thin film resistors in the metallization levels can significantly improve 1/f noise performance and other substrate losses. Key challenges for resistors in the interconnect are finding materials with moderate and tunable sheet resistance which are compatible with the standard interconnect materials and integration schemes, controllable thickness, and good etch selectivity to dielectrics with a modular integration scheme. Especially for Cu-metallization schemes, TaN has been found to be a promising candidate; however, other materials may see use in the near future.

More details on applications, typical requirements, and processing and integration challenges of the different passive devices (capacitors, inductors and resistors), including a list of recent references, can be found in the Appendix section for Passive Devices.

INTERCONNECT CHALLENGES AND REQUIREMENTS

DIFFICULT CHALLENGES

Table INTC5 highlights and differentiates the five key challenges in the near term (≥ 16 nm) and long term (< 16 nm). In the near term, the most difficult challenge for interconnects is the introduction of new materials that meet the wire conductivity requirements and reduce dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be mitigated.

Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. Dimensional control is a key challenge for present and future interconnect technology generations and the resulting difficult challenge for etch is to form precise trench and via structures in low-κ dielectric material to reduce variability in RC. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels.

Table INTC5 2009 Interconnect Difficult Challenges

Difficult Challenges ≥16 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials	Integration complexity, CMP damage, resist poisoning, and dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool.
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with its associated metrology) to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, and CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, and elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges <16 nm	*Summary of Issues*
Mitigation of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with its associated metrology)	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continue to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of wiring levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnects.
Identification of solutions which address 3D structures and other packaging issues	3D chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

TECHNOLOGY REQUIREMENTS

To adequately describe the interconnect wiring needs, near term (2009–2015) and long term (2016–2024), technology requirements and potential solutions are addressed for two specific classes of products: Logic (MPUs and ASICs) and DRAM. For MPUs, Metal 1, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a

hierarchical scaling methodology that has been broadly adopted. The 2007 roadmap recognized an acceleration of MPU product introduction to a two-year cycle for the next technology generation (2009) and reversion to a three-year cycle after 2009. It also projected that the M1 pitch for MPUs will become equivalent to that of DRAM in 2010. In addition, there is now no difference in pitch between the MPU M1 and intermediate wires. MPU M1 "contacted pitch" refers to wires with staggered rather than side-by-side contacts. The use of staggered contacts has been the standard MPU design methodology for quite some time.

The accelerated scaling of MPU pitch has aggravated the copper electromigration problem. J_{max} limits for current dielectric cap technologies for copper will be exceeded by 2013. Modification of the Cu surface to form CuSiN or use of alloys such as Cu-Al can yield significant electromigration improvements. Implementation of a selective metal cap technology for copper, such as CoWP, will result in even higher electromigration capability. However, there is still concern about yield loss due to metal shorts caused by these selective processes. Improved dielectric caps are also being explored.

Electron scattering models have been improved and can now predict the Cu resistivity rise as a function of linewidth and aspect ratio. There is a significant contribution to the increase in resistivity from both grain boundary and interface electron scattering. To date, research has not identified any potential solutions to this problem. Accordingly, Cu resistivity numbers for minimum M1, intermediate and global wires are now listed for all the years of the roadmap. The effect of this resistivity increase on the RC performance metrics is also calculated and included in the technology requirements table. Three-dimensional control of critical dimension (3DCD) interconnect features has been listed as one of the critical challenges in several editions of the ITRS. The total variability of M1 wire resistance due to CD variation and scattering has been calculated and is also included in the MPU technology requirements table. Since the length of Metal 1 and intermediate wires usually shrinks with traditional scaling, the impact of their delay on performance is minor. Global interconnects, which have the greatest wire lengths, will be impacted most by the degraded delay. The benefit of materials changes or some amelioration of the Cu resistivity rise will be insufficient to meet overall performance requirements. The trend toward multi-core MPU design has alleviated some of the delay issues associated with ever increasing lengths of global interconnects

In the long term, new design or technology solutions (such as 3D IC, optical or carbon nanotubes) will be needed to overcome the delay, power, and bandwidth limitations of traditional interconnects. Refer to "New Interconnect Concepts and Radical Solutions." Inductive effects will also become increasingly important as the operating frequency increases, and additional metal patterns or ground planes may be required for inductive shielding. As supply voltages are scaled or reduced, crosstalk becomes an issue for all clock and signal wiring levels. A crosstalk metric was introduced in the 2005 ITRS for M1, intermediate and minimum global wires. The metric calculates the line length where 25% of the switching voltage is induced on a minimum pitch victim wire. The 2009 Roadmap continues to reflect the ongoing reduction of dielectric constant for future technology generations as new porous low-κ dielectric materials and eventually air gap technology are introduced.

MPUs utilize a high number of metal layers with a hierarchical wiring approach of steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified, solely to meet performance requirements. ASICs share many of the technology attributes of MPUs, for example, Cu wiring and low-κ dielectrics. ASIC design methodology is generally more regular, consisting of M1, intermediate, semi-global (2× intermediate) and global (4× intermediate) wire pitches. Historically, DRAM interconnect technology reflected the most aggressive metal pitch and highest aspect ratio contacts; however, the MPU M1 pitch is projected to equal that of DRAM in 2010. The introduction of low-κ dielectric materials (fluorinated silica glass (FSG)) is underway and the change from aluminum to copper at 65 nm half pitch is occurring.

Damascene process flows dominate MPU/ASIC fabrication methodologies and usage in DRAM is expected to broaden. Figure INTC4 illustrates several typical inter-level dielectric (ILD) architectures used in the creation of interconnect wiring levels. While current copper damascene processes utilize PVD Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to the end of the forecasted roadmap but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of damascene features. Surface segregated, CVD, ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required. Figure INTC5 shows a typical cross-section of hierarchical scaling for an MPU device (left) and ASIC device (right).

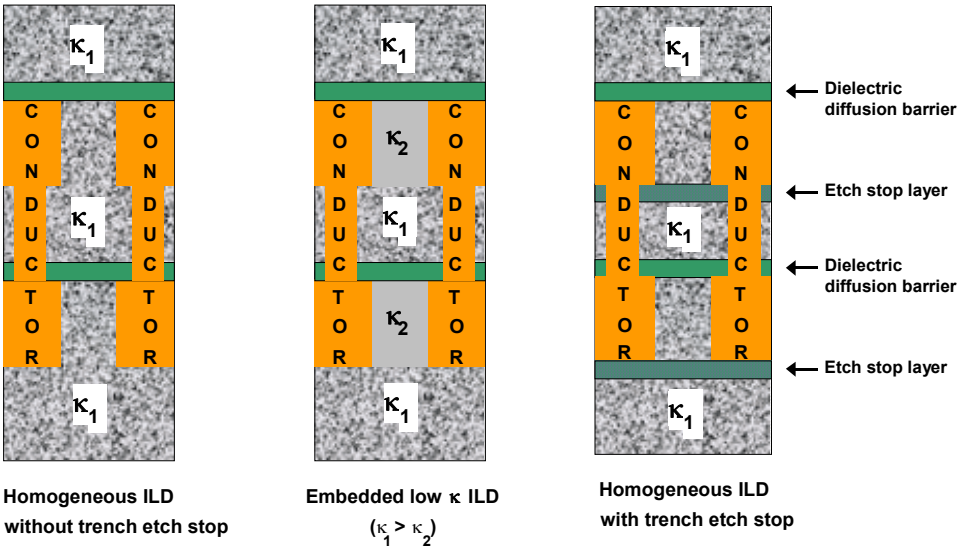


Figure INTC4 Typical ILD Architectures

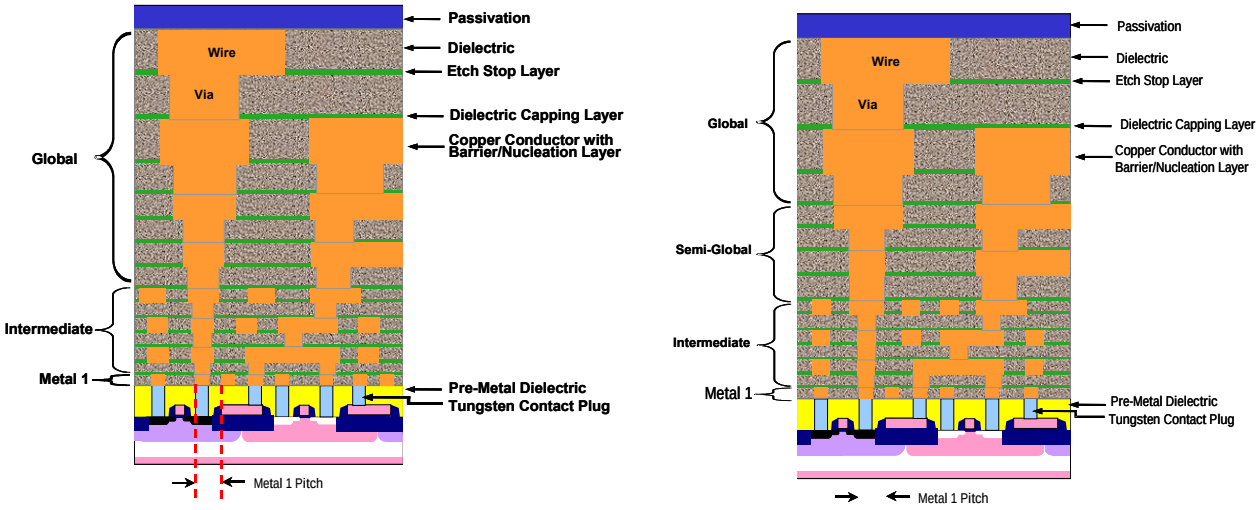


Figure INTC5 Typical Cross-sections of Hierarchical Scaling (MPU Device (left), ASIC Device (right))

Near-term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for decoupling and metal-insulator-metal (MIM) capacitors and materials with high remnant polarization for ferroelectric memories. The thermal, mechanical, and electrical properties of these new materials present a formidable challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials will be required which have sufficient optical contrast to serve as low-loss waveguides.

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long-term solution. For copper CMP, minimization of

erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Further research is needed to improve planarization processes (with associated end-point) which are compatible with low-κ dielectrics characterized by low density and poor mechanical strength. Improvements in post-CMP clean will be critical in achieving the low defect densities required for future devices. Etch, resist strip, and post-etch cleans must be developed which maintain the desired selectivity to etch stop layers and diffusion barriers, but which do not degrade low-κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

Table INTC6 MPU Interconnect Technology Requirements

Table INTC7 DRAM Interconnect Technology Requirements

Table INTC8 Interconnect Surface Preparation Technology Requirements

PROCESS MODULES

INTRODUCTION

DIELECTRIC

Damascene has been the dominant process scheme for fabricating Cu interconnect structures. In particular, dual damascene, in which there are fewer metallization and planarization steps than in single damascene, has generally been used since 1997. Following the adoption of Cu as the conductor, intensive research and development efforts have been carried out to minimize wire capacitance by incorporating dielectrics with lower dielectric constants (κ) than conventional oxides. The pace of incorporating advanced low-κ materials has been slowing down as compared to the earlier ITRS projections because of difficulties in manufacturing, including cost, and reliability.

Low-κ materials have been targeted mainly for use as intra/inter-layer dielectrics (ILD). But the influence of other dielectric layers, typically having higher κ values, on the effective κ has been growing. The effective κ value does not decrease in proportion to the decrease in the bulk κ value. Moreover, thinning of relatively high-κ layers tends to be more challenging than ILD since they are already as thin as possible. In the Passive Devices Appendix, Figures A1 and A2 show cross-sections of interconnect structures and the corresponding effective κ values. Historically, the highest-κ layers are Cu diffusion barriers. There have been high-κ materials at the top of the ILD to protect the porous low-κ ILD from the damage during CMP and plasma deposition, but they will be sacrificial with implementation of air-gap features. Reduction of thicknesses and bulk-κ values of diffusion barriers will be most important for decreasing RC delay. In addition to the improvement in capacitance reduction, diffusion barrier deposition pre-treatment has been investigated as a means of obtaining higher reliabilities. Scaling down the metal/hole-size and -spacing degrades electro-migration (EM) and time-dependent dielectric breakdown (TDDB), respectively. The interfaces just below the diffusion barriers will require improved adhesion, fewerdefects, less damage, etc.

Reduction of the ILD κ value is slowing down because of problems with manufacturability. The poor mechanical strength and adhesion properties of lower-κ materials are obstructing their incorporation. Delamination and damage during CMP are major problems at early stages of development, but for mass production, the hardness and adhesion properties needed to sustain the stress imposed during assembly and packaging must also be achieved. The difficulties associated with the integration of highly porous ultra-low-κ ($\kappa \leq 2$) materials are becoming clearer, and air-gap technologies are likely to be introduced earlier than projected in the previous editions of the ITRS.

Due to the increase in the development costs of process design kits, once a process technology is established, only relatively minor changes are made in the course of its improvement. In the future, new materials are expected to be introduced only when migrating to a new technology. The bulk κ values of ILD layers and the K_{eff} roadmap are shown in *Table INTC6*. The slowdown of low-κ since the 2007 edition was published was partly reflected in the 2008 update (Figure INTC6 below). In this edition, the trend is further reflected by delaying low-κ progress by one year in light of the actual pace of deployment of new technologies.

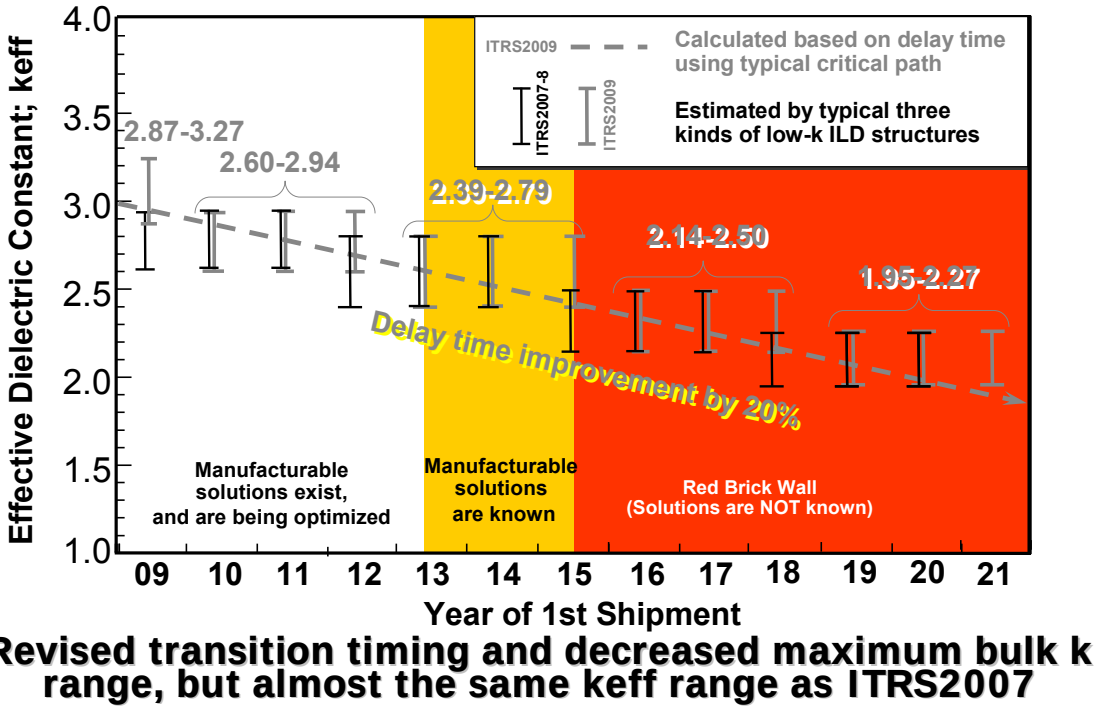


Figure INTC6 Low-κ Roadmap Progression

PRE-METAL DIELECTRIC (PMD)

The pre-metal dielectric (PMD) potential solutions chart (Figure INTC7) has been significantly updated. PSG (Phosphorous-doped spin-on glass) and BPSG (Boron-doped PSG) were deleted from the solutions because they are no longer used for gettering of heavy metals. Low-κ OSG, MSQ, and HSQ were also deleted because the high-κ stress liner (SiN), used for improving mobility of MOSFETs, dominates the capacitance at the PMD level.

While the requirement for the reduction of κ value has been dropped, the need for filling ability is becoming more critical. To fabricate small contact holes uniformly, the space between the side-walls of transistors must be filled without any voids. Combination of conventional and conformal deposition techniques is a possible way to achieve both fine-pitch filling and low cost. Thermal and plasma-assisted CVD SiO_2 and its planarization process will be used continuously because of their low cost, efficiency and reliability.Two-dimensional miniaturization is no longer a sufficient, nor the most effective means to increase the capacity of memories, and consequently three-dimensionally stacked memory cell structures have been reported for NAND Flash [1, 2]. In these devices, the gate electrode of a memory cell has a stepped structure, and very large steps are formed between the memory cell area and its periphery during fabrication. The stepped surface thus formed must be filled with an insulator, without leaving voids, and a contact hole must be made for each gate electrode. For this process, spin-on dielectrics (SOD) might be used because of their superior gap filling capability versus conventional CVD materials. Inthis case, the spin-on conditions required for filling a relatively large area with an irregular surface must be investigated. The SOD must also be amenable to planarization by CMP.

CONVENTIONAL LOW-K ILD

The primary conductor material changed from Al to Cu, and the damascene process became the dominant process for interconnect fabrication. The damascene process does not require dielectrics of high gap-filling capability because it is Cu that fills trenches and/or holes in the dielectrics. PECVD-SiO_2, which has lower gap-filling capability than HDP-SiO_2, has been used as an ILD material since the dawn of Cu interconnects. For the top few metal layers, used mainly for power/ground lines, attaining high mechanical strength to avoid cracking and/or peeling during assembly and packaging processes is more important than capacitance reduction. Given its cost efficiency, PECVD-SiO_2 will continue to be used for thick layers.

For the bottom few metal layers with thin wires, reduction of κ_{eff} is still critical. Many low-κ materials have been studied for use as inter/intra-layer dielectrics in order to decrease the interconnect capacitance. There are still difficulties in low-κ material integration caused by their poor mechanical and chemical strength. Further improvement of their material properties, as well as design and structure changes, will be required for the integration of highly porous ILDs.

Spin-on dielectrics have the benefit of less dependence on precursors than CVD, that is, one tool can handle a variety of materials, including porogen. Various spin-on low-κ materials including porous materials have been studied. However, PECVD-SiCOH has been the dominant low-κ ILD film. Non-porous spin–on materials have not been used except in some special cases. Spin-on polymer and spin-on MSQ with $\kappa \geq 2.4$ are unlikely to be used for actual logic/memory devices, consequently spin-on materials, except porous-MSQ, have been deleted from the potential solutions figure (See Figure INTC7).

In order to decrease κ_{eff} by adopting increasingly porous low-κ ILD materials, challenges in integration processes such as etching, CMP, and deposition on porous ILD layers must be tackled. Photolithography for porous ILD usually requires a dense layer to ensure a uniform resist coating and for preventing damage during resist strip. The layer can also act as a stopper during metal-CMP. SiO_2 has been widely used as a "hardmask" layer. However, low-κ ILD is damaged by active oxygen in the initial stages of the hardmask deposition. The hardmask and damaged layers should be removed in order to decrease the capacitance, especially in intra-layers. Those layers should be removed preferably by CMP after barrier metal is cleared up in order to minimize process steps. However, it also exposes the porous low-κ material to CMP conditions. Improvement of CMP or development of alternative processes that can produce flat and clean porous low-κ ILD is a key to successful fabrication of low-κ_{eff} interconnects.

Dry etching for trench or via formation also damages low-κ ILD. In order to minimize damage done by active species, "closed-pore" porous low-κ materials are actively being researched. Great efforts are being made to reduce etching damage and to recover the original low κ value of the material by *in situ* termination. The development of ultra-low-κ ILD ($\kappa < 2.3$) will become increasingly important in meeting harsh performance demands.

Formation of porous or ultra-porous low-κ films requires appropriate cure technologies such as decomposition and evaporation of porogen and chemical-bond bridging that gives higher mechanical strength. UV and e-beam assistance has commonly been used in low temperature cure processes, but their cost efficiency and effects on underlying layers invite serious consideration when applied to multi-stacked thin interconnect layers. With the assistance of cure processes, spin-on materials will be a realistic solution for ultra-low-κ ILD. However, PECVD has the advantage of easier integration of the cure system into a cluster tool. Overall cost of ownership will ultimately determine which materials are successful in mass production.

In spite of the tremendous efforts being made, a broad consensus is forming that κ_{eff} cannot be lowered much further by reducing the bulk κ value of ILD, once it has reached 2.0, due to mechanical integrity and plasma damage problems with porous low-κ materials. Ultra low-κ materials with $\kappa<2.0$ are discussed in the *Emerging Research Materials* chapter. A different, architectural (as opposed to material) approach to lowering κ_{eff} is to introduce air-gaps (described below) into ILD layers.

DIFFUSION BARRIER

Dielectrics for diffusion barriers typically have the highest κ values in conventional Cu interconnect structures. In a conventional Cu damascene process flow, the bottom and sides of Cu lines are covered by barrier metal, which is deposited before the Cu seed layer. Only the top of the Cu lines is covered by the diffusion barrier dielectric after CMP. Diffusion barriers must be free of pinhole defects and function as etch stop layers during via formation. These layers were referred to as the "via etch stop layers" in the 2007 edition of the Interconnect chapter.

Silicon nitride (SiN), whose κ value is over 6, was adopted as a diffusion barrier dielectric at the inception of Cu interconnects with PECVD-SiO_2 ILD. Since low-κ ILD materials were introduced, SiC, SiCN, or SiCO [3], whose κ value is less than 4, have widely been used as diffusion barrier dielectrics in order to decrease κ_{eff}. As the ILD layers become thinner, the relative contribution of the diffusion barrier κ to κ_{eff} is growing. While alternative lower-κ diffusion barriers have not been used to date, thinning of diffusion barriers and κ reduction are critically required.

The metal-capping process, in which a metal barrier is grown selectively on Cu lines, offers the possibility of omitting the insertion of a diffusion barrier between the low-κ ILD and the Cu lines. Because of the imperfect selectivity of existing metal capping processes, both capping metal and thin diffusion barrier dielectric can coexist in a transitional stage, but such redundant combinations should ultimately be avoided to reduce process costs.

CAPPING BARRIER DIELECTRIC

The interface between a diffusion barrier and the top of a Cu line has a direct impact on the reliability of damascene Cu interconnects [4]. Minimum spacing between metals usually appears at such interfaces by misalignment of vias with Cu lines. Time-dependent dielectric breakdown (TDDB) lifetime and electromigration reliability are strongly affected by the cleanliness of the interfaces. Dominant electromigration paths usually run along the interfaces of aCu lines, which are not covered with barrier metal. The requirement for fine interface formation will become more stringent as the metal width and spacing become narrower; EM and TDDB lifetimes will also be shortened.

Metal capping has been shown to give longer EM lifetimes compared with the conventional structure with a dielectric barrier on Cu. The capping metal, selectively grown on Cu lines, produces a strong metal connection between the wires and the via bottoms. Capping metal growth must be carried out with almost perfect selectivity on fine-pitched Cu lines to prevent leakage and TDDB. The selectivity is improved by cleaning the dielectric between metals. However, the cleaning process itself also has a selectivity problem. Improvement of the EM lifetime by the use of Cu-alloy seed and/or by barrier metal optimization is also being studied. Several metal materials are considered but tend to increase the resistance of Cu lines. Continuous research and development are needed to find feasible solutions.

Another process that gives better interface characteristics is pre-treatment of the Cu before the deposition of the dielectric diffusion barrier. *In-situ* CuSiN formation using silane and ammonia plasma, in the same apparatus as that used for the dielectric barrier deposition, gives a longer EM lifetime without TDDB degradation [5]. The resistance of the Cu wires depends on the silicon diffusion condition, so the exposure to silicon and nitridation must be carefully controlled. Recently, CuGeN formation using germane instead of silane was reported [6]. The resistivity of CuGeN is more controllable than CuSiN. Silane/germane sources, combined with ammonia, are suitable for mass production. But there will be possibilities for other powerful treatment processes with different materials. The recently proposed pre-treatment for preventing Cu migration by impurity metal doping is also a potential solution to high-reliability interface formation [7].

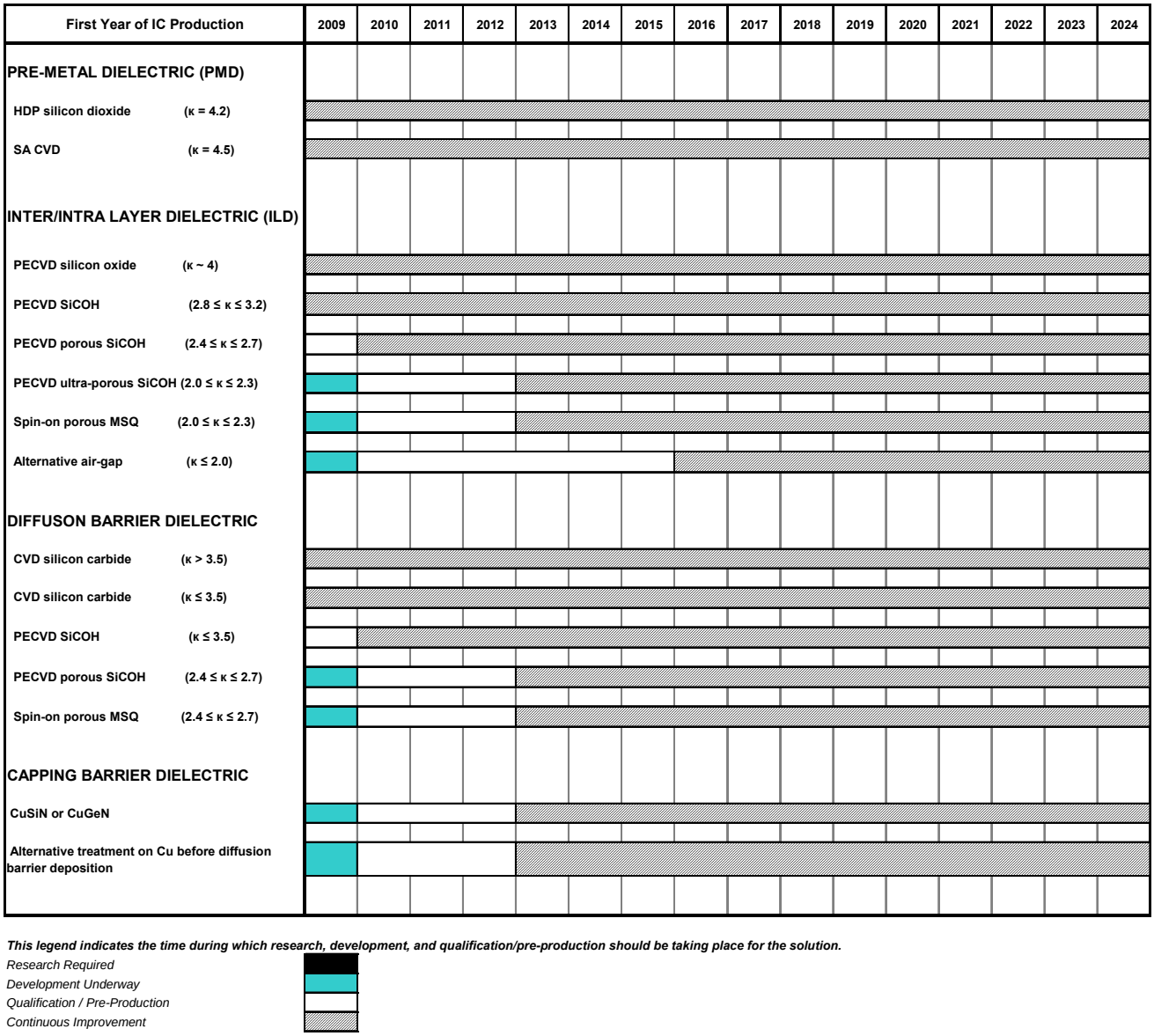


Figure INTC7 Dielectric Potential Solutions

AIR GAPS

Porous low-κ materials have poor mechanical integrity and sustain much damage from plasma etching. Integration of porous low-κ materials with $\kappa \leq 2.0$ is deemed to be extremely difficult. A gradual transition from ultra low-κ materials to air-gaps is now considered a real possibility. A hybrid of low-κ materials and air-gaps will be the most realistic solution to lowering κ_{eff} in the foreseeable future.

Introducing air-gap structures into interconnects will be one of the most significant challenges for semiconductor device fabrication in the coming decade. Several integration schemes and structures for air-gap formation have been reported. They can be classified into two categories according to whether gap formation is performed before or after the upper metal formation. In order to integrate air-gaps into Cu damascene structures, sacrificial materials located between metal lines must be removed because Cu-CMP should be carried out under non-gapped conditions.

In integration schemes in which gap formation is performed before the upper metal is formed, the sacrificial parts are removed after CMP, and then air-gaps are formed by dielectric deposition with low filling capability [8, 9]. The removed parts consist mostly of the sacrificial material. The gap shape is defined by the spacing between and aspect ratio of metal

lines along with deposition conformality. In most cases of gap formation during inter-layer dielectric deposition, air-gaps are formed in regions having a narrow line-to-line spacing, but the dielectric is also deposited in regions having a wider spacing. This gives different total ILD thicknesses in dense and sparse regions and necessitates a planarization process. Another process flow in this category uses the damage done by dry etching to the sides of trenches. Uniform gaps are formed during the subsequent wet treatment for any line-to-line spacing selectively in damaged regions. The gap formation before upper metal formation has a serious alignment problem for fine-pitched interconnect. Misaligned vias do not sit exactly on a metal line. If a via opening connects to an air-gap region, appropriate barrier metal deposition and Cu filling cannot be carried out. Exclusion of regions around upper vias from air-gap formation has been presented, but it is accomplished at the cost of more process steps, including an additional lithography step.

In the integration schemes in which air gaps are formed after the upper metal layer is constructed, there is no misalignment problem because via holes are filled with metal before gap formation [10-12]. Removing the sacrificial parts of multiple layers may be desirable for minimizing the number of process steps. The removal process applied in this scheme produces large gaps, which degrade the mechanical strength of the whole chip. Ceaseless efforts will be needed to develop air-gap structures with sufficient mechanical strength and can be formed with minimal process steps.

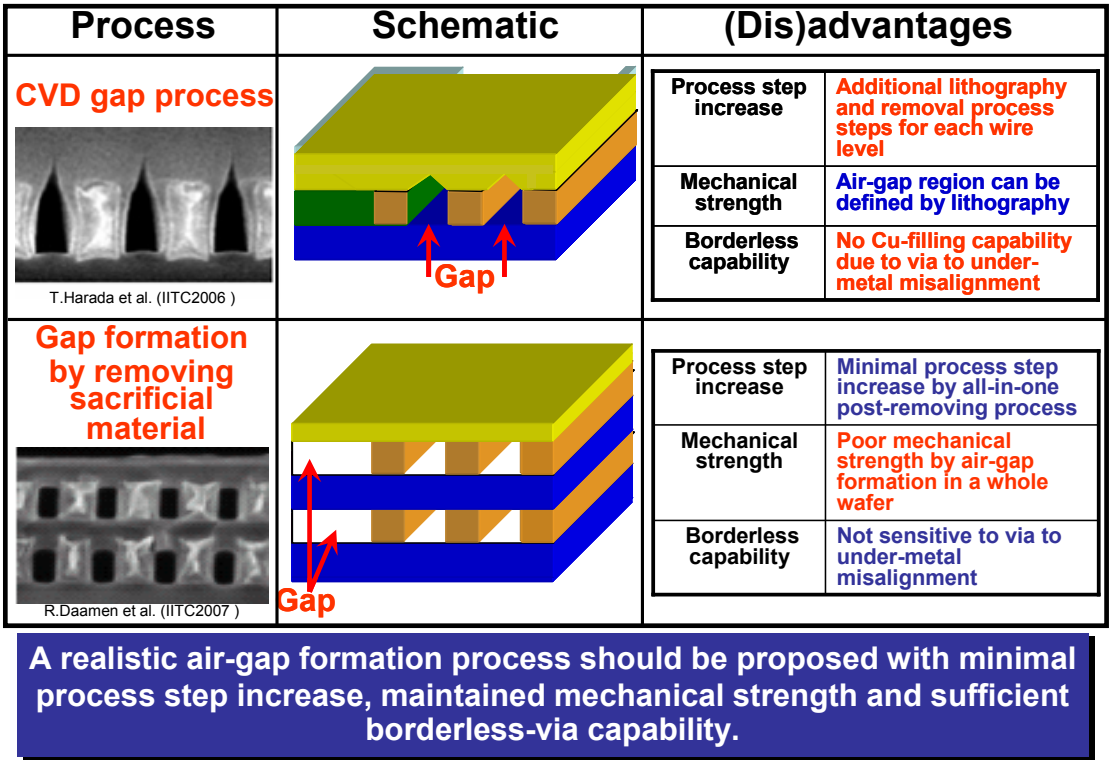


Figure INTC8 Typical Air-Gap Integration Schemes

ETCH / STRIP / CLEAN POTENTIAL SOLUTIONS

Beyond 32 nm, porous low-κ dielectric with κ value below 2.3 will be required to reduce RC delay for Cu interconnects. In order to achieve an integrated $\kappa_{eff} < 2.6$, for advanced technology nodes [1], a lower κ-value assist layer must be integrated. Bulk low-κ materials with $\kappa < 2.3$ alone will not be able to fulfill the requirements even when thinning currently used silicon oxy-carbide-based assist materials.

Unit process integration affects the final κ_{eff} value. Etching and ashing processes are among the worst processes for inducing damage to low-κ materials, affecting not only defectivity, but also electrical reliability. Challenges are:

- Profile control—CD control i.e., width and depth: directly linked to the integration strategy and etching chemistry process. Straight profiles are mainly required (compromise for reliability consideration) but

tapered profile versus bow profile is important for further metallic filling steps (PVD, CVD) and critical for scalability.

- Change of dielectric properties due to plasma-induced damage leading to κ value increase and impact on electrical reliability (species diffusion and moisture intake through the low-κ dielectric pores network). Metallic barrier precursor can also diffuse and alter material properties.
- Sidewall and bottom surface roughness—Plasma induces surface bottom roughening of damascene features and contributes to sidewall roughness of the photo resist. Both phenomena also impact Cu diffusion barriers by making it more difficult to form continuous thin barrier layers (below 3 nm). This has an important impact on reliability and electrical dispersion.
- Hard mask integration strategy—Two strategies are in competition—metallic versus organic hard mask. Metallic hard masks can induce a wiggling phenomenon for damascene small lines features due to relaxation of material stresses, potential micro-masking on the bottom of the structure, and metallic residues of the top of the mask after etching (non-volatile by-products). These points have to be addressed for scalability beyond 22 nm. Organic hard masks need an ashing process to remove the mask without degrading the exposed low-κ material or modifying the CD of the features after cleaning. Photoresist rework is also an issue for organic hard masks. Due to these issues, different parameters have to be considered.

PLASMA PROCESS CONTROL

Etching plasmas must be optimized for each material and structure. A tapered profile is preferred over a bowed one for metal filling consideration by manipulating hard mask faceting and maintaining good control of the passivation layer created during the etching process. Bottom surface roughness must be minimized. This is accomplished by optimizing both the carbon/fluorine ratio of the etch chemistry as well as ion bombardment (flux and energy). The choice of etching chemistry may also impact sidewall modifications and add the possibility of feature. Development of a post etching plasma treatment for fluoro-carbon species removal and/or low-κ restoration processes has to be considered. In terms of low-κ degradation (carbon depletion), hydrogen-containing chemistries (H_2, CH_2F_2, CHF_3 …) are preferred over oxygen-containing chemistries (e.g., O_2, CO, CO_2).

PLASMA HARDWARE CONTROLS

Continual refinement of current capacitive coupled plasma (CCP) source technology is expected to be able to adequately address the material challenges as well as shrinking trench and via dimensions at nearly constant aspect ratios. With the advances of porous low dielectric constant materials, ultra low-κ materials, and selective air-gap technology, metal hard mask implementation to reduce the ash damage is gaining momentum. Continual refinement of the current inductively coupled plasma (ICP) technology is expected to meet the metal hard mask requirements.

The development of specific cleaning procedures between two etching processes for recovering the initial chamber wall status (fluorine species elimination) is becoming critical in order to avoid any electrical dispersion and defectivity. This requires the use of a good top electrode material (Si-based) and good cleaning chemistries (oxidizing or reducing gases).

A futuristic concept such as plasma atomic layer etching (PALE) [2] [3] [4] [5] also has to be considered in order to attain extreme etching selectivity. To achieve monolayer control and selectivity over etching processes, a combination of active and passive control will be required. Passive control involves the use of chemistries that differentiate etch rate based on intrinsic chemical reactivity. Active control is based on the control of activation energy. In PALE, removal of single wafer layer is achieved in a two-step process. The first step passivates a single layer of material to lower its activation energy for removal below that of the underlying material. The second step removes that layer with regulated ion energy. The PALE concept could avoid the sidewall and bottom layer low-κ modification. Further studies using this technique in interconnect applications are required to assess the impact on profile and ion penetration.

INTEGRATION STRATEGY

Regarding process windows, 22 nm technologies and beyond will require the use of thinner photoresists as the critical dimension shrinks and aspect ratio limitations remain. Two masking strategies are in competition: metallic and organic. A multiple layer resist scheme will be required for better dimensional control, regardless of whether a hard mask integration scheme is employed. These advances will improve line edge roughness (LER) and allow thinner resist layers for high fidelity image transfer [6] [7]. With the advances in porous low dielectric constant materials and selective air-gap technology, metal hard mask implementation to reduce the ash damage is gaining favor. If a metallic hardmask approach is used [8], the development of post etching plasma treatment will be needed to remove metallic contamination on the damascene structure (mostly on the top surface of a metallic mask).

If metallic hard mask technology is not used, resist strip will be a constant challenge for low-κ integration. Damage free photoresist and residue removal would be facilitated by the development of etch processes that produce less deposited residue and/or re-deposited sputtered material, such as Cu sputtered during etch stop opening. Low damage photoresist and residue removal is facilitated by source technology (μwave plasma sources has to be considered using reducing based-technology).

Additional steps to repair damage and/or seal pores might be required for porous ULK dielectric etching [9]. These requirements may force the expansion of etching or stripping tools into multi-station systems. Problems such as moisture absorption or the reaction of moisture with damaged dielectrics could require *in situ* process flows that include etch, dry strip, wet strip, damage repair, degas, and pore sealing steps. Partial or total pore sealing could be managed by using plasma treatment with adapted chemistries as NH_3 [10] or CH_4 (creating a carbon-rich layer). These chemistries can create bonds which seal sidewall pores. Plasma treatments have specific advantages compared with other solutions including material deposition. Plasma treatment can potentially be done in the same process as the via or line etch (in-situ), which provides fast cycle time, low cost, and avoids exposure to air or wet chemistries before treatment. Gas or liquid restoration with Si – containing chemistries can also be used to restore the surface of the dielectric.

Ultimately, etch or strip tools could come to resemble PVD cluster platforms. Such platforms might also facilitate other processes where a variety of materials are present or where exposure of residue to the atmosphere would make it more difficult to remove. The extendibility of plasma-based dry strip technology is a concern. It might be necessary to replace it with alternative technologies at advanced technology nodes.

CLEANING PROCESS

A wet cleaning process is also mandatory in order to remove plasma sidewall polymer and metallic contamination. This cleaning process is commonly used between dual damascene etch and metal deposition. This step is mandatory because trapped fluorine gas and moisture on low-κ porous dielectric, as well as copper oxidation and sidewall polymer, impact the global yield (copper surface control is considered to be important for reliability). Process queue time between etching and cleaning must also be addressed.

According to these criteria, good advanced wet chemistry formulations must be efficient in removing native copper oxide and post etch residues and, at the same time, prevent copper surface corrosion and re-oxidation (copper is not electrochemically stable).

Conventional solvent chemistry commonly used for previous nodes could be replaced by dilute organic acids [10] [11] [12] in wet or vapor phases mainly for efficiency and cost considerations. Short process time with fresh chemistries is preferable. Organic acids act as chelating agents with copper while very dilute HF chemistry can address sidewall polymer removal with respect to CD control.

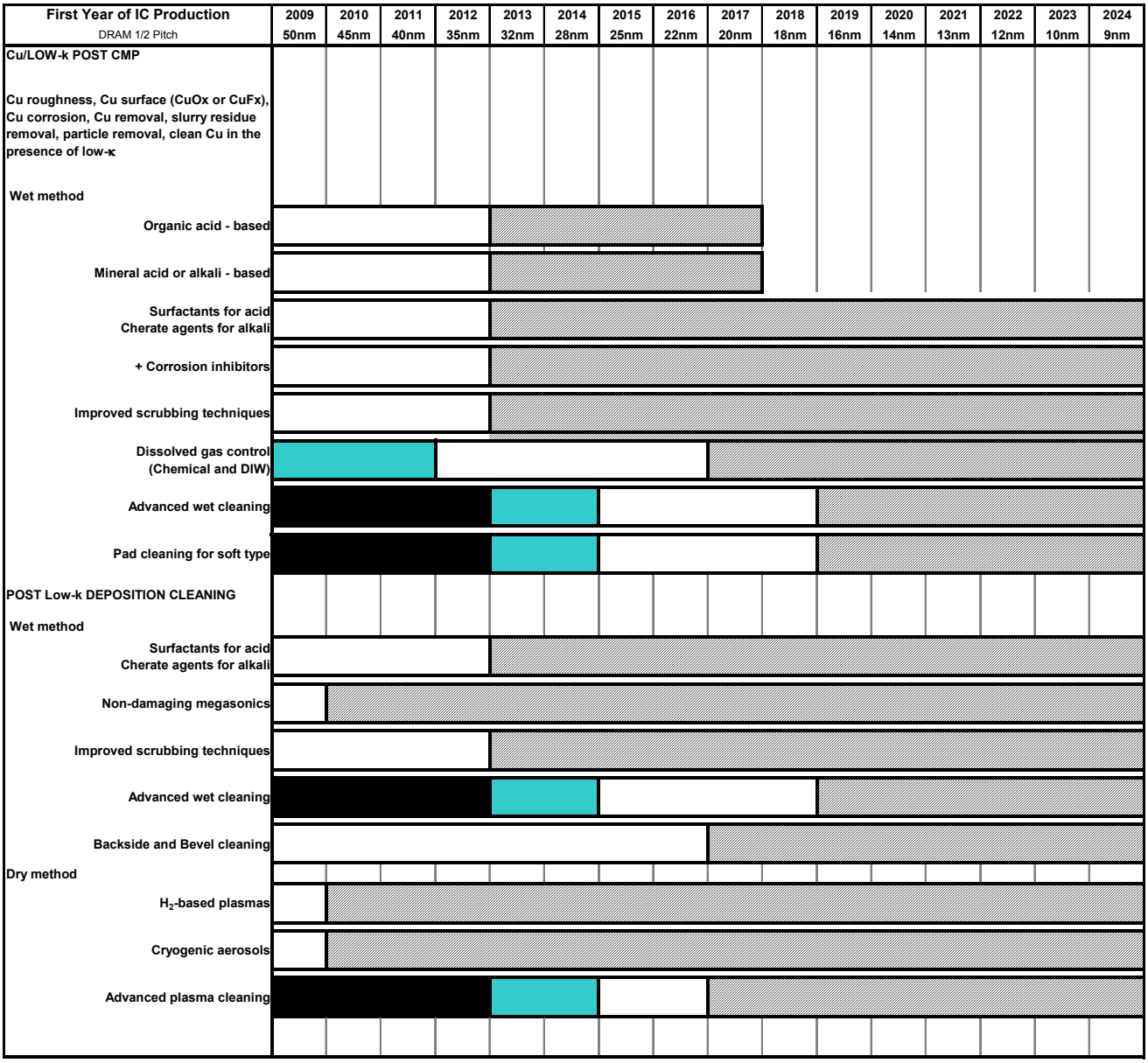


Figure INTC9 Post-CMP/Deposition Clean

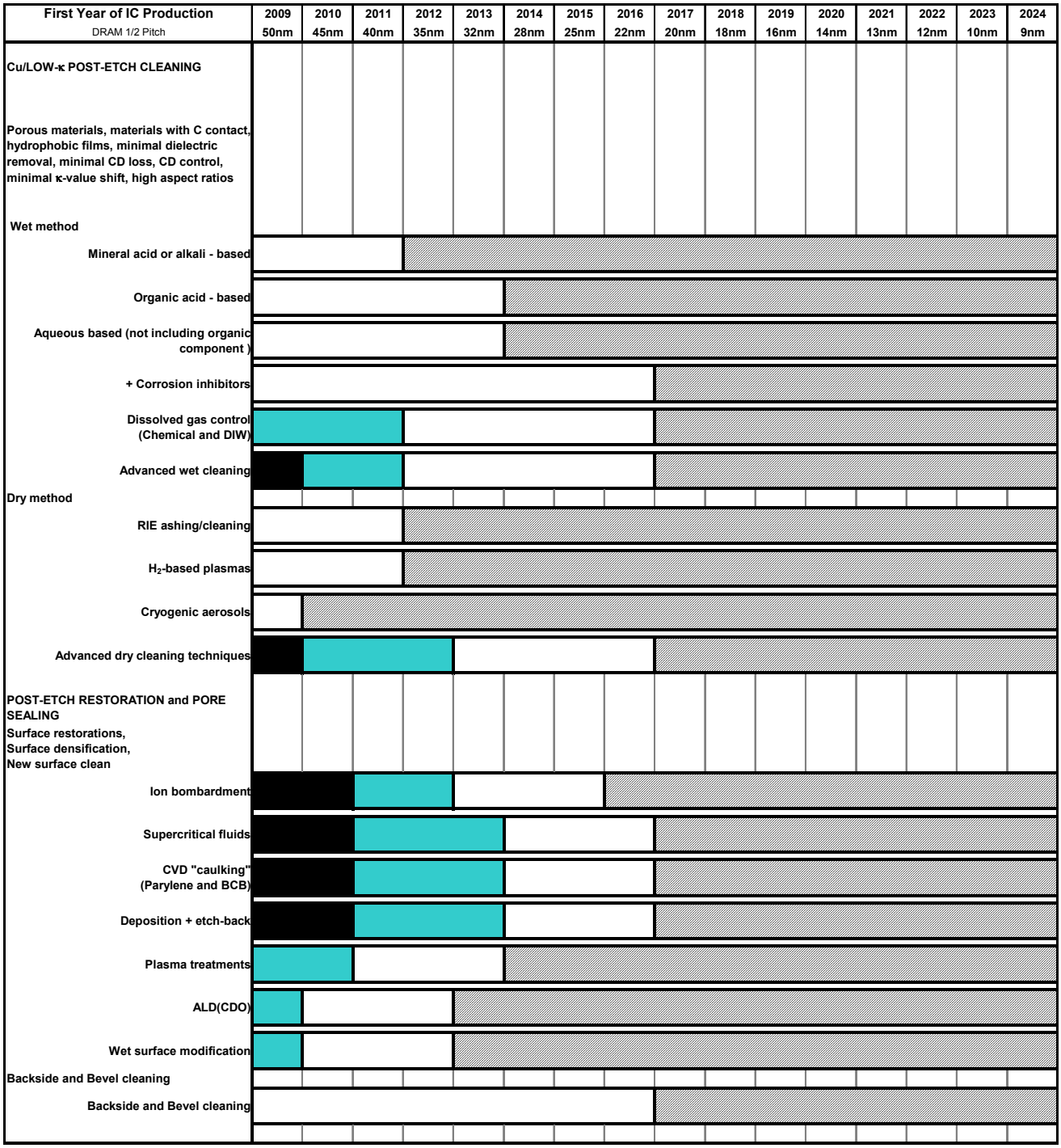


Figure INTC10 Post Dielectric Etch Clean

BARRIER POTENTIAL SOLUTIONS

Ti/TiN films [1] will continue to be used as barriers for tungsten local wiring, which is sometimes called metal zero, and for contact fill in the near term. Established deposition techniques such as ionized PVD,long throw PVD, along withCVD are being enhanced to improvecompatibility with key-hole free W used for high aspect ratio DRAM contacts . Development of ALD TI/TiN is underway and is likely to improve the overall W fill process by improving barrier conformality and reducing the top of contact "pinch-off" that leads to difficulty in W filling. Even with improvements, the Ti/TiN barrier is expected to be a significant contributor to future contact plug resistivity because of film thickness requirements and high resistivity. Development of alternative ALD barriers for W contact plugs, such as WN [2, 3], is underway and it appears that barrier resistivity and thickness can both be reduced versus Ti/TiN. In this case, the barrier contribution to overall contact plug resistance can be reduced.

Research is also underway to explore alternate materials and fill techniques for high aspect ratio contact structures which would allow simplification of the current contact/barrier/conductor film stack. Since one of the primary functions of the TiN or WN barrier is to prevent interaction of Ti with F from the WF_6 precursor, a change to non-fluorine containing tungsten precursors could allow for elimination of the barrier film entirely. Serious consideration is also being given to the use of Cu to replace W in contact studs. In this case, the standard PVD TaN/Ta [4], Ti [5], Ru or ALD Cu barrier alternatives would be used.

Cu wiring barrier materials must prevent Cu diffusion into the adjacent dielectric but also must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta [4] has become the predominant industry solution but other nitrides and silicon nitrides have also shown promise. Ionized PVD, and CVD deposition continue to be improved (while long throw transitions to a legacy status), enabling them to meet the challenging sidewall coverage requirements of future dual damascene structures. In fact, it appears that improvements in ionized PVD technology [6] will continue to be used at 22 nm. In addition, since the critical dimensions and aspect ratios for the upper global wiring levels for logic products remain relatively unchanged for future technology generations, they will continue to be compatible with PVD barrier technology. However, even these advanced PVD deposition techniques tend to narrow the upper part of the dual damascene trench and limit the fill capability of the ECD Cu process.

A great deal of effort is underway to develop ALD [7-10] barriers which are expected to become the predominant future solution for copper. ALD TaN and WNC (carbide) are further along in development but questions remain concerning their interface properties with Cu and whether adequate electromigration performance can be ensured. One potential solution to this issue is a PVD Ta flash layer followed by PVD Cu to provide the required interface to ECD Cu. ALD Ru appears to be compatible with direct plating of ECD Cu and also provides a good Cu interface, however, its barrier properties are suspect. Two advanced potential solutions are ALD TaN/ALD Ru and ALD WNC/ALD Ru bi-layer barriers. One major obstacle to the adoption of ALD for barriers is penetration of the precursor materials into the porous low-κ dielectrics targeted for future technology generations. *In situ* modification of the etched low-κ sidewalls may be used either with ALD or as a stand alone barrier to resolve this issue. The other major obstacle regarding adoption of ALD barriers is low throughput. This results in a significant increase in factory floor space and cost of ownership for ALD barrier/seed technology versus PVD barrier/seed solutions.

One promising area of development for Cu wiring technology is self-forming barriers, specifically Cu-Mn alloys [11]. This process eliminates the PVD barrier and instead utilizes a PVD Cu-Mn alloy seed layer. After ECP Cu deposition, an anneal causes the Mn to diffuse to the Cu surface and form a thin barrier. The Mn at the top surface of the annealed Cu is removed by the subsequent CMP operation. Another advantage of this process is that the Mn does not form a barrier in the underlying via region, resulting in a Cu-Cu via interface with very low via resistance.

Another focus area for metal barriers is the Cu top interface. PECVD dielectric Cu barriers such as Si_3N_4, SiCN, and SiC are predominately used for this application. Disadvantages are degraded Cu electromigration properties and a rise in the overall κ_{eff} of the structure because of their higher κ values. Some modifications to the top Cu interface for improved electromigration lifetime are targeted at ≤ 32 nm MPU/ASIC half pitch. Selective metal capping barriers such as W [12], CoWP [13], or NiMoP [14], CVD Co or CVD Ru are being explored and have resulted in improvements in Cu electromigration properties. The industry has been slow to adopt selective metal capping processes because of the risk of yield loss from metal shorts. The other major candidate for a capping process is formation of a CuSiN layer at the top Cu surface [15]. This is accomplished by sequential exposure of the surface to SiH_4 and NH_3. While the degree of electromigration improvement is not as large as with CoWP, there is also a much decreased risk of reliability issues due to metal shorts or leakage.

A great deal of research and development in the area of advanced barrier materials and deposition techniques is needed, since engineering the smoothness and other properties, such as the lattice mismatch between the barrier and the Cu interface, may help to ameliorate the expected Cu resistivity increase from electron scattering effects. Practical approaches to simultaneously suppressing electromigration and resistivity increases are essential.

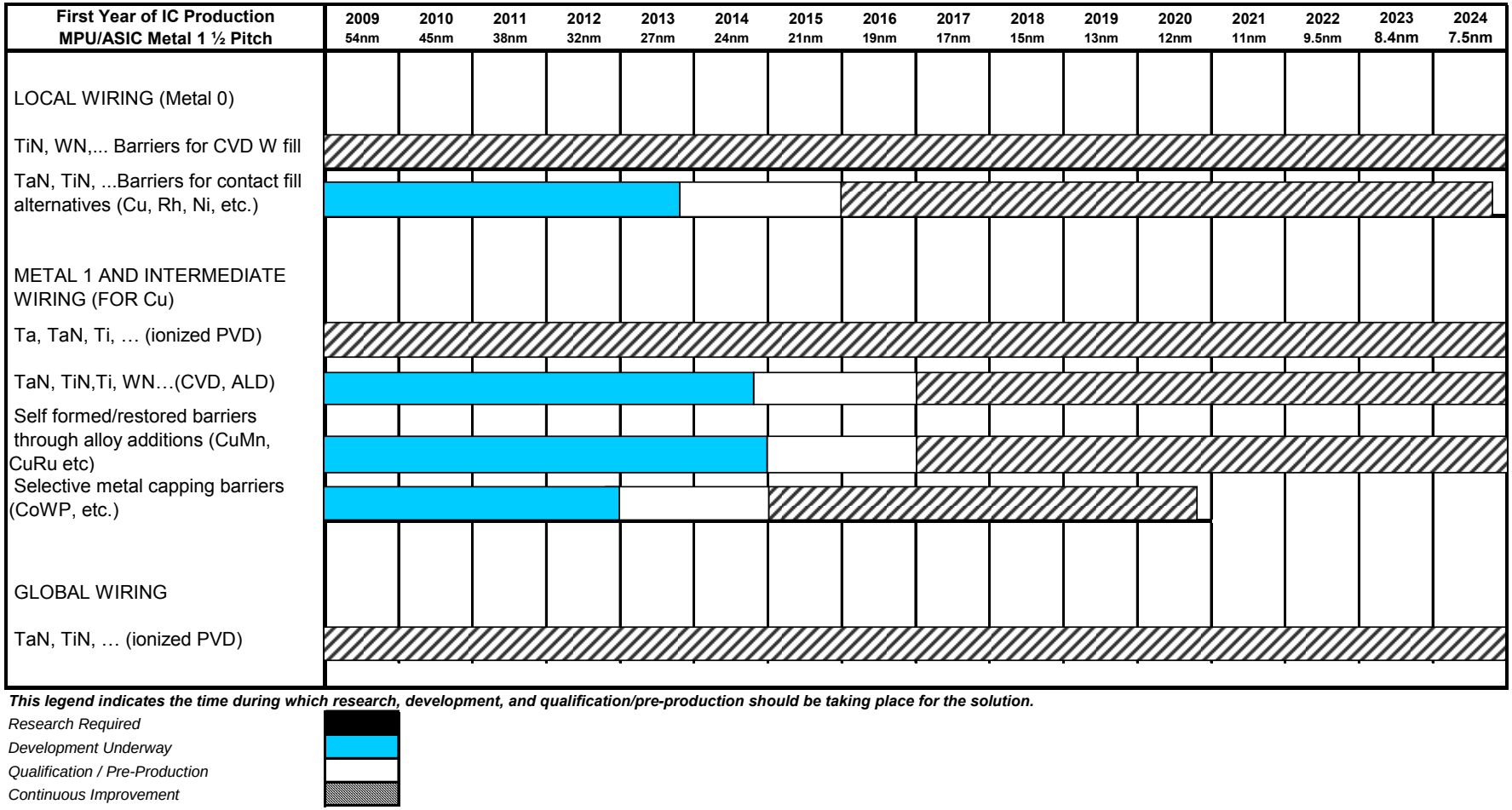


Figure INTC11 Barrier Potential Solutions

NUCLEATION POTENTIAL SOLUTIONS

The conformality and coverage of the nucleation layer is often the critical factor in determining whether the subsequent conductor deposition will be free of voids. For local wiring and contact fill, there will be continued improvement in ALD W nucleation layers which have been used to enable high aspect ratio W fill. These ALD nucleation layers are usually extremely thin so that the overall conductivity of the plug is generally improved.

An ALD WN combined barrier/nucleation layer [1, 2] process is in development as an alternative to CVD TiN. The alternatives to W as a contact plug include ECD Cu. The potential nucleation layers for Cu are discussed below while Ru [3], Co by CVD or ALD have been proposed for nucleation layers [4]. In the area of Al fill, the CVD Al nucleation layer may be extended to ALD to allow continuous improvement in the fill characteristics of this technology. Development is still underway for alternative materials and processes for high aspect ratio DRAM contacts, but ALD nucleation layers will likely be needed for this technology. For Metal 1, intermediate and global wiring, enhanced PVD Cu [5] deposited through various ionized techniques, occasionally combined with long throw, continues to be the dominant nucleation layer for ECD Cu. Improvement has been made in the sidewall coverage and uniformity of these layers, which will allow their use at the tightest dimensions of 22 nm technology. In addition, PVD Cu nucleation layers will continue to be used on the global wiring levels with larger critical dimensions. Eventually, these enhanced PVD techniques will not be able to provide reliable nucleation layers at the M1 and intermediate wiring levels and will be replaced by ALD technology, which includes obtaining Cu by hydrogen reduction. Several nucleation layer options, including electroless [6], ALD, and electrografted Cu technology [7], continue to be researched. Although ALD Ru [8] seems to be only a marginal barrier to Cu diffusion, it does appear to be a very good nucleation layer for ECD Cu. Therefore, it may be used in conjunction with other barriers, such as either ALD TaN or ALD WNC. Another potential solution to the problem of marginal PVD Cu sidewall coverage is repair of the nucleation layer [9] through ECD techniques. A more elegant solution involves modification of the ECD process and/or barrier to self-nucleation, thereby eliminating the need for a Cu nucleation layer.

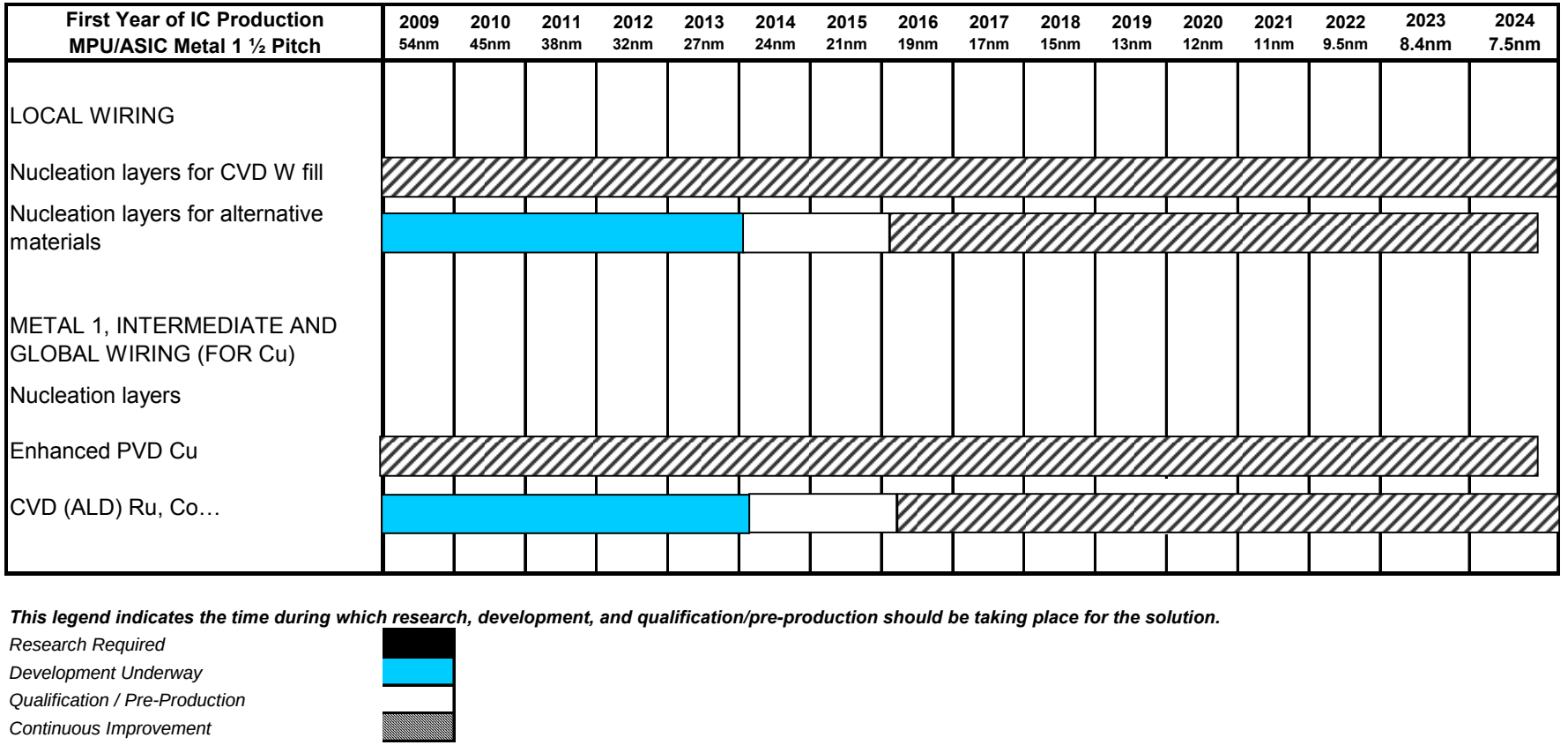


Figure INTC12 Nucleation Potential Solutions

CONDUCTOR POTENTIAL SOLUTIONS

Local wiring is limited to very short lengths and usually contacts adjacent transistors. Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, MPU/ASICs, Flash, and DRAM devices. ALD, in conjunction with CVD techniques, is being utilized first in the W deposition area. There has been a problem associated with the standard silane nucleation step in the CVD W process in that this Si-rich film takes up an ever-larger portion of the plug and will result in unacceptably high resistance for future technology generations. Modification of the process to minimize or eliminate this layer is an area of focus. Alternative materials and processes such as electroplated Rh [1] and electroplated Cu [2] which exhibit superfilling behavior are also being investigated as a replacement for W contact plugs. Continued development of ALD tungsten deposition will be needed to accomplish W fill of high aspect ratio (20:1 in 2009) contacts for stacked capacitor DRAM designs. Alternate materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts, which are projected to have aspect ratios greater than 25:1 by 2010.

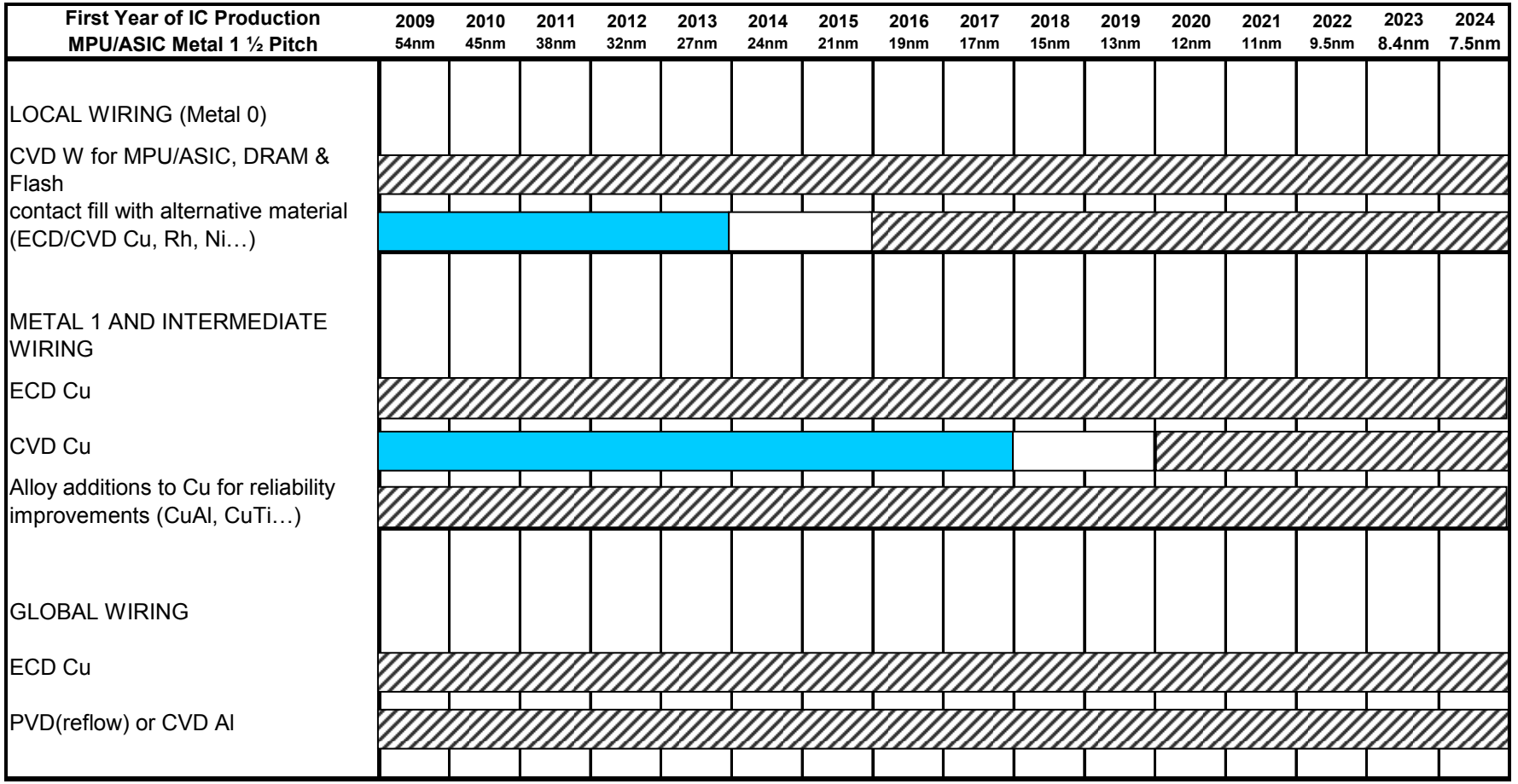
Cu will be the preferred solution for the Metal 1 and intermediate wiring levels in MPUs and ASICs and ECD continue to dominate the market in the near term [3-5]. There will be continuous improvement in plating chemistry and ECD tool design to allow seamless fill of smaller geometry, higher A/R structures. CVD technology is also needed for minimum feature sizes [6]. In the past few years, deposition and planarization in a single tool has been achieved by combining ECD with CMP ina form of chemically enhanced planarization (CEP). However, not having the Cu overburden present during the post deposition anneal is detrimental to grain growth and may impact reliability. This may limit the use of this CEP technology. It has been reported that even with the normal Cu overburden, there is ever increasing difficulty in transforming ECD Cu in minimum feature size damascene wires into the large-grain bamboo structures desired for good electromigration performance. As a consequence, Cu grain boundaries, as well as surface diffusion, must both be considered as potential failure modes for electromigration in the future. One potential solution to improving electromigration lifetime of the Cu conductor is through the use of Cu alloys such as Cu-Al [7], or Cu-Ti [8]. The alloying element is introduced through the use of PVD Cu alloy seed layers and then diffused through the entire conductor with a post-plating anneal. As one example of this, the use of this Cu-Al alloy along with an optimized Cu to dielectric cap interface resulted in a 50× improvement in electromigration lifetime. One downside to the use of alloying elements is an increase in resistivity when compared to the pure conductor.

Minimum feature size M1 and intermediate Cu wiring, in MPUs and ASICs, has already experienced a resistivity increase due to electron scattering [9-11]. The line lengths of these wiring levels tend to scale with technology generation so the impact on performance has been minimal. Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. The resistivity of the smallest pitch global wiring level is expected to increase about 40% by the end of this decade. This is more problematic, since global wiring traverses longer lengths and is more likely to impact performance than M1 and intermediate wiring. Cu interfaces, microstructures, and impurity levels will need to be engineered to alleviate the impact of this resistivity rise.

MPUs use a hierarchical wiring approach in which the pitch and thickness of the global wires are increased at each level. Indeed, the final global wiring level is little changed from one generation to the next and so will not be affected by electron scattering effects. In the 2009 table, the global wiring pitch will be estimated to be constant because significant changes are not expected. The resistivity of metals is a function of temperature and therefore cooling of IC chips is one potential solution to improved wire conductivity. However, this is probably not practical for most consumer and portable devices so it is likely that aluminum will continue to be used for global wiring and enhanced CVD/PVD flow techniques [12] will continue to be improved for damascene architectures.

Other design alternatives are the use of repeaters or oversized drivers, both of which impact chip size and power. The most likely near-term solution is the use of very high density TSVs as an enabling technology for three-dimensional chip stacking. This technology can reduce overall interconnect wire lengths while allowing incorporation of non-Si solutions for improved functional diversity. The other near-term solutions are judicious use of design and signaling options and packaging to minimize the effect of the narrower more resistive global wires. A great deal of research is underway on the use of either RF or optical techniques to resolve this issue. More radical solutions include superconductors, carbon nanotubes, etc. A full discussion of 3D IC, a proposed roadmap for high density TSV and other alternatives is contained in the New Interconnect Concepts and Radical Solutions section.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of MIM capacitors to improve yield and reliability. Both Al and Cu are in use for standard spiral inductors, but various magnetic materials may emerge with different inductor designs to reduce the area of these devices.



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement

Figure INTC13 Conductor Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Chemical mechanical polishing has become the standard technology for the planarization necessary to make leading interconnects. Any planarization process must produce an adequately flat surface across a wafer that is free of significant defects. This must be accomplished consistently and at a reasonable overall cost. Since feature size decreases and wafer size increases will continue, these planarization requirements become more severe over time. A brief overview of planarization technology, the latest problems, and potential solutions are discussed.

Before CMP, the main dielectric planarization techniques were processes such as bias CVD [1], TEOS-O_3 CVD [2] and Spin-On-Glass (SOG) [3]. Metal planarization was accomplished via processes such as reflow of Al interconnects [4] and etch-back after W CVD [5]. These technologies have largely been replaced by CMP for advanced devices. CMP, was initially adopted in early 80s, for ILD planarization. Since then, CMP has been adopted for a wide variety of structures and materials. With each technology generation, the number of CMP steps employed rises steadily[6]. Average process complexity is also rising as more materials need to be planarized within a single process step and as more CMP solutions involve multiple steps. All this is in addition to the significant challenge of meeting the new planarization needs for shrinking dimensions. An overview of planarization concepts is given in Figure INTC14.

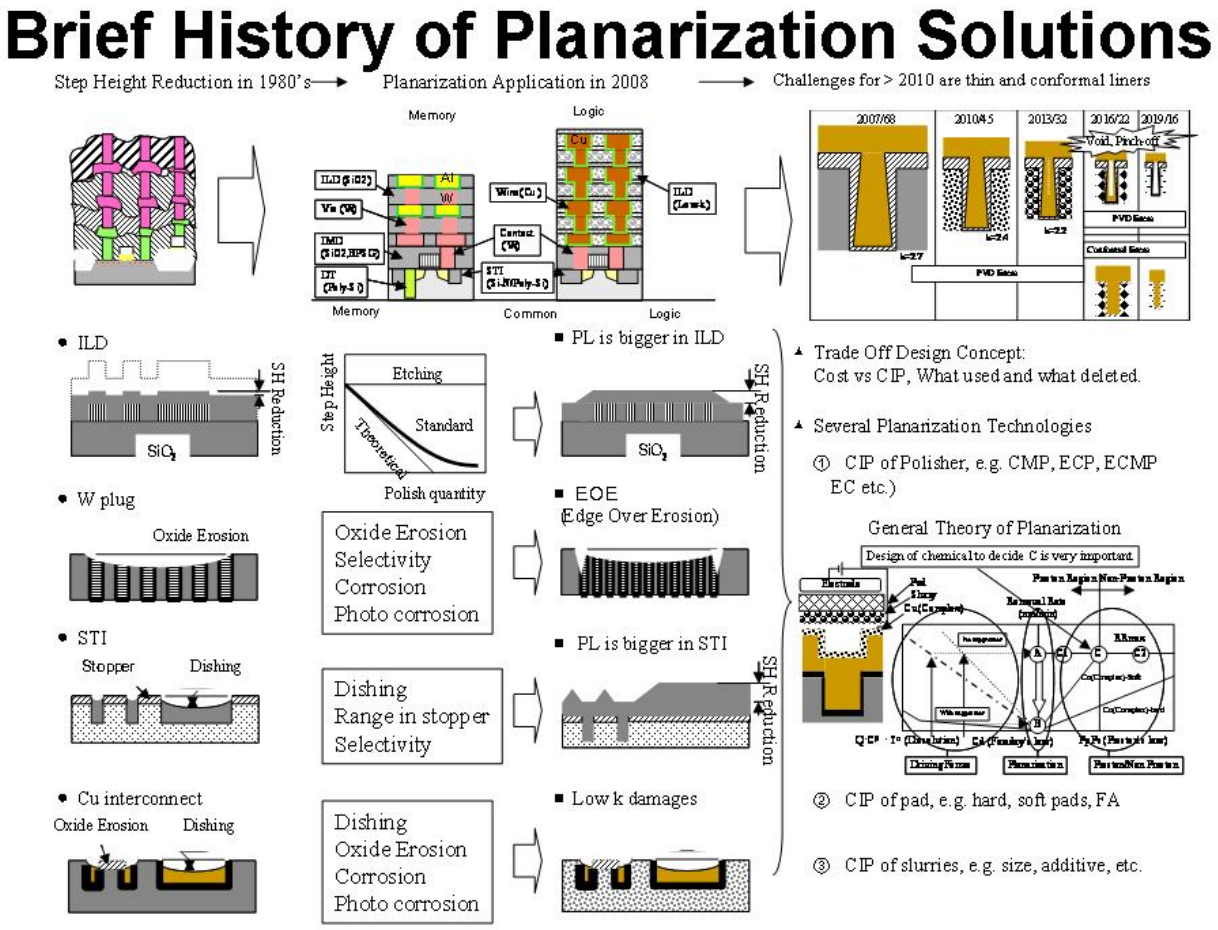


Figure INTC14 Brief History of Planarization Solutions

The planarization potential solutions chart, Figures INTC15 and INTC16, is broken into three sections. The first details a timeline for the major applications. This timeline serves as a preface to the potential solutions described in the equipment and consumables sections.

DIELECTRIC CMP

For most ICs, PMD CMP is the first interconnect planarization process. The PMD film is planarized and then thinned down to a desired target thickness over the gate stack. Defectivity is especially important for this step. It is standard in DRAM for the PMD CMP step to remove the dielectric down to the gate stack and stop on it with high selectivity.

The most common use of ILD CMP today is for the storage node and interconnects in memory devices. Figure INTC14 shows how ILD CMP can minimize step height created by lines and spaces. As scaling has progressed, the initial film profile entering CMP has drastically changed. Instead of creating a separate hump over each line, the dielectric creates a raised block or wide planarization length (PL) over the array of lines. The increased length effect has also been seen in shallow trench isolation (STI) CMP, which is discussed in the *Front-End Processes* chapter. In addition, nano-topography and roll off in the incoming material [7] need to be minimized to avoid affecting planarization performance. With scaling, the range in remaining thickness after CMP that can be tolerated also decreases.

Changes in structures and materials are leading to the creation of new planarization applications. Starting with 45 nm technology, metal gates were introduced. In the gate last integration scheme for creating metal gates, CMP of the pre-metal dielectric can be followed by a CMP step that polishes the nitride over the dummy gate while stopping on the pre-metal dielectric. CMP has been used as an option to aid lithography in double-patterning schemes and in planarization of photoresist for dual damascene patterning. The final backside Si thinning step for 3D-ICs can also be considered a new dielectric step where a high removal rate is desired.

CONDUCTOR CMP

The implementation of metal gates at 45 nm also led to a new planarization step. A bulk metal such as Al or TiN is deposited over the gate work function metal in the recess left by the dummy poly gate that was removed. The metal is polished back, stopping on the remaining pre-metal dielectric. Planarity and film loss control are important.

Polysilicon is still widely used for contacts and landing pads in DRAM technology. Over time, the contact process is moving from one that simply stops on dielectric to one that removes a combination of dielectric and nitride.

The first implementations of W for contacts and vias employed etchback processes. Manufacturability was enhanced by replacing these processes with CMP of the W and Ti-based liner. Leading logic devices today use W only at the contact level. In DRAM, the interconnect steps are migrating away from W and ILD CMP to Cu and barrier CMP. Due to the replacement of polysilicon etchback and emergence of double contact schemes, however, the overall number of W CMP steps is not dropping. An issue in W CMP has been the edge-over-erosion (EOE) effect where erosion increases at the edge of pattern arrays. This has been improved by development of slurries and pads. One avenue to improving overall planarity has been implementation of slurries with lower selectivity to dielectrics.

Cu and Barrier CMP involve more planarization steps than other layers. A multi-step process is performed in which the Cu is polished back to the Ta-based barrier layer and then Cu, the barrier, any hardmask material, and then the desired amount of dielectric are removed at rates that optimize the final topography and thickness. Corrosion including galvanic and photo-corrosion [8] is regarded as an eternal problem for conductor polishing in a conductive liquid. As technology progresses, the dielectric constant is being driven down. The combined effect of smaller features built from more fragile materials is driving the need to reduce maximum stresses applied during planarization in order to prevent structure damage. Stress improvements are being sought with CMP and alternatives such as Electrochemical CMP andChemical Etching (CE), and combinations of these are being investigated.[9] As the mechanical component of Cu removal is decreased, the chemical component is being increased. This must be done in such a way that corrosion protection is maintained and planarization is not only maintained but improved.

Barrier CMP processes for the future need to deal with these issues as well as additional concerns. As patterning and metal fill become more difficult, CMP is being asked to remove new barrier layers and an increasing number of dielectric or metal hardmask films. The effective dielectric constant needs to be minimized, which means polishing onto or into dielectrics with increasing porosity. Preventing change to the dielectric is being done through a combination of optimized CMP, post-CMP cleaning, and restoration techniques. Since the number of Cu and barrier steps in advanced flows is high, there is special attention placed on solving all the issues already mentioned in a way that drives throughput up and overall cost down.

Several new planarization applications for conductors are pending. W for contacts will eventually need to be replaced by a better conductor. New elements competing for adoption in barriers such as Ru, Mn, and Co will be needed and will add

challenges to the planarization processes. Porous dielectrics are likely to give way eventually to air-gap structures. A variety of non-volatile memory technologies beyond flash are being developed. Formation of the storage cells in those technologies is expected to shift towards damascene processing and CMP as they mature, which is being seen for the GeSbTe layer for PRAM today. As 3DIC technologies are becoming more widely adopted, improvements are needed in special high rate bulk metal and barrier processes to create those large features with low cost.

EQUIPMENT

Polishers with rotary motion and integrated cleaning, (called dry-in and dry-out), have been widely adopted. Although equipment is now more mature, modification and improvement must be continued to meet the needs of the new processes described above. Efforts to enhance Overall Equipment Efficiency (OEE) will also be continued. In addition, a new concept called "Trade-off design" in which parts necessary would be added and unnecessary parts abandoned is needed to decrease CMP equipment cost. Greater emphasis is being placed on endpoint and measurement capability which improve process control and non-uniformity. Endpoint metrology is preferred versus inline measurement, due to the delay between measurement and process adjustment. Barrier CMP is an application today in which measurement technology is used, but a true endpoint is desirable. Low pressure equipment is being designed to lower stress. Equipment must be created for novel low-stress planarization methods and must be designed together with the consumables. Both standard and novel methods need improvement in order to achieve tighter non-uniformities with smaller edge exclusions. The coming shift to 450 mm will drive a large amount of additional work.

CONSUMABLES

Consumables are the largest contributor to many planarization performance metrics, so significant advances will be required. High solids slurries utilized today are being driven to increased consistency, especially in defectivity. There is a drive to develop slurries which simultaneously lower defectivity, improve planarity, and decrease cost to support increasingly complex applications. Current trends to drive down solids and improve chemical activity will continue. The abrasives in use are increasingly being engineered specifically for CMP. They must have acceptable purity and unique surface and bulk characteristics. Robust processes are achieved by combining chemistries and abrasives in new ways. Many of the alternative planarization techniques will need new robust manufacturing-ready fluids in order to enable each technique. Cleaning chemistries must also be developed which optimize removal for specific slurries and substrates, without inducing issues such as corrosion. This challenge is especially steep for interconnects with porous films. New materials and form factors for the brushes in the post-CMP cleaners are needed.

Significant advances will also be needed from today's urethane pads to extend the range of hardness and chemical transport options for use across different applications. Pads containing abrasives are mainly used for STI. There is a strong need for development of a wide range of pad types that can be paired with slurries by application. Advanced pad conditioning methods are also needed, especially for new pad types.

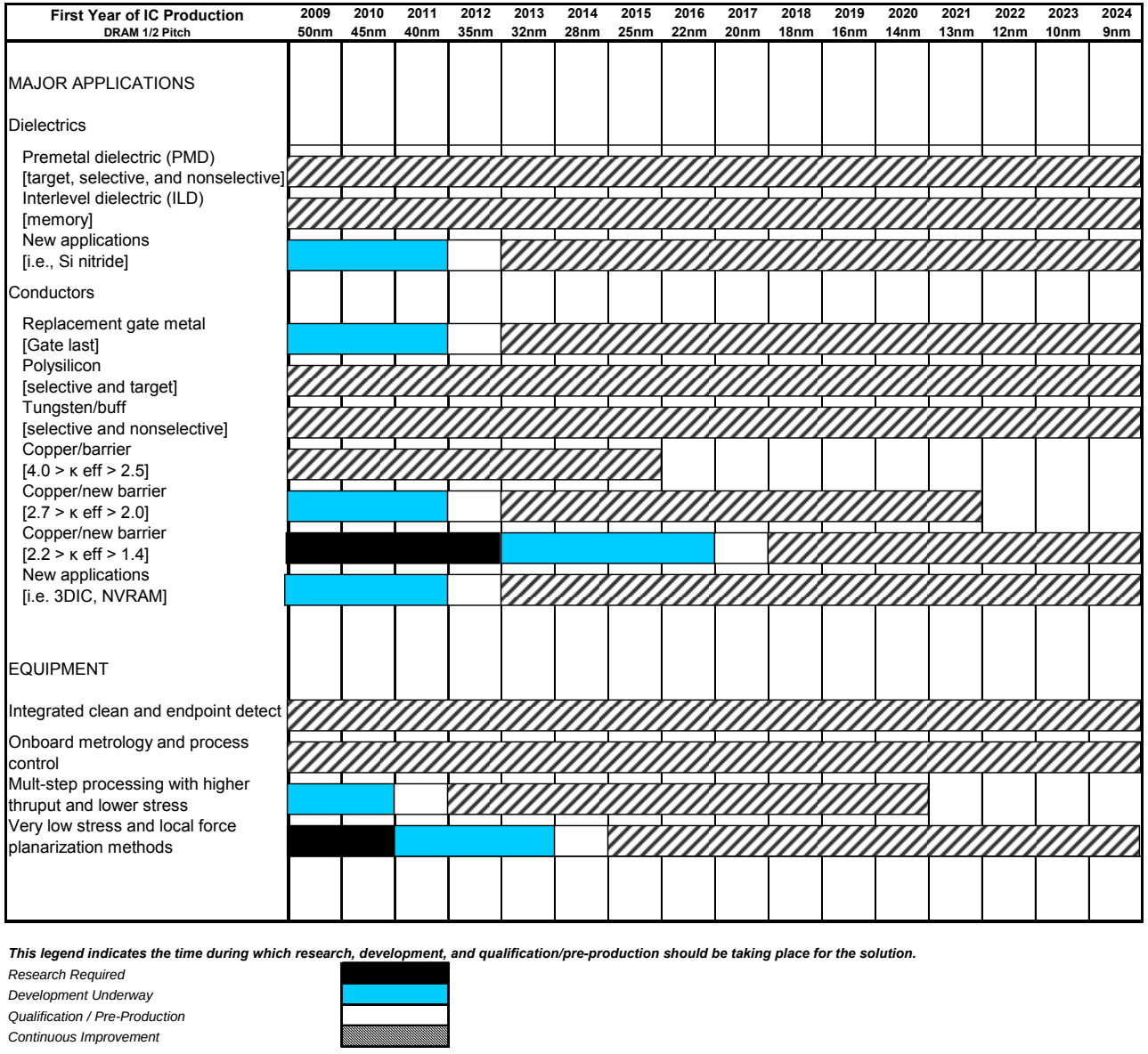
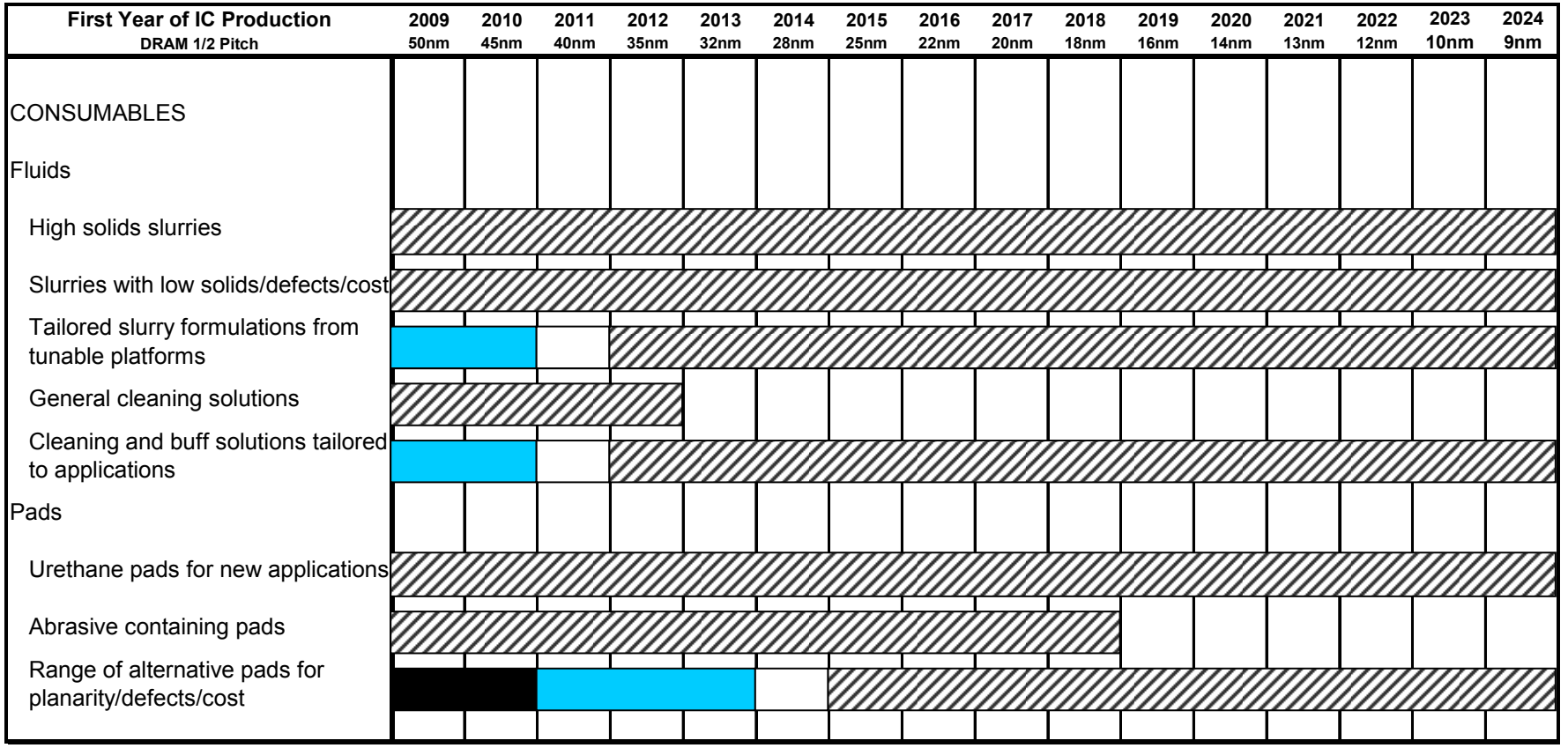


Figure INTC15 Planarization Applications and Equipment Potential Solutions



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement

Figure INTC16 Planarization Consumables Potential Solutions

THROUGH-SI-VIA (TSV), 3D STACKING TECHNOLOGY

INTRODUCTION

The 3D interconnect technology based on TSV interconnects basically consists of three main process modules: (1) the TSV module itself, (2) wafer thinning and backside processing, and (3) the die or wafer stacking process (permanent bonding and/or temporary bonding). Each of these steps requires rather specific equipment and process technologies and may be executed by different parts of the microelectronic supply chain. The discussion below on process modules is therefore organized along these three basic elements.

THROUGH SI VIA TECHNOLOGIES

A wide variety of techniques to realize via-connections through the Si-substrate of an integrated circuit have been proposed. The actual processing may be performed before, during, or after the IC fabrication process. Processing can also be done with the sole intention of forming silicon interposers without embedded active devices. However, a number of common features can be clearly defined: a hole has to be etched in the Si substrate; an isolation layer has to be provided to isolate the TSV electrically from the Si-substrate; a barrier layer has to be provided to prevent diffusion of metals into Si, and the via must be filled with a conductive material. The most common approaches to TSV technology are to provide for the TSV function before finalizing the wafer, (prevalent for 3D-SIC technology) or to realize the vias after finalizing the wafer (prevalent for 3D-WLP technology).

TSV ETCHING TECHNOLOGY

TSV holes are generally not etched through the entire wafer. Wafer processing with actual through-Si holes is not compatible with standard semiconductor or wafer-level-packaging processes and equipment. The prevalent technology is to use a "blind" via approach. The TSV is etched to a certain depth or until an etch-stop layer is reached, as shown in Figure INTC17.

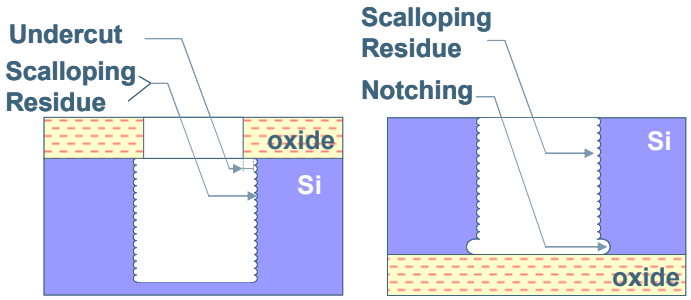


Figure INTC17 Schematic Representation of the Challenges for Si-TSV Plasma Etching

ETCHING THROUGH MASK, OXIDE OR BEOL LAYERS

Depending on the actual integration scheme used, etching a via hole in the Si substrate may require etching through resist, oxide or BEOL layers such as SiO, SiN, SiON, SiO(C) and, in certain cases, low-κ materials, as indicated in Figure INTC17**.** Before etching the TSV-via in the Si, the masking layers have to be etched. This can be done using a separate tool or chamber prior to the Si-etch or in the same tool as the Si-etch. Depending on the selectivity of the Si-etch with respect to the passivating or masking layers, there will be etch process development challenges when thick passivating/masking layers are used. There are also concerns with Si etch undercutting below the patterned passivating/masking layer.

ETCHING HIGH ASPECT RATIO SI HOLES/TRENCHES

The actual fabrication of the Si hole is commonly realized by plasma etching. A specific feature of TSV Si via etching is the need for etching deep, and often high aspect ratio holes in Si. This may require long processing times on expensive equipment, so fast etching processes are highly desirable.

Critical aspects of via hole etching include good control over sidewall tapering angle (both global and local), minimal sidewall roughness and scalloping, minimal residue/defect issues, minimal undercutting and notching issues, minimal local bowing effects right below masking layers, respectable etch rates, and excellent repeatability and within wafer center-to-edge depth and profile uniformity.

In order to avoid isotropic etching of the Si, the etching recipe balances sidewall passivation with bottom Si-etch process chemistries. The prevalent technique used is the "Bosch" recipe, in which passivation and etch steps alternate in time. During the passivation step, a polymer is deposited on the Si surface. During the Si etch step, the polymer is easily removed from the bottom surface of the hole, while remaining on the via sidewall, protecting the previously etched Si sidewall. An undesired characteristic of this technique is "scalloping" on the Si sidewall, as can be seen schematically in Figure INTC17. The periodic circular ridges formed along the perimeter of the sidewall after each cycle can add complexity to the the following steps.

Depending on the critical dimensions, aspect ratio, and final depth of the TSV etch process, there are also non-Bosch RIE process solutions which may be used. These usually involve hardware upgrades, followed by advanced process development to existing CMOS plasma etchers (oxide or polysilicon) [1] and primarily address three main attributes unique to the nominal feature size of a TSV structure: 1) high etch rates on the order of 5–15 microns per minute, 2) high anisotropicity/ability to modulate the taper angle, and 3) high selectivity to Si etch. From a manufacturing perspective, the main advantages of the non-Bosch RIE process over the Bosch process include smooth sidewalls with no scalloping; ability to modulate sidewall tapering angle; re-use of existing tools; minimal F-containing polymer residues, and minimal undercutting. It is noteworthy that when the critical dimension becomes too small (usually less than 1 micron) and the aspect ratio becomes too high (usually greater than 20:1), the type of RIE used may tip to favor Bosch etch.

After etching, cleaning the Si via hole is a critical process. In particular, the F-containing polymers deposited during the passivation cycle of a Bosch etch need to be fully removed before further processing.

Another inherent characteristic of deep Si etching processes is the aspect-ratio dependent etch rate. As vias are etched deeper into the Si wafer, or as viadiameter decreases, etch speed goes down. This typically causes a linear dependence between the average etch rate and the feature size aspect ratio. The consequence is that CD control for TSV patterning is critical to obtaining a uniform wafer-to-wafer processing speed.

TSV LINER PROCESS—ISOLATION LAYER, DEFINES TSV CAPACITANCE

In order to electrically isolate the TSV connections from the Si substrate, an isolation layer is required. The key requirements for this layer are that it should exhibit low leakage current, sufficiently large breakdown voltage, and low capacitance.

Deposition of the TSV liner layer must be compatible with the device process flow. For the deposition temperature, this implies for "via middle" a deposition temperature acceptable to the front-end process devices and for "via last" deposition temperatures, acceptable temperature for the back-end interconnect processes and, when processing on carriers, compatibility with the temporary bonding materials. In particular, for post-processing on DRAM memory devices, temperatures below 200°C may be required to avoid damage to device wafers.

Ideally this layer should planarize the Si sidewall roughness (e.g., scallops from Bosch etching). Conformal deposition on sidewall scallops may cause a more difficult surface topology for the following processing steps.

The most popular liners are oxide or nitride layers, deposited by CVD, although PVD techniques are also being evaluated. Obtaining a conformal fill is more difficult at low processing temperatures. Nitride results in a higher capacitance, but can also act as a barrier layer to prevent metal diffusion.

For 3D-WLP via-last TSVs, the use of polymer isolation layers is also possible. This allows for a significantly lower capacitance of these larger diameter structures and also allows the metal in the TSV structure to absorb some strain. [2]

TSV BARRIER LAYER

In order to avoid migration of TSV metal into the Si, a high quality, pin-hole free barrier layer is required. The prevalent barrier materials are Ta and TiN, which also improve adhesion between the TSV metal and the liner.

Prevalent technologies for barrier deposition are PVD and CVD. Different forms of CVD allow for barrier deposition on the most challenging, high aspect ratio TSV via holes. PVD technology has more limitations, with respect to coating

conformality and via aspect ratio, but is often preferred because of superior adhesion, the barrier properties of films and lower operational costs. Improvements in PVD equipment have extended the process window for PVD barrier deposition.

TSV METAL FILL PROCESS

The main approaches to realize conductive TSV structures are using electrochemical deposition (ECD) of Cu, CVD of W, CVD of Cu or, for via first approaches, poly-Si via fill. Several process options for Cu or W fill are available, and are discussed in more detail below. Figure INTC18 maps the different process options for Cu and W-based TSVs as a function of TSV diameter and aspect ratio, in relation to the 3D-TSV roadmap.

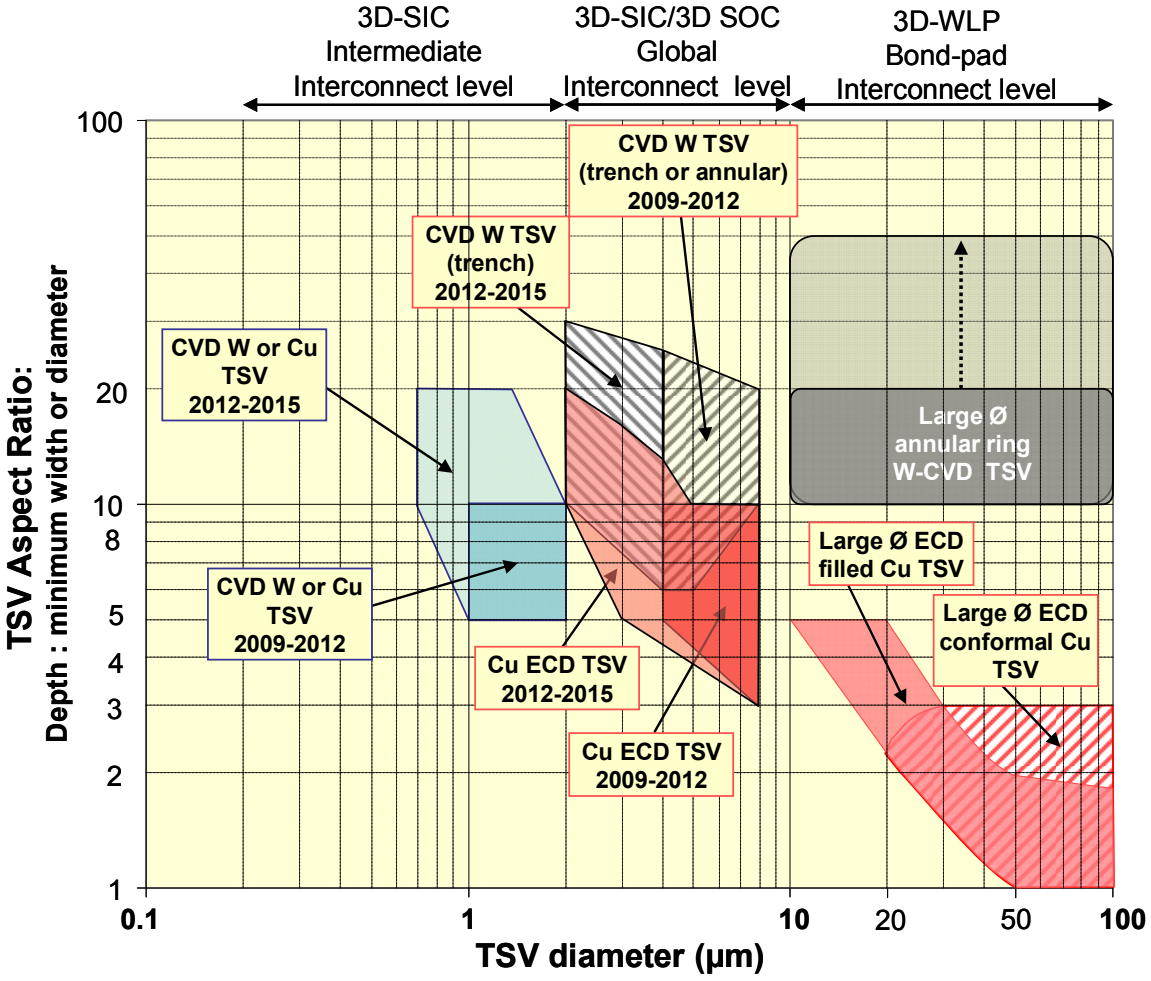


Figure INTC18 Cu and W-based TSV Options as a Function of TSV Diameter and Aspect Ratio, in accordance with the 3D Interconnect Hierarchy and Roadmap

(Trench and annular TSV refer to non-cylindrical TSV shapes which are narrow in one lateral dimension.)

Cu TSV

The process steps in Cu TSV are: Cu seed deposition, Cu-via fill by ECD, and CMP removal of Cu-overburden.

The prevalent technology is derived from commonly used single damascene Cu plating BEOL processes. The main difference is the high aspect ratio of the Cu TSV features.[3]

For the Cu seed deposition process, the prevalent technology is PVD. The main challenge is to obtain a continuous Cu seed layer in high aspect ratio TSV structures. The highest TSV aspect ratios successfully realized using Cu PVD are 5 to 10. Alternative technologies for high aspect ratio TSVs are CVD Cu, electrografting of Cu seed layers, and direct-on-barrier plating.

The main challenge for the ECD Cu filling process is to realize void-free Cu-filling of the Cu-TSV structures. This requires a "superfilling" of the etched via structures. This is achieved by carefully controlling additives to the plating solution which accelerate plating in the bottom of the via and suppress and smooth plating on the wafer top surface. The resulting processes are slow and require equipment that can run multiple wafers in parallel on a single tool.

After ECD Cu deposition, the Cu is annealed. A typical via-middle process is followed byCu-CMP. In addition to the Cu CMP, the barrier and liner layer must be removed to allow further BEOL processing.

W TSV—W CVD FILL, CMP

CVD can be used to fill narrow TSV structures with large aspect ratios. TSV with diameters up to 3µm have been reported. [4] Larger TSV structures are realized by combining multiple TSVs in parallel, using narrow slits or using annular ring TSVs. The W CVD process is highly conformal. A typical W TSV filled structure is characterized by a center-seam void.

Since relatively thick tungsten layers are required to fill the TSVs, a partial blanket W etchbackto a resulting film thickness < 500 nm is carried out, avoiding any peeling or delamination. The partial etchback also helps to decrease wafer bow to a moderate level.

After CVD W fill, the typical process consists of W CMP to remove the W on the wafer field. After this step, a barrier/liner layer CMP may have to be performed to allow for further wafer processing.

As an alternate to W CMP step, an etchback process can be used to define the contact pads to the W TSV structures. [5]

POLY-SI TSV: VIA-FIRST TECHNOLOGY

For via-first technologies, Cu and W TSV cannot be used because of compatibility problems with the FEOL process. Poly-Si can be used as a TSV fill. In this case, only a liner (no barrier layer) is required. After polysilicon deposition the wafers are polished and the standard Si process flow can be performed. This requires high quality pre-processing steps to avoid yield loss during device manufacturing. The higher resistivity of polysilicon limits the use of this approach to applications that allow for high-impedance TSV interconnects.

WAFER THINNING AND BACKSIDE PROCESSING

TSV BEFORE 3D-BONDING

This is a parallel processing approach to 3D integration. Wafers are prepared for 3D stacking by performing TSV processing and contact pad formation in parallel. At the end of the process, the different die or wafers are combined to realize the 3D-stack. (See Figure INTC19.)

Realizing TSV-vias before 3D-bonding implies processing on thinned wafers. For a via-last process this can be the actual fabrication of the TSV connections. For via-first and via-middle processes this typically consists of processes to expose the TSVs on the wafer backside, provide a backside passivation, and create redistribution and bump structures on the wafer backside. These processes may be extensive and require relatively high temperatures.

For flows using wafer thinning before bonding, a robust thin wafer carrier process is required. The requirements for 3D-stacking are significantly more stringent than classical wafer thinning and singulation processes used for 3D-SIP applications and require dedicated solutions.

The key steps for this process are as follows:

1. Thin Wafer Temporary Carrier Systems

   The thin wafers carrier system should allow for extensive post-processing of the thinned wafers in standard semiconductor processing tools. The temporary glue layer between the thin device wafer and the carrier should be stable during all the (high temperature) TSV processing steps and should be able to detach, without leaving residues or damaging the thin 3D die.

   Two main strategies are followed:

   a) One strategy is to use glass substrates as carriers. This allows for the use of optical techniques to cure (e.g., UV-cure) or debond (e.g., laser ablation) the carrier wafer from the thin TSV wafers at the end of the process. It also allows for optical back-to-front alignment for backside processing. Disadvantages of glass carriers are the need for

special Si CTE-matched glass, the cost of the carrier wafers, and compatibility with standard semiconductor processing tools.

b) The alternative option is to use Si wafers as a temporary carrier substrate. A typical process flow is shown in Figure INTC19. In order to avoid problems with the razor-sharp edges of silicon wafers after thinning, wafer edge trimming is performed. As a result, the thin wafer has a smaller diameter than the carrier wafer after thinning. This allows for more robust handling of the wafer in standard semiconductor equipment.

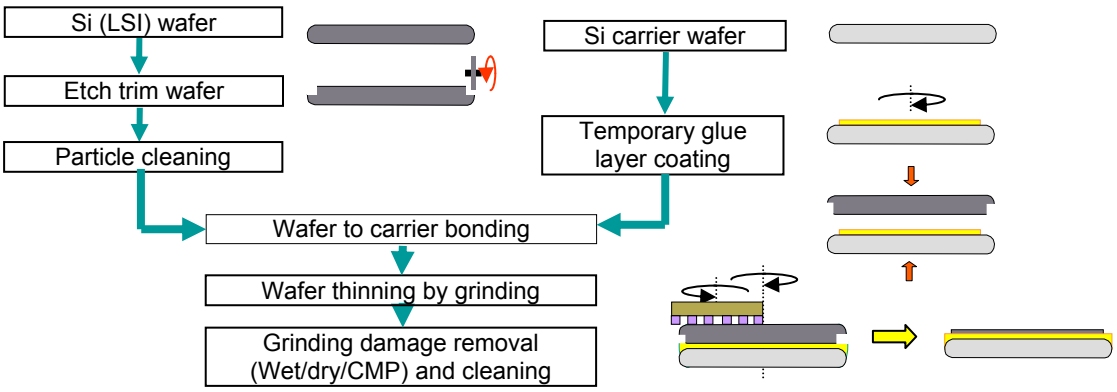


Figure INTC19 Temporary Carrier Strategy for Thin Wafer Post-processing

The temporary glue layers for this process are challenging and critical to the success of 3D-integration schemes. A complex combination of properties is required: Stability during processing with the capability of easy debonding. A wide variety of debonding mechanisms is being studied, such as laser-assisted (glass carriers), melting and sliding (thermoplastic adhesives), dissolution in solvents, and mechanical debonding (peeling).

2. Wafer Thinning

Wafer thinning by grinding is a well established process in semiconductor packaging. Critical for TSV technology is Si thickness control andsurface quality. The total thickness variation of the thinned wafer is a combination of the thickness variation of the carrier wafer, the temporary glue layer thickness variation, and the accuracy of the grinding tool. After mechanical grinding of the wafer, a thin damaged Si layer is present on the wafer backside. CMP, dry etch and wet etch techniques are used to remove this damaged layer. When grinding Si wafers with already processed TSV structures, particular attention must be paid to exposing the TSV structures from the wafer backside. This may require additional processing steps.

3. Wafer Cleaning After Thinning.

Mechanical back grinding may leave particles on the wafer backside. In order to allow re-introduction of these wafers into a process line for backside processing, a thorough particle cleaning is essential.

4. Wafer Backside Process Requirements

The thin wafer on carrier must be compatible with standard semiconductor processing equipment to allow for processing such as:

- Via-last TSV processing (particularly typical for 3D-WLP)
- Backside wafer passivation
- Optional backside interconnect redistribution
- Backside interconnect “bumping”

TSV AFTER STACKING OPTION

This is a sequential processing approach to 3D integration. Wafers are bonded together before 3D TSV processing. The process is repeated for multiple tier stacking. As a result, the bottom wafer goesthrough all TSV-processing steps:

- Wafer-to-wafer permanent bonding to bottom wafer or wafer stack
- Wafer thinning, total thickness variation and Si-surface quality, impact on devices
- Wafer cleaning after thinning, allowing re-introduction into a process line for further processing
- Wafer backside process requirements, TSV or pad metallization layer process

STACKING TECHNOLOGY MODULE

- Wafer-to-wafer bonding approaches:
  - Polymer or oxide W2W bonding
  - Metal to metal W2W bonding
  - Metal/oxide or metal/polymer W2W bonding

- Die-to-die or die-to-wafer bonding approaches:
  - Metal/metal thermo-compression bonding
  - Cu/Sn and similar μbump interconnect techniques
  - Other approaches: e.g., caulking

RELIABILITY AND PERFORMANCE

RELIABILITY INTRODUCTION

Rapid changes are occurring in interconnect materials and structures resulting in significant new reliability challenges. Failures are further exacerbated by continued increases in interconnect density, number of layers, and power consumption.

An interconnect system is typically composed of insulating dielectric materials and conductors arranged in a multilevel scheme, followed by chip packaging. In the case of Cu-based metallization, metallic and dielectric diffusion barriers are used to prevent copper migration into the dielectric. Each of these components plays an important role in the reliability of the system. The implementation of today's copper low-κ interconnects is strongly impacted by reliability, both for metals and dielectrics.

Metal reliability is generally assessed by studying electro-migration (EM) and stress induced voiding (SIV), while dielectric reliability is assessed by leakage and time dependent dielectric breakdown (TDDB) or triangular voltage (TVS) sweep measurements. Numerous novel barrier metals, alloys of copper and copper cap layers were recently proposed in order to cope with the increasing current density that conductors have to carry. While the theoretical description of the EM phenomenon is well-understood, due to the large number of possible combinations, careful testing of these schemes is important, in order to identify active failure mechanisms. As dielectric spacing between adjacent copper wires scales, BEOL dielectric reliability is becoming an increasingly important challenge, both for advanced logic and for memory devices.

While concerns regarding the importance of dielectric reliability are widespread in the community, strategies to assess and predict the expected lifetime at product level are lacking in consensus. It is commonly acknowledged that ensuring the necessary low-κ dielectric reliability margins is increasingly difficult [1-3] and that the importance of BEOL dielectric reliability increases with dimension and material scaling. The lack of consensus and of a fundamental understanding of BEOL dielectric reliability models, statistics and dominating controllable factors, calls for concentrated efforts on this topic.

Identification of failure modes and establishing correct prediction models is crucial. These models can be used for predicting reliability limits of entire circuits and of systems. In some cases, by monitoring the degradation of system and circuit parameters (due to degradation of metals and dielectrics) it may be possible to extend the reliability limits of the entire system by reducing the workload on one part of the circuit. Finally, in the context of full IC-system reliability, chip package interactions should not be neglected.

METALLIZATION RELIABILITY

ELECTROMIGRATION

Electromigration failures are generally described with Black's equation [4] which determines the maximum current density (J_{EM}) which can safely flow in a wire. The most common metals in today's ICs are aluminum and copper. Cu

interconnects were introduced in 1997, in a damascene scheme, to reduce wiring delay, but Al interconnects remain for specific applications and at several levels in multilevel interconnects. Electromigration limited current is currently investigated in Al interconnects using the usual EM physics rules.

ELECTROMIGRATION SCALING MODEL

In an interconnect subjected to an electrical current, the Cu atomic drift velocity is determined with an effective diffusion coefficient whichtakes into account the possible atomic diffusion paths existing in a metal [5]. An experimental EM activation energy (0.9eV) has been agreed upon and shown to remain constant over the interconnect nodes for the most common integration scheme: dual damascene Cu with a PVD TaN/Ta sidewall barrier and a Si(C)N dielectric cap layer. Following this, it is straightforward to consider that the EM-induced void growth rate remains constant for a given interconnect scheme, independent of interconnect geometry. Some authors report a risk of grain boundary diffusion in very narrow linewidths associated with an Ea =0.85eV. [6]

The lifetime (τ) of an interconnect is the time to reach the minimum void size which is able to electrically open the interconnect. Using the assumption, that the void is located at the cathode end of the interconnect wire containing a a single via, it has been shown [7] that τ scales with w*h/j, where w is the linewidth of the interconnect (or the via diameter),, h the interconnect thickness, and j the electrical current density responsible for electromigration Cu diffusion.

J_{EM} is the maximum current density providing the targeted lifetime and scales with the product w*h. J_{max} is defined by the maximum equivalent dc current expected to appear in a high-performance digital circuit divided by the cross-sectional area of an intermediate wire, which was calculated by the model shown in Figure INTC20. The comparison of the evolution of J_{max} and J_{EM} limited by the interconnect geometry scaling is shown in Figure INTC21. J_{max} increases with scaling due to reduction in the interconnect cross-section and increase in the maximum operating frequency. J_{max} will exceed the J_{EM} limit of conventional copper interconnects.

Process options should be oriented towards solutions to decrease Cu drift velocity. [8] Recent research has shown that there are at least three main experimental directions to reduce Cu drift velocity or significantly increase E_a to reach E_a~1.5eV:

1. Cu surface engineering before the SiCN deposition layer, also referred to CuSiN cap
2. Replacing the actual dielectric capp Si(C)N by a metal cap based on Co alloys such as CoWP
3. Adding Ti, Al, Mn, Ge doping of Cu seed layer

One should pay attention to the possible interconnect resistance increase of such Cu alloying processes. (See also Figure INTC22 to compare the lifetime improvement versus the resistivity increase.).

BLECH LENGTH EFFECT TO RELAX J_{EM}

From early studies of electromigration, it has been shown that short length interconnects (also called Blech length L_B) could be immortal [9]. Immortality is reached for any current density or wire length below the critical product: $J_C * L_B$. This critical product is the consequence of the mechanical confinement of the metal in the interconnect structure. Experimental research indicates a rather wide range of this immortality criteria with $J_C * L_B$ ranging from 1500 and 5000 A/cm.

More recently, it has been shown that other immortality criteria can be considered to model electromigration behavior in actual interconnects. [10] This proposal is based on the observation that a void can nucleate and reach a saturation size as the consequence of the backflow effect first proposed by Blech. [11] There are current and length conditions in which a stable void is created in the interconnect without an open circuit. Today, there are no metrics available for a more appropriate critical product.

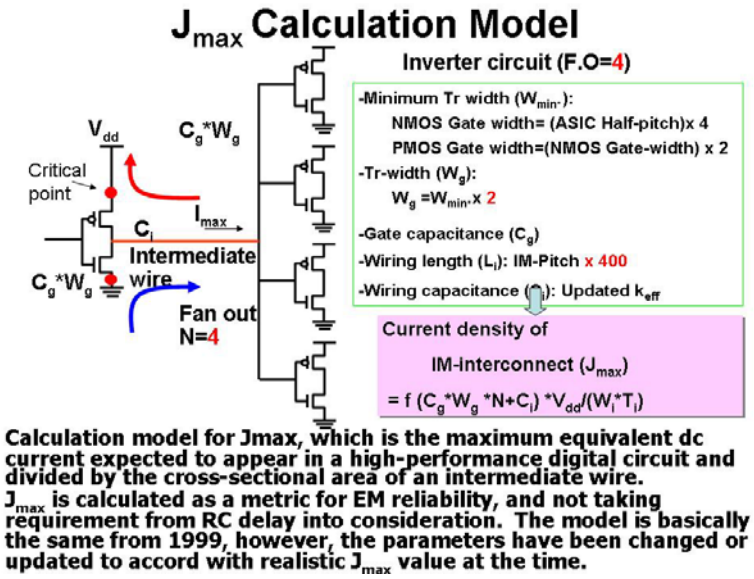


Figure INTC20 Calculation Model for J_{max},

(The maximum equivalent dc current expected to appear in a high-performance digital circuit divided by the cross-sectional area of an intermediate wire.)

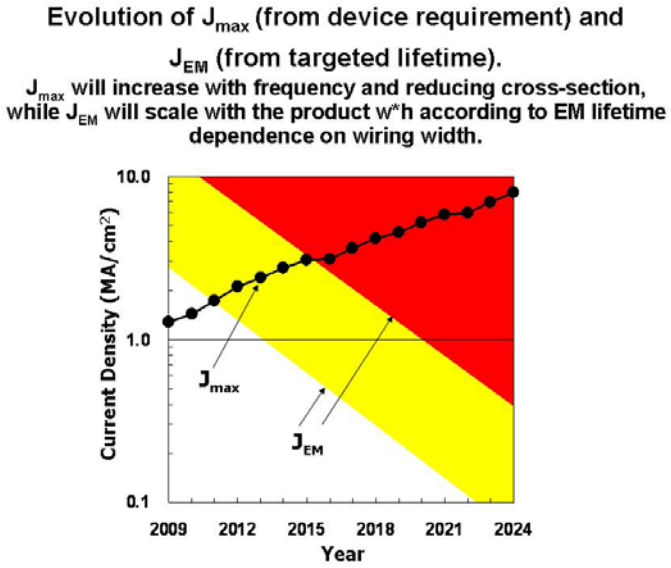


Figure INTC21 Evolution of J_{max} (from device requirement) and J_{EM} (from targeted lifetime)

*(J_{max} will increase with frequency and reducing cross-section, while J_{EM} will scale with the product w*h according to EM lifetime dependence on wiring width.)*

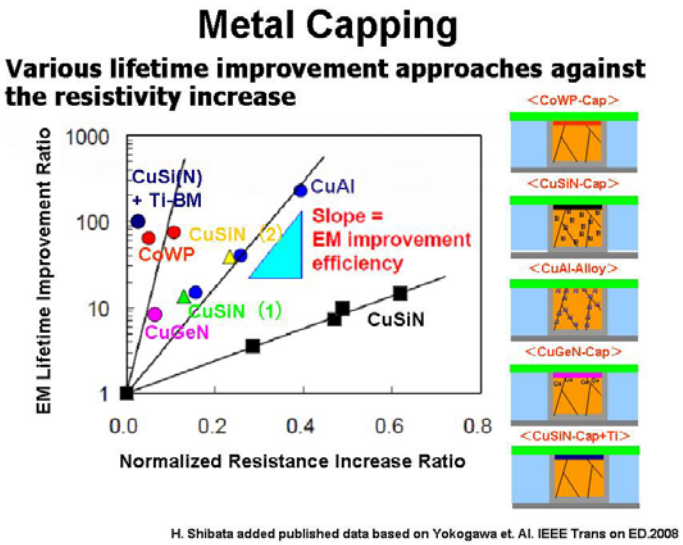


Figure INTC22 Comparison of the Lifetime Improvement versus the Resistivity Increase for Different EM Resistance Booster Technologies[7]

STRESS MIGRATION

Stress induced voiding (SIV) is the result of vacancy movement driven by stress gradients in and around vias that are connected to different metal layers. According to the literature, SIV can happen both below and in vias. To get voiding below a via, the main vacancy diffusion path is the copper cap interface (and possibly the grain boundary) and a reservoir of vacancies needs to be present in the metal layer under the via [12]. To get voiding in a via the main diffusion path is the copper barrier interface and a reservoir of vacancies needs to be present in the via itself. The literature attributes voids in vias to non-optimized via processing [13, 14]. A way to eliminate this failure mode is appropriate via to line geometry design,with large metal reservoirs prohibited and with linewidth ~ via diameter.

DIELECTRIC RELIABILITY

TIME DEPENDENT DIELECTRIC BREAKDOWN

Time dependent dielectric breakdown (TDDB) has rapidly gained wide acceptance as the test method of choice for assessing BEOL dielectric reliability. While a large number of factors and mechanisms have already been identified, the physical understanding is far from complete. The role of the CMP interface on TDDB lifetime was recognized early and analyzed in great detail [1]. Accordingly, plasma treatments were optimized to allow for copper-oxide reduction left after aCMP surface was exposed.

Recently, a quantitative relationship between the amount of copper residue and dielectric reliability using partially patterned damascene wafers was established [15]. It was found that at least 10^{12} atoms/cm^2 of residual copper are necessary for observing a noticeable copper-induced degradation. In these investigations, the degradation itself was not linked to copper migration during the electrical stress, but simply to the presence of a small amount of copper residue before even starting any reliability testing. Other investigations propose a link between copper drift and observed dielectric reliability during operation [3].

Another well documented damascene low-κ integration issue relates to the degradation of the inter-metal dielectric during the patterning steps. When CDO, OSG (or SiCO:H) dielectrics are exposed to patterning plasmas, unwanted modifications, such as carbon depletion and the incorporation of silanol groups can occur. While the aforementioned effects have been identified and are being addressed, their interaction and the interrelation of damascene fabrication steps require further efforts. At this stage, the failure is generally attributed more to the integration scheme than to the intrinsic material properties of the dielectrics.

[7] *(Modified from the figure by S. Yokogawa et al., IEEE Trans. Electron Devices, Vol. 55 (2008) pp.350-357.)*

TDDB investigation under dynamic conditions is important, but rarely assessed. On one hand, with changing polarity (AC versus DC [16]) defect relaxation can occur, which results in longer lifetime. On the other hand, a typical interconnect structure is metal-insulator-metal type, where the dielectric defects that are created during stress cannot be healed and hence the expected lifetime increase by this effect is small. Interaction of TDDB with other phenomena such as EM, SIV, adhesion stresses, etc. has not yet been properly addressed.

Air-gap integration changes the relevant physics. For air gaps, only interfaces are expected to contribute, hence the reliability margin can be potentially better or worse than that of intermetal dielectrics, depending on the interface quality. For example, some air-gap schemes remove the critical CMP interface contribution.

Besides TDDB, TVS and various V-ramp methods can be used for identification of electrically active components. In general, stress conditions more closely resembling real situations are desirable. Finally, establishing intrinsic reliability specifications and limits is expected to become very important.

IMPACT OF LER AND VIA MISALIGNMENT ON DIELECTRIC RELIABILITY

The electric field between wires is locally enhanced by the presence of LER and misaligned vias (MV). LER originates from lithography and etching of transistor gates and wires. It consists of an irregular side profile of the patterned poly or metal lines, featuring protrusions and notches with nanometer range amplitude. MV in interconnects are due to alignment limitations in patterning steps. In both cases, the field enhancement is caused by two distinct effects, namely the local space reduction between the wires and the increase of density charge in LER protrusions and in the steps formed by misaligned vias. Neither LER nor MV amplitudes scale with wire dimensions. Their relative importance becomes more pronounced with more advanced technology nodes.

LER and MV coexist in wires and the consequent field enhancement is not negligible in narrow lines. For short lines (~10μm) with vias, the impact of LER becomes probabilistic; in other words, the shorter the line, the more likely that the impact of MV is predominant. On the other hand, long lines (> 10μm) will have the contribution of both MV and the full LER contributions to field enhancement; one of these effects will be predominant according to the relative contribution of these two field enhancement factors in different scaling scenarios [17].

RELIABILITY ASSESSMENT, MODELING AND SIMULATION

TDDB acceleration models are fundamental for describing and predicting dielectric reliability margins at operating conditions. Typical tests are conducted at high electric field and these data are used for predicting lifetime at operating conditions. This often involves extrapolation of the data over several orders of magnitude. This is clearly an area where progress has to be made, because there is no consensus on prediction. As of today, the most conservative E-model is often used for prediction. However, there is significant work [3, 18] showing that the extrapolation to low field is characterized at least by a square root-E dependence. Such equations were derived from conduction mechanisms of electrons as well as from copper drift related phenomena. All acceleration models critically depend on the electric field. There are a number of factors that lead to local field enhancement in interconnects. Intrinsically, porosity introduction into a low-κ material is important (electric field enhancement induced by presence of pores) together with line edge roughness which does not scale with materials.

The electric field enhancement caused by LER has an evident impact on TDDB in advanced wire architectures. For long wires, the LER enhancement coexists with the area scaling, thus further reducing the predicted lifetime without LER; accurate TDDB prediction models must take this effect into account [17, 19, 20]. Models should account for these effects as well. Furthermore, there are extrinsic layout and interconnect shape-related field enhancement factors that need to be taken into account, since electric field enhancement locations are expected to be critical. In particular, the layout topology (regular versus irregular) and hence the correspondent application (memory versus logic) determines the presence of specific features (wire corners, turnings in the wires, sloped wires, misaligned vias, local cross-section asymmetry) which need to be modeled. Typically used damascene TDDB test structures are meander-comb, comb-comb, parallel lines or via chains. Length dependence as well as the layout effects need to be characterized in order to relate these to real products. Once the models are known, they can be linked to tools for predicting system level behavior. In that respect, gradual wear-out phenomena are of particular interest, because they cause gradual slowing of the interconnect wiring, which can be addressed at system level, although today's tools fail to incorporate them. To date, the most commonly observed dielectric failures are linked to hard breakdown or abrupt failures. Nonetheless, soft breakdown and gradual wear-out have also been reported in a few cases, which deserve attention [21].

Electron and ionic transport in dielectric materials needs to be understood and described in order to predict current levels. Recently, the defect properties of low-κ materials were studied by using photoemission [22, 23]. The defect density from

measuring transient currents, after photo excitation was stopped, was also derived— a value of about 6 x 10^{16} traps/cm^3 was obtained, which is orders of magnitude higher than typical trap densities in silicon dioxide. It is apparent that low-κ dielectrics are "intrinsically defective," when compared to SiO_2. Yet, the relation of defects to conduction and, in genera l the identification of electrically active defects still pose a challenge.

FUTURE CHALLENGES AND DIRECTIONS

- Description of the temperature and voltage acceleration of the dielectric lifetime, based on a commonly understood and acknowledged physical mechanism.
- Standardization of test methods (test conditions, structures, etc.).
- Setting of dielectric reliability figures of merit, commonly acknowledged by the interconnect community.
- Regular update of reliability understanding and consequent specifications in the roadmap, since materials and integration approaches are changing rapidly. Two examples: ultra low-κ, air gaps.
- Identification of electrically active defects, which are responsible for conduction in dielectrics.
- Study of the interaction between different reliability phenomena (e.g., metal/dielectric interaction).
- Study of the cumulative impact of co-existing reliability factors on interconnect lifetime, to be included in the mentioned figure of merit.
- Study and analysis of chip package interactions from the reliability point of view.
- Assessment and prediction of dielectric reliability at system level.
- Reliability with Pb-free and environmentally friendly materials

By adopting state-of-the-art reliability models, together with stress conditions extracted from real applications running on real ICs, it is possible to create a system level time-dependent interconnect reliability analysis framework. It can evaluate the impact of the resistance and delay degradation of wires due to electromigration and TDDB on the system performance. Using such a tool, the designer can predict when reliability degradation mechanisms will start introducing timing violations, which will lead to system malfunction [21].

The limit of this approach is in the need for accurate models of failure modes, which are not available for all reliability issues. At system level, it is also theoretically possible to monitor reliability degradation on real ICs and counteract it by reducing the activity of that part of the circuit in which the degradation is occurring. This approach is possible if the degradation dynamic is slow, and is more independent of accurate models of failure modes. In this respect, the slow breakdown mode is a suitable degradation to be monitored at circuit level and counteracted by reducing the activity of the circuit which shows this type of degradation mode. Intrinsic reliability limits as initial material screening on low-κ and ultra low-κ. Accurate assessment of intrinsic reliability of low-κ materials allows filtering out all the weak candidates which will fail the extrinsic (the materials are integrated in the real wire architecture) reliability criteria anyway.

Obviously, the materials passing the intrinsic reliability tests will have to be screened for extrinsic reliability as well. In general, it is expected that one or more alternate interconnect approaches, such as package-intermediated interconnect, 3D IC, or optical, will begin to be used within the next five years. It appears that carbon nanotube approaches are even further into the future. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

INTERCONNECT PERFORMANCE

INTRODUCTION

The adequacy of near-term interconnect technology (copper wires and low-κ dielectrics) to continue meeting performance requirements for ICs of next technology generations varies with the intended function of the interconnect net and the technology used to fabricate Cu wires. As requirements are becoming more stringent, it is increasingly necessary that interconnect be considered as part of a system that includes the package and silicon chip to satisfy all technology needs for ICs.

The resistivity increase in narrow wires due to electron scattering [1] strongly impacts line resistance and leads to a progressive increase of wire aspect ratio to partially balance R increase, thus causing a slight increase in coupling capacitance between wires, which is the main component of total wire capacitance [2]. This problem is worsened by the current issues in low-κ materials introduction: a) the increase of κ during integration of porous dielectrics with respect to the pristine value, due to processing damages, further exacerbated by dimensional scaling (sidewall damage in Cu-low-κ

trenches) [3]; b) the contribution of integrated low-κ materials to the reduction of total wire capacitance is becoming less important due to the presence of other dielectric materials with higher κ in the wire architecture, such as adhesion layers, etch stop, or hard mask layers and dielectric barriers [4]. How these issues, especially the increase of κ during integration of porous dielectrics, will limit circuit performance depends on circuit architecture and interconnect network properties, making a strong collaboration between the design and technology worlds mandatory in order to face the performance challenges of future technology nodes.

SIGNAL PROPAGATION

The most critical phenomenon affecting high performance products is interconnect delay. Generally, wire performance is related to RC product or RC delay. Actually, the critical length of interconnects, below which delay is C dominated and above which delay depends on both R and C, is rapidly decreasing from one node to the other (from a few hundreds of micrometers in 2000 down to a few tens of micrometers in 2010) [5]. However, the interconnect length scaling in local and intermediate hierarchies has kept RC delay almost constant in past years. On the other hand, semi-global and global wires represent a real performance constraint, since their typical wirelength does not scale, worsening the RC increase issue [6]. In this case, it is necessary to insert repeating inverters in the wires to keep the RC delay within viable limits [7]. This approach requires additional chip area and increases power consumption.Crosstalk and noise associated with decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits [8]. These trends are a strong function of design strategy and should be considered in that context. Crosstalk also induces delay uncertainty, increasing the unpredictability of system performance.

POWER CONSUMPTION

Power dissipated in digital IC interconnects is dynamic and depends on the capacitance of the wires as $\sim \alpha.C_{int}.V^2$ f for a wire, where f is the frequency of the digital signal, α is the wire activity factor, V stands for voltage swing between the two digital levels, and C_{int} is total interconnect capacitance of a certain wire length [9]. Dynamic power is directly impacted by wiring capacitance and can be minimized most efficiently by reducing V. Interconnect power is strongly influenced by capacitive coupling in the most dense hierarchy levels, at local and intermediate levels, thus creating a highly sensitive issue for low power applications.

In addition to the problems with scaled wires for clock and signalling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to the decreasing supply voltage, V, causes an increased voltage drop between the power supply and the bias point for fixed length wires. This issue is made critical by the resistance increase due to conductive section reduction and Cu resistivity increase. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires.

SYSTEM-LEVEL PERFORMANCE

Evaluation of IC performance requires dedicated modeling and simulation tools, including accurate technology modeling and system level considerations. At the system level, critical paths dictate performance of an IC system. These paths have to be carefully simulated, taking into account the entire link made of transmitter circuit, interconnect and receiver, each element with its own electrical characteristics as input/output resistance and capacitance. Interconnect RC delay is not sufficient to evaluate performance of a critical path accurately, especially considering current return path and its impact on parasitic inductance [10]. High frequency behavior might also be considered if the signals propagating through the wires have stringent requirements in terms of high frequency contents and limited distortion.

Alternative solutions at system design level are based on modular architectures to reduce the need for fixed length lines. One recent approach in this direction is the dual- or multi-core architecture in state-of-the-art microprocessors. Parallel data processing in the multi-cores allows comparable or even higher processor performance at lower core frequencies and reduced power consumption as compared to a single core high performance processor. Multi-core strategy reduces the interconnect length, and consequently C_{int}, and frequency, due to the exploitation of parallelism of multiple cores in executing certain tasks, and supply voltage, V, since a lower operating frequency requires lower V, thus reducing dynamic power consumption. The development of multicore architectures underline the need for a new kind of interconnect with high bandwidth (i.e., low C) to support inter-core communication through a chip level network on chip. However, such significant modifications to circuit architecture have the disadvantage of needing new design tools and new software and are not generally applicable to all designs. Revolutionary solutions include different interconnect concepts such as optical interconnects.

EMERGING INTERCONNECT SOLUTIONS

OVERVIEW

During the first four decades of the semiconductor industry, system performance was limited almost exclusively by transistor delay and power. Dimensional scaling has decreased transistor delay and power by over three orders of magnitude while interconnect performance has generally been negatively impacted by dimensional scaling. Specifically, if one assumes a node charging RC delay with constant metal resistivity and dielectric constant, geometrical scaling for local interconnects (path lengths which decrease with the scaling parameter, "d"), has a constant delay while global interconnect delay (paths with constant length) increases with scaling as 1/d. The replacement of Al with Cu and SiO_2 with low-κ materials can in principle lead to a reduction in delay, but unfortunately the resistivity of metals in small dimensions increases much more rapidly due to sidewall and grain boundary scattering, which leads to an increase in RC delay even for local interconnects with aggressive material scaling.

While this situation had relatively little impact on system performance a decade or more ago, interconnect delay is now directly impacting system performance. In the older 1.0 μm Al/SiO_2 technology generation the transistor delay was 20 psec and the RC delay for a 1 mm line was 1.0 psec, while in a projected 35 nm Cu/low-κ technology generation the transistor delay will be 1.0 psec and the RC delay for a 1 mm line will be 250 psec [1]. In the past decade, the industry has actively reduced interconnect delay by breaking up long global lines into shorter interconnect segments using transistor-driven repeaters. The use of repeaters effectively decreases the interconnect line length so that the delay per segment is roughly equal for the transistor and interconnect components. This provides a global interconnect delay which is linear with line length, instead of quadratic, but also consumes more power and requires the use of many more transistors and vias. The optimal repeater insertion length for interconnects decreases by roughly a factor of two every five years.

Looking forward, the vision for both global and local interconnects poses many challenges with only a few potential solutions. For global interconnects, extreme parallelism has limitations for most applications. For local interconnects the sidewall and grain boundary scattering in narrow metal trenches rapidly increases the resistivity and delay. For global interconnects, the geometrical path length reduction solution is the most viable. Clearly the multi-core designs reduced the longest interconnect path lengths and helped mitigate the problem.

A similar geometrical solution gaining momentum is the 3D solution which decreases interconnect path lengths by vertically stacking many thinned strata atop each other. For n stacked layers, this approximately reduces the global interconnect path lengths by sqrt(n). Beyond 3D stacking, further interconnect-based design innovations look promising. A viable RC alternative for interconnect is optical interconnects, which will be discussed later in this section.

For local interconnects, the challenges are also very difficult. The integration of low-κ material will help both local and global interconnects. The rapid increase in resistivity in narrow trenches requires the consideration of new, one-dimensional conduction systems which do not suffer from either sidewall or grain boundary scattering. Ballistic transport in one dimensional systems, such as silicides, carbon nanotubes, nanowires, or graphene nanoribbons, offers potential solutions. While ballistic transport has many advantages in narrow dimensions, most of these options incur fundamental, quantized resistances associated with any conversions of transport media, such as from Cu or silicides to CNTs. In addition to the quantum resistance, the technological problem of utilizing an additional conduction medium with its interface, substrate and integration issues, pose substantial barriers to the implementation of ballistic transport media.

It is important to note that the research to find new transistors or switches to replace FETs may present an important opportunity to implement new ballistic transport media for local interconnect. For example if graphene-based switches are identified as promising replacements to CMOS transistors, then it would be logical to use graphene conductors as the local interconnects. These interconnect applications, referred to as native device interconnects, need to explore the combined switch and local interconnect properties of the new system. In other words, a great switch which cannot communicate effectively with its neighboring switches would not improve system performance. The section on Native Device Interconnects discusses this in more detail.

There are basically three different applications for emerging interconnects: Cu extensions, Cu replacements, and native device interconnects. Cu extensions continue to utilize Cu as the conduction medium, but they employ either dielectric, geometrical, or propagation innovations to improve interconnect performance. These options are both the most mature and technologically viable and have been discussed in earlier sections of the Interconnect chapter. The Cu replacement options are disruptive since they replace the copper communication medium with other less mature technologies, including carbon-based and optical options. The native device interconnect options are highly speculative, but the consideration of their properties is essential for driving the roadmap towards the correct solutions beyond the timeframe of the FET switch. Table INTC9 lists brief summaries of the principal advantages and concerns for fifteen different emerging interconnect options. These options are grouped into the applications described above.

Table INTC9 Advantages and Concerns for Cu Extensions, Replacements and Native Device Interconnects

Application	Option	Potential Advantages	Primary Concerns
Cu Extensions:	Airgaps	Lower latency and power, mature technology	Reliability, cost, integration issues
	3D	Form factor, heterogeneous integration, reduced power and latency	3D design tools and standards, reliability of TSVs, extreme thinning, high aspect ratio TSV, thermal heat extraction
	LC Transmission Lines	Mature technology, reduced power and latency for long lines	Limited bandwidth due to wide pitch
Cu Replacements:	Other metals (Ag, silicides, stacks)	Potential lower resistance in fine geometries	Grain boundary scattering, integration issues, reliability
	Nanowires	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density, substrate interactions
	Carbon Nanotubes	Ballistic conduction in narrow lines, electromigration resistance	Quantum contact resistance, controlled placement, low density, chirality control, substrate interactions
	Graphene Nanoribbons	Ballistic conduction in narrow films, planar growth, electromigration resistance	Quantum contact resistance, control of edges, deposition and stacking, substrate interactions
	Optical (interchip)	High bandwidth, low power and latency, noise immunity	Connection and alignment between die and package, optical /electrical conversions
	Optical (intrachip)	Latency and power reduction for long lines, high bandwidth with WDM	Benefits only for long lines, need compact components, integration issues, need WDM
	Wireless	Available with current technology, parallel transport medium, high fan out capability	Very limited bandwidth, intra-die communication difficult, large area and power overhead
	Superconductors	Zero resistance interconnect, high Q passives	Cryogenic cooling, frequency dependent resistance, defects, low critical current density, inductive noise and crosstalk
Native Device Interconnects:	Nanowires	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, substrate interactions, fan out/branching and placement control
	Carbon Nanotubes	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, fan out/branching and placement control
	Graphene Nanoribbons	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, deposition and patterning processes.
	Spin Conductors- Si(Mn), Ga(Mn)As	Long diffusion length for spin excitons	Low T requirements, low speed, surface magnetic interactions

CU EXTENSIONS

The emerging Cu extension options are already being employed to a limited extent in products. Three Cu extension options are highlighted below: air gaps, 3D, and LC transmission lines. Two of these options were already discussed in detail in the dielectric and 3D sections of this chapter and are relatively mature. These options are included in the emerging section to provide context for the other, much more speculative options. In the 2007 roadmap, the air gap and 3D options were only discussed in the emerging interconnect solutions section.

Air-gap technologies selectively generate regions in close proximity to Cu lines which are devoid of any solid dielectric. These regions of vacuum or "air gaps" with $\kappa = 1$ can be generated by sacrificial thermal decomposition of material, selective growth of material, controlled pinchoff during growth, or selective etching of material. All air-gap approaches aim to generate as large a volume fraction of vacuum as possible, without seriously impacting structural integrity or reliability. The difficulty of integrating extremely porous dielectric materials has increased the interest in developing air-gap technologies. Several air-gap process flows have been reported with effective dielectric constants in the range from 2.5 to 2.2 [2].

All 3D interconnect options vertically stack multiple, thinned silicon/interconnect strata to achieve advantages, including a smaller footprint, shorter interconnect path length, higher inter-die bandwidth, and heterogeneous integration of divergent process flows. 3D emerging interconnect options have impacts on both global and intermediate length interconnects. 3D impacts global interconnects with a relatively coarse pitch of TSVs in the range of > 20 μm and target mostly system level integration of divergent process flows with a reduced form factor. 3D targeted for intermediate interconnects push the limits of TSV density to achieve both the greatest inter-die bandwidth and the greatest reduction in interconnect path length. Global 3D options are actively being driven by memory and cell phone applications and are already in production. Intermediate 3D options still require substantial improvements in process technology before high volume manufacturing becomes a reality.

LC or LRC transmission lines have been in use since the inception of microwave technology over 50 years ago. The fundamental concept of LC transmission lines is very different from conventional RC interconnects. LC transmission lines serve basically as waveguides for the transmission of electromagnetic waves which propagate at the speed of light in the associated dielectric medium, i.e., v = 1/sqrt(LC). To achieve appreciable signal at the end of the transmission line, the dissipative loss on the lines needs to be kept to a minimum, necessitating the use of very wide pitch structures. RC interconnects by contrast are based on multiple reflections of a signal that eventually increases the charge and voltage at the end of a line governed by its RC time constant.

The practical implementation of LC lines requires both wide metal pitches, on the order of 5 to 10 μm, and thick, > 2 μm, dielectric isolation. In addition, these large lines need to be driven by very large (e.g., 64×) drivers to help match the characteristic impedance of the line and minimize the signal reflection at the near end. While these overheads are severe, the latency and power metrics are very impressive for long LC transmission lines. In particular, 1 cm LC lines were found to have both faster propagation and lower power than either optical or conventional Cu / low-κ lines of the same length [3]. A pitch of 5 to 10 μm makes the bandwidth and associated processing cost of such interconnect lines prohibitive for any high bandwidth application.

CU REPLACEMENTS

Since the bulk electrical resistivity of Cu is superior to all conventional metals (except Ag), a metal's suitability as a potential Cu replacement is determined primarily by the impact of finite size effects on its electrical transport properties. Alternative materials have been investigated that may possess superior electrical resistivity to Cu at wire-widths consistent with end-of-roadmap dimensions, although the bulk electrical properties of these materials are inferior to those of Cu. Also, novel quantum effects in ultra-thin film or nano-line geometries of metallic non-Cu multi-layers may provide improved performance compared to conventional Cu/barrier systems. Potential options are described below.

METAL SILICIDES

The bulk electrical resistivity of nickel monosilicide conductors (~ 10 μΩ-cm) has been shown by several researchers to be unaffected by lateral wire dimension for single-crystal nanowires (SCNWs) approaching 50 nm[4-6]. This is attributed to the small electron mean free path (~ 5 nm) in NiSi. The preservation of bulk resistivity in NiSi SCNWs with diameters as small as 15 nm has been reported by one group to date [6] and compares favorably to expectations for polycrystalline Cu at those dimensions. Intrinsic integratability with Si-based devices and the prevalence of NiSi contacts in current FEOL processing is likely to keep interest high. Other nickel silicide phases have also shown bulk-like electrical resistivity in sub-50 nm diameter SCNWs. $NiSi_2$ SCNWs with diameters as low as 40 nm [7] exhibited an effective resistivity of 30 μΩ-cm, in line with bulk $NiSi_2$ values. Likewise, Ni_2Si SCNWs with diameters as low as 34 nm have shown an effective resistivity of 21 μΩ-cm [8]. Ultra-thin annular coatings of ALD-based $NiSi_2$ (~ 10 nm) on Si nanowires also point to bulk-like resistivity (~ 35 μΩ-cm) [9]. By virtue of their single-crystalline nature, several of these NiSi nanowire stoichiometries have demonstrated maximum current densities nearing or exceeding 10^7-10^8 A/m^2. Although the stability of bulk-like electrical resistivity in nickel silicide nanowires has been confirmed by several groups, it is only the monosilicide phase in particular that is relevant as a Cu replacement for BEOL processing as it approaches the effective Cu line resistivity at the 11 nm node.

Important demonstrations of top-down nickel monosilicide nanoscale wire processing have also been reported recently and will continue to receive experimental attention. Ni silicidation of patterned Si has yielded effectively single-crystal NiSi wires with widths below 25 nm. Bulk-like resistivity (~ 15 μΩ-cm) for wires fabricated via this approach for wire widths > 50 nm has been reported [7] while NiSi wire widths ≤ 30 nm exhibited a resistivity ~ 23 μΩ-cm [10]. In contrast, virtually no change in the measured electrical resistivities of 19.5 μΩ-cm and 19.7 μΩ-cm for similarly fabricated NiSi nanowires with cross sections of 23 × 31 nm^2 and 455 nm × 27 nm, respectively, has been observed [11]. This and the previous work clearly document a relatively low dimension impact factor for NiSi although maintaining a resistivity at or less than 10 μΩ-cm in a fully processed NiSi interconnect structure has yet to be demonstrated.

SILVER

Dimensional effects can substantially increase Ag electrical resistivity in thin films and narrow wire geometries due to its large mean free path (~ 58 nm) as documented recently in the literature [12, 13, 14]. More recent work has confirmed this trend, documenting an average electrical resistivity for single crystal FCC Ag wires of 11.9 μΩ-cm for wires with average diameters of 40-50 nm [15]. Still, there are examples of nanoscale Ag wires which have exhibited attractive values of electrical resistivity. Sub 100 nm diameter single-crystal Ag nanowires exhibiting a resistivity ~ 2.6 μΩ-cm have been demonstrated [16]. Although a relatively large wire diameter, this low value of resistivity indicates a substantial sensitivity to processing and will motivate continued work in Ag nanolines.

METALLIC PHONON ENGINEERING

Electron-phonon scattering contributes substantially to electrical resistivity at room temperature and above [17, 18]. Although surface scattering is expected to dominate at sub-32 nm wire widths, reduction of electron-phonon scattering should be pursued. Metal quantum wells have been shown to reduce electron-phonon coupling in the proper geometry and material. Ultra-thin (3 nm) Ag films on vanadium substrates have exhibited a reduction in electro-phonon coupling by 38% over bulk Ag [19]. This is expected to translate roughly to a 30% reduction in phonon-induced electrical resistivity at room temperature withnominal impact on local density of states and surface scattering [20]. Similarly, 13 nm Ag films on a Cu (111) substrate exhibit a 42% reduction in electron-phonon coupling compared to the bulk [21] holding the same promise for reduction of electrical resistivity. Although imperfect metal-metal interfaces may mask resistivity benefits due to reduced electron-phonon coupling, such multilayer geometries bear continued research emphasis.

METALLIC GEOMETRIC RESONANCE

Quantum confinement effects are generally deleterious regarding electrical resistivity. Such effects typically enhance electron scattering (whether from surfaces or phonons) due to restriction in density of states or inter-sub-band scattering [20, 22]. These effects result from finite size restrictions on electron quantum-state wave vectors [23]. A distinct type of quantum confinement effect was predicted based on electron surface scattering [24-26]. One implication was the presence of geometric resonances for multilayer films in which a layer interface coincided with a node in the transverse wave function (or its derivative). Several resonances existed for individual layer thicknesses in the range of 1-3 nm, in line with current and future cladding technologies. The end effect is a predicted reduction in inter-sub-band scattering which could enable near-ballistic transport (neglecting phonon-induced scattering). The investigations of such effects will see expansion as more core-shell nanoline geometries are investigated in conventional metallics as an alternative to Cu and carbon-based interconnects.

CARBON NANOTUBES

Carbon nanotubes (CNT) have aroused major research interest in their applicability as very-large-scale integration (VLSI) interconnects for future generations of technology because of their desirable properties such as large electron mean free paths, mechanical strength, high thermal conductivity, and large current carrying capacity. CNTs can be either single-wall (SWCNT) or multi-wall (MWCNT). SWCNTs consist of only one graphene shell, and their diameter may vary from 0.4 nm to 4 nm with a typical diameter of 1.4 nm [27,28]. MWCNTs consist of several concentric graphene cylinders, whose outer diameters may vary from a few to 100 nm [28, 29]; the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite [28]. Graphene cylinders, SWCNTs or shells forming MWCNTs, can be either metallic or semiconducting, depending on their geometrical structure (chirality). However, large diameter semiconductor shells (D > 5 nm) have bandgaps comparable to, or smaller than, the thermal energy of electrons and act like conductors at room temperature [28-30].

ADVANTAGES OF CNTS

CNTs offer several advantages compared to Cu/low-κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms:

1. *Higher conductivity*— Due to their one-dimensional nature, the phase space for electron scattering in CNTs is limited, and electron mean free path is in the micron range for high quality nanotubes, in contrast to 40 nm in bulk copper [31]. The conductivity of densely-packed CNTs is higher than scaled Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 kΩ [28, 32].
2. *Resistance to Electromigration*— The strong sp2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs; 10^9 A/cm^2 in contrast to 10^6 A/cm^2 in Cu [33]. In practice, however, contacts may limit the maximum current density in CNT interconnects.
3. *Thermal conductivity*— The longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W/mK, as suggested by theoretical models [34] and extrapolations on measured data from porous bundles [35]. The thermal conduction in CNTs is highly anisotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction.

CNT Integration Options

CNTs can potentially replace Cu/low-κ interconnects at most levels of interconnect hierarchy [36] except in places where low-resistance short interconnects are needed e.g., power and ground wires in the first interconnect level. CNTs can be integrated for on-chip interconnect applications in the following forms:

1. *SWCNT-Bundles*—A bundle of densely packed SWCNTs with the same dimensions as Cu/low-κ interconnects with high-quality contacts with the electrodes would be an ideal candidate for replacing Cu/low-κ interconnects to lower the interconnect resistance and address the problem of size effects in copper wires. This integration option provides significant delay improvement for long interconnects where the RC delay is dominant [27, 36-38].
2. *Few-Layer SWCNT Interconnects*—A few-layer arrangement of SWCNTs can reduce the capacitance of the CNT-based interconnects by as much as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects where the delay is dominated by capacitive loading and not resistance [43].
3. *Large-Diameter MWCNTs*—It has been proven both theoretically and experimentally that all shells within MWCNTs can conduct if proper connections are made to all of them [29, 30, 39]. There are reports of very large mean free paths in high-quality MWCNTs [29, 40], and theoretical models suggest that long large-diameter MWCNTs can potentially outperform Cu and even SWCNTs if the level of disorder in these tubes can be kept as low as those in SWCNTs and all shells can be properly connected to metal contacts [41]. Such MWCNTs would be suitable for semi-global and global interconnects. Recently MWCNT interconnects operating at gigahertz frequency range have been demonstrated. Conductivity of MWCNTs in these experiments, however, has been considerably lower than the theoretical models, mainly because of large defect density and a small ratio of outer to inner diameters [42].

CNT Challenges

There are numerous technical challenges that remain to be addressed before CNTs can be utilized as interconnects. The important challenges facing CNT integration are the following:

1. *Achieving a high-density integration with CNTs*—CNT-bundles can outperform copper wires in terms of conductivity only if they are dense enough. While dispersed SWCNTs can form dense regular arrays with constant 0.34 nm inter-tube spacing [43], in-place grown CNTs reported to date have been quite sparse. *Table INTC10* gives the minimum densities of metallic SWCNTs required to outperform minimum-size copper wires in terms of conductivity. As technology advances and size effects become more severe for Cu wires, the required minimum density becomes smaller. The material and size of catalyst particles are the key parameters determining diameter and density of nanotubes.
   The diameter of SWCNTs is assumed to be 1 nm, at which the phonon-limited electron mean free path is 1 μm at room temperature [44-46]. Contact resistance is assumed to be less than 10% of the intrinsic resistance of SWCNTs, which means longer bundles can tolerate larger contact resistances. Ideal density for a densely-packed all-metallic bundle of SWCNTs with 1 nm diameter is 0.66 nm^{-2}.

2. *Selective growth of metallic SWCNTs*—SWCNT growth processes developed to date cannot control chirality. Statistically, only one third of SWCNTs with random chirality are metallic [28]. Improving the ratio of metallic to semiconductor tubes would proportionally increase the conductivity of SWCNT-bundles. Semiconductor SWCNTs are not fatal for interconnect applications, and in contrast to transistor applications of CNTs, perfect control of chirality is not necessary
3. *Directional growth in CNTs*—At this time, an especially challenging step is the controlled growth of horizontal CNTs. The placement of catalysts on a vertical surface makes horizontal growth much more challenging than vertical growth. However, some progress has been made in this regard [47].
4. *Achieving low-resistance contacts*—The metal electrode contact with CNTs may cause reflection effects and cause contact resistance. These reflections occur due to inefficient coupling of the electron wavefunction from the electrode into the CNT. A promising close-to-ideal contact has been realized experimentally [30, 48]but the large number of publications reporting large contact resistances indicates a technological challenge in making good contacts. Because of the weak inter-tube coupling between SWCNTs in a bundle [43] and also between shells inside MWCNTs [28, 39], direct connections between all graphene shells and metallic contacts are required. CMP for vertical CNT bundles may be the solution for this requirement [49, 50].
5. *Achieving defect-free CNTs*—CNTs are very sensitive to adsorbed molecules. It is found that adsorbed molecules on the surface of CNTs affect electrical resistance [40, 51] imposing additional technical challenges to producing CNTs with stable characteristics.
6. *BEOL compatible CNT growth*—Most high-quality CNTs reported in the literature are grown at temperatures above 600°C, which is not acceptable for the silicon technology. Promising progress is reported that involves the growth of CNTs at temperatures as low as 400°C [30]. However, defect density typically increases as growth temperature is lowered. Furthermore, CNT interconnects are unlikely to replace all copper interconnects. CNT interconnect fabrication technology, therefore, needs to be compatible with Cu/low-κ technology.

Although CNT interconnects have been separately shown to be promising, there have been few efforts to successfully combine them in realistic circuits. There are still several process and reliability related challenges that need to be addressed before CNT-based devices and interconnects can enter mainstream VLSI processing. This makes it an exciting and open field for research. Problems such as purification, separation of carbon nanotubes, control over nanotube length, chirality and desired alignment, high density growth, low thermal budget and high quality contacts are yet to be fully resolved.

Table INTC10 Minimum Density of Metallic SWCNTs Needed to Exceed Minimum Cu Wire Conductivity

GRAPHENE NANORIBBONS

Graphene, a monolayer of carbon atoms packed in a hexagonal lattice, is a strictly two-dimensional material [52]. Graphene research has advanced rapidly since its first isolation in 2004, thanks to the expertise previously developed by carbon nanotube researchers. Graphene nanoribbons (GNR) can be considered unrolled CNTs, to which their electronic properties are similar. GNRs can be metallic or semiconducting depending on their geometry [53-55]. High-quality graphene sheets may have mean free paths (MFPs) close to those in CNTs [56], and they can conduct large current densities on the order of magnitude reported for SWCNTs [57]. The major advantage of GNRs over CNTs is their more straightforward fabrication processes.

The electronic properties of GNRs are determined by their width and geometry [55]. Tight-binding approximations predict that GNRs whose edges have a zigzag pattern are metallic (zero bandgap) [55]. GNRs with an armchair pattern, on the other hand, are metallic if the number of carbon atoms across their width is $3p+2$ where p is an integer. Armchair GNRs with $3p$ and $3p+1$ carbon atoms across their width are semiconducting and their bandgaps are inversely proportional to their widths [55]. All of GNRs measured to date are semiconducting and the bandgap varies inversely proportional to the width [56, 58, 59]. The existence of a gap in the bandstructure of all measured GNRs has been mostly attributed to edge roughness [58, 59]. Also, first principle calculations indicate that the spacing of carbon atoms along the edges of armchair GNRs is 3.5% smaller than the spacing between carbon atoms in 2D graphene [60]. This change in lattice constant opens a small gap in the band structure of $3p+2$ GNRs [60]. Likewise, a gap appears in the band structure of zigzag GNRs, once the spin degree of freedom is considered in first-principles calculations [60].

The fact that metallic GNRs may be unobtainable does not rule out the potential of GNRs as interconnects [61]. The bandgap in semiconducting GNRs is smaller than 0.1eV, even for the 11 nm interconnect width projected for the end of the ITRS [61]. The Fermi energies in graphene layers are often higher than 0.1eV. When the Fermi energy is a few k_BT

larger than half bandgap, the first conduction band becomes adequately populated [61]. For such GNRs, there would be a negligible difference between the ideal conductances of metallic and semiconducting GNRs.

ADVANTAGES OF GNRS

GNRs offer several advantages compared to Cu/low-κ interconnects:

1. *Higher conductivity*—Like carbon nanotubes, the mean free path of electrons in pure high-quality graphene can be quite large. Mean free paths as large as a few hundred nanometers have been reported in graphene [56]. Substrate-induced disorders are believed to be the dominant source of electron scattering and high mobilities corresponding to mean free paths as large as a few micrometers have been reported in the case of suspended graphene [62]. Conductivity of stacks of non-interacting GNRs with smooth edges and Fermi energies above 0.2 eV has been predicted to outperform those of copper wires, especially at small cross-sectional dimensions and long lengths [61].
2. *Resistance to electromigration*—The strong sp2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for GNRs; 10^9 A/cm^2 in contrast to 10^6 A/cm^2 in Cu [36]. In practice, however, contacts may limit the maximum current density in GNR interconnects.
3. *Thermal conductivity*—The in-plane thermal conductivity of suspended single layer graphene sheets has been measured to be 5300 W/mK [63]. This value is comparable to the highest values reported for SWCNTs bundles [63].

GNR INTEGRATION OPTIONS

GNRs can potentially be integrated for on-chip interconnect applications in the following two forms:

1. *Many-layer GNR interconnects*—These can potentially be used to lower interconnect resistance, especially at small interconnect dimensions where size effects severely limit conductivity of Cu wires. In the case of Bernal stacking, graphene layers have an ABAB ordered arrangement [64]. In this case, the layers become electronically coupled and form graphite. Graphite lacks the appealing electronic properties of isolated graphene sheets. It is therefore critical to have electronically decoupled layers in multilayer GNRs. Stacking disorders have been reported for epitaxial graphene grown on C-faced 4H-SiC substrates [64] and CVD grown multi-layer graphene films [65].
   The shift in Fermi energy that naturally occurs because of the charge trapped at the graphene-substrate interface is limited to the few graphene layers at the bottom of GNR stacks due to the screening effect [66]. Methods such as edge functionalization [67] must hence be adopted to shift the Fermi energy of all layers in GNR stacks.
2. *Few-layer GNR interconnects*—A few-layer arrangement of GNRs can be used to reduce the capacitance of the CNT-based interconnects by as much as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This is similar to the few layer arrangement of SWCNTs. The reduction in capacitance helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects in which the delay is dominated by capacitive loading and not resistivity.

GNR CHALLENGES

There are numerous technical challenges that remain to be addressed before CNTs can be utilized as interconnects. The important challenges facing CNT integration are the following:

3. *Graphene synthesis*—Wafer-level synthesis of high-quality graphene sheets on arbitrary substrates remains a major challenge. While epitaxial graphene grown on SiC substrates has the potential for wafer-level growth, it will not be a suitable option for interconnect applications in which graphene ribbons on dielectric materials are needed. Recently, graphene films have been obtained by using bilayer catalyst films (Co and TiN) and CVD at temperatures around 510°C [68]. In this method, multilayer graphene is created on top of vertical multiwall carbon nanotubes. The graphene film obtained is extremely flat with a thickness determined by the thickness of the Co film [68]. Continuous films of graphene have also been grown by ambient pressure CVD on polycrystalline Ni [65]. After wet-etching the Ni film, the CVD-derived films have been successfully transferred to a diverse set of substrates [65]. A similar approach has been taken in [69] where CVD grown graphene films on Ni are transferred to Si substrates; films with sheet resistances as small as 280 Ω per square and mobilities as

high as 3,700 $cm^2V^{-1}S^{-1}$ have been obtained. Wafer-level methods for graphene preparation still lack the uniformity and grain size needed for large scale integration of graphene devices.

4. *Patterning GNRs with smooth edges*—Resistance of a narrow GNR is quite sensitive to edge quality because electrons interact with the edges frequently when the GNR width becomes comparable to the intrinsic mean free path of non-patterned 2D graphene. Since the intrinsic mean free path in graphene can be as large as several hundred nanometers, the effective mean free path is determined by edge scattering for most interconnect widths of interest. The mean free path associated with edge scattering depends on the edge quality (roughness), GNR width, and the ratio of transverse to longitudinal electron speed. Edge roughness determines the backscattering probability at the edges. In chemically obtained GNRs with relatively smooth edges, a backscattering probability of 0.2 has been reported [70] whereas the data from lithographically patterned GNRs indicate a backscattering probability of 1 [53]. The product of GNR width and the ratio of longitudinal to transverse velocity determines the average length electrons move before interacting with edges [53, 70, 71]. Sub-bands further from the Dirac point have smaller longitudinal to transverse velocity ratios and therefore have shorter mean free paths.
5. *Edge functionalization or doping*—The Fermi energy of graphene layers close to the substrate is shifted from the neutral point because of the charge accumulated at the grapheme/substrate interface. However, this effect diminishes exponentially for upper layers because of the screening effect [66]. To utilize all layers within a multilayer GNR, the Fermi energy of upper layers must be shifted either through edge functionalization or doping. Otherwise, the conductance of upper levels would become considerably smaller because of their bandgap. This conductance degradation is more severe for narrower GNRs whose bandgap is larger. Edge-functionalization or doping must be done such that the effective mean free path is not adversely affected.
6. *Achieving low-resistance contacts*—Similar to carbon nanotubes, creating reliable low-resistance contacts to GNRs is challenging. For multilayer GNRs, it is desired that the graphene layers be electronically decoupled to preserve the attractive graphene qualities. Therefore, at the contacts, direct electrical connections to all layers in multilayer GNRs are needed.

OPTICAL INTERCONNECTS

CMOS-compatible optical solutions have been proposed for on-die interconnects (signaling and clock distribution) and I/O. The drivers for on-chip optical interconnects are the utilization of the speed-of-light signal propagation and the large bandwidth of waveguides. For I/O applications, optical solutions focus on increasing the aggregate bandwidth and/or communication distance, while decreasing the power per bit by overcoming the limitations imposed by losses in present package interconnects (metal and dielectric), and by avoiding or minimizing the need for high power equalization and pre-emphasis. Since I/O, signaling and clock distribution require similar optical components, research and production costs are shared.

Because of pitch constraints, as well as delay and power considerations, optical interconnects are not expected to fully replace the lower metal-dielectric interconnect layers in microprocessors. Instead, the focus is on cost-efficient implementations which take advantage of the unique properties of optical architectures to increase overall system performance. For such optical solutions to be viable, the development of CMOS-compatible optical components is of paramount importance. Although significant progress has been made, this area is not yet sufficiently mature to define an intersectionwith the existing interconnect roadmap.

OPTICAL INTERCONNECTS ADVANTAGES

The basic advantages of optical interconnects are speed-of-light signal propagation and large bandwidth, as noted above. However, other potential advantages also exist. Among these are minimum crosstalk between signal transmission paths and multi-wavelength capability. The capability for a single optical path to accommodate multiple wavelengths increases the data-carrying capacity manifold, providing bandwidth densities not achievable by electrical means.

INTEGRATION OPTIONS

Although a large number of optical architectures have been proposed, most of them fall into one of the following two categories, as follows:

- *Integrated light source architectures*—In this case there are multiple on-die directly modulated light sources (e.g., VCSELS) and on-die detectors. The main disadvantage is the large on-die power consumption/heat dissipation of the sources, and the significant challenges with integrating fast efficient CMOS-compatible light sources.
- *External light source architectures*—These are implementations that utilize one or a few off-die light sources on the package or the board, and on-die modulators and detectors. The main advantage of this

family of architectures is that the laser power is off-die (i.e., does not have to be delivered through the die). The main disadvantage is the coupling losses to bring the light into the chip.

In both cases above, wavelength-specific filters/modulators can be used to implement multiplexing, which enables multiple independent signals transmitted in each channel.

ADVANTAGES

- *Delay*—For the case of on-die signaling, it is possible to define a critical length above which optical interconnects are faster than their metal-dielectric counterpart. The critical length, which depends on the quality of the optical components, has been assessed to be on the order of mm [72].
- *Signal integrity*—Optical interconnects have the potential for simplifying design and layout constraints arising from undesirable crosstalk in metal-dielectric interconnects.
- *Skew and Jitter*—It has been proposed that the low latency and the absence of crosstalk in optical interconnects can potentially result in low skew and jitter clock distribution. However, advanced clock distribution designs implemented in conventional metal-dielectric systems are expected to meet microprocessor needs.

DISADVANTAGES

- Power
- Cost
- Complexity.

POTENTIAL USAGE IN THE INTERCONNECT HIERARCHY

Most of the proposed implementations of optical I/O can be grouped into one of the following two architectures.

- *Integrated I/O*—In this case, optical components are integrated into the digital logic chip. Part or all of the communications between the chip and the external world are done through optical signals.
- *Discrete I/O die*—These architectures use an optical I/O chip that receives electrical signals from the digital logic chip and transforms them into optical signals. Equivalently, the optical I/O chip receives optical signals that are transformed into electrical signals that are then provided to the digital logic chip.

The main advantage of integrated I/O is that it can potentially save power with respect to discrete I/O. On the other hand, discrete architectures remove some of the design and integration constraints which would be otherwise imposed if optical components were integrated on the microprocessor die.

ADVANTAGES

- High aggregate bandwidth and low power per bit
- Potential for long-distance I/O
- Removal or minimization of pre-emphasis and equalization requirements

DISADVANTAGES

- Cost
- Complexity

CHALLENGES

The primary challenges for optical interconnects at the present time are producing cost effective, low power components that are compatible with CMOS fabrication. Some of these components, and the associated challenges, are contained in the listing below.

COMPONENTS

On-chip implementation of optical interconnects for signaling, clock distribution, and/or I/O require some or all of the following components:

- *Light sources*—From a modulation perspective, light sources can be *directly modulated* or *non-modulated*. In the first case, the light sources can be turned on/off with an electrical signal; in the latter case, the light source is used in conjunction with modulators that can be controlled with electrical signals. From a location perspective, lasers can be off-die (package or board) or on-die. Key parameters are output power, efficiency, cost, thermal stability, cooling, and speed for directly modulated sources. Examples of light sources include

VCSELS, quantum dot lasers, and edge emitting semiconductor diode lasers. The most widely used wavelengths are 850, 1310, and 1550 nm.

- *Photodetectors*—As in the case of lasers, photodetectors can be integrated either on-die or off-die. Metal-Semiconductor-Metal photodetectors have received significant attention since they have the potential for being CMOS compatible [73], and can be fabricated using Ge, Si, and SiGe [74, 75, 76, 77]. Key technical parameters include responsivity, operation voltage, input capacitance, ratio of photocurrent to dark current, ratio of photocurrent to input capacitance, light coupling efficiency, dimensions. A key design parameter is the coupling of light into the photodetector. Recently, detectors that take advantage of plasmons to enhance the coupling of light into the photodetector have been proposed [78].
- *Modulators/filters*—Modulators and filters are used in combination with a non-modulated light source, typically located off-die. The main purpose of a modulator is the control of the flow of light into a particular waveguide with a standard digital signal. A frequency-dependent filter can be used to introduce multiplexing, which enables the transmission of multiple signals in a single waveguide. A large variety of CMOS compatible modulators have been proposed in the literature, including resonators and Mach Zehnders. The key performance parameters include coupling efficiency, operation voltage, switching time, waveguide loss, overall power, modulation depth/extinction ratio, and area.
- *Waveguides*—Waveguides provide the means for light propagation on the chip with minimum loses. They also need to enable implementation of "bends" and "turns", as well as an efficient coupling of the light into the detectors. A large refractive index contrast between the waveguide and the surrounding materials enables tight turn radii and small pitches, but at the expense of lower speed, which decreases with the inverse of the effective refractive index. Reported on-die waveguides using materials already common in the industry include, for example, Si, Si_3N_4, or $Si_3O_xN_y$ cores on SiO_2 cladding [79]. Key technical parameters include loss per unit length, refractive index contrast and pitch.
- *Couplers/splitters*—Couplers are used to bring light from an external source into the package and die. The key merit metrics are coupling efficiency, cost and alignment requirements. Power losses in couplers can potentially dominate the optical budget in optical systems. Splitters are used to divide a light source (laser or single waveguide) into two or more waveguides. Power losses and size are the two most important quality metrics of splitters.

Significant progress has been made towards developing CMOS-compatible optical components, especially in the case of waveguides and detectors. However, additional progress is still necessary to further develop modulators, light sources and couplers to fully deliver the potential of optical interconnect.

SUPERCONDUCTORS

The concept of zero resistance obviously has immediate appeal in attempts to minimize RC delay of interconnect systems. This has attracted some attention to the potential application of superconductors for interconnect systems. Unfortunately, there are several inconvenient realities that make the applications of superconductors much less attractive as interconnects. First, the superconductors need to be cooled to approximately 77K to provide reasonable properties, and such cooling solutions are prohibitively expensive. Second, high temperature superconductors typically require high growth temperatures on epitaxial substrates which are not compatible with CMOS integration. Third, the typical critical current densities of high temperature superconductors are in the 1E5 A/cm^2 range [80], which is similar to operating current densities. Fourth, superconductors have an intrinsic frequency dependent conductivity. At 77K, Cu and YBCO have equivalent surface resistances at 150 GHz. At 10 GHz, YBCO has approximately a two order of magnitude lower surface resistance than Cu [81]. Finally, even if R were to go to zero, signal transmission would then be similar to LC transmission lines for which the signal propagation speed would be 1/sqrt (LC).

WIRELESS INTERCONNECT

Wireless interconnects in integrated circuits use the substrate or substrate in combination with a dielectric layer that can be placed below the substrate for signal propagation. This provides a parallel channel to conventional interconnect layers, but requires additional areas for circuits and antennas as well as accompanying power consumption. Thick Si substrates with typical doping levels generate high losses and associated signal attenuation. The silicon substrate can be thinned below 100 μm to reduce this attenuation. It is also possible to communicate from an off-chip antenna to on-chip antennas through the silicon substrate backside. The antenna size scales down linearly with the operating frequency which can be as high as 25-50% of the peak cut-off frequency, f_T for transistors. The extinction coefficient also decreases with the operating frequency in the limit when the operating frequency times the permittivity is much larger than the conductivity

of the substrate. For 20 Ohm-cm substrates, this transition frequency is around 10 GHz. Eventually the dopant related plasma effects increase the extinction coefficient.

The bandwidth of wireless interconnects is limited by the bandwidth of the circuits that can be realized in a given process technology. The bandwidth is 25–50 % of transistor f_T. With the present CMOS technology, it should be possible to support a data rate of 100–200 Gbps, which makes wireless interconnects better suited for signals with low to moderate bandwidths. The aggregate bandwidth can be increased by dividing space into cells like what is done for cellular phone communications at the cost of increased circuit area and power consumption. Frequency division multiple access and code division multiple access schemes are additional options to increase the number of I/O lines. However, the hardware and power consumption overheads are usually too high compared to using Cu wires for intra-chip applications. Wireless interconnects are better suited for global signals with fan_outs 10-100 such as global clock, reset, sleep and other moderate bandwidth signals requiring multiple long metal lines. The area for synchronization at given clock frequency and skew tolerance can be increased by radiating clocks through the back side of an integrated circuit from an off-chip antenna.

Inter-chip wireless data communication within a printed circuit board using the free space between a metal cover and a ground plane on a PC board is also possible. The loss of medium is smaller than that of transmission lines on a PC board. Furthermore, since wired interconnects also need a transmitter and receiver, the power consumption and area overhead for wireless interconnects are more tolerable.

NATIVE DEVICE INTERCONNECTS

A diverse set of emerging devices is being investigated to augment or replace Si CMOS switches. The range of options being explored varies from field-effect transistors made from novel materials such as Si nanowires, carbon nanotubes, and graphene nanoribbons, to more disruptive devices that are based on new computational state variables such as electron spin. As each of these new device concepts are evaluated in terms of their intrinsic properties, their interconnection aspects must be examined as well. Otherwise, the delay and energy overhead associated with interconnects may wash out the intrinsic advantages of these novel devices. This becomes especially important for some emerging devices in which the boundary between device and interconnect blurs when they made from the same materials (native device interconnects). Carbon nanotubes, graphene nanoribbons, and silicon nanowires are examples of such materials. Also, non-charge based devices should be able to communicate their state variable in a fast and low-energy fashion, at least locally. Otherwise, the circuit, delay and energy overhead needed for signal conversion will be prohibitive. In this section, the interconnect challenges and opportunities offered by native device interconnects are discussed.

NANOWIRES

Chemically driven nanowires made from semiconducting materials such as Si and Ge can be locally doped or metallicized to form metal-semiconductor heterostructures. Such structures are especially useful in crossbar architectures in which molecular devices (e.g., diodes) are formed at the intersection of two orthogonal sets of nanowires [82]. Lithographically patterned wires are then used to address individual nanowires that have unique active profiles. The major advantage of crossbar architectures is high packing density,however, they are typically slow. Doped semiconductor nanowires are quite resistive (around hundreds of kilo-Ohms per micron) and can be used only for short lengths. Metallic nanowires such as single crystal NiSi, instead, are considerably better conductors with resistivities around 9 μΩ-cm [83]. Metallic-semiconducting NiSi-Si heterostructures are created by selectively coating Si nanowires with Ni and annealing them at elevated temperatures (~550^{o}C). The remaining Ni is later etched away, and pure single-crystal NiSi nanowires are obtained. The effective mean free path in single-crystal NiSi nanowires is around 5 nm; because of this, size effects are expected to be modest even in diameters as small as 10 nm [83]. Also, due to their single-crystal nature, NiSi nanowires can conduct current densities as large as 3×10^{8} A/cm^{2}.

CARBON NANOTUBES

Single-wall carbon nanotubes are quasi 1D materials. At any point in which SWCNTs are interfaced by 3D metallic contacts, extra quantum and contact resistances are introduced. While contact resistance can potentially be lowered by better metal-nanotube interfaces, quantum resistance is a fundamental limit that is unavoidable (6.5 kΩ for metallic SWNTs). Implementing multiple switches on the same carbon nanotube is an attractive option as it eliminates the extra quantum and contact resistances. In theory, chirality or diameter of a single nanotube can change along its length to form metal-semiconductor junctions. However, it is quite unlikely that this can be done in a controllable fashion as little

progress has been made on chirality control. A more practical approach is chemically or electrostatically doping certain regions to form such junctions and connect multiple nanotube switches in a seamless fashion. Chemical doping can degrade the mean free path if the dopants change sp2 bonds to sp3;dopants that can keep the sp2 bonding can preserve the large mean free path.

CNT-CNT junctions tend to be highly resistive (many mega Ohms) because electrons have to tunnel between nanotubes. This makes it necessary to use metallic contacts any time a fan-out is needed. Native CNT interconnects are thus useful mainly within logic gates, especially for gates that need multiple switches in series. Examples are multiple-input NAND and NOR gates. Potential performance of such gates, considering possible misalignment of some tubes, is modeled in [84].

GRAPHENE NANORIBBONS

GNRs can be considered as unrolled CNTs and have many electronic properties in common with CNTs. The bandgap in a GNR is determined by its width and edge geometry, and can therefore be controlled through proper patterning. This, in principle, provides a big advantage for GNRs over CNTs whose chirality cannot be controlled. A series of semiconductor-metal GNRs can be patterned by varying width along a GNR to form a complex of logic gates with the use of only a few graphene to metal contacts. Wide regions along a GNR have smaller bandgaps that, with the proper choice of Fermi energy, can be made conductive. The choices of widths and lengths for each region should be made properly since the eigenstates in the wide regions can penetrate into the narrow regions and destroy the semiconducting property of the narrow regions. To obtain adequately large bandgaps in GNRs, sub 5 nm widths are needed. This makes patterning nanoribbons a major challenge. Like carbon nanotubes, local doping, both chemically and electrostatically, can be used to form series of semiconductor-metal junctions in GNRs.

Bends and turns can be implemented in GNR circuits. However, if the overall length is short and a GNR operates in the ballistic transport regime, sharp bends and any sudden change in the number of conduction channels along the length of the GNR can reflect electrons and introduce large resistances [85]. This is due to the fact that a ballistic GNR behaves like a waveguide for electron waves. In the diffusive regime, however, GNR behavior is similar to a conventional conductor.

Fan-out in a GNR circuit can be done without the need for metal to graphene contacts, which is another advantage over CNT circuits. This is especially true for the diffusive regime. In the ballistic regime, the wave properties of electrons need to be taken into account, and special layouts may be required to avoid large electron reflections. While GNRs offer more flexibility in terms of layout, there is little routability within a single graphene sheet and other interconnect levels are needed for making most logic gates. These interconnect levels can be metallic or carbon-based. However, metallic vias are needed to interconnect these levels.

It should be noted that field-effect graphene transistors are not the only device options being pursued. Novel properties of graphene offer opportunities for new device concepts. Examples are devices based on electron spin (spintronics), electron pseudo-spin (valleytronics), and electron wave interference. These new device concepts will offer their own interconnection challenges and opportunities.

SPIN-BASED INTERCONNECTS

All devices whose computational state variable is electric charge suffer from the limitations imposed by energy dissipation of charging and discharging capacitances associated with devices and interconnects [86]. Spin is one of the novel state variables being pursued to achieve ultra low-power circuits [87-89]. Spintronics refers to the control and manipulation of the spin degree of freedom of one or a group of electrons, or electron-hole pairs called excitons. Potential advantages of spintronics are non-volatility, increased data processing speed, decreased power consumption, and increased integration density [90]. These potential advantages can be materialized only if spin is used as both input and output for spin-based logic devices [88]. Otherwise, if spin is solely used to control electric current (spin transistor) it will face the same scaling limits as charged based devices [88]. Fast low-power spin-based interconnects are therefore key in developing spin-based circuits which may potentially outperform their conventional counterpart.

Spin signals can be communicated by physical displacement of electrons or excitons carrying the spin information or through spin waves. Carriers can be moved around using electric field (drift) or taking advantage of concentration gradients (diffusion). Excitons have zero net charges and can be moved around by an electric field only if electrons and holes are in separate layers (indirect excitons) e.g., in bi-layer graphene [91]. The use of electric field to move carriers comes with an energy penalty and may result in stand-by power dissipation. Diffusion, on the other hand, can be used for both charged and non-charged carriers. It is a passive phenomenon and can hence be favorable in terms of energy

dissipation. Diffusion, however, is a slow process and can limit the speed of diffusion-based interconnects. This low speed must be compensated by a large reduction in power dissipation. Spin relaxation is also an important parameter that limits the length of spin-based interconnects. Spin relaxation length varies in different materials and is typically below a micron. In graphene, spin relaxation lengths as large as 2 micrometers at room temperature have been reported [92], and progress in graphene synthesis is expected to offer higher spin relaxation lengths [92].

It has been demonstrated recently that spin waves can be used to transfer information in spin-based logic [93-94]. A spin wave is a collective oscillation of spins in an ordered spin lattice around the direction of magnetization. The strength of exchange interaction between neighboring spins in the magnetic material determines the upper bound of spin wave velocity in the ferromagnetic material. The spin wave velocity does not exceed 10^5 m/s in experimentally studied materials such as Fe and Co (with high Curie temperatures) [94]. For a spin-wave bus implemented with NiFe, the maximum group velocity of the magnetostatic wave propagation mode is 10^4 m/s in the GHz frequency range, and it continually decreases at higher frequencies [94]. Thus, spin waves are also slow compared to electrical interconnects.

CROSSCUT CHALLENGES

ESH

Through the middle of the next decade, leading-edge interconnect technology can be expected to generally follow that which has served the industry for the past ten years: copper-based metallization and low-k dielectrics, following dual damascene processing approaches. However, within that general evolution, there will be a number of chemical/material changes, as well as process modifications, whose ESH implications must be considered. For metallization, these may include new formulations for copper ECD (including extending copper plating bath life or recycling), changes in barrier and nucleation films (especially if the dominant PVD processes move towards CVD/ALD processes), and the emergence of new capping layers and processes. For the dielectrics, increasingly porous films can involve new precursors and so new process emissions, all of which must be evaluated for ESH concerns. Such dielectrics can also require pore sealing agents. Finally, the supporting technologies of planarization and surface treatment will evolve as any of the films in the interconnect stack change, and the same ESH considerations must apply there as well.

The increasing use of planarization presents particular issues both in consumables (e.g., slurries, pads, and brushes), as well as in major chemicals and water use. Therefore, efforts should be made to develop planarization processes that will reduce overall water consumption. Water recycling and reclamation for planarization and post-planarization cleans is a potential solution for water use reduction.

High GWP (global warming potential) PFCs (perfluorocompounds) are used extensively in interconnect dry etch and chamber cleaning applications. For chamber cleaning, processes that do not use PFCs have been evaluated; note, however, that the residues of carbon-containing low-k films which are processed in such chambers can produce PFC emissions (e.g., CF_4) in any case. At present, dry etch processes for low-k dielectrics are all based on fluorocarbon compounds (whether or not they fall into the high GWP PFC family), and so PFC emissions as either byproducts or unreacted starting compounds must be managed. The semiconductor industry's near-term goal is to reduce absolute PFC emissions 10% from the 1995 baseline by 2010. To achieve this aggressive goal, and to ensure that these chemicals remain available for industry use, the industry must strive to reduce PFC emissions by process optimization, alternative chemistries, and/or abatement. Fluorinated heat transfer fluids also have high global warming potential, and these materials' emissions must be minimized. Another high GWP process chemical to be addressed is N_2O (used in oxynitride deposition processes).

With the emergence and expected rapid growth of chip-to-chip interconnects (commonly referred to as 3D technology), a new source of substantial PFC use has appeared, with processes based on PFCs such as sulfur hexafluoride, in development for TSV etch. This new application will place even greater demands on maintaining the PFC reduction goals versus the 1995 baseline.

To meet expected energy conservation goals, equipment (PECVD, dry etch, and CMP) power requirements must be minimized. These goals should include reducing support equipment energy consumption. Plasma processes are both energy-intensive and inefficient in the way they use input chemistries (e.g., often achieving only 10–30% dissociation, by design, in etch processes). Future generation tools will require R&D in low energy-consuming plasma systems. Etchers and CVD tools use point-of-use (POU) chillers and heat exchangers to maintain wafer and chamber temperatures in a vacuum. More efficient heating and cooling control systems (including eliminating simultaneous heating and cooling for temperature control devices) could help decrease energy use and improve control. Greater use of cooling water to remove heat from equipment, rather than dissipating heat into the cleanroom, results in fab energy savings.

By the middle of the next decade, an entirely new interconnect materials set may begin to emerge, including non-metallic conductors (likely based on carbon nanomaterials technology) and air-gap dielectrics. Thus, a new family of chemicals, materials and process emissions will need to be examined for ESH concerns – especially given the incomplete current definition of the ESH properties of nanomaterials. Finally, with such a dramatic shift in interconnect films, there is potential for additive processing. This is a radical shift from decades of lithography-based subtractive processing, but the ESH benefits which would be obtained, along with the process simplification advantages, should be substantial.

Potential solutions for interconnect include additive processing, low ESH impact CMP processes (e.g., slurry recycle or slurry-less CMP), non-PFC emitting TSV etch, low cost/high efficiency plasma etch emissions abatement, low temperature wafer cleaning, reduced volume process chambers for CVD and ALD, improved ALD process throughput (to reduce resource requirements), vacuum pumping with process-tool-demand-based speed control, reduced dependencies on high temperatures (both internal and external to the processes), and implementation of variable modulation for heating and cooling devices.

METROLOGY

INTERCONNECT METROLOGY

New processes and structures continue to drive metrology research and development. Porous low κ is moving into manufacturing, and 3DIC is being used in a great variety of implementations. Copper contact structures have been announced at key technical symposia. All areas of metrology, including materials characterization, in-line measurements, and advanced equipment and process control, are used for interconnect research, development, and manufacturing. Reliability of new processes such as copper contacts is largely unknown. As in the past, reliability testing is a critical part of evaluating new processes.

Interconnects, including all of the IC structures necessary to connect from silicon to the boards and boxes of the outside world, have become a potential performance roadblock for the continuation of the semiconductor industry on the Moore's Law curve. This roadblock has components in both technology and cost. It has technology components spanning the necessary transition from aluminum/SiO_2 to Cu/low κ, as well as in transitions to more radical approaches to interconnects beyond the metal/dielectric system. It has cost components in the anticipated high cost of fabrication of alternatives to the incumbent metal dielectric interconnect system for global interconnects using current technology. Among the potential roadblocks and cost issues inherent in the switch from aluminum/SiO_2 to Cu-low κ are the significant challenges for new metrology for process development, manufacturing validation, and process control. For example, in Cu-low κ it is desirable to produce minimal thickness barriers between Cu and dielectrics. This has resulted in a need for metrology for detailed characterization of extremely thin layers and "zero thickness" interfaces, without the undesirable effects occurring during destructive sample preparation. *One of the most challenging issues facing interconnect metrology is the lack of measurement capability for sidewalls of trenches and vias.* The anticipation of moves to radical interconnect options, such as optical interconnects, has led to new metrology issues such as the need to profile optical properties of very narrow waveguides, and to be able to identify extremely small optical defects in such waveguide materials. Some of the needed metrology problems have been solved with creative applications and advances of existing techniques, and new techniques have been developed. However, some problems have been identified as particularly difficult, and possibly not having solutions within the confines of currently envisioned metrology techniques.

Interconnect needs for metrology, as noted above, include continuing evolutionary advances in existing metrology techniques, as well as the increasing need for novel metrology approaches for more radical interconnect structures. The following sections will first describe some of the needs and status of existing metrology techniques for current interconnects, and will then address some of the needed advances for future directions in interconnects. In addition to the on-chip interconnect, a new approach to chip-to-chip interconnect known as 3DIC has emerged. This section will also discuss metrology for 3DICs.

3D INTERCONNECT ISSUES AND METROLOGY

TSVs provide a means of connecting die directly without using wires. TSV structures have high aspect ratios making them difficult to etch and fill despite their relatively large size. The first metrology challenge starts when the wafers are bonded. The alignment must be checked through the wafer, and the bonding integrity determined. Infrared microscopy is capable of measuring overlay target structures through the silicon since silicon is transparent in the IR. Scanning acoustic microscopy (SAM) is also capable of measuring subsurface features. SAM has been successfully applied to observation of voids and defects between bonded wafers. X-ray microscopy is another method capable of "seeing" through silicon

structures. All these methods require advances in spatial resolution especially as TSV diameter shrinks. A number of other measurement needs are receiving considerable attention including stress and adhesion (delamination) measurements. A list of TSV measurement needs includes:

- TSV Depth and Profile through multiple layers
- Alignment of chips for stacking – wafer level integration
- Bond strength
- Defects in bonding
- Damage to metal layers
- Defects in vias between wafers
- TSV aspect ratio CD
- Wafer thickness after thinning
- Defects after thinning including wafer edge

CU-LOW κ METALLIZATION ISSUES AND METROLOGY NEEDS

CU METALLIZATION ISSUES

Copper metallization has been used for several generations. The latest advance in copper metallization is the use of copper contacts to the transistor, replacing tungsten. With each shrink, the challenges of filling trenches and vias must be faced again. Among the most important of these is the need for precise control of ECD baths, and identification of very low-level impurities that may cause resistivity increases in electrochemically deposited copper. We now know that the reliability of copper metal interconnects is degraded by the effects of electro- and stress migration, and that the primary degradation modes are associated with surface diffusion of Cu along the interfaces between the Cu and dielectrics and barriers. Voids in metal lines and vias that occur during processing have also been identified as significant yield loss initiators. Voiding problems can show up after deposition/CMP/anneal, or from agglomeration of micro-voids due to electro- or stress migration. Another significant problem relating to voids is the need to be able to identify relatively small, isolated voids in large fields of patterned Cu conductors. These isolated voids often do not show up as yield loss, but can be an incipient cause of later reliability failures. These voids may be on the surface of the conductors, but are often buried within the conductor pattern or in vias. Additional issues with Cu metallization arise from the use of thin barriers to isolate the Cu from underlying dielectrics. These thin barriers raise significant needs for measurement capabilities of ultra-thin layers, interface properties, and defects and materials structure on sidewalls in very narrow channels.

The problems noted above have all been found to be important for Cu metallization at 90 nm and above. As the industry moves below 90 nm, it is expected that these issues will remain, but that additional issues will arise. While we do not know all of the new issues that will arise, several problems associated with our inability to extrapolate current techniques to the very small geometries, or increasing importance of currently acceptable limitations of metrology for future technology generations, are already clear. Among these future needs for Cu metallization metrology is the increasing importance of metrology for ultra thin layers—especially barriers on sidewalls. This necessitates not only the ability to establish the physical properties and structure of these layers with thicknesses < 2 nm, but also to identify and characterize defects in the films. An additional problem area, that is currently not extensively studied but that is expected to become increasingly important at smaller conductor geometries, is the interface between the Cu and the adjacent barrier or dielectric. As the Cu conductors become smaller, it is expected that interface scattering will cause significant increases in resistivity of very narrow lines.

CU METALLIZATION METROLOGY

Copper electroplating systems require quantitative determination of bath additives, byproducts, and inorganic components in order to maintain the desired properties in the electroplated film and *in situ* process monitoring to track bath aging. A mass spectrometry-based method of real-time sampling of bath contents provides a new potential solution. Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid chromatography can be used to quantitatively measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for monitoring inorganic contaminants.

Barrier layer metrology needs include measurement of thickness, spatial uniformity, defects, and adhesion. In-line measurement for 3D structures continues to be a major gap. Measurement of sidewall materials on low κ trenches is made

even more difficult by sidewall roughness. There is some concern about the application of statistical process control to very thin barrier layers. Interconnect technical requirements indicate that barrier layers for future technology will be < 5 nm thick. The 2001 ITRS specified a process window of 20% total thickness variation. The measurement precision (6σ) for a 6 nm film must be ≤ 0.12 nm, which is beyond current capabilities. It may be possible to use existing metrology capability to determine the presence or absence of these very thin films without using traditional SPC. Presently, a number of measurement methods are capable of measuring a barrier layer under seed copper when the films are horizontal. These include acoustic methods, X-ray reflectivity, and X-ray fluorescence. Some of these can be used on patterned wafers. In-line determination of the crystallographic texture (grain orientation) has been demonstrated using grazing X-ray diffraction. Detection of voids in copper lines is most useful after the CMP and anneal processes. A metric for copper void content has been proposed in the Interconnect Roadmap and in-line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Many of the methods are based on detection of changes in the total volume of the copper lines. The typical across-chip variation in the thickness of copper lines will mask the amount of voiding that these methods can observe. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, spatially resolved (for product wafers) multi-layer thickness measurements.

In-line measurement of crystallographic phase and crystallographic texture (grain orientation) of copper/barrier films is now possible using X-ray diffraction-based methods. This technology is under evaluation for process monitoring, and the connection to electrical properties and process yield is being investigated.

Post CMP processes for interconnect structures require measurement of dishing and erosion in the copper lines. Current optical and acoustic techniques have been explored, but need to address the statistical sampling requirements for the accurate detection of dishing and erosion in a manufacturing environment.

Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.

Advances in measurement technology have enabled *in situ* control of CMP and determination of the thickness of buried barrier films on horizontal surfaces. The pore size distribution of porous low κ can be measured using small angle X-ray scattering or ellipsometric porosimetry. Although voids can be detected in fields of copper lines, most methods determine a change in the volume of copper lines. Thus, process induced changes such as those that occur across the wafer from CMP can mask the presence of voids. Metrology for in-line control of bath chemistry is being implemented.

Some measurements remain elusive. For example, measurement of barrier and seed copper film thickness on sidewalls is not yet possible. Recently crystallographic texture measurements on sidewalls have been reported. Adhesion strength measurements are still destructive. End point etch detection must be developed for new porous low κ etch stop materials . Detection of killer pores and voids is not yet possible.

The accelerated reduction in feature size makes development of metrology for high aspect ratio features a greater challenge for on-chip interconnect development and manufacture. Critical dimension measurements are also a key enabler for development of interconnect processes. CD metrology must be extended to very high aspect ratio structures made from porous dielectric materials and requires 3D information for trench and via/contact sidewalls. These measurements will be further complicated by the underlying multi-film complexity.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the in-line measurements for interconnect structures are made on simplified structures or monitor wafers and are frequently destructive. Small feature sizes, including ultra-thin barrier layers, will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate with electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Metrology requirements and potential solutions for Interconnect are shown in *Table MET6*. The new measurement requirements for void detection in copper lines and killer pores in low κ appear to be difficult or impossible to meet. The need is to have a rapid, in-line observation of a very small number of voids/larger pores. The main challenge is the requirement that the information be a statistically significant determination at the percentage specified in *Table MET6*.

LOW κ DIELECTRIC ISSUES AND METROLOGY NEEDS

LOW κ DIELECTRIC ISSUES

The move from SiO_2 to other dielectrics to provide lower dielectric constants in interconnect structures is proving as much, if not more, of a challenge to the semiconductor industry than the move from Al metallization to Cu. This stems from the fact that the low κ materials thus far available have significantly different physical and mechanical properties than SiO_2. The primary differences are significantly different mechanical properties, and the presence of pores. The lower mechanical strength has resulted in back end manufacturing issues showing up as problems at assembly and packaging. Unfortunately, there are no convenient metrology tools or methodology to qualify materials at the back end process stage for assembly and packaging viability. A major issue with characterization of porous materials is the lack of atechnique to identify anomalously large or significantly connected pores (so called "killer pores") in otherwise smaller-pored materials. Metrology techniques for characterization of physical properties, chemical structure, and electrical performance of sidewall materials on low κ patterns are also lacking. Identification and quantification of thin sidewall layers is necessary and should be correlated with damage due to processes such as pore sealing and plasma etch. It is important to develop techniques for making measurements on sidewall surfaces, as well as into pores. The two issues noted above, along with the standard measurements associated with dielectrics, need to be addressed not only for today's dielectrics, but for those that will be used in the few nanometer generations of the not too distant future.

LOW-K METROLOGY

In-line metrology for non-porous low-κ processes is accomplished using measurements of film thickness and post CMP flatness. *In situ* sensors are widely used to control CMP. Metrology continues to be a critical part of research and development of porous low-κ materials. The need to transition some of the measurements used during process development into volume manufacturing is a topic of debate. One example is pore size distribution, which has been characterized off-line by small angle neutron scattering, positron annihilation, a combination of gas absorption and ellipsometry (ellipsometric porosimetry), and small angle X-ray scattering (SAXS). In a manufacturing line, SAXS and ellipsometric porosimetry can be either stand-alone or in-line. The need for moving these methods into the fab is under evaluation. Detection of large, "killer," pores in patterned low κ has been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap.

High-frequency measurement of low-κ materials and test structures has been developed up to 40 GHz. This needs to be extended to ~100 GHz because 20 GHz clocks have rising and falling edges much above 40 GHz. As a result of extensive evaluation, the interconnect community no longer considers this measurement a critical need in the near term. Low-κ materials seem to have constant dielectric functions over the frequency range of interest (from 1 GHz to 10 GHz).

Thinning of porous low κ during CMP must be controlled, and available flatness metrology further developed for patterned porous low-κ wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations have developed (and continue to develop) flatness tests that provide the information required for statistical process control that is useful for lithographic processing.

Interconnect specific CD measurement procedures must be further developed for control of etch processes. Key gaps include the ability to validate post etch clean effectiveness, sidewall damage layers and properties. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capability of current inline CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels. Furthermore, scatterometry must be extended to contact and via structures. Electrical test structures continue to be an important means of evaluating the RC properties of patterned low-κ films.

Measurement of low-κ mechanical properties helps to reduce the number of new candidate materials. Finally development of stress measurements in closely spaced trenches is needed.

CROSS-CUT BETWEEN INTERCONNECT AND DESIGN AND MODELING AND SIMULATION

The interconnect performance of future technology generations can no longer be provided by material and technology improvements alone. Therefore the interaction between material science, wafer technology, design, modeling, and simulation is becoming increasingly important in supporting continued interconnect scaling. Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Furthermore, the models are

largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and choose the correct interconnect routing, (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to utilize both the near-term and the far-term proposed interconnect systems effectively. Upcoming new interconnect challenges are outlined below.

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1cm). This capability will also be needed for systems using RF or terahertz wave interconnections.
2. The impact of the Cu resistivity increase on delay time must be considered in realistic models. These models need to take into account linewidth, line aspect ratio, sidewall roughness, metal grain size, and the coefficients for grain boundary-, surface- and impurity-scattering.
3. Signal delay uncertainties because of crosstalk effects between neighboring interconnects and the impact of dummy metal features need to be considered in appropriate models. Because of increasing line aspect ratios these effects may become major issues.
4. Process variations (e.g., CD tolerances, line height variations, sidewall roughness, etc.) will become increasingly important with further shrinking of interconnect line and via sizes. Therefore, variation tolerant designs and variation sensitive models and simulations are needed to support upcoming technology generations.
5. A means to optimally place function blocks will be needed for 3DICs, not only on an individual die but also now on a stack of die.
6. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
7. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurrences of reliability critical 'hot spots' within the die. Predictive thermal models, that can accommodate thermal impacts of low-κ dielectrics with reduced heat conductivity, RF standing waves, the multiple heat generating layers embedded in the 3D IC stack, and heat generated by, as well as thermal performance of, optical devices and quantum well devices will be needed

Modeling and Simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to prediction of the resistivity increases of further shrinking copper interconnects (due to grain structures, Cu/barrier interfaces and impurities) and the physical structure and properties of new low-κ dielectrics and other more exotic interconnect materials.

In all of these cases, Modeling and Simulation should provide predictions accurate enough to reduce as much as possible the need for and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for Modeling and Simulation is ever increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical, and electrical modeling.

Specific interconnect needs for modeling and simulation include: performance prediction (including high frequency effects and reliability) for complex (e.g., 3D) structures fabricated with real non-idealized processes (including etching, PVD, CMP), with the ability to choose the appropriate tradeoff between speed and accuracy for the application in question; tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; tools to calculate the degradation of electrical circuit performance due to resistivity increases over time of interconnect wires and vias, and materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier and dielectric). Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, and copper thinning and dishing in CMP. The treatment of the variability associated with LER, trench depth and profile, via shape, etch bias, and thinning due to cleaning is a key challenge to interconnects and their simulation.

APPENDICES

PASSIVE DEVICES

An important challenge for current and future interconnect architectures is the inclusion of precision on-chip passive elements, such as high quality capacitors, inductors, resistors and other components, into the metallization scheme. This demand is mainly driven by advanced mixed-signal, RF and SOC applications and is addressed in the standard CMOS platform and foundry technology offerings [1-10]. The traditional means of realizing passive circuit elements (e.g., capacitors, resistors) on ICs was integration during front-end processing. In this case, doped monocrystalline Si substrate, polycrystalline Si and the respective Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during front-end processing suffer increased performance degradation, especially when used at high RF frequencies. Therefore, there is an increasing demand for low loss, low parasitics but high quality passive devices in the interconnect levels. For interconnect integration the key challenge is to achieve this goal in a modular and cost effective way, without sacrificing overall interconnect performance or reliability.

Basically there are two approaches for passive integration. The first is the introduction of optional interconnect levels and new materials to accomplish the necessary functions with the highest performance, the highest quality factors (Q) and the lowest chip area consumption. The second is to realize the passive devices simply by design measures and by using the native properties of existing interconnect levels and materials. This second approach typically has significant cost advantages in the wafer manufacturing process, because additional process steps are unnecessary, but suffers in many cases from reduced performance and Q-factors and from increased chip area consumption.

In any case, excellent matching properties and the reduction and control of substrate coupling noise and other parasitics are the most important tasks for mixed-signal and RF CMOS applications. For the most widely used passive devices, (capacitors, resistors and inductors), the expected future requirements at the different technology nodes for analog, mixed-signal and RF products can be found in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter.

In the following, typical applications, requirements and integration challenges of capacitors (MIM and native), inductors and resistors are discussed. Published examples of new and innovative approaches for passive devices in interconnects will be highlighted as well.

CAPACITORS

APPLICATIONS IN CMOS, BICMOS AND BIPOLAR CHIPS

- Decoupling capacitors for MPUs used to reduce the transient currents across the on-chip voltage/ground-interconnects and the chip-to-package interconnects during the switching cycles of the CMOS circuits
- RF coupling and RF bypass capacitors, in high frequency oscillator and resonator circuits and in matching networks
- Filter and analog capacitors in high performance mixed-signal products, e.g., A/D or D/A converters
- Storage capacitors in DRAM and embedded DRAM / logic devices

TYPICAL CAPACITOR REQUIREMENTS

- Small feature size and high charge storage density
- Low leakage currents and dielectric loss
- High dielectric breakdown voltage and TDDB reliability
- High precision of absolute and/or relative capacitance between neighboring capacitors on the same chip
- High linearity over broad voltage range (low voltage coefficients)
- Small temperature dependence (small temperature coefficients)
- Low parasitic capacitance
- Low resistivity of electrodes and wiring to allow high switching speeds with high Q values, but without excessive heating

PROCESS INTEGRATION CHALLENGES

MIM CAPACITORS

- Very thin high quality dielectric films with excellent thickness uniformity and control

- Preferably high κ dielectric films in order to reduce capacitor size. Compare to the Dielectric Potential Solutions Figure, INTC7, for suitable materials
- Low defect densities for dielectric and metal films (low surface roughness)
- Low deposition temperatures (< 450°C) for compatibility with overall metallization requirements, especially when low-κ intermetal dielectrics are utilized
- Smart modular integration schemes making optimal use of existing metal levels in order to reduce overall costs, i.e., the number of additional process steps and optional lithography levels
- Realization of MIM capacitors in the upper metal levels to reduce parasitic substrate coupling and to maintain high Q values. The use of low-κ intermetal dielectrics should also be beneficial, but may introduce other integration challenges.

NATIVE CAPACITORS (MOM, VPP, VNCAP)

- Aggressive interconnect design rules (narrow lines and spaces, small via height)
- Tight alignment/overlay tolerance between the metal and via levels of the capacitor stack
- Tight thickness and CD control with minimal LER on metal lines
- Low defect densities for intermetal dielectrics (e.g., porous low-κ) and metal films
- Low etch and CMP damage in dielectric films, especially for porous low-κ films

Realizations of MIM capacitors is reported in the literature for both Al- based and Cu- based metallization schemes [1-4, 11, 12-14, 15, 16]. Today most MIM capacitors in manufacturing usesilicon oxide, silicon oxynitride or silicon nitride as MIM dielectrics with adequate material properties, reasonably good RF performance and easy integration into Al- or Cu-based interconnect technologies [17]. Different MIM capacitor architectures, single and stacked approaches, were realized and characterized in a 130 nm multi-level Cu interconnect technology [18]. A large area on-chip MIM decoupling capacitor (> 250 nF) with a triple dielectric stack of $HfO_2/Ta_2O_5/HfO_2$ with TaN electrodes (~ 8 fF/μm2) has been demonstrated for a 90 nm SOI microprocessor technology [19, 20]. On-chip MIM power-ground plane capacitor structures with high κ dielectrics are expected to significantly improve scaling problems for global interconnects such as IR drop, di/dt noise, and clock wire latency, as well as signal delay and energy per bit for global signal wires [21].

Several published papers showpromising data on the integration of interconnect compatible high κ MIM dielectrics (e.g., Al_2O_3, Ta_2O_5, HfO_2, Nb_2O_5, TiTaO, $TiSiO_4$, TaZrO, BST, STO, TiLaO, TiO_2, $Bi_5Nb_3O_{15}$) [3, 22-38]. The high κ MIM dielectrics are deposited either by PVD followed by an appropriate anneal or by CVD and especially ALD processes, keeping the overall temperature budget typically below 400-450°C. However, not all approaches with record breaking capacitance densities may be useful from a leakage current, voltage- & temperature-linearity or dielectric TDDB reliability point of view. Recently, laminated (multi-layered) films of different high κ MIM dielectrics were proposed in order to overcome these problems [27, 29, 39-41]. By proper work-function tuning of the electrode material (i.e., replacing TaN by Ni) a significant reduction in leakage current was observed for a MIM capacitor with STO high κ dielectric [33].

An innovative 3D damascene MIM capacitor architecture with 17 $fF/\mu m^2$ capacitance density was demonstrated by using a PEALD $TiN/Ta_2O_5/TiN$ electrode/dielectric/electrode stack embedded in a multilevel Cu metallization with only one added mask compared to the standard process flow [42-44]. In an extended study of this 3D MIM concept which combined the Ta_2O_5 dielectric with other PEALD high κ dielectric materials such as ZrO_2, HfO_2, and Al_2O_3, even higher capacitance densities up to 30 $fF/\mu m^2$ were achieved [44].

In a totally different approach, an ultra-thin MIM capacitor stack made use of the underlying Cu interconnect as the bottom electrode (approx. 100 nm total thickness, 10 nm SiN dielectric, 6.3 $fF/\mu m^2$) and fitting between two scaled down Cu interconnect layers was demonstrated with promising voltage and temperature linearity and > 10 years of TDDB reliability [45].

The manufacturing of MIM capacitors with high capacitance density, high quality Q, good reliability and low additional cost is a real challenge. Therefore, in many applications simply the parasitic or native capacitance of horizontal or vertical parallel plates or comb and finger like structures in different metal levels are used to realize an integrated capacitor with somewhat reduced area capacitance density [46, 47, 48]. In this approach, chip area is traded for a reduction in process complexity and manufacturing cost. The biggest benefit of native capacitors is that they can be realized and optimized by design and layout measures only, without any modification to the wafer manufacturing process. The continued scaling of the on-chip interconnects and the increasing number of interconnect layers in current and future CMOS technology nodes makes the native or natural capacitors more and more competitive, even from a capacitance density per chip area

perspective. For the 65 nm and 45 nm technology nodes, native capacitors with good linearity, TDDB robustness and capacitance densities > 2 fF/μm2 and Q-factors > 20 at 1 GHz are reported [49-51], while for the 32 nm node, capacitance densities even above 4 fF/μm2 are predicted [8]. Based on these promising results of today, native capacitors will be part of the standard offerings in CMOS platform and foundry technologies for the 65 nm node and beyond.

INDUCTORS

APPLICATIONS OF ON-CHIP INDUCTORS, ESPECIALLY IN RF CIRCUITS

- Impedance matching between different building blocks in today's microwave RF circuits. With increasing frequencies the on-chip inductors will gain even more in importance in the future [52-54]
- RF transceivers
- Filters
- Voltage controlled oscillators (VCO)
- Power amplifiers and low noise amplifiers (LNA)

TYPICAL INDUCTOR REQUIREMENTS

- High Q- factors at high inductance. Increasing inductance typically results in reduced Q- factors
- High self-resonant frequency
- Low Ohmic losses in the inductor coil (dominant at lower frequencies)
- Low capacitive substrate losses (dominant at high frequencies)
- Low eddy currents generated by inductor-substrate interactions, resulting in an increasing effective resistance at higher frequencies

PROCESS INTEGRATION CHALLENGES

- Making use of thick metal lines to achieve lower coil resistances. Cu metallization is beneficial as compared to traditional Al-interconnects. For spiral inductors built with Cu-damascene techniques, an improvement of Q by a factor of 2 has been reported as compared to similar Al-coils [55]. However, shunted Al-coils realized in different metal levels may also be feasible.
- Sufficient spatial separation of inductors and substrate, e.g., by putting the coils in the top metal levels or even above the passivation into the polyimide [56-59], helps to reduce capacitive and inductive parasitics and improves the Q-value. Again, low-κ materials help to reduce the capacitive parasitics and the substrate noise.
- Making use of higher resistive Si-substrates is also improving parasitic substrate losses, however this approach may not be feasible in every case [53].
- The introduction of metallic shielding (metal ground planes) in the lowest metal level underneath the inductors can reduce the eddy current losses in the substrate [52-54].

Currently, spiral coils realized in single Al- or Cu- metal levels are the most common type of on-chip inductors. However, shunted multilevel spirals and solenoidal types of inductor designs, which are supposed to have lower substrate losses, may be used in the future [55].

The influence of thick metal layers (5 μm – 22.5 μm) and innermost turn diameters on Q-factors of spiral inductors [60], as well as the questionable effect of an additional Al-layer on top of a Cu-based inductor stack [61], is reported.

A significant improvement in the quality factor was achieved by reducing the substrate coupling in making use of air gaps in suspended Al-spiral inductors [62] and Al-solenoidal inductors [63]. Using surface-micromachining, suspended spiral inductors of 1.38 nH (@ 1GHz) were demonstrated with a quality factor of 70 at a frequency of 6 GHz [64]. However, the thermal isolation of suspended inductors may result in significant self-heating effects which can shift Q and the operation point in RF circuits [65]. Another method for Q-value improvement (30%-70%) is the formation of localized semi-insulating Si-substrate areas under the inductor coils by proton bombardment after device fabrication, i.e., before interconnect, [66] or even after interconnect fabrication [67]. Porous silicon substrates were also reported to improve Q-values and resonant frequencies [68]. Areas with low-κ dielectrics partially embedded in the Si-substrate under spiral inductors showed suppressed parasitic capacitances and improved Q-factors [69]. In using SOI substrates excellent inductor Q-values ~ 20 were demonstrated without extra mask and processing steps [48]. Extremely high Q-values (~ 40)

were reported for above passivation (above IC) inductors using 5 µm Cu lines in BCB dielectric (k ~ 2.7) on top of a multi-layer Cu/oxide interconnect manufactured in a 90 nm RF-CMOS platform technology [70].

The successful integration of micro-inductors using magnetic materials was reported also. The introduction of a magnetic ground plane of CoZrTa increased the inductance of a square spiral inductor by 36 ~ 50 % [71]. A spiral inductor sandwiched between two layers of ferromagnetic CoNbZr was demonstrated to improve the inductance by 19 % and the quality factor by 23 % at 2 GHz [72]. Further improvements in inductance and Q was achieved by connecting the two magnetic layers with magnetic vias and a proper inductor layout making use of the uniaxial magnetic anisotropy of a CoZrTa alloy [73]. Another example is the integration of a ferromagnetic core ($Cr/Fe_{10}Co_{90}/Cr$) into a solenoidal inductor [74]. At lower frequencies (< 0.2 GHz) enhancements in inductance of up to eight-fold and improvements in quality factor of up to seven-fold have been achieved by using ferromagnetic cores. At higher frequencies however, those improvements are significantly degraded by ferromagnetic resonance losses in the ferromagnetic core and by eddy currents.

Crosstalk between adjacent 3-D solenoid on-chip inductors built in 4-layer interconnect stacks was found to be dominated by magnetic coupling and substrate noise and was reduced by arranging a guard ring between the inductor and the Si substrate [75].

Significant reduction in substrate noise is reported for an inductor on an ultra-thin (1.7 µm) Si-substrate top-chip with a Fe/Ni-permalloy film providing magnetic screening between the top and bottom chip in a 3DIC system in package approach [76]. Prefabricated RF inductors were transferred from a Si-substrate wafer to a flexible plastic packaging substrate (FR-4) by a wafer-transfer technology and showed significantly improved performance in Q and resonant frequency [77]. A variable on-chip inductor embedded in a wafer-level chip-scale package is proposed by making use of a movable metal plate over a spiral inductor [78]. A basic feasibility study of the variable inductor has been performed. However, the successful implementation of a MEMS actuator for moving the metal plate into the wafer-level package has still to be demonstrated.

RESISTORS

APPLICATIONS OF ON-CHIP THIN FILM RESISTORS, ESPECIALLY IN ANALOG AND MIXED-SIGNAL CIRCUITS

- Clock and bus terminators
- Precision resistor arrays and networks
- Voltage dividers

TYPICAL RESISTOR REQUIREMENTS

- Excellent matching properties
- Precision resistance control
- High voltage linearity (low voltage coefficients)
- Low temperature coefficients (TCR)
- Low 1/f current noise
- High Q values (low parasitics)

PROCESS INTEGRATION CHALLENGES

- Moderate and tunable sheet resistance
- Excellent thickness control (deposition uniformity)
- Modular integration scheme
- Good etch selectivity to dielectrics
- Using standard interconnect materials

Relatively little literature has been published on the integration of interconnect based thin film resistors. One interesting approach was the multi-functional use of a PVD TaN-based MIM capacitor base plate as a precision TaN thin film resistor with varying resistivity, based on different film stoichiometries. Low voltage linearity and temperature coefficients and excellent matching properties were reported for the TaN film [14]. Another approach using PVD WSi_x as a metallization based resistor with reasonably good TCR values was also reported [79]. A Ti/Ni(80%)Cr(20%) thin-film resistor with nearly zero TCR for integration into a standard CMOS process was reported [80].

DIELECTRIC APPENDIX

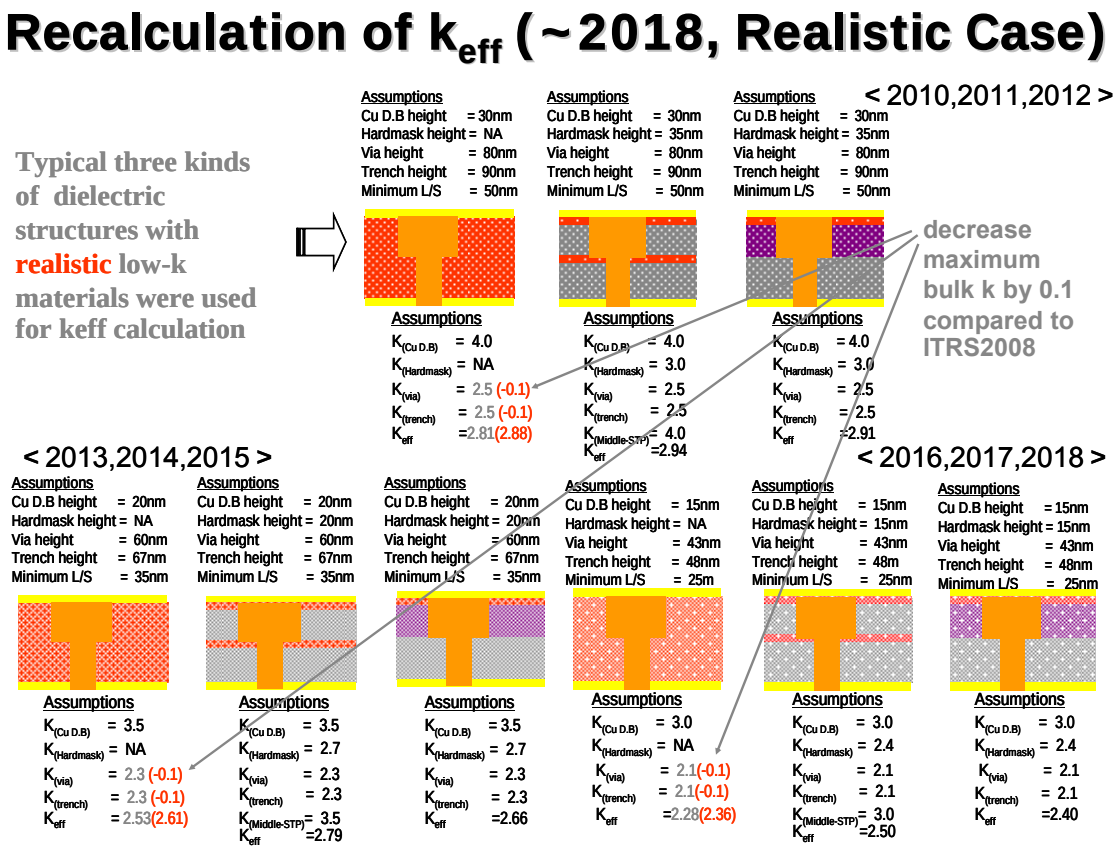


Figure A1 Dielectric Potential Solutions (2010~2018) Realistic Case

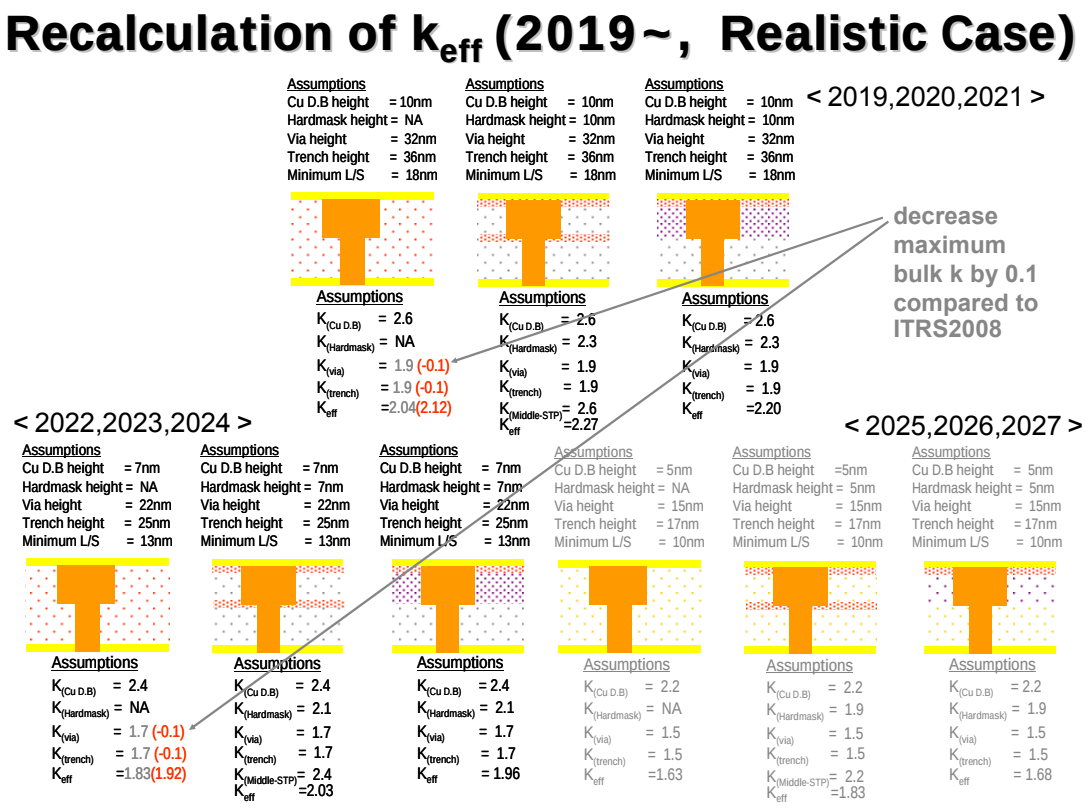


Figure A2 Dielectric Potential Solutions (2019~2027) Realistic Case

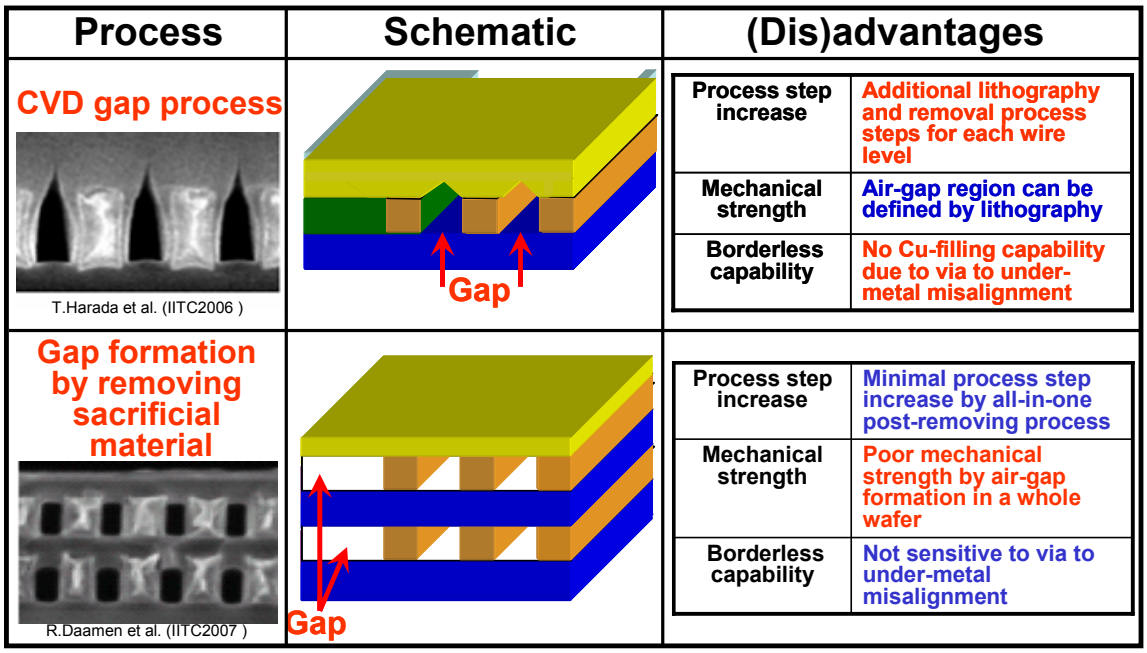


Figure A3 Two Kinds of Typical Air-gap Integration Schemes

INTERCONNECT MODEL ADOPTED FOR RC DELAY EVALUATION APPENDIX

- The model for RC calculation is based on a 2D cross-section of a central wire, surrounded by 2 conductive planes on top and bottom, and by 2 wires on the sides having the same dimensions as the center wire, as reported in the figure. The 2 planes represent the metal layers above and below the layer of the central conductor. All the surrounding conductors are considered grounded for the capacitance calculation. The extension of the planes over the 2 lateral conductors results in limited influence on the capacitance of the central conductor. No Miller effect is considered here.
- The dimensions w, s, h, h_v, AR and the material parameters K_{eff} and ρ_{eff} are taken from the ITRS Roadmap for each technology node.
- R per unit length is simply calculated as $\frac{R}{l} = \frac{\rho_{eff}}{h \cdot w}$.
- C per unit length is extracted from the 2D model by a static solver simulation as $\frac{C}{l} = \frac{2C_l + 2C_p + C_{fringe}}{l}$; inputs for the simulation are dimensions and K_{eff}.
- t =w*A/R (Cu); h_1 =w*A/R (Via); h_1 =h_2
- For M1 interconnect h_1 = t and Keff=4.2 in h_1 thickness.
- In presence of a range of values in the Roadmap for K_{eff}, the value used for the simulation is the average between min and max: K_{eff} = ($K_{eff\ max}$ - $K_{eff\ min}$)/2
- The wire width is considered as half pitch: w = s = p/2.

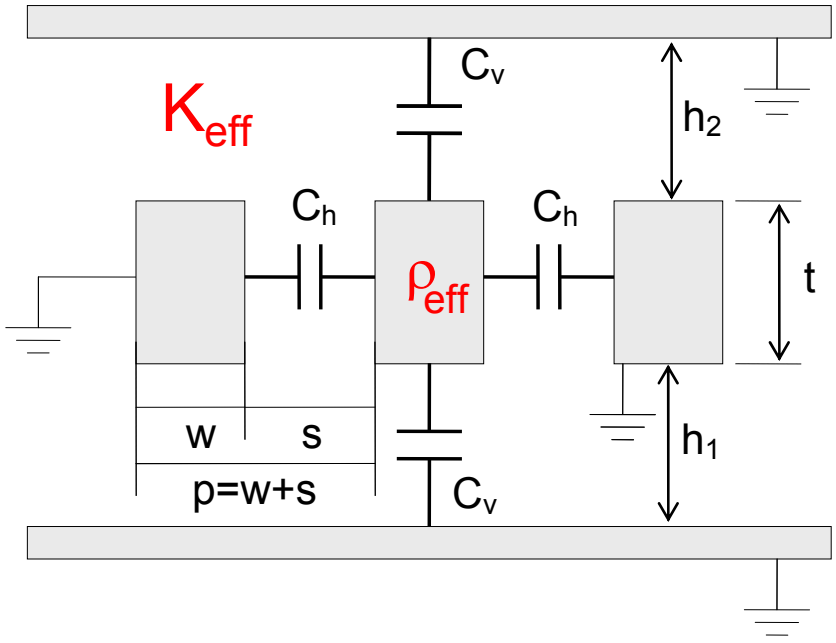


Figure A4 Interconnect Model

GLOSSARY OF 3D AND TSV DEFINITIONS

3D interconnect technology—Technology which allows for the vertical stacking of layers of basic electronic components that are connected using a layer 2D-interconnect fabric.

3D Bonding—An operation that joins two or more die or wafer surfaces together.

3D Stacking—3D bonding operation that also realizes electrical interconnects between the device levels.

3D-System-In-Package (3D-SIP)—3D integration using "traditional" packaging technologies, such as wire bonding, Package-on-package stacking or embedding in printed circuit boards.

3D-Wafer-Level-Packaging (3D-WLP)—3D integration using wafer level packaging technologies, performed after wafer fabrication, such as flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging and fan-out reconstructed wafer chip-scale packaging.

3D-System-on-chip (3D-SOC)—Circuit designed as a system-on-chip, SOC, but realized using multiple stacked die. 3D-interconnects directly connect circuit tiles in different die levels. These interconnects are at the level of global on-chip interconnects. Allows for extensive use/reuse of IP-blocks.

3D-Stacked-Integrated-Circuit (3D-SIC)—3D approach using direct interconnects between circuit blocks in different layers of the 3D die stack. Interconnects are on the global or intermediate on-chip interconnect levels. The 3D stack is characterized by a sequence of alternating front-end (devices) and back-end (interconnect) layers.

3D-Integrated-Circuit (3D-IC)—3D approach using direct stacking of active devices. The 3D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack

Through-Si-Via connection (TSV)—A galvanic connection between both sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections.

TSV liner—The isolation layer surrounding the TSV conductor

TSV barrier layer—Barrier layer in TSV in order to avoid diffusion of metal from the TSV into the Si-substrate.

"Via-first" TSV process—Fabrication of TSVs before the Si front-end (FEOL, Front-End-Of-Line) device fabrication processing

"Via-middle" TSV process—Fabrication of TSVs after the Si front-end (FEOL) device fabrication processing but before the back-end (BEOL, Back-End-Of-Line) interconnect process

"Via-last" TSV process—Fabrication of TSVs after (or in the middle of) the Si back-end (BEOL) interconnect process.

Wafer-to-Wafer (W2W, WtW) bonding—3D-stacking strategy that uses a wafer on wafer alignment and bonding strategy. Stacked die must be equal in size and wafer stepping pattern.

Die-to-Wafer (D2W, DtW) bonding—3D-stacking strategy that uses a die on wafer alignment and bonding strategy. Stacked die can have different sizes and partial population of a wafer is possible.

Die-to-Die (D2D, DtD) bonding—3D-stacking strategy that uses a die on die alignment and bonding strategy. Stacked die can have different sizes.

Face-to-Face (F2F, FtF) bonding—3D-stacking strategy where the sides of the die or wafers with active devices (="Face"-side) face each other after bonding.

"Frontside" TSVs—TSVs realized starting from the top surface of the wafer 5device and interconnect side of the wafer) .

"Backside" TSVs—TSVs starting from the thinned wafer backside.

Back-to-Face (B2F, BtF) bonding—3D-stacking strategy where the backsides of the die or wafers face each other after bonding.

Outer TSV-Aspect ratio—Ratio depth of the TSV to the maximum diameter of etch hole in the Si substrate.

Inner TSV-Aspect ratio—Ratio depth of the TSV to the maximum diameter of conductive layer of the TSV. (Aspect ratio, excluding the liner thickness)

REFERENCES

INTERCONNECT ARCHITECTURES

[1] E.Beyne, IEEE ISSCC, 15-19 February 2004, San Francisco, pp.138-145 (2004).

DIELECTRIC POTENTIAL SOLUTIONS REFERENCES

[1] J. Jang, et al., Proc. of Symp. VLSI Tech., pp.192-193 (2009).
[2] T. Yaegashi et al., Proc. of Symp. VLSI Tech., pp.190-191 (2009).
[3] K. Yoneda, et al., Proc. of 2006 IITC, pp.184-186 (2006).
[4] T.Usui et al., Proc. of.IRPS 2004, pp.246-250 (2004).
[5] T.Usami et al., Proc.of 2006IITC, pp.125-127(2006).
[6] C.S.Liu et al., Proc. of 2008IITC, pp.199-201(2008).
[7] Y.Hayashi et al., Proc. of 2009IITC, pp.252-254(2009).
[8] J. Noguchi, et al., Proc. of 2004IITC, p.81-83.
[9] S.Nitta et al., Adv.Metal.Conf.,2007, pp.329-336.
[10] L.G.Gosset et al., Proc.of 2007IITC, pp.58-60.
[11] R. Daamen et al., Proc.of 2007IITC, pp.61-63.
[12] N.Nakamura et al., Proc. of 2008IITC, pp.193-195.

ETCH / STRIP / CLEAN REFERENCES

[1] ITRS Road Map 2007 Edition Interconnect chapter.
[2] R. Kinder and M. Kushner, J. Appl Phys **90**, 3699 (2001)
[3] Y. Yand, M. Wang, N. Yu, Babaeva and M. J. Kushner PESM 2009
[4] Yang Yang et al. Iowa State University Proc. of IITC 2008 p. 90
[5] O. Joubert et al., Proc. MAM 2009
[6] A. Yamaguchi et al. Proc. of IITC 2009 p. 225.
[7] Zs. Tökei et al. Proc. of IITC 2009 p. 228.
[8] Th. Chevolleau et al. Proc. PESM 2007,
[9] N. Possémé et al. Proc. of IITC 2009 p. 240.
[10] L. Broussous et al.Proc. of IITC 2008, p. 87.
[11] H. Kudo et al. Proc. of IITC 2008, p. 93.
[12] D.Tee et al. Solid State Phenomena Vols 143 – 146 (2009) p. 335.

BARRIER POTENTIAL SOLUTIONS REFERENCES

[1] Choe, H.S., et al., "MOCVD TiN Diffusion Barriers for Copper Interconnects," IITC, 1999, p. 62
[2] Ashtiani, K., et al., "Pulsed Nucleation Layer of Tungsten Nitride Barrier Film and its Application to DRAM and Logic Manufacturing," Semi Tech. Symposium, Semicon Korea 2006.
[3] Chen, Y.C., et al., "Optimizing ALD WN Process for 65 nm Node CMOS Contact Application," IITC, 2007, p. 105
[4] Edelstein, D., et al., "A High Performance Liner for Copper Damascene Interconnects," IITC, 2001, p. 9
[5] Sakata, A., et al., "Reliability Improvement by Adopting Ti-barrier Metal for Porous Low-κ ILD Structure," IITC 2006, p. 101
[6] Sakai, H., et al., "Novel PVD process of barrier metal for Cu interconnects extendable to 45 nm node and beyond," Proceedings of AMC, 2006, p. 185
[7] Haukka, S., et al., "Deposition of Cu Barrier and Seed Layers with Atomic Layer Control," IITC, 2002, p. 279
[8] Mori, K., et al., "A New Barrier Metal Structure with ALD-TaN for Highly Reliable Cu Dual Damascene Interconnects," Proceedings of AMC, 2004, p. 693
[9] Rossnagel, S.M., et al., "From PVD to CVD to ALD for Interconnects and Related Applications," IITC, 2001, p. 3
[10] van der Straten, O., et al., "Thermal and Electrical Barrier Performance Testing of Ultrathin Atomic Layer Deposition Tantalum-Based Materials for Nanoscale Copper Metallization," IITC, 2002, p. 188
[11] Watanabe, T., et al "Self-Formed Barrier Technology using CuMn Alloy Seed for Cu Dual-Damascene Interconnect with Porous-SiOC/ Porous-Par Hybrid Dielectric," IITC, 2007, p. 7
[12] Saito, T., et al., "A Reliability Study of Barrier-Metal-Clad Copper Interconnects With Self-Aligned Metallic Caps," IEEE Trans. Electron Devices, 48, p. 1340

[13] Hu, C.K., et al., "A Study of Electromigration Lifetime for Cu Interconnects Coated with CoWP, Ta/TaN, or SiCxNyHz," Proceedings of AMC, 2003, p. 253
[14] Petrov, N., et al., "Material Properties and Thermal Stability of Electroless Co Alloys for Copper Interconnects," AMC 2004, p. 853
[15] Gosset, L., et al., "Self Aligned Barrier Approach: Overview on Process, Module Integration and Interconnect Performance Improvement Challenges," IITC, 2006, p. 84

NUCLEATION POTENTIAL SOLUTIONS REFERENCES

[1] Ashtiani, K., et al., "Pulsed Nucleation Layer of Tungsten Nitride Barrier Film and its Application to DRAM and Logic Manufacturing," Semi Tech. Symposium, Semicon Korea 2006.
[2] Chen, Y.C., et al., "Optimizing ALD WN Process for 65 nm Node CMOS Contact Application," IITC, 2007, p. 105
[3] Nakamura, N., et al., "Design Impact Study of Wiring Size and Barrier Metal on Device Performance toward 22 nm-node featuring EUV Lithography," IITC, 2009, p. 14.
[4] Kumar, N., et al., "Advanced Metallization Needs Integrate Copper into Memory," Semiconductor International, Vol. 31(5), 2008, p. 26.
[5] Ho, P., et al., "Extending PVD Copper Barrier Process Beyond 65 nm Technology," AMC, 2005, p. 421.
[6] Gandikota, S., et al., "Characterization of Electroless Copper as a Seed Layer for sub 0.1 μm Interconnects," IITC, 2001, p. 30
[7] Haumesser, P.H., et al., "Electro-grafting: A New Approach for Cu Seeding or Direct Plating," Proceedings of AMC, 2003, p. 575
[8] Malhotra, S.G., et al., "Integration of Direct Plating of Cu onto a CVD Ru Liner," Proceedings of AMC, 2004, p. 525.
[9] Roule, A., et al., "Seed Layer Enhancement by Electrochemical Deposition: The Copper Seed Solution for beyond 45 nm," Microelectronics Eng., Vol. 84, 2007, p. 2610.

CONDUCTOR POTENTIAL SOLUTIONS REFERENCES

[1] Shao, I. et al., "An Alternative Low Resistance MOL Technology with Electroplated Rhodium as Contact Plugs for 32 nm CMOS and Beyond," IITC, 2007, p. 102
[2] Demuynck, S., et al., "Impact of Cu Contacts on Front End Performance: A Projection Towards 22 nm Node," IITC, 2006, p. 178
[3] Edelstein, D., et al., "Full Copper Wiring in a Sub-0.25 μm CMOS ULSI Technology," Tech. Digest IEEE IEDM Meeting, 1997, p .773
[4] Heidenreich, J., et al., "Copper Dual Damascene Wiring for Sub-0.25 μm CMOS Technology," IITC, 1998, p. 151
[5] Reid, J., et al., "Optimization of Damascene Feature Fill for Copper Electroplating Process," IITC, 1999, p. 284
[6] Norman, J., et al., "New Precursor for CVD Copper Metallization," Microelectronic. Eng., Vol. 85, 2008, p. 2159.
[7] Tada, M. et al., "A Metallurgical Prescription for Electromigration (EM) Reliability Improvement in Scaled-down, Cu Dual Damascene Interconnects," IITC, 2006, p. 89
[8] Tonegawa, T., et al., "Suppression of Bimodal Stress-Induced Voiding using High-diffusive Dopant from Cu-alloy Seed Layer," IITC, 2003. p. 216.
[9] Kuan, T.S., et al., "Fabrication and Performance Limits of Sub-0.1 Micrometer Cu Interconnects," Mat. Res. Soc. Symp. Proc., 2000, Vol. 612, D7.1.1
[10] Jiang, O-T., et al., "Line Width Dependency of Copper Resistivity," IITC, 2001, p. 227
[11] Schindler, G., et al., "Assessment of Future Nanoscale Interconnects: Resistivity of Copper and Aluminum Lines," Proceedings of AMC, 2004, p. 305
[12] Clevenger, L., et al., "A Novel Low Temperature CVD/PVD Al Filling Process for Producing Highly Reliable 0.175 μm Wiring/0.35 μm Pitch Dual Damascene Interconnections in Gigabit Scale DRAMS," IITC, 1998, p. 137

PLANARIZATION REFERENCES

[1] G.C.Smith et al.: J.Electrochem.Soc.32,11,Nov., (1985), p.2721
[2] H.Kotani et al.: Tech.Dia.IEDM,(1989), p.669
[3] D.S.Balance et al.: Extg.Abst.VMIC Conf.,(1992),p180
[4] S.suguro et al.: Extended Abstracts of SSDM, Makuhari, (1993),pp.171-173
[5] C.W.Kaanta et al.: VLSI Multeilevel Interconnection Conf., IEEE, (1991), p144
[6] P. Feeney et al. : The Increasing Needs and New Solutions in CMP, ICPT 2009 Conf

[7] M. Tsujimura, Wet Process Revolution, pp.132-139
[8] US6,153,043, Elimination of photo-induced electrochemical dissolution in chemical mechanical polishing
[9] M. Tsujimura et al. "General Principle of Planarization Governing CMP, ECP, ECMP & CE", Proceedings 2004 IMIC-030/00/0267, pp. 267-274

THROUGH-SI-VIA (TSV), 3D STACKING TECHNOLOGY

[1] W.H. Teh, R. Caramto, S. Arkalgud, T. Saito, K. Maruyama, and K. Maekawa, Proc. IITC, pp. 53-55 (2009)
[2] D. Sabuncuoglu Tezcan et al., Proc. 57th IEEE ECTC, 29 May - 1 June 2007, Reno, NV, USA (2007).
[3] J. Van Olmen et al., IEEE IEDM, 15-17 December 2008, San Francisco, CA, USA, pp. 603-606 (2006).
[4] A. Klumpp, R. Wieland, R. Ecke, and S.E. Schulz in "Handbook of 3D Integration", edited by P. Garrou, C. Bower and P. Ramm, Wiley-VCH, ISBN: 978-3-527-32034-9 (2008) 157-173
[5] P. Ramm, D. Bonfert, R. Ecke, F. Iberl, A. Klumpp, S. Riedel, S. E. Schulz, R. Wieland, M. Zacher and T. Gessner, Proc. Advanced Metallization Conf. AMC 2001, Montreal, edited by A. J. McKerrow, Y. Shacham-Diamand, S. Zaima, T. Ohba, Materials Research Society, Warrendale, Pennsylvania (2002) 159-165

RELIABILITY REFERENCES

[1] J. Noguchi, IEEE TED, 52, 2005, pp. 1743-1750
[2] G.S. Haase, J. Appl. Phys., 105(4), 2009, 044908
[3] F. Chen, et al., IEEE T. El. Dev., 56(1), 2009, pp. 2-12
[4] J.R. Black, Proceedings of the IEEE, 57, (1969), pp.1587-1589
[5] C.K. Hu et al., Applied Physics Letters, 74, (1999), pp.2945-2947
[6] C.K. Hu et al., IEEE IIITC (2007) pp.93-95
[7] C.K. Hu et al., Microelectronics Reliability 46 (2006), pp.213-231
[8] E. Zschech et al., IEEE transaction on device and materials reliability, 9, (2009), p. 20
[9] I.A. Blech, J. Appl. Phys. (1976), pp.1203-1208
[10] A.S. Oates, IEEE IRPS (2009), pp. 452.
[11] L. Doyen et al ,J. Appl. Phys, vol 104 (2008) p. 12352
[12] E.T. Ogawa, IEEE IRPS , (2002), P. 312
[13] T. Oshima et al., IEEE- IEDM(2002)
[14] H.Y. Lin et al., IEEE IRPS, (2008), pp. 687-688
[15] N. Heylen et al., Proc. AMC, 2008, pp. 415-421
[16] S-Y Jung et al., IEEE IRPS, 2009
[17] M. Stucchi et al., IEEE IITC, 2008, pp. 174-176
[18] J.R. Lloyd et al., J. Appl. Phys., 98(8), 2005, 084109
[19] Zs. Tokei et al., IEEE IITC, 2009, pp. 228-230
[20] A. Yamaguchi et al., IEEE IITC, 2009, pp. 225-227
[21] J. Guo et al., IEEE TDMR, 8(4), 2008, pp. 652-663
[22] S. Shamuilia et al., Appl. Phys. Lett., 89(20), 2006, 202909
[23] J.M. Atkin et al., J. Appl. Phys., 103, 2008, 094104

INTERCONNECT PERFORMANCE REFERENCES

[1] W.F.A. Besling et al., Proc. of IEDM, 2006, pp. 325-328
[2] S.-P. Sim et al., IEEE Trans. on Electron Devices, 50 (6), 2003, pp. 1501-1510
[3] M.R. Baklanov et al., Proc. of IITC, 2004, pp. 187-189
[4] A. Farcy et al., Proc. of AMC, 2007, pp. 285-291
[5] M. Sellier et al., Proc. of ISQED, 2008, pp. 492-497
[6] R. Ho et al., Proc. of the IEEE, 2001, pp. 490-504
[7] M. Nanua et al., Proc. of ISQED, 2007, pp. 639-646
[8] M.A. El-Moursy et al., VLSI journal of Integration, 38, 2004, pp. 205-225
[9] N. Magen, Proc. of SLIP, 2004
[10] L. David et al., IEEE Trans. on Adv. Packaging, 2007, pp. 295-300

EMERGING INTERCONNECT REFERENCES

[1] N. Rana, et al., "Investigation of substrate selective covalent attachment for genetically engineered molecular interconnects", Materials Research Soc. Research Symp. Proceedings Vol. 728 (2002).

[2] R. Daamen, et. al., "The evolution of multi-level air gap integration towards 32 nm node interconnects", Microelectronics Engineering Vol. 84, Issues 9-10, 2007, pp 2177-2183.

[3] M. Bamal, et al., "Performance comparison of interconnect technology and architecture options for deep submicron technology nodes", IEEE International Interconnect Technology Conference 2006, pp. 202-204 (June 5-7, 2006, San Francisco, CA)

[4] J. Kim and W. A. Anderson, *Nano Lett.* 6, 1356-1359 (2006).

[5] C. A. Decker, R. Solanki, J. L. Freeouf, J. R. Carruthers, and D. R. Evans, *Appl. Phys. Lett.* 84, 1389-1391 (2004).

[6] Yue Wu1, Jie Xiang, Chen Yang, Wei Lu, and C. M. Lieber, *Nature* 430, 61-65 (2004).

[7] Chung-Yang Lee, Ming-Pei Lu, Kao-Feng Liao, Wei-Fan Lee, Chi-Te Huang, Sheng-Yu Chen, and Lih Juann Chen, *J. Phys. Chem. C* 113, 2286-2289 (2009).

[8] Yipu Song, Andrew L. Schmitt, and Song Jin, *Nano Lett*. 7, 965-969 (2007).

[9] J. H. Lee, E. T. Eisenbraun, and R. E. Geer, University at Albany-SUNY, *unpublished results* (2009).

[10] Q Wang , Q Luo and C Z Gu, *Nanotechnology* 18 195304, 1-5 (2007).

[11] Bin Li, Zhiquan Luo, Li Shi, Ji Ping Zhou , Lew Rabenberg, Paul S Ho, Richard A Allen and Michael W Cresswell, *Nanotechnology* 20, 085304, 1-7 (2009).

[12] Hsueh-Chung Chen, Hsien-Wei Chen, Shin-Puu Jeng, C.-H.M. Wu, and J.Y.-C. Sun, *Proceedings of the VLSI Technology, Systems, and Applications Symposium*, p. 1-2, (2006).

[13] Yugang Sun, Yadong Yin, Brian T. Mayers, Thurston Herricks, and Younan Xia, *Chem. Mat.* 14, 4736-4745 (2002).

[14] Zhi-Min Liao, Jia-Bin Xu, Xiao-Ming Sun, Ya-Dong Li, Jun Xu, Da-Peng Yu, *Physics Letters A* 373 1181-1184 (2009).

[15] Xiaohua Liu, Jing Zhu, Chuanhong Jin, Lian-Mao Peng, Daiming Tang and Huiming Cheng, *Nanotechnology* 19, 085711, 1-6 (2008).

[16] Yi Cui, Stanford University, *unpublished results* (2008).

[17] J. J. Plombon, Ebrahim Andideh, Valery M. Dubin, and Jose Maiz, *Appl. Phys. Lett.* 89, 113124-113126 (2006).

[18] Werner Steinhogl, Gunther Schindler, Gernot Steinlesberger, and Manfred Engelhardt, *Phys. Rev. B* 66, 075414-075417 (2002).

[19] M. Kralj, A. Siber, P. Pervan, M. Milun, T. Valla, P. D. Johnson, and D. P. Woodruff, *Phys. Rev. B.* 64, 085411-085419 (2001).

[20] Ratan Lal, *Phys. Rev. B* 68, 115417-115426 (2003).

[21] S. Mathias, M. Wiesenmayer, M. Aeschlimann and M. Bauer, *Phys. Rev. Lett.* 97, 236809-236812 (2006).

[22] N. Trivedi and N. W. Ashcroft, *Phys. Rev. B.* 38, 12298-12309 (1988).

[23] Supriyo Datta, Quantum Transport: Atom to Transistor (Cambridge Press, NY, 2005).

[24] A. E. Meyerovich and A. Stepaniants, *Phys. Rev. B*. 60, 9129-9144 (1999).

[25] A. E. Meyerovich and I. V. Ponomarev, *Phys. Rev. B* 67, 165411-165420 (2003).

[26] Yiying Cheng and A. E. Meyerovich, *Phys. Rev. B* 73, 085404-085415 (2006).

[27] A. Nieuwoudt and Y. Massoud, "Evaluating the impact of resistance in carbon nanotube bundles for VLSI interconnect using diameter-dependent modeling techniques," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2460-2466, 2006.

[28] M. S. Dresselhaus, G. Dresselhaus, and P. Avouris, *Carbon nanotubes: synthesis, structure, properties, and applications*. Berlin; New York:: Springer, 2001.

[29] H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Physical Review Letters,* vol. 95, pp. 086601-4, 2005.

[30] M. Nihei, D. Kondo, A. Kawabata, S. Sato, H. Shioya, M. Sakaue, T. Iwai, M. Ohfuti, and Y. Awano, "Low-resistance multi-walled carbon nanotube vias with parallel channel conduction of inner shells," in *Proc. IEEE Int. Interconnect Tech. Conf.*, 2005, pp. 234-236.

[31] P. L. McEuen, M. S. Fuhrer, and P. Hongkun, "Single-walled carbon nanotube electronics," *Nanotechnology, IEEE Transactions on,* vol. 1, pp. 78-85, 2002.

[32] S. Reich, C. Thomasen, and J. Maultzsch, *Carbon Nanotubes: Basic Concepts and Physical Properties*: Wiley-VCH, 2004.

[33] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied Physics Letters,* vol. 79, pp. 1172-1174, 2001.

[34] S. Berber, Y.-K. Kwon, and D. Tománek, "Unusually High Thermal Conductivity of Carbon Nanotubes," *Physical Review Letters,* vol. 84, p. 4613, 2000.

[35] J. Hone, M. Whitney, C. Piskoti, and A. Zettl, "Thermal conductivity of single-walled carbon nanotubes," *Physical Review B,* vol. 59, p. R2514, 1999.
[36] A. Naeemi and J. D. Meindl, "Design and Performance Modeling for Single-Walled Carbon Nanotubes as Local, Semiglobal, and Global Interconnects in Gigascale Integrated Systems," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 26-37, 2007.
[37] S. Salahuddin, M. Lundstrom, and S. Datta, "Transport effects on signal propagation in quantum wires," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 1734-1742, 2005.
[38] A.S. Verhulst, M. Bamal, and G. Groeseneken, "Carbon nanotube interconnects: will there be a significant improvement compared to copper?", poster at INC3, Brussels, Belgium, 17-19 April 2007.
[39] J. Y. Huang, S. Chen, S. H. Jo, Z. Wang, D. X. Han, G. Chen, M. S. Dresselhaus, and Z. F. Ren, "Atomic-Scale Imaging of Wall-by-Wall Breakdown and Concurrent Transport Measurements in Multiwall Carbon Nanotubes," *Physical Review Letters,* vol. 94, pp. 236802-4, 2005.
[40] C. Berger, Y. Yi, Z. L. Wang, and W. A. de Heer, "Multiwalled carbon nanotubes are ballistic conductors at room temperature," *Applied Physics A: Materials Science & Processing,* vol. 74, pp. 363-365, 2002.
[41] A. Naeemi and J. D. Meindl, "Compact Physical Models for Multiwall Carbon-Nanotube Interconnects," *Electron Device Letters, IEEE,* vol. 27, pp. 338-340, 2006.
[42] G. F. Close, S. Yasuda, B. Paul, S. Fujita, and H. S. P. Wong, "A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors," *Nano Lett.,* vol. 8, pp. 706-709, 2008.
[43] K. Liu, P. Avouris, R. Martel, and W. K. Hsu, "Electrical transport in doped multiwalled carbon nanotubes," *Physical Review B,* vol. 63, p. 161404, 2001.
[44] T. Hertel and G. Moos, "Electron-Phonon Interaction in Single-Wall Carbon Nanotubes: A Time-Domain Study," *Physical Review Letters,* vol. 84, p. 5002, 2000.
[45] E. Pop, D. Mann, J. Reifenberg, K. Goodson, and H. Dai, "Electro-thermal transport in metallic single-wall carbon nanotubes for interconnect applications," in *IEEE IEDM Digst.*, 2005, pp. 253-256.
[46] A. Naeemi and J. D. Meindl, "Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects," *Electron Device Letters, IEEE,* vol. 28, pp. 135-138, 2007.
[47] A. Cao, R. Baskaran, M. J. Frederick, K. Turner, P. M. Ajayan, and G. Ramanath, "Direction-Selective and Length-Tunable In-Plane Growth of Carbon Nanotubes," *Advanced Materials,* vol. 15, pp. 1105-1109, 2003.
[48] D. Mann, A. Javey, J. Kong, Q. Wang, and H. Dai, "Ballistic Transport in Metallic Nanotubes with Reliable Pd Ohmic Contacts," *Nano Lett.,* vol. 3, pp. 1541-1544, November 12, 2003 2003.
[49] M. Nihei, T. Hyakushima, S. Sato, T. Nozue, M. Norimatsu, M. Mishima, T. Murakami, D. Kondo, A. Kawabata, M. Ohfuti, and Y. Awano, "Electrical Properties of Carbon Nanotube Via Interconnects Fabricated by Novel Damascene Process," in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 204-206.
[50] M. Nihei, A. Kawabata, T. Hyakushima, S. Sato, T. Nozue, D. Kondo, H. Shioya, T. iwai, M. Ohfuti, and Y. Awano, "Carbon Nanotube Via Technologies for Advanced Interconnect Integration," in *Extended abstracts 2006 Int. Conf. on Solid State Devices and Materials*, 2006, pp. 140-141.
[51] P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme Oxygen Sensitivity of Electronic Properties of Carbon Nanotubes," *Science,* vol. 287, pp. 1801-1804, March 10, 2000 2000.
[52] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials,* vol. 6, pp. 183-191, 2007.
[53] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. deHeer, "Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics," *J. Phys. Chem. B,* vol. 108, pp. 19912-19916, December 30, 2004 2004.
[54] B. Obradovic, R. Kotlyar, F. Heinz, P. Matagne, T. Rakshit, M. D. Giles, M. A. Stettler, and D. E. Nikonov, "Analysis of graphene nanoribbons as a channel material for field-effect transistors," *Applied Physics Letters,* vol. 88, pp. 142102/1-142102/3, Apr 2006.
[55] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Physical Review B,* vol. 54, pp. 17954-17961, Dec 1996.
[56] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic Confinement and Coherence in Patterned Epitaxial Graphene," *Science,* vol. 312, pp. 1191-1196, May 26, 2006 2006.
[57] T. Ohta, A. Bostwick, T. Seyller, K. Horn, and E. Rotenberg, "Controlling the Electronic Structure of Bilayer Graphene," *Science,* vol. 313, pp. 951-954, August 18, 2006 2006.
[58] M. Y. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, "Energy Band-Gap Engineering of Graphene Nanoribbons," *Physical Review Letters,* vol. 98, pp. 206805-4, 2007.
[59] P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nature Nanotechnology,* vol. 2, pp. 605-615, 2007.

[60] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy Gaps in Graphene Nanoribbons," *Physical Review Letters,* vol. 97, pp. 216803-4, 2006.
[61] A. Naeemi and J. D. Meindl, "Performance Benchmarking for Graphene Nanoribbon, Carbon Nanotube, and Cu Interconnects," in *Int. Interconnect Technology Conference*, June 2008, pp. 183-185.
[62] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Communications,* vol. 146, pp. 351-355, 2008.
[63] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior Thermal Conductivity of Single-Layer Graphene," *Nano Letters,* vol. 8, pp. 902-907, 2008.
[64] C. Faugeras, A. Nerriere, M. Potemski, A. Mahmood, E. Dujardin, C. Berger, and W. A. de Heer, "Few-layer graphene on SiC, pyrolitic graphite, and graphene: A Raman scattering study," *Applied Physics Letters,* vol. 92, pp. 011914-3, 2008.
[65] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters,* vol. 9, pp. 30-35, 2009.
[66] H. M. Wang, Y. H. Wu, Z. H. Ni, and Z. X. Shen, "Electronic transport and layer engineering in multilayer graphene structures," *Applied Physics Letters,* vol. 92, pp. 053504-3, 2008.
[67] F. Cervantes-Sodi, G. Csanyi, S. Piscanec, and A. C. Ferrari, "Edge-functionalized and substitutionally doped graphene nanoribbons: Electronic and spin properties," *Physical Review B (Condensed Matter and Materials Physics),* vol. 77, pp. 165427-13, 2008.
[68] D. Kondo, S. Sato, and Y. Awano, "Self-organization of Novel Carbon Composite Structure: Graphene Multi-Layers Combined Perpendicularly with Aligned Carbon Nanotubes," *Applied Physics Express,* vol. 1, p. 074003, 2008.
[69] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature,* vol. 457, pp. 706-710, 2009.
[70] Y. Ouyang, X. Wang, H. Dai, and J. Guo, "Carrier scattering in graphene nanoribbon field-effect transistors," *Applied Physics Letters,* vol. 92, pp. 243124-3, 2008.
[71] A. Naeemi and J. D. Meindl, "Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects," *Electron Device Letters, IEEE,* vol. 28, pp. 428-431, 2007.
[72] Siegert, M.; Loken, M.; Glingener, C.; Buchal, C.; "Efficient optical coupling between a polymeric waveguide and an ultrafast silicon MSM photodiode," *IEEE Journal on Selected Topics in Quantum Electronics*, Volume 4, Issue: 6, Nov.-Dec. 1998, pp. 970 -974.
[73] Buca, D., Winnerl, S., Lenk, S., Mantl, S. And Buchal, Ch., "Metal-Germanium-Metal Ultrafast Infrared Detectors," *J. Appl. Phys*., Vol. 92, no. 12, December 2002, pp. 7599-7605.
[74] Oh, J., Banerjee, S.K. and Campbell, J.C., "Metal-Germanium-Metal Photodetectors on Heteroepitaxial Ge-on-Si with Amorphous Enhancement Layers," *IEEE Phot. Tech. Lett*., vol. 16, no. 2, February 2004, pp. 581-583.
[75] Yang, B., Schaub, J.D., Csutak, S.M., Rogers, D.L., and Campbell, J.C., "10 Gb/s All-Silicon Optical Receiver," *IEEE Phot. Tech. Lett.*, vol. 15, no. 5, May 2003, pp. 745-747.
[76] Colace, L., Masini, G. and Assanto, G., "Ge on Si Approaches to the Detection of Near-Infrared Light," *IEEE J. of Quantum Electronics*, vol. 35, no. 12, pp. 1843-1852.
[77] Matsuura, T., Yamada, A, Murota, J., Tamechika, E., Wada, K, and Kimerling, L.C., "Optoelectronic Conversion Through 850 nm Band Single mode Si3N4 Photonic Waveguides for Si-On-Chip Integration," *Device Research Conference*, 2002, 60th DRC. Conference Digest, June 24-26. 2002, pp. 93-94.
[78] Junichi Fujikata, Tsutomu Ishi, Daisuke Okamoto, Kenichi Nishi, and Keishi Ohashi, "Highly Eficient Surface-Plasmon Antenna and its Application to Si Nano-Photodiode", IEEE Lasers & Electro-Optics Society, 2006, pp. 476-477.
[79] K. Cadien, M. Reshotko, B. Block, A. Bowen, D. Kencke, and P. Davids, "Challenges for On-Chip Optical Interconnects," Proceedings of SPIE 2005, Vol. 5730, pp. 133-143.
[80] Superconductivity Fundamentals and Applications, Werner Buckel and Reinhold Kleiner, Wiley-VCH Verlag, 2004, p. 360.
[81] Superconductivity Fundamentals and Applications, Werner Buckel and Reinhold Kleiner, Wiley-VCH Verlag, 2004, p. 389.
[82] Andr and Dehon, "Nanowire-based programmable architectures," *J. Emerg. Technol. Comput. Syst.,* vol. 1, pp. 109-162, 2005.
[83] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature,* vol. 430, pp. 61-65, 2004.
[84] N. Patil, D. Jie, S. Mitra, and H. S. P. Wong, "Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits," *Nanotechnology, IEEE Transactions on,* vol. 8, pp. 37-45, 2009.

[85] A. Naeemi and J. D. Meindl, "Electron Transport Modeling for Junctions of Zigzag and Armchair Graphene Nanoribbons (GNRs)," *Electron Device Letters, IEEE,* vol. 29, pp. 497-499, 2008.
[86] V. V. Zhirnov, R. K. Cavin, III, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling - a gedanken model," *Proceedings of the IEEE,* vol. 91, pp. 1934-1939, 2003.
[87] R. Cavin, V. Zhirnov, D. Herr, A. Avila, and J. Hutchby, "Research directions and challenges in nanoelectronics," *Journal of Nanoparticle Research,* vol. 8, pp. 841-858, 2006.
[88] D. Nikonov and G. Bourianoff, "Operation and Modeling of Semiconductor Spintronics Computing Devices," *Journal of Superconductivity and Novel Magnetism,* vol. 21, pp. 479-493, 2008.
[89] D. D. Awschalom and M. E. Flatte, "Challenges for semiconductor spintronics," *Nature Physics,* vol. 3, pp. 153-159, 2007.
[90] G. Bourianoff, "The future of nanocomputing," *Computer,* vol. 36, pp. 44-53, 2003.
[91] J.-J. Su and A. H. MacDonald, "How to make a bilayer exciton condensate flow," *Nat Phys,* vol. 4, pp. 799-802, 2008.
[92] N. Tombros, C. Jozsa, M. Popinciuc, H. T. Jonkman, and B. J. van Wees, "Electronic spin transport and spin precession in single graphene layers at room temperature," *Nature,* vol. 448, pp. 571-574, 2007.
[93] A. Khitun and K. L. Wang, "Nano scale computational architectures with Spin Wave Bus," *Superlattices and Microstructures,* vol. 38, pp. 184-200, 2005.
[94] A. Khitun, D. E. Nikonov, M. Bao, K. Galatsis, and K. L. Wang, "Efficiency of Spin-Wave Bus for Information Transmission," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3418-3421, 2007.

PASSIVE DEVICE APPENDIX REFERENCES

[1] R. Mahnkopf et al., Digest 1999 IEDM, p. 849
[2] T. Schiml et al., Digest 2001 VLSI Technology Symposium, p. 101
[3] K. Miyashita et al., Digest 2001 VLSI Technology Symposium, p. 11
[4] C.C. Lin et al., Proc. 2001 IITC, p. 113
[5] K. Kuhn, et al.; Digest 2002 IEDM, p. 73
[6] S. Lee, et al.; Digest 2007 VLSI Technology Symposium, p. 54
[7] P. Gilbert, et al.; Digest 2007 IEDM, p. 259
[8] S.-Y. Wu, et al.; Digest 2007 IEDM, p. 263
[9] S. Ekbote, et al.; Digest 2008 VLSI Technology Symposium, p. 160
[10] C.-H. Jan, et al.; Digest 2008 IEDM, p. 637
[11] A. Kar-Roy et al., Proc. 1999 IITC, p. 245
[12] R. Liu et al., Proc. 2000 IITC, p. 111
[13] M. Armacost et al., Digest 2000 IEDM, p. 157
[14] P. Zurcher et al., Digest 2000 IEDM, p.153
[15] S. Van Huylenbroeck, et al., IEEE Electron Dev. Lett., Vol.23, 2002, p.191
[16] C.H. Ng, et al., Digest 2002 IEDM, p.241
[17] C.H. Ng, et al.; IEEE Electron Dev. Lett., Vol. 24, 2003, p. 506
[18] C.H. Ng, et al.; IEEE Electron Dev. Lett., Vol. 25, 2004, p. 489
[19] D. Roberts, et al.; Digest 2005 IEDM, p. 77
[20] H. Sanchez, et al.; Proc. 2007 IITC, p. 84
[21] D. C. Sekar, et al.; Proc. 2006 IITC, p. 48
[22] T. Ishikawa, et al., Digest 2002 IEDM, p. 940
[23] P. Mazoyer, et al., Proc. 2003 IITC, p.117
[24] Y.L. Tu, et al., Digest 2003 VLSI Technology Symposium, p. 79
[25] S.J. Kim, et al., Digest 2003 VLSI Technology Symposium, p. 77
[26] X. Yu, et al., IEEE Electron Dev. Lett., Vol. 24, p. 63, 2003
[27] S.J. Kim, et al.; Digest 2005 VLSI Technology Symposium, p. 56
[28] K.C. Chiang, et al.; Digest 2005 VLSI Technology Symposium, p. 62
[29] S.-J. Kim, et al.; IEEE Electron Dev. Lett., Vol. 26, 2005, p. 625
[30] D. Brassard, et al.; IEEE Electron Dev. Lett., Vol. 28, 2007, p. 261
[31] Y. H. Jeong, et al.; IEEE Electron Dev. Lett., Vol. 28, 2007, p. 17
[32] K.C. Chiang, et al.; Digest 2006 VLSI Technology Symposium, p. 126
[33] K.C. Chiang, et al.; IEEE Electron Dev. Lett., Vol. 28, 2007, p. 235
[34] N. Inoue, et al.; Proc. 2006 IITC, p. 63
[35] C.H. Cheng, et al.; IEEE Electron Dev. Lett., Vol. 28, 2007, p. 1095

[36] C.H. Cheng, et al.; IEEE Electron Dev. Lett., Vol. 29, 2008, p. 845
[37] K.-H. Cho, et al.; IEEE Electron Dev. Lett., Vol. 30, 2009, p. 614
[38] I. Kume, et al.; Proc. 2008 IITC, p. 225
[39] H. Hu, et al.; Digest 2003 IEDM, p. 379
[40] Y. Jeong, et al.; Digest 2004 VLSI Technology Symposium, p. 222
[41] K. Takeda, et al.; Proc. 2005 IITC, p. 91
[42] M. Thomas, et al.; Proc. 2007 IITC, p. 158
[43] M. Thomas, et al.; Digest 2007 VLSI Technology Symposium, p. 58
[44] S. Jeannot, et al.; Digest 2007 IEDM, p. 997
[45] N. Inoue, et al.; Digest 2007 IEDM, p. 989
[46] R. Aparicio, et al., IEEE J. Solid-State Circuits, Vol. 37, 2002, p. 384
[47] J. Kim, et al., Digest 2003 VLSI Circuits Symposium, p. 29
[48] N. Zamdmer, et al.; Digest 2004 VLSI Technology Symposium, p. 98
[49] D. Kim, et al.; IEEE Electron Dev. Lett., Vol. 28, 2007, p. 616
[50] A.H. Fischer, et al.; Proc. 2008 IRPS, p. 126
[51] I.M. Kang, et al.; IEEE Electron Dev. Lett., Vol. 30, 2009, p. 538
[52] J.N. Burghartz, Proc. 1997 ESSDERC, p. 143
[53] J.N. Burghartz, Digest 1998 IEDM, p. 523
[54] J.N. Burghartz, Proc. 1999 ESSDERC, p. 56
[55] D.C. Edelstein, J.N. Burghartz, Proc. 1998 IITC, p. 18
[56] J. Rogers et al., Proc. 1999 IITC, p.239
[57] K. Saito et al., Proc. 2000 IITC, p. 123
[58] Y. Nakahara et al., Digest 1999 IEDM, p.861
[59] S. Jenei et al., Proc. 2001 IITC, p. 107
[60] Y.S. Choi, et al.; IEEE Electron Dev. Lett., Vol. 25, 2004, p. 76
[61] L.F. Tiemeijer, et al.; IEEE Electron Dev. Lett., Vol. 25, 2004, p. 722
[62] C.-H. Chen, et al., IEEE Electron Dev. Lett., Vol. 22, 2001, p. 522
[63] C.S. Lin, et al.; IEEE Electron Dev. Lett., Vol. 26, 2005, p. 160
[64] J.-B. Yoon, et al., IEEE Electron Dev. Lett., Vol. 23, 2002, p. 591
[65] H. Sagkol, et al.; IEEE Electron Dev. Lett., Vol. 26, 2005, p. 541
[66] A. Chin, et al.; Digest 2003 IEDM, p. 375
[67] D.D. Tang, et al.; Digest 2003 IEDM, p. 673
[68] K. Chong, et al.; IEEE Electron Dev. Lett., Vol. 26, 2005, p. 93
[69] K. Hijioka, et al.; Proc. 2006 IITC, p. 60; Y.Hayashi; Digest 2006 IEDM, p. 363
[70] W. Jeamsaksiri, et al.; Digest 2005 VLSI Technology Symposium, p. 60
[71] D. Gardner et al., Proc. 2001 IITC, p. 101
[72] M. Yamaguchi, et al., IEEE Trans. Microw. Theory Techn., Vol. 49, 2001, p.2331
[73] D.S. Gardner; et al.; Digest 2006 IEDM, p. 221
[74] Y. Zhuang, et al., IEEE Electron Dev. Lett., Vol. 24, 2003, p. 224
[75] K. Hijioka, et al.; Proc. 2008 IITC, p.186
[76] T. Ohguro, et al.; Digest 2004 VLSI Technology Symposium, p. 220
[77] L. H. Guo, et al.; IEEE Electron Dev. Lett., Vol. 26, 2005, p. 619
[78] K. Okada, et al.; IEEE Transactions on Electron Devices, Vol. 53, 2006, p. 2401
[79] C.S. Pai, et al.; Proc. 2001 IITC, p. 216
[80] D. Nachrodt, et al.; IEEE Electron Dev. Lett., Vol. 29, 2008, p. 212