INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2009 EDITION

LITHOGRAPHY

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SCOPE

In 2009 and beyond, maintaining the rapid pace of half-pitch reduction requires overcoming the challenge of improving and extending the incumbent optical projection lithography technology while simultaneously developing alternative, next generation lithography technologies to be used when optical projection lithography is no longer more economical than the alternatives. Extending optical projection lithography at 193 nm wavelength using immersion lenses and developing multiple exposure techniques pose significant technical challenges. Not only is it necessary to invent novel technical solutions, but it is also critical that die costs remain economical with rising design, process development, and mask costs and cost of ownership of the tool and process. Extending optical projection lithography and developing next generation lithographic technology requires advances in the following areas:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask-making equipment, and materials
- Metrology equipment for critical dimension measurement, overlay control, and defect inspection

This chapter outlines a fifteen-year roadmap of difficult challenges, technology requirements, and potential solutions in lithography. Additionally, it defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for *Design*, *Front End Processing (FEP)*, *Process Integration, Devices, and Structures (PIDS)*, *Environment, Safety, and Health (ESH)*, *Yield Enhancement*, *Factory Integration, Metrology*, and *Modeling and Simulation*.

The key requirements of lithography for manufacturing integrated circuits are summarized below. *Table LITH3* lists the requirements that are needed based on the device type and half-pitch:

- *Critical Dimension (CD) Control*—The size of many features in a design needs to be precisely controlled. CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer. CD control is required for obtaining adequate transistor, interconnect, and consequently overall circuit performance.
- *Overlay*—The placement of the image with respect to underlying layers needs to be accurate in all locations on each integrated circuit to achieve adequate yield.
- *Defect Control*—The desired pattern must print in all locations with no additional anomalies. No particles should be added to the wafer during the lithography process.
- *Low Cost*—The cost of tools, materials (including resists), and masks needs to be as low as possible while still meeting the CD control, overlay, and defect control requirements. To minimize cost, the lithography step should be performed as quickly as possible. Masks should be used to expose as many wafers as possible. Equipment needs to be reliable and ready to expose wafers when needed.

To continue as the dominant technique for leading-edge critical layer lithography, resolution enhancement techniques (RETs) such as off-axis illumination (OAI), phase shifting masks (PSMs), and optical proximity corrections (OPCs) are being used with imaging systems at the 193 nm wavelength. In addition to RETs, lenses with increasing numerical apertures and decreasing aberrations will be required to extend the life of optical lithography. Liquid immersion imaging with a fluid between the final lens element and the wafer is also being used to extend optical lithography. *Table LITH1* shows the progression of RET and other techniques to extend optical lithography. It become much more difficult and expensive to implement OPC and resolution enhancement at each successive technology generation, new techniques such as source mask optimization (SMO) and inverse lithography (IL) are being introduced to further extend the process latitude associated with the multiple pattern types that the designers create. These improvements are being combined with design for manufacturing (DFM) to permit optimal solutions. Some of the DFM tricks include designing critical geometries in one direction. The range of pitches is also being limited. All of these techniques lower the k1 of the solution space and provide more process latitude for low k1 solutions.

DIFFICULT CHALLENGES

Table LITH2a and *Table LITH2b* show the most difficult of near-term challenges and long-term challenges of the continually shrinking minimum half-pitch, respectively. The dividing point between the two tables comes at the 20 nm half-pitch. Above 20 nm, traditional optical solutions can still be used, but below there are no proven optical solutions. The tables divide the challenges by level of difficulty as determined by the international community.

DIFFICULT CHALLENGES—NEAR TERM > 22 NM

MASK MAKING

The leading challenge for the near term and a significant challenge for the long term is the mask. Mask-making capability and cost escalation continue to be critical to future progress and will require continued focus. Masks are both a commodity and an enabler of progress along the roadmap. The need for expensive high-end capital equipment in the mask shop along with low initial market volumes makes the market difficult for commercial mask shops. As a consequence, the mask industry has experienced numerous consolidations and partnerships to address the issues. This has in turn decreased the volume of capital equipment that is sold into the leading-edge market, further driving costs up, resulting in just-in-time capital equipment that is needed to develop the mask process for the industry.

The mask specifications have increased more quickly than the half-pitch designated by the roadmap.[1] Historically, this increase has been driven by the MPU gate line width (post-etch) and the greater mask error enhancement factor (MEEF) associated with low k_1 lithography. The need for 2X patterns on the mask (i.e., sub-resolution enhancement patterns) has also contributed to the specifications, and double patterning demands mask registration specifications that far outpace the half-pitch in the roadmap (See *Table Lith5b.*).

Progressive defect formation has become a greater problem with organic and inorganic deposits forming on masks after many wafers are exposed. This has caused a 13X increase in the reworking of masks made for 193 nm lithography compared to older 248 nm technology.[2] Mask damage from electrostatic discharge (ESD) has long been a concern; it is expected to be even more problematic when mask feature sizes shrink. As CDs become more critical, electric field migration (EFM) has also been shown to change CD sizes.

DOUBLE PATTERNING/SPACER TECHNOLOGY

Meeting the required resolution with a single exposure is driving the use of multiple exposures to define each device layer. Some double exposure techniques are already being used, including alternating phase shift plus trim and double dipole exposures. These techniques allow for imaging at closer to the diffraction limit (k_1=0.25). New multiple exposure techniques are designed to form images beyond the single-exposure diffraction limit; these place additional requirements on lithography that vary by the specific type of multiple exposure technique *(*Table LITH5b).

Two basic processes, *pitch splitting* (PS) and *spacer patterning* (SP), and their requirements are defined by the differences in their critical lithography patterning steps. PS includes the traditional double *patterning* (DP) of two separate lithography/etch steps to define a single device layer, often called (litho etch litho etch [LELE]), and double exposure (DE), which is two lithographic exposures into one material with only one etch step. This can incorporate non-linear resists or a litho freeze process. The SP process uses one critical lithography step and then additional thin film deposition and etches steps in a spacer-like process to define two sets of critical features. (Note that this process also requires a second cut mask similar to the dipole lithography cut mask.) Spacer double patterning eliminates an exposure, but the allowable shapes are limited because the single exposure defines the location of the features. Figure LITH1 is a schematic of the process flows for these different approaches.[3, 4, 5, 6]

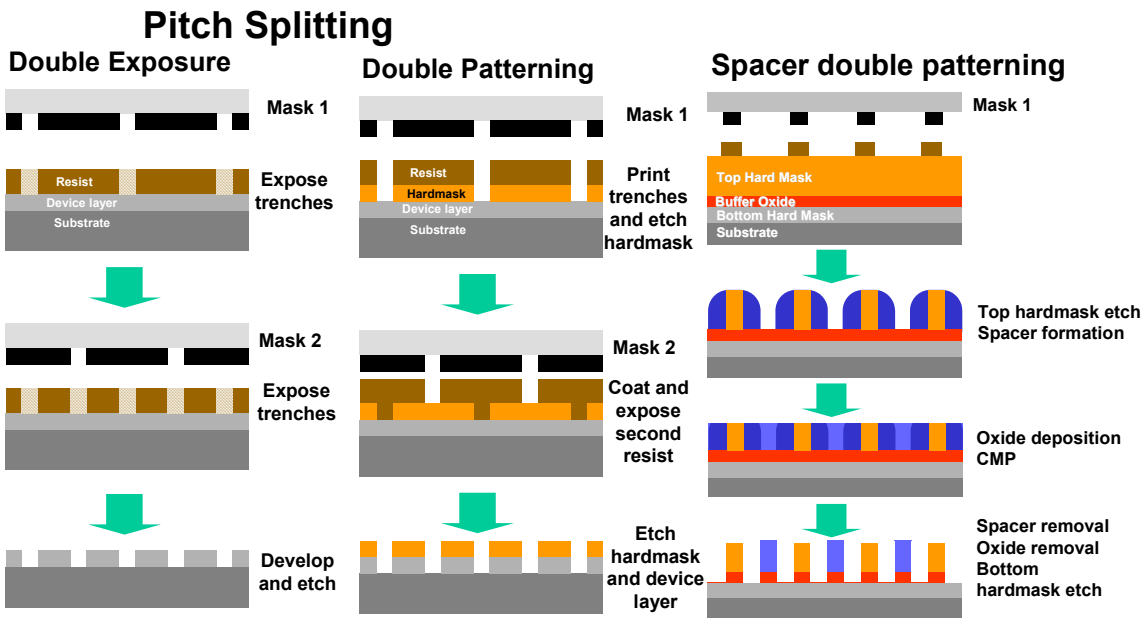

Figure LITH1 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

All these technologies present their own challenges, as listed in *Table LITH2A and B*. Overlay and CD challenges are defined in *Table LITH5b*.

COST CONTROL

Many drivers dictate the direction of future technology. Sometimes this is called Moore's Law, but even that is based on cost of ownership (COO) in that halving the area of a chip every 2–3 years decreases its cost. Thus, the COO of emerging technologies must be watched to address their cost-effectiveness and weigh it against the level of difficulties that they will pose. Figure LITH2 summarizes wafer cost of ownership from the 65 nm node out to the 22 nm node. It considers two of the four future technologies (DP and EUV) for a device used for just 5000 wafers/device (or mask set).[7] Note that this represents the projected cost difference of one of the critical layers and thus exaggerates the overall difference since not all layers are critical. The bottom of the mask (reticle) cost bar shows the cost of all the process steps other than the mask cost. At the 45 nm half-pitch node, a DP process is about 2× the cost of a single exposure litho process. This is true with or without the mask cost bar. Note also that the cost of the two masks is about 1.5× the cost of a single mask due to more data for the two masks and longer inspection and repair times. For each successively smaller node, content on the mask typically grows by a factor of 2. In fact, to accommodate the optical pattern correction to achieve sub-wavelength imaging, the data growth per node has been expanding much faster than what doubling the pattern content would imply. The historical data growth rate has been 2.7× per node over the last 8 years rather than 2× would be expected. At the 32 nm node, the cost of an EUV lithography tool and consumables is more than double its optical counterpart. But the mask cost of an optical mask far outweighs litho tool costs because of the excessive data to write these masks. Write time estimates for an optical mask at the 32 nm node exceed 35 hours, whereas an EUV mask is projected to be written in under 9 hours. This is because OPC for EUV masks is significantly simpler. The COO difference between EUV and double patterning continues to accelerate into the 22 nm node.

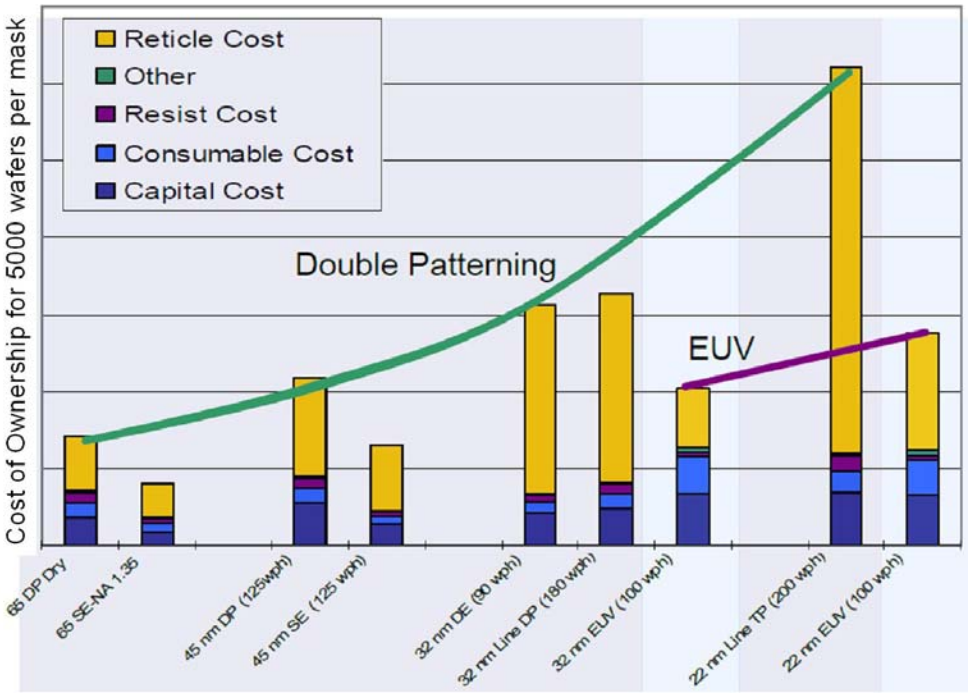

Figure LITH2 Relative Cost of Ownership for the critical level of a 5000 wafer run device

PROCESS CONTROL

Many challenges are associated with variability control, not just scaling. Variability control not only must keep up with dimensional scaling, but often needs to improve even faster.

To achieve demanding CD control tolerances, resolution enhancement techniques, design restrictions, and automated process control are being employed, as shown in *Table LITH1*. To further extend optical lithography, new practices are required to better comprehend the increasing variation of critical dimensions as a fraction of the feature size in the design process. These practices are usually referred to as "design for manufacturing" (DFM). DFM allow designers to account for manufacturing variations during circuit design optimization, enabling the IC fabrication process to be optimized to provide the highest performance at a minimal cost. Ultimately, the designer could optimize the circuit with knowledge of all physical variations in the fabrication process and their statistical distribution. At the simplest level, designers are being made aware of library cells that have yielded well in manufacturing. Furthermore, simulations of the lithography, etch, and CMP processes are being used to examine the full chip area for weak spots in the layout that are most susceptible to manufacturing variations. Coordinates of these weak points are provided to mask and wafer CD metrology tools. Focus and exposure are optimized for printing weak spot regions with maximum process latitude rather than for test structures. The topographical features of these printed weak spots need to be evaluated with pattern fidelity metrology. The weak spot locations are then targeted for layout modification and monitoring during manufacturing. Automation of software to analyze these weak spots in design and feedback to the physical layout of cells is being aggressively pursued by electronic design automation (EDA) suppliers. DFM tools and techniques will be essential to minimizing mask revisions and achieving adequate yield in the wafer fab. See the *Design chapter* for more information on DFM.

Table LITH1 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography

DIFFICULT CHALLENGES—LONG TERM ≤ 22 NM

In the far term, lithography will have to move to one of several *next generation lithography* (NGL) approaches. The leading candidate is EUV, which leads the list of challenges in *Table LITH2b* followed by resist materials, EUV masks, and cost of

ownership. Among EUV concerns, source power is most prominent followed by cost of ownership, resist, and mask defects. These issues have been at the forefront of EUV issues for over the 5 years that they have been tracked.[8] The leading choice of source power has changed in the last 2 years from DPP to LPP. Concerns about COO have been consistent since the difficulties associated with the EUV technology and its infrastructure constantly involve new and more challenging materials and technologies. Resist challenges involve pushing the limits of LER and exposure dose at leading-edge pitches. If all these needs cannot be met simultaneously, EUV will not be cost-effective. The mask issues are numerous, involving many new changes that must be met simultaneously. Masks will require LTEM substrates, zero-defect multilayer reflecting surfaces, and new pattern absorber materials. The greatest concern is with phase defects, which for 22 nm half-pitch lithography can be as small as a 20 disk that is 180 deg in phase or (2.5–3.5 nm high) (*Table LITH5b line 28-29*). The infrastructure for detecting this size has still not been developed on either substrates or blank or patterned masks, although programs are underway to realize this.

In the longer term, even more demanding overlay, defect, and CD control requirements will continue to pose challenges for process control, resist development, and mask development. The possible use of maskless lithography will probably require die-to-database inspection of wafers to replace die-to-database inspection of masks. Because imprint lithography templates have the same dimensions as the wafer pattern, mask fabrication becomes more challenging. Resist materials will also require significant improvements. Acid diffusion in chemically amplified resist might limit the ultimate minimum half-pitch that can be achieved with high sensitivity resists unless diffusion length is reduced or new methods of sensitizing resists are found. Resist materials with inherently high dimensional control for uniform CD and low line width roughness patterning will also be needed.

Table LITH2A Lithography Difficult Challenges >22nm

Difficult Challenges > 22 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features Registration, CD, and defect control for masks Eliminating formation of progressive defects and haze during exposure Understanding and achieving the specific signature and specifications for a Double Patterned mask Establishing a stable process so that signatures can be corrected.
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs Availability of high productivity scanner, track, and process to maintain low cost-of-ownership Photoresists with independent exposure of multiple passes Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time ROI for small volume products Resources for developing multiple technologies at the same time Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume 450 mm diameter wafer infrastructure
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error Controlling LER, CD changes induced by metrology, and defects < 10 nm in size Greater accuracy of resist simulation models Accuracy of OPC and OPC verification, especially in presence of polarization effects Lithography friendly design and design for manufacturing (DFM)

Table LITH2B Lithography Difficult Challenges ≤22 nm

Difficult Challenges ≤22 nm	*Summary of Issues*
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm rms figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion length Materials with improved dimensional and LWR control add (limits) Resist and antireflection coating materials composed of alternatives to PFAS compounds Low defects in resist materials (size < 10nm) Line width roughness < 1.4nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair) Mask process control methods and yield enhancement Cost control and return on investment
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput Development of cost-effective post-optical masks Cost effective 450mm lithography systems Achieving ROI for small volume products
193 nm Immersion Multilple Patterning	Cost control and return on investment Wafer processing to tighter overlay and CD controls Mask fabrication to tighter specifications
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s Metrology for achieving < 2.8 nm 3s wafer overlay error Template inspection for 1X Imprint Patterned Masks Phase shifting masks for EUV
Gate CD control improvements and process control	Development of processes to control gate CD < 1.5 nm 3s with < 1.4 nm 3s line width roughness Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3s overlay error, especially for imprint lithography

Table LITH2B Lithography Difficult Challenges ≤22 nm

Difficult Challenges ≤22 nm	*Summary of Issues*
Maskless Lithography	Wafer Throughput Cost control and return on investment Die-to-database inspection of wafer patterns written with maskless lithography Pattern placement - including stiching Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free Imprint templates at 1X dimensions Infrastructure for 1X technology Templates (key here is inspection!) Template fabrication to tighter specifications Protection of Imprint templates from defects without pellicles Mask Life time Throughput Cost control and return on investment Overlay Process control methods to compensate for systematic CD and overlay errors

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Table LITH3)
- Resist Requirements (Tables LITH4a and b)
- Mask Requirements (Tables LITH5a-d)
- Maskless Requirements (Table LITH6)

Table LITH3 Lithography Technology Requirements

The format of Table LITH3 reflects the differences in the lithographic requirements that are set by ORTC - Product Generations and Chip Size Model Technology Trend Targets .The table specifies three device types that push the lithographic requirements the most: DRAM half-pitch (contacted), MPU/ASIC Metal half-pitch, and Flash half-pitch (uncontacted poly). The Flash device pushes the half-pitch the most while MPU pushes the physical gate length and CDs the most. Each of these technologies needs a different specification for CD control, contact size, and overlay depending on the half-pitch and design. The table uses the values from the ORTC table (fixed numbers) and then equations to determine the other specific parameters associated with a particular specification. For example, CD control for the DRAM device is 12% of the DRAM half-pitch times the percentage of the error budget shared between lithography and etch (in quadrature).

For each device type, the k1 needed to image the required half-pitch is defined. In general, if k1 is less than 0.28, a double patterning process is needed (colored light blue). If k1 is less than 0.13, more than double patterning will be needed (hence, it is color-coded red).

At the bottom of the table are other wafer specifications from other ORTC tables. Note that NA specifications also show an increasing trend over time until they are coded red, indicating that practical physics will not allow us to move higher at this time.

Requirements for a short MPU gate length after etch create significant challenges for metrology and process control. Controlling critical dimensions to a required ± 12% tolerance of the final etched gate CD is becoming increasingly more difficult. This 12% includes cross-field, cross-wafer, wafer-to-wafer, and lot-to-lot variations. Post-development line width reduction techniques are becoming more prevalent and more capable. Printing larger features in resist improves CD control by providing for a larger lithography process window. Integrated circuit manufacturers are also modifying design rules to make the patterning task more feasible. Metrology will play a critical role in defining these lithography-friendly design rules.

Table LITH4a Resist Requirements

Photoresists need to be developed that provide good pattern fidelity, good line width control, low line width roughness, and few defects. As feature sizes get smaller, defects and monomers will have comparable dimensions with implications for the filtering of resists. See Table LITH4a.

The effects of line edge roughness (LER) and line width roughness (LWR) are also becoming increasingly apparent in device performance; therefore, metrology tools need to be modified to accurately measure these variations. High frequency line width roughness affects, dopant concentration, profiles and interconnect wire resistance. Line width roughness at higher spatial frequencies results in variations of transistor gate length over the active region of the device. This variation increases leakage and causes the speed of individual transistors to vary, which in turn leads to IC timing issues. The line width and line edge roughness also contributes to the CD uniformity error budget for small gate lengths and long LER/LWR correlation lengths. The CD uniformity component from LER/LWR is likely to drive the required LER/LWR numbers even more aggressively than in previous roadmaps. Because of the particular challenges associated with imaging contact holes, the size of contact holes after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gate length. See *Table LITH3* for the technology requirements.

Table LITH4b Resist Sensitivities

The resist sensitivity tables are based on the CoO associated with the different lithography approaches. The more sensitive the resist the more wafers that can be processed. But in general there is a limit associated with the three parameters that the resist has to maintain: sensitivity, resolution, and LWR. Improvements of any one of these usually come at the cost of the other specifications. Moves to improve the photon quantities by increasing the illumination power associated with the lithography tools are going on. This will allow faster throughput or may allow users to use less sensitive resists for improved resolution and LWR.

Table LITH5a Optical Mask Requirements

Mask requirements center on critical layers. Early volumes are assumed to be relatively small and difficult to produce. Optical masks are addressed in two tables (Tables LITH5a and LITH5b) to cover single and double layer lithography. The masks for all next generation lithographies (NGLs) are different from optical masks, and no NGL technology can support a pellicle. Because the requirements for NGL masks are substantially different from those for optical lithography, EUV masks and imprint templates are addressed in separate tables (Tables LITH5c, LITH5d, respectively).

CD control and overlay tolerances are the most difficult requirements to achieve. Overlay tolerances have become more demanding to fabricate memory circuits with higher yield. To minimize the effect of lens distortion on overlay error, a single exposure tool may be used to print multiple critical layers on the same wafers. Both feedback and feed-forward approaches need to be supported by process tools (scanners and tracks). The automation framework and CIM system need to comply with a large set of correcting models and algorithms, which might be highly non-linear. See the *Crosscut* section under Factory Integration for more detail on automated process control (APC) requirements.

The table presents basic wafer requirements from LITH3 (top) followed by mask magnification and specific mask specifications. The equations for generating the specification are shown in the function box. These equations have been used for the last 8 years. The mask overlay contribution is set at 15% of the wafer overlay budget. The mask CD contribution is set at 40% of the wafer CD uniformity budget. The specific specification is then driven by the MEEF associated with printing that particular feature.

Table LITH5b Double Patterning Requirements

The double patterning table is divided into four parts, leading with wafer requirements and then two sets of lithographic requirements (Generic Pitch Splitting - Double Patterning Requirements Driven by MPU metal Half-Pitch and Generic Spacer Patterning Requirements - Driven by Flash). The lithography requirements are different for each process; the requirements for pitch splitting are based on the MPU metal half-pitch. The fundamental premise is that both the line and the space must meet

the 12% CD specification. Since the space depends on the overlay and printed line width, meeting the 12% specification drives the overlay specification for double pattering. Further, to make the overlay specification as large as possible, the line width needs to be controlled to the tightest possible. In the tables, this means the double patterning line width must be controlled to the specification that an MPU gate line width would be controlled to. The mask specifications needed to support this specification are shown in the bottom rows. The matched double patterning mask image placement must be tighter than a single mask overlay by the square root of 2. Therefore, the mask-to-mask overlay contribution in any particular location must be 20% of the total pitch splitting error budget.

The wafer CD error budgets for spacer patterning are also driven by the need to have both the line and space within the 12% CD specification. The specifications are based on what has been demonstrated. Core gap line width control is based on what can be done with an MPU gate line. The lines widths are based on current deposition technologies. The mean space CD difference of the two space distributions then depends on the 12% space CD error budget and the CD errors in the lines and the core gap space. The overlay specification associated with the cut mask is then driven by the need to place the edge of the cut in the middle of the space and in the CD control of the pattern that is being imaged. This is about the same as the single pattern overlay specification.

Although the optical mask table is extended to 9 nm DRAM half-pitch, no optical solutions are yet known below the 23 nm DRAM half-pitch in 2017.

Table LITH5c EUV Mask Requirements

Table LITH5c covers the requirements for EUV masks. Note that some requirements are common to optical masks and some are EUV mask-specific. The common requirements (CD and registration related) are developed in the same way that the optical requirements are. Note that since the k1 is larger, the role of MEEF is less and detailed in the equation rather than itemized in a specific line. This makes the patterning of EUV CDs easier than optical masks. The patterned defect size requirements are the same as optical masks but the coloring indicates that detection capability with just a reflected light inspection is more difficult. The data volume needed for the EUV mask is less than optical since EUV masks are made for a higher k1 and the OPC content a lot less.

The EUV-specific mask requirements include substrate/blank defects, substrate reflectivity, sidewall angle, LWR, and mask flatness. The blank defect line is new this year; the values are based on phase defects that can occur when fabricating the multilayer reflective coating and substrate defects (pits and bumps). This is a complicated term since a phase defect has an associated phase (driven by height) and a size characteristic. This specification is based on a worst-case defect approach as is done with all the defect specifications in the roadmap. Thus the specification is the size of a 180 degree defect, which is 3 nm high for an EUV reflective mask. As is noted in the footnote, a 90 degree defect (1.5 nm high) will also cause a CD defect if it is about twice the specification size. As EUV moves closer to manufacturing, this specification and the substrate specification will be improved.[9, 10, 11, 12]

EUV mask flatness has a very tight specification, since non-flatness causes a registration error associated with the off-axis illumination of the masks. The specification for flatness is such that it contributes an equal amount to the wafer registration error as mask patterning does. Ongoing research may allow this specification to be loosened in the future. This is being based on the concept of measuring a mask's non-flatness and then correcting the position of the patterns such that when the mask is imaged the pattern will be in the correct location even if the mask did not meet the flatness specification.[13, 14]

EUV mask blanks must be free of small defects, requiring development of new inspection tools and low defect fabrication processes. Solutions for protecting the masks from defects added during storage, handling, and use in the exposure tool need to be developed and tested because there are no known pellicle options for EUV masks or imprint templates. These different NGL mask requirements can be expected to exacerbate, rather than relieve, the high costs of masks.

Table LITH5d Imprint Template Requirements

Imprint may take several forms. The table lists requirements specific to ultraviolet nanoimprint lithography (UV-NIL), in which UV radiation is used to cure the liquid filling the template. Imprint templates have surface relief features that are the same size as the wafer features, but the area that needs to be controlled for CD, pattern placement, and defects is 16× smaller than for comparable 4× masks for other technologies. The mask specification are developed the same way that optical mask specifications are but they are tighter because the magnification is 1×. Inspecting defects on these masks is difficult because the wafer requirements are translated directly to the mask as 10% of the wafer CD specification. The registration is also difficult but is shared equally in quadrature between the two masks and the system overlay.

Table LITH6 Maskless Technology Requirements

The maskless requirements are the same as the wafer requirements. The only unique ones are that the data volume is half that of an optical mask and the grid size is one-quarter of the optical requirements. All these specifications will be reviewed in the next versions of the ITRS.

POTENTIAL SOLUTIONS

The potential solutions for leading-edge, critical layer lithography are presented in Figure LITH3 Potential Solutions. The order of the options represents the probability of a particular technology to be the dominant solution for a given technology generation with the most probable options listed first. All of the infrastructure required to use the lithography technologies at the time shown must be ready—including tools, masks, and resist. Immersion Optical lithography at 193 nm wavelength is the dominant approach through DRAM 45 nm half pitch. But this is the last node that simple single patterning approaches will be used. Below 45 the k1 is less than 0.3 for single patterning and some form of double patterning or spacer doubling will be used. Flash memory is the pitch driver into the future. It is leading the way at the 32 nm half pitch in 2010. It is using a spacer technology to achieve the half pitch with the litho imaging technology of the 45 nm node. By 2013 Flash, MPU and DRAM will use either a double patterning—spacer technology or EUV if all of the infrastructure is ready for the 22 nm and 32 nm nodes respectively. ML2 and Imprint still are a possibility at this time but they appear not to be the most cost effective solutions.

No proven 193 optical solutions are available beyond the 22 nm half-pitch. Doubling the half-pitch of a 193 high NA stepper gets us to the 20 nm half-pitch with a k1 of 0.28.

The post-optical alternatives are potential solutions at and below DRAM 22 nm half-pitch. Of the possible alternative technologies, multiple geographical regions consider EUV, maskless, and imprint lithography as potential successors to optical lithography. Considering only post-optical approaches, EUV is viewed as the most likely for 22 nm and 16 nm half-pitch patterning. Maskless lithography has been applied to niche applications for prototyping and transistor engineering and to low volume application-specific integrated circuit (ASIC) production, but its role could be expanded. Breakthroughs in direct-write technologies that achieve high throughput could be a significant paradigm shift, eliminating the need for masks and reducing cost and cycle time. Maskless lithography for applications beyond prototyping is currently at the alpha tool phase, but many technological challenges will need to be overcome for ML2 to be viable for cost-effective semiconductor manufacturing. Imprint lithography has the potential to be a cost-effective solution, but several problems need to be solved for this to happen, including the difficulties associated with 1× templates, defects, template lifetime, and overlay. This technology appears to have found a niche market in the pattern media market that will help evolve many of the solutions that are needed for the semiconductor market place. This technology also has beta tools strategically placed in the semiconductor community to help understand and solve its manufacturing difficulties.

It is unclear whether any technology currently identified as a potential solution will indeed be capable of meeting the requirements for DRAM 16 nm half-pitch and below, necessitating innovative technology development. Among these, directed self-assembly, in which the molecular structure of the imaging material drives the sub-lithographic feature sizes and control, is thought to be a viable option.

Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions within industry and between industry and universities are necessary to narrow the options for these future generations and focus support to enable one or perhaps two technologies to be ready for manufacturing at the desired time. The introduction of non-optical lithography will be a major paradigm shift that will be necessary to meet the technical requirements and complexities for continued adherence to Moore's Law at DRAM 22 nm half-pitch and beyond. This shift will drive major changes throughout the lithography infrastructure and require significant resources for commercialization. These development costs must necessarily be recovered in the costs of tools, masks, and materials.

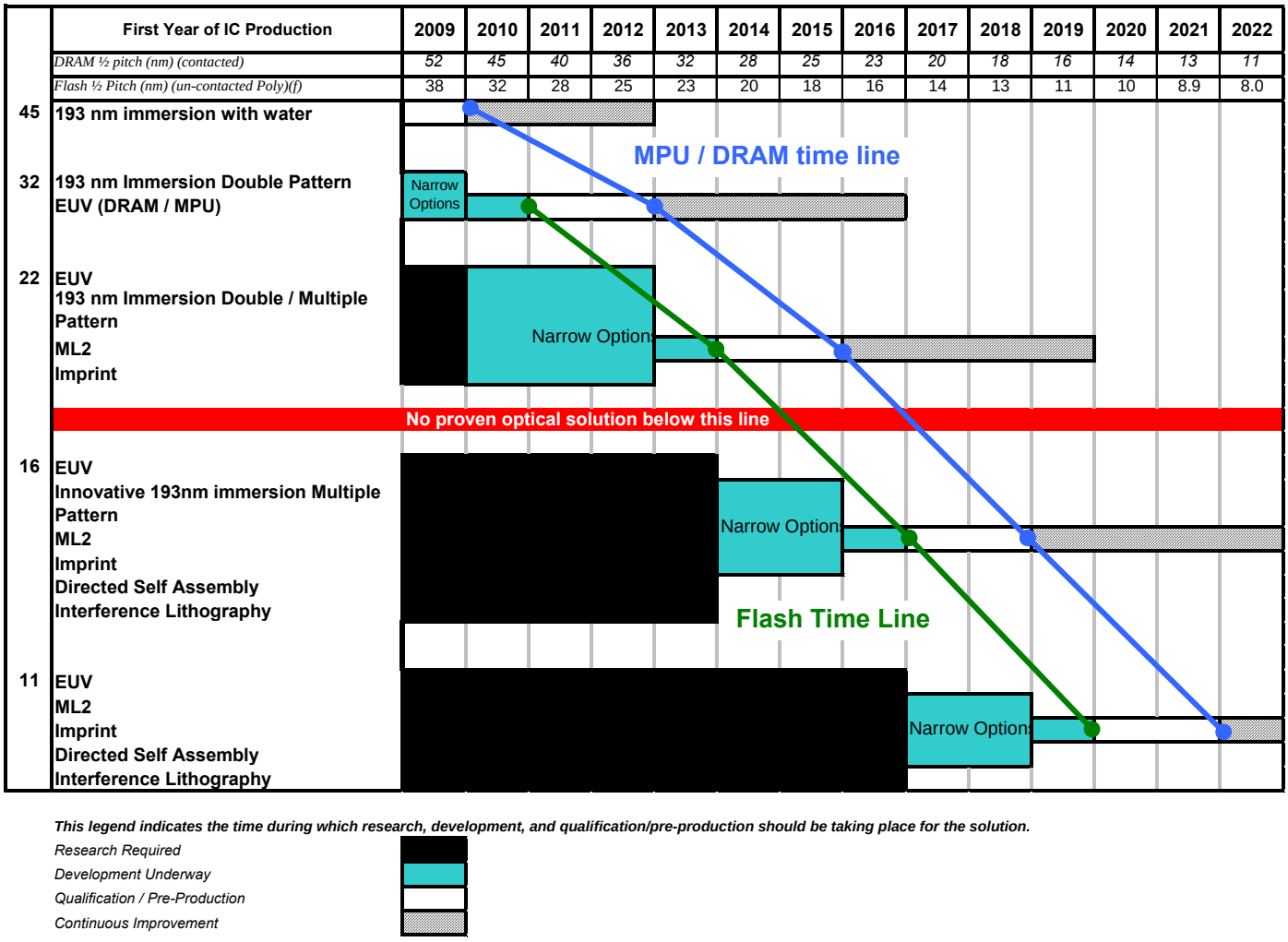

Figure LITH3 Lithography Exposure Tool Potential Solutions

CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions involving Lithography, *ESH*, *Factory Integration*, *Yield Enhancement*, *Metrology*, *Modeling and Simulation*, device and circuit performance, and *Emerging Research Devices* and *Emerging Research Materials* are outlined in this section.

ENVIRONMENT, SAFETY, AND HEALTH

Recent discussion of the continued use of perfluoroalkyl sulfonates (PFAS) in photochemicals has shown that long and commonly used materials can have ESH issues that only now are being comprehended. The introduction of new technologies necessarily means the use of materials and chemicals whose health and environmental implications are even less well known. The efficiency of EUV sources also needs to be maximized to minimize the facility and power requirements to operate these sources at the power needed for high throughput EUV lithography. Specifically, the wall-plug efficiency of the sources needs to be increased to minimize the power to generate EUV photons and to cool the source components. Practices for using and disposing of the chemicals used in lithography must evolve with careful regard for the safety of workers and their environment. Refer to the *Environment, Safety, and Health* chapter for comprehensive information and for a link to a new chemical screening tool in the electronic chapter (*Chemical Restrictions Table*).

FACTORY INTEGRATION

To maintain adequate process control, advanced process control capabilities are essential in the lithography cluster in the wafer fab. These capabilities are becoming increasingly important in mask-making facilities as well. Leveraging the learning from the wafer factory automation experience will also be essential to mask making. Several mask shops have developed custom solutions for automating data handling for defect inspection and repair. Further opportunities for automation exist. Leveraging existing standards that are used today in wafer fabs, such as the adoption of SECS/GEM into the mask-making tool infrastructure, will help reduce manufacturing errors.

An accurate wafer tracking system across various process modules is required to identify the working flow of any wafer in process. Several integrated metrology modules able to evaluate one or more parameters—CD, litho stack thickness, target profile, overlay, macro inspection with automated defect classification, and wafer flatness—are also recommended. Track and stepper/scanner should be able to use data recorded by any kind of internal or external sensors to adjust processes. Other possible requirements, which may call for major upgrades of equipment software and in several cases even of related hardware, include simultaneously managing different module flows on tracks to accommodate optimal metrology sampling plans and accepting overrides to downloaded (or selected) recipe set points. Moreover, on any track module, being able to update all relevant set points wafer by wafer, even within the same lot, is desirable. On exposure tools, the software should allow the host to update dose, focus/tilt, and overlay input parameters wafer by wafer, even within the same lot or perhaps for each exposure field. Calibration, self-calibration, and matching activities on metrology modules should be allowed without a significant loss in litho cell throughput.

YIELD ENHANCEMENT

Yield enhancement is expected to become a major challenge as critical defect sizes become smaller than the limits of optical detection. Inspection systems are increasingly challenged to meet the required sensitivity and speed requirements. Non-optical methods of defect detection have not yet demonstrated the acquisition rates for controlling defects in semiconductor manufacturing on the entire wafer, but they are being used to control the lithographic hot spots and improve yield. Furthermore, die-to-database inspection of wafers is probably required for using ML2.

DFM practices are being used, but need to be developed further to minimize systematic sources of yield loss. Control of airborne molecular contamination (AMC) is also critical to maximize yield by minimizing local poisoning of resist and mitigating the formation of progressive defects on masks during exposure. See the *Yield Enhancement* chapter for quantitative AMC control requirements related to lithography. Mask handling practices to maintain EUV masks and imprint templates (without pellicles) free from defects remain a significant challenge.

METROLOGY

The rapid advancement of lithography technology and resultant decrease in feature dimensions continues to challenge wafer and mask metrology capability. The existing precision of CD measurement tools does not meet the somewhat relaxed 20% measurement precision-to-process tolerance metric for the most advanced technology generations. Precision includes measurement tool variation from short- and long-term tool variation as well as tool-to-tool matching. Wafer and mask CD technology is evolving to meet the need for 3D measurements. A key requirement is the measurement of line width roughness. Measurement precision for LWR must be better than line width precision. The quantitative effects of LWR on device performance need to be better understood to optimize metrology for LWR.

Overlay metrology is also challenged by future technology generations. Memory makers are requiring more stringent overlay control to achieve desired circuit yields. Traditional overlay test structures do not capture all possible overlay errors that can occur to phase shift and optical proximity correction masks. The expected usage of double exposure/double processing techniques will require even more accurate measurements to guarantee an adequate degree of alignment between the two masks composing the final layer layout.

The complete discussion of Lithography Metrology is in the Lithography Metrology and Microscopy sections of the *Metrology* chapter, which also includes lithography metrology technology requirements and potential solutions.

MODELING AND SIMULATION

Support from modeling and simulation is critical both to push the limits of traditional optical lithography and to assess new next generation lithography technologies. The application of simulation tools in lithography largely benefits from the well-known physical basis of Maxwell's equations that govern lithographic imaging. Applying these equations to model

lithographic imaging requires a problem-specific and efficient implementation in simulation tools. Furthermore, an intimate link between equipment-scale and feature-scale simulation is required for state-of-the-art lithography simulation. Equipment scale effects often require modeling with random variables with user-defined or user-measured probability distributions.

New techniques used in future next generation lithography techniques, such replacing lenses by multilayer mirrors and using reflecting masks for EUV lithography must be appropriately modeled and included in the simulation programs. Mask pattern generators and some ML2 options involve imaging with electrons. Simulations of stochastic space charge effects, geometrical aberrations, and electron optical lens design performance using either magnetic or electrostatic lens elements are needed. Support from simulation for narrowing the technology options has been and will continue to be important.

With the introduction of immersion lithography come several additional requirements for modeling and simulation. Optical systems with NA <1.35 must be simulated, which especially requires the appropriate treatment of polarized illumination and partial polarization by mask structures and materials. Simulation should also help to assess whether specific defects are due to bubbles in the immersion liquid.

A specific challenge for lithography modeling and simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as line edge roughness. Better calibration techniques are required to both develop models and to customize models in commercial tools to appropriately describe the photoresists in question. Calibration obviously depends on the quality of input data, for example, CD measurements. Therefore, measurement errors must be better understood and estimated. Systematic errors should be dealt with by models of the measurement tools, such as CD-SEMs. With the growing importance of LWR and LER, lithography simulation needs to help assess their influence on device and interconnect performance (LER) and variability (LWR). Since the roughness of etched structures and not the resist pattern ultimately affects device performance, intimate coupling between resist and etching simulation is indispensable. Intimate links with etching simulation must also be established to predict the geometry of non-ideal mask edges that frequently result from mask-making lithography steps.

Besides models of image formation and resist profile generation, mechanical models are also critical for designing lithography tools. Refinement and application of finite element methods is important for assuring exposure tools, masks, and wafers remain stable enough to meet demanding overlay tolerances. Equilibrium and non-equilibrium models of thermal effects are also essential for designing exposure tools, especially for modeling the heating of the immersion fluid and its effect on distortion and aberrations. Models of fluid flow for immersion have also been essential in designing fluid delivery systems that minimize immersion-specific defect formation. See the *Modeling and Simulation* chapter for details on developments needed to satisfy these requirements.

INTER-FOCUS ITWG DISCUSSION

Gate CD and line width roughness control capability impacts devices (Refer to the 2009 ITRS chapters for *Process Integration, Devices, and Structures (PIDS*), *Front-End Processes (FEP), Metrology*, and *Design*. Depending upon the level of CD control that is possible, requirements will impact other processes that affect transistor performance, such as implant, diffusion, and etch. Tight CD control will require metrology that can support the control requirements. Design will need to take into account the collective capabilities of all processes that affect transistor performance. The Design TWG simulated circuit delay and power variability as a function of the most significant process and device variables. The simulations indicated that increasing the CD control requirement to ± 12% would result in a tolerable variation of circuit delay and power variation given the variations of all the significant parameters affecting these circuit attributes.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES AND MATERIALS

Emerging devices are expected to impact lithography in at least three areas. First, several devices need critical layer patterning over non-planar substrates, which will require lithographic solutions that can provide tight CD control over the topography. For example, bilayer resists represent a possible solution to this problem. Greater depth of focus may become a compelling advantage for certain lithographic technologies. Second, emerging devices and materials could provide relief in controlling gate CDs. This will impact all aspects of lithographic technology, including masks, resists, exposure tools, and metrology. Another potential area for cross-cut studies is the development of “litho-friendly” materials, such as “directed self-assembly” molecules.

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