INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

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YIELD ENHANCEMENT

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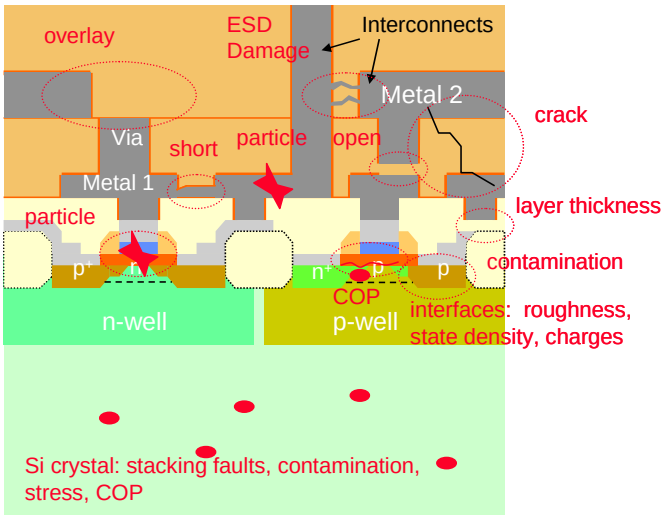
YIELD ENHANCEMENT

SCOPE

Yield in most industries has been defined as the number of products that can be sold divided by the number of products that can be potentially made. In the semiconductor industry, yield is represented by the functionality and reliability of integrated circuits produced on the wafer surfaces. The scope of this chapter is limited to the yield of front end processing. The YE chapter does not discuss manufacture line yield, assembly/packaging yield, and final test yield. Yield Enhancement (YE) for manufacturing of integrated devices addresses the improvement from research and development yield to mature yield. The YE chapter displays the current and future requirements for high yielding manufacturing of DRAM, MPU, and Flash. Furthermore, it has the objective to identify the red brick wall for manufacturing, and to discuss potential solutions.



During the manufacturing of integrated circuits yield loss is caused for example by defects, faults, process variations, and design. During processes as implantation, etching, deposition, planarization, cleaning, lithography, etc. failures responsible for yield loss are observed. Several examples of contaminations and mechanisms responsible for yield loss are listed in the following: a) Airborne Molecular Contamination (AMC) or particles of organic or inorganic matter caused by the environment or by the tools; b) process induced defects as scratches, cracks, and particles, overlay faults, and stress; c) process variations resulting, e.g., in differing doping profiles or layer thicknesses; d) the deviation from design, due to pattern transfer from the mask to the wafer, results in deviations and variations of layout and critical dimensions; and e) diffusion of atoms through layers and in the semiconductor bulk material.

The determination of defects and yield, and an appropriate yield to defect correlation are essential for yield enhancement. This correlation is of major importance, because not all defects change device properties or cause failure of devices or integrated circuits. Therefore, the yield enhancement chapter addresses not only the identification of tolerable contamination limits for processes and media, but also the tolerable budgets for particulate contamination of tools. The specification of tools for defect detection and classification of defects for root cause analysis addresses the technology requirements for detection and characterization of faults and failures.

The YE chapter has three focus topics: 'Yield Model and Defect Budget', 'Defect Detection and Characterization', and 'Wafer Environment Contamination Control'. These three topics crosscut front end process technology, interconnect processes, lithography, metrology, design, process integration, test, and facility infrastructures. Yield learning is discussed without identification of the red brick wall for manufacturing or potential solutions.

Yield Model and Defect Budget—Yield model has been developed for the purpose of predicting the yield of products and providing information how to improve them. Historically, yield has been limited by extra and missing materials generated in the fabrication environment, and showed good correlation with defect density of the wafer. Defect budget have had a role of breaking down the targeted yield into the targeted control limit of every process module in the fabrication line. However, current most serious yield issue has been changed from said physical defect to insufficient compensation or

countermeasure for manufacturability at the design stage. General consensus or agreements of modeling abovementioned issue have not been established yet.

Defect Detection and Characterization—Physical device dimensions and corresponding defect dimensions continue shrinking, posing new challenges to detection and tolerable contamination. The wafer edges were identified to show significant impact on yield as well as process variations and design. Development of defect detection, defect review, and classification technologies showing highest sensitivity at high throughput is crucial for cost efficient manufacturing. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and work-in-progress data, will have to be developed to enhance root cause analysis and therefore enable rapid yield learning.

Wafer Environment Contamination Control—Order-of-magnitude improvements in process critical fluid and gas impurity levels are not considered to be necessary in the foreseeable future. New materials and their precursors, however, introduce challenges that require continuous study. Clarification of potential contamination from point-of-supply to point-of-process will define control systems necessary for delivered purity. There are several locations in the pathway from the original delivery package, i.e., the Point of Supply (POS) of a liquid or gas to the location where that material contacts the wafer, i.e., the Point of Process (POP), for ascertaining purity. This has led to a considerable amount of confusion and ambiguity in discussing the quality of process fluids, including the data found in Table YE7. Table YE1 summarizes the major fluid handling and/or measurement nodes found along the typical systems supplying process fluid. This table is an effort to create a common language for the discussion of attributes and requirements at these different node points. Further information regarding pathway nodes can be found in the supplementary materials and references, such as the Semiconductor Equipment and Materials International (SEMI) Standards.

Table YE1 Definitions for the Different Interface Points

	POS *Delivery Point of Gas/Chemical Supplier*	*POD* *Outlet of Central Facility System*	*POC* *Submain or VMB/VMP Take off Valve*	*POE* *Entry to Equipment or Sub Equipment*	*POU* *Entry to the Process Chamber*	*POP* *Contact with Wafer*
Interfaces	*SEMI Standards Focus Area*	*ITRS Factory Integration Facilities Group Focus Area*		*ITRS Factory Integration Equipment Group Focus Area*		*ITRS Front End Processes, Lithography, Interconnect TWG Focus Area*
Ultrapure water	Raw water	Outlet of final filtration in UPW plant	Outlet of submain take off valve	Inlet of wet bench or subequipment	Inlet of wet bench bath, spray nozzle, or connection point to piping, which is also used for other chemicals	Wafer in production
Process chemicals	Chemical drum/tote/bulk supply	Outlet of final filtration of chemical distribution unit	Outlet of VMB valve	Inlet of wet bench or intermediate tank	Inlet of wet bench bath or spray nozzle	Wafer in production
Specialty gases	Gas cylinder or bulk specialty gas systems	Outlet of final filtration of gas cabinet	Outlet of VMB valve	Inlet of equipment	Inlet of chamber (outlet of MFC)	Wafer in production
Bulk gases	Bulk gas delivered on site or gas generator	Outlet of final filtration/purification	Outlet of submain take off valve or VMB valve	Inlet of equipment/ subequipment	Inlet of chamber (outlet of MFC)	Wafer in production
Cleanroom and AMC	Outside air	Outlet of make-up air handling unit	Outlet of filters in cleanroom ceiling	Inlet to mini-environment or sub equipment for AMC, outlet of the tool filter for particles	Gas/air in vicinity to wafer/substrate	Wafer/substrate in production (AMC/ SMC)

POD—point of delivery POC—point of connection POE—point of entry POU—point of use VMB— valve manifold box VMP— valve manifold post UPW—ultra pure water MFC—mass flow controller AMC—airborne molecular contamination SMC—surface molecular contamination

DIFFICULT CHALLENGES

The difficult challenges for the Yield Enhancement chapter are summarized in Table YE2. Currently, the most important key challenge will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high through put. Furthermore, it is a dare to identify but yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority the requirement for 3D inspection was identified. This necessitates for inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects,

and sub-surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases. E-beam inspection seems not to be the solution for all those tasks any more.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- Process Stability vs. Absolute Contamination Level
- Wafer Edge and Bevel Monitoring and Contamination Control

In 2009 a new long term key challenge was identified. This is the introduction of 450 mm wafers which is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450 mm wafers requires a new generation of inspection tools. The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 450 mm wafer size. Therefore, the tool costs are crucial. 450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review. Due to the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates. Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

Furthermore, in the long term the following key challenges are identified:

- Non-Visual Defects and Process Variations
- In - line Defect Characterization and Analysis
- Development of model-based design-manufacturing interface

Table YE2 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection of Multiple Killer Defects / Signal to Noise Ratio - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	*Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity.* *Reduction of inspection costs and increase of throughput is crucial in view of CoO.* *Detection of line edge roughness due to process variation.* *Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision.* *Reduction of background noise from detection units and samples to improve the sensitivity of systems.* *Improvement of signal to noise ratio to delineate defect from process variation.* *Where does process variation stop and defect start?*
3D Inspection – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.	*Detection of non visible defects e.g., voids, embedded defects, and sub surface defects in the structures.* *The demand for high-speed and cost-effective inspection is crucial.* *Large number of contacts and vias per wafer* *E-beam inspection seems not to be the solution for all those tasks any more.* *Sensitivity of the inspection tool to process variation and definition of maximum process variation (control limits).*
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	*Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product* *Relative importance of different contaminants to wafer yield.* *Define a standard test for yield/parametric effect.*
Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.	*Currently, the monitoring and contamination control methods require intensive development.*
Difficult Challenges < 16 nm	*Summary of Issues*
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	*Systematic Mechanism Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to:* *a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows.* *b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge.* *c) Logic diagnosis runs time per die.* *d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model.* *Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.*
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	*Data volume + quality: strong increase of data volume due to miniaturization* *The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution.* *It will be recommended to supply information on chemical state and bonding especially of organics.* *Small volume technique adapted to the scales of technology generations.* *Capability to distinguish between the particle and the substrate signal.*
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	*A lot of models should be operated at the design stage. For example, Optical Proximity Correction, Well Proximity, Stress Proximity, CMP and so on* *The Amount of models seems to be rapidly increasing.* *Not only accuracy of models, but also optimization of trade-off between models might be requested.* *Development of test structures for new technology generations*
The introduction of 450 mm wafers is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450 mm wafers requires a new generation of inspection tools.	*The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 450 mm wafer size. Therefore, the tool costs are crucial.* *450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review.* *Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important.* *Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.*

YIELD LEARNING

INTRODUCTION

Yield learning is defined as the collection and application of process and wafer knowledge to improve device yield through the identification and resolution of systematic and random manufacturing events. Currently, yield learning is not described by technology requirements and potential solutions.

The semiconductor industry operates in an environment of exponentially decaying product prices, which put semiconductor manufacturers under time-to-market pressure. Profitability is derived from an early and successful yield ramp. The sooner a semiconductor manufacturer generates high yield, the earlier the manufacturer ramps to volume production, and the more profitable the semiconductor manufacturer's integrated circuit venture is likely to be. Improving the systematic component of yield, which frequently constrains yield in the early stages of manufacturing, can enhance profitability by enabling production at a point in time when chip prices are very high. Yield learning in the early stages of manufacturing may thus differ significantly from yield learning in the later stages of manufacturing. Beside this, any transition from one technology generation to the next is accompanied by a decrease in initial yield. Along with a technology generation change, for example, new materials or litho processes have to be introduced. These changes have to be implemented in parallel with new technology generations. Monitoring capabilities, inspection, metrology to properly cover the issues of latest technology generations cause enormous expenses and require concentrated research and development.

The key requirements for achieving highly sophisticated yield ramps include the detection of ever-shrinking, yield-detracting defects of interest, timely identification of root causes with growing data volume, chip complexity, process complexity, and improving the yield learning rate per each cycle of learning. With increasing process complexity and longer cycle times, tools and methods are needed to increase the number of yield learning cycles for each technology generation. Also, with continuous move to smaller features and longer processes, larger wafers, and new materials, numerous tools and methods are required to understand the entire yield detracting interactions.

DATA MANAGEMENT AND ADVANCED PROCESS CONTROL AND FAULT DETECTION AND CLASSIFICATION (FDC)

Yield Management in a factory is going to be more closely coupled to data management. The rapid identification of defect and fault sources through integrated data management is the essence of rapid yield learning. Learning must proceed at an accelerated rate to maintain the yield ramp from introduction to maturity within the expected timeline, despite the growth in circuit complexity and the larger amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. This is getting significant importance now and in the future. In advanced manufacturing, any data generated could potentially hold the key to understanding and solving a yield issue that is identified at wafer sort, and needs to be recorded in an accessible way for the yield engineers, if required. Accessing the raw data in such a way as to generate meaningful correlations and results, is going to be a critical requirement for manufacturing. Data storage, and consequently the user interfaces to access this data, cannot be handled as an afterthought, if these factories are to be successful during the start up.

How the data from all generating sources of the factory is collected, stored, compiled, and accessed, is going to be crucial. In the face of this increased complexity, strategies and software methods for integrated data management have been identified as critical for maintaining productivity. Integrated device manufacturing must comprehend integrated circuit design, visible and non-visual defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the integrated device manufacturing system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. Integrated device manufacturing will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as Automatic Defect Classification (ADC) and Spatial Signature Analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information.

Implemented Advanced Process Control (APC) and Fault Detection and Classification (FDC) solutions will be of increasing importance. However, these control solutions will require tremendous data transport and data processing systems to support a full-scale implementation. Managing this, which must all be done in real time to benefit the factory, is a monumental undertaking. Maintaining standards, and open access systems allowing the best internal and external solutions to work together, is a must.

Down stream, or rather offline analysis of all the factories' data will also require new approaches, in addition to the existing ones, to fully grasp all information that can be correlated to yield. The greatest challenge to a comprehensive data management system required for yield learning is the ability to deal with and integrate data streams that are continuous, periodic, sporadic, and interval-based so they can all be linked through some common coupling system or user interface and be resolved by engineers. Keeping data aligned down to the wafer level or possibly to the die level, requires automated data matching techniques. It is also critical to have all data sources open and accessible by multiple user interfaces in order to maximize the effectiveness of yield engineering resources in finding problems. The best-of-breed data systems going forward will allow internal as well as multiple third party software solutions and Graphical User Interfaces (GUIs) to access the raw data formats, giving engineers the greatest flexibility in identifying and solving yield limiting issues. Barriers such as these must be eliminated.

The current practice in Data Management System (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient integrated device manufacturing is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect and fault sourcing capabilities, methods must be established for integrating workflow information (WIP) such as data determined with the DMS, particularly in commercial DMS systems. This will be important when addressing issues of advanced process and tool control beyond simple tool shutdown, e.g., lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time based data generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time based data that can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

FOUNDRY SPECIFIC YIELD LEARNING

Yield learning in a foundry differs substantially from yield learning in a fabrication facility that produces a few high-volume products. The high-volume producer will be constrained by batch yield in the early stages of manufacturing. Line yield will be the limiting factor once batch yield is high and volume production has begun. By contrast, a foundry may introduce a plethora of low-volume products into a relatively mature process on a routine basis. On occasion, one lot of wafers may provide a lifetime inventory of a particular design, which sells into a very short market window. A few chips of the design must exit the fabrication facility by a specific date. Due to this it is more important to get a initially defect free design of the integrated circuit, to get a initially flawless masks; and to obtain immediately a rapid cycle time through the line combined with a high line yield instead of a high batch yield.

DEFECTS

The various types of defects are described in the following.

Visible Defects—Tools are needed to detect, review, classify, analyze, and source continuously shrinking visible defects.

Non-visual Defects—Defects that cause electrical failure, but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-visual defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance or timing; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-visual defects) will become increasingly challenging. Techniques need to be developed that rapidly isolate failures and partition them into those caused by visible defects, non-visual defects, and parametric issues.

Parametric Defects—As minimum feature size decreases, so does the systematic mechanism limited yield (SMLY or Y_s). A major contributor to the Y_s component of yield is parametric variation within a wafer and wafer-to-wafer. Parametric

defects have traditionally been referred to as 'non-visual defects'. However, parametric defects require separation from the "non-visual defects" for rapid sourcing.

Electrical Faults—As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the pattern number of a wafer times the number of process steps, forming a defect sourcing complexity factor. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity. Moreover, the soft failures caused by sporadic cross-chip timing variation will require innovative new approaches to identify the root causes since these type of failures reside between a hard spot defect failure and consistent systematic failure issue.

NEEDED RESEARCH

The technology requirements and potential solutions described in 2007 call for continued cooperation between all stakeholders. For example, tool defect data is needed from semiconductor manufacturers and equipment manufacturers to specify design processes and the required equipment. A challenge for the future will be the detection of smallest defects at high throughput. Currently, there are no solutions known. This situation is also observed for control of critical dimensions with respect to the expected scaling down progress. As e-beam inspection is too slow, the development of scatterometry or other optical methodologies seems more promising. Furthermore, the future transition of metrology tools to inspection tools has to be performed as the yield issues get more and more complex related to the small feature sizes at atomic scale. 2007 the importance of flatness control of surfaces was recognized during cross technical working group discussions. The problem is solved for bare wafer inspection but not for pattern wafer inspection. Enormous R&D efforts are required to obtain solutions for the above mentioned red brick wall within the next years.

In order to maintain manufacturing costs while improving yield, contamination control must focus on impact at the point of process. Innovative ideas, such as local removal of undesirable contamination from a re-usable process gas or fluid, must be examined. For new thin-film materials, understanding of purity requirements for deposition chemicals is needed.

Performance analysis indicates replacements for SEM/EDX that are also activated by e-beam illumination. Auger-electron spectroscopy can be used in the short-term to augment and replace SEM/EDX analysis because Auger-electron generation can only escape a target particle from a depth of approximately 3 nm or less. This property of Auger electrons specifically avoids a large sampling volume.

In the next two to three years, SEM/EDX can be further improved by more versatile e-beam acceleration control and X-ray detection methods. More sensitive detection methods include micro-calorimetry and WDS.

For elemental and bonding analysis of particles that are 60 nm diameter and below, Scanning Transmission Electron Microscopy (STEM) / Electron Energy Loss Spectroscopy (EELS) holds good promise for performance in the next 3 to 5 years. STEM/EELS has the capabilities to simultaneously capture elemental analysis while imaging the atomic structure of the constituents of a particle. Automated sample preparation must be improved and accelerated to achieve timely ultra-thin samples of 50-100 nm thickness. Aberrations of incoming and transmitted e-beams must be mitigated to enable the identification of constituent elements and compounds by the sizing of these constituents from images alone.

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

The overall die yield of an IC process can be described as a product of material-defect limited yield (Y_M), systematic mechanism limited yield (SMLY - Y_S) and random-defect limited yield (Y_R) (see Equation 1). Y_M separates yield degradation caused by defects embedded in a starting material from Y_S and/or Y_R during wafer fabrication. Further information about Y_M is described in FEP chapter. In most cases, Y_M is negligible. Y_S requires problem specific modeling and general formula to describe Y_S is currently unknown. A negative binomial yield model is adopted to calculate Y_R in YE chapter. A is the area of the device, D_0 is the electrical fault density, and α is the cluster factor. Parameters required to calculate D_0 are defined in Table YE3.

$$Y_{Die} = Y_M * Y_S * Y_R = Y_M * Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha} \quad (1)$$

$$PWP_n = PWP_{n-1} \times \frac{F_n}{F_{n-1} \left(\frac{S_{n-1}}{S_n} \right)^2} \quad (2)$$

The previously published tables for defect budgets (YE4 and YE5 in ITRS 2007) were deleted because of the lack of accuracy supported by surveys among semiconductor manufacturers. Although based on results of old studies (1997, 1999, and 2000) of Particles per Wafer Pass (PWP) levels at SEMATECH member companies, they are still useful as a reference for investigating defect reduction target toward new technology generation or discussing difference between several specific processes. In the Equation 2, PWP is the particles per wafer pass defect density per square meter, F is the average faults per mask level (determined by the random electrical fault density (D_0) divided by number of masks at a given technology generation), S is the minimum critical defect size, and n refers to the technology generation.

Table YE3 states the yield and the product maturity assumptions that were used in calculating electrical fault density values and PWP defect budget target values for MPUs /DRAMs/Flashs, respectively. These assumptions for the most part are as defined in the 2009 *Overall Roadmap Technology Characteristics* (ORTC). Cluster parameter value of 2 permits slight non-uniformity of fault distribution on wafers. The electrical fault density that is used to calculate faults per mask level is based on only the periphery (logic/decoder) area of the chip. This periphery area can be calculated from cell array area at production defined in *Table ORTC-2A*. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM/Flash can implement redundancy to attain the overall yield target of 85%.

Besides continuous improvement in tool cleanliness, there are at least three other major challenges that must be addressed going forward in order to achieve acceptable yields:

1. The issues of particles and defects which are located not only at the front surface of a wafer but also at wafer bevel/edge portion and backside surface needs to be addressed.
2. With Systematic Mechanisms Limited Yield (SMLY) dominating the rate of yield learning, a concerted effort is required to understand, model, and eliminate SMLY detractors.
3. New methodology including APC should be evaluated the possibility of becoming a new variation/defect source.

Table YE3 Defect Budget Technology Requirement Assumptions

Product	*MPU*	*DRAM*	*Flash*
Yield Ramp Phase	*Volume Production*	*Volume Production*	*Volume Production*
$Y_{OVERALL}$	75%	85%	85%
Y_{RANDOM}	83%	89.50%	89.50%
$Y_{SYSTEMATIC}$	90%	95%	95%
$Y_{MATERIAL}$	>99%	>99%	>99%
Chip Size	$140mm^2$	$93mm^2$	144
Cluster Parameter	2	2	2

DEFECT DETECTION AND CHARACTERIZATION

The ability to detect in-line yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production-process research and development, yield ramp, and volume production — broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabrication facilities begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the integrated device manufacturers just in time for each phase of the process cycle. Tools that meet the requirements for process research and development are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate yield ramp must be available several months before production begins. Finally, the ability to monitor excursions at a technology generation is needed when the product hits high yield levels.

Technology requirements are presented by three tables covering the needs for: a) patterned wafer - and e-beam inspection; b) unpatterned wafer inspection, macro and bevel inspection and defect review; and c) Defect Review and Automated Defect Classification (ADC). The complexity of processes and integration schemes for manufacturing of integrated devices requires intense defect inspection for process and tool monitoring. Unpatterned wafer inspection is extensively used for tool qualification. Both defect inspections use subsequent defect review for root cause analysis, posing challenging requirements to the accuracy of defect coordinates. Furthermore, the cleanliness of inspection tools is of increasing importance. Due to the observed impact of defects on wafer bevel and edge on yield, backside and bevel wafer inspection needs a defect review possibility in order to be used to the full extent. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is inspected on e-beam tools which find their application also in detection of small defects.

One of the major challenges is to get to the defect of interest. Therefore, the signal-to-noise ratio is an important criterion for all inspection tools. The more nuisance defects are captured the less valuable the results are as defects of interest might not be recognized even after intense review. Furthermore, an efficient separation of DOI from noise will enable an increased throughput of the subsequent review.

The inspection of bevel, apex, and wafer edge on the top and bottom on multilayer product wafers is nowadays possible with a variety of tools. Anyway the variety of process problems having their origin in those areas of the wafer requires defect classification which is challenging for any inspection tool. Important criteria, besides coverage of all areas, sensitivity, and speed, are the ADC and the optical review capability on the tool as well as a standard result file allowing SEM review.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside inspection requirements are based on the Lithography chapter technology requirements table, and also ask for specification of tool cleanliness of the inspection tools themselves, this was introduced

Several other defect modes need to be addressed by detection tools. A better understanding of non-visible killers, defects that can not be detected with conventional optical technologies, is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected.

Many have electrically significant impact to device performance and can occur in both the front end of the process (process steps prior to contact oxide deposition) and the back end of the process. Macro defects impacting large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved matching the wafer throughput (plus overhead of the inspection) of the lithography, and possibly CMP, systems at every technology generation.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The cost of the investment, fab space occupied, and the throughput of defect detection tools are major contributors to their cost of ownership (CoC). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput, the sensitivity, as well as the use of adaptive recipe options of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table YE4, YE5, and YE6 have been stipulated on the basis of detecting accurately sized PolyStyrene Latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pits pattern flaws, surface roughness, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

Table YE4 Defect Inspection on Pattern Wafer Technology Requirements

Table YE5 Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements

Table YE6 Defect Review and Automated Defect Classification Technology Requirements

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table YE7.

Wafer environment control—The wafer environment control includes the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in PODs/FOUPs. As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to effective wafer and reticle isolation deployment.

Airborne molecular contamination—Outgassing from materials of construction in the cleanroom, wafer processing equipment, and wafer environmental enclosures as well as fugitive emissions from chemicals used in wafer processing are the two main sources of AMC. Oxygen and water vapor as well as low concentration atmospheric contaminants (e.g., CO) can also be considered as part of the AMC burden. Acid vapors in the air have been linked with the release of boron from HEPA filters and the impact of amines on Deep UltraViolet (DUV) photoresists are well known examples of AMC affecting wafer processing. The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation in the cleanroom to measure AMC at the part per trillion level (by volume). Surface Acoustic Wave (SAW) devices and Atmospheric Pressure Ionized Mass Spectroscopy (APIMS) have been used to measure low level AMC, but low cost, routine monitoring may be

required as devices approach molecular dimensions, see also *AMC monitoring programs*. Hydrocarbon films of only a few monolayers may lead to loss of process control, especially for front-end processes. Although numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures, the need for nitrogen purging of wafer environment enclosures is being investigated for critical process steps. Not all process steps will be impacted by AMC. For example, future lithography systems will require vacuum processing and are not expected to impose new AMC control requirements in the cleanroom environment. The potential for AMC to impact new processes should be considered in all process integration studies. A detailed definition of critical impurities is provided in *AMC definitions*.

Temperature and humidity specifications have been added to Table YE7 this year for the most critical applications, e.g., lithography for several reasons.

1) The strictest requirements are driven by the lithography process, which is protected by an environmental chamber. The specifications in the Table YE7 reflect the inlet condition to each individual environmental chamber. Here especially, the maximum variation over time is important, which the environmental chamber must be able to compensate. At the POP lower specifications down to ± 0.03° K are maintained.

2) But also in the coater/developer track temperature and humidity specifications must be guaranteed to maintain stable conditions for the resist.

3) The temperature variation is also important for the stepper itself, since minor temperature variations can result due to different thermal extension coefficients in misalignments between the stepper foundation/wafer stage and the lens column. Steppers need up to a week to stabilize after a temperature change.

4) Another critical requirement is driven by metrology equipment which depend either on laser beams (the air density depend on temperature and humidity) and by measurements where misalignments are important.

The temperature and humidity stability over different locations within critical areas is less important. Also in other areas temperature and humidity variations shall be controlled to less strict limits since it may have an impact on the surface (native oxide formation) or alignments. Some companies choose not to have different specifications for critical and non-critical areas to allow flexibility in the cleanroom use as well as simplify the temperature and humidity control and the associated segregation.

These specifications are variational specifications and set points can be chosen in a wide range. A recent benchmarking study between fabs has shown values between 19.5 and 24°C for temperature and values between 35% and 48% for the relative humidity. There are different drivers for that. The temperature set point is normally chosen based on comfort level and climatic conditions and the resulting energy consumption. The set point for relative humidity takes into consideration higher electrostatic charges at lower humidity and higher corrosion/native oxide formation at higher relative humidity. Capacity of AMC filters also depends on the humidity.

Another process area with temperature/humidity control as well as AMC control requirements is the location of the lithography excimer lasers, if they are installed in the subfab and not in the main cleanroom.

Process critical materials—Additional experimental investigation is required to support our understanding of impurity specifications in novel materials, such as Cu plating solutions, CMP slurries, or chemical vapor deposition (CVD) precursors to high/low-κ dielectrics and other thin film materials. For many years the critical particle size concept was used to judge whether particles will have an impact on yield or not. This concept has to be rethought since particles do not impact the process yield alone by their physical size but also by their chemical composition. The allowable particle concentration thereby depend also on product parameters such as cell size and have therefore been aligned with the particle concentration on the surface as derived by the FEP surface preparation group calculation model.

Ultrapure water—UPW is generally considered to be 18.2 MegΩ-cm resistivity at 25°C, low ppt in metals, less than 50 ppt in inorganic anions and ammonia, less than 0.2 ppb in organic anions, and below 1 PPB total oxidizable carbon (TOC) and silica (dissolved and colloidal). Particle levels are reduced using the best available ultrafiltration technology. Bacteria are present, on surfaces and to a lesser degree in the bulk fluid, and controlled to very low levels, typically <1 colony forming unit (cfu)/L in the bulk fluid. The 2007 Roadmap values, presented in Table YE7, represent typical UPW quality currently in use to manufacture the most advanced semiconductor devices and have been validated by benchmark surveys. More stringent criteria beyond 2007 are only projected where there is evidence that manufacturing process requirements demand improvements. UPW is generally the cleanest fluid available in the manufacturing process. As such there is not much data to suggest that it is has a significant negative impact on process yields. For this reason the UPW Roadmap is relatively stable over time. The UPW group is evaluating Gibbs Free Energy deposition models to

indicate the potential for critical elements to deposit on the wafer under various process conditions. *A discussion of the UPW requirements can be found in the UPW supplemental material online.*

The UPW section of Table YE7 considers some parameters as process variables rather than contaminants. It is clear that the stability of the wafer environment can be as important as the level of contaminants present for some parameters. Some semiconductor manufactures now treat Dissolved Oxygen (DO) in this way, while others still consider it a contaminant Stability of temperature and pressure continue to be important, the former being critically important for immersion lithography.

Contaminant quality levels in UPW must be viewed in the context of where that quality is required and where it is to be measured. Points of measurement are referred to as the POD, POE, and POU. The POD is just after the last treatment step of the UPW system, the POE is at the tool connection point, and the POU is in the tool. Refer to Table YE1 for detailed description of sample locations. The 2007 Roadmap defines UPW quality at the POE in Table YE7. UPW quality can change between these three locations, especially between the POE and POU, and requires particular attention to maintain quality throughout. In addition sampling techniques are critical to ensure accurate analytical results. As UPW specifications shift from the POE to the POU, sampling methods will become more difficult and costly. Most benchmark data has been collected at POD or POE and is the basis for parameters in Table YE7. A benchmark of POE and POU values was conducted in 2007 however results were not received in time for publishing. These results will be considered for the 2008 update. Where contaminant levels have been extended to POU this has been done based on engineering judgment assuming the semiconductor processing tool is well designed and operated with regard to maintaining fluid purity in accordance with applicable SEMI standards.

Ozonated UPW is not addressed in this Roadmap as it is considered a dilute process chemistry that is generally applied at the process tool. At the time of printing immersion lithography posed no special requirements for UPW other than possible degasification and additional closer temperature control, which would be done at the process tool.

Immersion Lithography processes which use UPW as the lens fluid is very sensitive to temperature and hazing of the lens. Tool manufacturers are interested in minimizing all potential sources of organics. Accelerated hazing tests are being conducted to see if the organic species known and thought to be in UPW can contribute to lens hazing. Results were not available at the time of printing but will be considered in the 2008 update.

UPW recycle—To promote resource optimization UPW use efficiency improvements are typically required. Cost effective technologies, including treatment and analytical methods, are needed to ensure UPW quality is maintained, as more water is recycled back through the system. A well-implemented recycle program has been shown to improve final water quality by using a "cleaner" stream for the feed, in addition to providing other benefits. Further information and requirements can be found in the *Environmental, Safety, and Health* chapter.

UPW measurement methodologies—General test methodologies for monitoring contaminants in UPW are indicated in the Figure YE1 below. Over the past few years the ITRS UPW team has benchmarked many advanced UPW systems to determine water quality. The 2007 benchmark effort includes Non Volatile Residue Monitoring and particles by SEM with a novel sample collection method. Past benchmark efforts have identified the inadequacy of some measurement methodologies to quantify contaminants in UPW. The following analytical methods are not sensitive to present levels of contamination in UPW: resistivity, total oxidizable carbon, inorganic anions, and organic ions, as well as some organic species. Speciation of organics has been limited by these methods. Sensitivity of the following methods is presently adequate: viable bacteria, dissolved gasses, and metals. While particle measurement is generally not adequately sensitive at the critical dimension it may be technically sound to extrapolate particle size and concentration data to the critical dimension. Benchmarking has shown this size distribution to be unique to a particular UPW system and/or measurement technique. Each user of the Roadmap is advised to determine a particle distribution for their fab empirically. Benchmarking has indicated a log: log distribution relationship with slopes from -1 to -5. A more complete treatment of *UPW concerns* is covered in the supplemental material of this chapter online, where also a *conversion tool* can be found.

Parameter	*Measured (POD/POC)*	*Test Method*
Resistivity	*Online*	*Electric cell*
Viable bacteria	*Lab*	*Incubation*
TOC	*Online*	*Conductivity/CO_2*
Inorganic anions and NH_4+	*Lab*	*Ion chromatography*
Organic ions	*Lab*	*Ion chromatography*
Other organics	*Lab*	*Various, e.g., ES TOF, ICP-MS*
Reactive silica	*Online or lab*	*Colorimetric*
Dissolved N_2	*Online*	*Electric cell*
Total silica	*Lab*	*ICP-MS or GFAAS*
Particle monitoring	*Online*	*Light scatter*
Particle count	*Lab*	*SEM—capture filter at various pore sizes*
Cations, anions, metals	*Lab*	*Ion chromatography, ICP-MS*
Dissolved O_2	*Online*	*Electric cell*

ES TOF—Electro spray time of flight ICP-MS—inductively coupled plasma mass spectrometry
GFAAS—graphite furnace atomic absorption spectrometry

Figure YE1 General Test Methodology for Ultrapure Water

UPW and liquid chemicals particle measurement—Problem Definition and Goals: The sensitivity limit of particle counters for UPW and liquid chemicals has not kept pace with decreases in the critical particle size (the size of particles which are thought to be detrimental to wafer yield). Although this concept needs to be discussed again since particles not only impact yield because of their physical dimensions, but even more by the chemical composition, e.g., as spot Fe contamination, the fact remains the same. It is important to measure even smaller particles than we can do today. Measurements of these nanoparticles are made difficult by the low scattering efficiency of them. Low particle concentrations and small sample volumes of current particle monitors can result in large sample-to-sample variability. More sensitive particle measurement methodology with adequate measurement statistics is needed to meet projected purity goals.

The Sensitivity Problem: As of 2007, the highest sensitivity particles counter commercially available for UPW is 0.05 microns and for liquid chemicals is 0.065 microns. Experiments have shown that small particles may even deposit preferentially [M. Knotter] and therefore the impact is increased even further. Past improvements in particle counter sensitivity for UPW have been accomplished by increases in laser power. While improvements in sensitivity for liquid chemical particle counters are viable, further sensitivity improvements for UPW using this approach are unlikely, due to the significant cost implications. In addition, high-cost solutions do not necessarily guarantee a production-worthy metrology tool. High initial expense coupled with increased cost of ownership impact the viability of higher sensitivity instruments. To estimate the concentration of smaller particles currently an extrapolation assumes a $1/d^3$ relationship between particle counts and particle size in liquids. The further away the particle size of interest gets from actual measurement capabilities, the higher the potential for error-error being defined as the difference in the projected value to the true value. Therefore, it is still important for the industry to develop a more sensitive method that can measure particle concentrations at greater sensitivity to validate the particle count versus particle size relationship so that the relationship can continue to be reliably used.

The Measurement Precision Problem: Statistical process control is increasingly being used to monitor the consistency of process parameters. Process variation of fluid purity can be as critical to wafer yield as the absolute purity of the fluids. Therefore, it is important that measurement methods detect sufficient number of events to ensure confidence in measured particle concentrations. Development of other statistically significant particle counting methods or a higher sample volume particle counter is needed to improve confidence in reported particle counts. The sample volume (volume of fluid measured) will determine the number of particle counts that are detected during the sample interval. *Refer to Supplemental Information link Particle monitoring for more detail.*

Although the gas/liquid chemical section of Table YE7 shows an essentially flat purity trend, there is likelihood that specific process steps may require higher purity. Yield improvements may be achieved more by reducing variations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control of contamination levels during manufacturing and delivery of these process materials.

Overview for gases and liquid chemicals— The recommended contaminant values for gases and chemicals in Table YE7 represent typical gas/liquid chemical quality requirements at the point of entry to the process tool (POE) for the more demanding manufacturing processes in the roadmap. In many applications, the requirements for the contaminants in these gases and/or liquid chemicals may be relaxed as dictated by the specific process requirements. On the other hand, some manufacturers have claimed benefits from lower contaminant levels. Considering that a given process can be run successfully within a “window” defined by a range of material purity and also by ranges in other parameters (purging time, etc.), it follows that, in practice, trade-offs exist between imposed purity requirements, process throughput, etc. Pushing a process to the upper limit of its “purity window” may require significant investment of time and effort in optimizing other parameters, and the economics of pursuing that effort will depend on the environment. It may also be that benefits attributed to low contaminant levels are more attributable to the reduction in contaminant variations achieved with high-purity process gases and chemicals. This topic is addressed in more detail below regarding the push for the adoption of statistical process control, SPC, for specifying process fluid purity.

There are three primary sources of process environment contamination: One is the impurities in the process materials as supplied. The second is the delivery system or the process itself. The third is decomposition, which may be caused thermally or by reaction with adventitious contaminants e.g., moisture. These contamination sources are found throughout the pathway from the delivered gas or chemical to the wafer surface. Table YE1 describes the several interfacial points of process materials with equipment found along these paths and associates them with the various TWGs within the ITRS and other organizations such as SEMI that focuses on them. This helps to clarify the relationship of these organizations with the WECC while also removing ambiguity about the definition of various points along the process path.

While purity measurements at the Point of Process, POP (that is, in the processing chamber itself), would provide the most direct correlation between gas or liquid quality and process performance, these measurements are often very difficult

to obtain with the exception of certain fluid properties in wafer immersion baths. Examples include both particulate generation during plasma processes and wafer outgassing. The latter is the most important source of water vapor contamination in many processes, often obscuring moisture contributions from the process fluid. Measurements at the POU provide the most direct information of the quality of process fluids going directly into the process chamber, but these are also not available for many of the common processes.

Because of these difficulties, the values in Table YE7 are intended to represent those at the Point of Entry, POE, defined as the inlet to the process tool as described in Table YE1. There are sufficient measurement data on bulk gases and aqueous fluids to provide guidance with regard to POE impurity levels for many applications, although measurements on these fluids are often performed at the POS, POD, or POC. For these materials, which are relatively unreactive and delivered in large volume, the extrapolation to POE is generally very reasonable. In the case of Specialty Gases and other reactive process fluids, such extrapolation is more delicate because delivered volumes are smaller, increasing sensitivity to contamination effects, and degradation in the distribution system related to materials of construction, atmospheric contamination, thermal degradation, etc. is more likely. These factors are minimized with normal best construction and operations practices, and therefore the best guidance available is often regarding POS specification and to a lesser extent POD or POC measurements, which are interpreted as equivalent to POE. In summary, while the intention is to recommend POE purity levels for all gases and liquids, in practice, the supporting data has more often been collected at POS, POD, or POC.

The targeted levels can be reached either by bulk delivery of a fluid with requisite purity or through use of a local purification/filtration. Care should be taken, at a minimum, to maintain the quality of the gas coming from the source, ensuring that contamination is not added downstream of the POS, as may occur due to particle generation at components, moisture out gassing, byproduct generation due to incompatible materials, etc. Particle filtration as close to the POU as possible is generally advisable for gases. For the most critical applications a local purifier may be used to enhance or ensure ultimate purity at the POU. In those cases, the prevailing approach is to seek POC levels that are adequate for the process and to view the purifier as "insurance." The challenge to the purifier is minimal, and long purifier lifetimes can normally be expected.

Specific purity challenges will be discussed below, but generally there is little objective evidence to suggest that the purity levels listed in Table YE7 are not suitable for multiple generations of semiconductor manufacturing. Yield improvements are expected to be achieved by reducing variations in purity. Statistical process control (SPC) on incoming materials will reduce variation at the POS. Inconsistencies at the POU may remain due to variations in downstream contributions, e.g., when the flow in a distribution system is decreased, moisture contamination due to out gassing tends to increase. Elimination of these variations may require purification at the appropriate point (e.g., POU purification, POUP).

The major bulk gases are listed separately in Table YE7. The 2007 roadmap had indicated an increase in purity requirements post 45 nm. This type of improvement might be anticipated, based upon historical trends as design rules tightened, but there is again little objective evidence to support the need for improvements across the range of bulk gases. Informal poling of several large semiconductor manufacturing organizations suggests that an increase above current purity requirements for the majority of bulk gases is not necessary to meet post 45 nm design rule manufacturing. For very special applications where extraordinarily higher purities are critical, special purity grades or additional purification will be required. As exemplified above, downstream POUP might also be utilized as an additional means of removing variability in POS gases. Therefore, Table YE7 has been modified from 2005 to remove many of the step improvements scheduled for future manufacturing nodes except where specific information has been identified to justify the change.

The situation is similar for many of the Specialty Gases, although several additional categories of applications have been added to better identify needs for specific processes, e.g., etch, deposition, doping and laser applications. Like the Bulk gases, the values in Table YE7 have been left at current levels, unless an objective justification for increased purity can be identified. Although changes to the current table YE7 values for gases are small, the introduction of so many new materials and the process innovations required to meet future design rules, e.g., atomic layer deposition, will require close monitoring. *More details with regard to bulk and specialty gases are provided in the Gas supplemental documents.*

The 2005 roadmap identified the growing need for statistical process control for process gases and liquids. Several companies have begun requesting materials with specifications related to the statistical control of variability of the materials, but there are no standards accepted across the industry that define the SPC process. Currently there is a Semi sponsored task force, composed of representatives from the end user and supplier communities that is creating a common set of characteristics for defining "in control" specifications for gases and liquids.

The promise of providing "in control" process fluids is anticipated to improve process yields by either minimizing the overall variability of the manufacturing process or in simply reducing the likelihood of a process crash resulting from large variations in material quality that would still nominally have met a more standard specification.

An informal survey of several large semiconductor manufacturing companies on their implementation of statistical process control requirements for their bulk and specialty gas purchases indicates that SPC processes are already being applied to many of the materials utilized in manufacturing, or will be shortly. However, the criteria that form the basis of "in control" varies substantially. Survey responses suggest that customer expectation is that the application of process control for the preparation of POS materials will improve their semiconductor manufacturing process stability and are critical for high yield manufacturing. Initial implementation, will likely focus on specialty gases that exhibit the greatest potential for causing semiconductor process variability, e.g., anhydrous HCl but will be used on new and existing products for both memory and microprocessors.

Liquid chemicals—Table YE7 summarizes the purity requirements for liquid chemicals delivered to process tools. Pre-diffusion cleaning requirements drive the most aggressive impurity levels. Liquid particle level targets are shown to become purer each technology generation. These target values are derived from the purity requirements on a wafer as calculated by the FEP surface preparation group assuming a linear relationship between the concentration in the liquid and on the wafer. Particle counters currently are capable of measuring only to 65 nm for liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes, but this will be influenced by the level of filtration utilized. Another measurement challenge for several chemicals is the differentiation between particles and bubbles, which is currently not possible.

The ability to accurately analyze organic, anion, and cation contamination in process chemicals is becoming more critical to successful wafer processing. In the supplementary materials an *ion table* and a *mixing calculation* is provided which shows for which chemicals which ions are important and in which chemicals they could actually occur/have been observed. With the increased use of CMP and plating chemicals, there must be a better understanding of purity requirements for the delivered chemicals. Table YE7 contains information only for very few CVD/ALD precursors. The variety of layers and the respective contaminants is enormous. Therefore, a link to the *precursor table* is provided in the supplementary materials online. The precursor table provides information by application as to which precursors are potential candidates at different technology generations, and the nature of contamination that can be expected. A major challenge is the development of accelerated yield learning for critical processes that introduce new precursors that will only be used for one or two generations.

Bulk/specialty gases—There were only a few changes to the bulk gas purity requirements. The measurement of organic refractory components at <0.1 ppb is a detect ability challenge for both nitrogen and helium used in lithography applications. The roadmap indicates these areas as orange from 2007 to 2010 because this is at the limit of detection for current analytical methods.

In addition, changes were made to better delineate the need to control Ar as an impurity. The N_2 specification was changed to eliminate Ar as a critical impurity, although it was left in the O_2 specification. Even so, the 50 ppbv limit given in 2005 was raised to an Ar limit of <1000 ppbv. The ongoing requirement in O_2 derives from the potential for uncontrolled Ar impurities to impact plasma etching processes, although typical Ar specifications for O_2 used for etching is more consistent with the <1000 ppbv level.

For some processes, such as advanced lithography, very small quantities of "high molecular weight/high boiling point" (e.g., C_6-C_{30}) hydrocarbons are detrimental because of increased adherence to the exposed surfaces, and potential for photochemical degradation to leave non-volatile residues on lenses, masks, mirrors, etc. However, any organics, even ones with retention times less than C_6 are considered detrimental if they can result in refractory deposits. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities. In order to detect such species with ultimate sensitivity, it is necessary to directly detect the relevant species and calibrate the analyzer with the appropriate standard. The methods used are analogous to those for AMC, such as TD gas chromatography (GC)/mass spectroscopy (MS) (TD = thermal desorption) or TD GC/FID, or ion mobility spectroscopy (IMS). Even these approaches may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks. For methods using adsorbent traps, it is very important to determine the trap efficiency. Using APIMS to provide real time measurement of individual hydrocarbons is possible, in principle, but calibration is difficult, because larger hydrocarbons are collisionally dissociated in the ionization process.

A compromise approach that has gained some acceptance is to use TD GC/MS and sum all peaks corresponding to C6 and higher. The instrument is usually calibrated with a multi-component standard and results are reported "hexadecane".

While the quantization provided by this method is approximate, and some species may be overlooked, it does at least emphasize the heavier hydrocarbons while providing a straightforward calibration.

Applications for both O_2 and H_2 generally tolerate higher levels of N_2 contamination than other contaminants and the table reflects this observation. Requirements for critical clean dry air (CDA), lithography purge gases, and supercritical CO_2 supply are included. Whereas critical CDA may not always be conveniently or cheaply available, there is no technological barrier to its production. Analytical methods are usually the same as used for airborne molecular contamination in clean room air, such as bubbling through ultra pure water (for metals, sulfates, amines, etc.) or trapping on an adsorbent trap for organics. In each case, the sampler concentrates impurities so that requisite sensitivities are achieved when the sample is introduced to the analyzer (ICP-MS or ion chromatography for aqueous samples, GC-MS for desorption of organics). Such methods are time consuming by nature, and direct methods would be preferred if available. However, there is no apparent pressing need for real-time analysis. For SO_2 there are convenient on line methods, e.g., UV fluorescence.

For specialty gases, contaminant values in etchants, dopants, and deposition gases have been expanded in Table YE7 to reflect the increase number of different materials in use, and to better delineate the processes they are used for. Particulate contamination is omitted, since online monitoring of particle concentrations is not commonly practiced and the efficacy of POU particle filters is well established. Whereas there is evidence that the most demanding applications, such as low temperature epi and its cleaning gases, will continue to benefit from improvements in purity as deposition temperatures are lowered, this is expected to be reflected in wider use of the best available purity rather than substantial improvements of those levels.

Tighter control over the variation in purity in both bulk and specialty gases is anticipated to be more important than improvement in absolute purity levels. However, the often more chemically reactive specialty gases present a more formidal challenge for maintaining of POS purity levels throughout the delivery to the point of process. Selected specialty gases, e.g., HCl are also expected to be among the first targeted for statistical process control at the POS.

Novel materials—More detailed consideration of the impurity levels found in the growing number of novel materials used in processing will be increasingly important. Requisite purity levels for critical materials such as novel metal oxides, CMP slurries, low/high k dielectric materials, precursor materials (such as CVD and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied, and many of these materials have not been called out in Table YE7. An early attempt to start to catalogue and characterize the properties of the thin film precursors utilized in semiconductor processing is found in the supplementary material for this chapter. (provide link)

Deposition precursors for thin film materials are often sensitive to moisture, air and high temperatures. Control over the delivery process from the POS to the reaction chamber is critical to high yielding performance. The use of very high purity carrier and purge gases in these systems are often required to prevent decomposition that can contribute detrimental molecular and particulate impurities. Traditionally bulk purifiers were used in the bulk gas delivery systems to remove particles and other homogeneous chemical contaminations like oxygen, or moisture present in the supply gases. However, with the development and commercial availability of point-of-use (POU) purifiers, there is a strong interest from end users to utilize point-of-use (POU) purifiers particularly for specialty gases needed for critical process steps with very critical level of contamination control. These point-of-use purifiers (POU) are highly effective to remove chemical contaminants to extreme low level (~ ppt), easy to use, easy to replace, with low cost-of-ownership. The capability of placing those point-of-use (POU) purifiers very close to inlet of process chamber, assures least travel path (less contamination) for process gases after chemical purification and filtration.

Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements. Additional detail on the variety of thin film precursors under consideration can be found in Liquid Chemicals section of Table YE7 and the supplementary *precursor table*.

Table YE7 Technology Requirements for Wafer Environmental Contamination Control

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

Very small particles will request study of thermophoresis and/or Van Der Waals force to understand behavior in the near future. Currently yield society does not have enough experience about particles between molecular and optically visible particles. Research into precise yield model assisted by TCAD is becoming important because SMLY issues tend to restrict yield ramping rate and attainment level. Ever increasing NRE also requests understanding of SMLY and its effective implementation to product. Parametric limited yield issues including line edge roughness and design to process mismatch also tend to limit yield. This will require research into new characterization devices and statistical methods to organize measured data. Figure YE2 illustrates a few potential solutions that may help address the technology requirements for future yield modeling.

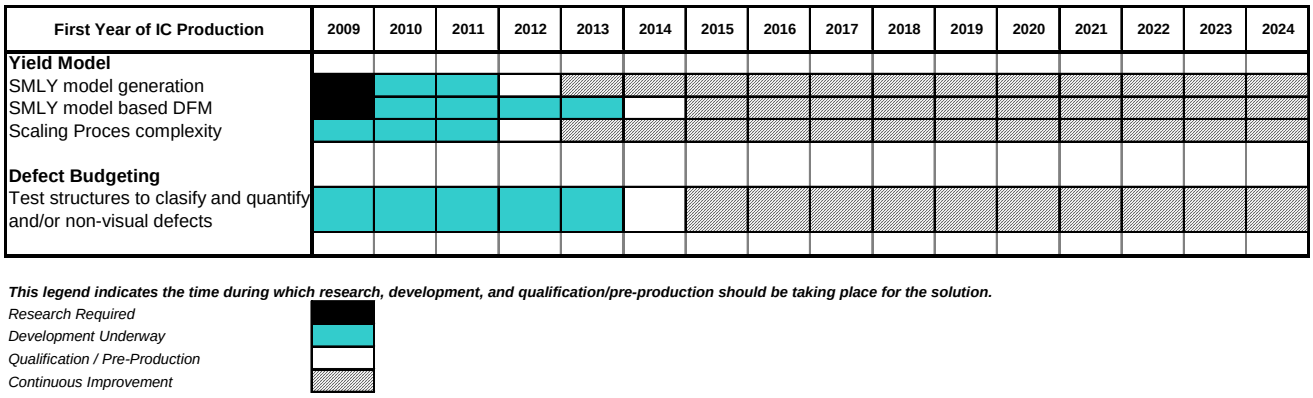


Figure YE2 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION AND CHARACTERIZATION

For pattern wafer inspection the requirements the next years will be to overcome issues of detection of the defects within the nuisance signal. This is correlated to the issue to obtain high sensitivity at high throughput. Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. Wafer edge/bevel inspection will require methods to filter and to classify defects. Really challenging is the review capability at the wafer edge. The review is the enabler for defect to yield correlation and therefore essential for high yielding production. The research and development should focus on methods to filter out the defects of interest automatically. The high aspect ratio inspection is still requiring for high yield at high throughput due to the high cost of ownership of the inspection tools. This requires also a good separation of the defect signals from the noise. The introduction of 450 mm substrates will start research activities in the area data quality and reduction of data amount. Also impacted and a need for research is the coordinate accuracy of inspection and subsequent review. As mentioned before this is essential for the yield improvement, especially required during ramp up. Due to the doubled surface area of the new substrates a research topic for the next years will be the throughput simulation and according improvement.

Figure YE3 Defect Detection and Characterization Potential Solutions

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and continue to enable cost-effective high volume manufacturing for device dimensions below 90 nm. Refer to Figure YE4. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Process critical materials—Figure YE4 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities.

In order to accelerate yield enhancement for processes that incorporate new materials, it is very desirable that development studies include purity data as much as is practical. Studies of new materials (e.g., for gate dielectrics) are initially concerned with basic process performance, and later with integration issues. During those stages of development contamination is a relatively minor concern. However, if no information is collected, later yield enhancement efforts proceed with inadequate technical basis. Collecting and reporting both environmental and material contamination data whenever practical will lead to long-term benefits.

UPW—UPW systems meeting specifications do not appear to be large defect drivers for current device geometries. Based on this the Roadmap does not predict that significant changes are required for future geometries. As a Roadmap priority, specific defect mechanisms related to UPW are required to drive significant changes. The current focus is to understand

the impact of the tool upon water quality, specifically particles, bacteria, and dissolved gasses, as well as to identify species that are suspected to be in UPW but are below the detection limit of available measurement methods. Improved measurement methodologies are required for organics, and organic ions to specify low-level contaminants in UPW. Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water.

Chemicals—Figure YE4 shows various technological areas that may be required to enhance and measure the purity of delivered chemicals to the wafer manufacturing process.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low outgassing, and non-absorbing materials development are key to effective wafer isolation deployment.

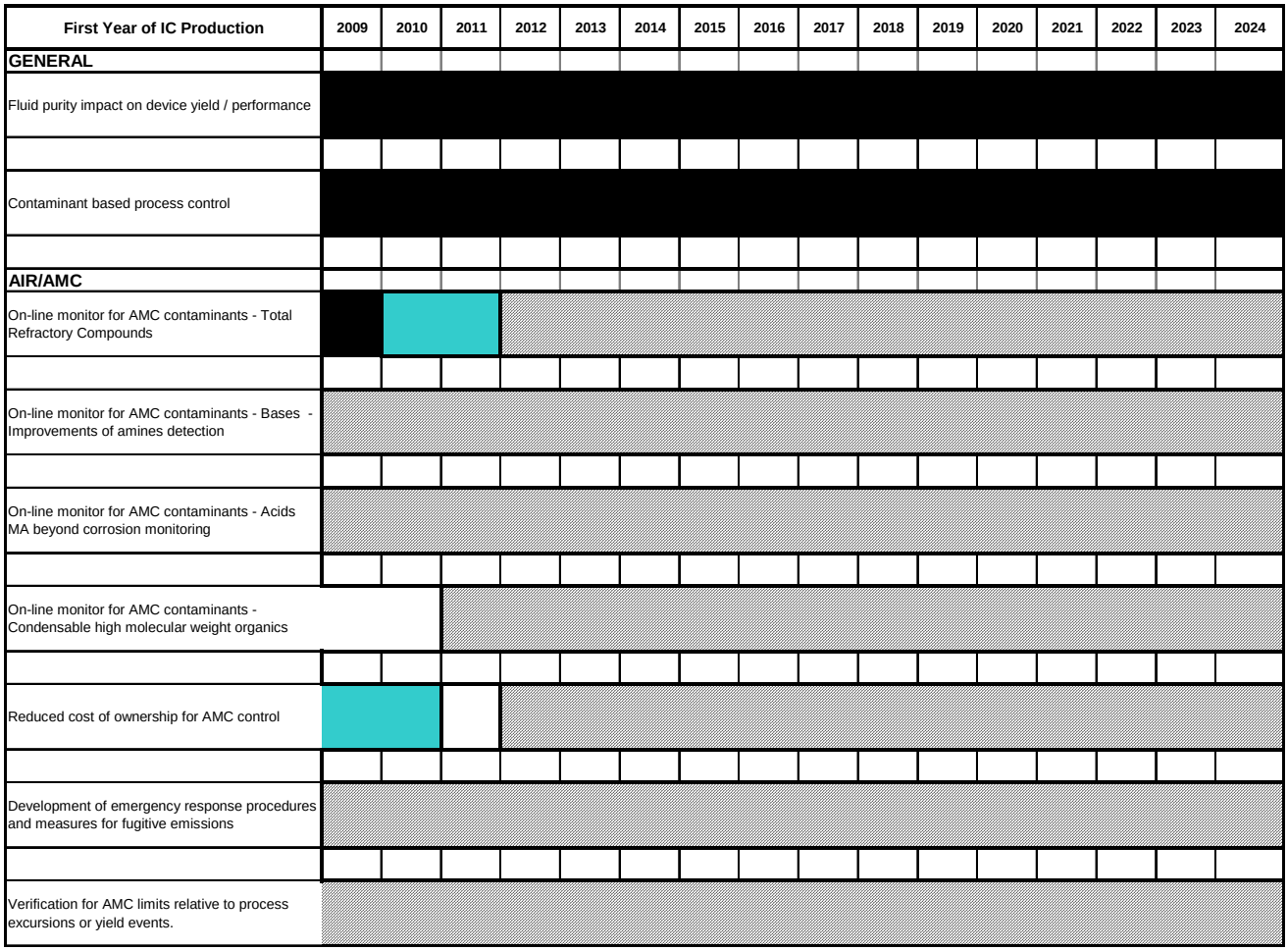


Figure YE4 Wafer Environmental and Contamination Control Potential Solutions

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
ULTRAPURE WATER																
Metal sampling/detection capability																
Metal deposition Understanding																
Tool blanketing to preclude dissolved O2 increase																
Particle counting techniques for direct measurement of smaller particles																
Colloidal Silica as a surrogate measure of particles in UPW																
Organics speciation and analytical capabilities to provide information about organic molecular weight and chemical species / class																
Yield impacts of various organic species																
TOC: analysis for chemical family and molecular weight identification																

Figure YE4 Wafer Environmental and Contamination Control Potential Solutions (continued)

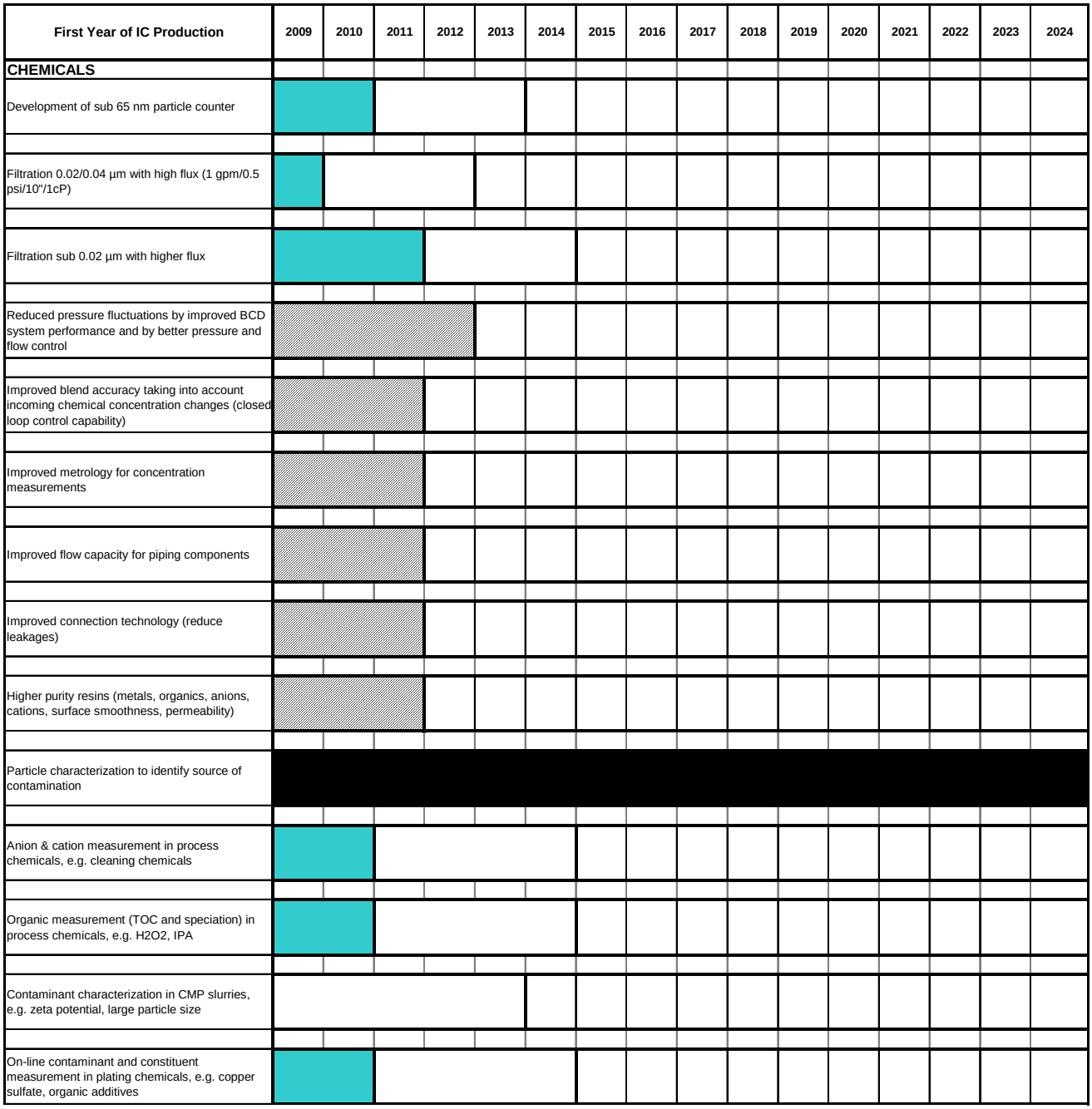


Figure YE4 Wafer Environmental and Contamination Control Potential Solutions (continued)

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
PRECURSORS																
Particle measurement for precursors																
Other analyzer techniques for precursors (precursor specific contaminants, see supplementary table)																
GASES																
Development of statistically process controlled (SPC) based specifications for critical specialty gases																
Bulk gas purity requirements, specifically of carrier and purge gases for moisture sensitive materials																
Blending accuracy for low concentrations of dopant mixtures																

Figure YE4 Wafer Environmental and Contamination Control Potential Solutions (continued)